Memory Circuits & Systems

Exercise 6
DRAM Differential Sense Amplifier

Professor Po-Tsang Huang

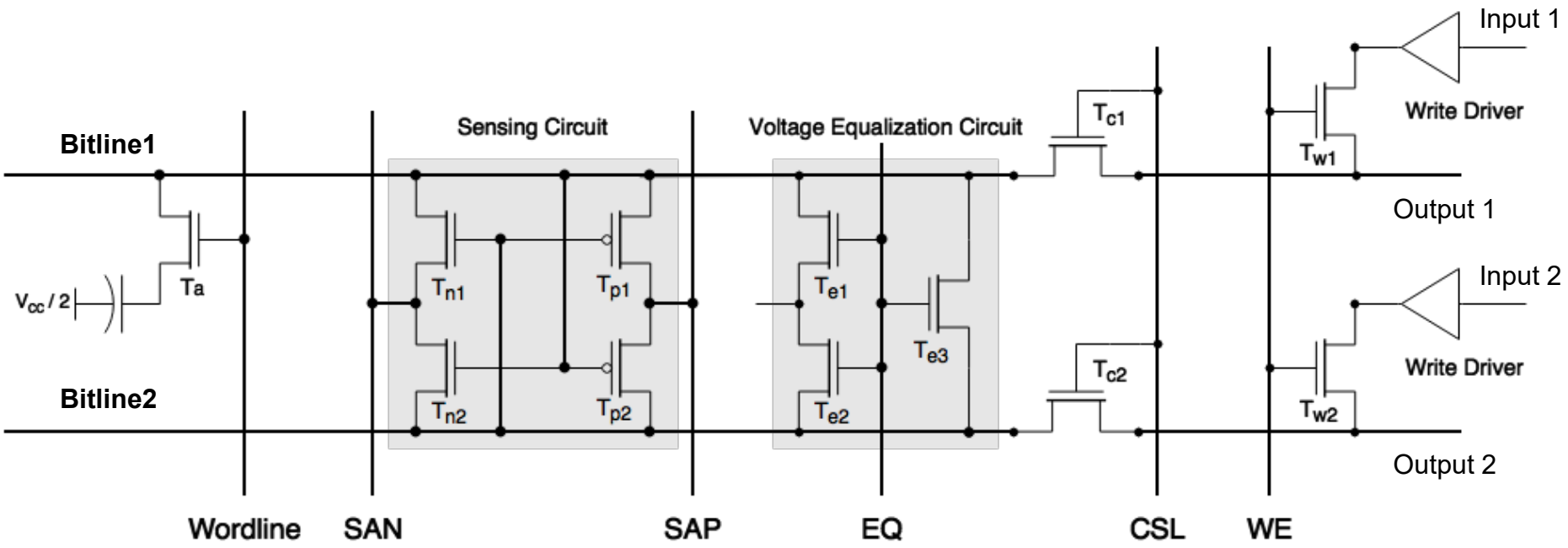
International College of Semiconductor Technology
National Yang Ming Chiao Tung University

DRAM Differential Sensing Amplifier

- Implementation Read & Write operation of DRAM using 7nm FinFET model (just for evaluation)
  - Input: WE, CSL, EQ, SAP, SAN, WL
  - Output: Output1 of Bitline1, Output2 of Bitline2
  - Design a differential sensing amplifier and simulate DRAM Behavior (1T1C cell, C = 20 fF)
  - Estimate loading of Bitline1 and Bitline2 (Add an extra C to emulate the parasitic C on BL)
    - $C_{(BL)}$: $C_{(C)}$ typically in the range 3 : 1 ~ 6 : 1
  - Please compare and analyze the relationship of loading of DRAM cell between Bitline1 and Bitline2

Differential SA Structure for DRAM

- Architecture of a differential SA for DRAM.



Read/Write mode of DRAM

- Read mode [32%]
  - Step1:Precharge
  - Step2: Access
  - Step3:Sense
  - Step4: Restore
- Write mode [40%]
  - Step1:Precharge
  - Step2: Access
  - Step3:Sense
  - Step4: Restore
  - Step5: Write Recovery
- Please compare and analyze the relationship of loading of DRAM cell between BL & BLB. [28%]

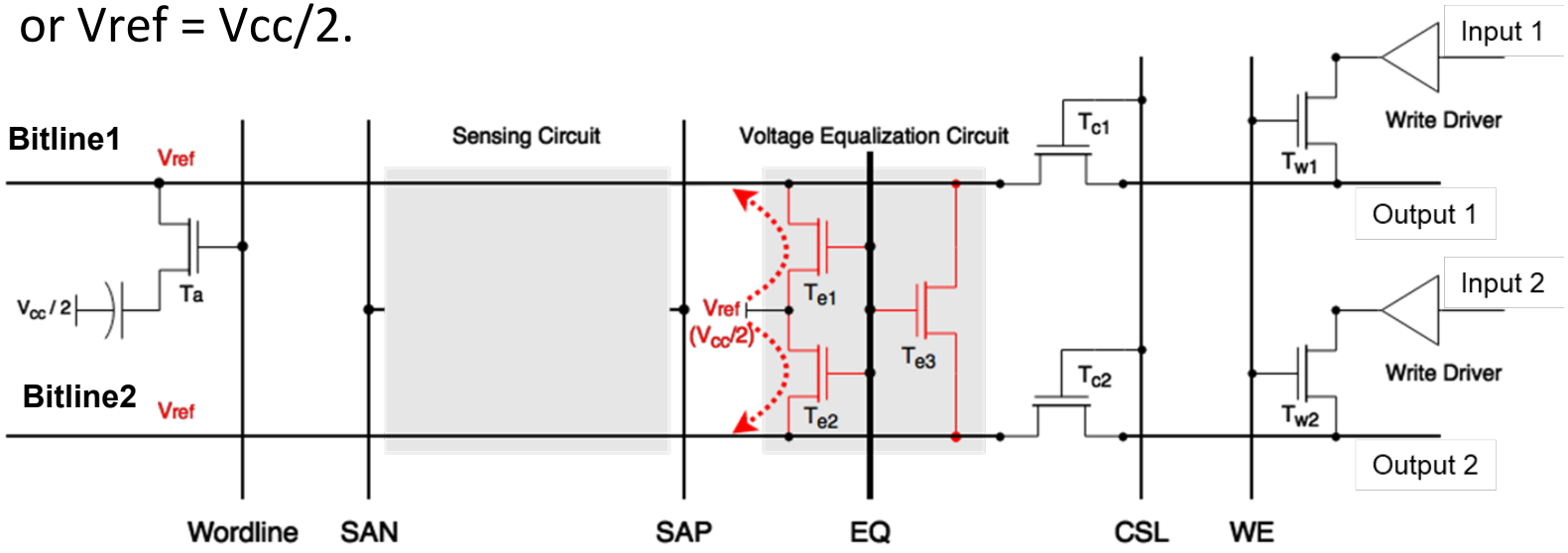
Submission on E3 platform

- Please compress your **report** & **source codes in a single compressed file (.zip/.rar)** and upload this single file on E3 platform
  - Source code
    - Hspice code of differential SA for DRAM
    - Input pattern (include read & write mode)
  - Report:
    - Waveform: should include the information of each step in Read/Write mode.
    - Comparison & analysis
  - Naming rules of the compressed file
  - Upload file: **Ex6_#ID.zip (including report & source code)**
- Due date: 6 /6 P.M. 23:55

Read mode of DRAM

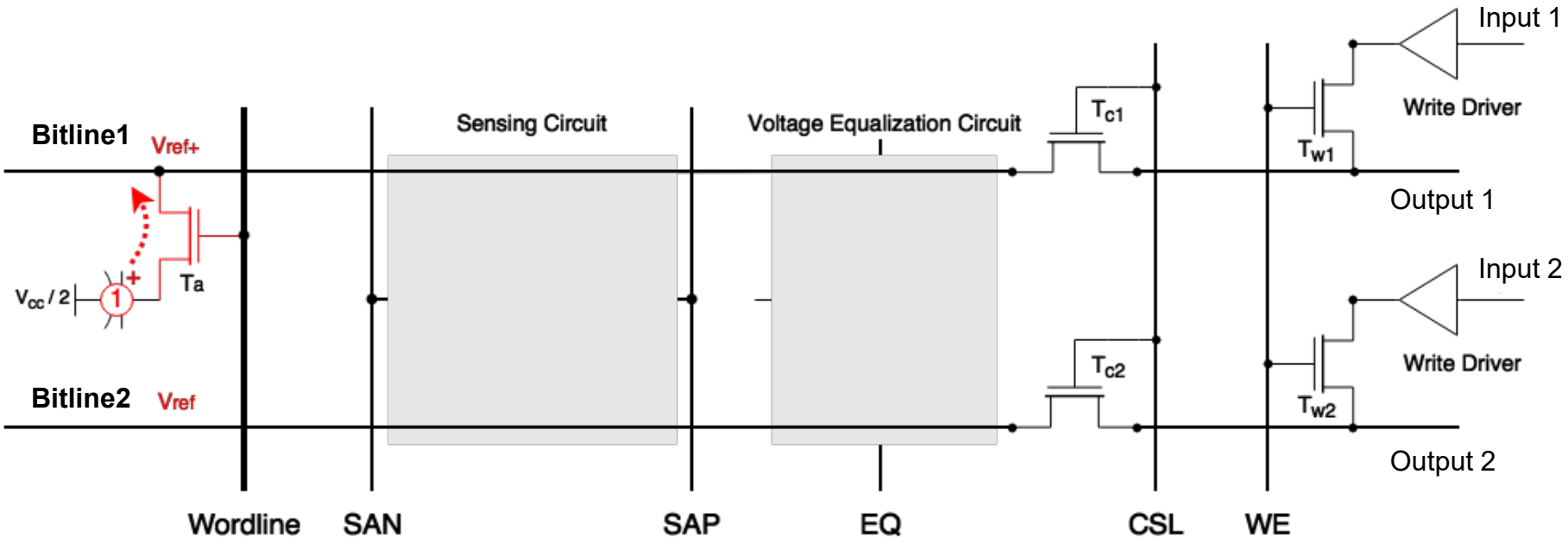
Step 1: Precharge

- **Controlling the EQ signal:** The EQ signal is a gate signal used to control the precharge transistors Te1, Te2, and Te3. When the EQ signal is high, these transistors turn on.
- **Te1, Te2, Te3 transistors turn on:** When the Te1, Te2, and Te3 transistors turn on, they form a path that connects the Bitline1 and Bitline2 to the power supply Vcc and the reference voltage Vref.
- **Bitline1 and Bitline2 voltages stabilize at Vref:** Due to the conduction of the Te1, Te2, and Te3 transistors, the charges on the Bitline1 and Bitline2 will flow until their voltages stabilize at Vref. Vref is typically half of Vcc, or Vref = Vcc/2.



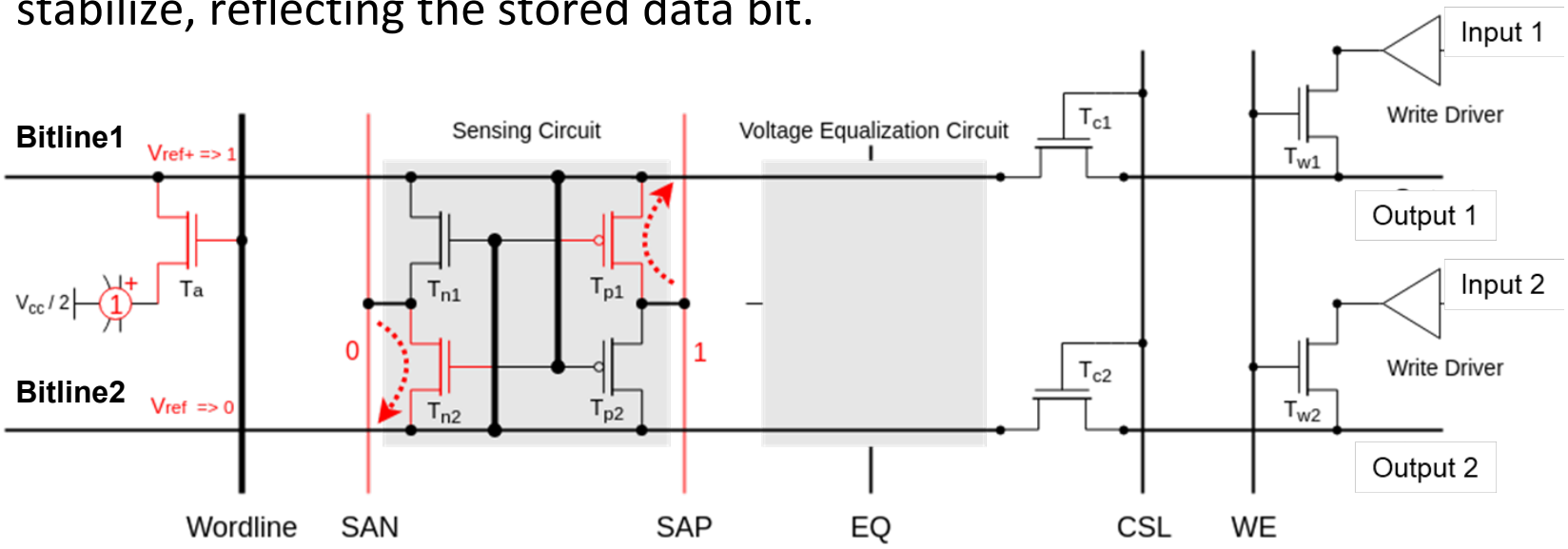
Read mode of DRAM

- Step2: Access
  - **Wordline signal:** The Wordline signal selects the storage cell for data write operation.
  - **Ta transistor:** The Ta transistor connects the Storage Capacitor to the Bitline1.
  - **Data write:** The stored positive charges in the Storage Capacitor flow to the Bitline1, raising its voltage to Vref+.



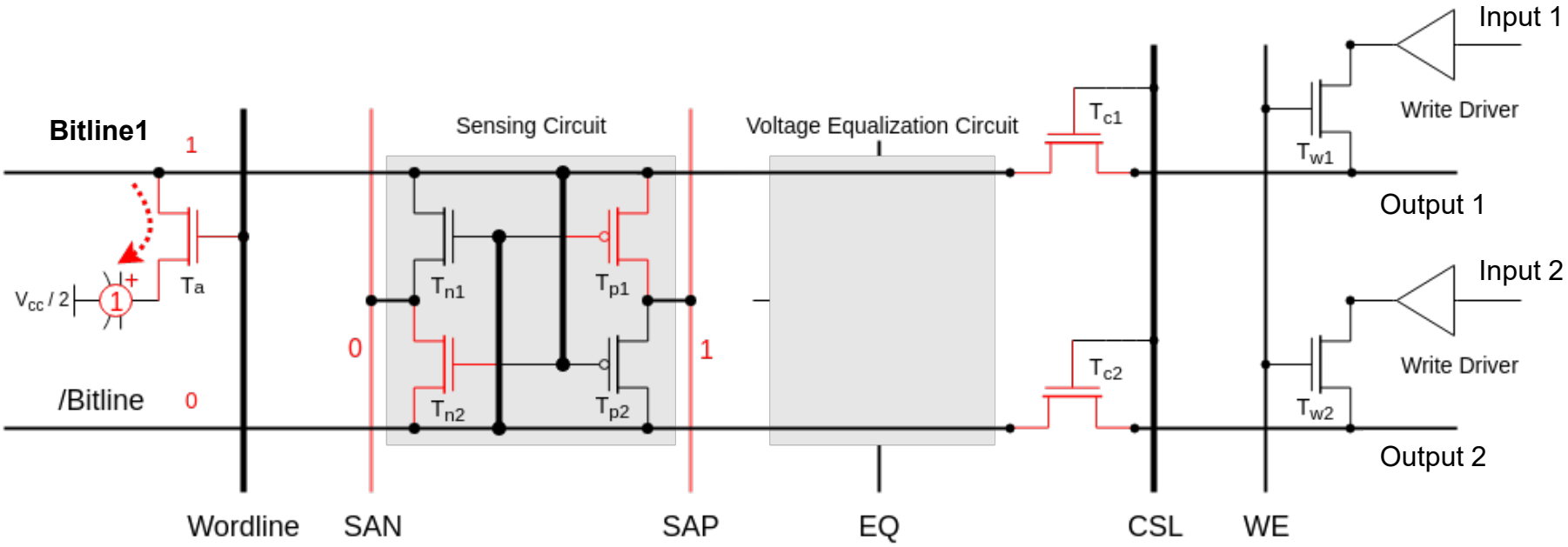
Read mode of DRAM

- Step3: Sense
  - **SAN and SAP voltages:** SAN (logic 0) and SAP (Vcc) control the sense amplifier.
  - **Tn2 stronger than Tn1, Tp1 stronger than Tp2:** Due to Access stage, Tn2 conducts more than Tn1, and Tp1 conducts more than Tp2.
  - **SAN pulls down Bitline2, SAP pulls up Bitline1:** SAN pulls down Bitline2 faster, and SAP pulls up Bitline1 faster.
  - **Tp1 and Tn2 on, Tp2 and Tn1 off:** Tp1 and Tn2 turn on, Tp2 and Tn1 turn off.
  - **Bitline1 and Bitline2 voltages stabilize:** Bitline1 and Bitline2 voltages stabilize, reflecting the stored data bit.



Read mode of DRAM

- Step4: Restore
  - **Bitline1 voltage stable:** Bitline1 voltage remains at Vcc after the Sense stage.
  - **Bitline1 charges Storage Capacitor:** Bitline1 charges the Storage Capacitor through Tp1.
  - **Storage Capacitor charge restored:** The Storage Capacitor's charge is restored to its pre-read state.



Write mode of DRAM

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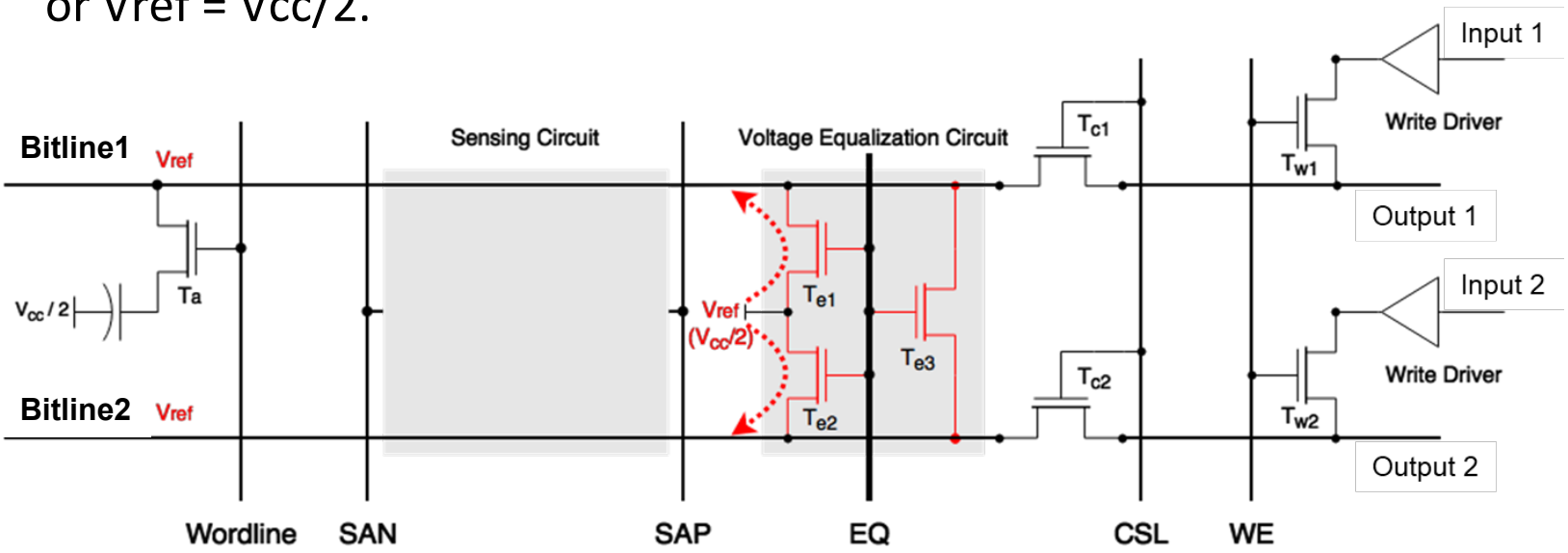

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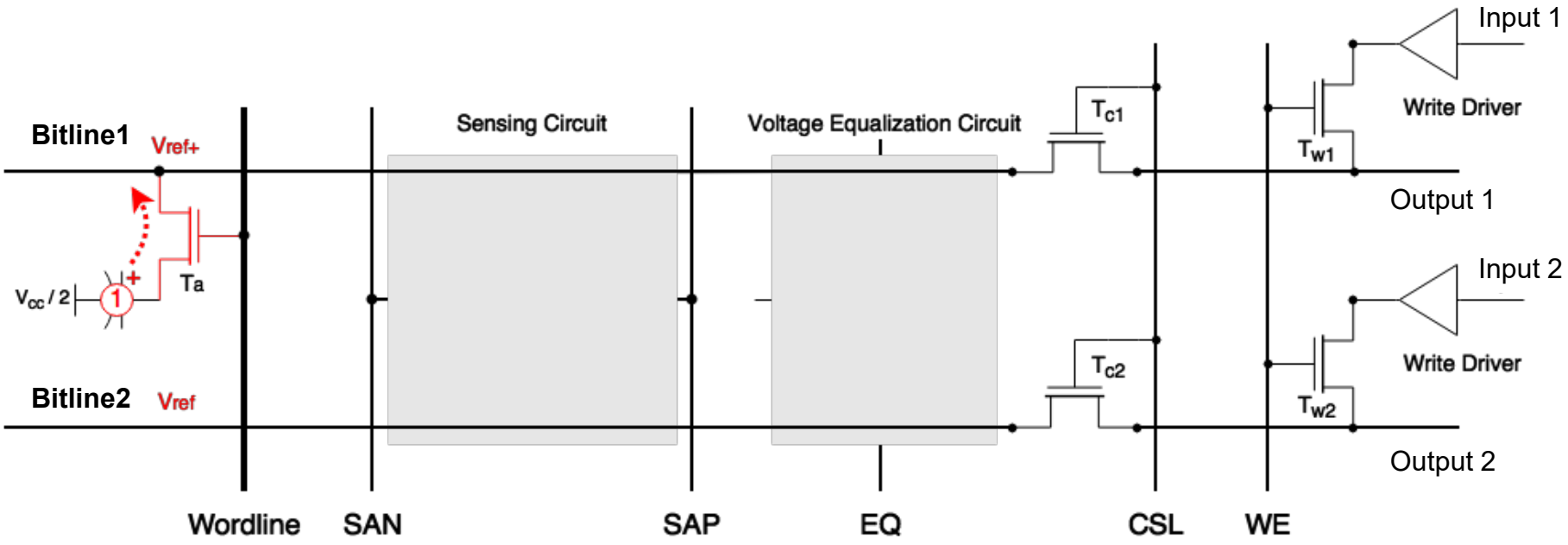

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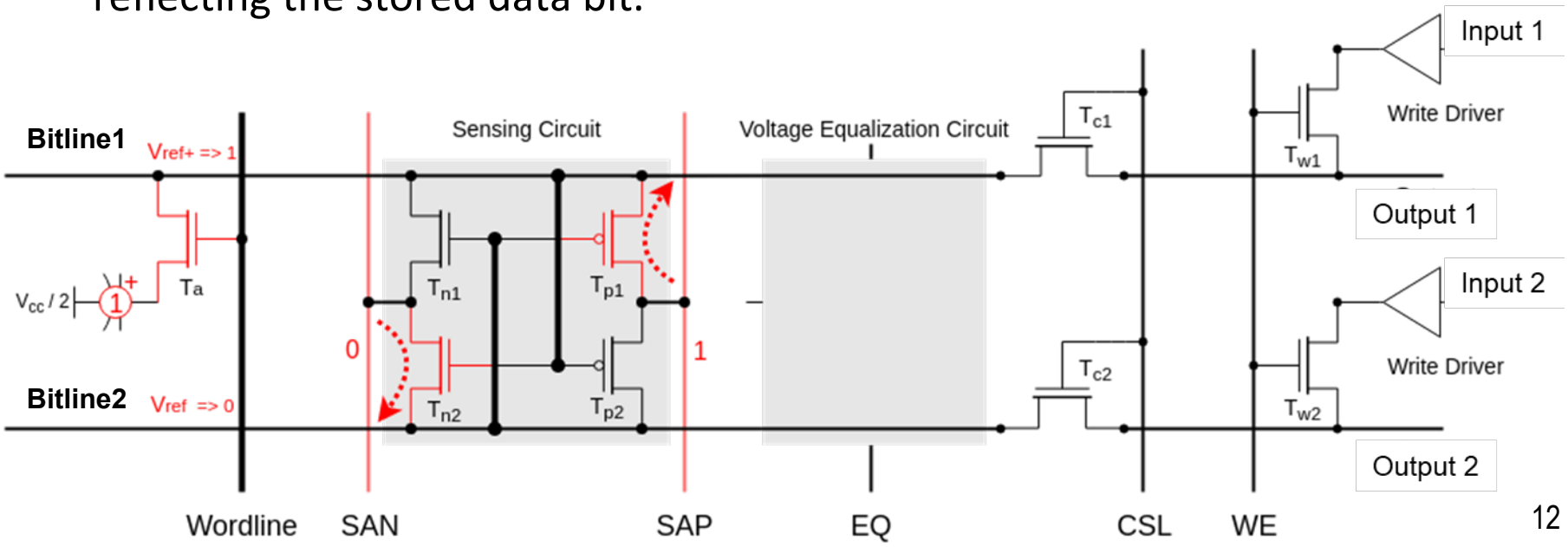

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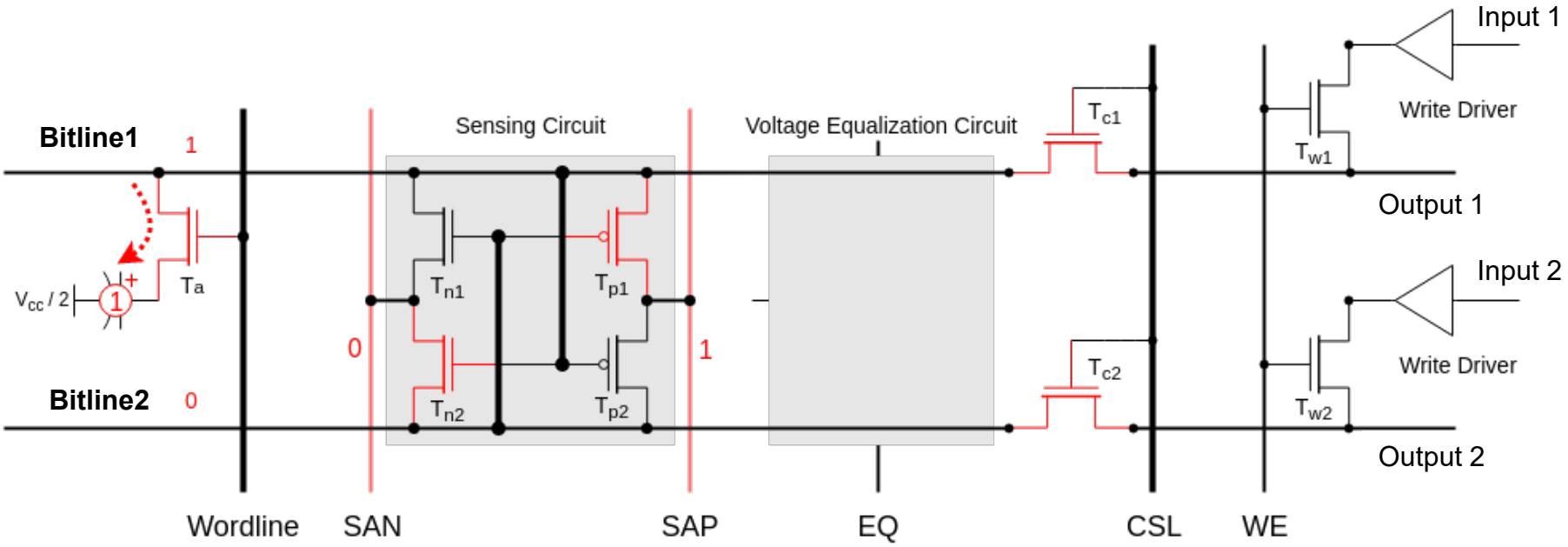

Write mode of DRAM

- Step5: Write Recovery
  - **Maintaining WE signal low:** Prevents further data writing.
  - **Stabilizing Bitline1 and Bitline2 voltages:** Keeps Bitline1 at logic 0 and Bitline2 at logic 1.
  - **Discharging Storage Capacitor:** Gradually discharges the Storage Capacitor to 0.
  - **Cutting off Access Transistor:** Isolates the Storage Capacitor from Bitline1 and Bitline2.
  - **Completion of Write Operation:** Data is stable, and the write operation is complete.