Memory Circuits & Systems

Exercise 1
Static Noise Margin of SRAM

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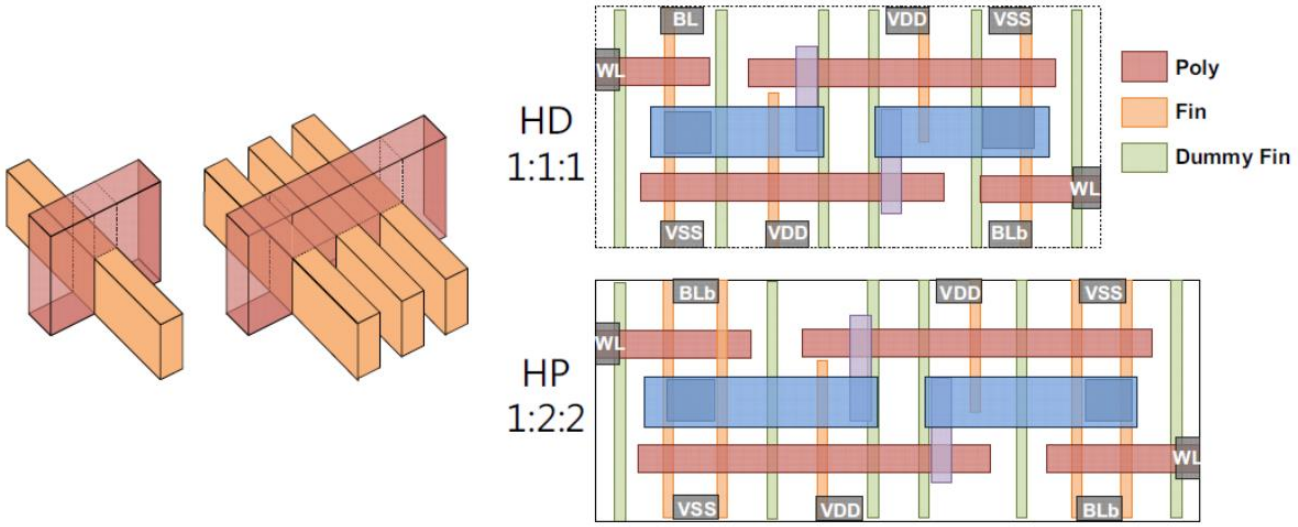
FinFET SRAM

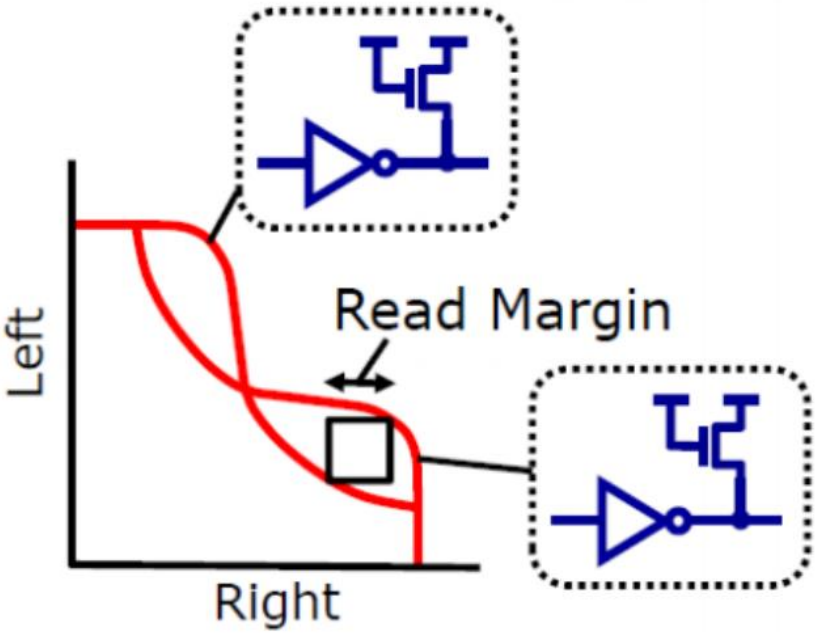
- In FinFET, the width which is given by $W = (T_{FIN} + 2H_{FIN}) \times N_{FIN}$ is quantized.
- For a high-density FinFET 6T-SRAM cell and a high-performance FinFET 6T-SRAM cell, the width ratio of Pull-Up PMOS, pass-gate NMOS and Pull-down NMOS are 1:1:1 and 1:2:2, respectively

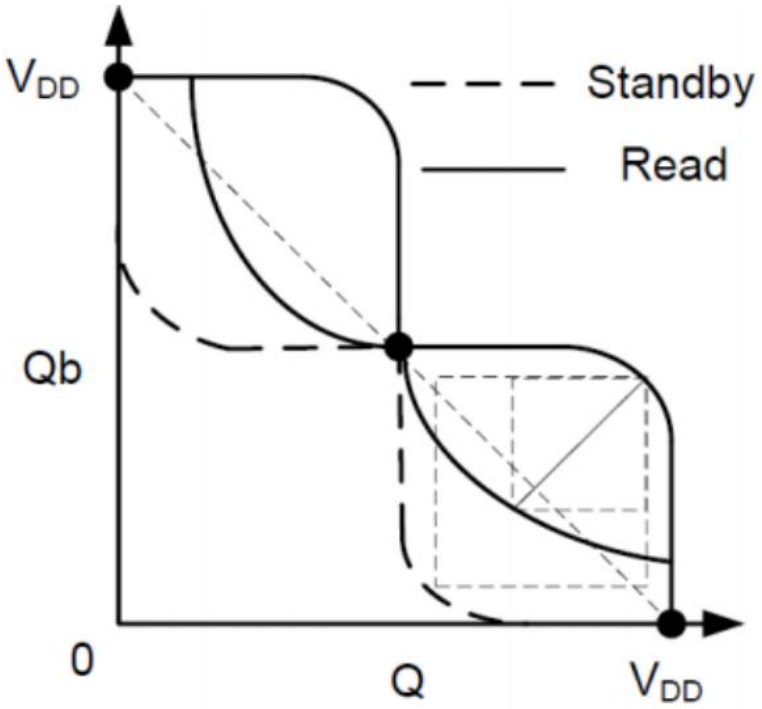


Fin-based SRAM bitcell design

Butterfly Curve of SNM and RSNM [30%]

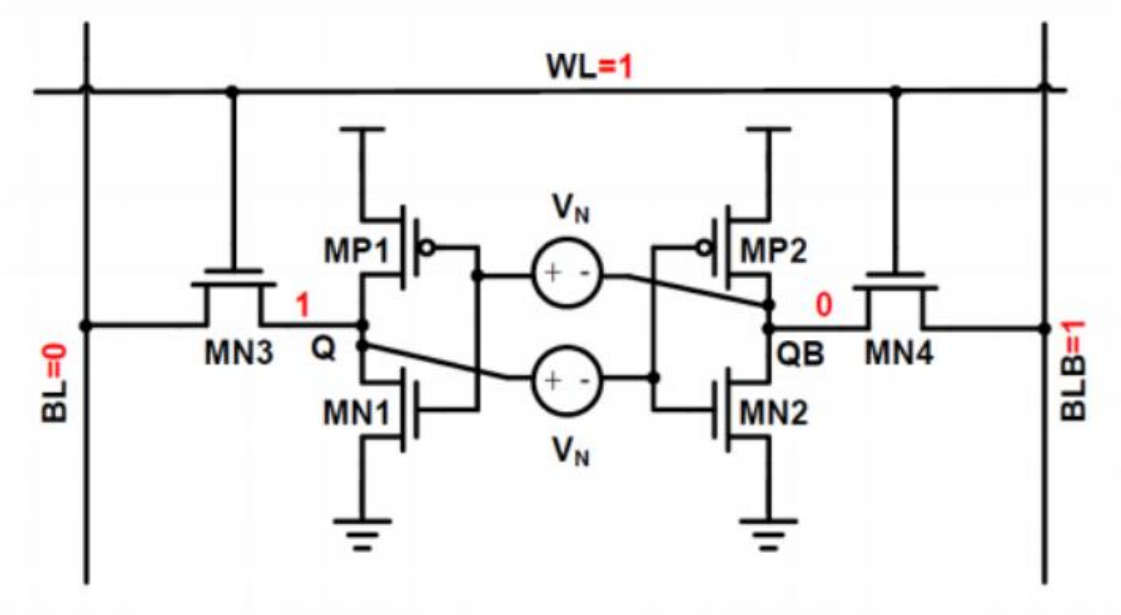
- Using 7nm FinFET model to analyze SNM and RSNM of 1:1:1 and 1:2:2 FinFET SRAM cells
  - Plot butterfly curve of data retention and read modes
    - Hint: DC analysis and get data by .print

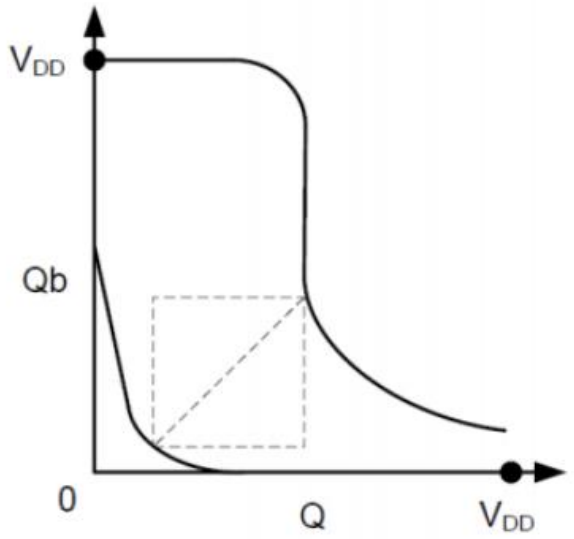




Write Noise Margin (WNM) Curve [30%]

- Using 7nm FinFET model to analyze WNM of 1:1:1 and 1:2:2 FinFET SRAM cells
  - Measure the transfer curve of the inverter and plot the curve





Static Noise Margin Analysis [40%]

- Analyze SNM, RSNM and WNM of 1:1:1 and 1:2:2 FinFET SRAM cells under
  - different supply voltages from 0.7V to 0.4V
    - Bitline/wordline voltages are the same as that of cell voltage
  - different wordline voltages
    - 0.9V to 0.5V when VDD =0.7V

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