# Memory Circuits & Systems

## Exercise 3
## Sensing Amplifier

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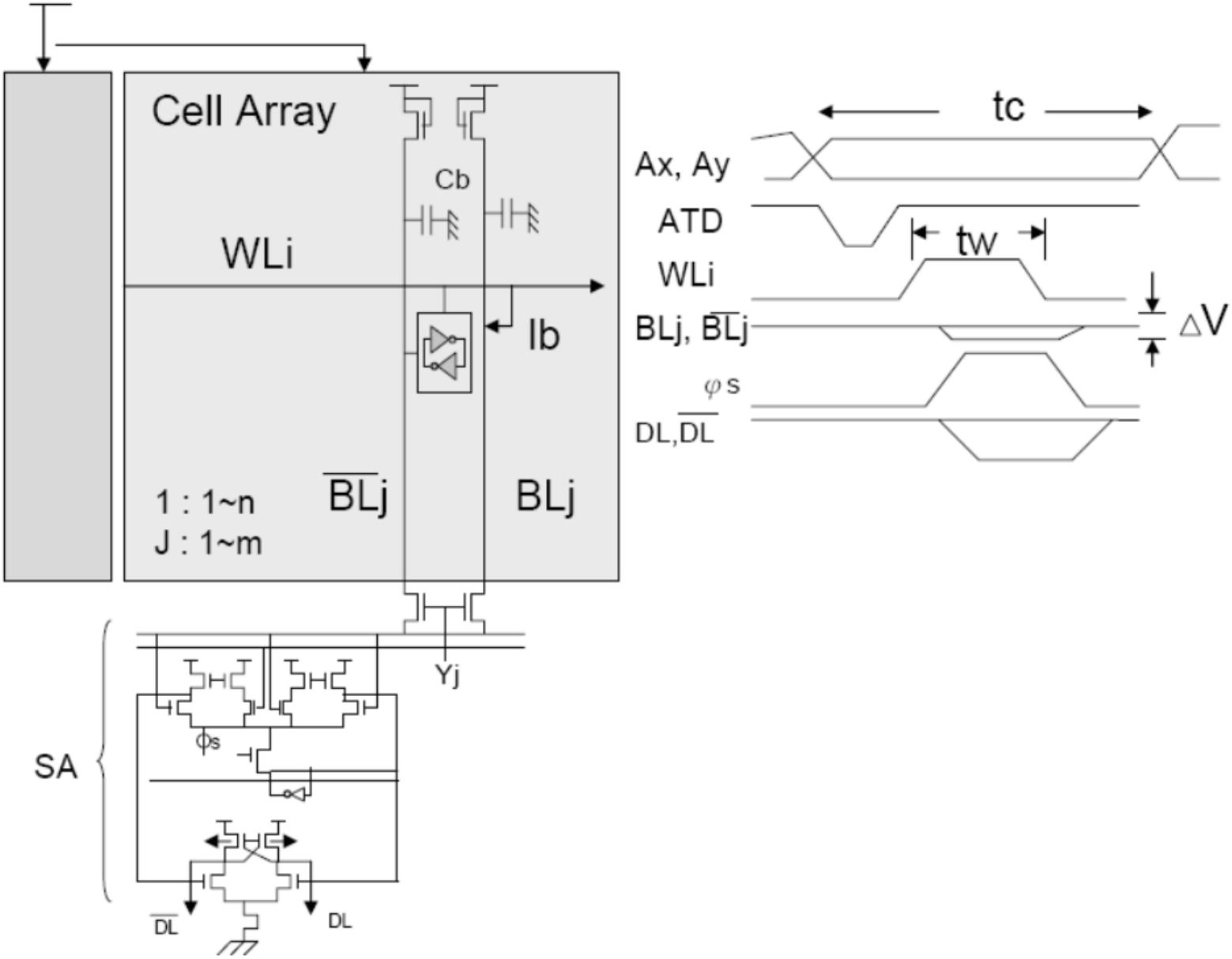
# Design & Analysis of Sensing Amplifier

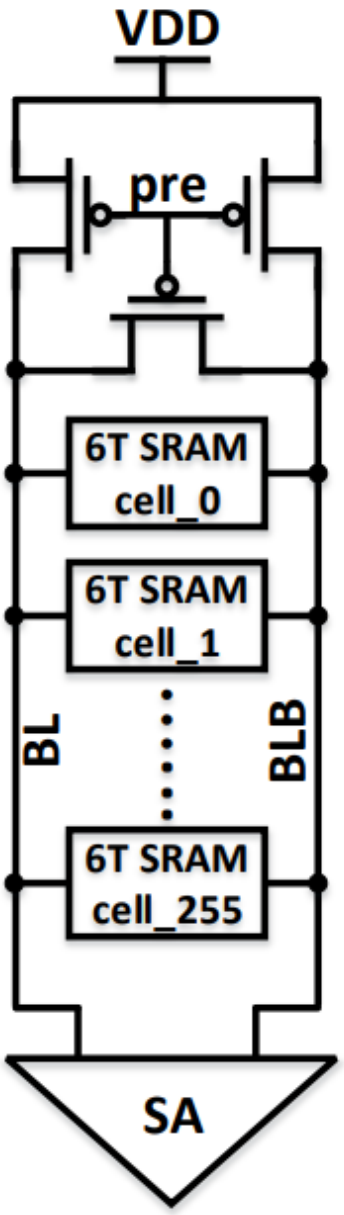
- Implementation read operation of SRAM using 7nm FinFET model (frequency = 1GHz)
  - Input: PRE, WL, SEN, C-SEL
  - Output: dout
  - Design three types of sensing amplifiers and simulate 1 column with 512 SRAM cells
    - Current-mode SA
    - Voltage-mode SA
    - Voltage mode SA with pre-charging circuits
  - Estimate loading of BL and BLB (cells + wire loading)
  - Please compare and analyze the performance in terms of read power and sensing timing of the 3 sensing amplifiers

# Data Sensing for Read Operation of SRAM



# Read mode of SRAM

- Step 1:
  - BL and BLB precharged by precharger
- Step2:
  - Activate WL of the selected row
- Step3:
  - Depend on the data of the selected cell, BL or BLB discharged by the pull down NMOS
- Step4:
  - Enable the sense amplifier
- Step5:
  - Sense read data



# Submission on E3 platform

- Please compress your **report** & **source codes in a single compressed file (.zip/.rar)** and upload this single file on E3 platform
  - **Report: simulation results(read power & sensing timing), comparison and analysis of 3 Sensing Amplifiers**
  - Naming rules of the compressed file
  - Upload file: **Ex3_#ID.zip (including report & source code)**
- Due date: 4/25 P.M. 23:55