Memory Circuits & Systems

Exercise 2
6-to-64 Row Decoder Design

Professor Po-Tsang Huang

International College of Semiconductor Technology
National Yang Ming Chiao Tung University

6-to-64 row decoder

- Design **a 6-to-64 row decoder** for a SRAM array no whether which logic style. The I/O descriptions of the row decoder design are list in Table 1. All the **input data must be connected to a buffer** so that the inputs won't have infinite driving ability.
- Bonus:
  - Use high-level program to generate the spice code, such as C/C++, Python, Verilog.

Table 1. I/O description for register file

Pin Name	I/O	Description
Clock	Input	Clock input
Address[5:0]	Input	Read/Write Address
Wordline[63:0]	Output	64 Word-lines

Specifications of row decoder

- The frequency (data sampling rate) should reach to 1GHz (50% duty cycle).
- Address signals are changed at the falling edge of clock.
- The wordline would be asserted when clock is 1.
- The wordline capacitances depend on gate capacitances of the pass transistors in memory cells and wire loading.
  - The loading of each wordline is based on 1:1:1 SRAM and 7nm wire model. (64 SRAM cells on a row)
- The rise time and fall time of inputs are 0.05ns respectively.

Submission on E3 platform

- Please compress your **report** & **source codes in a single compressed file (.zip/.rar)** and upload this single file on E3 platform
  - **Report: Report your analysis and results, including the architecture, performance and power consumption.**
- Naming rules of the compressed file
  - Upload file: **Ex2_#ID.zip (including report & source code)**
- Due date: 4/11 PM 23:55