# Memory Circuits & Systems

## Exercise-4
## SRAM-based Analog CIM for Binary CNN

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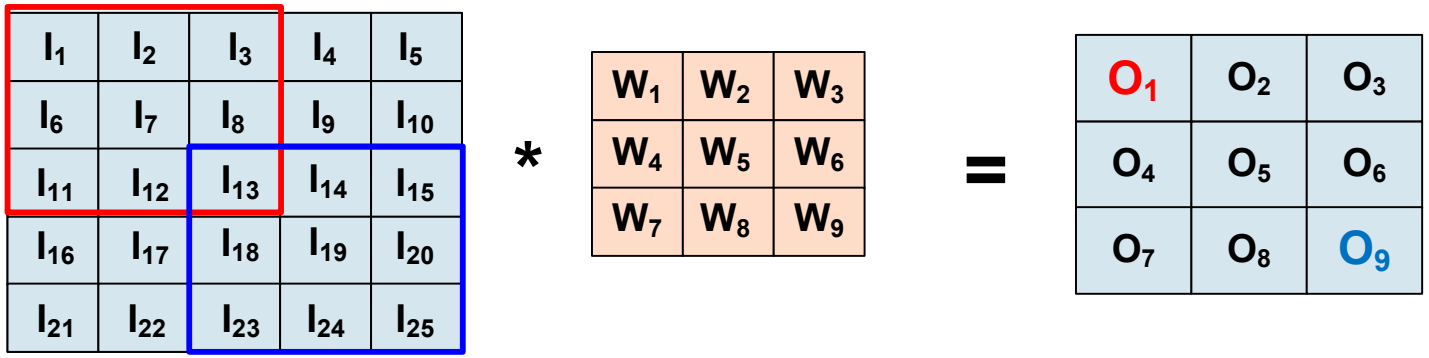
# Introduction of 3x3 Convolution

- Example of a 3x3 convolution

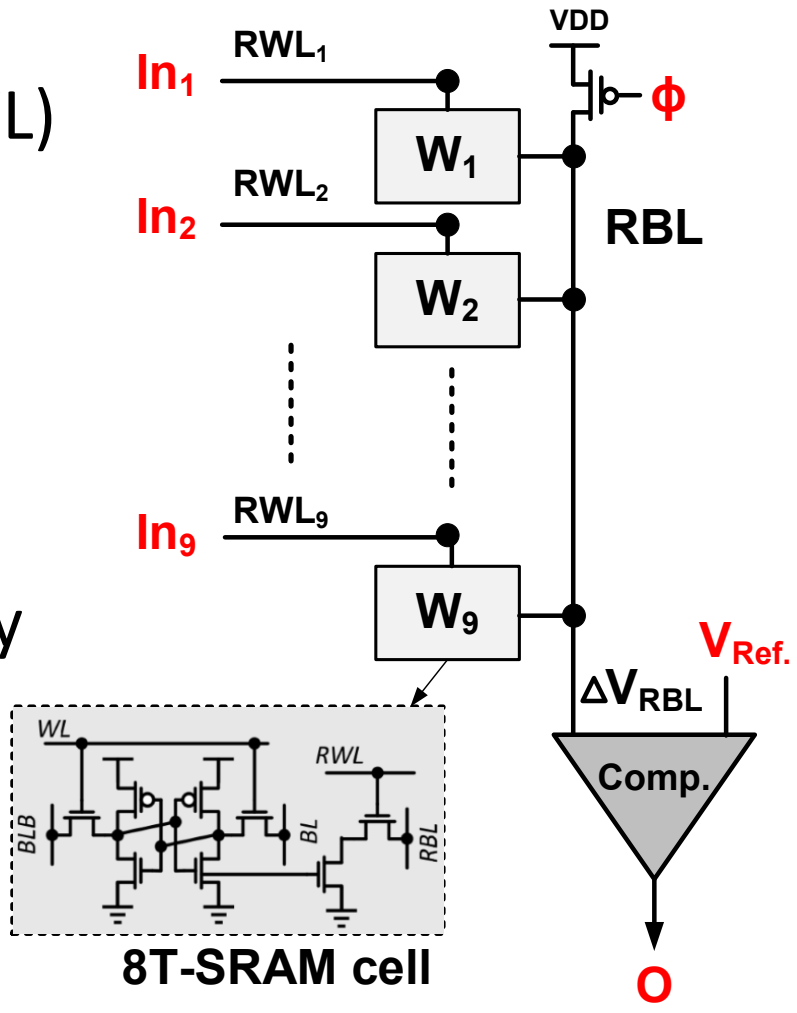



$$O_1 = W_1 \times I_1 + W_2 \times I_2 + W_3 \times I_3 + W_4 \times I_6 + W_5 \times I_7 + W_6 \times I_8 + W_7 \times I_{11} + W_8 \times I_{12} + W_9 \times I_{13}$$

$$O_9 = W_1 \times I_{13} + W_2 \times I_{14} + W_3 \times I_{15} + W_4 \times I_{18} + W_5 \times I_{19} + W_6 \times I_{20} + W_7 \times I_{23} + W_8 \times I_{24} + W_9 \times I_{25}$$

# Design a SRAM based CIM for 3x3 convolution

- The followings should be defined by yourself:
  - $V_{Ref}$
  - Input pulse width for 0/1 (RWL)
  - Cycle time of inputs and clock
- Design hints:
  - 8T-SRAM cells
  - 1 column with 9 rows
  - Store weights in SRAM cells by initial conditions (.IC)
  - $BL = \overline{BL}$ are biased at *VDD*
  - WL is biased at *GND*




Reminder: RBL should be precharged before multiplying

# Input Specification

## ◆Input :

| Input | Description |
|---|---|
| $In_1$ - $In_9$ | Input feature map, each input is 1 bit |
| $V_{Ref}$ | Reference voltage |
| $\phi$ | Precharge signal |

**Input feature map:**

| | | | | |
|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 1 |
| 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |

*

**Weights**

| | | |
|---|---|---|
| 1 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |

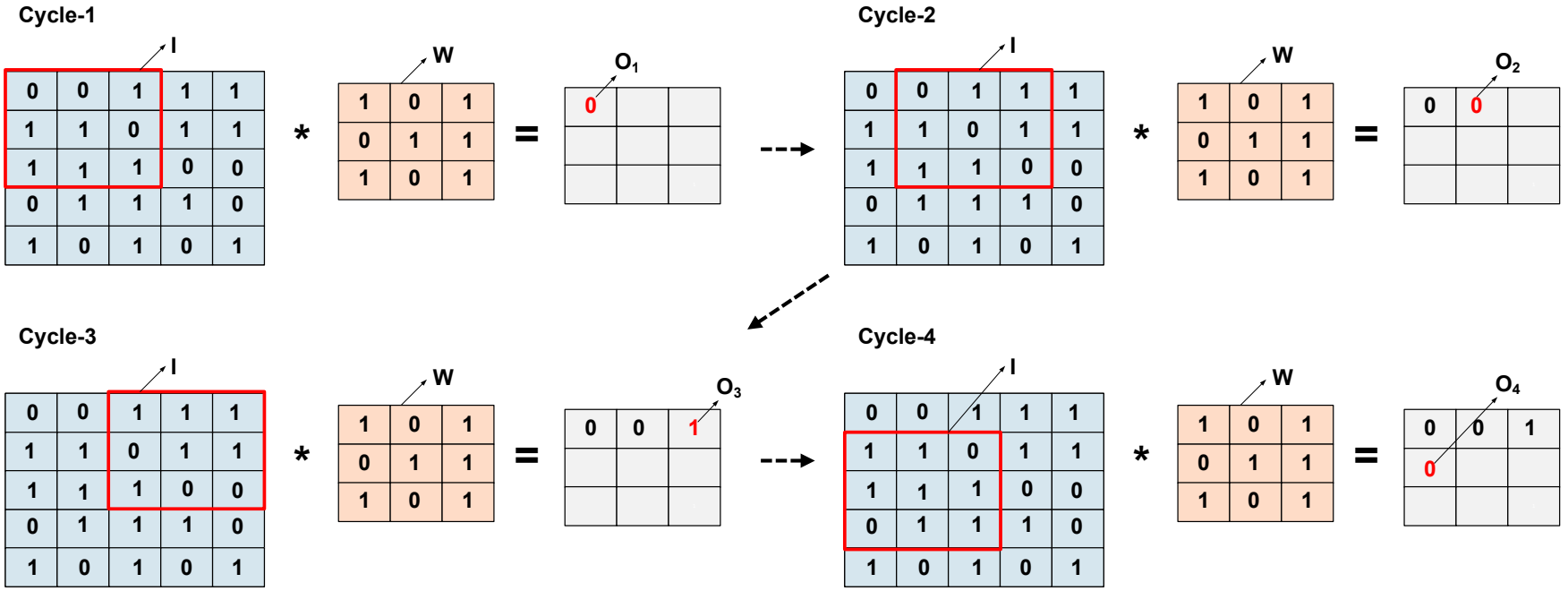
# Output Specification

## ◆Output :

| Output | Bit width | Description |
|---|---|---|
| O | 1 | Output feature map |

◆ The output should be quantized to 1-bit: O = Q( $\sum IxW$ ), where Q(x) = $\begin{cases} 0 & x < 5 \\ 1, & x \geq 5 \end{cases}$

◆ Hints:



# Measurement & Analysis

- Measure:
  - Delay (from the first cycle of 9 input features to the last cycle of the ninth convolutional output)
  - Power
- Calculate: **(1MAC = 2OPs)**
  - Energy efficiency (TOPs/W)
  - Throughput (TOPs/s)

Submission: Report & Source codes
Deadline: 2024/05/9 P.M. 23:55