Memory Circuits & Systems

Exercise 5
Cache Performance

1. For a direction-mapped cache design with 32-bit address, the following bits of the address are used to access the cache.

Tag	Index	offset
31-10	9-4	3-0

(a) What is the cache block size (in bits)?

(b) How many entries does the cache have?

(c) What is the ratio between the total bits required for such a cache implementation over the data storage bits?

(d) Starting from power on, the following byte-addressed cache references are recorded. How many blocks are replaced?

Address (in Decimal)	Hex
0	0x0000 0000
4	0x0000 0004
16	0x0000 0010
132	0x0000 0084
232	0x0000 00E8
160	0x0000 00A0
1024	0x0000 0400
30	0x0000 001E
140	0x0000 008C
3100	0x0000 0C1C
180	0x0000 00B4
2180	0x0000 0884

(e) What is the hit ratio?

2. The following C program is run (with no optimizations) on a processor with a cache that has eight-word (32-byte) blocks and holds 256 bytes of data:

```
int i, j, c, stride, array[512];
for (i = 0; i < 10000; i++)
for (j = 0; j < 512; j = j + stride)
c = array[j] + 17;
```

If we consider only the cache activity generated by references to the array and we assume that integers are words, what is the expected miss rate when the cache is direct mapped and stride = 256? How about if stride = 255? Would either of these change if the cache were two-way set associative?

Submission Deadline: 2024/05/23 P.M. 23:55