Two Stage Opamp Using Miller Compensation Technique for 28nm Technology

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***Abstract*—An analog amplifier is an essential block required in most of the circuits, which is used to amplify the signal. This paper talks about design of a two stage operational with Miller frequency compensation. The amplifier is designed to have gain greater than 40dB, phase margin greater than 60◦, slew-rate of 10V/us and CMRR greater than 60dB.**

Keywords—Opamp, Miller compensation, Frequency compensation

I. INTRODUCTION TO TWO STAGE AMPLIFIER

A two-stage operational amplifier comprises a differential amplifier in its first stage, followed by a simple common source amplifier in its second stage. The first stage takes a differential input and returns an amplified, 180◦ phase-shifted signal. The second stage boosts the gain and causes another 180◦ phase shift.

The phase margin is reduced to a negative value. As a result, in order to overcome this instability, we'll need to make changes to the design. Frequency compensation Technique is a method of adjusting the op-loop amp's gain frequency response so that it behaves like a single break frequency response with enough positive phase margin. Here, in this paper, Miller frequency compensation technique is used.

II. DESIGN OF TWO STAGE AMPLIFIER

Table [1] shows the specification used for designing two stage opamp

DC Gain	≥40dB
Gain Bandwidth Product	5MHz
Phase Margin	60◦
Slewrate	10V/µs
C_L	10pF
V_{DD}	5V
CMRR	≥60dB

Table 1. Design Specifications

The aspect ratio of all the mosfets are calculated based on given specifications in table [1]. Table [2] shows W/L of mosfets.

$W/L_{1,2}$	1
$W/L_{3,4}$	17
W/L_5	16
W/L_7	28
W/L_6	56

Table 2. W/L ratios

Figure [2] shows design of two stage amplifier. C_C is Miller compensated capacitor. The technology used for this project is 28nm.

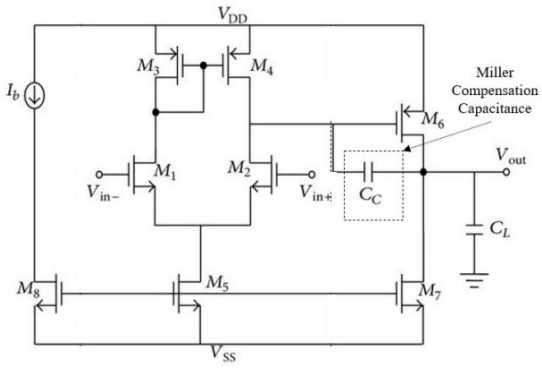


Figure 2. Schematic of Two stage opamp with Miller compensated capacitor

III. SIMULATION AND RESULTS

Figure [3] shows the expected waveform. It is a gain v/s frequency and phase v/s frequency plot.

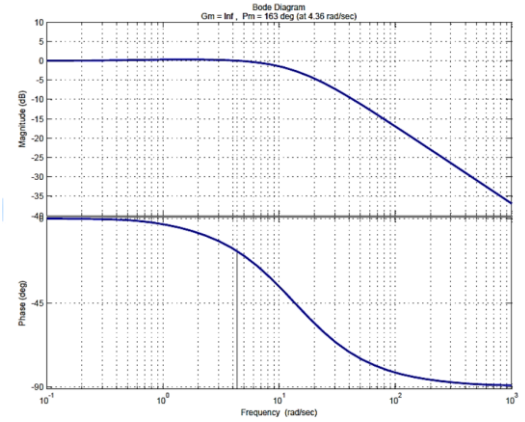
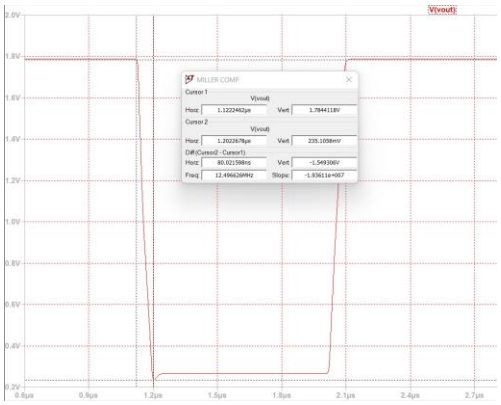


Figure 3. Expected Bode Plot

The area report wiil be generated once the simulations are done.



IV. REFERENCE

[1] B. Razavi, Design of analog CMOS integrated circuits., 2005.

[2] J. Ruiz-Amaya, A. Rodrıguez-P´erez, and M. Delgado-Restituto, "A comparative study of low-noise amplifiers for neural applications," in 2010 International confer ence on microelectronics, IEEE, 2010, pp. 327–330