MCIMX93-SOM

(MCIMX93-EVK: SOM+BB)

Table of Content

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1. Interrupted lines coded with the same letter or letter combinations are electrically connected.

2. Device type number is for reference only. The number varies with the manufacturer.

3. Special signal usage:
   _B Denotes - Active-Low Signal
   <> or [] Denotes - Vectored Signals

4. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.

Preliminary - Subject to Change without Notice!

This board was designed for maximum flexibility in software development and demonstrates multiple functions possible with i.MX processors. Although best design practices have been applied, some areas may not be suitable for a mass-production design.

Revision History

Rev. Code	Date	By	Description
A	*2022-01-14*	*nxa22324*	*Initial version*
A1	*2022-03-24*	*nxa22324*	*Update the i.MX93 BOOT MODE table and I2C DEV table*
B	*2022-08-08*	*nxa22324*	*Change U901 to DML3006, U903,U906,U908,U910 to TPS22990 due to NCP45541 out of stock* *Change R908 to 1K OHM; Remove R925, R940,R954, R986* *Change R1036,R1037,R975,R976,R977 to PULL-UP* *Change U901,U903,U906,U908,U910 enable signals to FSC_CTRL_H1-5*
B1	*2023-01-30*	*nxa22324*	*Update U701 PMIC symbol* *Change VDD_SOC_0V8 to VDD_SOC_0V85*
B2	*2023-04-11*	*nxa22324*	*Update U101 symbol for USB ID power domain* *Change VDD_SOC sample resistor R932 to 5mΩ to reduce power drop* *Change ADC power rail with more CAP+FB, install C720, change L102 to 1K OHM FB* *Add R211 to support LPDDR4/X w/ 2CS*
	2024-02-26	*nxa22324*	*Update C102 to 1uF to improve voltage ripple* *Add note for VFBGA100 LPDDR4/X reset compatible design* *Update U201 from MT53E1G16D1FW-046 AAT:A to MT53E1G16D1ZW-046 AAT:C due to EOL*

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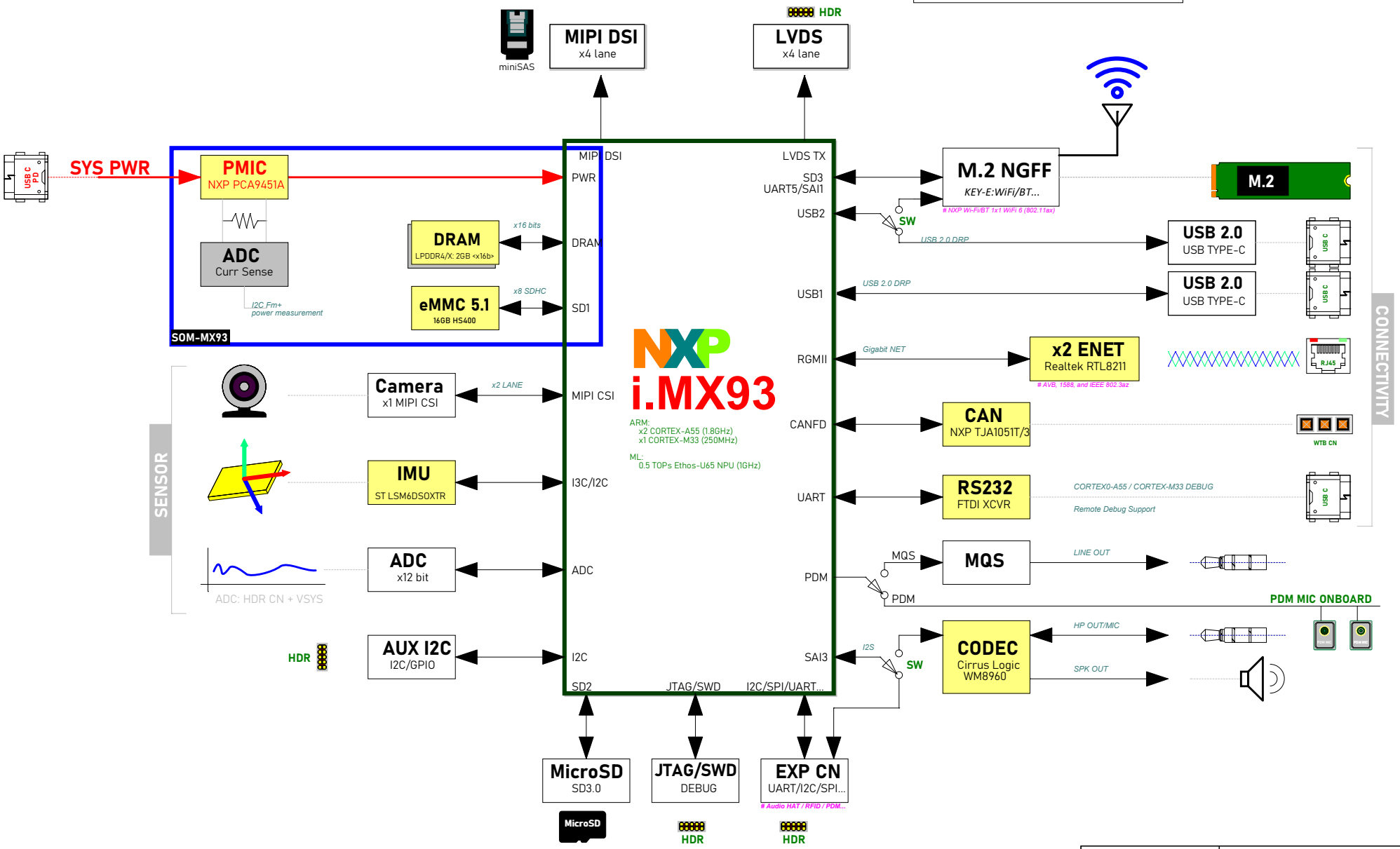
BLOCK DIAGRAM

MCIMX93-EVK	51960
├ MCIMX93-SOM	51943
└ MCIMX93-BB	51961



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i.MX93 EVK PWR TREE

When PER_12V is required, VBUS_IN must be at least 12V!!!

USB C SNK PD

VBUS_IN
12-20V

DCDC BUCK
MPS MP8759GD

VSYS
5V/3A

DCDC_5V
5V/5A

DCDC BUCK
MPS MP2147

VEXT_3V3
3.3V/4A

Load SW
MOSFET

VDD_5V
5V/3A

DCDC BUCK
MPS MP2263GD

PER_12V
12V/3A

PMIC: PCA9451A CFG

SEQ		REGULATOR	VOL (V)	MAX I (mA)
1		LDO1	1.8	10
-				
2	T1	BUCK1/3 DP	0.85	4000
3	T2	LDO4	0.8	200
4				
5	T4	BUCK5	1.8	2000
6	T5	BUCK6	1.1	1500
7	T6	BUCK2	0.6	2000
8	T7	BUCK4	3.3	3000
8	T7	Load Switch	-	400
9	T8	LDO5	1.8/3.3	150
-	-			
12		POR_B	--	--

SoC: i.MX93

ITEM	PWR RAIL	TYP VOL(V)	REQ I (mA)
1	NVCC_BBSM_1V8	1.8	2
PMIC_ON_REQ			
2	VDD_SOC	DVS	Ref to DS
3	VDD_ANA_0P8	0.8	186
4			
4	VDD_ANA_1P8/NVCC_WAKEUP	1.8	389
5	VDD2_DDR/LPD4 VDDQ	1.1	676
6	VDDQ_DDR (0.6V for LPD4x)	0.6	360
7	NVCC_GPIO/VDD_USB_3P3	3.3	30/2870
7	SD_CARD	3.3	
8	NVCC_SD2	1.8/3.3	
-			
POR_B			

LPDDR4/X
VDD1 <1.8V>
VDD2 <1.1V>
VDDQ <0.6V/1.1V>

eMMC
VCCQ <1.8V>
VCC <3.3V>

MicroSD
VCC <3.3V>

Audio CODEC
AVDD/DVDD <3.3V>
SPKVDD <5V>

ETHERNET
DVDD_REG <1.8V>
AVDD/DVDD <3.3V>

USB C DRP/ A HOST
VBUS <5V>

M.2 KEY-E
3.3V

MIPI DSI / LVDS
3.3V
5V
12V

MIPI CSI
3.3V

RPi
3.3V
5V

PDM/MQS/CAN
3.3V
5V

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Page Title: Power Tree
Approved: <Approver>
Size: Custom
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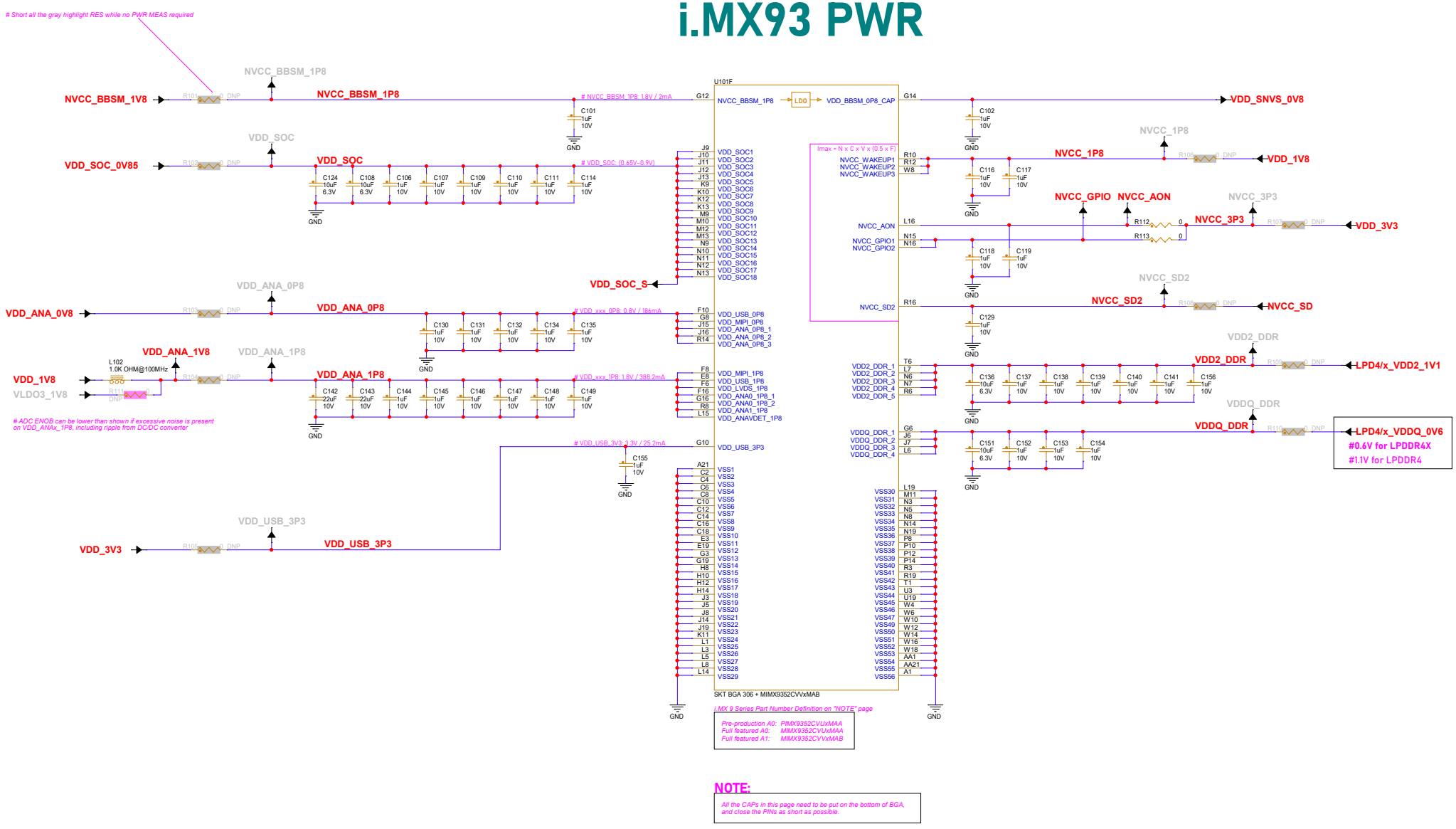
i.MX93 PWR



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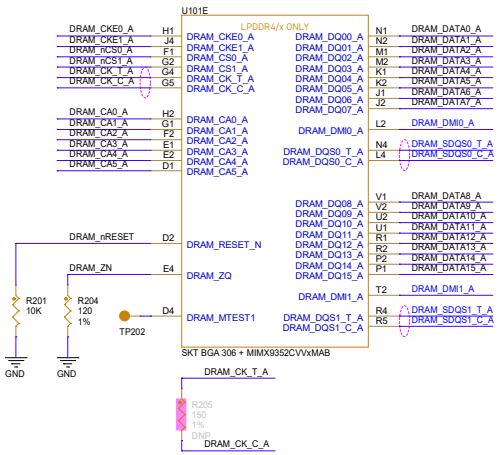
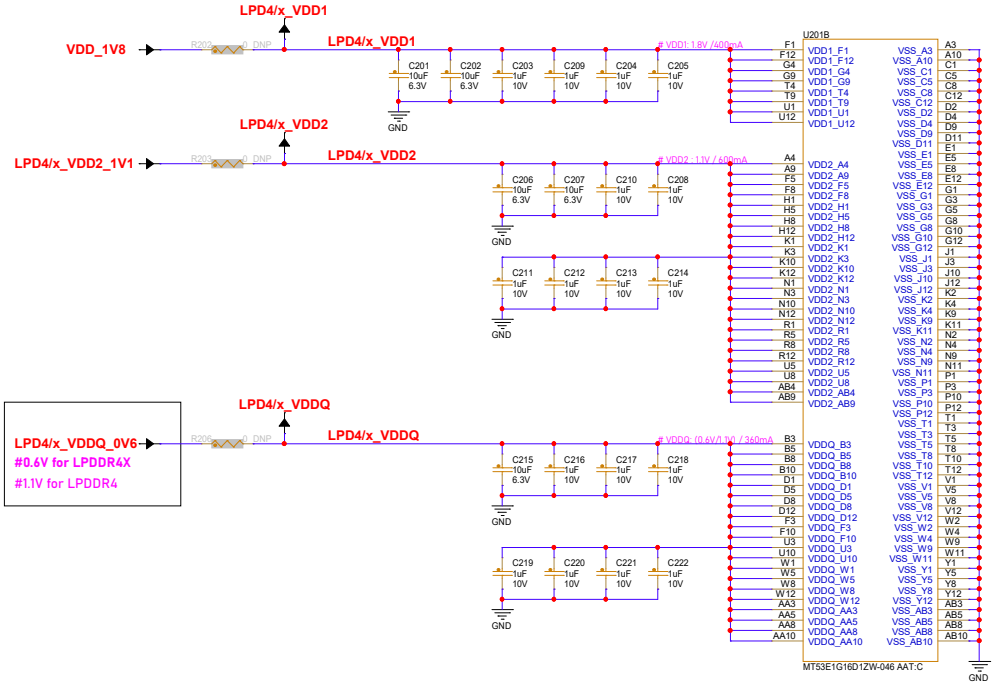
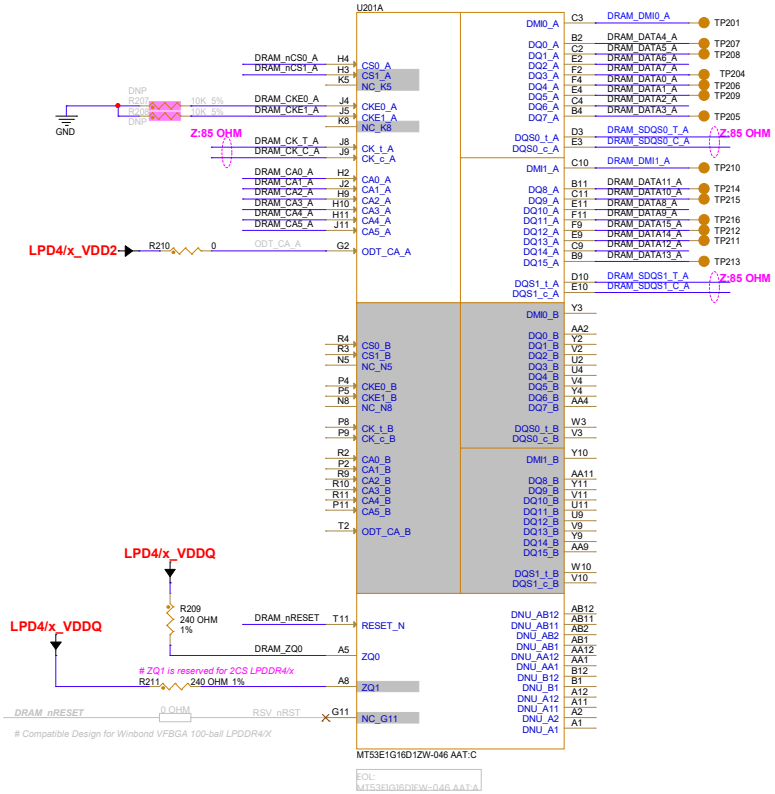
LPDDR4/X





LPDDR4X: 2GB (x16)



Power Supply Voltage Sequence:

RESET_n is held LOW.
VDD1 >= VDD2
VDD2 >= VDDQ-200mV

Power ramp duration tINIT0 (Tb–Ta) must not exceed 20ms.

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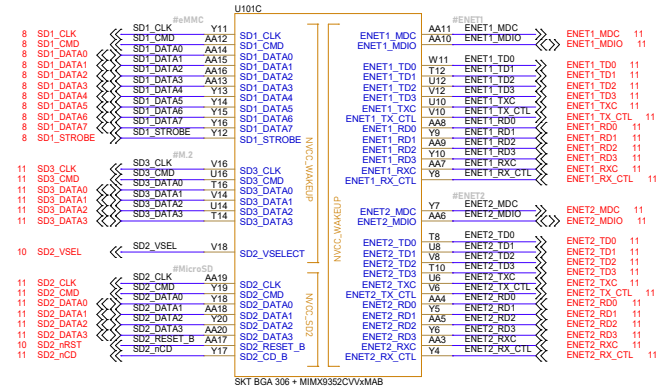
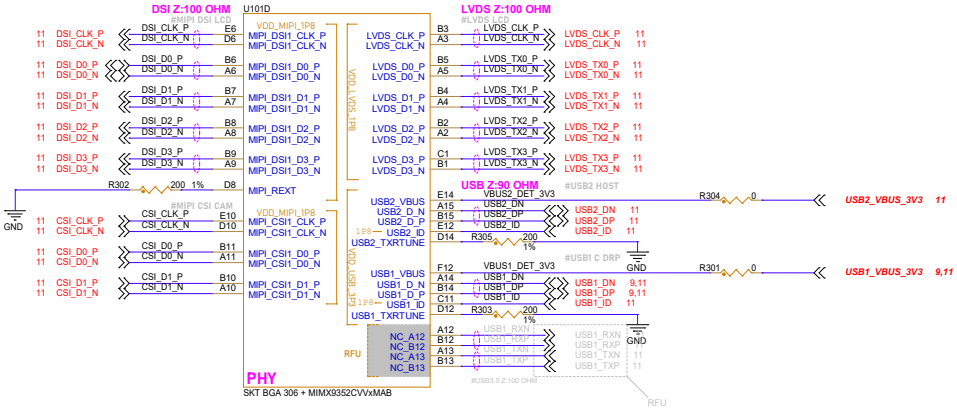
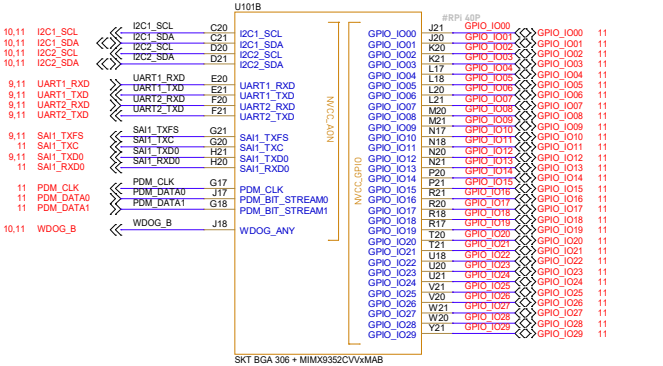
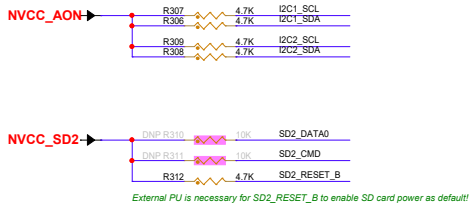
i.MX93 IO/PHY









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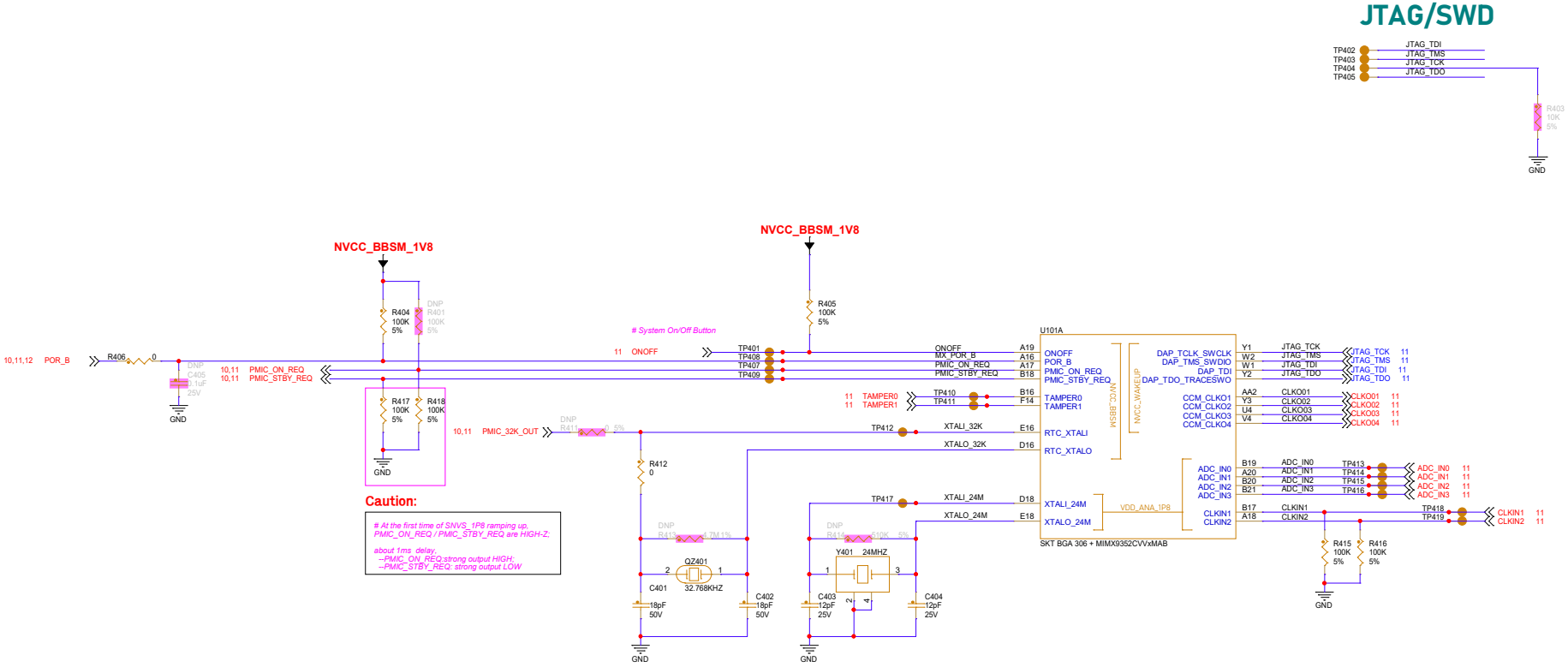
i.MX93 MISC



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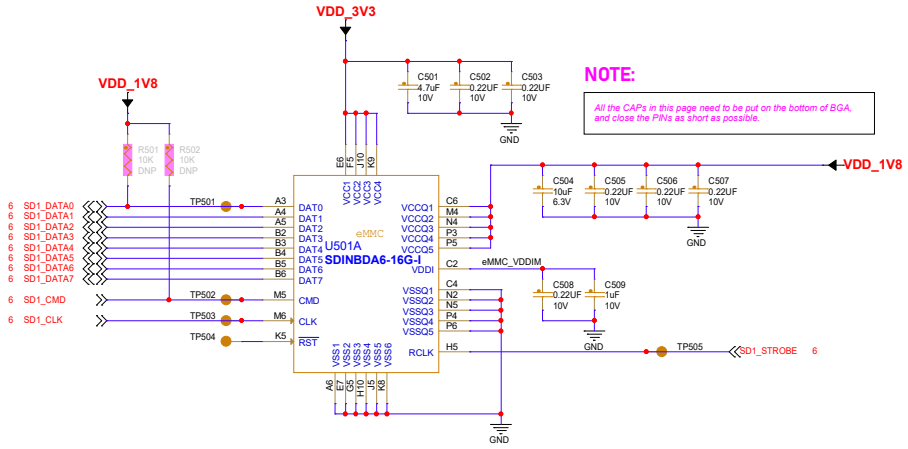
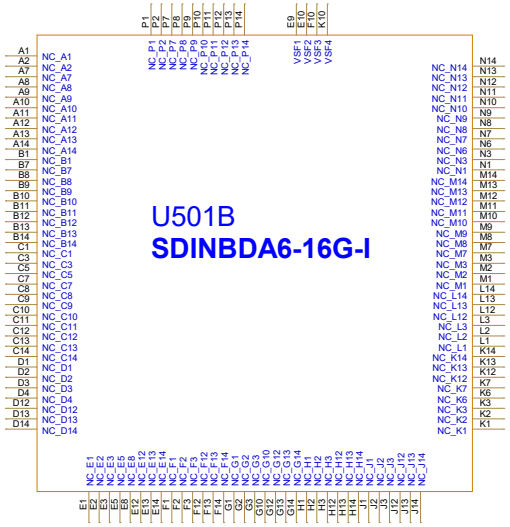
FLASH: eMMC <5.1>





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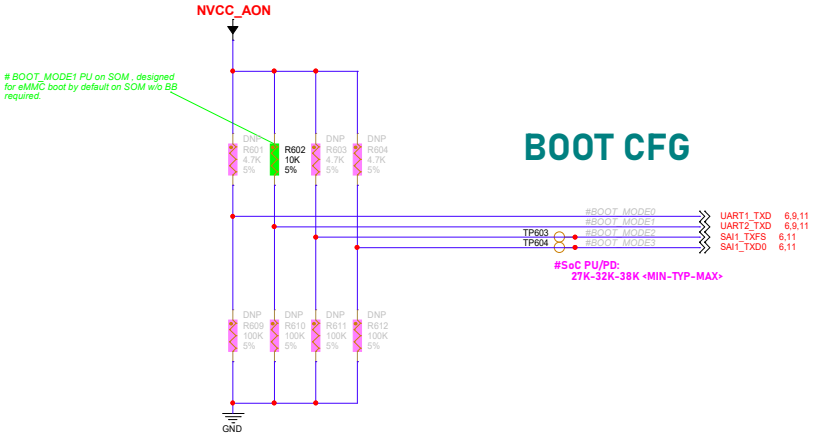
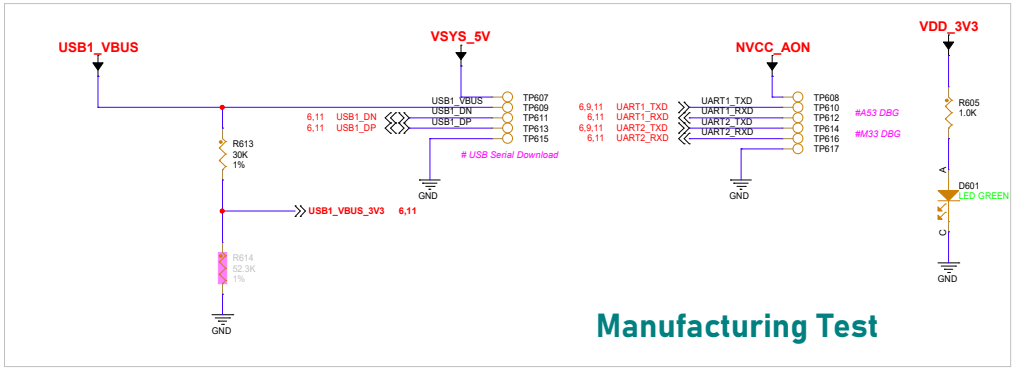
Boot Mode and CFG Switch

i.MX93 BOOT MODE

BOOT_MODE[3:0]	BOOT CORE	BOOT DEVICE	COMMENT
0000	Cortex-A55	From internal fuses	
0001	Cortex-A55	Serial Downloader	USB1/2
0010	Cortex-A55	USDHC1 8-bit eMMC 5.1	
0011	Cortex-A55	USDHC2 4-bit SD3.0	
0100	Cortex-A55	FlexSPI Serial NOR	with SFDP (JESD-216) discoverable parameters
0101	Cortex-A55	FlexSPI Serial NAND 2K page	
0110	Cortex-A55	Infinite Loop	
0111	Cortex-A55	Test Mode	
1000	Cortex-M33	From internal fuses	
1001	Cortex-M33	Serial Downloader	USB1
1010	Cortex-M33	USDHC1 8-bit eMMC 5.1	
1011	Cortex-M33	USDHC2 4-bit SD3.0	
1100	Cortex-M33	FlexSPI Serial NOR	with SFDP (JESD-216) discoverable parameters
1101	Cortex-M33	FlexSPI Serial NAND 2K page	
1110	Cortex-M33	Infinite Loop	
1111	Cortex-M33	Test Mode	





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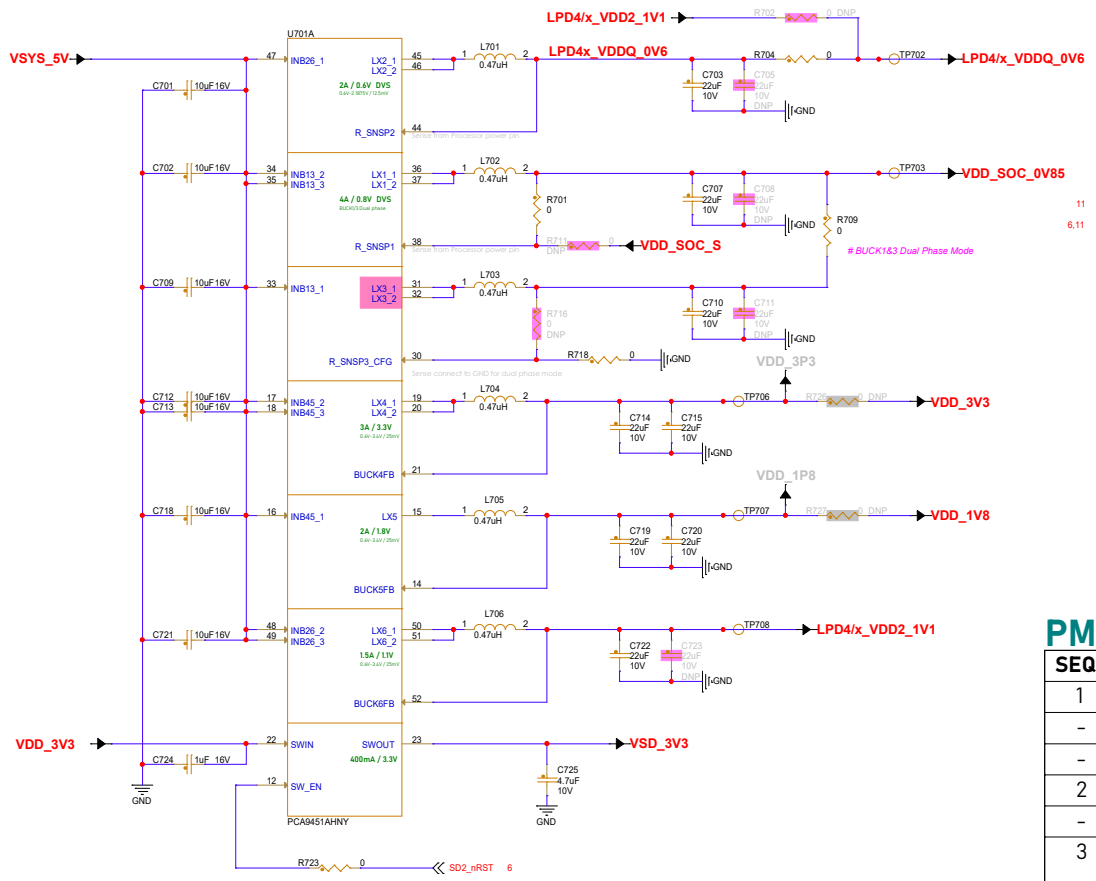
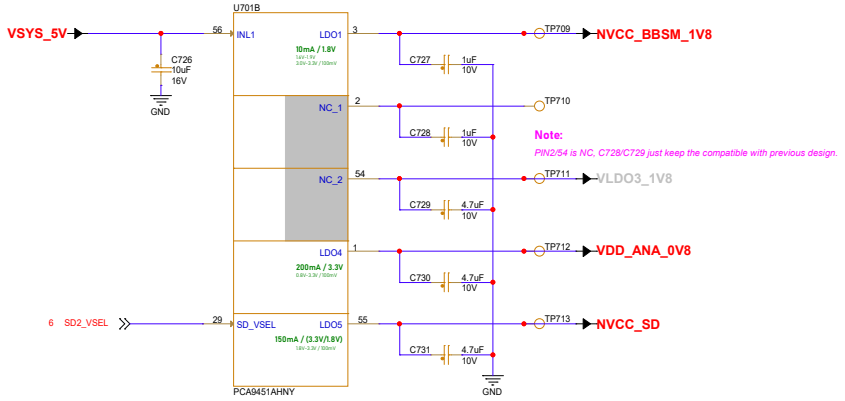
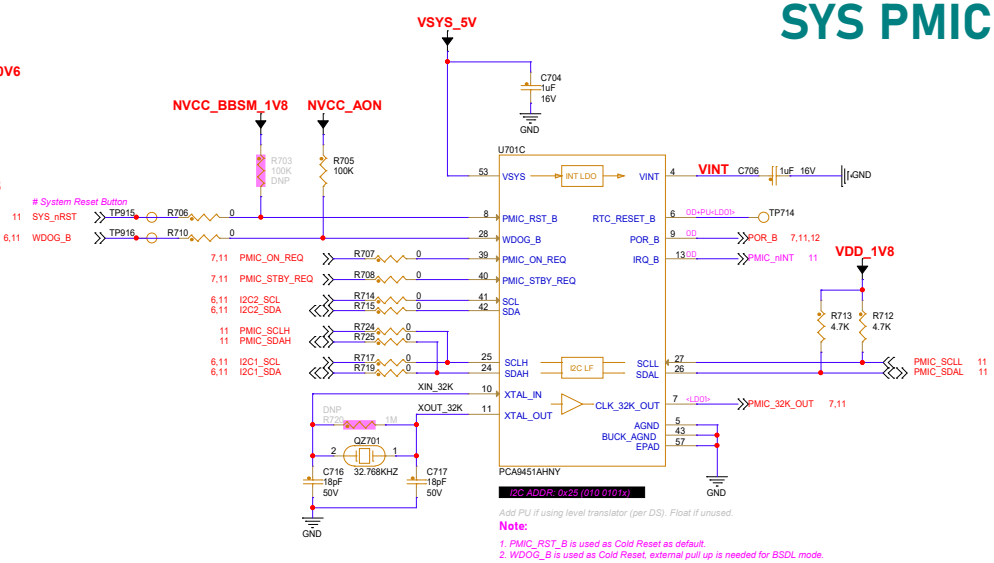
SYS PMIC







PMIC: PCA9451A CFG

SEQ	tstep=2ms	REGULATOR	VOL (V)	MAX I (mA)	PWR RAIL	TYP VOL(V)	REQ I (mA)
1		LDO1	1.8	10	NVCC_BBSM_1V8	1.8	2
-							
-					PMIC_ON_REQ		
2	T1	BUCK1/3 DP	0.85	4000	VDD_SOC	DVS	Ref to DS
-							
3	T2	LDO4	0.8	200	VDD_ANA_0P8 VDD_MIPI_0P8 VDD_USB_0P8	0.8	186
4							
5	T4	BUCK5	1.8	2000	VDD_ANAx_1P8 VDD_LVDS_1P8 VDD_MIPI_1P8 VDD_USB_1P8 NVCC_GPIO	1.8	1040 PERI INCLUDE
6	T5	BUCK6	1.1	1500	VDD2_DDR VDDQ_DDR (1.1V for LPD4)	1.1	676
7	T6	BUCK2	0.6	2000	VDDQ_DDR (0.6V for LPD4x)	0.6	360
8	T7	BUCK4	3.3	3000	NVCC_GPIO VDD_USB_3P3	3.3	2870 PERI INCLUDE
8	T7	Load Switch	-	400	SD_CARD (from BUCK4)	3.3	
9	T8	LDO5	1.8/3.3	150	NVCC_SD2	1.8/3.3	
-	-						
12		POR_B	--	--	POR_B		

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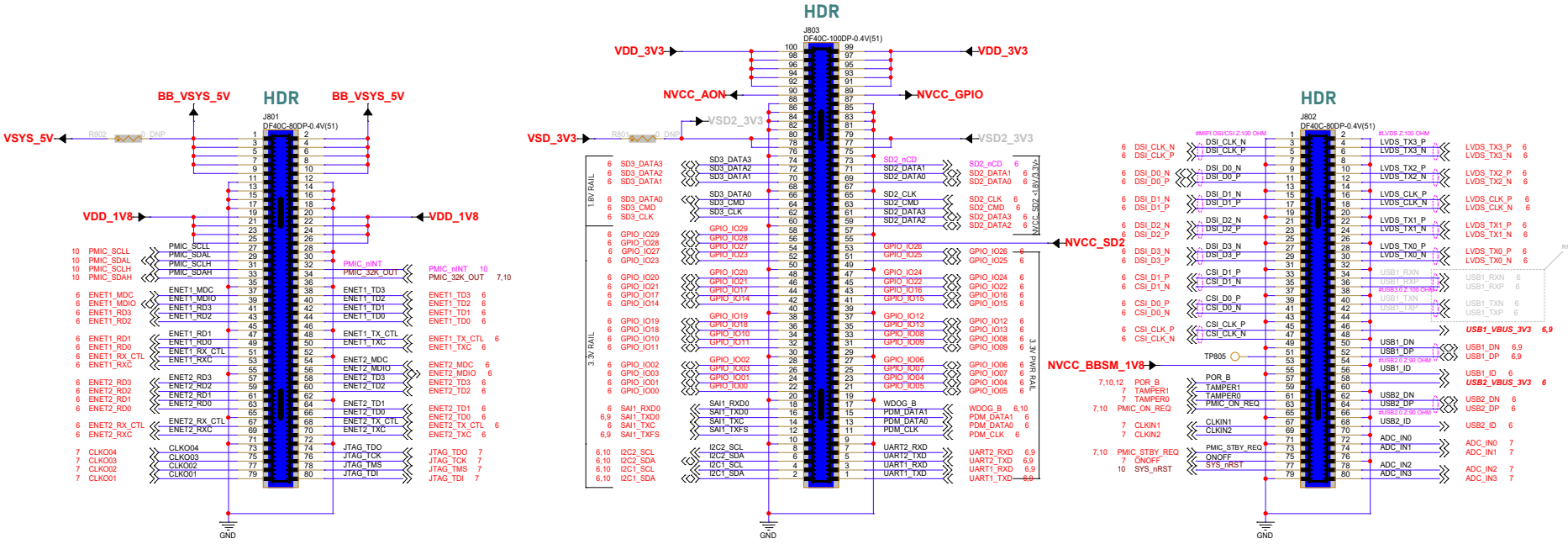
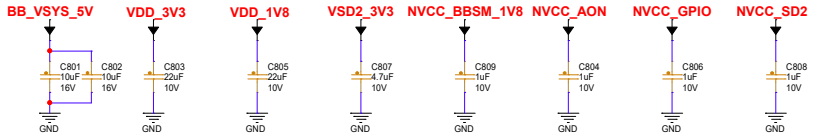
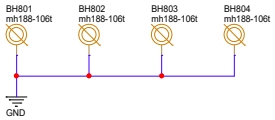
B2B CN for CPU SOM

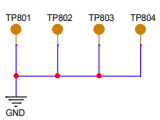




SCREW HOLE



GND TP



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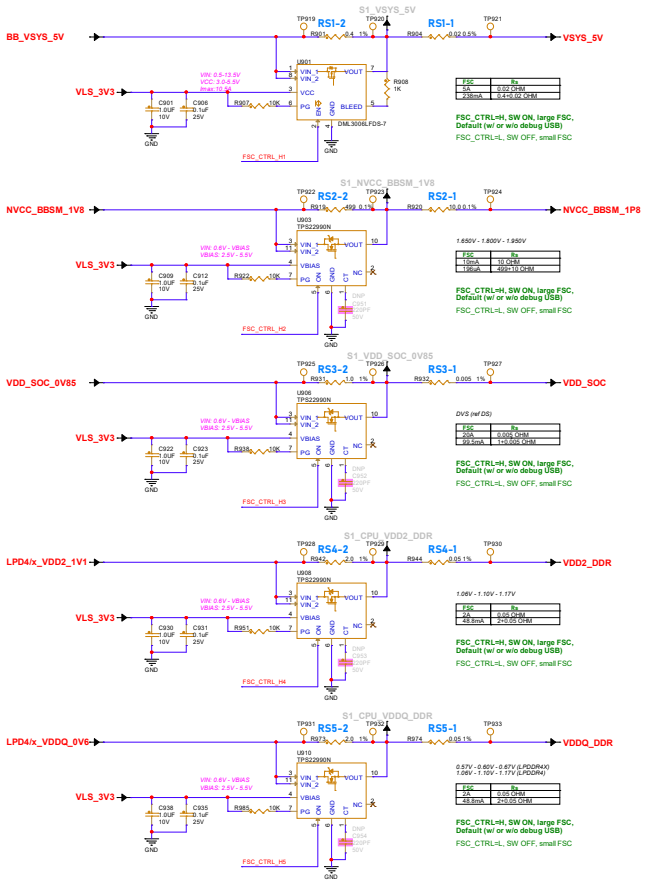
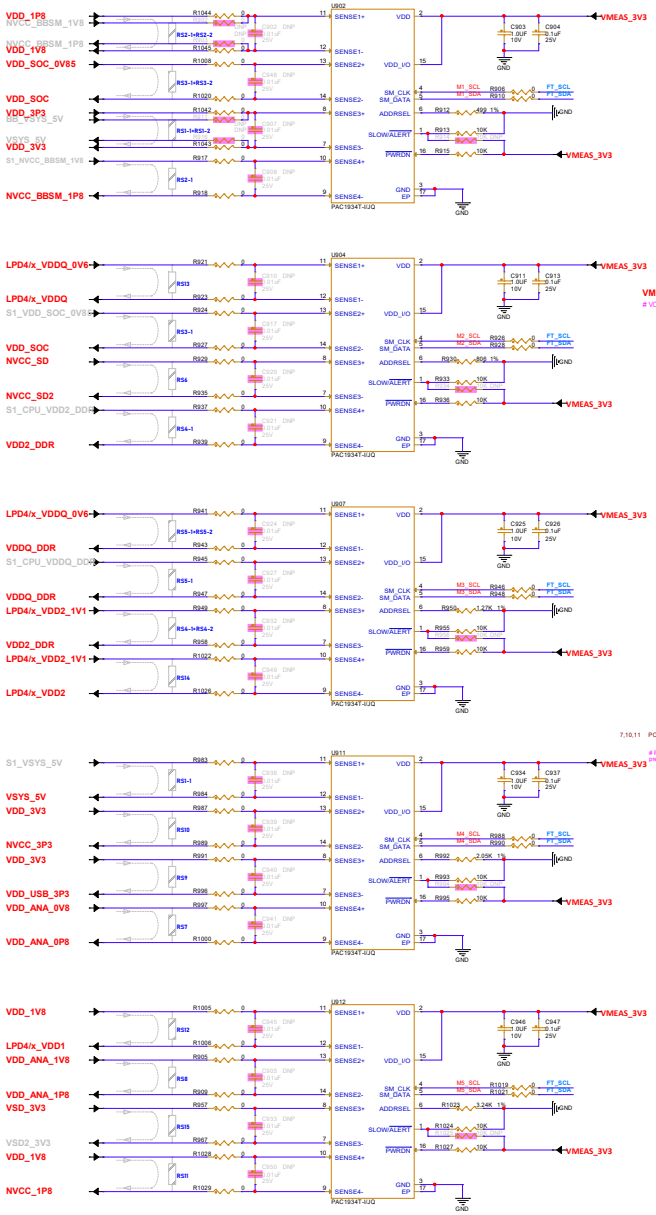
Currt Sense Range SEL



Curr Monitors



PAC1934T ADDR SEL RES

Resistor (1%)	SMBus Address
0 (TietoGND)	0010_000x
499	0010_001x
820	0010_010x
1,270	0010_011x
2,050	0010_100x
3,240	0010_101x
5,230	0010_110x
8,450	0010_111x
13,300	0011_000x
21,500	0011_001x
34,000	0011_010x
54,900	0011_011x
88,700	0011_100x
140,000	0011_101x
226,000	0011_110x
Tieto VDD	0011_111x

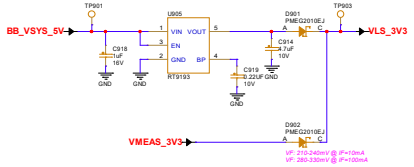
FT4232 I2C Address Table

Part	Type	Device	Address	Voltage
U902	M1	PAC1934T	0x11(0010001x)	3.3V
U904	M2	PAC1934T	0x12(0010010x)	3.3V
U907	M3	PAC1934T	0x13(0010011x)	3.3V
U911	M4	PAC1934T	0x14(0010100x)	3.3V
U912	M5	PAC1934T	0x15(0010101x)	3.3V
U909	IO EXP	PCA9672BS	0x20(0100000x)	3.3V
U913	T-sensor	PCT2075	0x48(1001000x)	3.3V

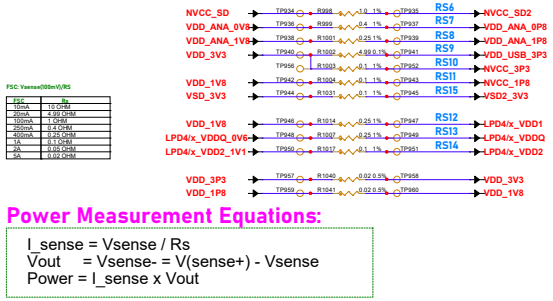
PWR MEAS I/F

IO EXP for PWR MEAS (SOM)

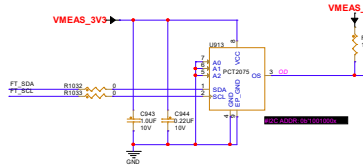
Always-on LDO for Ld SW



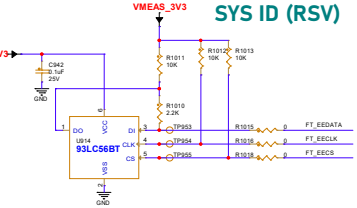
Fixed Curr Sense RES



SOM TEMP SENSOR



SYS ID (RSV)



Power Measurement Equations:

I_sense = Vsense / Rs
Vout = Vsense- = V(sense+) - Vsense
Power = I_sense x Vout

REMOVE THIS PAGE IF PWR MEAS NOT USED!!!

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Designed: NXP SE	Microcontroller Product Group, 6501 William Cannon Drive West, Austin, TX 78735-8598
Drawn by: NXP SE	Drawing Title: MCIMX93-SOM <MCIMX93-EVK>
Approved: <Approver>	Page Title: PWR MEAS
	Size: D; Document Number: SCH-51943 PDF: SPF-51943; Rev: B2
	Date: Monday, March 18, 2024; Sheet 12 of 14

NOTE:

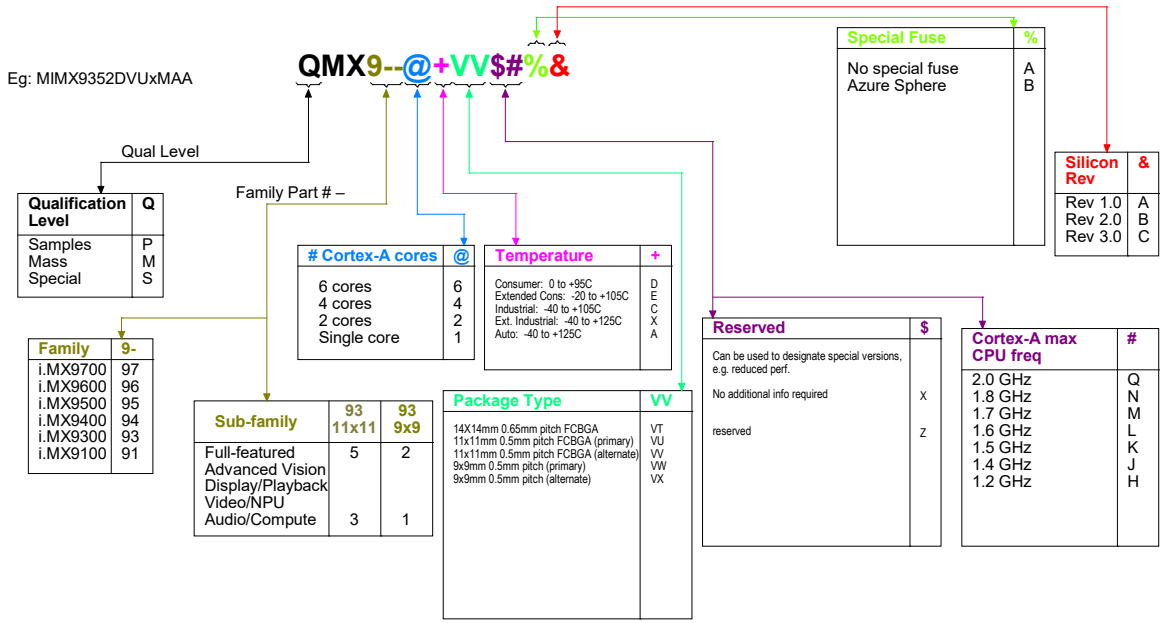
I2C DEV TABLE

BOARD	PART	DEVICE	I2C ADDR <7bit>	PORT	SPEED	VOL	DESCRIPTION
BB	U101	PCAL6524HEAZ	0x22 (0b'01000[10]x)	MX-I2C2 /I2C1	1MHz Fm+	3.3V	**IO EXP for IRQ/OUTPUT**
BB	U103	ADP5585ACPZ-00-R7	0x34 (0b'0110100x)	MX-I2C2 /I2C1	1MHz Fm+	3.3V	IO EXP for OUTPUT
BB	U301	PTN5110NHQZ	0x52 (0b'10100[10]x)	MX-I2C1 /I2C3/4	1MHz Fm+	3.3V	USB C PD PHY
BB	U307	PTN5110NHQZ	0x51 (0b'10100[01]x)	MX-I2C1 /I2C3/4	1MHz Fm+	3.3V	USB C PD PHY
BB	U401	PTN5110NHQZ	0x50 (0b'10100[00]x)	MX-I2C1 /I2C3/4	1MHz Fm+	3.3V	USB C PD PHY
BB	U402	NX20P3483UK	0x71 (0b'11100[01]x)	MX-I2C1 /I2C3/4	1MHz Fm+	3.3V	USB Load Switch
BB	U305	NX20P3483UK	0x73 (0b'11100[11]x)	MX-I2C1 /I2C3/4	1MHz Fm+	3.3V	USB Load Switch
BB	U1001	LSM6DSOXTR	0x6A (0b'110101[0]x)	MX-I2C1 /I2C3	I3C-12.5 Mbps/I2C-400KHz	3.3V	IMU (I3C support)
BB	U1201	WM8962BECSN/R	0x1A (0b'0011010x)	MX-I2C1 /I2C4	526KHz	3.3V	Audio CODEC
BB		AR0144	0x10 (0b'0010000x)	MX-I2C3	400KHz	3.3V	MIPI CSI Camera
BB				MX-I2C1 /I2C4	400KHz	3.3V	CTP/LCD <LVDS>
BB				MX-I2C1	400KHz	1.8V	CTP/LCD <MIPI DSI>
BB				MX-I2C1	400KHz	1.8V	M.2 / NGFF KEY-E
BB	U1409	PCA9655EMTTXG	0x21 (0b'0100001x)	FTDI-I2C	1MHz Fm+	3.3V	RDPM IO EXP
BB	U204	PAC1934T	0x16 (0b'0010110x)	FTDI-I2C	1MHz Fm+	3.3V	Base Board Power Monitor
BB	U1201	WM8960 (EVK REV A)	0x1A (0b'0011010x)	MX-I2C1 /I2C4	526KHz	3.3V	Audio CODEC
BB	U1004	PCF2131TF	0x53 (0b'1010011x)	MX-I2C3	400KHz	3.3V	Ext RTC
SOM	U701	PCA9451AHN	0x25 (0b'0100101x)	MX-I2C2	1MHz Fm+	3.3V	PMIC
SOM	U902	PAC1934T	0x11 (0b'0010001x)	FTDI-I2C	1MHz Fm+	3.3V	Power Monitor
SOM	U904	PAC1934T	0x12 (0b'0010010x)	FTDI-I2C	1MHz Fm+	3.3V	Power Monitor
SOM	U907	PAC1934T	0x13 (0b'0010011x)	FTDI-I2C	1MHz Fm+	3.3V	Power Monitor
SOM	U911	PAC1934T	0x14 (0b'0010100x)	FTDI-I2C	1MHz Fm+	3.3V	Power Monitor
SOM	U912	PAC1934T	0x15 (0b'0010101x)	FTDI-I2C	1MHz Fm+	3.3V	Power Monitor
SOM	U909	ADP5585ACPZ-00-R7	0x34 (0b'0110100x)	FTDI-I2C	1MHz Fm+	3.3V	Power Monitor
SOM	U913	PCT2075	0x48 (0b'1001000x)	FTDI-I2C	1MHz Fm+	3.3V	Power Monitor

MIPI CSI Camera:
- Camera: AR1335 — 0x36 (0b'0110110x)
- Camera: AR0144 — 0x10 (0b'0010000x)
- Ext ISP: AP1302 — 0x3C (0b'0111100x)
- IO EXP: ADP5585ACPZ-01-R7 — 0x34 (0b'0110100x)

CTP/LCD <MIPI DSI>:
- DSI->HDMI: ADV7535 — 0x3D (0b'0111101x)
- IO EXP: PCAL6408AEX1Z — 0x20 (0b'0100000x)

i.MX 9 Series Part Number Definition



Microcontroller Product Group
6501 William Cannon Drive West
Austin, TX 78735-8598

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ICAP Classification: CP: IUO: A PUBI:

Designer: NXP SE	Drawing Title: MCIMX93-SOM <MCIMX93-EVK>		
Drawn by: NXP SE	Page Title: NOTE		
Approved: <Approver>	Size C	Document Number SCH-51961 PDF: SPF-51961	Rev B2
	Date: Monday, March 18, 2024	Sheet 13 of 14	

i.MX93 IOMUX:

IOPAD	Alt0	Alt1	Alt2	Alt3	Alt4	Alt5	Alt6	Alt7	DEF MUX	PS	PE	IS	IO
RTC_XTALI	bbsmmix.RTC								bbsmmix.RTC				
RTC_XTALO													
PMIC_STBY_REQ	bbsmmix.PMIC_STBY_REQ								ccmsrcgpcmix.PMIC_STBY_REQ				
PMIC_ON_REQ	bbsmmix.PMIC_ON_REQ								bbsmmix.PMIC_ON_REQ				
ONOFF	bbsmmix.ONOFF								bbsmmix.ONOFF				
POR_B	bbsmmix.POR_B								bbsmmix.POR_B				
TAMPER0	bbsmmix.TAMPER0								bbsmmix.TAMPER0				
TAMPER1	bbsmmix.TAMPER1								bbsmmix.TAMPER1				
GPIO_IO00	gpio2.IO[0]	i2c3.SDA	isi.PCLK	lcdif.PCLK	spi6.PCS0	uart5.TX	i2c5.SDA	flexio1.FLEXIO[0]	gpio2.IO[0]				
GPIO_IO01	gpio2.IO[1]	i2c3.SCL	isi.D[0]	lcdif.DE	spi6.SIN	uart5.RX	i2c5.SCL	flexio1.FLEXIO[1]	gpio2.IO[1]				
GPIO_IO02	gpio2.IO[2]	i2c4.SDA	isi.FRAME_VALID	lcdif.VSYNC	spi6.SOUT	uart5.CTS_B	i2c6.SDA	flexio1.FLEXIO[2]	gpio2.IO[2]				
GPIO_IO03	gpio2.IO[3]	i2c4.SCL	isi.LINE_VALID	lcdif.HSYNC	spi6.SCK	uart5.RTS_B	i2c6.SCL	flexio1.FLEXIO[3]	gpio2.IO[3]				
GPIO_IO04	gpio2.IO[4]	tpm3.CH0	pdm.CLK	lcdif.D[0]	spi7.PCS0	uart6.TX	i2c6.SDA	flexio1.FLEXIO[4]	gpio2.IO[4]				
GPIO_IO05	gpio2.IO[5]	tpm4.CH0	pdm.BIT_STREAM[0]	lcdif.D[1]	spi7.SIN	uart6.RX	i2c6.SCL	flexio1.FLEXIO[5]	gpio2.IO[5]				
GPIO_IO06	gpio2.IO[6]	tpm5.CH0	pdm.BIT_STREAM[1]	lcdif.D[2]	spi7.SOUT	uart6.CTS_B	i2c7.SDA	flexio1.FLEXIO[6]	gpio2.IO[6]				
GPIO_IO07	gpio2.IO[7]	spi3.PCS1	isi.D[1]	lcdif.D[3]	spi7.SCK	uart6.RTS_B	i2c7.SCL	flexio1.FLEXIO[7]	gpio2.IO[7]				
GPIO_IO08	gpio2.IO[8]	spi3.PCS0	isi.D[2]	lcdif.D[4]	tpm6.CH0	uart7.TX	i2c7.SDA	flexio1.FLEXIO[8]	gpio2.IO[8]				
GPIO_IO09	gpio2.IO[9]	spi3.SIN	isi.D[3]	lcdif.D[5]	tpm3.EXTCLK	uart7.RX	i2c7.SCL	flexio1.FLEXIO[9]	gpio2.IO[9]				
GPIO_IO10	gpio2.IO[10]	spi3.SOUT	isi.D[4]	lcdif.D[6]	tpm4.EXTCLK	uart7.CTS_B	i2c8.SDA	flexio1.FLEXIO[10]	gpio2.IO[10]				
GPIO_IO11	gpio2.IO[11]	spi3.SCK	isi.D[5]	lcdif.D[7]	tpm5.EXTCLK	uart7.RTS_B	i2c8.SCL	flexio1.FLEXIO[11]	gpio2.IO[11]				
GPIO_IO12	gpio2.IO[12]	tpm3.CH2	pdm.BIT_STREAM[2]	lcdif.D[8]	spi8.PCS0	uart8.TX	i2c8.SDA	sai3.RX_SYNC	gpio2.IO[12]				
GPIO_IO13	gpio2.IO[13]	tpm4.CH2	pdm.BIT_STREAM[3]	lcdif.D[9]	spi8.SIN	uart8.RX	i2c8.SCL	flexio1.FLEXIO[13]	gpio2.IO[13]				
GPIO_IO14	gpio2.IO[14]	uart3.TX	isi.D[6]	lcdif.D[10]	spi8.SOUT	uart8.CTS_B	uart4.TX	flexio1.FLEXIO[14]	gpio2.IO[14]				
GPIO_IO15	gpio2.IO[15]	uart3.RX	isi.D[7]	lcdif.D[11]	spi8.SCK	uart8.RTS_B	uart4.RX	flexio1.FLEXIO[15]	gpio2.IO[15]				
GPIO_IO16	gpio2.IO[16]	sai3.TX_BCLK	pdm.BIT_STREAM[2]	lcdif.D[12]	uart3.CTS_B	spi4.PCS2	uart4.CTS_B	flexio1.FLEXIO[16]	gpio2.IO[16]				
GPIO_IO17	gpio2.IO[17]	sai3.MCLK	isi.D[8]	lcdif.D[13]	uart3.RTS_B	spi4.PCS1	uart4.RTS_B	flexio1.FLEXIO[17]	gpio2.IO[17]				
GPIO_IO18	gpio2.IO[18]	sai3.RX_BCLK	isi.D[9]	lcdif.D[14]	spi5.PCS0	spi4.PCS0	tpm5.CH2	flexio1.FLEXIO[18]	gpio2.IO[18]				
GPIO_IO19	gpio2.IO[19]	sai3.RX_SYNC	pdm.BIT_STREAM[3]	lcdif.D[15]	spi5.SIN	spi4.SIN	tpm6.CH2	sai3.TX_DATA[0]	gpio2.IO[19]				
GPIO_IO20	gpio2.IO[20]	sai3.RX_DATA[0]	pdm.BIT_STREAM[0]	lcdif.D[16]	spi5.SOUT	spi4.SOUT	tpm3.CH1	flexio1.FLEXIO[20]	gpio2.IO[20]				
GPIO_IO21	gpio2.IO[21]	sai3.TX_DATA[0]	pdm.CLK	lcdif.D[17]	spi5.SCK	spi4.SCK	tpm4.CH1	sai3.RX_BCLK	gpio2.IO[21]				
GPIO_IO22	gpio2.IO[22]	usdhc3.CLK	spdif1.IN	lcdif.D[18]	tpm5.CH1	tpm6.EXTCLK	i2c5.SDA	flexio1.FLEXIO[22]	gpio2.IO[22]				
GPIO_IO23	gpio2.IO[23]	usdhc3.CMD	spdif1.OUT	lcdif.D[19]	tpm6.CH1		i2c5.SCL	flexio1.FLEXIO[23]	gpio2.IO[23]				
GPIO_IO24	gpio2.IO[24]	usdhc3.DATA0		lcdif.D[20]	tpm3.CH3	dap.TDO_TRACESWO	spi6.PCS1	flexio1.FLEXIO[24]	gpio2.IO[24]				
GPIO_IO25	gpio2.IO[25]	usdhc3.DATA1	can2.TX	lcdif.D[21]	tpm4.CH3	dap.TCLK_SWCLK	spi7.PCS1	flexio1.FLEXIO[25]	gpio2.IO[25]				
GPIO_IO26	gpio2.IO[26]	usdhc3.DATA2	pdm.BIT_STREAM[1]	lcdif.D[22]	tpm5.CH3	dap.TDI	spi8.PCS1	sai3.TX_SYNC	gpio2.IO[26]				
GPIO_IO27	gpio2.IO[27]	usdhc3.DATA3	can2.RX	lcdif.D[23]	tpm6.CH3	dap.TMS_SWDIO	spi5.PCS1	flexio1.FLEXIO[27]	gpio2.IO[27]				
GPIO_IO28	gpio2.IO[28]	i2c3.SDA						flexio1.FLEXIO[28]	gpio2.IO[28]				
GPIO_IO29	gpio2.IO[29]	i2c3.SCL						flexio1.FLEXIO[29]	gpio2.IO[29]				
CCM_CLKO1	ccmsrcgpcmix.CLKO1				flexio1.FLEXIO[26]	gpio3.IO[26]			ccmsrcgpcmix.CLKO1				
CCM_CLKO2	ccmsrcgpcmix.CLKO2				flexio1.FLEXIO[27]	gpio3.IO[27]			ccmsrcgpcmix.CLKO2				
CCM_CLKO3	ccmsrcgpcmix.CLKO3				flexio2.FLEXIO[28]	gpio4.IO[28]			gpio4.IO[28]				
CCM_CLKO4	ccmsrcgpcmix.CLKO4				flexio2.FLEXIO[29]	gpio4.IO[29]			gpio4.IO[29]				
DAP_TDI	dap.TDI	mqs2.LEFT		can2.TX	flexio2.FLEXIO[30]	gpio3.IO[28]	uart5.RX		dap.TDI				
DAP_TMS_SWDIO	dap.TMS_SWDIO				flexio2.FLEXIO[31]	gpio3.IO[29]	uart5.RTS_B		dap.TMS_SWDIO				
DAP_TCLK_SWCLK	dap.TCLK_SWCLK				flexio1.FLEXIO[30]	gpio3.IO[30]	uart5.CTS_B		dap.TCLK_SWCLK				
DAP_TDO_TRACESWO	dap.TDO_TRACESWO	mqs2.RIGHT		can2.RX	flexio1.FLEXIO[31]	gpio3.IO[31]	uart5.TX		dap.TDO_TRACESWO				
ENET1_MDC	enet_qos.MDC	uart3.DCB_B	i3c2.SCL	usb1.OTG_ID	flexio2.FLEXIO[0]	gpio4.IO[0]			gpio4.IO[0]				
ENET1_MDIO	enet_qos.MDIO	uart3.RIN_B	i3c2.SDA	usb1.OTG_PWR	flexio2.FLEXIO[1]	gpio4.IO[1]			gpio4.IO[1]				
ENET1_TD3	enet_qos.RGMII_TD3		can2.TX	usb2.OTG_ID	flexio2.FLEXIO[2]	gpio4.IO[2]			gpio4.IO[2]				
ENET1_TD2	enet_qos.RGMII_TD2	enet_qos.TX_CLK/.ENET_REF_CLK_ROOT	can2.RX	usb2.OTG_OC	flexio2.FLEXIO[3]	gpio4.IO[3]			gpio4.IO[3]				
ENET1_TD1	enet_qos.RGMII_TD1	uart3.RTS_B	i3c2.PUR	usb1.OTG_OC	flexio2.FLEXIO[4]	gpio4.IO[4]	i3c2.PUR_B		gpio4.IO[4]				
ENET1_TD0	enet_qos.RGMII_TD0	uart3.TX			flexio2.FLEXIO[5]	gpio4.IO[5]			gpio4.IO[5]				
ENET1_TX_CTL	enet_qos.RGMII_TX_CTL	uart3.DTR_B			flexio2.FLEXIO[6]	gpio4.IO[6]			gpio4.IO[6]				
ENET1_TXC	enet_qos.RGMII_TXC	enet_qos.TX_ER			flexio2.FLEXIO[7]	gpio4.IO[7]			gpio4.IO[7]				
ENET1_RX_CTL	enet_qos.RGMII_RX_CTL	uart3.DSR_B		usb2.OTG_PWR	flexio2.FLEXIO[8]	gpio4.IO[8]			gpio4.IO[8]				
ENET1_RXC	enet_qos.RGMII_RXC	enet_qos.RX_ER			flexio2.FLEXIO[9]	gpio4.IO[9]			gpio4.IO[9]				
ENET1_RD0	enet_qos.RGMII_RD0	uart3.RX			flexio2.FLEXIO[10]	gpio4.IO[10]			gpio4.IO[10]				
ENET1_RD1	enet_qos.RGMII_RD1	uart3.CTS_B		lptmr2.ALT1	flexio2.FLEXIO[11]	gpio4.IO[11]			gpio4.IO[11]				
ENET1_RD2	enet_qos.RGMII_RD2			lptmr2.ALT2	flexio2.FLEXIO[12]	gpio4.IO[12]			gpio4.IO[12]				
ENET1_RD3	enet_qos.RGMII_RD3		wakeupmix.flexspi_usdhc_tester_trigger	lptmr2.ALT3	flexio2.FLEXIO[13]	gpio4.IO[13]			gpio4.IO[13]				
ENET2_MDC	enet2.MDC	uart4.DCB_B	sai2.RX_SYNC		flexio2.FLEXIO[14]	gpio4.IO[14]			gpio4.IO[14]				
ENET2_MDIO	enet2.MDIO	uart4.RIN_B	sai2.RX_BCLK		flexio2.FLEXIO[15]	gpio4.IO[15]			gpio4.IO[15]				
ENET2_TD3	enet2.RGMII_TD3		sai2.RX_DATA[0]		flexio2.FLEXIO[16]	gpio4.IO[16]			gpio4.IO[16]				
ENET2_TD2	enet2.RGMII_TD2	enet2.TX_CLK/ENET_REF_CLK_ROOT	sai2.RX_DATA[1]		flexio2.FLEXIO[17]	gpio4.IO[17]			gpio4.IO[17]				
ENET2_TD1	enet2.RGMII_TD1	uart4.RTS_B	sai2.RX_DATA[2]		flexio2.FLEXIO[18]	gpio4.IO[18]			gpio4.IO[18]				
ENET2_TD0	enet2.RGMII_TD0	uart4.TX	sai2.RX_DATA[3]		flexio2.FLEXIO[19]	gpio4.IO[19]			gpio4.IO[19]				
ENET2_TX_CTL	enet2.RGMII_TX_CTL	uart4.DTR_B	sai2.TX_SYNC		flexio2.FLEXIO[20]	gpio4.IO[20]			gpio4.IO[20]				
ENET2_TXC	enet2.RGMII_TXC	enet2.TX_ER	sai2.TX_BCLK		flexio2.FLEXIO[21]	gpio4.IO[21]			gpio4.IO[21]				
ENET2_RX_CTL	enet2.RGMII_RX_CTL	uart4.DSR_B	sai2.TX_DATA[0]		flexio2.FLEXIO[22]	gpio4.IO[22]			gpio4.IO[22]				
ENET2_RXC	enet2.RGMII_RXC	enet2.RX_ER	sai2.TX_DATA[1]		flexio2.FLEXIO[23]	gpio4.IO[23]			gpio4.IO[23]				
ENET2_RD0	enet2.RGMII_RD0	uart4.RX	sai2.TX_DATA[2]		flexio2.FLEXIO[24]	gpio4.IO[24]			gpio4.IO[24]				
ENET2_RD1	enet2.RGMII_RD1	spdif1.IN	sai2.TX_DATA[3]		flexio2.FLEXIO[25]	gpio4.IO[25]			gpio4.IO[25]				
ENET2_RD2	enet2.RGMII_RD2	uart4.CTS_B	sai2.MCLK	mqs2.RIGHT	flexio2.FLEXIO[26]	gpio4.IO[26]			gpio4.IO[26]				
ENET2_RD3	enet2.RGMII_RD3	spdif1.OUT	spdif1.IN	mqs2.LEFT	flexio2.FLEXIO[27]	gpio4.IO[27]			gpio4.IO[27]				
SD1_CLK	usdhc1.CLK				flexio1.FLEXIO[8]	gpio3.IO[8]			gpio3.IO[8]				
SD1_CMD	usdhc1.CMD				flexio1.FLEXIO[9]	gpio3.IO[9]			gpio3.IO[9]				
SD1_DATA0	usdhc1.DATA0				flexio1.FLEXIO[10]	gpio3.IO[10]			gpio3.IO[10]				
SD1_DATA1	usdhc1.DATA1				flexio1.FLEXIO[11]	gpio3.IO[11]	ccmsrcgpcmix.INT_BOOT		gpio3.IO[11]				
SD1_DATA2	usdhc1.DATA2				flexio1.FLEXIO[12]	gpio3.IO[12]	ccmsrcgpcmix.PMIC_READY		gpio3.IO[12]				
SD1_DATA3	usdhc1.DATA3	flexspi.A_SS1_B			flexio1.FLEXIO[13]	gpio3.IO[13]			gpio3.IO[13]				
SD1_DATA4	usdhc1.DATA4	flexspi.A_DATA[4]			flexio1.FLEXIO[14]	gpio3.IO[14]			gpio3.IO[14]				
SD1_DATA5	usdhc1.DATA5	flexspi.A_DATA[5]	usdhc1.RESET_B		flexio1.FLEXIO[15]	gpio3.IO[15]			gpio3.IO[15]				
SD1_DATA6	usdhc1.DATA6	flexspi.A_DATA[6]	usdhc1.CD_B		flexio1.FLEXIO[16]	gpio3.IO[16]			gpio3.IO[16]				
SD1_DATA7	usdhc1.DATA7	flexspi.A_DATA[7]	usdhc1.WP		flexio1.FLEXIO[17]	gpio3.IO[17]			gpio3.IO[17]				
SD1_STROBE	usdhc1.STROBE	flexspi.A_DQS			flexio1.FLEXIO[18]	gpio3.IO[18]			gpio3.IO[18]				
SD2_VSELECT	usdhc2.VSELECT	usdhc2.WP	lptmr2.ALT3		flexio1.FLEXIO[19]	gpio3.IO[19]	ccmsrcgpcmix.EXT_CLK1		gpio3.IO[19]				
SD3_CLK	usdhc3.CLK	flexspi.A_SCLK			flexio1.FLEXIO[20]	gpio3.IO[20]			gpio3.IO[20]				
SD3_CMD	usdhc3.CMD	flexspi.A_SS0_B			flexio1.FLEXIO[21]	gpio3.IO[21]			gpio3.IO[21]				
SD3_DATA0	usdhc3.DATA0	flexspi.A_DATA[0]			flexio1.FLEXIO[22]	gpio3.IO[22]			gpio3.IO[22]				
SD3_DATA1	usdhc3.DATA1	flexspi.A_DATA[1]			flexio1.FLEXIO[23]	gpio3.IO[23]			gpio3.IO[23]				
SD3_DATA2	usdhc3.DATA2	flexspi.A_DATA[2]			flexio1.FLEXIO[24]	gpio3.IO[24]			gpio3.IO[24]				
SD3_DATA3	usdhc3.DATA3	flexspi.A_DATA[3]			flexio1.FLEXIO[25]	gpio3.IO[25]			gpio3.IO[25]				
SD2_CD_B	usdhc2.CD_B	enet_qos.1588_EVENT0_IN	i3c2.SCL		flexio1.FLEXIO[0]	gpio3.IO[0]	ccmsrcgpcmix.TESTER_ACK		gpio3.IO[0]				
SD2_CLK	usdhc2.CLK	enet_qos.1588_EVENT0_OUT	i3c2.SDA		flexio1.FLEXIO[1]	gpio3.IO[1]	ccmsrcgpcmix.OBSERVE0		gpio3.IO[1]				
SD2_CMD	usdhc2.CMD	enet2.1588_EVENT0_IN	i3c2.PUR	i3c2.PUR_B	flexio1.FLEXIO[2]	gpio3.IO[2]	ccmsrcgpcmix.OBSERVE1		gpio3.IO[2]				
SD2_DATA0	usdhc2.DATA0	enet2.1588_EVENT0_OUT	can2.TX		flexio1.FLEXIO[3]	gpio3.IO[3]	ccmsrcgpcmix.OBSERVE2		gpio3.IO[3]				
SD2_DATA1	usdhc2.DATA1	enet2.1588_EVENT1_IN	can2.RX		flexio1.FLEXIO[4]	gpio3.IO[4]	ccmsrcgpcmix.WAIT		gpio3.IO[4]				
SD2_DATA2	usdhc2.DATA2	enet2.1588_EVENT1_OUT	mqs2.RIGHT		flexio1.FLEXIO[5]	gpio3.IO[5]	ccmsrcgpcmix.STOP		gpio3.IO[5]				
SD2_DATA3	usdhc2.DATA3	lptmr2.ALT1	mqs2.LEFT		flexio1.FLEXIO[6]	gpio3.IO[6]	ccmsrcgpcmix.EARLY_RESET		gpio3.IO[6]				
SD2_RESET_B	usdhc2.RESET_B	lptmr2.ALT2			flexio1.FLEXIO[7]	gpio3.IO[7]	ccmsrcgpcmix.SYSTEM_RESET		gpio3.IO[7]				
I2C1_SCL	i2c1.SCL	i3c1.SCL	uart1.DCB_B	tpm2.CH0		gpio1.IO[0]			gpio1.IO[0]				
I2C1_SDA	i2c1.SDA	i3c1.SDA	uart1.RIN_B	tpm2.CH1		gpio1.IO[1]			gpio1.IO[1]				
I2C2_SCL	i2c2.SCL	i3c1.PUR	uart2.DCB_B	tpm2.CH2	sai1.RX_SYNC	gpio1.IO[2]	i3c1.PUR_B		gpio1.IO[2]				
I2C2_SDA	i2c2.SDA		uart2.RIN_B	tpm2.CH3	sai1.RX_BCLK	gpio1.IO[3]			gpio1.IO[3]				
UART1_RXD	uart1.RX	seco.RX	spi2.SIN	tpm1.CH0		gpio1.IO[4]			gpio1.IO[4]				
UART1_TXD	uart1.TX	seco.TX	spi2.PCS0	tpm1.CH1		gpio1.IO[5]/ccmsrcgpcmix.BOOT_MODE[0]			gpio1.IO[5]/ccmsrcgpcmix.BOOT_MODE[0]				
UART2_RXD	uart2.RX	uart1.CTS_B	spi2.SOUT	tpm1.CH2	sai1.MCLK	gpio1.IO[6]			gpio1.IO[6]				
UART2_TXD	uart2.TX	uart1.RTS_B	spi2.SCK	tpm1.CH3		gpio1.IO[7]/ccmsrcgpcmix.BOOT_MODE[1]			gpio1.IO[7]/ccmsrcgpcmix.BOOT_MODE[1]				
PDM_CLK	pdm.CLK	mqs1.LEFT			lptmr1.ALT1	gpio1.IO[8]	can1.TX		gpio1.IO[8]				
PDM_BIT_STREAM0	pdm.BIT_STREAM[0]	mqs1.RIGHT	spi1.PCS1	tpm1.EXTCLK	lptmr1.ALT2	gpio1.IO[9]	can1.RX		gpio1.IO[9]				
PDM_BIT_STREAM1	pdm.BIT_STREAM[1]	m33.NMI	spi2.PCS1	tpm2.EXTCLK	lptmr1.ALT3	gpio1.IO[10]	ccmsrcgpcmix.EXT_CLK1		gpio1.IO[10]				
SAI1_TXFS	sai1.TX_SYNC	sai1.TX_DATA[1]	spi1.PCS0	uart2.DTR_B	mqs1.LEFT	gpio1.IO[11]/ccmsrcgpcmix.BOOT_MODE[2]			gpio1.IO[11]/ccmsrcgpcmix.BOOT_MODE[2]				
SAI1_TXC	sai1.TX_BCLK	uart2.CTS_B	spi1.SIN	uart1.DSR_B	can1.RX	gpio1.IO[12]			gpio1.IO[12]				
SAI1_TXD0	sai1.TX_DATA[0]	uart2.RTS_B	spi1.SCK	uart1.DTR_B	can1.TX	gpio1.IO[13]/ccmsrcgpcmix.BOOT_MODE[3]			gpio1.IO[13]/ccmsrcgpcmix.BOOT_MODE[3]				
SAI1_RXD0	sai1.RX_DATA[0]	sai1.MCLK	spi1.SOUT	uart2.DSR_B	mqs1.RIGHT	gpio1.IO[14]			gpio1.IO[14]				
WDOG_ANY	wdog1.WDOG_ANY					gpio1.IO[15]			gpio1.IO[15]				
CLKIN1	anamix.CLKIN1	anamix.esd_diode											
CLKIN2	anamix.CLKIN2	anamix.atx											
XTALI_24M	anamix.xtali_24M												
XTALO_24M	anamix.xtalo_24M												
ADC_IN0	anamix.adc_in0												
ADC_IN1	anamix.adc_in1												
ADC_IN2	anamix.adc_in2												
ADC_IN3	anamix.adc_in3												

Microcontroller Product Group
6501 William Cannon Drive West
Austin, TX 78735-8598

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ICAP Classification: CP: IUO: A PUBt:

Designer: NXP SE	Drawing Title: MCIMX93-SOM <MCIMX93-EVK>	
Drawn by: NXP SE	Page Title: IOMUX	
Approved: <Approver>	Size: Custom	Document Number: SCH-51961 PDF: SPF-51961 — Rev: B2
	Date: Monday, March 18, 2024	Sheet 14 of 14