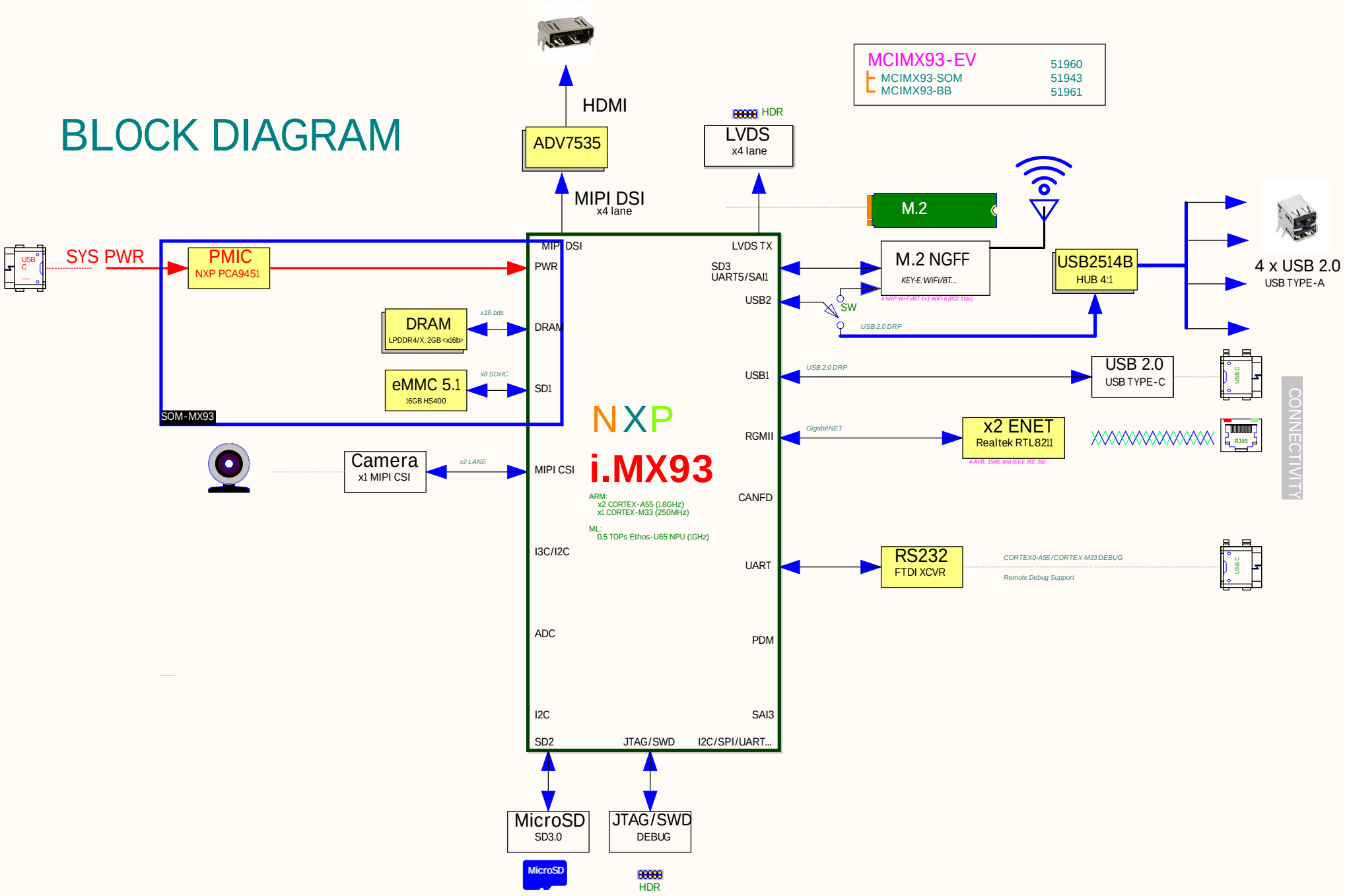
BLOCK DIAGRAM



i.MX93 EVK PWR TREE

When PER_12V is required, VBUS_IN must be at least 12V!!!

USB C SNK PD

VBUS_IN

12-20V

DCDC BUCK

MPS MP8759GD

VSYS

5V/3A

DCDC_5V

5V/5A

DCDC BUCK

MPS MP2147

VEXT_3V3

3.3V/4A

Load SW

MOSFET

VDD_5V

5V/3A

DCDC BUCK

MPS MP2263GD

PER_12V

12V/3A

PMIC: PCA9451A CFG

SEQ		REGULATOR	VOL (V)	MAX I (mA)
1		LDO1	1.8	10
-				
2	T1	BUCK1/3 DP	0.85	4000
3	T2	LDO4	0.8	200
4				
5	T4	BUCK5	1.8	2000
6	T5	BUCK6	1.1	1500
7	T6	BUCK2	0.6	2000
8	T7	BUCK4	3.3	3000
8	T7	Load Switch	-	400
9	T8	LDO5	1.8/3.3	150
-	-			
12		POR_B	--	--

SoC: i.MX93

ITEM	PWR RAIL	TYP VOL(V)	REQ I (mA)
1	NVCC_BBSM_1V8	1.8	2
PMIC_ON_REQ			
2	VDD_SOC	DVS	Ref to DS
3	VDD_ANA_0P8	0.8	186
4	RFU: VDD_ANA_1P8 (250mA)	1.8	250
4	VDD_ANA_1P8/NVCC_WAKEUP	1.8	389
5	VDD2_DDR/LPD4 VDDQ	1.1	676
6	VDDQ_DDR (0.6V for LPD4x)	0.6	360
7	NVCC_GPIO/VDD_USB_3P3	3.3	SYS
7	SD_CARD	3.3	
8	NVCC_SD2	1.8/3.3	
-			
POR_B			

LPDDR4/X

VDD1 <1.8V>
VDD2 <1.1V>
VDDQ <0.6V/1.1V>

eMMC

VCCQ <1.8V>
VCC <3.3V>

MicroSD

VCC <3.3V>

ETHERNET

DVDD_REG <1.8V>
AVDD/DVDD <3.3V>

USB C DRP/ A HOST

VBUS <5V>

M.2 KEY-E

3.3V

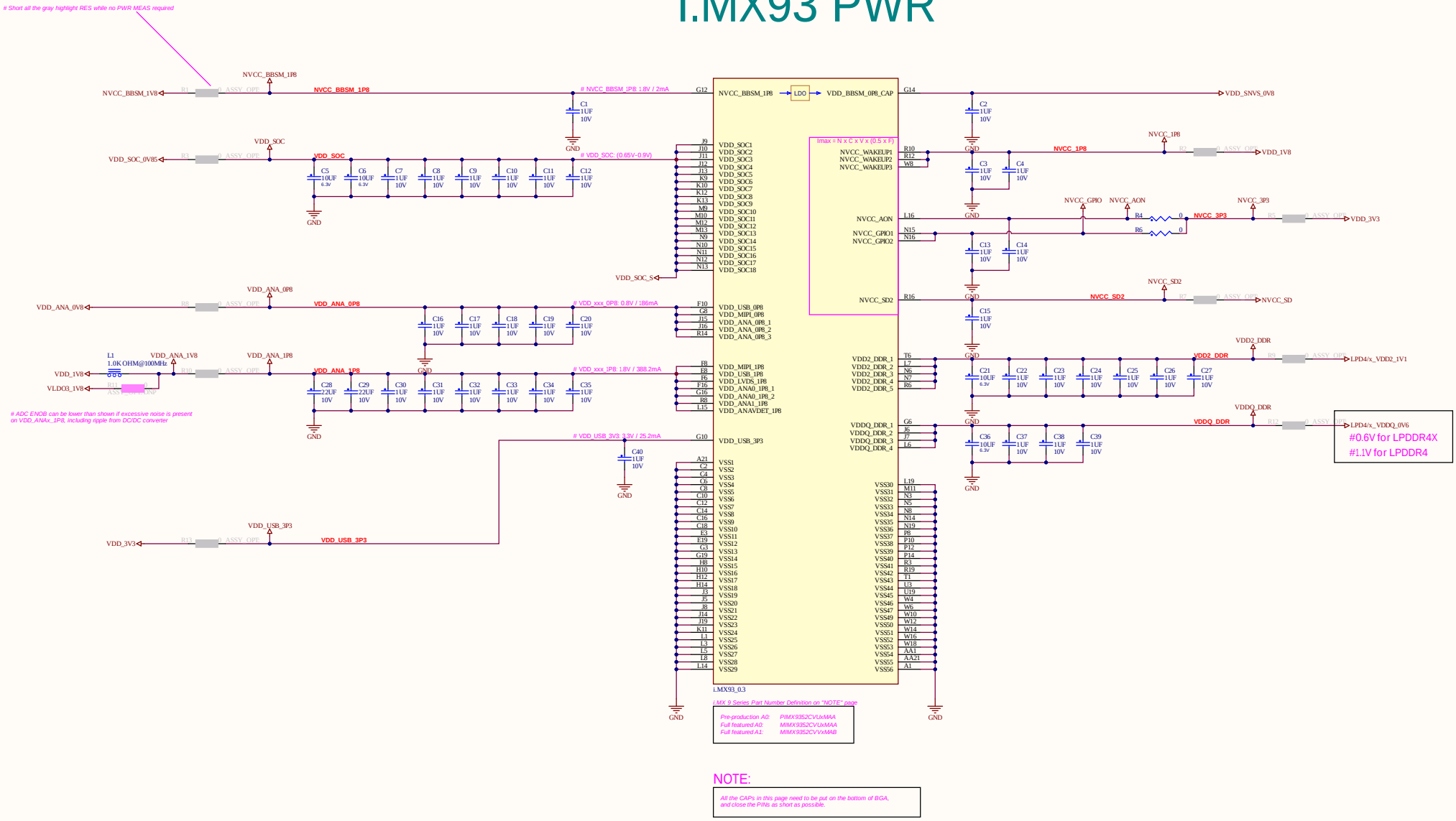
MIPI DSI / LVDS

3.3V
5V
12V

MIPI CSI

3.3V

i.MX93 PWR



NOTE:

All the CAPs in this page need to be put on the bottom of BGA, and close the PINs as short as possible.

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Drawn by: NXP SE	Page Title: CPU PWR
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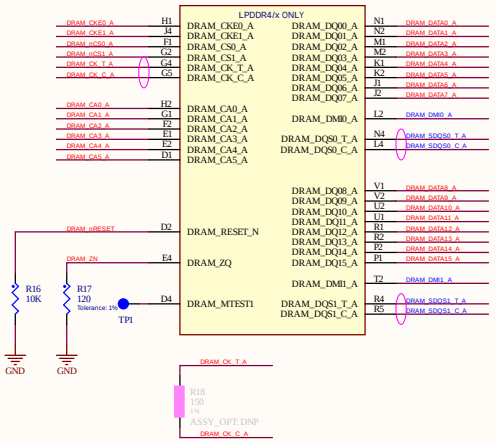
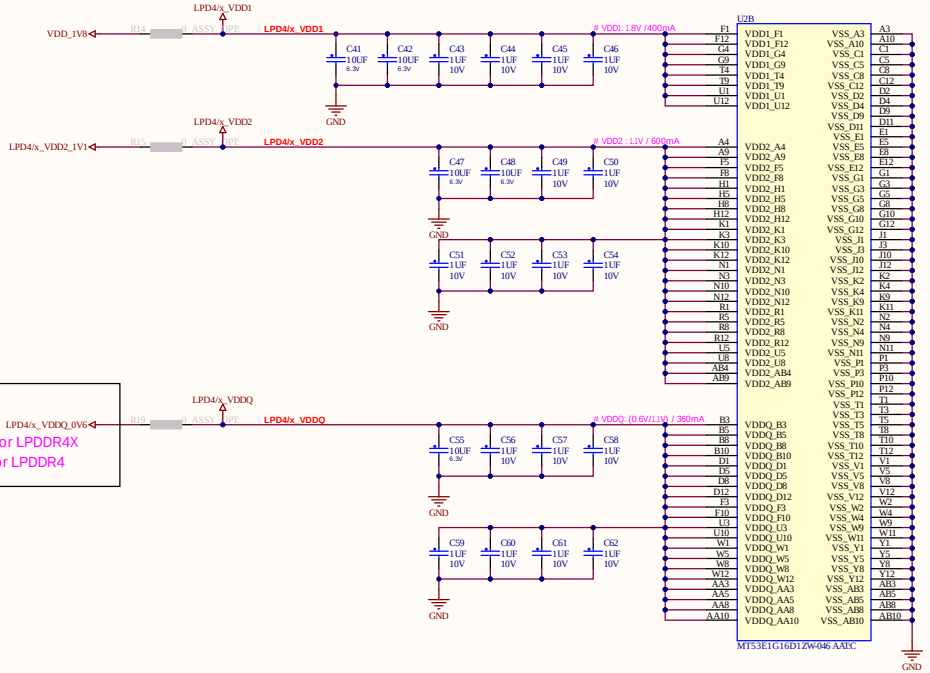
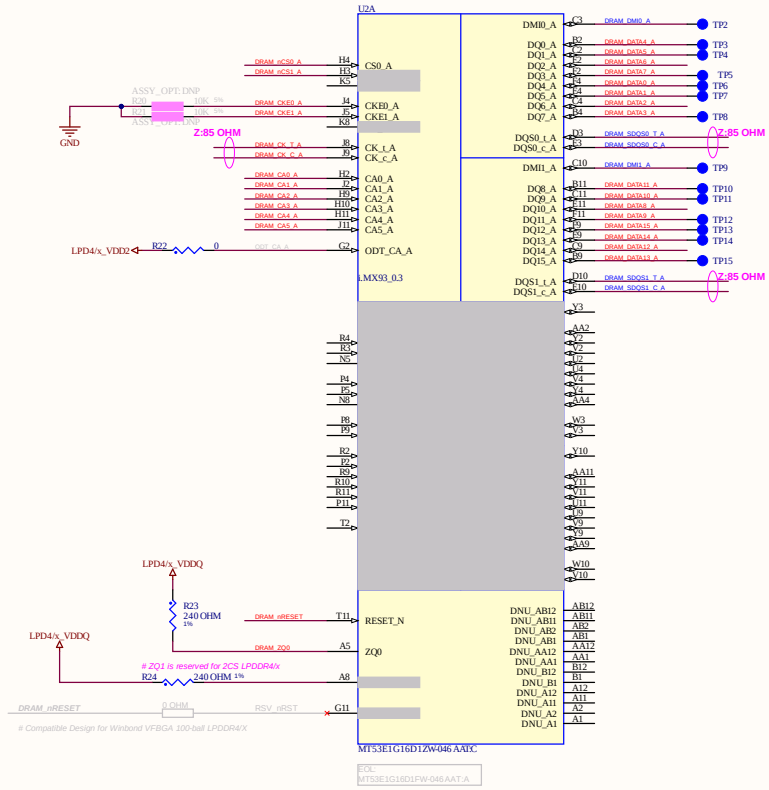
	Date: *; Sheet: 4 of 14

LPDDR4/X





LPDDR4X: 2GB (x16)



Power Supply Voltage Sequence:

RESET_n is held LOW.
VDD1 >= VDD2
VDD2 >= VDDQ-200mV

Power ramp duration tINIT0 (Tb˚CTa) must not exceed 20ms.

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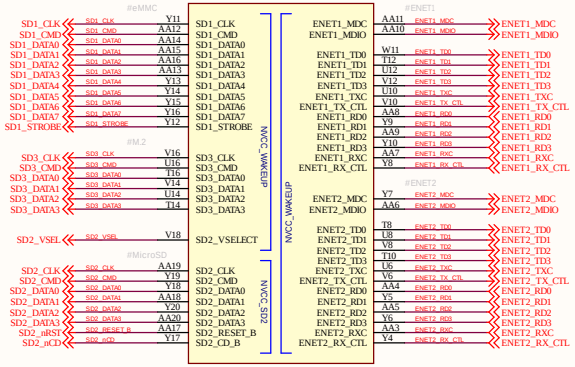
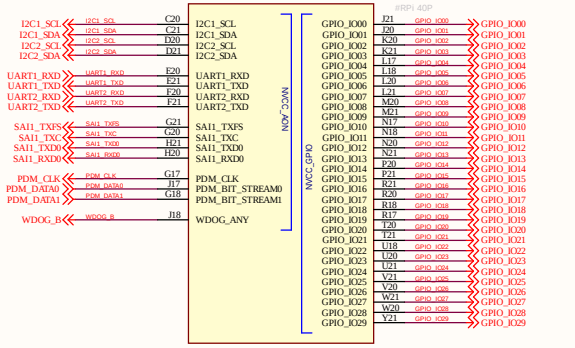
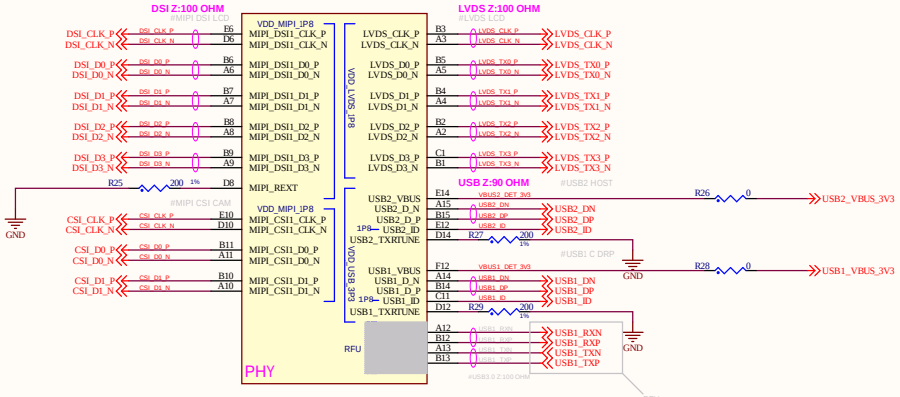
Drawn by: NXP SE	Page Title: DDR4	
Approved:	Size: NC	Document Number: SCH-51943 PDF: SPF-51943 Rev: B2
	Date: *	Sheet: 5 of 14

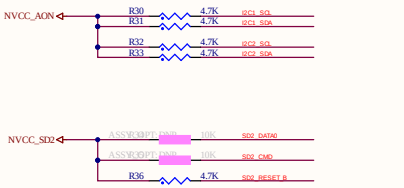
i.MX93 IO/PHY





i.MX93_0.3





i.MX93_0.3

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Drawn by: NXP SE	Page Title: CPU IO
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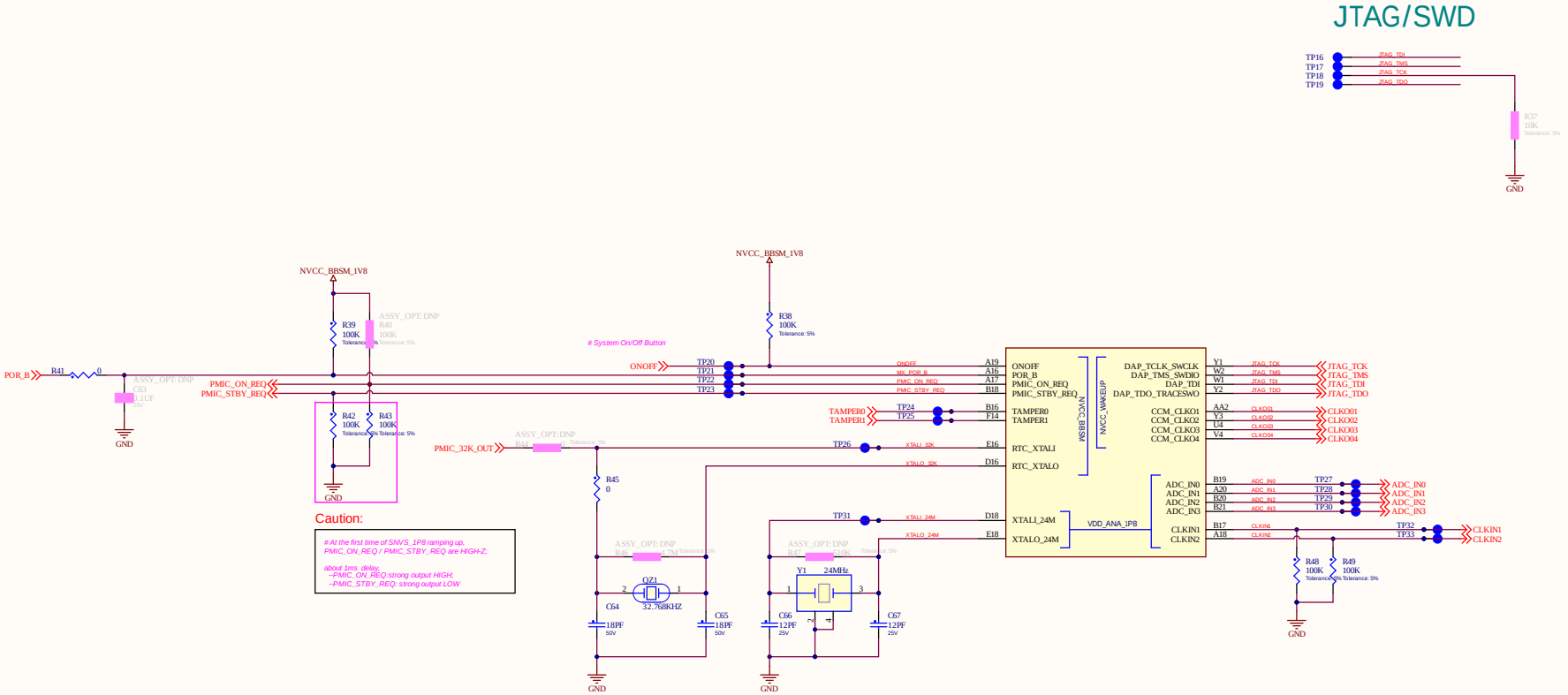
Date: *	Sheet 6 of 14

i.MX93 MISC



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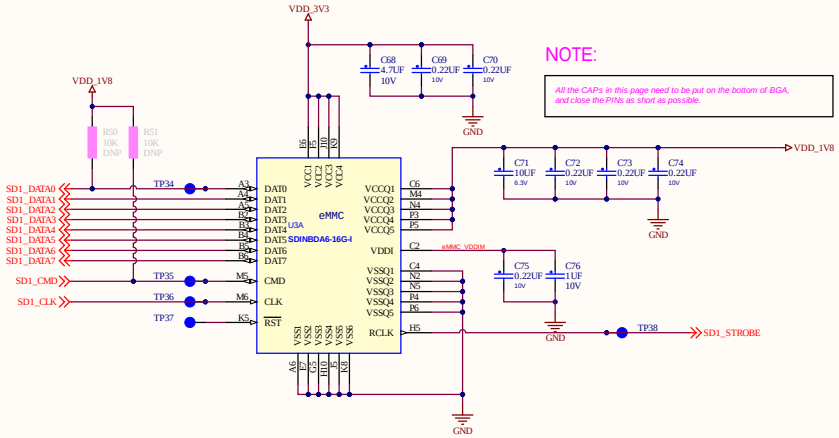
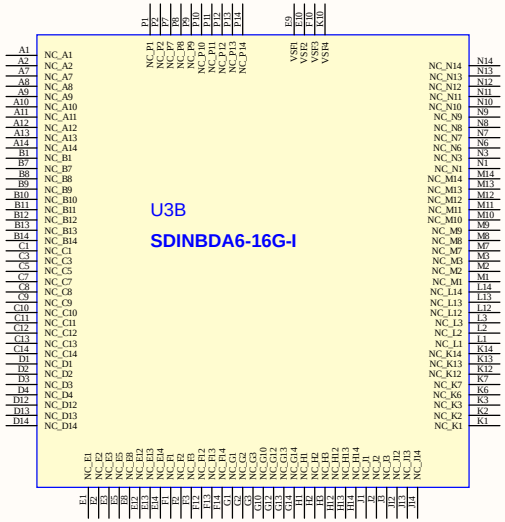
FLASH: eMMC <5.1>





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Drawn by: NXP SE	Page Title: **eMMC**
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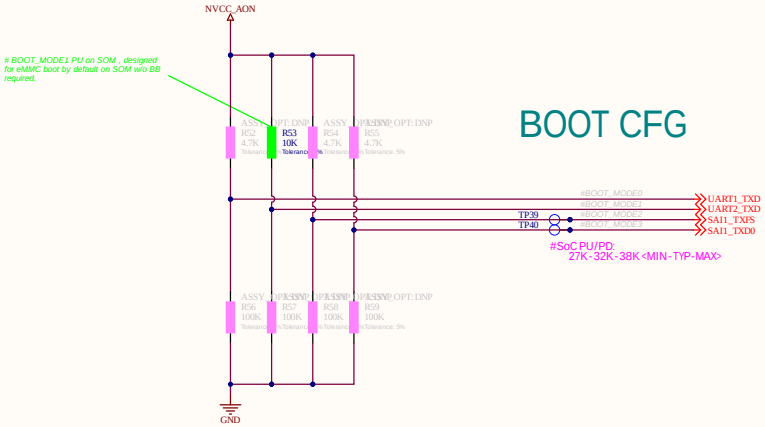
	Date: *; Sheet: 8 of 14

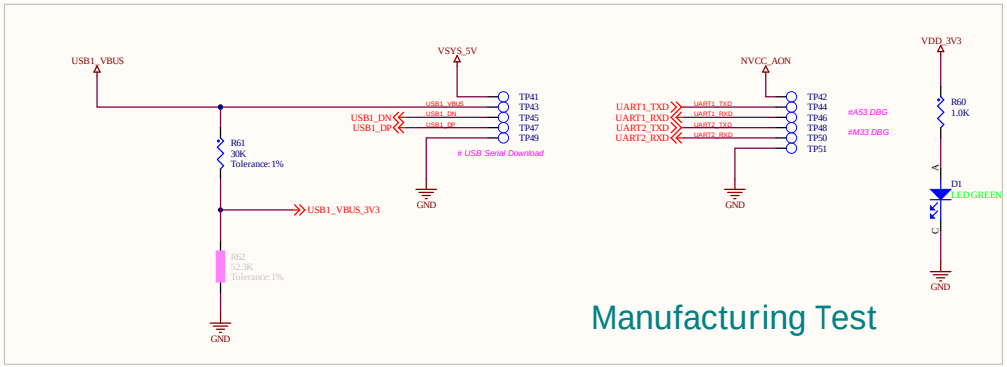
Boot Mode and CFG Switch

i.MX93 BOOT MODE

BOOT_MODE[3:0]	BOOT CORE	BOOT DEVICE	COMMENT
0000	Cortex-A55	From internal fuses	
0001	Cortex-A55	Serial Downloader	USB1/2
0010	Cortex-A55	USDHC1 8-bit eMMC 5.1	
0011	Cortex-A55	USDHC2 4-bit SD3.0	
0100	Cortex-A55	FlexSPI Serial NOR	with SFDP (JESD-216) discoverable parameters
0101	Cortex-A55	FlexSPI Serial NAND 2K page	
0110	Cortex-A55	Infinite Loop	
0111	Cortex-A55	Test Mode	
1000	Cortex-M33	From internal fuses	
1001	Cortex-M33	Serial Downloader	USB1
1010	Cortex-M33	USDHC1 8-bit eMMC 5.1	
1011	Cortex-M33	USDHC2 4-bit SD3.0	
1100	Cortex-M33	FlexSPI Serial NOR	with SFDP (JESD-216) discoverable parameters
1101	Cortex-M33	FlexSPI Serial NAND 2K page	
1110	Cortex-M33	Infinite Loop	
1111	Cortex-M33	Test Mode	



BOOT CFG



Manufacturing Test

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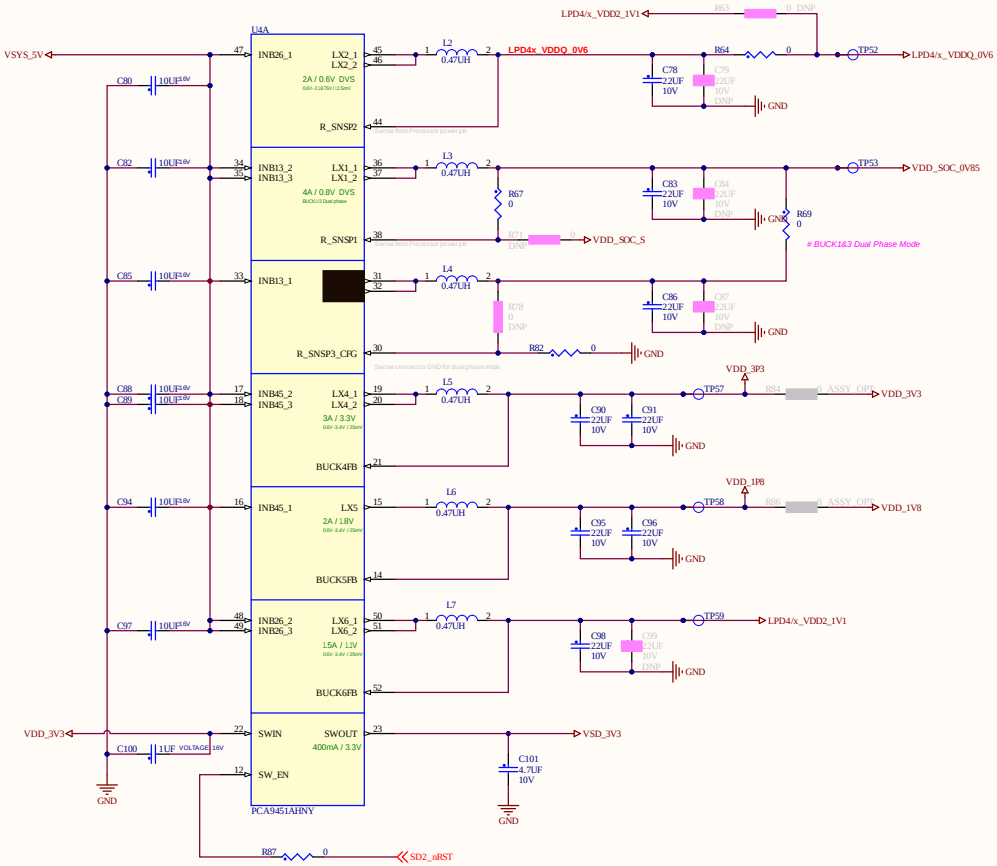
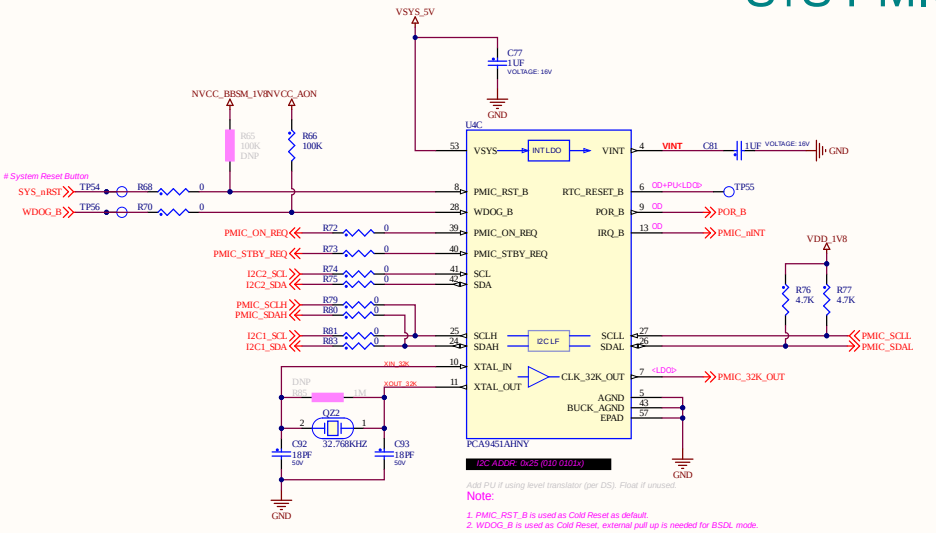
SYS PMIC





PMIC: PCA9451A CFG

SEQ	tstep=2ms	REGULATOR	VOL (V)	MAX I (mA)	PWR RAIL	TYP VOL(V)	REQ I (mA)
1		LDO1	1.8	10	NVCC_BBSM_1V8	1.8	2
-							
-					PMIC_ON_REQ		
2	T1	BUCK1/3 DP	0.85	4000	VDD_SOC	DVS	Ref to DS
-							
3	T2	LDO4	0.8	200	VDD_ANA_0P8 VDD_MIPI_0P8 VDD_USB_0P8	0.8	186
4							
5	T4	BUCK5	1.8	2000	VDD_ANAx_1P8 VDD_LVDS_1P8 VDD_MIPI_1P8 VDD_USB_1P8 NVCC_GPIO	1.8	1040 PERI INCLUDE
6	T5	BUCK6	1.1	1500	VDD2_DDR VDDQ_DDR (1.1V for	1.1	676
7	T6	BUCK2	0.6	2000	VDDQ_DDR (0.6V for LPD4x)	0.6	360
8	T7	BUCK4	3.3	3000	NVCC_GPIO VDD_USB_3P3	3.3	2870 PERI INCLUDE
8	T7	Load Switch	-	400	SD_CARD (from BUCK4)	3.3	
9	T8	LDO5	1.8/3.3	150	NVCC_SD2	1.8/3.3	
-	-						
12		POR_B	--	--	POR_B		

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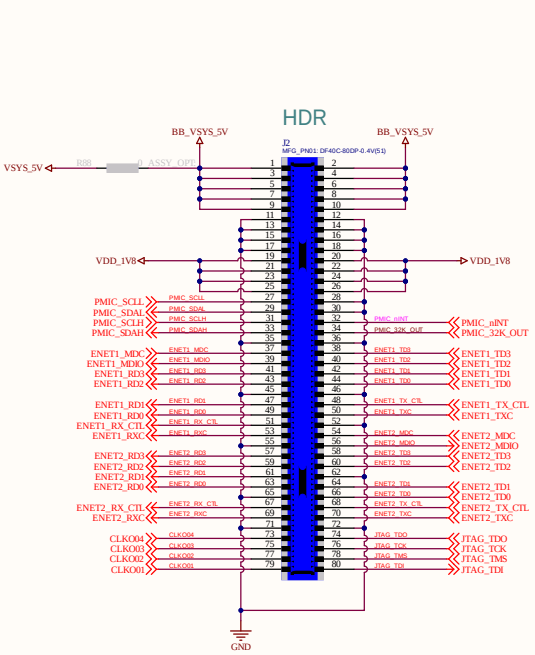
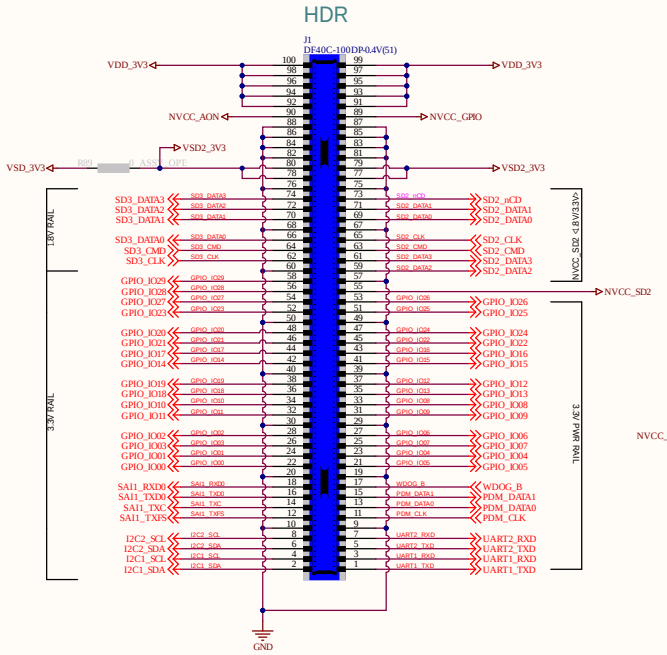
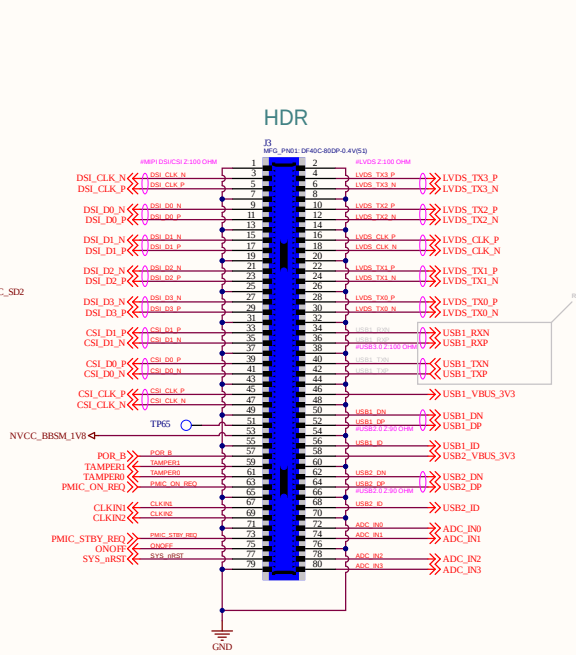
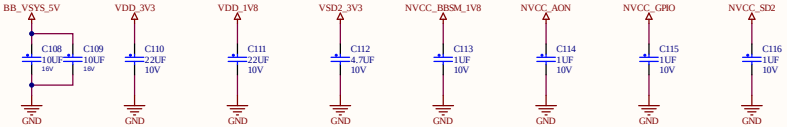
B2B CN for CPU SOM

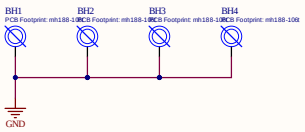




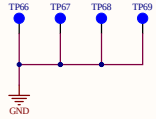




SCREW HOLE



GND TP



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