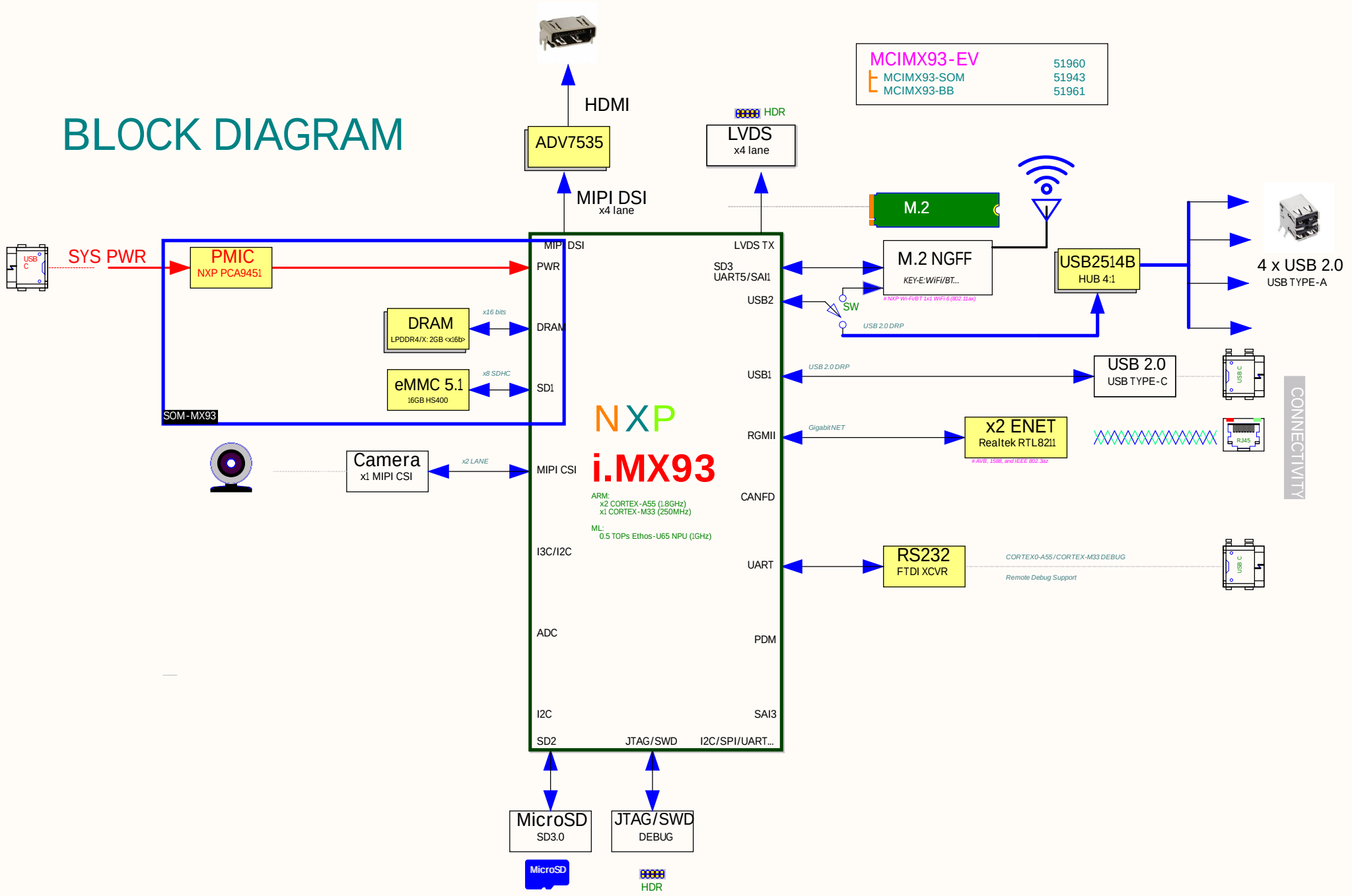
BLOCK DIAGRAM



i.MX93 EVK PWR TREE

When PER_12V is required, VBUS_IN must be at least 12V!!!

USB C SNK PD

VBUS_IN

12-20V

DCDC BUCK

MPS MP8759GD

VSYS

5V/3A

DCDC_5V

5V/5A

DCDC BUCK

MPS MP2147

VEXT_3V3

3.3V/4A

Load SW

MOSFET

VDD_5V

5V/3A

DCDC BUCK

MPS MP2263GD

PER_12V

12V/3A

PMIC: PCA9451A CFG

SEQ		REGULATOR	VOL (V)	MAX I (mA)
1		LDO1	1.8	10
-				
2	T1	BUCK1/3 DP	0.85	4000
3	T2	LDO4	0.8	200
4				
5	T4	BUCK5	1.8	2000
6	T5	BUCK6	1.1	1500
7	T6	BUCK2	0.6	2000
8	T7	BUCK4	3.3	3000
8	T7	Load Switch	-	400
9	T8	LDO5	1.8/3.3	150
-	-			
12		POR_B	--	--

SoC: i.MX93

ITEM	PWR RAIL	TYP VOL(V)	REQ I (mA)
1	NVCC_BBSM_1V8	1.8	2
PMIC_ON_REQ			
2	VDD_SOC	DVS	Ref to DS
3	VDD_ANA_0P8	0.8	186
4	RFU: VDD_ANA_1P8 (250mA)	1.8	250
4	VDD_ANA_1P8/NVCC_WAKEUP	1.8	389
5	VDD2_DDR/LPD4 VDDQ	1.1	676
6	VDDQ_DDR (0.6V for LPD4x)	0.6	360
7	NVCC_GPIO/VDD_USB_3P3	3.3	SYS
7	SD_CARD	3.3	
8	NVCC_SD2	1.8/3.3	
-			
POR_B			

LPDDR4/X

VDD1 <1.8V>

VDD2 <1.1V>

VDDQ <0.6V/1.1V>

eMMC

VCCQ <1.8V>

VCC <3.3V>

MicroSD

VCC <3.3V>

ETHERNET

DVDD_REG <1.8V>

AVDD/DVDD <3.3V>

USB C DRP/ A HOST

VBUS <5V>

M.2 KEY-E

3.3V

MIPI DSI / LVDS

3.3V

5V

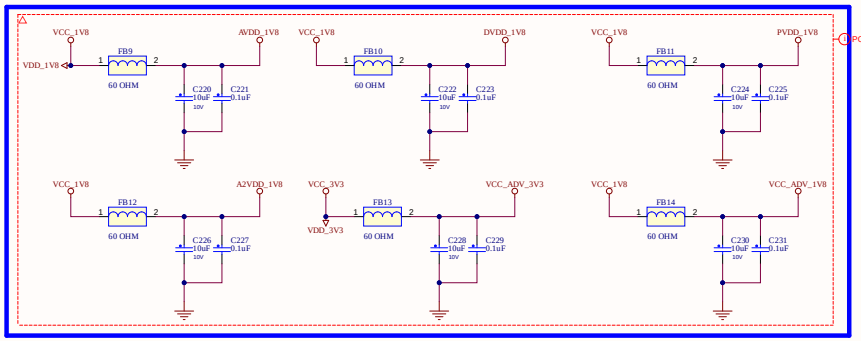
12V

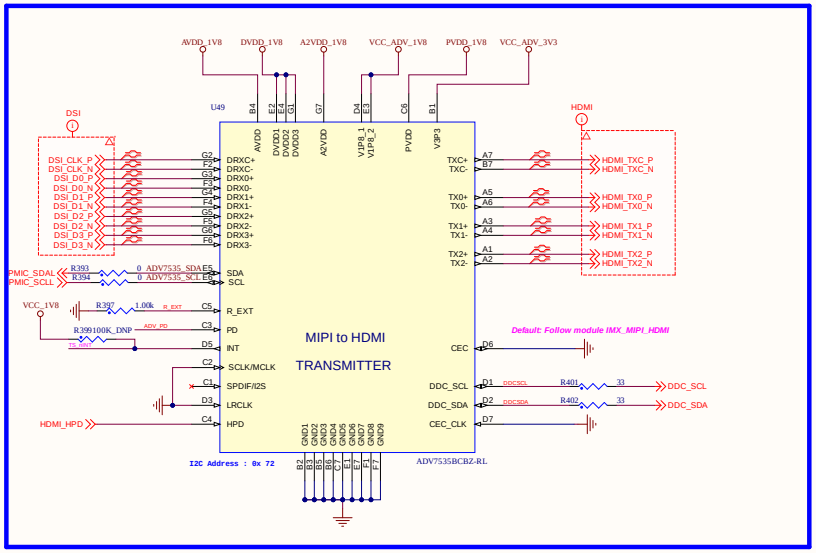
MIPI CSI

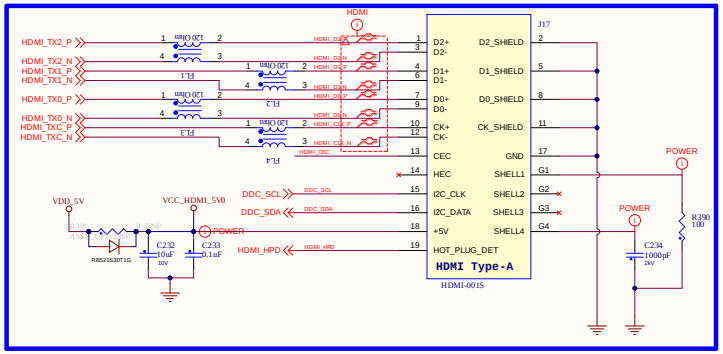
3.3V

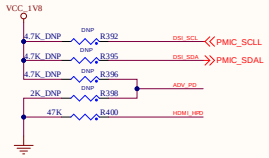
REVISION	DESCRIPTION	DATE	APPROVED

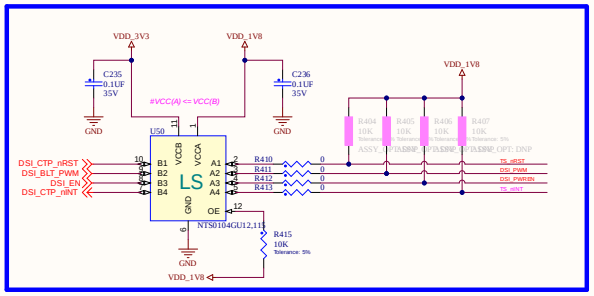
IMX_MIPI_HDMI

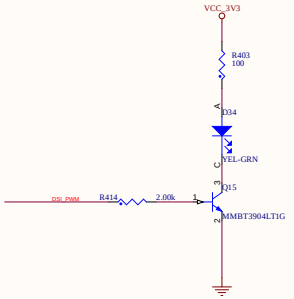




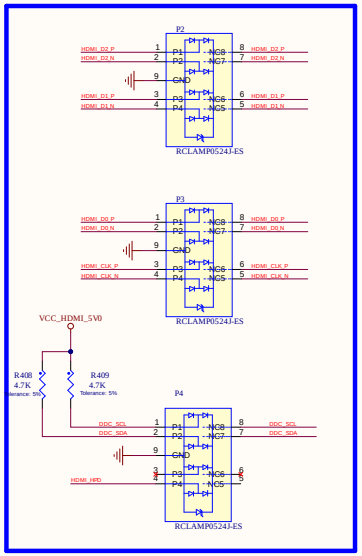








TVS_PROTECTION



APPROVALS	DATE	PROJECT
ENG: *		Altium
DSN: *		PROJECT REVISION: Not in version control
CHK: *		DOCUMENT REVISION: Not in version control
REFERENCE DOCUMENTS		DESIGN ITEM:
BOM:		TITLE: *
ASSY DWG:		SIZE: C
FAB DWG:		CAGE CODE
PCB DWG:		DWG NO.
		REV
		SCALE:
		FILE NAME: Convert MIPI to HDMI.SchDoc
		SHEET * OF *

i.MX93 I/O

<B2B CN for CPU SOM>

INTERRUPT
GPIO
FUNC

RECEPTACLE

J2
DF40C-80DS-0.4V(51)

RECEPTACLE

J1
DF40C-100DS-0.4V(51)

RECEPTACLE

J3
DF40C-80DS-0.4V(51)

COMP DESIGN w/ AUTO

I2C IO EXP

U1 PCAL6524HEAZ

#PU RES for IRQ

#Share IRQ due to TCPC level trigger rather edge trigger

#1 MHz I2C I/F for IRQ fast response!!!

U2 ADP5585ACPZ-00-R7

U3 74AUP1G07GW

SW1 CHS-04TA

M.2 802.15.4

Microcontroller Product Group

6501 William Cannon Drive West
Austin, TX 78735-8598

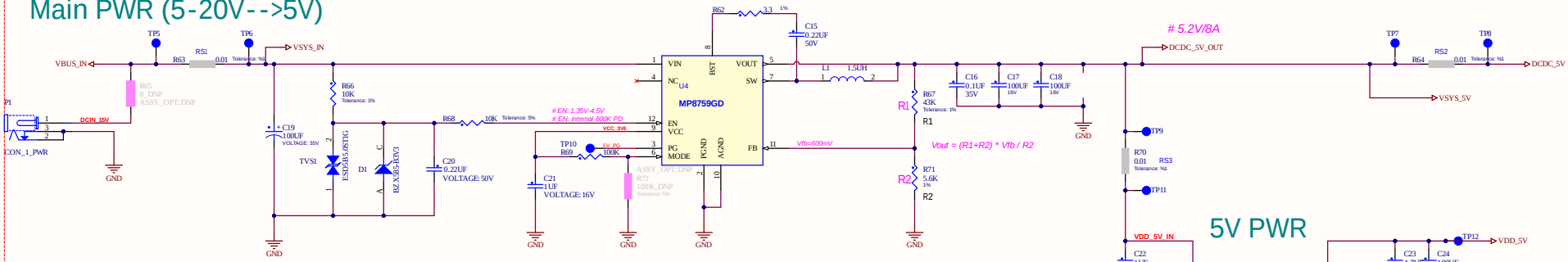
ICAP Classification: CP: ___ IUO: A PUBI: ___

Designer: NXP SE	Drawing Title: MCIMX93-BB <MCIMX93-EVK>
Drawn by: NXP SE	Page Title: SOM BB
Approved:	Size: NC; Document Number: SCH-51961 PDF: SPF-51961; Rev: B5
	Date: *; Sheet 4 of 19

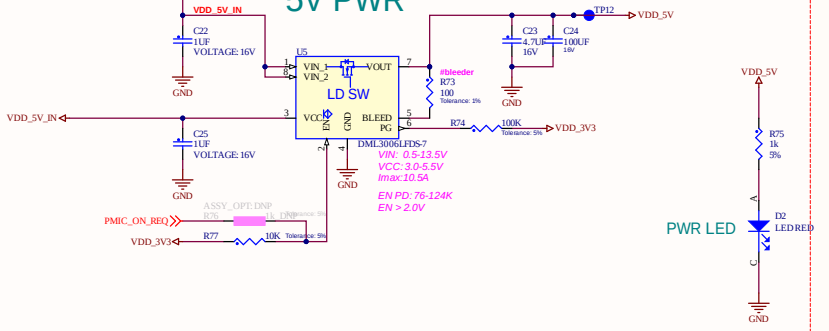
SYSTEM POWER

When PER 12V is required, VBUS_IN must be at least 12V!!!

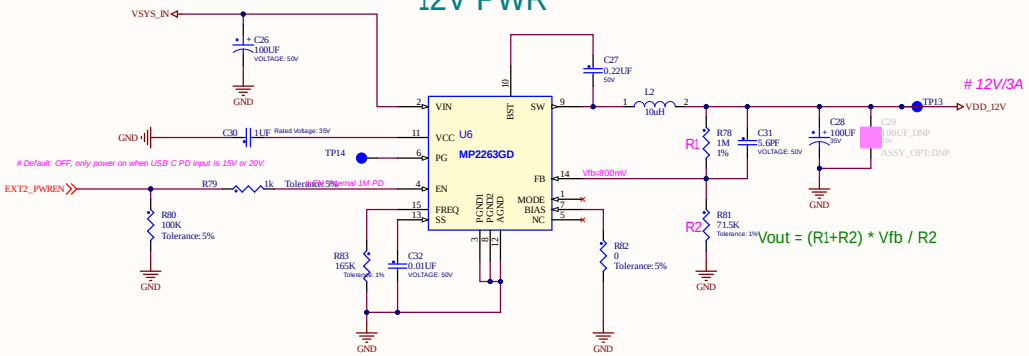
Main PWR (5-20V-->5V)



5V PWR



12V PWR



SOM SCREW

BH1 SMTSO-M2 · BH2 SMTSO-M2 · BH3 SMTSO-M2

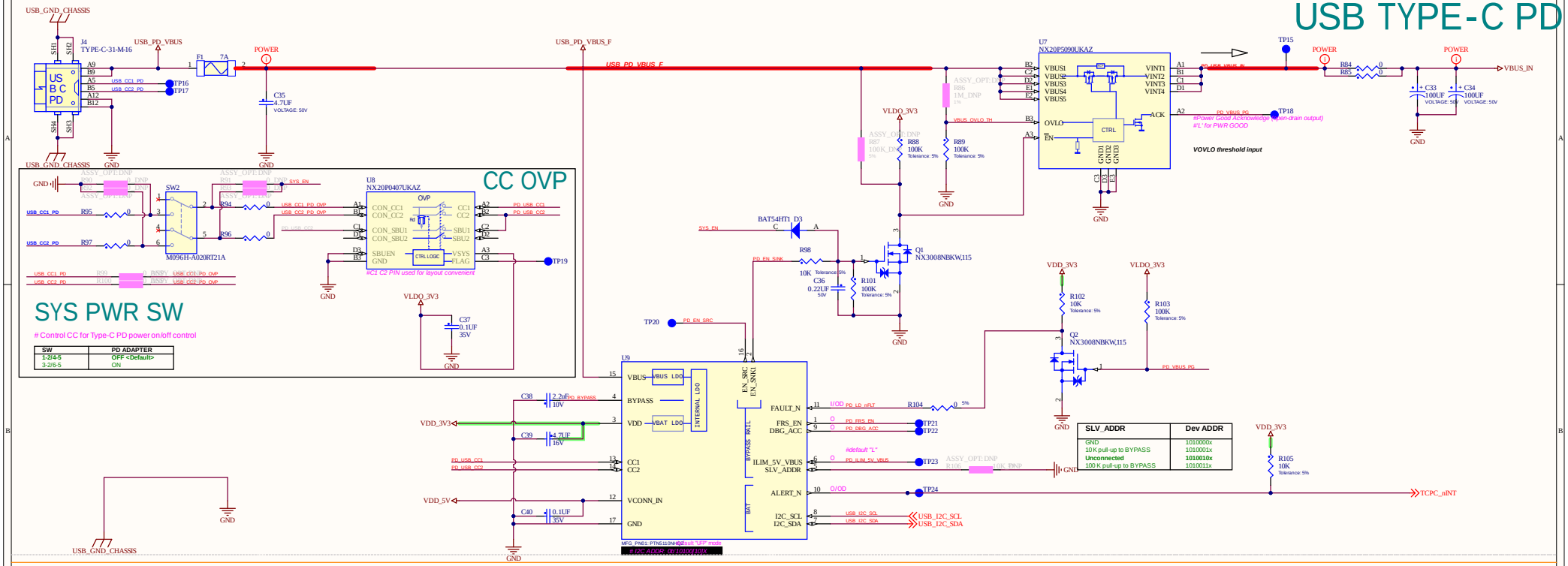
BB SCREW

BH4 STANDOFF M2.5 ASSY_OPT: DNP · BH5 STANDOFF M2.5 ASSY_OPT: DNP · BH6 STANDOFF M2.5 ASSY_OPT: DNP · BH7 STANDOFF M2.5 ASSY_OPT: DNP

Microcontroller Product Group	6501 William Cannon Drive West, Austin, TX 78735-8598
Designer: NXP SE	Drawing Title: MCIMX93-BB <MCIMX93-EVK>
Drawn by: NXP SE	Page Title: SYS PWR
Approved:	Size: NC · Document Number: SCH-51961 PDF: SPF-51961 · Rev: B5
	Date: * · Sheet: 5 of 19

ICAP Classification: CP: ___ IUO: A PUBI: ___

USB TYPE-C PD


USB_GND_CHASSIS
J4
TYPE-C-31-M-16
USB_PD_VBUS
F1 7A
POWER
C35 4.7UF VOLTAGE: 50V
USB_PD_VBUS_F
U7
NX20P5090UKAZ
VBUS1
VBUS2
VBUS3
VBUS4
VBUS5
VINT1
VINT2
VINT3
VINT4
OVLO
EN
ACK
CTRL
VOVLO threshold input
TP15
TP18
R84 0
R85 0
C33 100UF VOLTAGE: 50V
C34 100UF VOLTAGE: 50V
VBUS_IN
VLDO_3V3
R88 100K Tolerance: 5%
R89 100K Tolerance: 5%
CC OVP
U8
NX20P0407UKAZ
OVP
CON_CC1
CON_CC2
CON_SBU1
CON_SBU2
SBUEN
GND
CC1
CC2
SBU1
SBU2
VSYS
FLAG
CTRL LOGIC
TP19
C37 0.1UF 35V
SW2
M096H-A020RT21A
R95 0
R97 0
R94 0
R96 0
SYS PWR SW
Control CC for Type-C PD power on/off control
SW | PD ADAPTER
1-2/4-5 | OFF <Default>
3-2/6-5 | ON
BAT54HT1 D3
Q1
NX3008NBKW,115
R98 10K Tolerance: 5%
R101 100K Tolerance: 5%
C36 0.22UF 50V
TP20
PD_EN_SRC
U9
VBUS
BYPASS
VDD
CC1
CC2
VCONN_IN
GND
FAULT_N
FRS_EN
DBG_ACC
ILIM_5V_VBUS
SLV_ADDR
ALERT_N
I2C_SCL
I2C_SDA
VBUS_LDO
VBAT_LDO
INTERNAL_LDO
EN_SRC
EN_SNK1
BYPASS_RAIL
VBAT
C38 2.2uF 10V
C39 4.7UF 16V
C40 0.1UF 35V
R104 0
TP21
TP22
TP23
TP24
R102 10K Tolerance: 5%
R103 100K Tolerance: 5%
Q2
NX3008NBKW,115
SLV_ADDR | Dev ADDR
GND | 1010000x
10 K pull-up to BYPASS | 1010001x
Unconnected | 1010010x
100 K pull-up to BYPASS | 1010011x
R105 10K Tolerance: 5%
TCPC_nINT
USB_I2C_SCL
USB_I2C_SDA

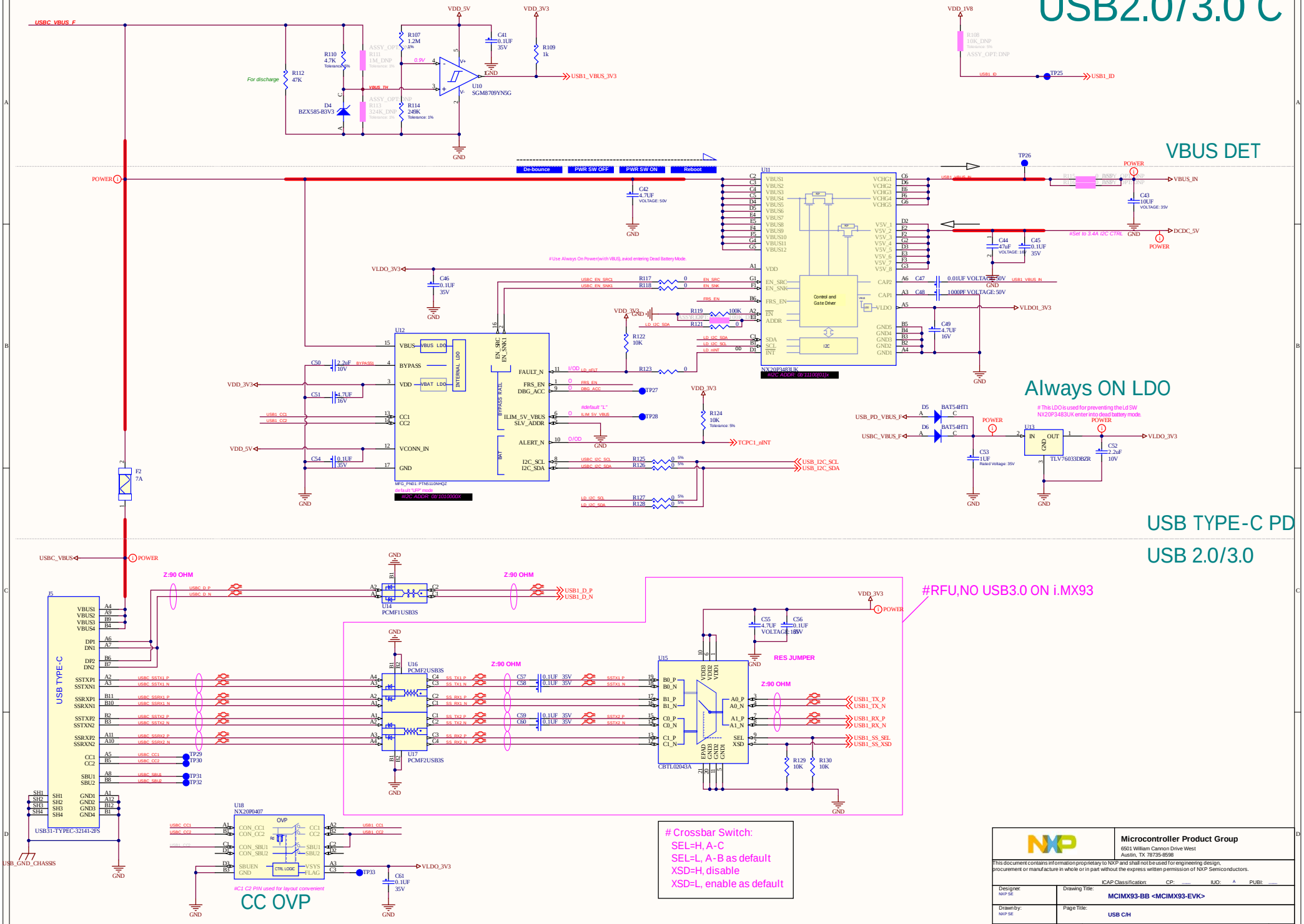
USB2.0/3.0 C

VBUS DET

Always ON LDO

USB TYPE-C PD

USB 2.0/3.0



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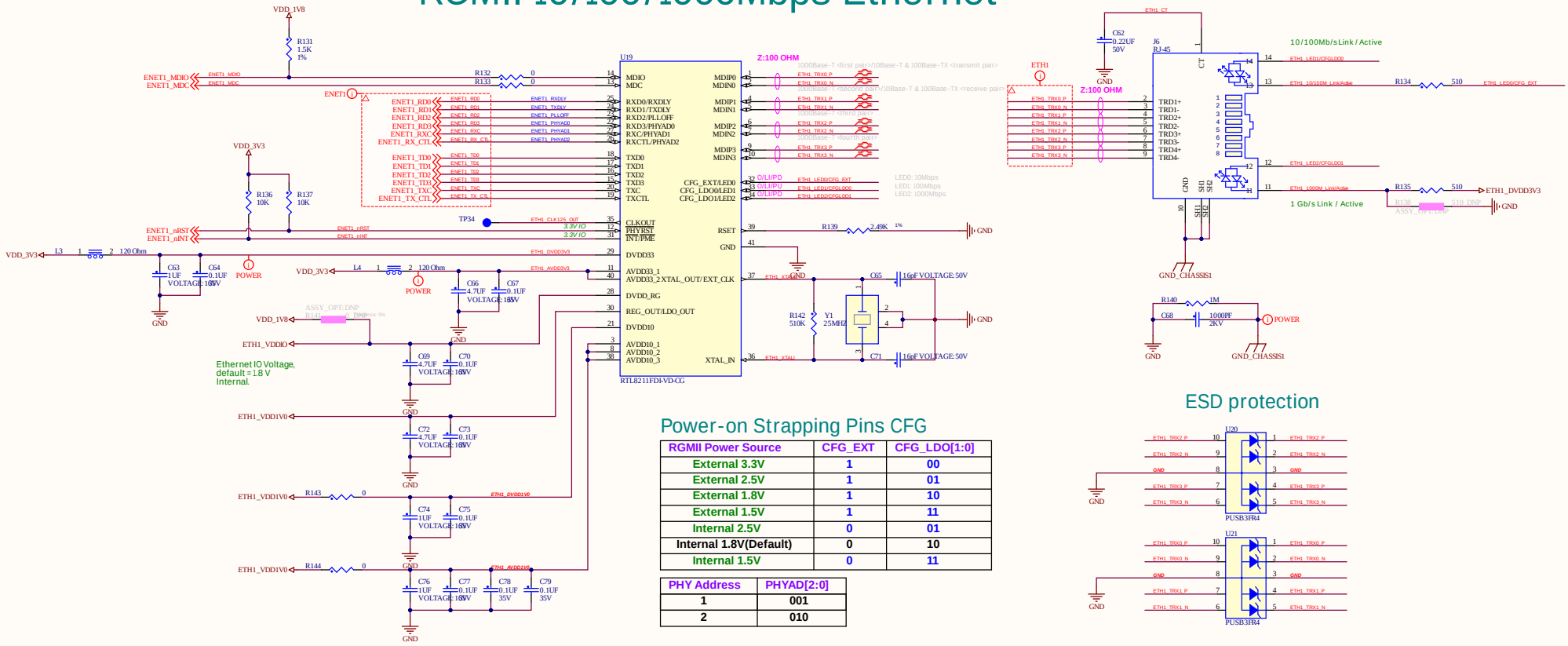
6501 William Cannon Drive West
Austin, TX 78735-8598

ICAP Classification: CP: ___ IUO: A PUBI: ___

Designer: NXP SE	Drawing Title: MCIMX93-BB <MCIMX93-EVK>
Drawn by: NXP SE	Page Title: USB C/H
Approved:	Size: NC; Document Number: SCH-51961 PDF: SPF-51961; Rev: B5
	Date: *; Sheet: 7 of 19

RGMII 10/100/1000Mbps Ethernet

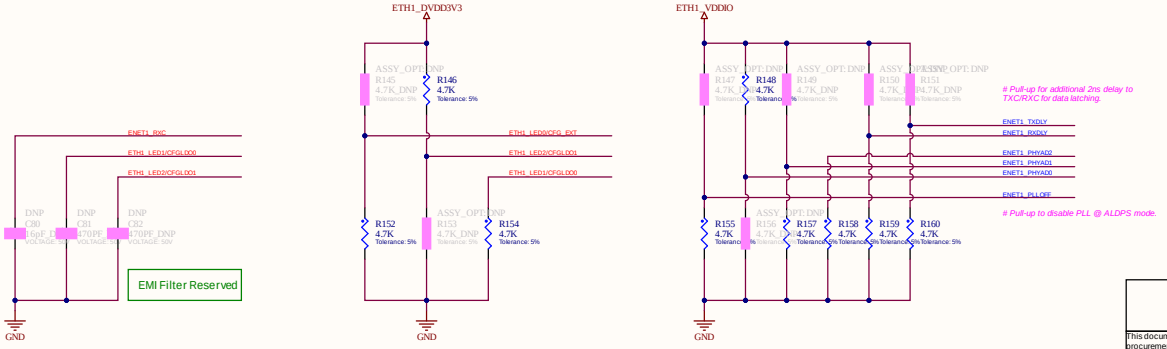


Power-on Strapping Pins CFG

RGMII Power Source	CFG_EXT	CFG_LDO[1:0]
External 3.3V	1	00
External 2.5V	1	01
External 1.8V	1	10
External 1.5V	1	11
Internal 2.5V	0	01
Internal 1.8V(Default)	0	10
Internal 1.5V	0	11

PHY Address	PHYAD[2:0]
1	001
2	010

ESD protection



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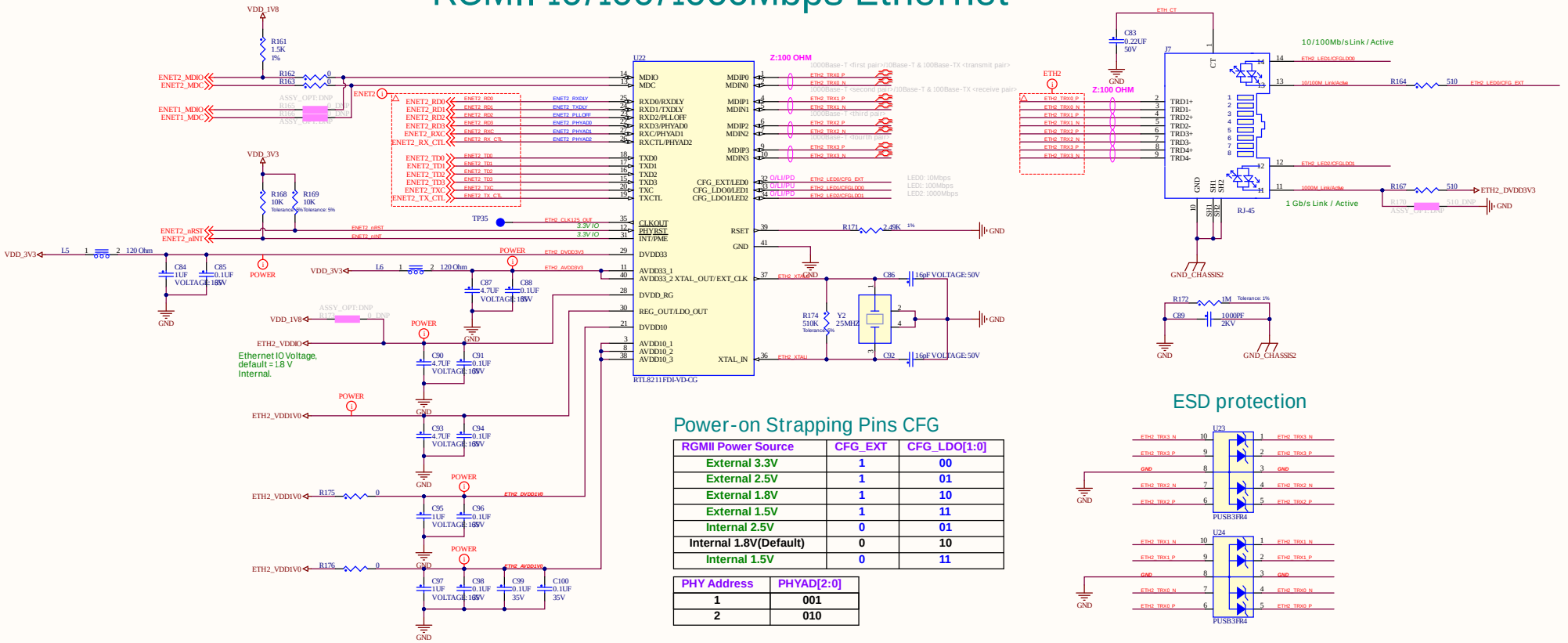
Austin, TX 78735-8598

ICAP Classification: CP: ___ IUO: A PUBI: ___

Designer: NXP SE	Drawing Title: MCIMX93-BB <MCIMX93-EVK>
Drawn by: NXP SE	Page Title: ENET1
Approved:	Size: NC; Document Number: SCH-51961 PDF: SPF-51961; Rev: B5
	Date: *; Sheet: 8 of 10

RGMII 10/100/1000Mbps Ethernet

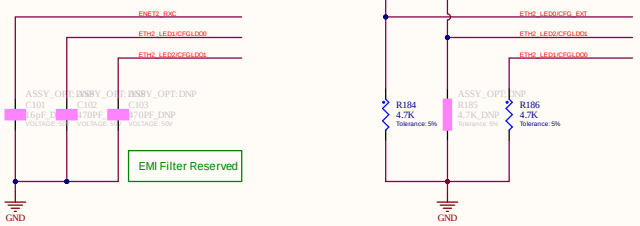


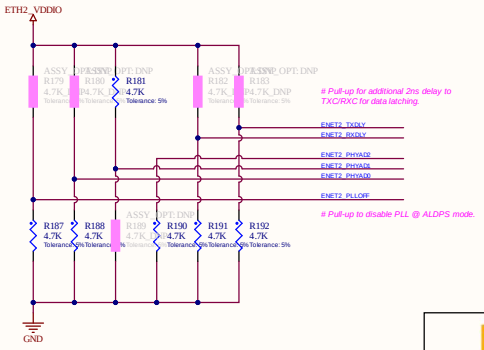
Power-on Strapping Pins CFG

RGMII Power Source	CFG_EXT	CFG_LDO[1:0]
External 3.3V	1	00
External 2.5V	1	01
External 1.8V	1	10
External 1.5V	1	11
Internal 2.5V	0	01
Internal 1.8V(Default)	0	10
Internal 1.5V	0	11

PHY Address	PHYAD[2:0]
1	001
2	010

ESD protection





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ICAP Classification: CP: ___ IUO: A PUBI: ___

Designer: NXP SE	Drawing Title: MCIMX93-BB <MCIMX93-EVK>
Drawn by: NXP SE	Page Title: ENET2
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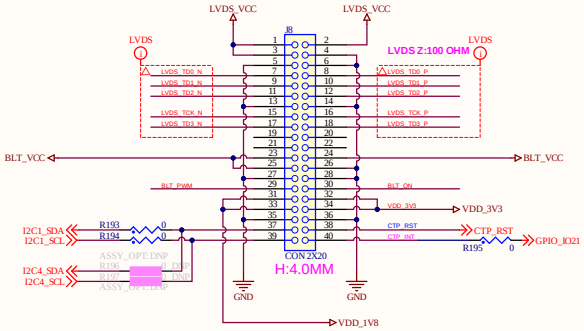
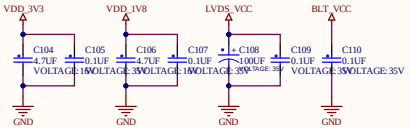
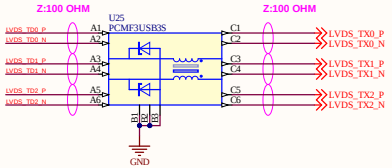
	Date: *; Sheet: 9 of 19

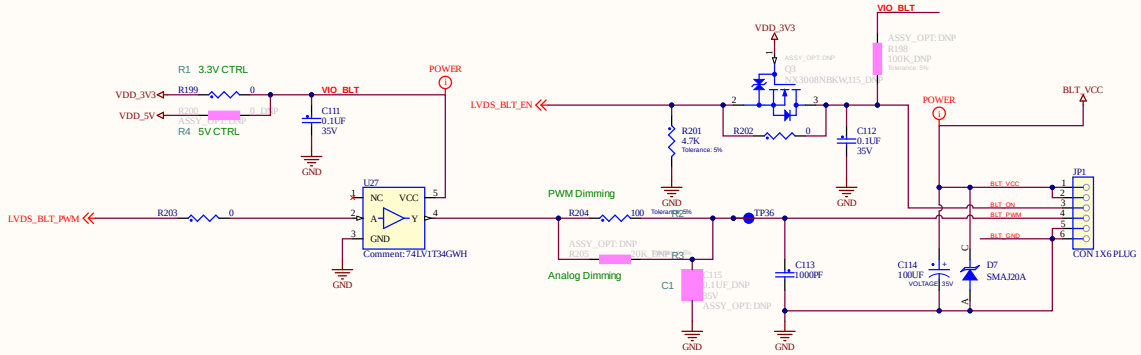
LVDS

LVDS *LVDS DATA FORMAT* VESA JEITA





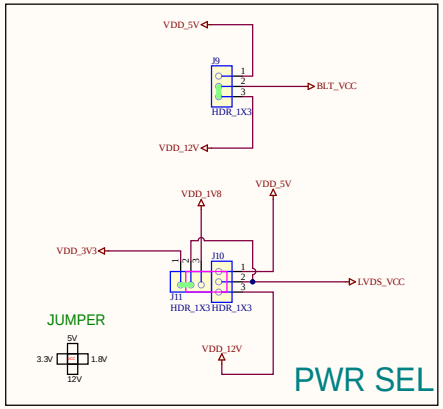




LVDS LCD BLT

Dimming CTRL

ITEM	INSTALL	DNP	NOTE
3.3V PWM Dimming	R1, R2	R4,R3,C1	PWM frequency according SPEC
5.0V PWM Dimming	R4,R2	R1,R3,C1	PWM frequency according SPEC
3.3V Analog Dimming	R1,R3,C1	R2,R4	0<Vadj<3.3V
5.0V Analog Dimming	R4,R3,C1	R1,R2	0<Vadj<5.0V



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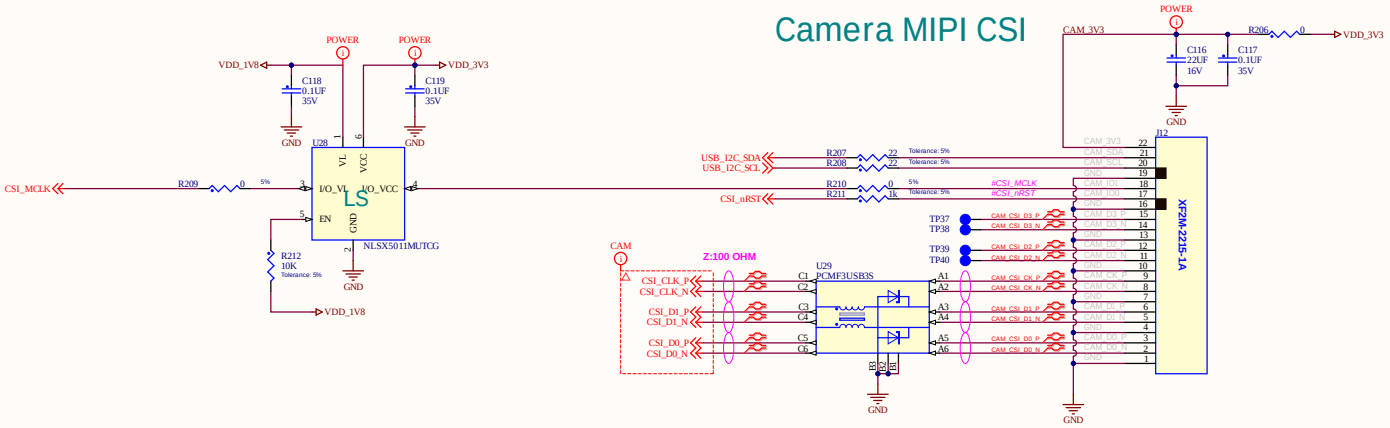
Austin, TX 78735-8598

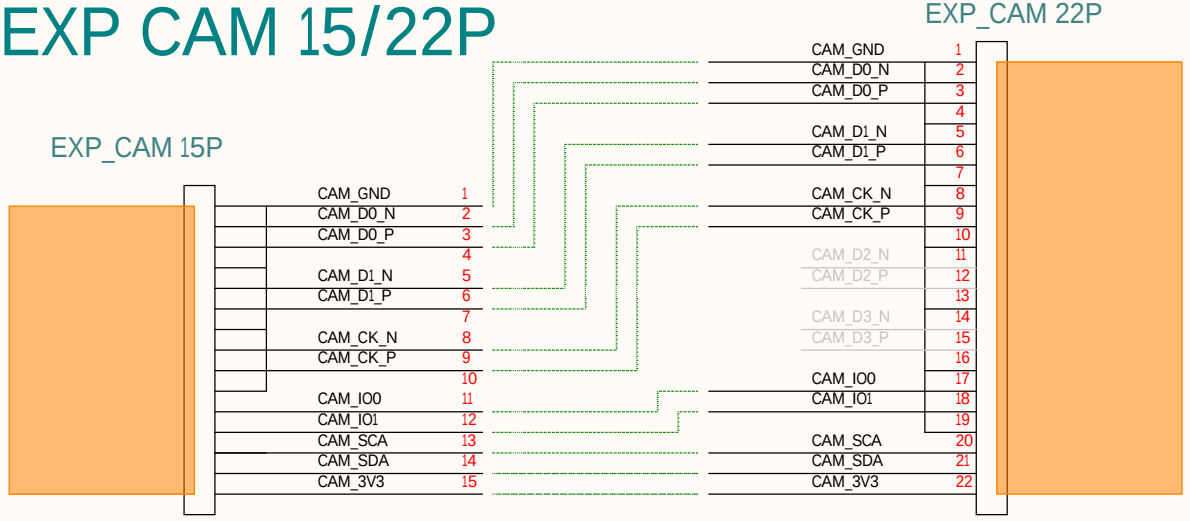
ICAP Classification: CP: ___ IUO: A PUBI: ___

Designer: NXP SE	Drawing Title: MCIMX93-BB <MCIMX93-EVK>
Drawn by: NXP SE	Page Title: MIPI/LVDS
Approved:	Size: NC; Document Number: SCH-51961 PDF: SPF-51961; Rev: B5
	Date: *; Sheet: 10 of 19

MIPI CSI



EXP CAM 15/22P



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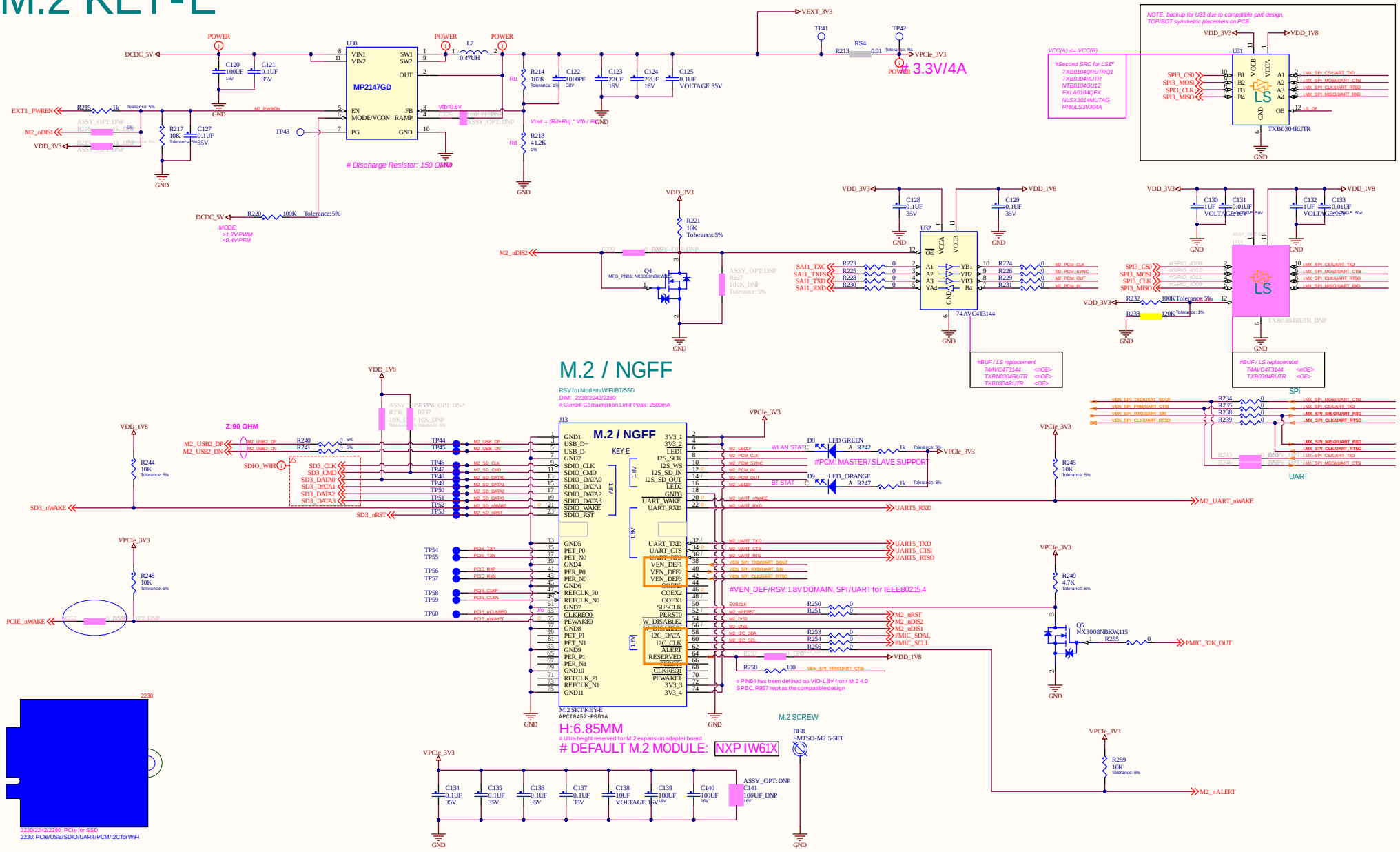
Designer: NXP SE	Drawing Title: MCIMX93-BB <MCIMX93-EVK>	
Drawn by: NXP SE	Page Title: MIPI CSI	
Approved:	Size: NC Document Number: SCH-51961 PDF: SPF-51961 Rev: B5	
	Date: * Sheet 11 of 19	

M.2 KEY-E



Key ID	Pin	Interface	Key Definition
A	8-15	2x PCIe x1 / USB 2.0 / I2C / DP x4	Display Port Based Connectivity
B	12-19	PCIe x2 / SATA / USB 2.0 / USB 3.1 Gen1 / HSIC / SSIC / Audio / UIM / I2C / SMBus	WWAN/SSD/Others Primary Key
C	16-23	PCIe/M-PCIe / USB 2.0 / USB 3.1 Gen1 / SSIC / I2C-SlimBUS / UIM / ANTCTL	WWAN Key
D	20-27	Reserved for Future Use (RFU)	RFU
E	24-31	2x PCIe x1 / USB 2.0 / I2C / SDIO / UART / PCM	SDIO Based Connectivity
F	28-35	Future Memory Interface (FMI)	Future Memory Interface
G	39-46	Not Used for M.2; for Custom/Non-Standard Apps	Generic (Not used for M.2)
H	43-50	Reserved for Future Use (RFU)	RFU
J	47-54	Reserved for Future Use (RFU)	RFU
K	51-58	Reserved for Future Use (RFU)	RFU
L	55-62	Reserved for Future Use (RFU)	RFU
M	59-66	PCIe x4 / SATA / SMBus	SSD 4 Lane PCIe

i.MX93 GPIO8-11

#GPIO_IO08	#SPI3_CS	#UART7_TXD
#GPIO_IO09	#SPI3_MISO	#UART7_RXD
#GPIO_IO10	#SPI3_MOSI	#UART7_CTS <I>
#GPIO_IO11	#SPI3_CLK	#UART7_RTS <O>

IW61X GPIO12-15

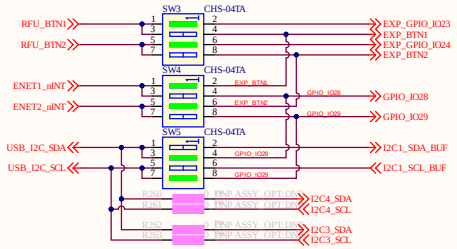
#GPIO_IO15	#SPI_TXD	#UART2_SOUT
#GPIO_IO14	#SPI_RXD	#UART2_SIN
#GPIO_IO13	#SPI_FRM	#UART2_RTS <O>
#GPIO_IO12	#SPI_CLK	#UART2_CTS <I>

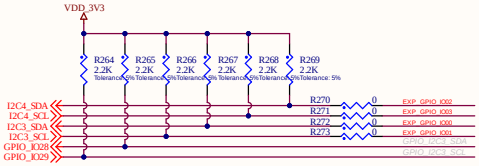
Microcontroller Product Group
6501 William Cannon Drive West
Austin, TX 78735-8598

ICAP Classification: CP: ___ IUO: A PUBI: ___

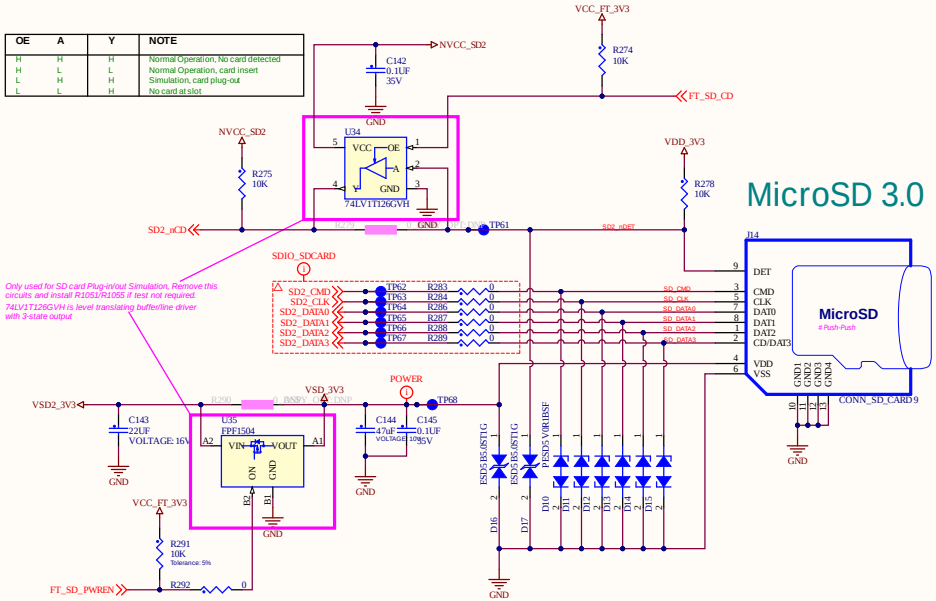
Designer: NXP SE	Drawing Title: MCIMX93-BB <MCIMX93-EVK>
Drawn by: NXP SE	Page Title: M.2 E-KEY
Approved:	Size: NC; Document Number: SCH-51961 PDF: SPF-51961; Rev: B5
	Date: *; Sheet: 12 of 19

RFU BTN JUMPER



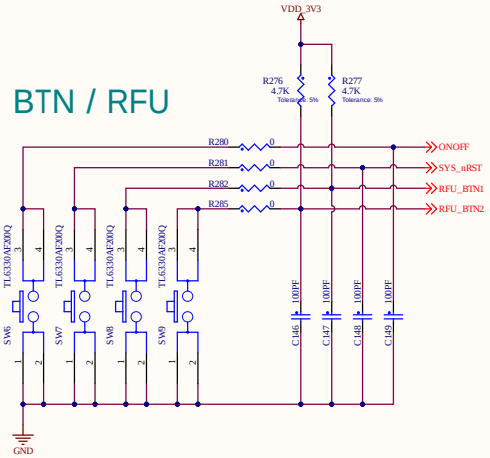


OE	A	Y	NOTE
H	H	H	Normal Operation, No card detected
H	L	L	Normal Operation, card insert
L	H	H	Simulation, card plug-out
L	L	H	No card at slot



MicroSD 3.0

BTN / RFU



Microcontroller Product Group
6501 William Cannon Drive West
Austin, TX 78735-8598

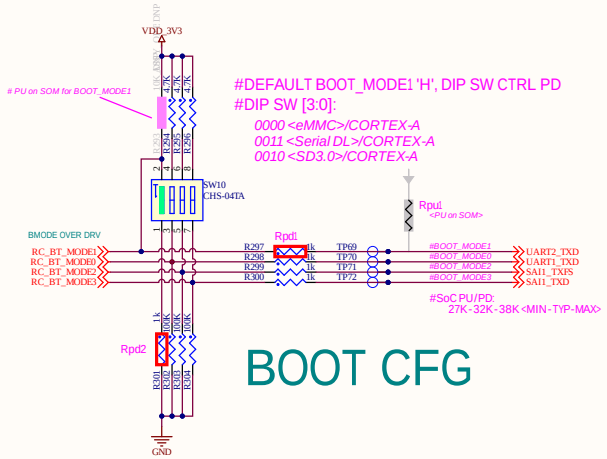
ICAP Classification: CP: ___ IUO: A PUBI: ___

Designer: NXP SE	Drawing Title: MCIMX93-BB <MCIMX93-EVK>
Drawn by: NXP SE	Page Title: MicroSD/IMU/MFi/RPi/ADC
Approved:	Size: NC; Document Number: SCH-51961 PDF: SPF-51961; Rev: B5
	Date: *; Sheet 13 of 19

BOOT MODE CFG

i.MX93 BOOT MODE

DIP SW[3:0]	BOOT_MODE[3:0]	BOOT CORE	BOOT DEVICE	COMMENT
0001	0000	Cortex-A55	From internal fuses	
0011	0001	Cortex-A55	Serial Downloader	USB1/2
0000	0010	Cortex-A55	USDHC1 8-bit eMMC 5.1	
0010	0011	Cortex-A55	USDHC2 4-bit SD3.0	
0101	0100	Cortex-A55	FlexSPI Serial NOR	with SFDP (JESD-216) discoverable parameters
0111	0101	Cortex-A55	FlexSPI Serial NAND 2K page	
0100	0110	Cortex-A55	Infinite Loop	
0110	0111	Cortex-A55	Test Mode	
1001	1000	Cortex-M33	From internal fuses	
1011	1001	Cortex-M33	Serial Downloader	USB1
1000	1010	Cortex-M33	USDHC1 8-bit eMMC 5.1	
1010	1011	Cortex-M33	USDHC2 4-bit SD3.0	
1101	1100	Cortex-M33	FlexSPI Serial NOR	with SFDP (JESD-216) discoverable parameters
1111	1101	Cortex-M33	FlexSPI Serial NAND 2K page	
1100	1110	Cortex-M33	Infinite Loop	
1110	1111	Cortex-M33	Test Mode	



Microcontroller Product Group
6501 William Cannon Drive West
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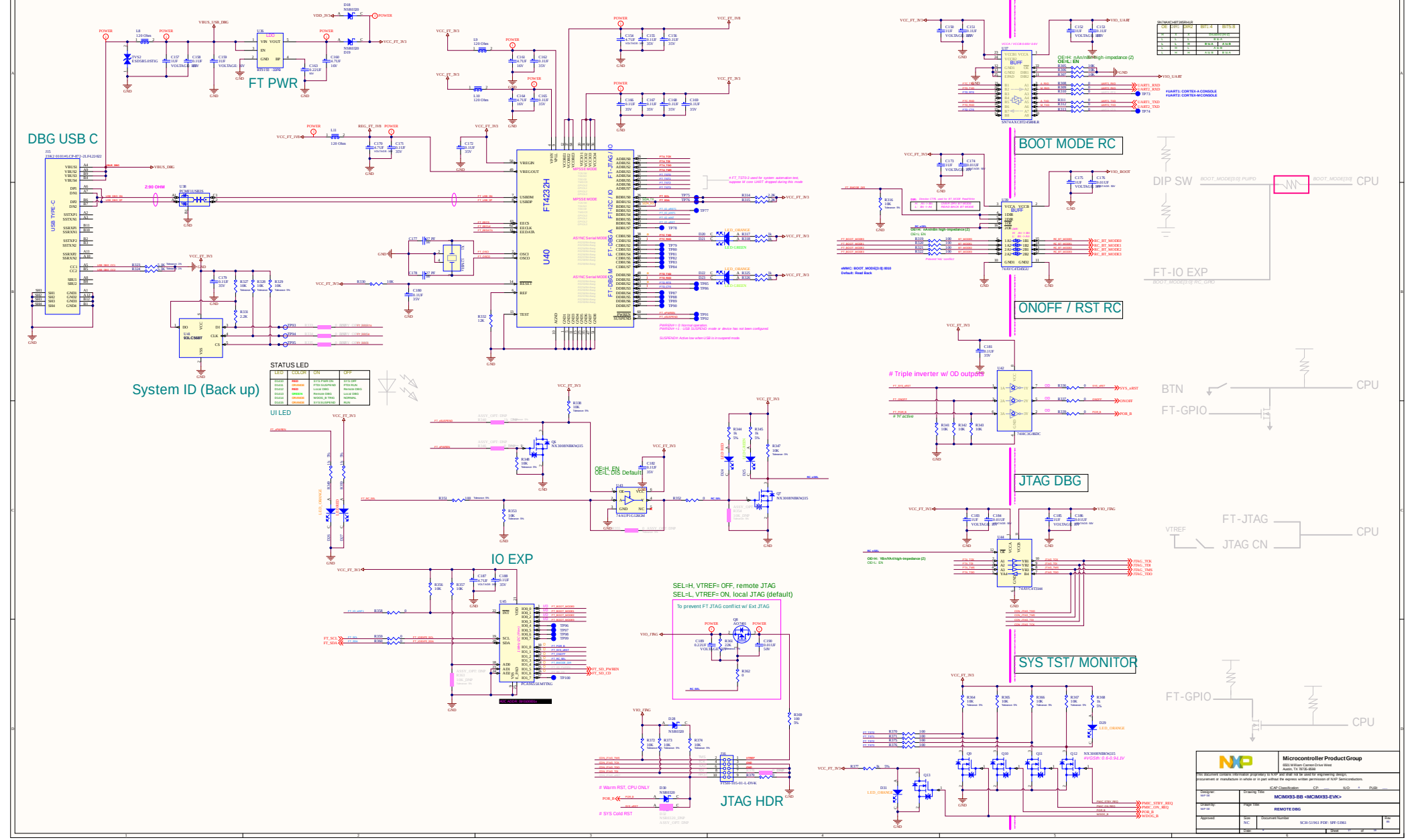
ICAP Classification: CP: ___ IUO: A PUBI: ___

Designer: NXP SE	Drawing Title: MCIMX93-BB <MCIMX93-EVK>
Drawn by: NXP SE	Page Title: PDM/MQS
Approved:	Size: NC; Document Number: SCH-51961 PDF: SPF-51961; Rev: B5
	Date: *; Sheet: 16 of 19

REMOTE DEBUG

REMOVE THIS PAGE IF NOT USED!!!

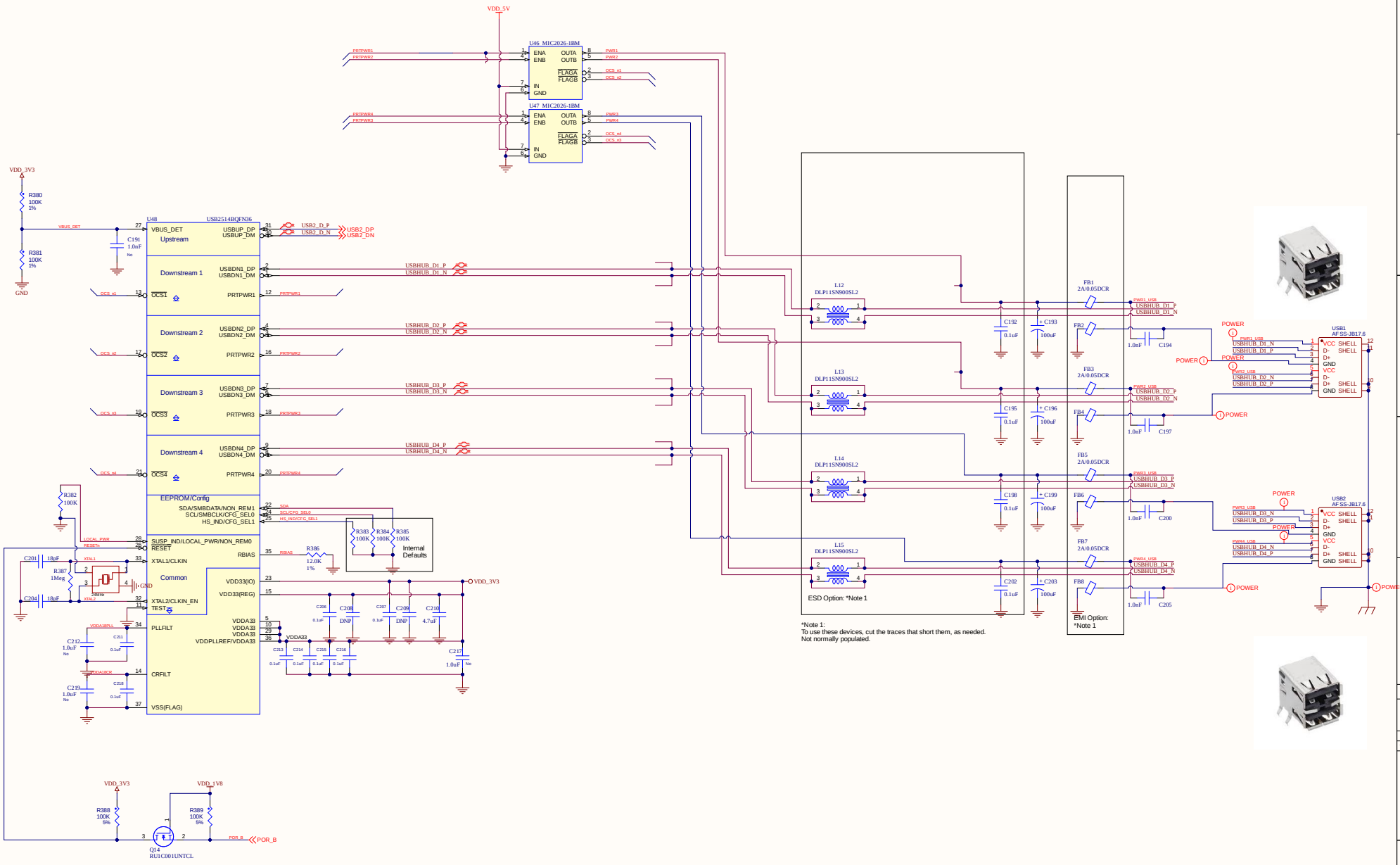


LED	COLOR	ON	OFF
D1510	RED	SYS PWR ON	SYS OFF
D1511	ORANGE	SYS SUSPEND	RUN
D1512	RED	Local DBG	Remote DBG
D1513	GREEN	Remote DBG	Local DBG
D1514	ORANGE	WDOG_B TRIG	NORMAL
D1515	ORANGE	SYS SUSPEND	RUN

OE	DIR	SRC	BIT=4	BIT=8
H	X	X	Isolation (Hi-Z)	
L	L	H	B to A	
L	H	L	A to B	
L	L	L	B to A	

Microcontroller Product Group	
6501 William Cannon Drive West Austin, TX 78735-8598	
Designer:	Drawing Title: MCIMX93-BB <MCIMX93-EVK>
Engineering:	Page Title: REMOTE DBG
Approved:	Size: A3 / Document Number: SCH-51961 / Rev: A1
	Date: / Sheet: 37 of 38

REVISION	DESCRIPTION	DATE	APPROVED



*Note 1:
To use these devices, cut the traces that short them, as needed.
Not normally populated.

APPROVALS	DATE
ENG:	
DSN:	
CHK:	
REFERENCE DOCUMENTS	
BOM:	
ASSY DWG:	
FAB DWG:	
PCB DWG:	

PROJECT: Altium

PROJECT REVISION: Not in version control | DOCUMENT REVISION: Not in version control | DESIGN ITEM:

TITLE: *

SIZE	CAGE CODE	DWG NO.	REV
C			

SCALE: | FILE NAME: HUB_USB 4 1.SchDoc | SHEET * OF *