MCIMX93-BB

(i.MX93 Reference Board SOM+BB)

MCIMX93-EVK 51960
MCIMX93-SOM 51943
MCIMX93-BB 51961

Table of Content

1. Interrupted lines coded with the same letter or letter combinations are electrically connected.

2. Device type number is for reference only. The number varies with the manufacturer.

3. Special signal usage:
   _B Denotes - Active-Low Signal
   <> or [] Denotes - Vectored Signals

4. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.

Preliminary - Subject to Change without Notice!

This board was designed for maximum flexibility in software development and demonstrates multiple functions possible with i.MX processors. Although best design practices have been applied, some areas may not be suitable for a mass-production design.

Revision History

Rev. Code	Date	By	Description
A	2022-01-14	nxa22324	Initial version
B	2022-03-24	nxa22324	Update U410 VDD to 3.3V Update U309 to TMUX1574RSVR Change U204 Power supply to VCC_FT_3V3 Change U904 to 74AVC4T3144 due to PU/PD on BOOT MODE Change CODEC U1201 to WM8962B Update ENET PHY to RTL8211FDI-VD-CG Add U902 as the backup of U905 for the symmetric compatible part Change R513 PU to ETH1_DVDD3V3 Remove D1103 due to CANFD 5MHz speed require Low C Add U1309, R1331 for PDM CLK buffer and level translator Install R161, R162, DNP R169,R170,R173,R174,U107 due to U107 abnormal connected I3C BUS Add R1491,R1492 for RC_nSEL 3.3V Level DNP D1409, install D1408 to avoid system reboot failure which halt by Trace32 nRST Add U1411 as backup for U1402 Add R528, R630 as LED PWR SRC,DNP R507, R608
B1	2022-07-20	nxa22324	DNP R403, R323, chang to 1.8V PU due to USB ID power domain is 1.8V Add R182,R183,TP105 as USB TCPC shared interrupt to support level trigger mode Change R127 connected with HP_DET which used as audio jack detection Change R132 connected with AUD_nINT to maintain the SW compatible Add R1226, DNP R1203 as audio jack detection to GPIO IRQ path Add R1070, R1071 for GPIO28/29 I2C PU Add R956,R957 for M.2 compatible design Remove R134,C308, change BH205-BH208 to GND net Change J801 CSI I2C to USB_I2C_SDA/SCL Add U1004,D1011,D1012,R1072,R1073-R1085,C1021-C1024,BT1001,TP1015-TP1021 RTC module circuits Add R807 as backup usage, change R801,R803 to 22OHM Change L503,L504,L603,L604 to 0 OHM Add R958,R959 to use RTC_CLKO
B2	2023-01-30	nxa22324	DNP R1036,R1037,R1038 due to those GPIO may used as I2C on daughter card Install R181, DNP R131 to support CTP interrupt multi-touch
B3	2023-04-18	nxa22324	Install R1203 to keep WM8962B GPIO5 PU Change U701 to PESD3USB3S, U702 to PESD2USB3S due to MIPI DSI compliance test Change R1205, R1206, R1207, R1208 to 51 OHM to improve I2S signals
B4	2023-04-18	nxa22324	Update J302, J401, J1401 USB C connector to longe pin length (footprint compatible) to improve the reliability of soldering
B5	2023-08-23	nxa22324	Remove D1011, change D1012, R1083, TP1022,TP1023 circuits to support PCF2131 VBAT power charge function Add R435, D404, R360, D302, DNP R404, R407, R321,R324 for USB PWR detection backup DNP R960, Change R131 as EXP_PWREN,add U1005,U1006 circuits, DNP L1001, L1002 as i.MX91P compatible LCD design Change R1010 to 1K (DNP default) due to mid-voltage caused by LSM6DSOXTR internal PD Update D502, D503, D602, D603 due to ESD EOL

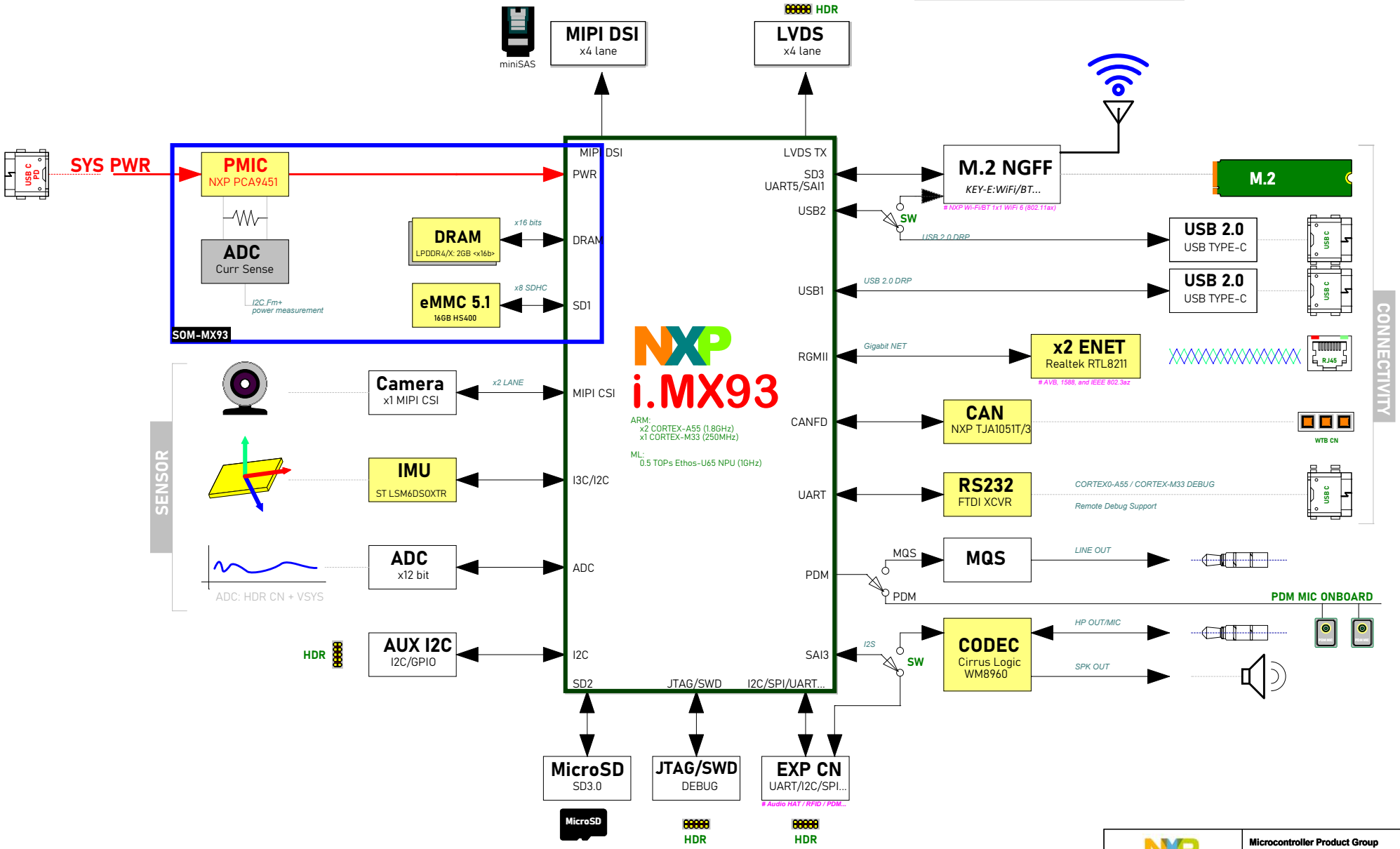
Microcontroller Product Group
6501 William Cannon Drive West
Austin, TX 78735-8598

ICAP Classification: CP: IUO: X PUBI:

Designer: NXP SE	Drawing Title: MCIMX93-BB <MCIMX93-EVK>		
Drawn by: NXP SE	Page Title: Title and Rev History		
Approved: <Approver>	Size C	Document Number SCH-51961 PDF: SPF-51961	Rev B5
	Date: Monday, September 04, 2023	Sheet 1 of 19	

BLOCK DIAGRAM

MCIMX93-EVK	51960
├ MCIMX93-SOM	51943
└ MCIMX93-BB	51961



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Drawn by: NXP SE	Page Title: Block Diagram	
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	Date: Monday, September 04, 2023	Sheet 2 of 19

i.MX93 EVK PWR TREE

When PER_12V is required, VBUS_IN must be at least 12V!!!

USB C SNK PD

VBUS_IN
12-20V

DCDC BUCK
MPS MP8759GD

VSYS
5V/3A

DCDC_5V
5V/5A

DCDC BUCK
MPS MP2147

VEXT_3V3
3.3V/4A

Load SW
MOSFET

VDD_5V
5V/3A

DCDC BUCK
MPS MP2263GD

PER_12V
12V/3A

PMIC: PCA9451A CFG

SEQ		REGULATOR	VOL (V)	MAX I (mA)
1		LDO1	1.8	10
-				
2	T1	BUCK1/3 DP	0.85	4000
3	T2	LDO4	0.8	200
4				
5	T4	BUCK5	1.8	2000
6	T5	BUCK6	1.1	1500
7	T6	BUCK2	0.6	2000
8	T7	BUCK4	3.3	3000
8	T7	Load Switch	-	400
9	T8	LDO5	1.8/3.3	150
-	-			
12		POR_B	--	--

SoC: i.MX93

ITEM	PWR RAIL	TYP VOL(V)	REQ I (mA)
1	NVCC_BBSM_1V8	1.8	2
PMIC_ON_REQ			
2	VDD_SOC	DVS	Ref to DS
3	VDD_ANA_0P8	0.8	186
4	RFU: VDD_ANA_1P8 (250mA)	1.8	250
4	VDD_ANA_1P8/NVCC_WAKEUP	1.8	389
5	VDD2_DDR/LPD4 VDDQ	1.1	676
6	VDDQ_DDR (0.6V for LPD4x)	0.6	360
7	NVCC_GPIO/VDD_USB_3P3	3.3	SYS
7	SD_CARD	3.3	
8	NVCC_SD2	1.8/3.3	
-			
POR_B			

LPDDR4/X
VDD1 <1.8V>
VDD2 <1.1V>
VDDQ <0.6V/1.1V>

eMMC
VCCQ <1.8V>
VCC <3.3V>

MicroSD
VCC <3.3V>

Audio CODEC
AVDD/DVDD <3.3V>
SPKVDD <5V>

ETHERNET
DVDD_REG <1.8V>
AVDD/DVDD <3.3V>

USB C DRP/ A HOST
VBUS <5V>

M.2 KEY-E
3.3V

MIPI DSI / LVDS
3.3V
5V
12V

MIPI CSI
3.3V

RPi
3.3V
5V

PDM/MQS/CAN
3.3V
5V

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Approved: <Approver>

Drawing Title: MCIMX93-BB <MCIMX93-EVK>
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Document Number: SCH-51961 PDF: SPF-51961
Rev: B5
Date: Monday, September 04, 2023
Sheet 3 of 19

i.MX93 I/O

<B2B CN for CPU SOM>

INTERRUPT
GPIO
FUNC

RECEPTACLE

J101
DF40C-80DS-0.4V(51)

VSYS_5V
VDD_1V8

PMIC_SCLL
PMIC_SDAL
PMIC_SCLH
PMIC_SDAH
PMIC_nINT
PMIC_32K_OUT

ENET1_MDC
ENET1_MDIO
ENET1_RD3
ENET1_RD2
ENET1_RD1
ENET1_RD0
ENET1_RX_CTL
ENET1_RXC
ENET1_TD3
ENET1_TD2
ENET1_TD1
ENET1_TD0
ENET1_TX_CTL
ENET1_TXC

ENET2_MDC
ENET2_MDIO
ENET2_RD3
ENET2_RD2
ENET2_RD1
ENET2_RD0
ENET2_RX_CTL
ENET2_RXC
ENET2_TD3
ENET2_TD2
ENET2_TD1
ENET2_TD0
ENET2_TX_CTL
ENET2_TXC

CLKO04
CLKO03
CLKO02
CLKO01

IMU_INT1
CSI_MCLK
EXP_nIRQ
SD3_nWAKE

JTAG_TDO
JTAG_TCK
JTAG_TMS
JTAG_TDI

1.8V RAIL
3.3V RAIL

GND

C110 10uF 16V
C111 10uF 16V
C117 22uF 10V
C118 0.1uF 35V

RECEPTACLE

J102
DF40C-100DS-0.4V(51)

VDD_3V3
NVCC_AON
NVCC_GPIO
VSD2_3V3
NVCC_SD2

SD3_DATA3
SD3_DATA2
SD3_DATA1
SD3_DATA0
SD3_CMD
SD3_CLK

GPIO_IO29
GPIO_IO28
GPIO_IO27
GPIO_IO23
GPIO_IO20
GPIO_IO21
GPIO_IO17
GPIO_IO14
GPIO_IO19
GPIO_IO18
GPIO_IO10
GPIO_IO11
GPIO_IO02
GPIO_IO03
GPIO_IO01
GPIO_IO00

SAI1_RXD0
SAI1_TXD0
SAI1_TXC
SAI1_TXFS

I2C2_SCL
I2C2_SDA

SD2_nCD
SD2_DATA1
SD2_DATA0
SD2_CLK
SD2_CMD
SD2_DATA3
SD2_DATA2

GPIO_IO26
GPIO_IO25
GPIO_IO24
GPIO_IO22
GPIO_IO16
GPIO_IO15
GPIO_IO12
GPIO_IO13
GPIO_IO08
GPIO_IO09

WDOG_B
PDM_DATA1
PDM_DATA0
PDM_CLK

UART2_RXD
UART2_TXD
UART1_RXD
UART1_TXD

1.8V RAIL
3.3V RAIL
NVCC_SD2 (1.8V/3.3V)

SW101
CHS-04TA
JTAG_TDO
JTAG_TCK
JTAG_TMS
JTAG_TDI
UART5_TXD
UART5_CTSI
UART5_RTSO
UART5_RXD

GND

VDD_3V3
VSD2_3V3
NVCC_BBSM_1V8

C112 22uF 10V
C113 0.1uF 35V
C115 22uF 10V
C116 0.1uF 35V
C114 1uF 16V

GND

VDD_3V3
NVCC_AON
NVCC_GPIO

R165 DNP
R166 DNP
R167 DNP
R168 DNP

I2C1_SCL
I2C1_SDA
PMIC_SCLH
PMIC_SDAH

COMP DESIGN w/ AUTO

RECEPTACLE

J103
DF40C-80DS-0.4V(51)

#MIPI DSI/CSI Z:100 OHM
#LVDS Z:100 OHM

DSI_CLK_N
DSI_CLK_P
DSI_D0_N
DSI_D0_P
DSI_D1_N
DSI_D1_P
DSI_D2_N
DSI_D2_P
DSI_D3_N
DSI_D3_P
CSI_D1_P
CSI_D1_N
CSI_D0_P
CSI_D0_N
CSI_CLK_P
CSI_CLK_N

LVDS_TX3_P
LVDS_TX3_N
LVDS_TX2_P
LVDS_TX2_N
LVDS_CLK_P
LVDS_CLK_N
LVDS_TX1_P
LVDS_TX1_N
LVDS_TX0_P
LVDS_TX0_N

USB1_RXN
USB1_RXP
USB1_TXN
USB1_TXP
#USB3.0 Z:90 OHM
USB1_VBUS_3V3
USB1_DN
USB1_DP
USB1_ID
USB2_VBUS_3V3
USB2_DN
USB2_DP
USB2_ID
ADC_IN0
ADC_IN1
ADC_IN2
ADC_IN3

TP104
POR_B
TAMPER1
TAMPER0
PMIC_ON_REQ
CLKIN1
CLKIN2
PMIC_STBY_REQ
ONOFF
SYS_nRST

GND

I2C IO EXP

VDD_3V3

C102 0.1uF 35V
C101 0.1uF 35V

#PU RES for IRQ

U101
PCAL6524HEAZ
1 MHz I2C (Fm+)

#OD, PU MX93
BUF_POR
EXP_nIRQ
TCPC1_nINT
TCPC2_nINT

#Share IRQ due to TCPC level trigger rather edge trigger

#1 MHz I2C I/F for IRQ fast response!!!

I2C2_SCL
I2C2_SDA
I2C1_SCL
I2C1_SDA

P0_0 TCPC_nINT
P0_1 RTC_nINTA
P0_2 PCIE_nWAKE
P0_3 M2_UART_nWAKE
P0_4 HP_DET
P0_5 EXP_BTN1
P0_6 EXP_BTN2
P0_7 DSI_CTP_nINT

P1_0 EXP_PWREN
P1_1 AUD_nINT
P1_2 M2_nALERT
P1_3
P1_4
P1_5 EXT1_PWREN
P1_6 EXT2_PWREN
P1_7 ENET1_nRST

P2_0 ENET2_nRST
P2_1 CTP_RST
P2_2 M2_nRST
P2_3 M2_nDIS2
P2_4 M2_nDIS1
P2_5 USB1_SS_SEL
P2_6 USB1_SS_XSD
P2_7 USB2_SEL

#I2C ADDR: 0b01000[10]x

VDD_3V3

C105 0.1uF 35V

U103
ADP5585ACPZ-00-R7

BUF_POR
EXP_nIRQ1

I2C2_SCL
I2C2_SDA
I2C1_SCL
I2C1_SDA

R0 CSI_nRST
R1 AUD_PWREN
R2 PDM/MQS_SEL
R3 LVDS_BLT_PWM
R4 EXP_SEL
C0 CAN_STBY
C1 DSI_EN
C2 DSI_BLT_PWM
C3 LVDS_BLT_EN
C4 DSI_CTP_nRST

#1 MHz I2C I/F for IRQ fast response!!!

#I2C ADDR: 0b0110100x

GND

SHARED PIN w/ EXP

VDD_3V3

C103 1uF 16V
C104 0.1uF 35V

U102
TMUX1574RSVR

CODEC

GPIO_IO16
GPIO_IO19
GPIO_IO20
GPIO_IO26

SAI3_TXC
SAI3_TXD
SAI3_RXD
SAI3_TXFS

EXP_GPIO_IO16
EXP_GPIO_IO19
EXP_GPIO_IO20
EXP_GPIO_IO26

SEL=H: SxB->Dx
SEL=L: SxA->Dx
EXP_SEL

RPi

R140 10K 5%
R141 10K 5%

GND

VDD_3V3

C119 1uF 16V
C120 0.1uF 35V

U106
TMUX1574RSVR

M.2 802.15.4

GPIO_IO08
GPIO_IO09
GPIO_IO10
GPIO_IO11

SPI3_CS0
SPI3_MISO
SPI3_MOSI
SPI3_CLK

EXP_GPIO_IO08
EXP_GPIO_IO09
EXP_GPIO_IO10
EXP_GPIO_IO11

SEL=L: SxA->Dx
SEL=H: SxB->Dx
EXP_SEL

RPi

R157 10K 5%

GND

VDD_3V3

R139 10K 5%
R156 18K 1%
R155 15K 1%

PMIC_nINT
SD3_nRST

GND

VDD_3V3

C121 0.1uF 35V
C122 0.1uF 35V

U107 DNP
PCA9617ADPJ

MX_I2C1_SCL
MX_I2C1_SDA

I2C1_SCL_BUF
I2C1_SDA_BUF

FM+ I2C REPEATER

#ONLY I2C MODE can be used, remove while I3C enabled.

VDD_3V3

GND

VDD_3V3

C106 1uF 16V
C107 0.1uF 35V

U104
TMUX1574RSVR

CAN2

GPIO_IO17
GPIO_IO21
GPIO_IO25
GPIO_IO27

SAI3_MCLK
CTP_INT
CAN2_TX
CAN2_RX

EXP_GPIO_IO17
EXP_GPIO_IO21
EXP_GPIO_IO25
EXP_GPIO_IO27

SEL=L: SxA->Dx
SEL=H: SxB->Dx
EXP_SEL

RPi

R142 10K 5%

GND

VDD_1V8

C109 0.1uF 35V

U105
74AUP1G07GW

POR_B
#BUF w/ OD

R145 10K 5%

BUF_POR

VDD_3V3

MX_I2C1_SCL
MX_I2C1_SDA

I2C1_SCL_BUF
I2C1_SDA_BUF

BUF

I3C1_SCL
I3C1_SDA

I3C

I2C1_SCL
I2C1_SDA

I2C

GND

NXP

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Austin, TX 78735-8598

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Designer: NXP SE	Drawing Title: MCIMX93-BB <MCIMX93-EVK>		
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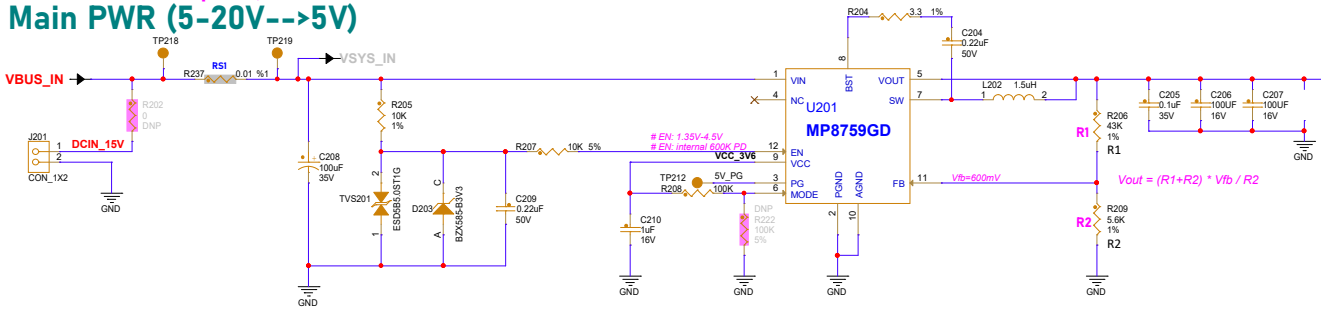
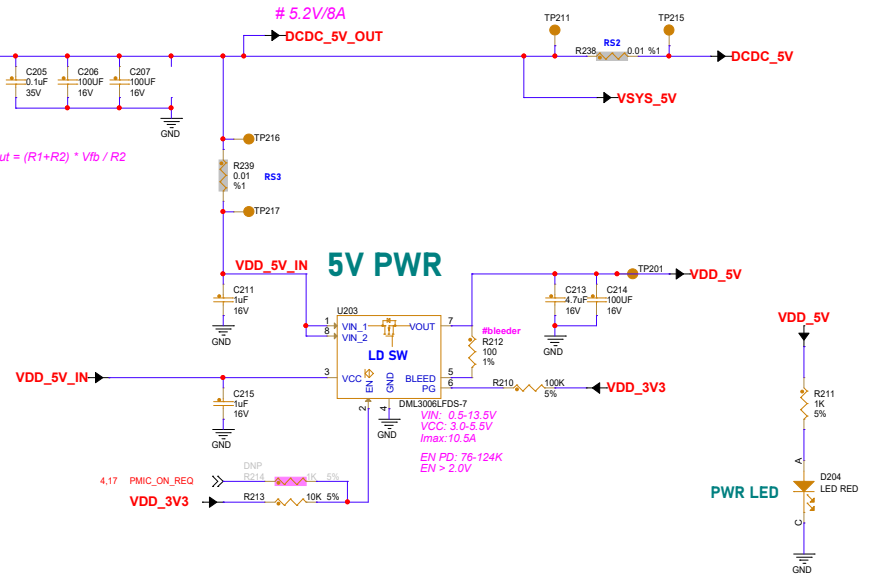
Approved: <Approver>	Size C	Document Number SCH-51961 PDF: SPF-51961	Rev B5
	Date: Monday, September 04, 2023	Sheet 4 of 19	

SYSTEM POWER

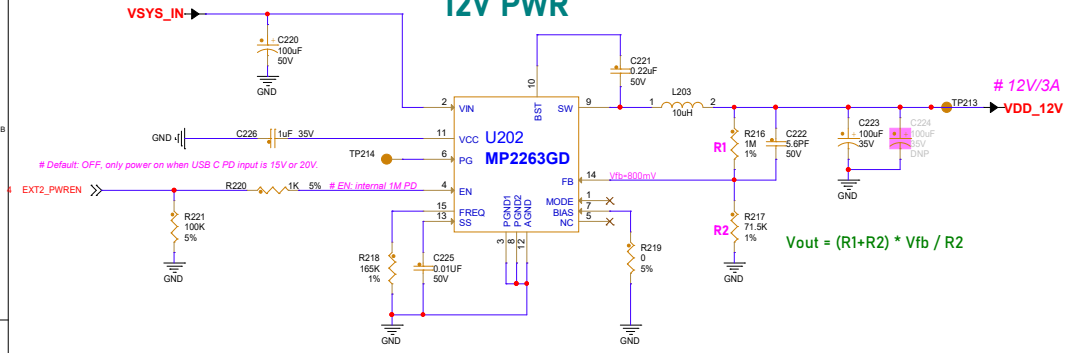
When PER 12V is required, VBUS_IN must be at least 12V!!!

Main PWR (5-20V-->5V)



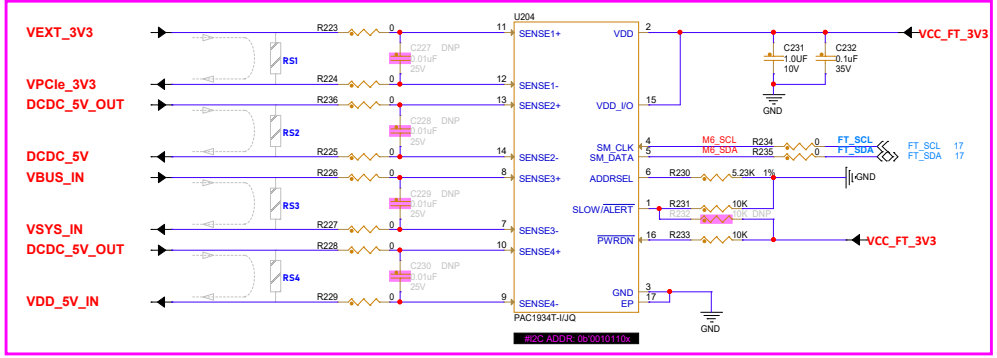


12V PWR



ONLY FOR Base Board Power Measurement

Remove if not required!!!



SOM SCREW

BH201 SMTSO-M2
BH202 SMTSO-M2
BH203 SMTSO-M2
BH204 SMTSO-M2

BB SCREW

BH205 STANDOFF M2.5 DNP
BH206 STANDOFF M2.5 DNP
BH207 STANDOFF M2.5 DNP
BH208 STANDOFF M2.5 DNP

GND Testpoints

TP202 TP204 TP206 TP208
TP210 TP203 TP205 TP207 TP209

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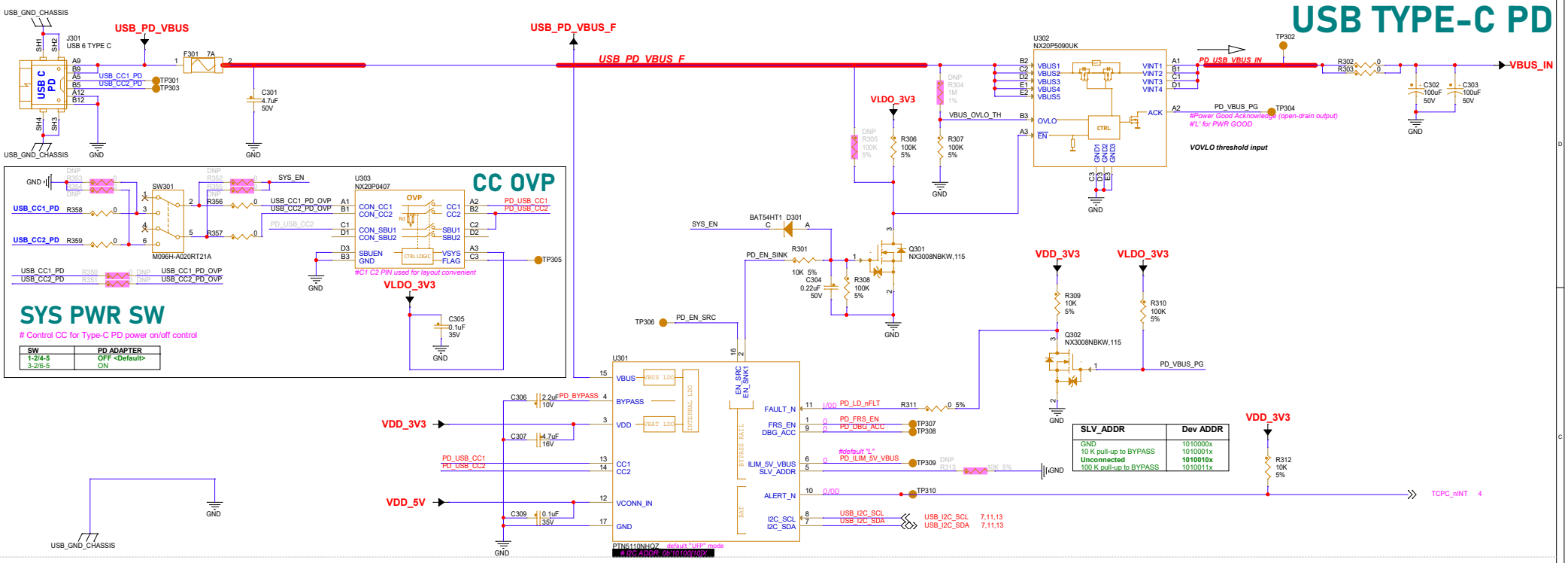
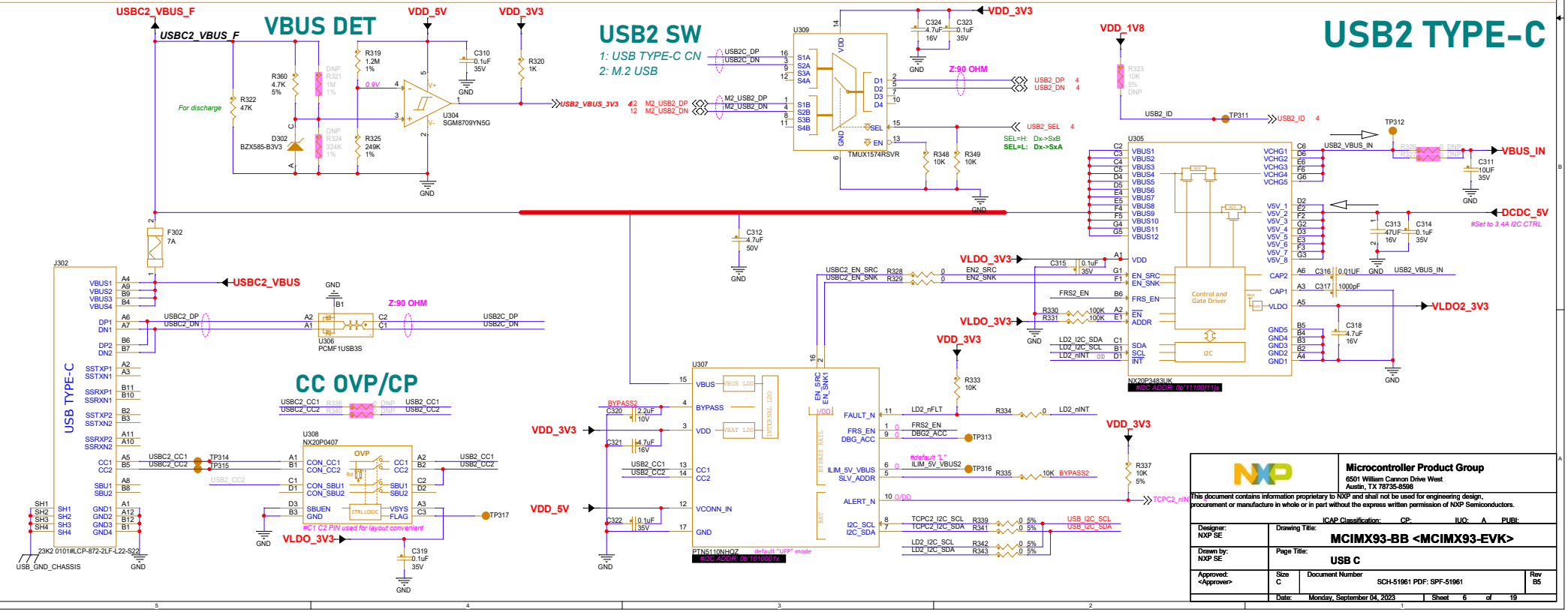
	Date: Monday, September 04, 2023	Sheet 5 of 19	

USB TYPE-C PD



USB2 TYPE-C



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Approved: <Approver>	Size: C	Document Number: SCH-51961 PDF: SPF-51961	Rev: B5
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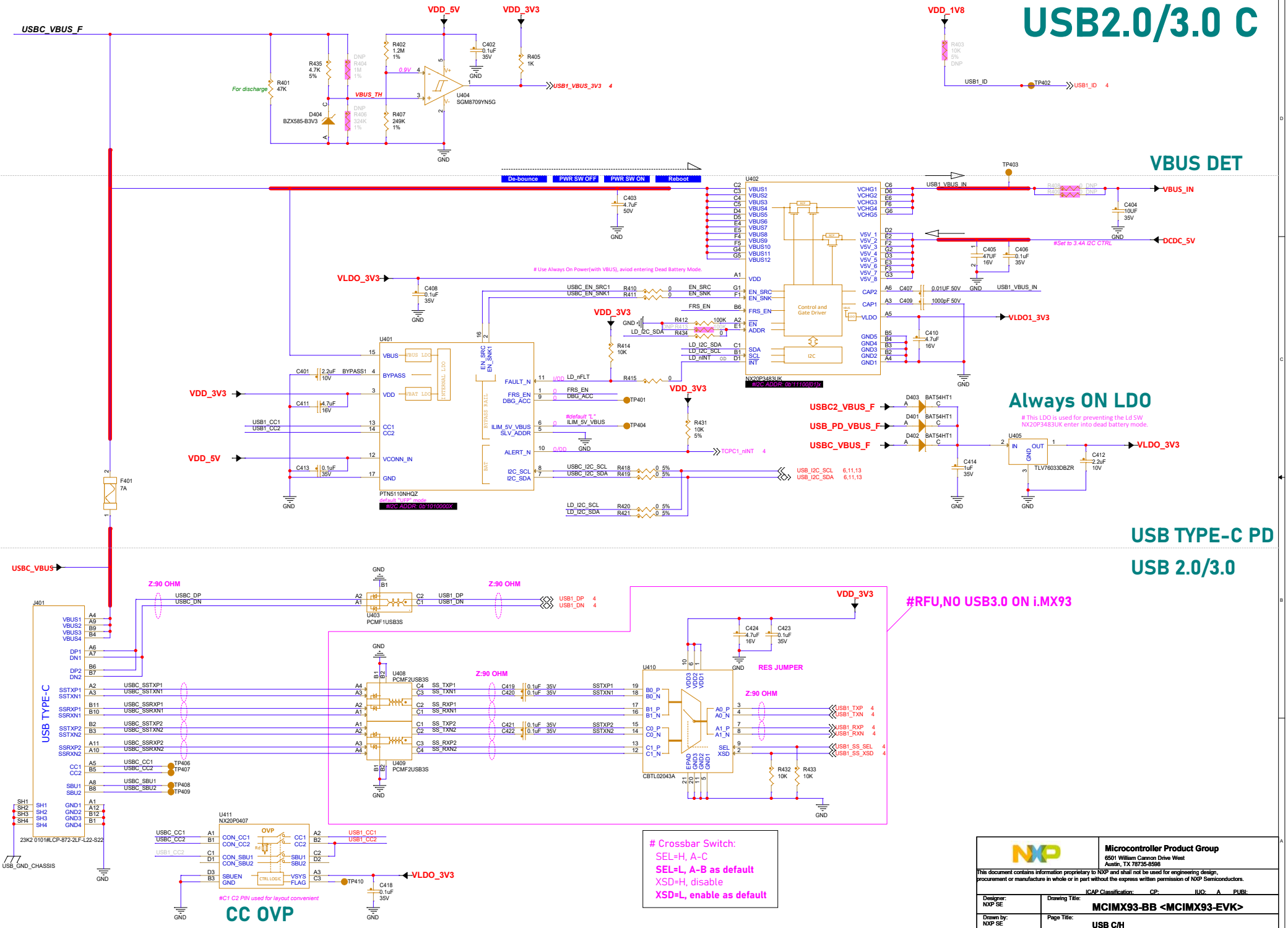
USB2.0/3.0 C

VBUS DET

Always ON LDO

USB TYPE-C PD

USB 2.0/3.0



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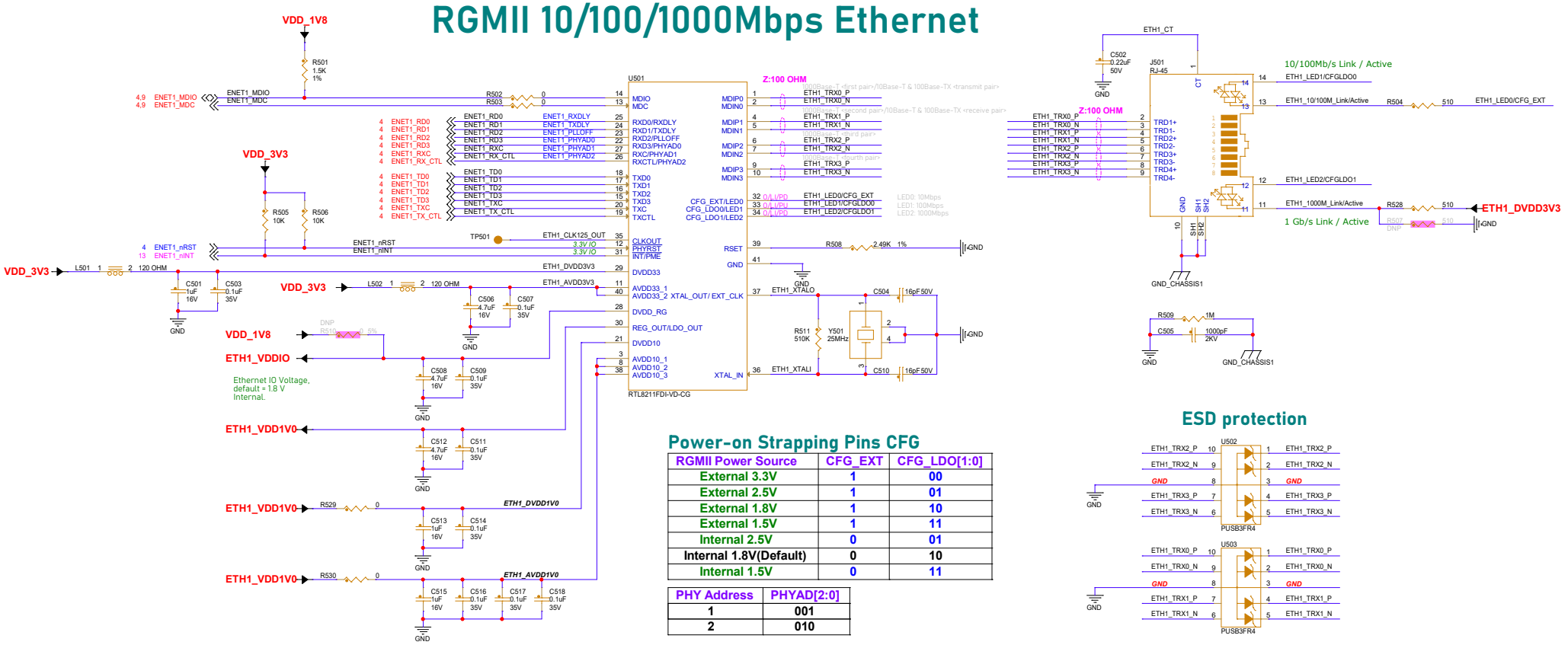
Drawn by: NXP SE	Page Title: USB C/H		
Approved: <Approver>	Size C	Document Number SCH-51961 PDF: SPF-51961	Rev B5
	Date: Monday, September 04, 2023	Sheet 7 of 19	

RGMII 10/100/1000Mbps Ethernet

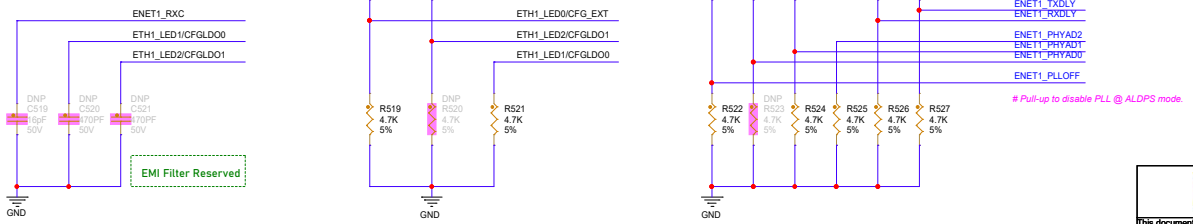


Power-on Strapping Pins CFG

RGMII Power Source	CFG_EXT	CFG_LDO[1:0]
External 3.3V	1	00
External 2.5V	1	01
External 1.8V	1	10
External 1.5V	1	11
Internal 2.5V	0	01
Internal 1.8V(Default)	0	10
Internal 1.5V	0	11

PHY Address	PHYAD[2:0]
1	001
2	010

ESD protection



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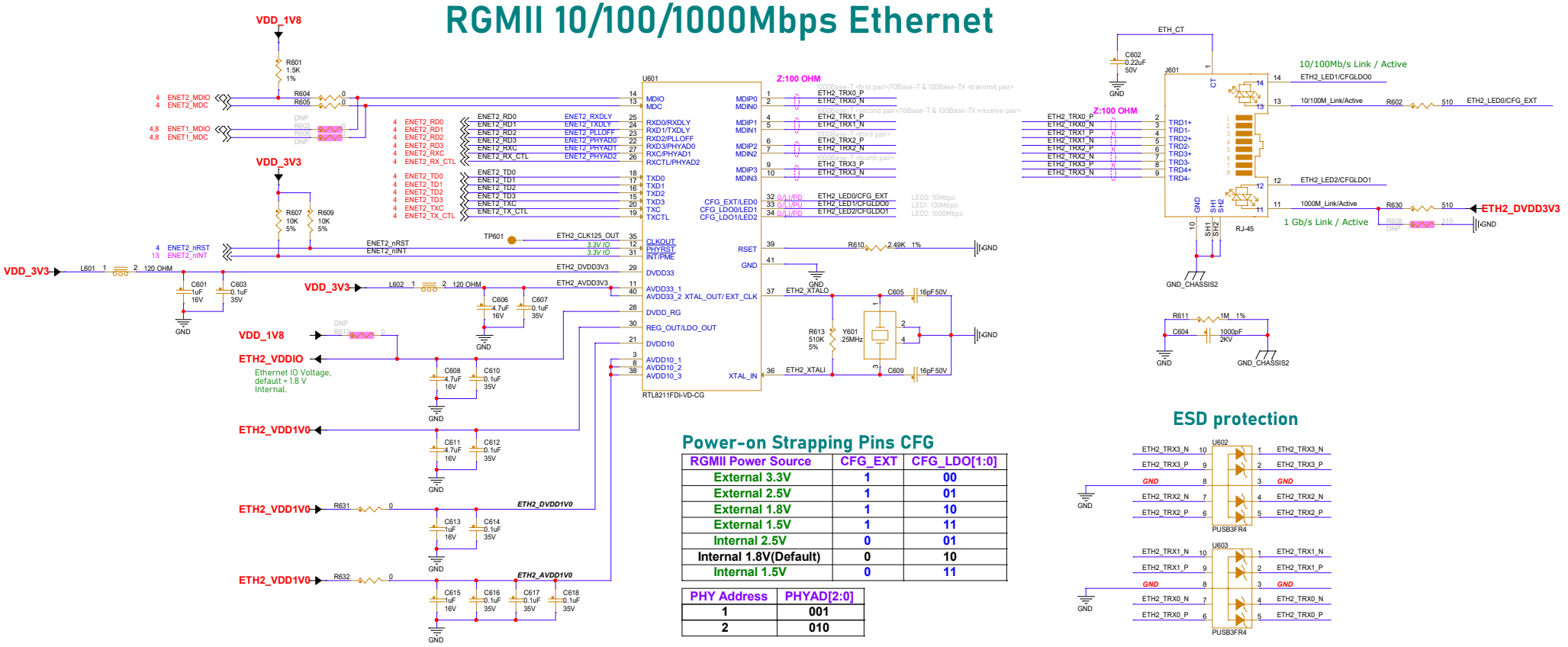
	Date: Monday, September 04, 2023	Sheet 8 of 19	

RGMII 10/100/1000Mbps Ethernet

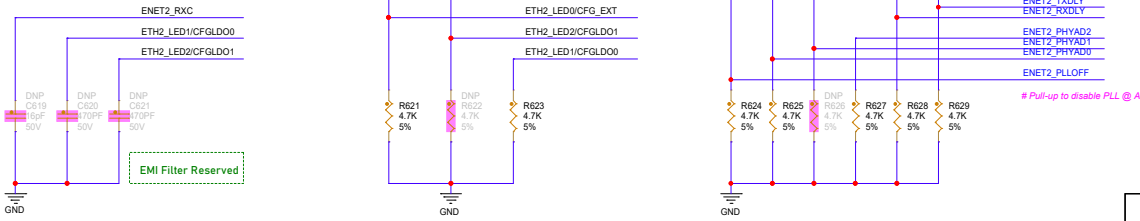


Power-on Strapping Pins CFG

RGMII Power Source	CFG_EXT	CFG_LDO[1:0]
External 3.3V	1	00
External 2.5V	1	01
External 1.8V	1	10
External 1.5V	1	11
Internal 2.5V	0	01
Internal 1.8V(Default)	0	10
Internal 1.5V	0	11

PHY Address	PHYAD[2:0]
1	001
2	010

ESD protection



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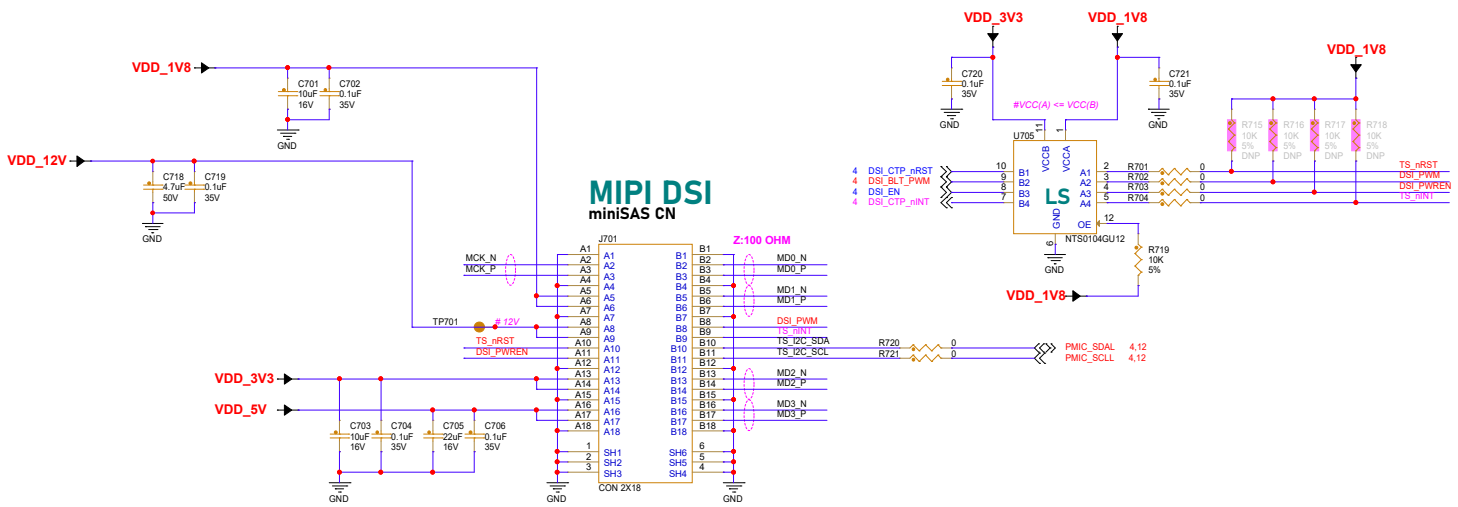
Drawn by: NXP SE	Page Title: ENET2
Approved: <Approver>	Size C; Document Number SCH-51961 PDF: SPF-51961; Rev B5
	Date: Monday, September 04, 2023; Sheet 9 of 19

Microcontroller Product Group
6501 William Cannon Drive West
Austin, TX 78735-8598

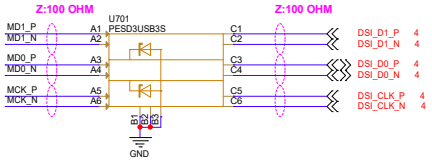
ICAP Classification: CP: IUO: A PUBI:

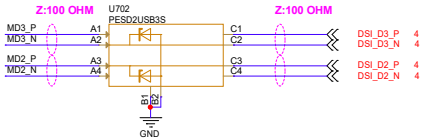
LVDS/MIPI DSI

MIPI DSI
miniSAS CN

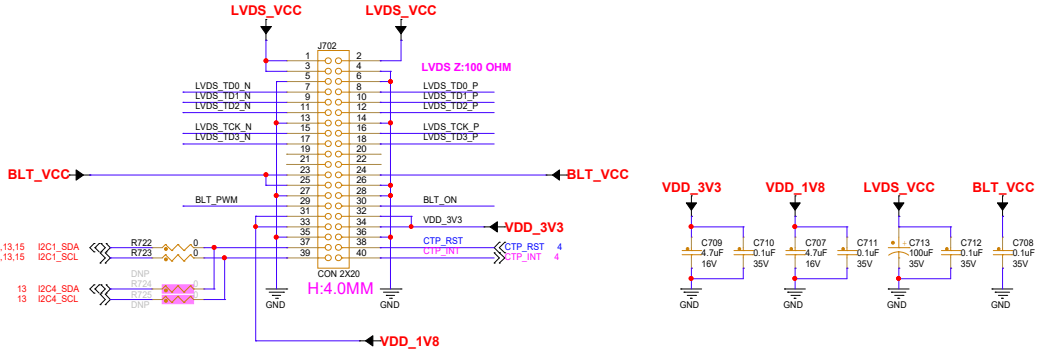


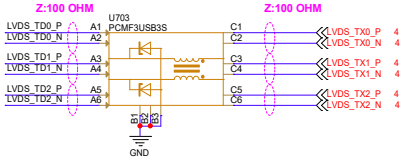
CMF+ESD

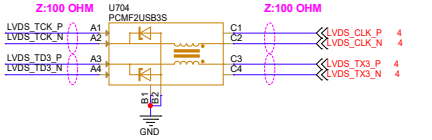


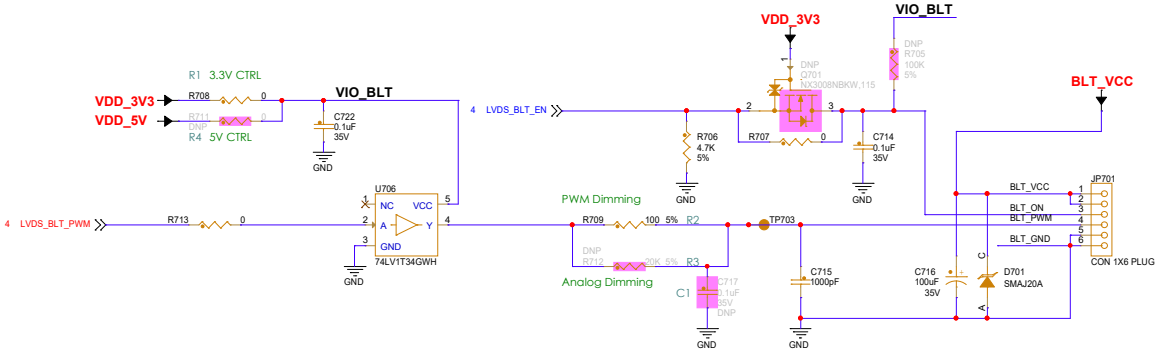


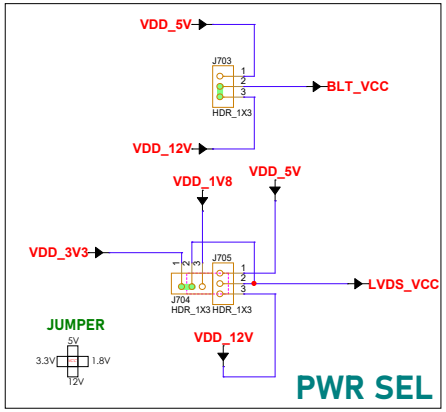
LVDS
LVDS DATA FORMAT VESA JEITA











LVDS LCD BLT

Dimming CTRL

ITEM	INSTALL	DNP	NOTE
3.3V PWM Dimming	R1, R2	R4,R3,C1	PWM frequency according SPEC
5.0V PWM Dimming	R4,R2	R1,R3,C1	PWM frequency according SPEC
3.3V Analog Dimming	R1,R3,C1	R2,R4	0<Vadj<3.3V
5.0V Analog Dimming	R4,R3,C1	R1,R2	0<Vadj<5.0V

Microcontroller Product Group
6501 William Cannon Drive West
Austin, TX 78735-8598

ICAP Classification: CP: IUO: A PUBI:

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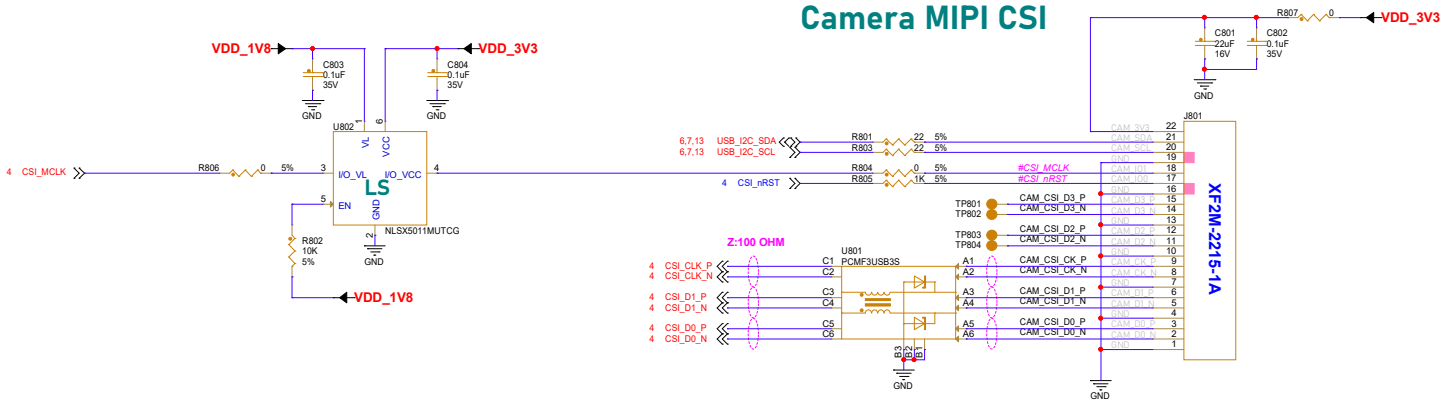
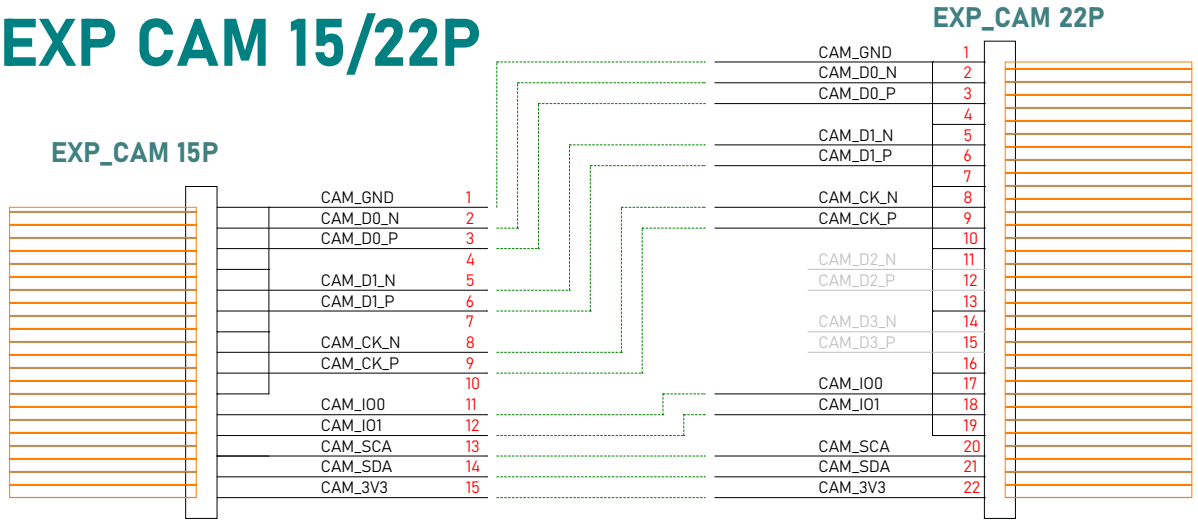
Drawn by: NXP SE	Page Title: MIPI/LVDS		
Approved: <Approver>	Size C	Document Number SCH-51961 PDF: SPF-51961	Rev B5
	Date: Monday, September 04, 2023	Sheet 10 of 19	

MIPI CSI

Camera MIPI CSI



EXP CAM 15/22P



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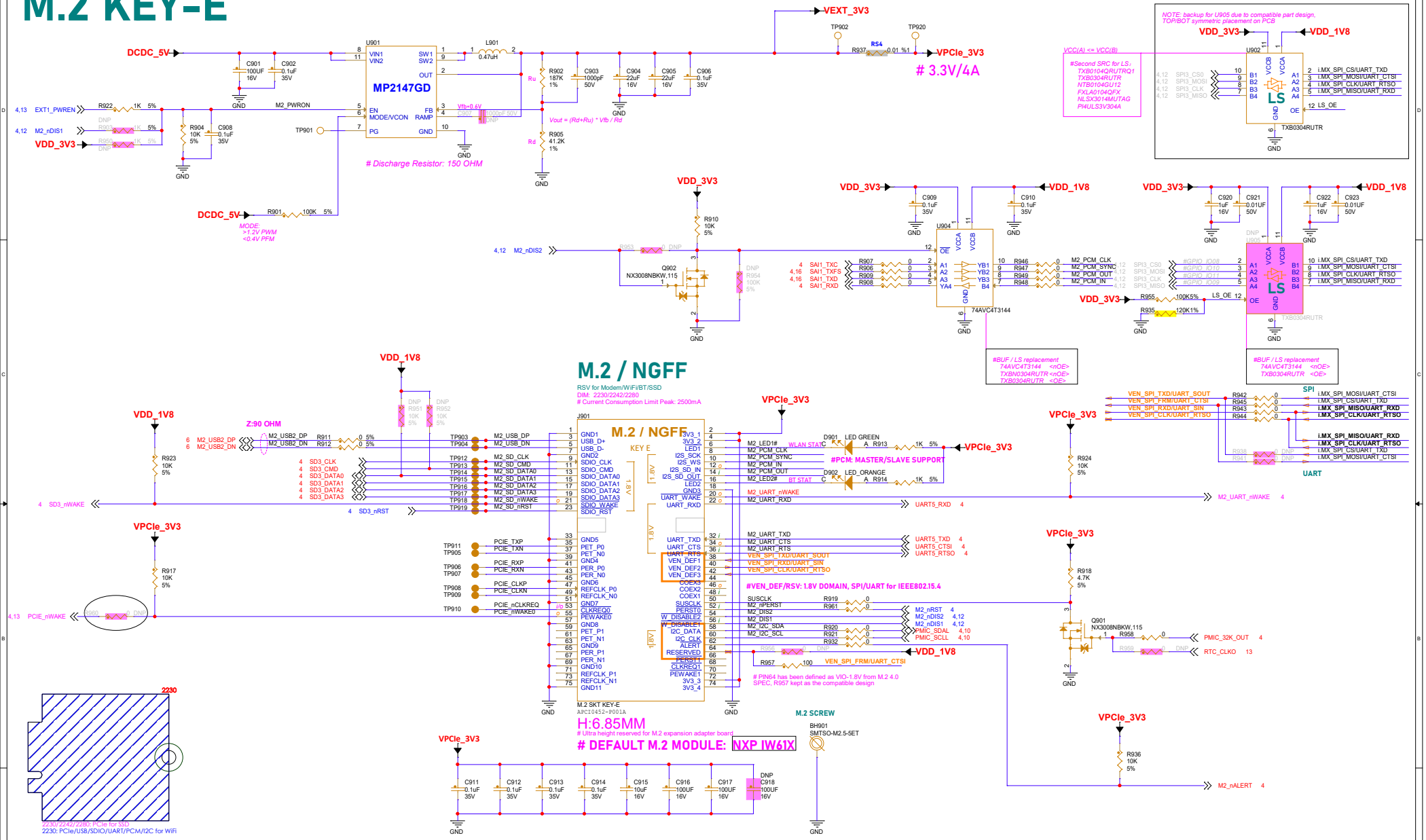
Drawn by: NXP SE	Page Title: MIPI CSI	
Approved: <Approver>	Size C / Document Number SCH-51961 PDF: SPF-51961	Rev B5
	Date: Monday, September 04, 2023	Sheet 11 of 19

M.2 KEY-E



Key ID	Pin	Interface	Key Definition
A	8-15	2x PCIe x1 / USB 2.0 / I2C / DP x4	Display Port Based Connectivity
B	12-19	PCIe x2 / SATA / USB 2.0 / USB 3.1 Gen1 / HSIC / SSIC / Audio / UIM / I2C / SMBus	WWAN/SSD/Others Primary Key
C	16-23	PCIe/M-PCIe / USB 2.0 / USB 3.1 Gen1 / SSIC / I2C-SlimBUS / UIM / ANTCTL	WWAN Key
D	20-27	Reserved for Future Use (RFU)	RFU
E	24-31	2x PCIe x1 / USB 2.0 / I2C / SDIO / UART / PCM	SDIO Based Connectivity
F	28-35	Future Memory Interface (FMI)	Future Memory Interface
G	39-46	Not Used for M.2; for Custom/Non-Standard Apps	Generic (Not used for M.2)
H	43-50	Reserved for Future Use (RFU)	RFU
J	47-54	Reserved for Future Use (RFU)	RFU
K	51-58	Reserved for Future Use (RFU)	RFU
L	55-62	Reserved for Future Use (RFU)	RFU
M	59-66	PCIe x4 / SATA / SMBus	SSD 4 Lane PCIe

i.MX93 GPIO8-11

#GPIO_IO08	#SPI3_CS	#UART7_TXD
#GPIO_IO09	#SPI3_MISO	#UART7_RXD
#GPIO_IO10	#SPI3_MOSI	#UART7_CTS <I>
#GPIO_IO11	#SPI3_CLK	#UART7_RTS <O>

IW61X GPIO12-15

#GPIO_IO15	#SPI_TXD	#UART2_SOUT
#GPIO_IO14	#SPI_RXD	#UART2_SIN
#GPIO_IO13	#SPI_FRM	#UART2_RTS <O>
#GPIO_IO12	#SPI_CLK	#UART2_CTS <I>

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	Date: Monday, September 04, 2023	Sheet 12 of 19	

IMU: *Accelerometer/Gyroscope (w/o eCompass)*

#I3C SUPPORT

RFU BTN JUMPER

EXP GPIO

MicroSD 3.0

BTN / RFU

RGB LED w/ PWM

TAMPER

I2C CN

ADC x4 CH

Ext. RTC

OE	A	Y	NOTE
H	H	H	Normal Operation, No card detected
H	L	L	Normal Operation, card insert
L	H	H	Simulation, card plug-out
L	L	H	No card at slot

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Drawn by: NXP SE	Page Title: MicroSD/IMU/MFi/RPi/ADC
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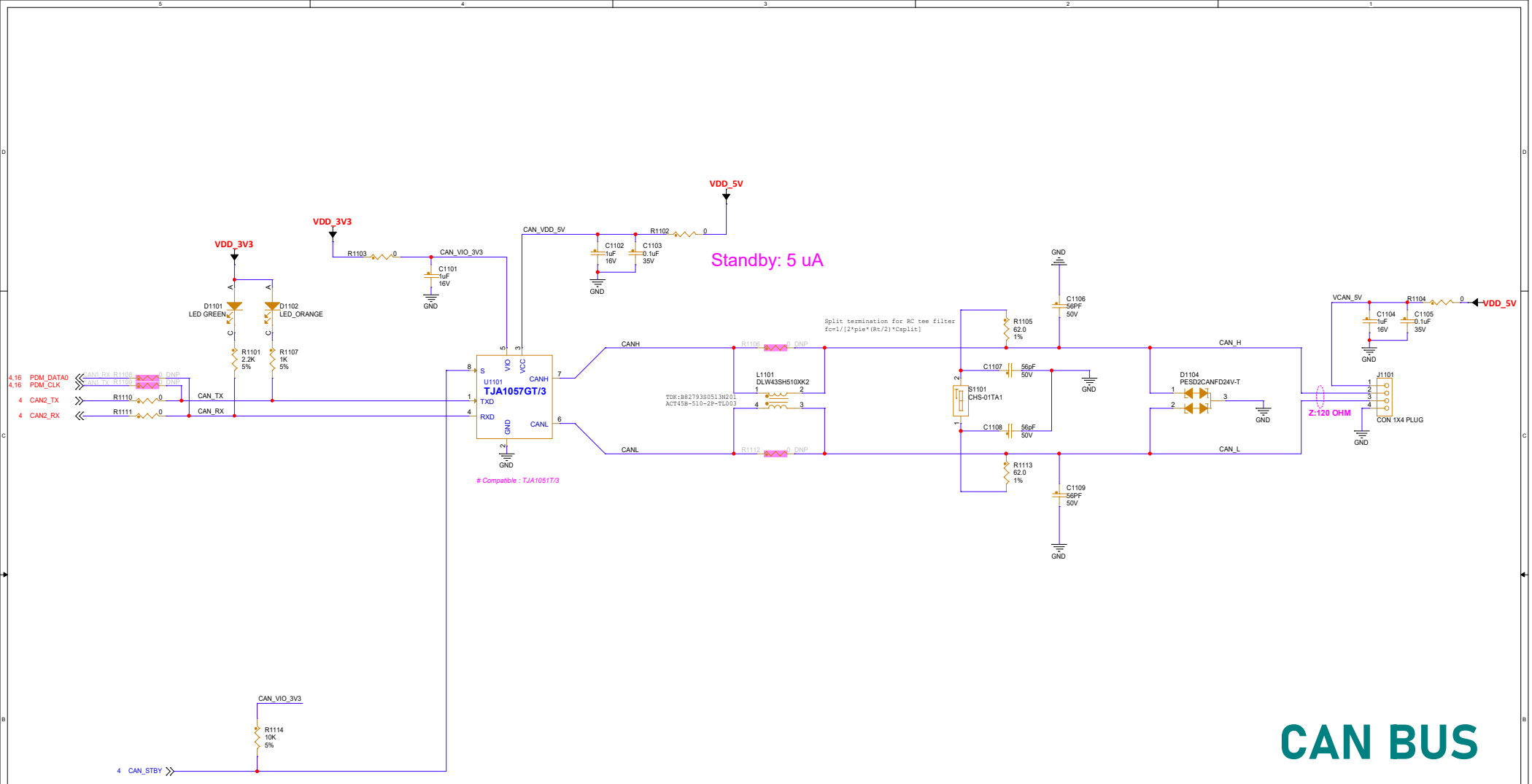

CAN BUS

NXP	Microcontroller Product Group 6501 William Cannon Drive West Austin, TX 78735-8598	
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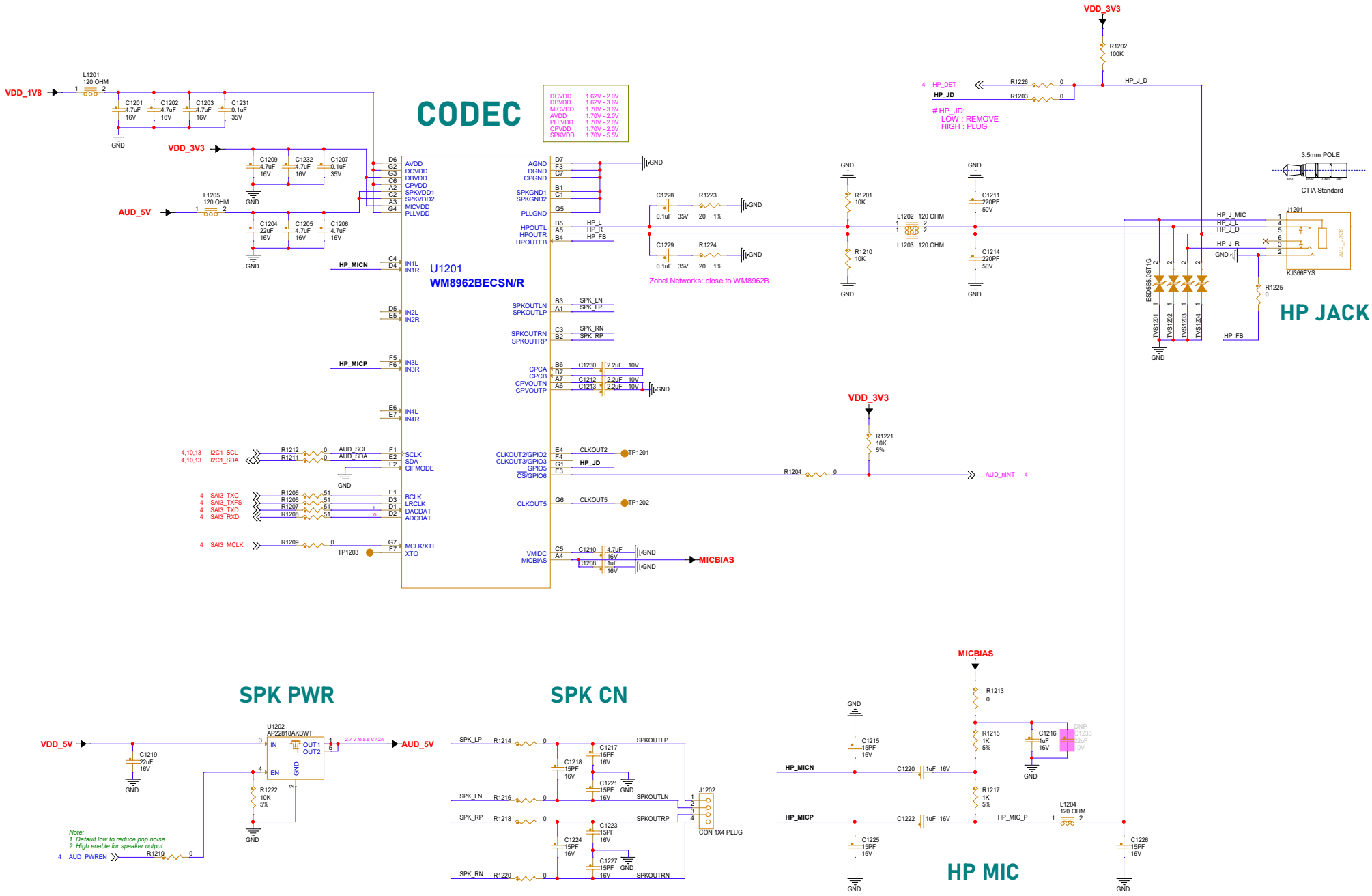
Approved: <Approver>	Size C / Document Number SCH-51961 PDF: SPF-51961	Rev B5
	Date: Monday, September 04, 2023	Sheet 14 of 19



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Drawn by: NXP SE	Page Title: CODEC		
Approved: <Approver>	Size C	Document Number SCH-51961 PDF: SPF-51961	Rev B5
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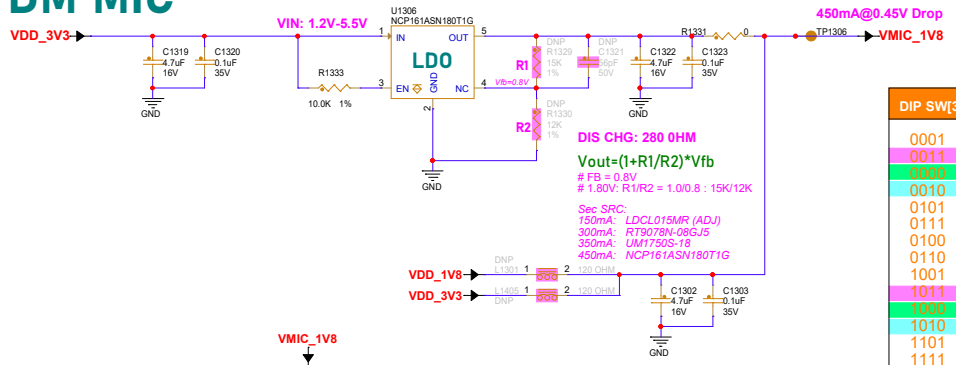
PDM MIC

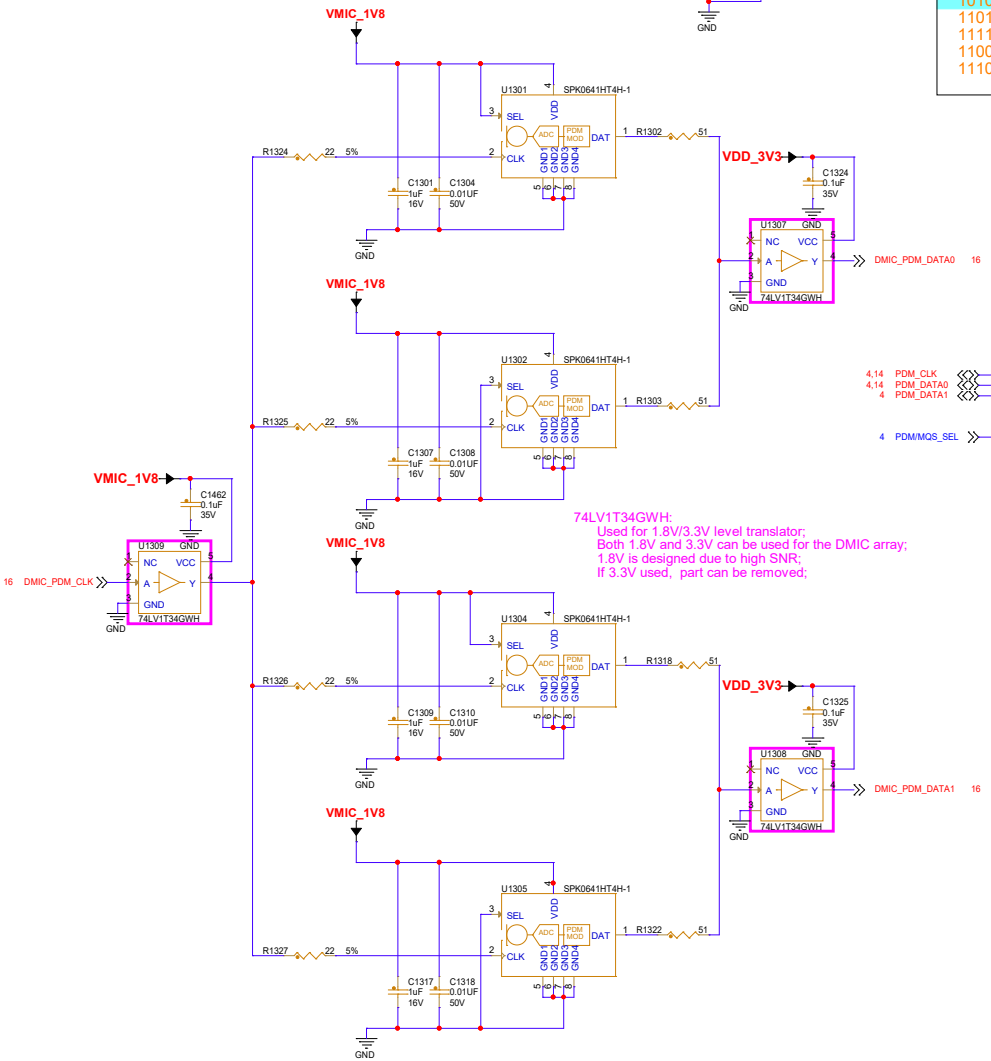
LDO 1.8V for DMIC



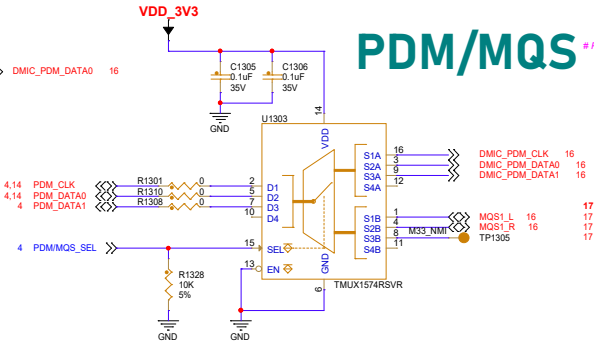
BOOT MODE CFG

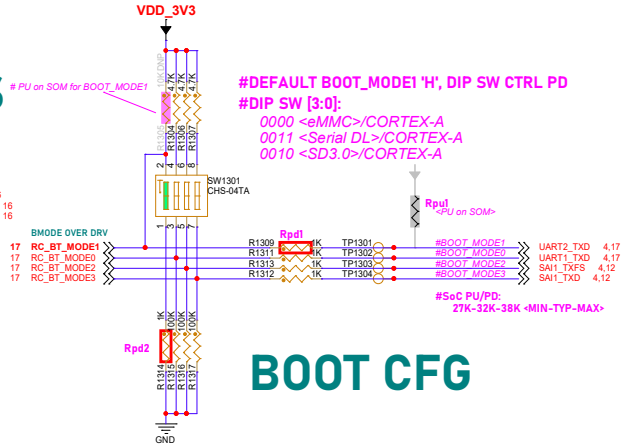
i.MX93 BOOT MODE

DIP SW[3:0]	BOOT_MODE[3:0]	BOOT CORE	BOOT DEVICE	COMMENT
0001	0000	Cortex-A55	From internal fuses	
0011	0001	Cortex-A55	Serial Downloader	USB1/2
0000	0010	Cortex-A55	USDHC1 8-bit eMMC 5.1	
0010	0011	Cortex-A55	USDHC2 4-bit SD3.0	
0101	0100	Cortex-A55	FlexSPI Serial NOR	with SFDP (JESD-216) discoverable parameters
0111	0101	Cortex-A55	FlexSPI Serial NAND 2K page	
0100	0110	Cortex-A55	Infinite Loop	
0110	0111	Cortex-A55	Test Mode	
1001	1000	Cortex-M33	From internal fuses	
1011	1001	Cortex-M33	Serial Downloader	USB1
1000	1010	Cortex-M33	USDHC1 8-bit eMMC 5.1	
1010	1011	Cortex-M33	USDHC2 4-bit SD3.0	
1101	1100	Cortex-M33	FlexSPI Serial NOR	with SFDP (JESD-216) discoverable parameters
1111	1101	Cortex-M33	FlexSPI Serial NAND 2K page	
1100	1110	Cortex-M33	Infinite Loop	
1110	1111	Cortex-M33	Test Mode	



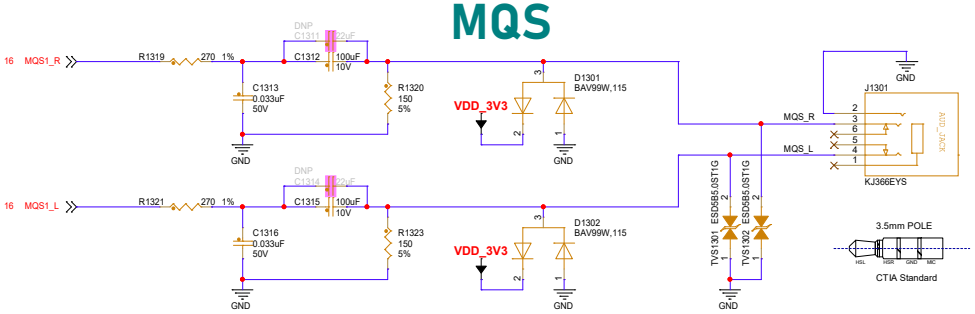
PDM/MQS





BOOT CFG

MQS



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REMOTE DEBUG

REMOVE THIS PAGE IF NOT USED!!!

DBG USB C

FT PWR

System ID (Back up)

UART BUF

i.MX SoC RC I/F

BOOT MODE RC

ONOFF / RST RC

JTAG DBG

SYS TST/ MONITOR

NXP RDPM I/F

(Romote Debug & Power Measurement Interface)

NXP RDPM I/F

(Romote Debug & Power Measurement Interface)

Make sure that power meas status need to recover to default status once system reset

UI LED

IO EXP

PWR MEAS B2B CN

JTAG HDR

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Drawn by: NXP SE	Page Title:	REMOTE DEBG	
Approved: <Approver>	Size: D	Document Number: SCH-51961 PDF: SPF-51961	Rev: B5
	Date: Monday, September 04, 2023	Sheet 17 of 19	

NOTE:

I2C DEV TABLE

BOARD	PART	DEVICE	I2C ADDR <7bit>	PORT	SPEED	VOL	DESCRIPTION
BB	U101	PCAL6524HEAZ	0x22 (0b'01000[10]x)	MX-I2C2 /I2C1	1MHz Fm+	3.3V	**IO EXP for IRQ/OUTPUT**
BB	U103	ADP5585ACPZ-00-R7	0x34 (0b'0110100x)	MX-I2C2 /I2C1	1MHz Fm+	3.3V	IO EXP for OUTPUT
BB	U301	PTN5110NHQZ	0x52 (0b'10100[10]x)	MX-I2C1 /I2C3/4	1MHz Fm+	3.3V	USB C PD PHY
BB	U307	PTN5110NHQZ	0x51 (0b'10100[01]x)	MX-I2C1 /I2C3/4	1MHz Fm+	3.3V	USB C PD PHY
BB	U401	PTN5110NHQZ	0x50 (0b'10100[00]x)	MX-I2C1 /I2C3/4	1MHz Fm+	3.3V	USB C PD PHY
BB	U402	NX20P3483UK	0x71 (0b'11100[01]x)	MX-I2C1 /I2C3/4	1MHz Fm+	3.3V	USB Load Switch
BB	U305	NX20P3483UK	0x73 (0b'11100[11]x)	MX-I2C1 /I2C3/4	1MHz Fm+	3.3V	USB Load Switch
BB	U1001	LSM6DSOXTR	0x6A (0b'110101[0]x)	MX-I2C1 /I2C3	I3C-12.5 Mbps/I2C-400KHz	3.3V	IMU (I3C support)
BB	U1201	WM8962BECSN/R	0x1A (0b'0011010x)	MX-I2C1 /I2C4	526KHz	3.3V	Audio CODEC
BB		AR0144	0x10 (0b'0010000x)	MX-I2C3	400KHz	3.3V	MIPI CSI Camera
BB				MX-I2C1 /I2C4	400KHz	3.3V	CTP/LCD <LVDS>
BB				MX-I2C1	400KHz	1.8V	CTP/LCD <MIPI DSI>
BB				MX-I2C1	400KHz	1.8V	M.2 / NGFF KEY-E
BB	U1409	PCA9655EMTTXG	0x21 (0b'0100001x)	FTDI-I2C	1MHz Fm+	3.3V	RDPM IO EXP
BB	U204	PAC1934T	0x16 (0b'0010110x)	FTDI-I2C	1MHz Fm+	3.3V	Base Board Power Monitor
BB	U1201	WM8960 (EVK REV A)	0x1A (0b'0011010x)	MX-I2C1 /I2C4	526KHz	3.3V	Audio CODEC
BB	U1004	PCF2131TF	0x53 (0b'1010011x)	MX-I2C3	400KHz	3.3V	Ext RTC
SOM	U701	PCA9451AHN	0x25 (0b'0100101x)	MX-I2C2	1MHz Fm+	3.3V	PMIC
SOM	U902	PAC1934T	0x11 (0b'0010001x)	FTDI-I2C	1MHz Fm+	3.3V	Power Monitor
SOM	U904	PAC1934T	0x12 (0b'0010010x)	FTDI-I2C	1MHz Fm+	3.3V	Power Monitor
SOM	U907	PAC1934T	0x13 (0b'0010011x)	FTDI-I2C	1MHz Fm+	3.3V	Power Monitor
SOM	U911	PAC1934T	0x14 (0b'0010100x)	FTDI-I2C	1MHz Fm+	3.3V	Power Monitor
SOM	U912	PAC1934T	0x15 (0b'0010101x)	FTDI-I2C	1MHz Fm+	3.3V	Power Monitor
SOM	U909	ADP5585ACPZ-00-R7	0x34 (0b'0110100x)	FTDI-I2C	1MHz Fm+	3.3V	Power Monitor
SOM	U913	PCT2075	0x48 (0b'1001000x)	FTDI-I2C	1MHz Fm+	3.3V	Power Monitor

MIPI CSI Camera:
- Camera: AR1335 — 0x36 (0b'0110110x)
- Camera: AR0144 — 0x10 (0b'0010000x)
- Ext ISP: AP1302 — 0x3C (0b'0111100x)
- IO EXP: ADP5585ACPZ-01-R7 — 0x34 (0b'0110100x)

CTP/LCD <MIPI DSI>:
- DSI->HDMI: ADV7535 — 0x3D (0b'0111101x)

M.2 / NGFF KEY-E:
- IO EXP: PCAL6408AEX1Z — 0x20 (0b'0100000x)

Microcontroller Product Group
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Drawn by: NXP SE	Page Title: NOTE	
Approved: <Approver>	Size C / Document Number SCH-51961 PDF: SPF-51961	Rev B5
	Date: Monday, September 04, 2023	Sheet 18 of 19

i.MX93 IOMUX:

IOPAD	Alt0	Alt1	Alt2	Alt3	Alt4	Alt5	Alt6	Alt7	DEF MUX	PS	PE	IS	IO
RTC_XTALI	bbsmmix.RTC								bbsmmix.RTC				
RTC_XTALO													
PMIC_STBY_REQ	bbsmmix.PMIC_STBY_REQ								ccmsrcgpcmix.PMIC_STBY_REQ				
PMIC_ON_REQ	bbsmmix.PMIC_ON_REQ								bbsmmix.PMIC_ON_REQ				
ONOFF	bbsmmix.ONOFF								bbsmmix.ONOFF				
POR_B	bbsmmix.POR_B								bbsmmix.POR_B				
TAMPER0	bbsmmix.TAMPER0								bbsmmix.TAMPER0				
TAMPER1	bbsmmix.TAMPER1								bbsmmix.TAMPER1				
GPIO_IO00	gpio2.IO[0]	i2c3.SDA	isi.PCLK	lcdif.PCLK	spi6.PCS0	uart5.TX	i2c5.SDA	flexio1.FLEXIO[0]	gpio2.IO[0]				
GPIO_IO01	gpio2.IO[1]	i2c3.SCL	isi.D[0]	lcdif.DE	spi6.SIN	uart5.RX	i2c5.SCL	flexio1.FLEXIO[1]	gpio2.IO[1]				
GPIO_IO02	gpio2.IO[2]	i2c4.SDA	isi.FRAME_VALID	lcdif.VSYNC	spi6.SOUT	uart5.CTS_B	i2c6.SDA	flexio1.FLEXIO[2]	gpio2.IO[2]				
GPIO_IO03	gpio2.IO[3]	i2c4.SCL	isi.LINE_VALID	lcdif.HSYNC	spi6.SCK	uart5.RTS_B	i2c6.SCL	flexio1.FLEXIO[3]	gpio2.IO[3]				
GPIO_IO04	gpio2.IO[4]	tpm3.CH0	pdm.CLK	lcdif.D[0]	spi7.PCS0	uart6.TX	i2c6.SDA	flexio1.FLEXIO[4]	gpio2.IO[4]				
GPIO_IO05	gpio2.IO[5]	tpm4.CH0	pdm.BIT_STREAM[0]	lcdif.D[1]	spi7.SIN	uart6.RX	i2c6.SCL	flexio1.FLEXIO[5]	gpio2.IO[5]				
GPIO_IO06	gpio2.IO[6]	tpm5.CH0	pdm.BIT_STREAM[1]	lcdif.D[2]	spi7.SOUT	uart6.CTS_B	i2c7.SDA	flexio1.FLEXIO[6]	gpio2.IO[6]				
GPIO_IO07	gpio2.IO[7]	spi3.PCS1	isi.D[1]	lcdif.D[3]	spi7.SCK	uart6.RTS_B	i2c7.SCL	flexio1.FLEXIO[7]	gpio2.IO[7]				
GPIO_IO08	gpio2.IO[8]	spi3.PCS0	isi.D[2]	lcdif.D[4]	tpm6.CH0	uart7.TX	i2c7.SDA	flexio1.FLEXIO[8]	gpio2.IO[8]				
GPIO_IO09	gpio2.IO[9]	spi3.SIN	isi.D[3]	lcdif.D[5]	tpm3.EXTCLK	uart7.RX	i2c7.SCL	flexio1.FLEXIO[9]	gpio2.IO[9]				
GPIO_IO10	gpio2.IO[10]	spi3.SOUT	isi.D[4]	lcdif.D[6]	tpm4.EXTCLK	uart7.CTS_B	i2c8.SDA	flexio1.FLEXIO[10]	gpio2.IO[10]				
GPIO_IO11	gpio2.IO[11]	spi3.SCK	isi.D[5]	lcdif.D[7]	tpm5.EXTCLK	uart7.RTS_B	i2c8.SCL	flexio1.FLEXIO[11]	gpio2.IO[11]				
GPIO_IO12	gpio2.IO[12]	tpm3.CH2	pdm.BIT_STREAM[2]	lcdif.D[8]	spi8.PCS0	uart8.TX	i2c8.SDA	sai3.RX_SYNC	gpio2.IO[12]				
GPIO_IO13	gpio2.IO[13]	tpm4.CH2	pdm.BIT_STREAM[3]	lcdif.D[9]	spi8.SIN	uart8.RX	i2c8.SCL	flexio1.FLEXIO[13]	gpio2.IO[13]				
GPIO_IO14	gpio2.IO[14]	uart3.TX	isi.D[6]	lcdif.D[10]	spi8.SOUT	uart8.CTS_B	uart4.TX	flexio1.FLEXIO[14]	gpio2.IO[14]				
GPIO_IO15	gpio2.IO[15]	uart3.RX	isi.D[7]	lcdif.D[11]	spi8.SCK	uart8.RTS_B	uart4.RX	flexio1.FLEXIO[15]	gpio2.IO[15]				
GPIO_IO16	gpio2.IO[16]	sai3.TX_BCLK	pdm.BIT_STREAM[2]	lcdif.D[12]	uart3.CTS_B	spi4.PCS2	uart4.CTS_B	flexio1.FLEXIO[16]	gpio2.IO[16]				
GPIO_IO17	gpio2.IO[17]	sai3.MCLK	isi.D[8]	lcdif.D[13]	uart3.RTS_B	spi4.PCS1	uart4.RTS_B	flexio1.FLEXIO[17]	gpio2.IO[17]				
GPIO_IO18	gpio2.IO[18]	sai3.RX_BCLK	isi.D[9]	lcdif.D[14]	spi5.PCS0	spi4.PCS0	tpm5.CH2	flexio1.FLEXIO[18]	gpio2.IO[18]				
GPIO_IO19	gpio2.IO[19]	sai3.RX_SYNC	pdm.BIT_STREAM[3]	lcdif.D[15]	spi5.SIN	spi4.SIN	tpm6.CH2	sai3.TX_DATA[0]	gpio2.IO[19]				
GPIO_IO20	gpio2.IO[20]	sai3.RX_DATA[0]	pdm.BIT_STREAM[0]	lcdif.D[16]	spi5.SOUT	spi4.SOUT	tpm3.CH1	flexio1.FLEXIO[20]	gpio2.IO[20]				
GPIO_IO21	gpio2.IO[21]	sai3.TX_DATA[0]	pdm.CLK	lcdif.D[17]	spi5.SCK	spi4.SCK	tpm4.CH1	sai3.RX_BCLK	gpio2.IO[21]				
GPIO_IO22	gpio2.IO[22]	usdhc3.CLK	spdif1.IN	lcdif.D[18]	tpm5.CH1	tpm6.EXTCLK	i2c5.SDA	flexio1.FLEXIO[22]	gpio2.IO[22]				
GPIO_IO23	gpio2.IO[23]	usdhc3.CMD	spdif1.OUT	lcdif.D[19]	tpm6.CH1		i2c5.SCL	flexio1.FLEXIO[23]	gpio2.IO[23]				
GPIO_IO24	gpio2.IO[24]	usdhc3.DATA0		lcdif.D[20]	tpm3.CH3	dap.TDO_TRACESWO	spi6.PCS1	flexio1.FLEXIO[24]	gpio2.IO[24]				
GPIO_IO25	gpio2.IO[25]	usdhc3.DATA1	can2.TX	lcdif.D[21]	tpm4.CH3	dap.TCLK_SWCLK	spi7.PCS1	flexio1.FLEXIO[25]	gpio2.IO[25]				
GPIO_IO26	gpio2.IO[26]	usdhc3.DATA2	pdm.BIT_STREAM[1]	lcdif.D[22]	tpm5.CH3	dap.TDI	spi8.PCS1	sai3.TX_SYNC	gpio2.IO[26]				
GPIO_IO27	gpio2.IO[27]	usdhc3.DATA3	can2.RX	lcdif.D[23]	tpm6.CH3	dap.TMS_SWDIO	spi5.PCS1	flexio1.FLEXIO[27]	gpio2.IO[27]				
GPIO_IO28	gpio2.IO[28]	i2c3.SDA						flexio1.FLEXIO[28]	gpio2.IO[28]				
GPIO_IO29	gpio2.IO[29]	i2c3.SCL						flexio1.FLEXIO[29]	gpio2.IO[29]				
CCM_CLKO1	ccmsrcgpcmix.CLKO1				flexio1.FLEXIO[26]	gpio3.IO[26]			ccmsrcgpcmix.CLKO1				
CCM_CLKO2	ccmsrcgpcmix.CLKO2				flexio1.FLEXIO[27]	gpio3.IO[27]			ccmsrcgpcmix.CLKO2				
CCM_CLKO3	ccmsrcgpcmix.CLKO3				flexio2.FLEXIO[28]	gpio4.IO[28]			gpio4.IO[28]				
CCM_CLKO4	ccmsrcgpcmix.CLKO4				flexio2.FLEXIO[29]	gpio4.IO[29]			gpio4.IO[29]				
DAP_TDI	dap.TDI	mqs2.LEFT		can2.TX	flexio2.FLEXIO[30]	gpio3.IO[28]	uart5.RX		dap.TDI				
DAP_TMS_SWDIO	dap.TMS_SWDIO				flexio2.FLEXIO[31]	gpio3.IO[29]	uart5.RTS_B		dap.TMS_SWDIO				
DAP_TCLK_SWCLK	dap.TCLK_SWCLK				flexio1.FLEXIO[30]	gpio3.IO[30]	uart5.CTS_B		dap.TCLK_SWCLK				
DAP_TDO_TRACESWO	dap.TDO_TRACESWO	mqs2.RIGHT		can2.RX	flexio1.FLEXIO[31]	gpio3.IO[31]	uart5.TX		dap.TDO_TRACESWO				
ENET1_MDC	enet_qos.MDC	uart3.DCB_B	i3c2.SCL	usb1.OTG_ID	flexio2.FLEXIO[0]	gpio4.IO[0]			gpio4.IO[0]				
ENET1_MDIO	enet_qos.MDIO	uart3.RIN_B	i3c2.SDA	usb1.OTG_PWR	flexio2.FLEXIO[1]	gpio4.IO[1]			gpio4.IO[1]				
ENET1_TD3	enet_qos.RGMII_TD3		can2.TX	usb2.OTG_ID	flexio2.FLEXIO[2]	gpio4.IO[2]			gpio4.IO[2]				
ENET1_TD2	enet_qos.RGMII_TD2	enet_qos.TX_CLK/.ENET_REF_CLK_ROOT	can2.RX	usb2.OTG_OC	flexio2.FLEXIO[3]	gpio4.IO[3]			gpio4.IO[3]				
ENET1_TD1	enet_qos.RGMII_TD1	uart3.RTS_B	i3c2.PUR	usb1.OTG_OC	flexio2.FLEXIO[4]	gpio4.IO[4]	i3c2.PUR_B		gpio4.IO[4]				
ENET1_TD0	enet_qos.RGMII_TD0	uart3.TX			flexio2.FLEXIO[5]	gpio4.IO[5]			gpio4.IO[5]				
ENET1_TX_CTL	enet_qos.RGMII_TX_CTL	uart3.DTR_B			flexio2.FLEXIO[6]	gpio4.IO[6]			gpio4.IO[6]				
ENET1_TXC	enet_qos.RGMII_TXC	enet_qos.TX_ER			flexio2.FLEXIO[7]	gpio4.IO[7]			gpio4.IO[7]				
ENET1_RX_CTL	enet_qos.RGMII_RX_CTL	uart3.DSR_B		usb2.OTG_PWR	flexio2.FLEXIO[8]	gpio4.IO[8]			gpio4.IO[8]				
ENET1_RXC	enet_qos.RGMII_RXC	enet_qos.RX_ER			flexio2.FLEXIO[9]	gpio4.IO[9]			gpio4.IO[9]				
ENET1_RD0	enet_qos.RGMII_RD0	uart3.RX			flexio2.FLEXIO[10]	gpio4.IO[10]			gpio4.IO[10]				
ENET1_RD1	enet_qos.RGMII_RD1	uart3.CTS_B		lptmr2.ALT1	flexio2.FLEXIO[11]	gpio4.IO[11]			gpio4.IO[11]				
ENET1_RD2	enet_qos.RGMII_RD2			lptmr2.ALT2	flexio2.FLEXIO[12]	gpio4.IO[12]			gpio4.IO[12]				
ENET1_RD3	enet_qos.RGMII_RD3		wakeupmix.flexspi_usdhc_tester_trigger	lptmr2.ALT3	flexio2.FLEXIO[13]	gpio4.IO[13]			gpio4.IO[13]				
ENET2_MDC	enet2.MDC	uart4.DCB_B	sai2.RX_SYNC		flexio2.FLEXIO[14]	gpio4.IO[14]			gpio4.IO[14]				
ENET2_MDIO	enet2.MDIO	uart4.RIN_B	sai2.RX_BCLK		flexio2.FLEXIO[15]	gpio4.IO[15]			gpio4.IO[15]				
ENET2_TD3	enet2.RGMII_TD3		sai2.RX_DATA[0]		flexio2.FLEXIO[16]	gpio4.IO[16]			gpio4.IO[16]				
ENET2_TD2	enet2.RGMII_TD2	enet2.TX_CLK/ENET_REF_CLK_ROOT	sai2.RX_DATA[1]		flexio2.FLEXIO[17]	gpio4.IO[17]			gpio4.IO[17]				
ENET2_TD1	enet2.RGMII_TD1	uart4.RTS_B	sai2.RX_DATA[2]		flexio2.FLEXIO[18]	gpio4.IO[18]			gpio4.IO[18]				
ENET2_TD0	enet2.RGMII_TD0	uart4.TX	sai2.RX_DATA[3]		flexio2.FLEXIO[19]	gpio4.IO[19]			gpio4.IO[19]				
ENET2_TX_CTL	enet2.RGMII_TX_CTL	uart4.DTR_B	sai2.TX_SYNC		flexio2.FLEXIO[20]	gpio4.IO[20]			gpio4.IO[20]				
ENET2_TXC	enet2.RGMII_TXC	enet2.TX_ER	sai2.TX_BCLK		flexio2.FLEXIO[21]	gpio4.IO[21]			gpio4.IO[21]				
ENET2_RX_CTL	enet2.RGMII_RX_CTL	uart4.DSR_B	sai2.TX_DATA[0]		flexio2.FLEXIO[22]	gpio4.IO[22]			gpio4.IO[22]				
ENET2_RXC	enet2.RGMII_RXC	enet2.RX_ER	sai2.TX_DATA[1]		flexio2.FLEXIO[23]	gpio4.IO[23]			gpio4.IO[23]				
ENET2_RD0	enet2.RGMII_RD0	uart4.RX	sai2.TX_DATA[2]		flexio2.FLEXIO[24]	gpio4.IO[24]			gpio4.IO[24]				
ENET2_RD1	enet2.RGMII_RD1	spdif1.IN	sai2.TX_DATA[3]		flexio2.FLEXIO[25]	gpio4.IO[25]			gpio4.IO[25]				
ENET2_RD2	enet2.RGMII_RD2	uart4.CTS_B	sai2.MCLK	mqs2.RIGHT	flexio2.FLEXIO[26]	gpio4.IO[26]			gpio4.IO[26]				
ENET2_RD3	enet2.RGMII_RD3	spdif1.OUT	spdif1.IN	mqs2.LEFT	flexio2.FLEXIO[27]	gpio4.IO[27]			gpio4.IO[27]				
SD1_CLK	usdhc1.CLK				flexio1.FLEXIO[8]	gpio3.IO[8]			gpio3.IO[8]				
SD1_CMD	usdhc1.CMD				flexio1.FLEXIO[9]	gpio3.IO[9]			gpio3.IO[9]				
SD1_DATA0	usdhc1.DATA0				flexio1.FLEXIO[10]	gpio3.IO[10]			gpio3.IO[10]				
SD1_DATA1	usdhc1.DATA1				flexio1.FLEXIO[11]	gpio3.IO[11]	ccmsrcgpcmix.INT_BOOT		gpio3.IO[11]				
SD1_DATA2	usdhc1.DATA2				flexio1.FLEXIO[12]	gpio3.IO[12]	ccmsrcgpcmix.PMIC_READY		gpio3.IO[12]				
SD1_DATA3	usdhc1.DATA3	flexspi.A_SS1_B			flexio1.FLEXIO[13]	gpio3.IO[13]			gpio3.IO[13]				
SD1_DATA4	usdhc1.DATA4	flexspi.A_DATA[4]			flexio1.FLEXIO[14]	gpio3.IO[14]			gpio3.IO[14]				
SD1_DATA5	usdhc1.DATA5	flexspi.A_DATA[5]	usdhc1.RESET_B		flexio1.FLEXIO[15]	gpio3.IO[15]			gpio3.IO[15]				
SD1_DATA6	usdhc1.DATA6	flexspi.A_DATA[6]	usdhc1.CD_B		flexio1.FLEXIO[16]	gpio3.IO[16]			gpio3.IO[16]				
SD1_DATA7	usdhc1.DATA7	flexspi.A_DATA[7]	usdhc1.WP		flexio1.FLEXIO[17]	gpio3.IO[17]			gpio3.IO[17]				
SD1_STROBE	usdhc1.STROBE	flexspi.A_DQS			flexio1.FLEXIO[18]	gpio3.IO[18]			gpio3.IO[18]				
SD2_VSELECT	usdhc2.VSELECT	usdhc2.WP	lptmr2.ALT3		flexio1.FLEXIO[19]	gpio3.IO[19]	ccmsrcgpcmix.EXT_CLK1		gpio3.IO[19]				
SD3_CLK	usdhc3.CLK	flexspi.A_SCLK			flexio1.FLEXIO[20]	gpio3.IO[20]			gpio3.IO[20]				
SD3_CMD	usdhc3.CMD	flexspi.A_SS0_B			flexio1.FLEXIO[21]	gpio3.IO[21]			gpio3.IO[21]				
SD3_DATA0	usdhc3.DATA0	flexspi.A_DATA[0]			flexio1.FLEXIO[22]	gpio3.IO[22]			gpio3.IO[22]				
SD3_DATA1	usdhc3.DATA1	flexspi.A_DATA[1]			flexio1.FLEXIO[23]	gpio3.IO[23]			gpio3.IO[23]				
SD3_DATA2	usdhc3.DATA2	flexspi.A_DATA[2]			flexio1.FLEXIO[24]	gpio3.IO[24]			gpio3.IO[24]				
SD3_DATA3	usdhc3.DATA3	flexspi.A_DATA[3]			flexio1.FLEXIO[25]	gpio3.IO[25]			gpio3.IO[25]				
SD2_CD_B	usdhc2.CD_B	enet_qos.1588_EVENT0_IN	i3c2.SCL		flexio1.FLEXIO[0]	gpio3.IO[0]	ccmsrcgpcmix.TESTER_ACK		gpio3.IO[0]				
SD2_CLK	usdhc2.CLK	enet_qos.1588_EVENT0_OUT	i3c2.SDA		flexio1.FLEXIO[1]	gpio3.IO[1]	ccmsrcgpcmix.OBSERVE0		gpio3.IO[1]				
SD2_CMD	usdhc2.CMD	enet2.1588_EVENT0_IN	i3c2.PUR	i3c2.PUR_B	flexio1.FLEXIO[2]	gpio3.IO[2]	ccmsrcgpcmix.OBSERVE1		gpio3.IO[2]				
SD2_DATA0	usdhc2.DATA0	enet2.1588_EVENT0_OUT	can2.TX		flexio1.FLEXIO[3]	gpio3.IO[3]	ccmsrcgpcmix.OBSERVE2		gpio3.IO[3]				
SD2_DATA1	usdhc2.DATA1	enet2.1588_EVENT1_IN	can2.RX		flexio1.FLEXIO[4]	gpio3.IO[4]	ccmsrcgpcmix.WAIT		gpio3.IO[4]				
SD2_DATA2	usdhc2.DATA2	enet2.1588_EVENT1_OUT	mqs2.RIGHT		flexio1.FLEXIO[5]	gpio3.IO[5]	ccmsrcgpcmix.STOP		gpio3.IO[5]				
SD2_DATA3	usdhc2.DATA3	lptmr2.ALT1	mqs2.LEFT		flexio1.FLEXIO[6]	gpio3.IO[6]	ccmsrcgpcmix.EARLY_RESET		gpio3.IO[6]				
SD2_RESET_B	usdhc2.RESET_B	lptmr2.ALT2			flexio1.FLEXIO[7]	gpio3.IO[7]	ccmsrcgpcmix.SYSTEM_RESET		gpio3.IO[7]				
I2C1_SCL	i2c1.SCL	i3c1.SCL	uart1.DCB_B	tpm2.CH0		gpio1.IO[0]			gpio1.IO[0]				
I2C1_SDA	i2c1.SDA	i3c1.SDA	uart1.RIN_B	tpm2.CH1		gpio1.IO[1]			gpio1.IO[1]				
I2C2_SCL	i2c2.SCL	i3c1.PUR	uart2.DCB_B	tpm2.CH2	sai1.RX_SYNC	gpio1.IO[2]	i3c1.PUR_B		gpio1.IO[2]				
I2C2_SDA	i2c2.SDA		uart2.RIN_B	tpm2.CH3	sai1.RX_BCLK	gpio1.IO[3]			gpio1.IO[3]				
UART1_RXD	uart1.RX	seco.RX	spi2.SIN	tpm1.CH0		gpio1.IO[4]			gpio1.IO[4]				
UART1_TXD	uart1.TX	seco.TX	spi2.PCS0	tpm1.CH1		gpio1.IO[5]/ccmsrcgpcmix.BOOT_MODE[0]			gpio1.IO[5]/ccmsrcgpcmix.BOOT_MODE[0]				
UART2_RXD	uart2.RX	uart1.CTS_B	spi2.SOUT	tpm1.CH2	sai1.MCLK	gpio1.IO[6]			gpio1.IO[6]				
UART2_TXD	uart2.TX	uart1.RTS_B	spi2.SCK	tpm1.CH3		gpio1.IO[7]/ccmsrcgpcmix.BOOT_MODE[1]			gpio1.IO[7]/ccmsrcgpcmix.BOOT_MODE[1]				
PDM_CLK	pdm.CLK	mqs1.LEFT			lptmr1.ALT1	gpio1.IO[8]	can1.TX		gpio1.IO[8]				
PDM_BIT_STREAM0	pdm.BIT_STREAM[0]	mqs1.RIGHT	spi1.PCS1	tpm1.EXTCLK	lptmr1.ALT2	gpio1.IO[9]	can1.RX		gpio1.IO[9]				
PDM_BIT_STREAM1	pdm.BIT_STREAM[1]	m33.NMI	spi2.PCS1	tpm2.EXTCLK	lptmr1.ALT3	gpio1.IO[10]	ccmsrcgpcmix.EXT_CLK1		gpio1.IO[10]				
SAI1_TXFS	sai1.TX_SYNC	sai1.TX_DATA[1]	spi1.PCS0	uart2.DTR_B	mqs1.LEFT	gpio1.IO[11]/ccmsrcgpcmix.BOOT_MODE[2]			gpio1.IO[11]/ccmsrcgpcmix.BOOT_MODE[2]				
SAI1_TXC	sai1.TX_BCLK	uart2.CTS_B	spi1.SIN	uart1.DSR_B	can1.RX	gpio1.IO[12]			gpio1.IO[12]				
SAI1_TXD0	sai1.TX_DATA[0]	uart2.RTS_B	spi1.SCK	uart1.DTR_B	can1.TX	gpio1.IO[13]/ccmsrcgpcmix.BOOT_MODE[3]			gpio1.IO[13]/ccmsrcgpcmix.BOOT_MODE[3]				
SAI1_RXD0	sai1.RX_DATA[0]	sai1.MCLK	spi1.SOUT	uart2.DSR_B	mqs1.RIGHT	gpio1.IO[14]			gpio1.IO[14]				
WDOG_ANY	wdog1.WDOG_ANY					gpio1.IO[15]			gpio1.IO[15]				
CLKIN1	anamix.CLKIN1	anamix.esd_diode											
CLKIN2	anamix.CLKIN2	anamix.atx											
XTALI_24M	anamix.xtali_24M												
XTALO_24M	anamix.xtalo_24M												
ADC_IN0	anamix.adc_in0												
ADC_IN1	anamix.adc_in1												
ADC_IN2	anamix.adc_in2												
ADC_IN3	anamix.adc_in3												

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