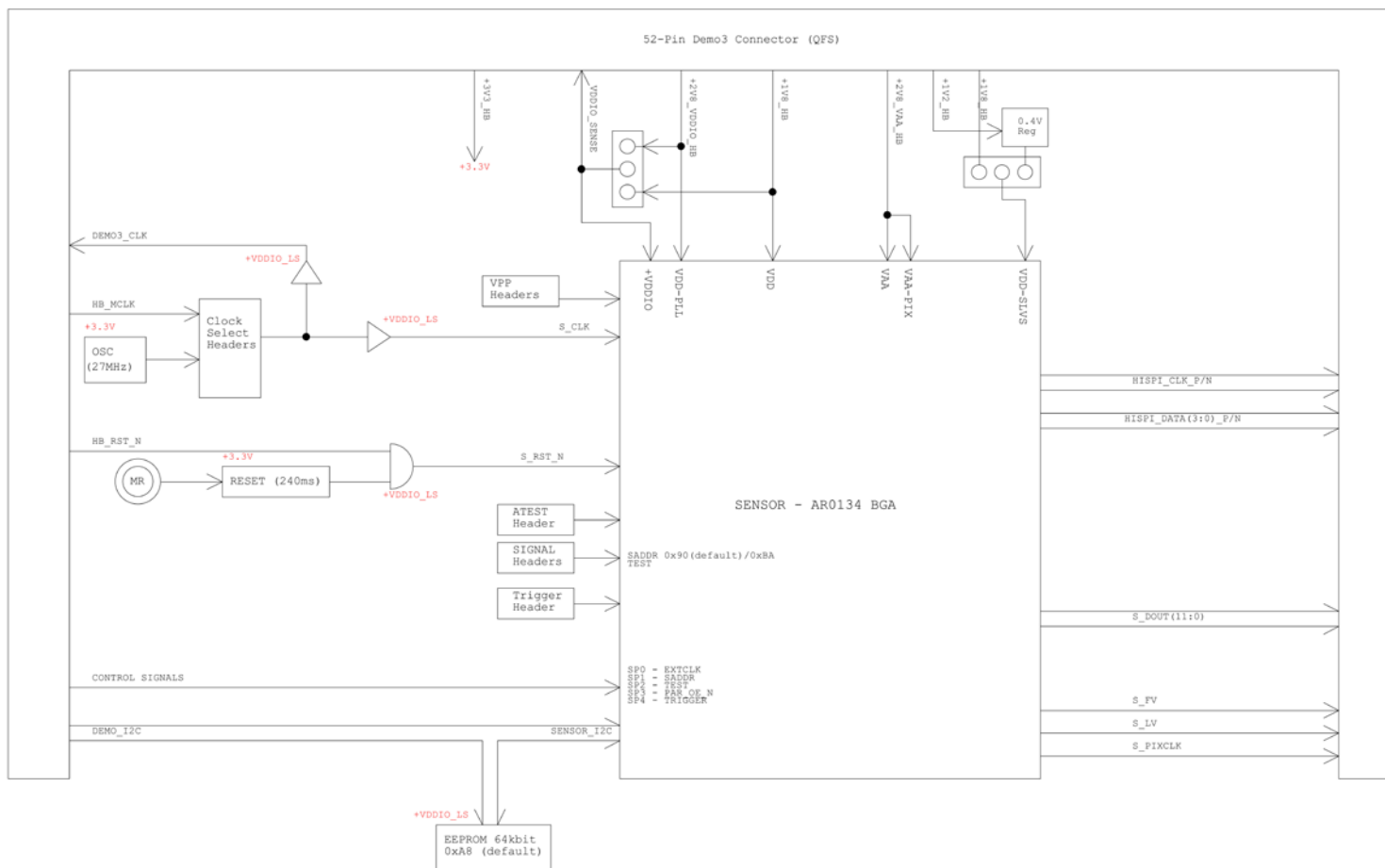


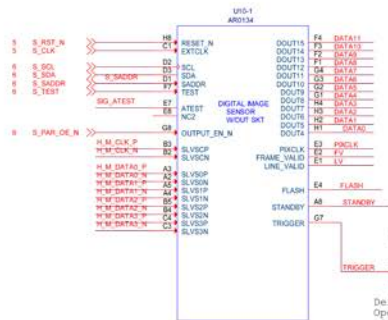
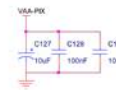
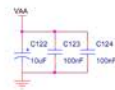
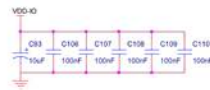
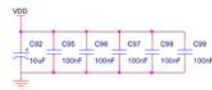
Block Diagram



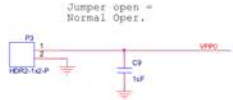
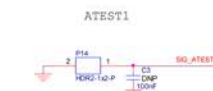
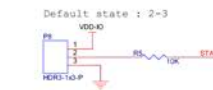
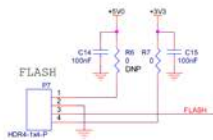
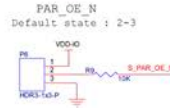
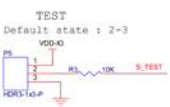
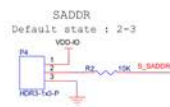


Sensor

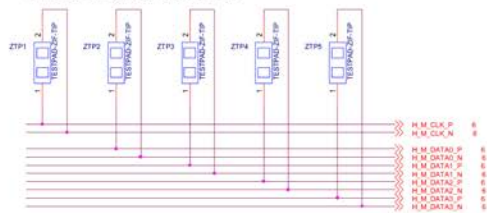
HVS	4	HVS	4
LV	4.5	LV	4.5
VDDIO_LB	4.5.6	VDDIO_LB	4.5.6
VDD	4	VDD	4
VDDIO	4	VDDIO	4
VDDIO_LV	4	VDDIO_LV	4
VDDIO_PLL	4	VDDIO_PLL	4
VAA	4	VAA	4
VAA-PK	4	VAA-PK	4



Default state : 1-2 shorted
Open: Connect generator between pins 1 and ground



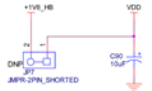
(Note for layout: - Place these testpads near the Demo3 I/F connector at the top side of PCB)



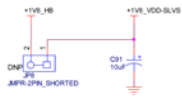


Debug Headers: Cut away the shorted trace and mount header for power debugging

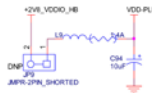
VDD 1.8V SUPPLY



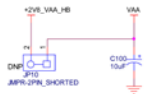
VDD-SLVS 1.8V SUPPLY



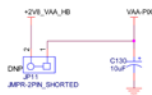
VDD-PLL 2.8V SUPPLY



VAA 2.8V SUPPLY

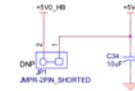


VAA-PIX 2.8V SUPPLY



Power

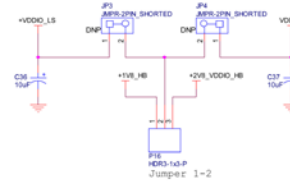
PERIPHERAL 5V SUPPLY



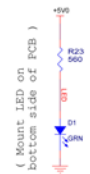
PERIPHERAL 3.3V SUPPLY



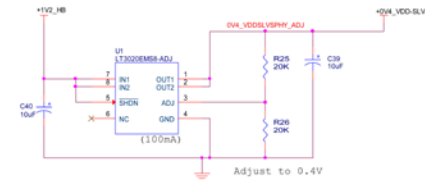
VDDIO & VDDIO LS 1.8V/2.8V SUPPLY



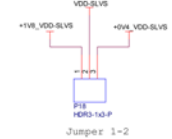
5V LED



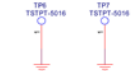
VDDSLVSPHY 0.4V SUPPLY



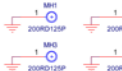
Selection of 0.4V or 1.2V/1V8 for VDDSLVSPHY supply



Ground Testpoints



Mounting Holes

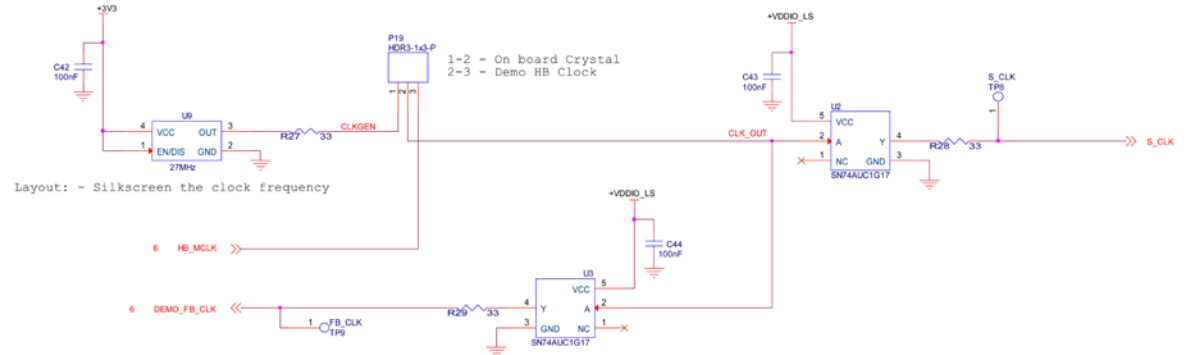




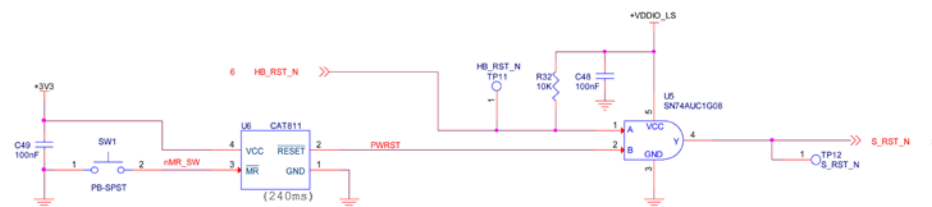
Clock and Reset

+5V0 3.4
+3V0 3.4
+VDDIO_LS 4.8

CLOCK CIRCUIT



RESET CIRCUIT



+5V0_HB		+5V0_HB	4
+3V3_HB		+3V3_HB	4
+2V5_VAA_HB		+2V5_VAA_HB	4
+2V5_VDDIO_HB		+2V5_VDDIO_HB	4
+1V8_HB		+1V8_HB	4
+1V2_HB		+1V2_HB	4
+3V3		+3V3	3.4.5
+VDDIO_LS		+VDDIO_LS	4.5

The schematic shows two identical signal conditioning stages for the HDMR-20-P module. Each stage includes a 100nF capacitor (C63 or C64) connected to a +VDDIO_1.8 supply. This is followed by a resistor network consisting of a 1.5k resistor (R36 or R37) and a 1.5k resistor (R38 or R39), both labeled as DNP (Do Not Populate). A pull-up resistor P24 is also present. The input signals, DEMO_SDA and DEMO_SCL, are connected to pins 2 and 6 respectively. The output signals, S_SDA and S_SCL, are connected to pins 1 and 5 respectively. A jumper is indicated between pins 1-2 and 3-4, with a note stating "(default status)".

EPROM Address Switch Settings:

A2 = HIGH, A1 = LOW, A0 = LOW: Address => 0xA8 (default)
 A2 = HIGH, A1 = HIGH, A0 = LOW: Address => 0xAC
 A2 = LOW, A1 = HIGH, A0 = LOW: Address => 0xA4
 A2 = LOW, A1 = LOW, A0 = LOW: Address => 0xA0

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