

PHD STUDENT IN MODEL DRIVEN SOFTWARE ENGINEERING

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Education

PhD at LISE (Laboratory of Model-Driven Engineering for Embedded Systems)

Saclay, France

THESIS TITLE: METHOTHODOLOGIES FOR MODEL-CODE SYNCHRONIZATION FOR REACTIVE SYSTEM DEVELOPMENT

Nov. 2014 - Present

- Working place: Laboratory of Model-Driven Engineering for Embedded Systems (LISE), CEA-List, Saclay, France.
- Brief Synopsis of Research: The use of MDE in industry is increasing. However, on one hand, its adoption is still low in comparison to the use of programming languages in software engineering. On the other hand, fully operational code is hardly generated from graphical modeling languages, using current MDE approaches. This thesis proposes an approach for synchronizing code and model specified by using component-based modeling and UML state machines for reactive system development. The objective is three-fold: (1) improve flexibility in MDE by allowing modifications in model and code; (2) harmonize MDE with traditional programming practices; and (3) foster collaboration between MDE adopters and traditional software developers.
- Research interests: My current research centers around Model-Driven Engineering and its applications, model transformation and synchronization, and software language engineering

U-PSUD(University of Paris-Sud)

Orsay, France

MASTER IN EMBEDDED SYSTEMS AND SIGNAL PROCESSING

Sept. 2013 - Sept. 2014

- Program: Embedded Systems and Signal Processing (SETI) cooperated by University of Paris Sud, ENS Cachan, INSTN and ENSTA ParisTech, Franc
- Scholarship Student of International Relationships of University of Paris-Sud
- Modules included: Real-time Control Numeric Systems, Complex Embedded System Design, Algorithm-Architecture Ad-equation, Network and Quality of Services, Multimedia Data Compression, Data Fusion, Statistic Learning and Neural Network, and Initiation to Research.

HUST(Hanoi University of Science and Technology)

Hanoi, Vietnam

ENGINEER IN INFORMATION SYSTEM AND COMMUNICATION

Sept. 2007 - Jul. 2012

- Program: Programme de Formation d'Ingenieur d'Excellence au Vietnam (PFIEV)
- Final project: Understanding pros and cons of the client-server and peer-to-peer models, and combining these two models for developing distributed applications.

Employment.

Laboratory of Model-Driven Engineering for Embedded Systems (LISE), CEA-LIST

CEA, Saclay, France

PHD STUDENT AT LABORATORY OF MODEL-DRIVEN ENGINEERING FOR EMBEDDED SYSTEMS (LISE)

Nov. 2014 - Present

• Iwork as a PhD Student, under supervision of Dr. Ansgar RADERMACHER, Dr. Sébastien GÉRARD, and Dr. Shuai LI, at the LISE laboratory in the field of MDE, especially the use the UML modeling language and the synchronization between model-model and between model-generated code. My work involves the use of different languages for model transformation and code generation such as QVT, Xtend; the use of UML for modeling component-based architecture and event-driven behaviors for reactive systems in the context of the Papyrus modeling tool - an extension of the Eclipse Modeling Framework (EMF); and different techniques for synchronization of model and code.

Laboratory of Model-Driven Engineering for Embedded Systems (LISE), CEA-LIST

CEA, Saclay, France

Internship at Laboratory of Model-Driven Engineering for Embedded Systems (LISE)

Apr. 2014 - Sept. 2014

• I worked as an intern undersupervison of Dr. Ansgar RADERMACHER in the context of applying MDE and the FCM component-based model to distributed system development, especially the modeling of ZeroMQ middleware-based interaction components between distributed components.

Toshiba Software Development Vietnam (TSDV)

Hanoi, Vietnam

SOFTWARE ENGINEER FOR COMPUTERS AND EMBEDDED SYSTEM

Jul. 2012 - Aug. 2013

• I worked as a software developer in two projects: (1) deal with requirement analysis, detailed design, implementation, unit test, integration test, and optimization at the programming level for software of an embedded system: Toshiba G2R protection relay. The development using C as the development language includes using IEC 60870-5-103 to control and communicate between smart electric device, and testing on real hardware and using debug tools to debug on hardware; (2) develop a desktop application to control electric devices by using a private protocol of Toshiba and the C# language. The application polls the devices to receive data of recorded errors, and creates a chart for analysis of errors causes.

MAY 17, 2017 VAN CAM. PHAM · RÉSUMÉ

Skills and Experiences.

Programming JAVA, C/C++, C#, Androind, JavaScript, ASM, Matlab, Python

UML (class, state machine, composite structure, deployment, ALF, profile, PSCS, PSSM),

MARTE, Papyrus, Model-Driven Engineering (model transformation (QVT, ATL), code **Modeling**

generation (Xtend, Acceleo)), Component-based software modeling, event-driven behavior modeling for reactive systems, round-trip engineering for model-model and model-code

LaTeX, Papyrus, Visual Studio, NetBeans, Eclipse, CodeBlocks, QT, TomCat, Android Studio,

Framework and Tools Oracle

Other skills

Operating Systems Ubuntu, Windows 7, 10, XP

> Supervise practicals for undergraduate students in Android Programming, SQL for database **Teaching**

query, C++ and JAVA Programming

Languages English, French, Vietnamese

TCP/IP, application layer protocols, routing protocols, wireless network **Network experiences**

Neural network for statistic learning, VHDL for simulation, real-time tasks scheduling,

multimedia compression

Reserch Interests

Model-Driven Software Engineering

The main research interest of my PhD thesis is methodologies for synchronization of code and model specified in UML-based component-based modeling and UML state machines, and studying different techniques for model transformation such as QVT, ATL, Triple-Graph Grammar (TGG), and Change-driven transformation, for model synchronization such as QVT-Relation, TGG. I'm also involved in researching approaches for mapping between UML model containing the ALF code, and programming language code. This mapping will enable a synchronization of UML model with ALF and programming code, and eventually provide synchronization of a platform-independent model with code. Furthermore, I'm also interested in approaches for generating fully operational code from models, especially UML models, which might contain ALF code, approaches for optimizing software system at the model level (e.g. optimization ALF code or UML state machines), and if possibly approaches for model interpretation and compilation. The final goal is of course harmonization of software programming and MDE practices.

Application to Modeling and Development of Distributed Systems

In my thesis, I work in the context of the Papyrus Designer - an extension of the Papyrus modeling tool. Papyrus Designer provides component-based modeling and code generation for distributed embedded systems, using the concepts of interaction components to model remote interactions between distributed components. I'm interested in studying methodologies for applying Papyrus Designer with its UML profile to distributed systems, especially component-based distributed reactive systems.

State Machine-Based Language Engineering and Transformation

A major part of my thesis work is about extending, engineering, and transforming software programming language. Especially, I'm interested in extending current programming languages to support a state machine-based event-driven model for developing reactive systems.

References_

Dr. Ansgar RADERMACHER Ansgar.RADERMACHER@cea.fr Laboratory: LISE CEA-LIST, CEA, Saclay, France

Dr. Shuai Ll Shuai.Ll@cea.fr Laboratory: LISE CEA-LIST, CEA, Saclay, France

Dr. Sebastien GERARD Sebastien.GERARD@cea.fr Laboratory: LISE CEA-LIST, CEA, Saclay, France



Conference Proceedings and Journal Articles

- V. C. Pham, Ö. Gürcan, and A. Radermacher. Interaction Components Between Components based on a Middleware. In 1st International Workshop on Model-Driven Engineering for Component-based Software Systems (ModComp'14), 2014.
- V. C. Pham, S. Li, A. Radermacher, S. Gerard, and C. Mraidha. Fostering Software Architect and Programmer Collaboration. In 21st International Conference on Engineering of Complex Computer Systems, ICECCS 2016, Dubai, United Arab Emirates, November 6-8, 2016, pages 3–12, 2016a. doi: 10.1109/ICECCS.2016.011. URL http://dx.doi.org/10.1109/ICECCS.2016.011.
- V. C. Pham, A. Radermacher, and S. Gérard. From UML State Machine to Code and Back Again! In *Position Papers of the 2016 Federated Conference on Computer Science and Information Systems, FedCSIS 2016, Gdańsk, Poland, September 11-14, 2016.*, pages 283–290, 2016b. doi: 10.15439/2016F485. URL http://dx.doi.org/10.15439/2016F485.
- V. C. Pham, A. Radermacher, S. Gérard, and F. Noyrit. Change Rule Execution Scheduling in Incremental Roundtrip Engineering Chain: From Model-to-Code and Back. In MODELSWARD 2016 Proceedings of the 4rd International Conference on Model-Driven Engineering and Software Development, Rome, Italy, 19-21 February, 2016., pages 225–232, 2016c. doi: 10.5220/0005687702250232. URL http://dx.doi.org/10.5220/0005687702250232.
- V. C. Pham, A. Radermacher, S. Gérard, and S. Li. Bidirectional Mapping Between Architecture and Code for Synchronization. In *ICSA 2017 Proceedings of the 14th International Conference on Software Architecture, Gothenburg, Sweeden, 3-7 April, 2017.*, 2017a.
- V. C. Pham, A. Radermacher, S. Gérard, and S. Li. Complete Code Generation from UML State Machine. In MODELSWARD 2017 Proceedings of the 5th International Conference on Model-Driven Engineering and Software Development, Porto, Portugal, 19-21 February, 2017., 2017b.
- V. C. Pham, A. Radermacher, S. Gérard, and S. Li. UML State Machine and Composite Structure-Based Modeling and Code Generation for Reactive Systems. *Springer Communications in Computer and Information Science*, 2017c. to be appeared.

Presentation and Courses Attended

14th ICSA (International Conference on Software Architecture)

Gothenburg, Sweeden

PRESENTER FOR CONFERENCE PAPER: BIDIRECTIONAL MAPPING BETWEEN ARCHITECTURE AND CODE FOR

Synchronization

Apr. 2017

Presented an approach, which enables a bidirectional mapping between UML-based architecture model and code. This proposed
mapping is part of a synchronization approach, which synchronizes code and UML-based model, using UML component-based modeling and UML state machines.

5th MODELSWARD (International Conference on Model-Driven Engineering and Software Development)

Porto, Portugal

PRESENTER FOR CONFERENCE PAPER: COMPLETE CODE GENERATION FROM UML STATE MACHINES

Feb. 2017

• Presented an approach, which enables generating efficient code from UML state machines with full UML state machine features, including pseudo states and UML events. The generated code is evaluated for its runtime execution semantics conforming to the UML specification, its performance in event processing speed, and its static and dynamic memory consumption.

21th ICECCS (International Conference on Engineering of Complex Computer Systems)

Dubai, UAE

PRESENTER FOR CONFERENCE PAPER: FOSTER SOFTWARE ARCHITECT AND PROGRAMMER COLLABORATION

Nov. 2016

• Presented a model-code synchronization methodological pattern, which allows model and code to be concurrently modified by software architects and programmers, respectively, and synchronizes the modifications made in the model and the code.

36th SEW (International Software Engineering Workshop)

Gothenburg, Sweed

PRESENTER FOR CONFERENCE PAPER: FROM UML STATE MACHINE TO CODE AND BACK

Sept. 2016

• Presented a mapping between UML state machine elements and object-oriented code. The purpose is to provide a round-trip engineering between UML state machine and code, which means that modifications in code can be reflected back to model.

6th Summer School on Domain Specific Modelling Theory and Practice (DSM-TP)

Antwerp, Belgium

ATTENDEE AT SUMMER SCHOOL

Aug. 2015

 Attended as a doctoral student. I learned different concepts and practices of MDE in this summer school such as model transformation, domain-specific modeling language design, mapping abstract and concrete syntax as well as the theory of temporal logic.