# Mid-term report: Code generation and model-code synchronization

Van Cam Pham, Ansgar Radermacher, Sebastien Gerard
CEA-List, Laboratory of Model-Driven Engineering for Embedded Systems (LISE)
Gif-sur-Yvette, France
Email: first-name.lastname@cea.fr

## I. INTRODUCTION

Internet of Things [1] raises the complexity of embedded systems today rapidly. Model-Driven Engineering (MDE) is recognized as an efficient means to deal with the complexity. MDE [2] promotes abstraction and automation. The latter often relies on chaining transformations from source models at high level abstraction to target models and finally to code. Those two techniques are identified as model to model (M2M) and model to code (M2C) transformations. Among modeling languages, the Unified Modeling Language (UML) is most widely used. UML and its diagrams are much more useful to design such systems than text-based languages. Especially, in embedded system domains such as vehicle controlling, UML State Machines [3] are used as a powerful means to describe the dynamic behavior of such complex systems.

Ideally, a full model-centric approach is preferred by the MDE community due to its advantages [2]. However, in industrial practice, there is significant reticence [4] to adopt it. The reticence is due in part to the perceived gap [5] between diagram-based languages and textual languages. On one hand, programmers prefer to use the more familiar textual programming language. On the other hand, software architects, working at higher levels of abstraction, tend to favor the use of models, and therefore prefer graphical languages for describing the architecture of the system (see Fig. 1).

The survey described in [6] polled stakeholders in companies who use MDE approaches. The survey reveals that UML is the prominent and dominating language. 85% of the respondents used UML for various purposes, especially problem understanding and automation such as code generation (88,2%). It notes that 70% of the respondents primarily work with models, but still require manually-written code to be integrated. Furthermore, 35% of the respondents answered that they spend a lot of time and effort synchronizing model and code. The need of synchronization is critically required by systems today. Besides the synchronization aspect, efficiency of code generated from models is a concern for the respondents.

Yet, still in another survey [7], the authors compare code-centric and model-centric approaches by asking the participants, who mostly come from Canada, United States and other countries such as United Kingdom, France, Indian, Australia and Singapore, questions related to different activities in software development such as fixing a bug, creating efficient software and a system as quickly as possible. The results shows that most activities tend to be easier in a model-centric approach but many participants believe that a code-centric approach is much easier a model-centric approach. This confirms the importance of automatically keeping model and code synchronized.

The code modified by programmers and the model are then inconsistent. Round-trip engineering (RTE) [8] achieves synchronization between related artifacts that may evolve concurrently by incrementally updating each artifact to reflect editions made in the other artifacts. RTE enables actors (software architect and programmers) to freely move between different representations [9] and stay efficient with their favorite working environment.

Even, if the code is not intended to be modified by programmers, RTE is still helpful in the state-of-the-art MDE practice, e.g. debugging generated code. Some code generators generate fully operational code. The debugging support helps developers trace bugs in the generated code back to precise model elements.

The back-and-forth switching between diagram-based and textual languages, as well as between model and code, has hindered the adoption of MDE in industrial practice. To solve this issue, we believe that the sharp distinction between model and code must be blurred. We feel that a collaborative solution must be offered to different categories of developers (e.g. architects, programmers), who use different development practices.

Collaboration between developers producing different types of artifacts, in different languages, using different tools, raises the issue of artifact synchronization. This is a well-known concern with round-trip engineering [10]. It is related to traditional software engineering disciplines such as forward and reverse engineering [11].

Usually, a direct synchronizing between the architecture model and the code is hard because of the large abstraction gap. The synchronization is therefore decoupled into several synchronization steps of artifacts participating in one of the transformation phases of the chain. Hence, the whole synchronization is achieved if these steps do.

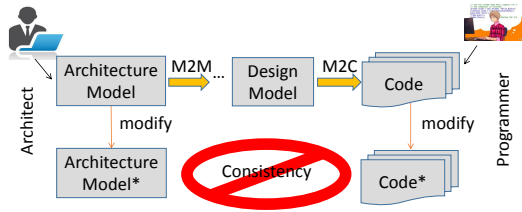To sum up, the thesis can be divided into two related major

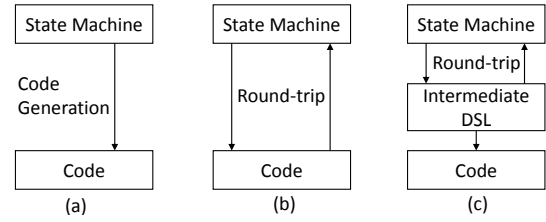Fig. 1.   Concurrent modifications made to different artifacts



Fig. 2.   Different usages of UML State Machine code generators and RTE: (a) state machines are generated to code and modifications only made to the state machines; (b) code generated from state machines is modified and synchronized directly with the state machines; and (c) generated code is modified indirectly via a text-based domain specific language (DSL).

parts as followings:

### A. Major topics

- **Artifact synchronization**: As previously discussed, this is critical for step-by-step integrating MDE into current software development practices and collaborating these with MDE methodologies. Particularly, synchronization of artifacts is realized by means of incremental model-to-model and model-to-text transformations. Architecture models are often at a higher level abstraction than low level implementation code. Mappings from the architecture are usually not one-to-one. This raises the difficulty in mapping code-side elements back to architecture model-side elements. The existing synchronizations (state of the art) mainly focus on static parts while the dynamics are missing.

- **Improving code generation solutions and towards synchronization for UML State Machine**: UML State Machines are widely used for reactive, real-time and embedded systems. However, on the one hand, the OMG seeks to raise the usefulness of UML State Machine by providing more modeling concepts supporting software architects for modeling and designing complex systems. On the other hand, the support of existing generation approaches, over the years of research and development, is still limited to simple cases, especially when considering concurrency of *doActivity* and orthogonal regions, pseudo states such as history, and different events, e.g. Rhapsody does not support *doActivity*, junction or truly concurrent execution orthogonal regions[1] or Sinelabore [12] restricts choice and junction, and does not support fork, join, terminate, junction and concurrent states. Tools such as Enterprise Architect [13], Rhapsody [14] only support CallEvent and TimeEvent while SignalEvent and ChangeEvent (see **??** for formal definitions) are missing. This again enlarges the gap between the UML State Machine semantics and the actual generated code. Furthermore, the synchronization between UML State Machine and generated code is not supported by any other approaches, even though it is critical.

In reality, UML State Machine might be used for different use-cases, either with RTE or not. We consider the second topic in different use-cases. Fig. 2 shows three cases. There are trade-offs between these. In the use-case (a), code generators can generate efficient code from state machines with full features (this is detailed in this report). The case (b) (see V-B) only supports a small sub-set of modeling features and trades a reversible mapping with a memory overhead. The case (c) is a harmonization of the other two but restricts developers to a domain specific language (DSL).

### B. Objective

The transformation from architecture models to code directly involves chaining model-to-model and model-to-text transformations. Therefore, to synchronize the architecture models and code, the following objectives need to be met:

- A generic methodology, which synchronizes two different system artifacts (model and code). This method is based on incremental model transformation and synchronization. It will be used in different specific synchronization cases developed in the thesis deployment.

- A specific synchronization between UML State Machine with full features and code. Therefore, one task is needed to seamlessly make the behavior of the code generated from UML State Machine complied with the semantics specified by the Precise Semantics of UML State Machine (PSSM) [15]. To do it, the objective of this part is to provide a complete generation solution, especially considering the concurrency support for real-time systems. From the generation solution, a specific synchronization methodology combined with the generic one as above is also desired.

### C. Contributions

The contributions of this report are the followings:

- An extensible generic methodology, which synchronize two different system artifacts (model and code).
- A complete generation solution from UML State Machine to code with respect to the Precise Semantics State Machine (PSSM).
- A specific methodology derived from the generic one supporting the synchronization of UML State Machine and code.

---

[1]IBM Rhapsody and UML differences, http://www-01.ibm.com/support/docview.wss?uid=swg27040251

- A method for synchronization based on incremental model transformations, which prevent one artifact from begin overwritten when propagating changes from the other artifact.

### D. Structure of the report

The remaining of this report is structured as followings: Section II presents a generic pattern for artifact synchronization in case of concurrent modifications made to model and code. Section **??** describes a complete code generation solution from UML State Machine with respect to concurrency semantics. Section IV presents some ongoing works including a specific synchronization of UML State Machine and code, which is derived from the generic pattern and the approach as in Fig. 2 (c), and a verification of semantic-conformance of generated code runtime execution. Section V sketches other works which are not detailed in this report.

## II. A GENERIC MODEL-CODE SYNCHRONIZATION PATTERN

This section describes our generic artifact synchronization methodology pattern. For the sake of generality, we postulate that the architect and programmer are actors with starkly opposite development practices. This allows the approach to be used even in cases where model and code can both be used for the full implementation of a system, rather than just architectural design for the former, and code implementation for the latter.

### A. Definitions

In this section we define the actors who will use our model-code synchronization approach to collaborate during development. Some basic concepts related to the actors and use-cases are also defined in this section.

First, we introduce the concepts of *development artifact* and *baseline artifact*.

**Definition II.1** (Development artifact)**.** A development artifact is an artifact, as defined in [16], that can be used for the full implementation of the system.

In our work, we assume that model and code are both development artifacts. A development artifact may be the baseline artifact, defined in this paper as follows:

**Definition II.2** (Baseline artifact)**.** A baseline artifact is one which may be edited manually. All other artifacts are produced from the baseline artifact through some process, and only through a process. Manual edition of artifacts other than the baseline artifact is forbidden.

Two primary actors, called *model-driven developer* and *code-driven developer*, are introduced.

**Definition II.3** (Model-driven developer)**.** A model-driven developer is an actor in a software development process for whom the baseline artifact is the model.

The code must always be produced from the model automatically by some process that guarantees that the code is consistent with the model. A software architect is a kind of the model-driven developer who edits the model to specify the architecture of the system.

**Definition II.4** (Code-driven developer)**.** Code-driven developer is an actor in a software development process for whom the code is the baseline artifact.

A programmer is a specialization of the code-driven developer. Indeed, programmers may modify the code, such as editing method bodies.

There are some use-cases for manual edition of artifacts. The `Edit Artifact` use-case implies that the IDE must have some tool to let the developer manually edit an artifact. The `Edit Model` and `Edit Code` use-cases are specializations of the `Edit Artifact` use-case where the artifact is the model or code.

There are also some use-cases related to the synchronization of artifacts. The `Synchronize Artifact` use-case (1) compares two artifacts, (2) updates each with editions made in the related artifact, and (3) reconciles conflicts when appropriate. The `Synchronize Model` and `Synchronize Code` use-cases are specializations where, respectively, the model or the code are the artifacts being synchronized.

The `Generate Code` use-case is related to forward engineering. It is the production of code in a programming language from a model. The developer can either use `Generate Code (Batch)` or `Generate Code (Incremental)`.

**Definition II.5** (Batch code generation [17])**.** Batch code generation is a process of generating code from a model, from scratch. Any existing code is overwritten by the newly generated code.

Incremental code generation is a specialization of incremental model transformation, which is defined in [17] as model transformation that does not generate the whole target model from scratch but only updates the target model by propagating editions made in the source model.

Incremental code generation is defined in this paper as follows:

**Definition II.6** (Incremental code generation)**.** In-cremental code generation is the process of taking as input an edited model, and existing code, and then updating the code by propagating editions in the model to the code.

Finally, the `Reverse Code` use-case is related to reverse engineering. `Reverse Code` is the production of a model, in a modeling language, from code, written in a programming language. The developer can either use `Reverse Code (Batch)` or `Reverse Code (Incremental)`, which are defined in this paper as follows:

**Definition II.7** (Batch reverse engineering)**.** Batch reverse

engineering is a process of producing a model from code, from scratch. The existing model is overwritten by the newly produced model.

**Definition II.8** (Incremental reverse engineering). Incremental reverse engineering is the process of taking as input a edited code, and an existing model, and then updating the model by propagating editions in the code to the model.

In the next section, the use-cases of the IDE are integrated into a process that covers model-code synchronization.

### B. Processes to synchronizing model and code

We propose two synchronization strategies for this scenario. The general approach behind our strategies is to represent one artifact in the language of its corresponding other artifact. These two can then be compared. For this, we define a concept of a *synchronization artifact*:

**Definition II.9** (Synchronization artifact). An artifact used to synchronize a model and its corresponding code is called a synchronization artifact. It is an image of one of the artifacts, either the model or the code. In this context, an image $I$ of an artifact $A$ is a copy of $A$ obtained by transforming $A$ to $I$. $A$ and $I$ are semantically equivalent but are specified in different languages.

For example, a synchronization artifact can be code that was generated from the edited model in batch mode. In that case, it is code that represents an image of the edited model (being image requires that the model is able to be reconstructed from the code).

Using the concept of synchronization artifact, two strategies are proposed in this paper: one in which the synchronization artifact is code, and the other in which the synchronization artifact is a model. The developer can choose to either use these two use-cases of the IDE. The choice may be determined by preferred development practices or the availability of suitable tools (e.g. the programmer may prefer to synchronize two artifacts, both represented in the same programming language, because he prefers to work exclusively with code).

Figure 3 shows the first synchronization strategy based on using code as the synchronization artifact. The general steps of the process shown in Figure 3 are described as follows:

Step 1 Both the model and code may be edited concurrently. (To simplify Figure 3, we don't show the Read and Write interactions for this step.) After both artifacts have been edited concurrently, we need to synchronize them.

Step 2 First we create a synchronization artifact from the edited model by generating code in batch mode. This synchronization artifact is code and it is an image of the edited model.

Step 3 The synchronization artifact is synchronized with the edited code. Since the synchronization artifact is
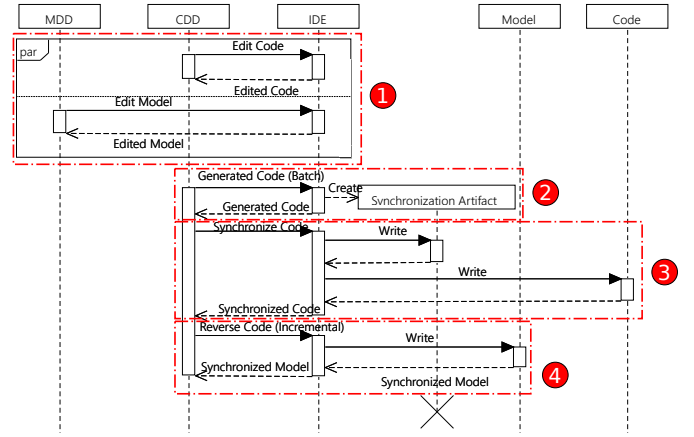


Fig. 3. Synchronization process, in which the model and the code are concurrently edited with code as the synchronization artifact (CDD = Code-Driven Developer, MDD = Model-Driven Developer). The API calls for Model and Code are represented generically as "Read" and "Write".

code itself, this step is done with the `Synchronize Code` use-case of the IDE.

Step 4 Once synchronization artifact and edited code are synchronized, the former is reversed incrementally to update the edited model.

The second strategy, based on using model as the synchronization artifact, is the opposite of the first strategy. In the second strategy, the synchronization artifact is obtained by reversing the edited code in batch mode. Afterwards the synchronization artifact is synchronized with the edited model. Finally, we generate code incrementally from the synchronization artifact to update the edited code.

We propose two strategies based on the preferences of the developers. They may even use both strategies, successively, as a kind of hybrid strategy. This may be useful when developers want to synchronize parts of the system using one strategy, and other parts using the other strategy.

### III. APPROACH

This section presents our RTE approach. At first, it sketches USM concepts supported by this study. The outline and the detail of the approach are presented afterward.

### A. Scope

A USM describes the behavior of an active UML class which is called context class. A USM has a number of states and well-defined conditional transitions. A state is either an atomic state or a composite state that is composed of sub-states and has at most one active sub-state at a certain time. Transitions between states can be triggered by external or internal events. An action (effect) can also be activated by the trigger while transitioning from one state to another state. A state can have associated actions such as *entry/exit/doActivity* executed when the state is entered/exited or while it is active, respectively.
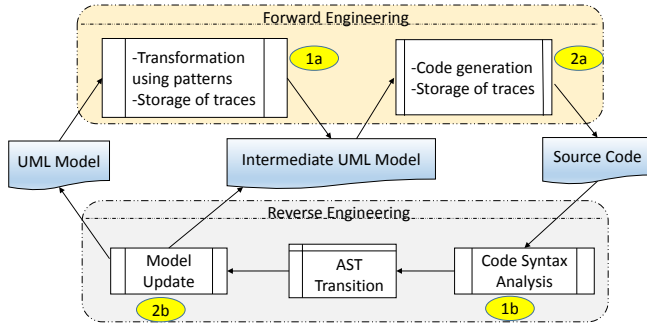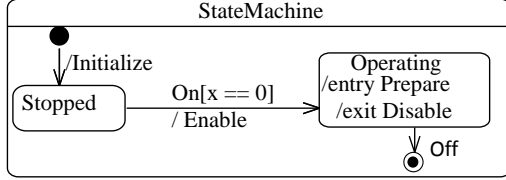
Fig. 4.   Outline of state machine and code RTE



Fig. 5.   An example of USM for tracing table

### B. Approach outline

Our RTE approach is based on the double-dispatch pattern presented in [18] for mapping from USM to a set of classes with embedded code fragments. Fig. 4 shows the outline of our RTE approach consisting of a forward and a backward/reverse (engineering) process. In the forward process, a USM is transformed into UML classes in an intermediate model. The use of the intermediate model facilitates the transformation from the USM to code. Each class of the intermediate model contains attributes, operations and method bodies (block of text) associated with each implemented operation. The transformation utilizes several patterns which will be presented later.

When the source code is modified, a syntactic analysis process belonging to the backward transformation checks whether the modified code conforms to the USM semantics (see Subsection III-D3 for the detail of the analysis). This transformation takes as input the created intermediate model and the USM to update these models sequentially. While the forward process can generate code from hierarchical and concurrent USMs, the backward one only works for hierarchical machines excluding pseudo-states which are *history*, *join*, *fork*, *choice* and *junction*. These features are in future work.

### C. From UML state machine to UML classes

This section describes the forward process which utilizes transformation patterns for states, transitions, and events to an intermediate model and code. We start by a simple USM example in Fig. 5. It consists of two states (*Stopped* and *Operating*), two external events (*On* and *Off*), transitions, and an initial and a final pseudo state. Listing 1 shows a code portion generated from the USM following our approach.

Listing 1.   A segment of C++ generated code

```cpp
class CompositeState: public State {
protected:
  State* activeSubState;
public:
  bool dispatchEvent(Event* event) {
    bool ret = false;
    if (activeSubState != NULL) {
      ret = activeSubState->dispatchEvent(event);}
    return ret || event->processFrom(this);}}
StateMachine::StateMachine(Client* ctx){
  this->context = ctx;
  stopped = new Stopped(this, ctx);
  operating = new Operating(this, ctx);
  this->setIniDefaultState();
  this->activeSubState->entry();}
void StateMachine::setIniDefaultState(){
  this->context->Initialize();
  this->activeSubState = stopped;}
bool StateMachine::transition(Stopped* state,
    On* event) {
  if(this->context->guard(event)){
    this->activeSubState->exit();
    this->context->Enable(event);
    this->activeSubState = this->operating;
    this->activeSubState->entry();
    return true;}
  return false;}
bool StateMachine::transition(
    Operating* state, Off* event) {
  this->activeSubState->exit();
  //no action defined
  this->activeSubState = NULL;
  return true;}
class Stopped: public State {
private:
  StateMachine* ancestor;
public:
  virtual bool processEvent(On* event) {
    return ancestor->transition(this, event);}
}
class On: class Event {
public:
  processFrom(State* state) {
    state->processEvent(this);}
}
class Operating: public State {
private:
  StateMachine* ancestor;
public:
  void onEntryAction() {
    context->Prepare();}
  void onExitAction() {
    context->Disable();}
}
```

*1) Transformation of states:* Each state of the USM is transformed into a UML class. A state class inherits from a base class, namely, *State* (the detail of this class is not shown due to space limitation). *State* defines a reference to the context class, a process event operation for each event, state actions (*entry/exit/doActivity*). A bidirectional relationship is established between a state class and the state class associated with the containing state. For example, the USM example, considered as a composite state, has attributes typed by classes associated with its contained states, *Stopped* and *Operating* in Listing 1, lines 12-13. Inversely, attributes named *ancestor* (line 36) and typed by *StateMachine* in the classes *Stopped* and *Operating* are used to associate with the parent state.

A composite state class, which inherits from a base composite class (line 1), has an attribute *activeSubState* (line 3) indicating the active sub-state of the composite state and a *dispatchEvent* operation (line 5), which dispatches incoming events to the appropriate active state.

The *dispatchEvent* method implemented in the base composite state class delegates the incoming event processing to its active sub-state (line 8). If the event is not accepted by the active sub-state, the composite state processes it (line 9).

*2) Transformation of events:* Each event is transformed into a UML class (see lines 41-45 in Listing 1). An event can be either a *CallEvent*, *SignalEvent* or *TimeEvent* (see the UML specification for definitions of these events). An event class associated with a *CallEvent* inherits from a base event class and contains the parameters in form of attributes typed by the same types as those of the associated operation. The operation must be a member of the context class (a component as described above). For example, a call event *CallEventSend* associated with an operation named *Send*, which has two input parameters typed by *Integer*, is transformed into a class *CallEventSend* having two attributes typed by *Integer*. When a component receives an event, the event object is stored in an event queue.

A signal event enters the component through a port typed by the signal. The implementation view of this scenario depends on the mapping of component-based to object-oriented concepts. In the following, we choose the mapping done in Papyrus Designer [**?**]. In this mapping, the signal is transferred to the context class by an operation provided by the class at the associated port. Therefore, the transfer of a signal event becomes similar to that of *CallEvent*. For example, a signal event containing a data *SignalData* arrives at a port *p* of a component *C*. The transformation derives an interface *SignalDataInterface* existing as the provided interface of *p*. *SignalDataInterface* has only one operation *pushSignalData* whose body will be generated to push the event to the event queue of the component. Therefore, the processing of a *SignalEvent* is the same as that of a *CallEvent*. In the following sections, the paper only considers *CallEvent* and *TimeEvent*.

A *TimeEvent* is considered as an internal event. The source state class of a transition triggered by a *TimeEvent* executes a thread to check the expiration of the event duration as in [19] and puts the time event in the event queue of the context class.

*3) Transformation of transitions and actions:* Each action is transformed into an operation in the transformed context class. *Entry/Exit/doActivity* actions have no parameters while transition actions and guards accept the triggering event object. *doActivity* is implicitly called in the *State* class and executed in a thread which is interrupted when the state changes.

*OnEntryAction* and *OnExitAction* - abstract methods in the base state class *State* - are called by the entry and exit methods, respectively. Lines 50-53 in Listing 1 show how these methods are overwritten by the *Operating* class. *Prepare* and *Disable*,
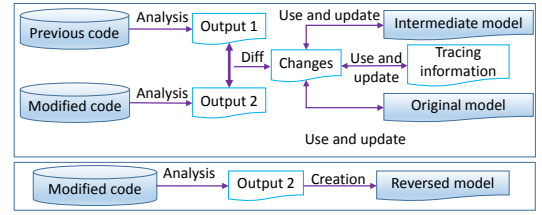


Fig. 6.  Overall method for reversing code to state machine

implemented in the context class, are called in these methods, respectively.

A transition is transformed into an operation taking as input the source state object and the event object similarly to DD. Transitions transformed from triggerless transition which has no triggering events accept only the source state object as a parameter. For example, the *Enable* action in the example is created in the context class and called by the transition method in lines 19-26. The guard *guard* is implemented as a method in the context class and called in line 21.

*D. Reverse engineering from code to USM*

This section describes the backward process.

*1) Method Overall:* The overall method for backward transformation is shown in Fig. 6. The modified code is first analyzed by partly inspecting the code syntax and semantics to guarantee that it is reversible. There are cases in which not all code modifications can be reversed back to the USM. The analysis also produces an output (*output2*) whose format is described later. If the intermediate model or the original USM is absent (the lower part of Fig. 6), a new intermediate model and a new USM are created from the UML model. In the contrary, the previous code taken, for instance, from control versioning systems is also semantically analyzed to have its output (*output1*) (the upper part of Fig. 6). *Output1* and *Output2* are then compared with each other to detect actual semantic changes which are about to be propagated to the original model.

Due to space limitation, we only show how to reconstruct (create) a new USM from the modified code.

*2) Illustration example:* To give an overview how the backward works, Fig. 7 presents a partition for mapping from the code segments generated from the example in Fig. 5 to actual USM concepts. Each partition consists of a code segment and the corresponding model element which are mapped in the backward direction. The *Stopped* class in code is mapped to a state.

*3) Semantic Analysis:* The output of the semantic analysis contains a list of event names, a list of state names, a list of transitions in which each has a source state, a target state, a guard function, an action function and an event represented in so called abstract syntax tree (AST) transition [15]. For example, Fig. 8 presents the EMF [20] representation of transitions in a **C++** AST in which *IStructure* and *IFunctionDeclaration*
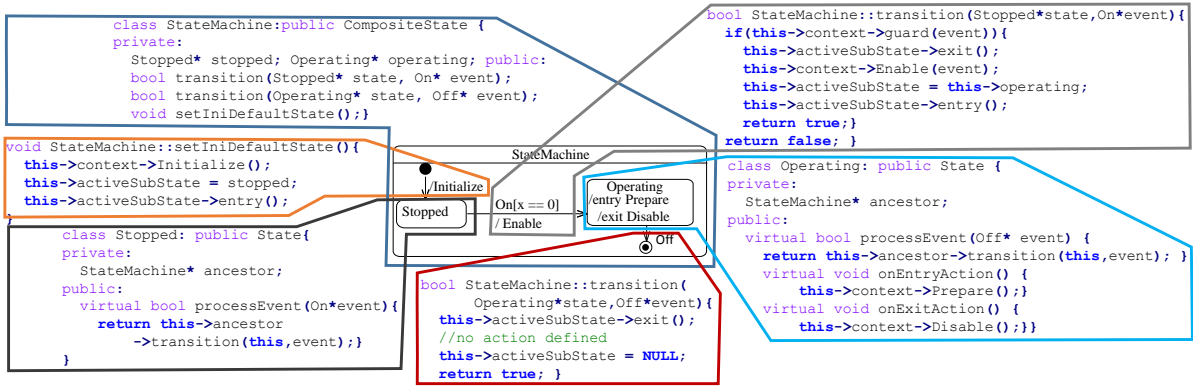
```
class StateMachine:public CompositeState {
private:
    Stopped* stopped; Operating* operating; public:
    bool transition(Stopped* state, On* event);
    bool transition(Operating* state, Off* event);
    void setIniDefaultState();}
```

```
bool StateMachine::transition(Stopped*state,On*event){
    if(this->context->guard(event)){
        this->activeSubState->exit();
        this->context->Enable(event);
        this->activeSubState = this->operating;
        this->activeSubState->entry();
        return true;}
    return false; }
```

```
void StateMachine::setIniDefaultState(){
    this->context->Initialize();
    this->activeSubState = stopped;
    this->activeSubState->entry();
```

```
class Operating: public State {
private:
    StateMachine* ancestor;
public:
    virtual bool processEvent(Off* event) {
        return this->ancestor->transition(this,event); }
    virtual void onEntryAction() {
        this->context->Prepare();}
    virtual void onExitAction() {
        this->context->Disable();}}
```

```
class Stopped: public State{
private:
    StateMachine* ancestor;
public:
    virtual bool processEvent(On*event){
        return this->ancestor
            ->transition(this,event);}
    }
```

```
bool StateMachine::transition(
        Operating*state,Off*event){
    this->activeSubState->exit();
    //no action defined
    this->activeSubState = NULL;
    return true; }
```

Fig. 7. USM element-code segment mapping partition

represent a structure and a function in **C++**, respectively. Each state name is also associated with an ancestor state, an entry action, an exit action, a default sub-state and a final state. The output is taken by analyzing the AST. The analysis process consists of recognizing different patterns. Table I shows the main patterns including state, transition and event.

---

**Algorithm 1** Semantic Analysis

---

**Input:** AST of code and a list of state classes $stateList$
**Output:** Output of semantic analysis
1: **for** $s$ in $stateList$ **do**
2:    **for** $a$ in attribute list of $s$ **do**
3:       **if** $a$ and $s$ match child parent pattern **then**
4:          put a and s into a state-to-ancestor map;
5:       **end if**
6:    **end for**
7:    **for** $o$ in method list of $s$ **do**
8:       **if** $o$ is $onEntryAction \parallel o$ is $onExitAction$ **then**
9:          $analyzeEntryExit(o)$;
10:      **else if** $o$ is $processEvent$ **then**
11:         $analyzeProcessEvent(o)$;
12:      **else if** $o$ is $setInitDefaultState$ & $s$ is composite **then**
13:         $analyzeInitDefaultState(s)$;
14:      **else if** $o$ is timeout & $s$ is a timedstate **then**
15:         $analyzeTimeoutMethod(o)$;
16:         $analyzeProcessEvent(s,o)$;
17:      **end if**
18:    **end for**
19: **end for**

---

Algorithm 1 shows the algorithm used for analyzing code semantics. Due to space limitation, *analyzeEntryExit*, *analyzeProcessEvent*, *analyzeInitDefaultState*, *analyzeTimeoutMethod* and *analyzeProcessEvent* are not presented but they basically follow the pattern description as above. In the first step of the analysis process, for each state class, it looks for an attribute typed by the state class, the class containing the attribute then becomes the ancestor class of the state class. The third steps checks whether the state class has an entry or exit action by looking for the implementation of the *onEntryAction* or *onExitAction*, respectively, in the state class to recognize the *Entry/Exit* action pattern. Consequently, event processing, initial default state of composite state and time event patterns are detected following the description as above.

*4) Construction of USM from analysis output:* If an intermediate model is not present, a new intermediate model and a new USM are created by a reverse engineering and
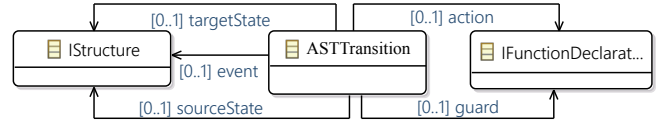


Fig. 8. Transitions output from the analysis

transformation from the output of the analysis process. The construction is straightforward. At first, states are created. Secondly, UML transitions are built from the AST transition list. Lastly, action/guard/triggering event of a UML transition is created if the associated AST transition has these.

For example, assuming that we need to adjust the USM example shown in Fig. 5 by adding a guard to the transition from *Operating* to the final state. The adjustment can be done by either modifying the USM model or the generated code. In case of modifying code, the associated transition function in Listing 1 is edited by inserting an *if* statement which calls the guard method implemented in the context class. The change detection algorithm adds the transition function into the updated list since it finds that the source state, the target state and the event name of the transition is not changed. By using mapping information in the mapping table, the original transition in the USM is retrieved. The guard of the original transition is also created.

## IV. ONGOING AND FUTURE WORK

### A. Towards synchronization of UML State Machine and programming languages

#### 1) Problem statement:

- Although code generation from UML State Machine is proposed by multiple approaches, a complete generation solution is not achieved yet (see I-A). Furthermore, none of existing code generators allows round-trip engineering or synchronization. This is, as previously discussed, one of the reasons why software development practitioners are reluctant to adopt MDE into practice.
- Synchronization of UML State Machine and code is hard,

TABLE I
PATTERN RECOGNITION FOR REVERSE ENGINEERING GENERATED CODE

| Pattern | Description |
|---|---|
| State | A state class inherits from the base state class or the composite base state class. For each state class, there must exist exactly one attribute typed by the state class inside another state class. The latter becomes the ancestor of the state class. |
| Composite state | A composite state class (CSC) inherits from the base composite state. For each sub-state the CSC has an attribute typed by the associated sub-state class. The CSC also implements a method named *setInitDefaultState* to set its default state. The CSC has a constructor is used for initializing all of its sub-state attributes at initializing time. |
| Entry action | If a state has an entry action, its associated state class implements *onEntryAction* that calls the corresponding action method implemented in the context class. Activity and exit patterns are recognized in the same way. |
| Event processing | If a state has an outgoing transition triggered by an event, the class associated with the state implements the *processEvent* method having only one parameter typed by the event class transformed from the event. The body calls the corresponding transition method of the ancestor class. |
| CallEvent | A call event class inherits from the base event class. The associated operation is found if the types of attributes of the event class match with the types of parameters of one method in the context class. A signal event is treated as a *CallEvent* as previously described. |
| TimeEvent | A transition is triggered by a *TimeEvent* if the state class associated with its source state implements the timed interface. The duration of the time event is detected in the transition method whose name is formulated as *"transition" + duration*. |
| Transition | Transition methods are implemented in the ancestor class, which is the class associated with the composite state owning the source state of the transition. The first parameter of the methods is the class representing the source state. The second parameter is the triggering event. Methods associated with *triggerless* transitions do not have a second parameter. The body of external and internal transition methods contains ordered statements including exiting the source state, executing transition action (effect), changing the active state to the target or null if the target is the final state, and entering the changed active state by calling entry. The body can have an if statement to check the guard of the transition. |
| Effect/ guard | Transition actions and guards are implemented in the context class. |

even impossible in case of resource constraints since one-to-one mappings from UML State Machine concepts to code statements are hard to achieve. Even, in simple cases where only states and transitions are used, the generated code size has a slightly larger memory overhead (see V-B) compared to traditional approaches such as if/else or nested switch statements.

*2) Idea overview:*

*a) **General idea:***
The general idea is to provide a mechanism from which software engineering stakeholders can profit in practice, e.g. software architects work with diagram-based languages while programmers are productive with text-based languages. This study is the realization of the approach in Fig. 2. To do it, A text-based domain specific language is proposed. This proposed language is descriptive and seamlessly integrated with diagrams and programming languages. The idea is inspired by the model-oriented programming language *Umple*[2]. The purpose of the proposed language is to provide a text-based DSL compliant to the UML State Machine specification, which is not correctly defined by Umple.

The language allows programmers productively write **UML-compliant and complete state machines** without restrictions in a textual way. **UML-compliance and completeness** focus on the full support for UML State Machine features and the semantics of generated code, and are key characteristics used to differentiate this proposed language from other non UML-compliant languages such as Umple and ThingML[3]. This proposed language is synchronized with UML State Machine in diagrammatic forms by using the generic pattern proposed in Section II. Generated code with full UML State Machine

features is achieved by using the generation solution in Section **??**. This language is a convergence of the generic pattern and the complete code generation to provide an efficient and productive way to develop reactive, real-time and embedded systems.

*b) **Advantages:***
Followings are advantages of this proposition:

- Software architects are freely to describe the behavior of systems by using state machine diagrams.
- Programmers are freely to work with a text-based environment to be productive.
- State machines used for generating code are not restricted to simple or non-concurrent cases as in other approaches.
- At anytime, generated code and software architects-built diagrams are consistent by using the generic synchronization pattern.

### B. Verification of semantic-conformance of generated code runtime execution

UML State Machine and its visualizations are widely used for modeling and designing real-time embedded systems. Although many existing approaches can generate code from state machines, the semantic conformance of runtime execution of generated code is not verified yet. The goal of this study is to provide a verification of code generated by the above generation approach.

Two approaches can be candidates for the verification. The first is to use bi-simulation (see Fig. 9), in which a state machine is simulated by the MOKA engine [21], which is a model simulator and offers PSSM. The same state machine is also used for generating code, which is compiled and executed. The execution traces obtained from the simulation and execution are then compared to each other. Generated code

---

[2]Umple, http://cruise.eecs.uottawa.ca/umple/
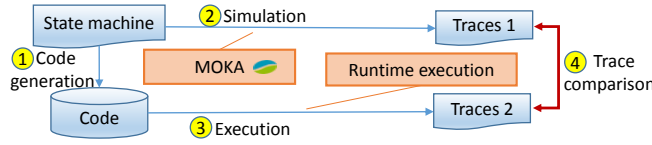[3]ThingML, http://thingml.org/

Fig. 9. Bi-simulation to test the semantic-conformance of generated code runtime execution

for a given state machine is considered semantic-conformant, within the scope of PSSM, if both of the traces are identical. Existing approaches had little chance to do the verification since PSSM is very new. The second one is to utilize model checking techniques, which model checks the generated code conforming to a specification, which is transformed from the state machine.

## V. OTHER WORK

This section summaries other works not detailed in this report. The first one is an rule execution scheduling for rule-based incremental transformations, which are directly related to the thesis. This work is published in **MODELSWARD** 2016[4]. The second one is a round-trip engineering approach for UML State Machine and object-oriented code. A paper based on this work is submitted to **SEW**[5] 2016.

### A. A rule execution scheduling-based incremental model transformation

Incremental model transformations (IMT) are used to synchronize different artifacts contributed by the stakeholders. IMTs detect changes on the source model and execute change rules to propagate updates to the target model. However, the execution of change rules is not straightforward. A rule is only correctly executed if its precondition is satisfied at execution time. The precondition checks the availability of certain source and target elements involved in the rule. If a rule is executed when the precondition is false, either the execution is blocked or stopped. Therefore, the produced target model becomes incorrect. This study presents two approaches to the scheduling of change rule execution in incremental model transformations. These approaches are also applied to the case of model and code synchronization and implemented in a tool named IncRoundtrip that transforms and generates code for distributed systems. We also compare the runtime execution performance of different incremental approaches with batch transformation and evaluate their correctness.

### B. From UML State Machine to code and back again

Although many industrial tools and research prototypes can generate executable code from such a graphical language, generated code could be manually modified by programmers. After code modifications, round-trip engineering is needed

to make the model and code consistent, which is a critical aspect to meet quality and performance constraint required for software systems. Unfortunately, current UML tools only support structural concepts for round-trip engineering such as those available from class diagrams.

This study addresses the round-trip engineering of UML state-machine and its related generated code as sketched in Fig. 2 (b). We propose an approach consisting of a forward process which generates code by using transformation patterns, and a backward process which is based on code pattern detection to update the original state machine model from the modified code.

This round-trip engineering only works for a limited sub-set of UML State Machine features. Specifically, only hierarchical state machines without pseudo states such as fork, join, junction, histories, choice are supported. Furthermore, to achieve the reverse direction of the RTE, the code generation of this approach uses a reversible mapping, which is an extension of the state pattern [22], [23]. Although the maintainability and collaboration (because of the RTE) are gained, compared to existing approaches such as switch/if [24], this pattern adds a slight memory overhead (around 13%).

## VI. CONCLUSION

Model-Driven Engineering is considered an efficient way to dealing with the complexity of systems today. MDE relies on two mechanisms abstraction and automation. The latter are realized by artifact synchronizations. Despite many advantages of MDE, the adoption level of MDE into industries is still not high as expected. In order to raise the adoption level, the core technologies of MDE need to be enhanced. This report presents the scope of the thesis, whose focus is to improve the core technologies of MDE such as artifact transformation, synchronization and code generation.

The report starts with describing major topics covered and developed in the deployment of the thesis. Different approaches around the technologies are proposed for wider integrating MDE into industrial practice to gain software quality and productivity. The proposed approaches are designed to support a continuous collaboration between software architects and programmers allowing each to use the working practices of choice

Two approaches including a generic pattern for artifact synchronization and a complete generation solution for UML State Machine are chosen to be detailed in this report because of their importance. Other works are also mentioned in the report. The overview of some ongoing and future works is also described to provide readers a plan for the next steps of the thesis deployment.

## REFERENCES

[1] S. Li, L. D. Xu, and S. Zhao, "The internet of things: a survey," *Information Systems Frontiers*, vol. 17, no. 2, pp. 243–259, 2015.

---

[4]MODELSWARD 2016, http://www.modelsward.org/?y=2016
[5]IEEE SEW 2016, https://www.fedcsis.org/2016/sew

[2] B. Selic, "What will it take? A view on adoption of model-based methods in practice," *Software & Systems Modeling*, vol. 11, no. 4, pp. 513–526, Oct. 2012.

[3] J. A. Cruz-Lemus, M. Genero, M. E. Manso, and M. Piattini, *Model Driven Engineering Languages and Systems: 8th International Conference, MoDELS 2005, Montego Bay, Jamaica, October 2-7, 2005. Proceedings*. Berlin, Heidelberg: Springer Berlin Heidelberg, 2005, ch. Evaluating the Effect of Composite States on the Understandability of UML Statechart Diagrams, pp. 113–125. [Online]. Available: http://dx.doi.org/10.1007/11557432_9

[4] J. Hutchinson, M. Rouncefield, and J. Whittle, "Model-driven engineering practices in industry," in *Proceedings of the 33rd International Conference on Software Engineering*, ser. ICSE '11. New York, NY, USA: ACM, 2011, pp. 633–642.

[5] N. C. C. Brown, M. Kolling, and A. Altadmri, "Position paper: Lack of keyboard support cripples block-based programming," in *Proceedings of the 2015 Blocks and Beyond Workshop*, Atlanta, GA, USA, 2015.

[6] J. Hutchinson, J. Whittle, and M. Rouncefield, "Model-driven engineering practices in industry: Social, organizational and managerial factors that lead to success or failure," *Science of Computer Programming*, vol. 89, pp. 144–161, Sep. 2014.

[7] A. Forward and T. C. Lethbridge, "Problems and Opportunities for Model-Centric Versus Code-Centric Software Development," *Proceedings of the 2008 international workshop on Models in software engineering - MiSE '08*, p. 27, 2008.

[8] T. Hettel, M. Lawley, and K. Raymond, "Model synchronisation: Definitions for round-trip engineering," in *Lecture Notes in Computer Science (including subseries Lecture Notes in Artificial Intelligence and Lecture Notes in Bioinformatics)*, vol. 5063 LNCS, 2008, pp. 31–45.

[9] S. Sendall and J. Kuster, "Taming Model Round-Trip Engineering."

[10] S. Sendall and J. Küster, "Taming model round-trip engineering," in *Proceedings of Workshop on Best Practices for Model-Driven Software Development*, Vancouver, Canada, 2004.

[11] E. J. Chikofsky, J. H. Cross, and others, "Reverse engineering and design recovery: A taxonomy," *Software, IEEE*, vol. 7, no. 1, pp. 13–17, 1990.

[12] SinelaboreRT, "Sinelabore Manual," http://www.sinelabore.com/lib/exe/fetch.php?media=wiki:downloads:sinelaborert.pdf. [Online]. Available: http://www.sinelabore.com/lib/exe/fetch.php?media=wiki:downloads:sinelaborert.pdf

[13] SparxSystem, "Enterprise Architect," http://www.sparxsystems.com/products/ea/, 2016.

[14] IBM, ""ibm rational rhapsody"," http://www.ibm.com/developerworks/downloads/r/rhapsodydeveloper/, 2016, [Online; accessed 14-Mar-2016].

[15] OMG, "Precise Semantics Of UML Composite Structures," no. October, 2015.

[16] ——, "Software & Systems Process Engineering Metamodel specification (SPEM) Version 2.0," http://www.omg.org/spec/SPEM/2.0/PDF, 2008.

[17] H. Giese and R. Wagner, "Incremental Model Synchronization with Triple Graph Grammars," in *Proceedings of the 9th international conference on Model Driven Engineering Languages and Systems*, Genova, Italy, 2006.

[18] V. Spinke, "An object-oriented implementation of concurrent and hierarchical state machines," *Information and Software Technology*, vol. 55, no. 10, pp. 1726–1740, Oct. 2013. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0950584913000670

[19] I. Niaz and J. Tanaka, "Mapping UML statecharts to java code." *IASTED Conf. on Software Engineering*, pp. 111–116, 2004. [Online]. Available: http://www.actapress.com/PDFViewer.aspx?paperId=16433

[20] R. Gronback, "Eclipse Modeling Project." [Online]. Available: http://www.eclipse.org/modeling/emf/

[21] "Moka Model Execution," https://wiki.eclipse.org/Papyrus/UserGuide/ModelExecution.

[22] A. Shalyto and N. Shamgunov, "State machine design pattern," *Proc. of the 4th International*, 2006. [Online]. Available: http://wscg.zcu.cz/rotor/net{\_}2006/papers{\_}2006/!proceedings{\_}short{\_}papers{\_}2006.pdf{\#}page=55

[23] B. P. Douglass, *Real-time UML : developing efficient objects for embedded systems*, 1999.

[24] G. Booch, J. Rumbaugh, and I. Jacobson, *The Unified Modeling Language User Guide*, 1998, vol. 3. [Online]. Available: http://portal.acm.org/citation.cfm?id=1088874
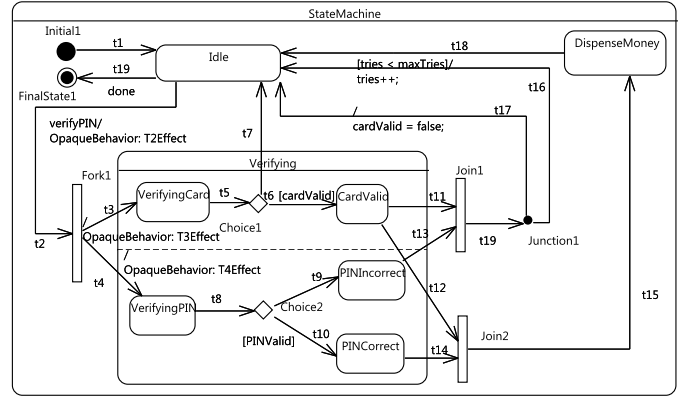
## VII. APPENDIX



Fig. 10. ATM State machine example

Listing 2. IState interface and function pointers in C++, in which S0 is one

```cpp
typedef struct IState {
  int previousActives[2];     int actives[2];
  EventId defEvents[2];
  void (C::*entry)();   void (C::*exit)();
  void (C::*doActivity)();
} IState;
class C {
private:
  IState states[NUM_STATES];
public:
  C() {
    states[S0_ID].entry = &C::S0_entry;
    defEvents[0] = EVENT_MAX;
    defEvents[1] = EVENT_MAX;
    ...
  }
  void S0_entry {...}
}
```

Listing 3. Example code generated for doActivity, the method in takes as input a state id to use and call the appropriate mutex and *doActivity*,

```cpp
void doActivity(int stateId) {
  isStarts[stateId] = false;
  while(true) {
    mutex[stateId].lock();
    while(!isStarts[stateId]) {
      mutex[stateId].wait();
    }
    states[stateId].doActivity();
    isStarts[stateId] = false;
    mutex[stateId].unlock();
    if (!isStops[stateId]) {
      if (stateId == IDLE_ID || stateId ==
    DISPENSEMONEY_ID ...) {
        pushCompletionEvent(stateId);
      }
    }
  }
}
```

Listing 4. Example code generated for the region of S1

```cpp
void S1Region1Enter(int enter_mode){
  if (enter_mode == DEFAULT) {
    states[S1_ID].actives[0] = S3_ID;
    states[S3_ID].entry();   sendStartSignal(S3_ID);
    S3Region1Enter(DEFAULT);
  } else if (enter_mode == S2_MODE) {  // entry
```

```
7        states[S1_ID].actives[0] = S2_ID;
         states[S2_ID].entry();    sendStartSignal(S2_ID);
9    } if (enter_mode == SH_MODE) {
         StateIDEnum his;
11       if (states[S1_ID].pres[0] != STATE_MAX){
            his = states[S1_ID].pres[0];
13       } else {
            his = S2_ID;
15       }
         states[S1_ID].actives[0] = his;
17       states[his].entry();    sendStartSignal(his);
         if (S3_ID == his) {
19          S3Region1Enter (S3_REGION1_DEFAULT);
         }
21   } else if (enter_mode == S4_MODE) {
         states[S1_ID].actives[0] = S3_ID;
23       states[S3_ID].entry();    sendStartSignal(S3_ID);
         S3Region1Enter(S4_MODE);
25   } else if (enter_mode == ENP_MODE) { ... }
```

Listing 4 shows the C++-like example code generated for entering the state $S1$ in **??**. In this case the entering model values are $\{DEFAULT = 0, SH\_MODE = 1, S2\_MODE = 2, S4\_MODE = 3, ENP_MODE = 4\}$. By default, the active sub-state of the region is set after the execution of any effect associated with the initial transition, $S3$ is set as active sub-state of $S1$. It is worth noting that after

the execution of each entry, a start signal is sent to activate the waiting thread associated with *doActivity* of the corresponding state.

Listing 5. Example code generated for *Join*1 and *Junction*1

```
1  if((states[VERIFYING_ID].actives[0]==CARDVALID_ID)
      &&(states[VERIFYING_ID].actives[1]==
         PININCORRECT_ID)) {
3     Junction1 = 0; //else outgoing transition of
         Junction1
      if (tries < maxTries) {Junction1 = 1;}
5     FORK(R1Exit); FORK(R2Exit);
      //JOIN ...
7     sendStopSignal(VERIFYING_ID); exit(VERIFYING_ID)
         ;
      FORK(effect_t11); FORK(effect_t13);
9     //JOIN ...
      if (Junction1=1) {
11       tries++;
         activeStateID = IDLE_ID;    entry(IDLE_ID);
         sendStartSignal(IDLE_ID);
13    } else {
         cardValid = false;
         activeStateID = IDLE_ID;    sendStartSignal(
         IDLE_ID);
      }
17 }
```

## VIII. CV and Global visions of activities

### A. Education

**6-2007**: Baccalaureate of high school Ly Thai To, Bac Ninh, Vietnam.

**2007-2012**: Hanoi University of Science and Technology, Vietnam.

- Programme: Programme de Formation d'Ingénieur d'Excellence au Vietnam (PFIEV).
- Specialty: Information System and Communication.
- Engineer Degree - Mention: Very well - Ranking: 3rd of the promotion.

**9/2013-9/2014**: Scholarship student of University of Paris Sud in Master 2 Research.

- Specialty: Embedded Systems and Information Processing cooperated by University of Paris Sud, ENS Cachan, INSTN and ENSTA ParisTech.

**From 11/2014**: PhD student at the laboratory of Model-Driven Engineering for Embedded Systems (LISE).

### B. Doctoral activities

#### 1) Publications: published, submitted and ongoing:

- Rule execution scheduling in incremental model transformation (Modelsward 2016, accepted): as mentioned in V-A, this work focuses on the execution order of transformation rules in incremental model transformations. Some preliminary results obtained through the experiments conducted with the model transformations defined in the Papyrus Designer framework, which offers a methodology and a framework for component and model-based development for distributed, real-time, embedded systems.

- Fostering Software Architect and Programmer Collaboration (ASE 2016, submitted): This work is originally motivated by the wish to support better collaboration between software architects and programmers in the project Papyrus-RT. The latter is developed under the cooperation between CEA and ZeligSoft. A generic pattern is proposed to synchronize different artifacts, which are concurrently modified. The pattern is evaluated by experiments, which are detailed in the paper.

- From UML State Machine to code and back again (SEW 2016, submitted): The objective is to provide a round-trip engineering from UML State Machine to code with some limitations to programmers' manipulation on the code-side. The output is a round-trip engineering approach supporting basic concepts of hierarchical UML State Machine. The approach is evaluated by experiments dedicated to different aspects of round-trip engineering and code generation.

- UML State Machine: Towards a complete code generation solution (to be submitted to ICECCS/APSEC 2016): This work is motivated by the project Papyrus Designer, in which the behavior of components is described using UML state machines. The purpose is to provide a complete code generation solution for full UML State Machine concepts with respect to the UML State Machine Specification, especially the concurrency. Furthermore, the code generated from state machines needs to be efficient in event processing speed and small enough in size to be suitable to micro-controllers. Preliminary experiments show that, for the same state machines, the size of the binary file compiled from the generated code is smaller around 50 times than that produced by the boost framework. Furthermore, the processing speed is faster around 40 times.

#### 2) Software Prototypes:

- CompleteUSM: An Eclipse plug-in, an extension of Papyrus, used to generate full UML State Machine with the support of all modeling features, especially concurrency aspect.

- PapyrusRTE: An Eclipse plug-in, an extension of Papyrus, used to collaborate software architects and programmers by synchronizing concurrently modified artifacts (model and code), and to help stakeholders produce high quality software.

- IncRoundtrip: A prototype supporting incremental model transformations in Papyrus Designer.

#### 3) Non-research activities:
**Teaching** at IUT

- Android programming project
- SQL and database

*4) Visits out of the student team:*

- Summer school DSM-TP: The summer school took place between 23-28 August 2015, in Belgium. This is an international summer school dedicated to practitioners over the world to join and discuss the different prospects of Model-Driven Engineering such as creating a domain specific modeling language or model transformation.

- Lise au Vert: This activity took place between 20-21 January, 2016, in Strasbourg, France. Participants are PhD students and post-docs of the laboratory LISE and two external professors. The purpose is to create an active working environment, outside of the laboratory, for young researchers, to find relationships between different research topics, and to possible propose a research project for the laboratory.

*C. Experiences*

**Internship at the laboratory of Model-Driven Engineering for Embedded Systems (LISE) - CEA**

- Works are in the context of methodologies of component-based development. The mission is to model interactions between components based on model-driven engineering: Understanding middleware ZeroMQ and DDS, using Papyrus to create UML distributed application models and the tool Qompass to transform these models to code. The code generated runs on those middleware.

**Project of embedded software architecture design for a SAFECRANE system**

- Requirements analysis of SafeCrane system which is established to provide a safe usage of the crane. It monitors some environment and physical characteristics to protect humans against crane collapses. The system warns human agents if the crane is unbalanced wind is too strong, activates an alarm and sends a message to the base-station.

**Software engineer for developing computer and embedded applications at Toshiba, Vietnam**:

- Requirements analysis, software architecture and detail design, coding (language C and C++ in Visual Studio 2010), unit test, integration test and optimization for software part of relay protection equipment. Using IEC 60870-5-103 to control and communicate between smart electric devices.

- Construction of PC application to control devices by using the private protocol of Toshiba and language C#.

**Project of design and implementation of multimedia player application** Using IDE Qt and the C++ library ffmpeg to implement a multimedia player application on Linux in Toshiba Company