A Comparative Study On Low Power Adders Using Microwind EDA Tool

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Abstract-- **From the past few years a variety of low power adders have been proposed to reduce the overall power consumption of micro-electronic systems. The role of adders are important I almost all filed of engineering and applied sciences. With the help of low power adders, all the other systems which make use of adders may dissipate less power. This study presents a detailed comparison between various low power 1-bit full adders. This study focus mainly on the comparisons among conventional CMOS adder, bridge style adder, transmission gate adder, square root based adder and static energy recovery full adder, etc. All the simulation results are done using Digital Schematic editor (DSCH) and the functionality is verified using the layout editor tool, Microwind. The sole objective of this study to conclude with a better estimate and ease in selecting a low power adder for the required application.**

Keywords- Bridge adder, CMOS adder, low power, Microwind, transmission gate, SERF

I. INTRODUCTION

Due to the semiconductor evolution technology growth, VLSI design engineers face challenges to design low power micro-electronic circuit subsystems. Designers have to propose with new ideas for digital low power VLSI design at the cost of area. While achieving the low power design, the area of the layout becomes overhead. This is the trade off experienced by most of the designers in the industry. Engineers who are specialist in design low power, high speed circuits with low area are most welcome in the application specific integrated circuits (ASIC) industry [1].

Adders are playing a crucial role in computer arithmetic logic circuit designs. Also in the field of signal processing integrated circuits, they are important for the operations like multiply and accumulate instructions [2]. Low power adders help in producing the low power multipliers which are most important in all kind of computing applications. By modifying the design little, adders may work as subtractors. A full adder help in counting the number of one's available in the given data which makes suitable for few applications like compression [3].

The importance of green energy and smart application based systems are understood by all kind of people to save the energy and power. Nowadays, these low power circuit designs are most suitable for the better environment. Since the battery technology evolution growth is poor compared semiconductor technology growth, the engineers focus designing low power systems by proposing suitable optimized circuit. For few applications, designers concentrate on power only at the cost of area and high speed. Because of the VLSI design trend and growth, the designers may integrate more and more number of transistors without worrying the size of the design. With respect to power, there are two major categories like static power dissipation and dynamic power dissipation. Static or leakage power occurs while the transistors are in the "off" mode and the dynamic power dissipation occurs during the switching activity of the transistors [1][4].

By reducing the supply voltage and the clock frequency of the system, the dynamic power dissipation is reduced dramatically. Also less loading capacitance helps in the reduction of switching power of the system [1]. By suppressing the unwanted transistors during the operation of the system, the static or leakage power is reduced in a significant manner.

This study discuss various adder design styles and compare them with respect to area and power dissipation. The simulation results are obtained with the help of DSCH and Microwind electronic computer aided design (ECAD) tools [5]. The first one, DSCH tool helps in obtaining the schematic for all the designs and the corresponding Verilog hardware description language (HDL) script is generated. The second one, Microwind helps to generate a layout by compiling the corresponding Verilog HDL script [6]. A functionality verification is done with each layout of the designs. The conventional adder is discussed in the section II. Al the remaining adders like bridge style adder, transmission gate adder, transmission function adder, square root based adder and static energy recovery adders are discussed with schematic in the section III. All the simulation results are obtained in the section IV with a comparison survey.

II. STANDARD CMOS ADDER

Standard CMOS adder has been the basic circuit for 1-bit addition with a total number of 28 transistors [7]. Here the sum operation requires four additional transistors than that of the carry operation and hence its output response shows an additional delay when simulated in the microwind tool. The circuit could be realized from the implementation of the following Boolean expressions (1):

$$Cout=ab+bc+c$$

Sum= $a \oplus b \oplus c$ (1)

This circuit is also found to consume more power because of its large number of transistors. It has been implemented using DSCH and then a Verilog file is generated and compiled in microwind with different technologies [5]. Fig.1 shows the schematic diagram of its implementation in DSCH and the timing diagram verification result is shown in Fig.2.

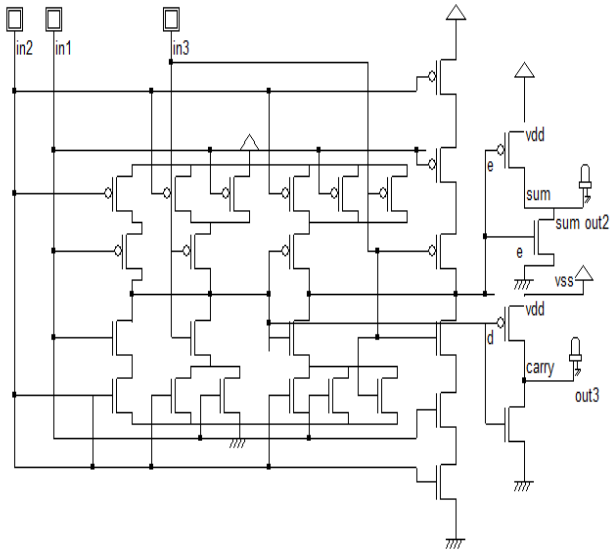

Figure 1. Standard CMOS adder

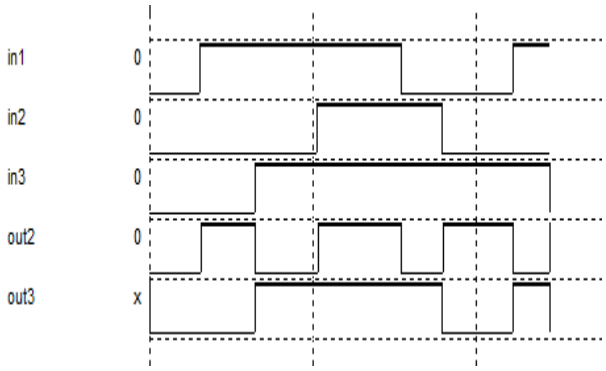

Figure 2. Timing diagram result

III. VARIOUS LOW POWER ADDER DESIGN – A COMPARISON STUDY

A. *Bridge style adder*

The bridge style adder is an effective implementation of two independent sum and carry outputs with only 26 transistors. Since the sum and carry circuits are independent of each other ,the delay from one is not transmitted to the other. As mention in reference[8][9], the transistors form a conditional conjunction between two nodes providing a new path to the output from source. The circuit can be realized from the standard boolean expression.

The implementation of this circuit requires few inputs to be negated, thus increasing the overall number of transistors by 6. However the circuit is capable of operating at high frequencies. The below shown figure suggests the circuit diagram. The circuit when implemented in microwind tool ,proved to consume more power than the standard CMOS adder. This bridge style is shown in Fig.3.

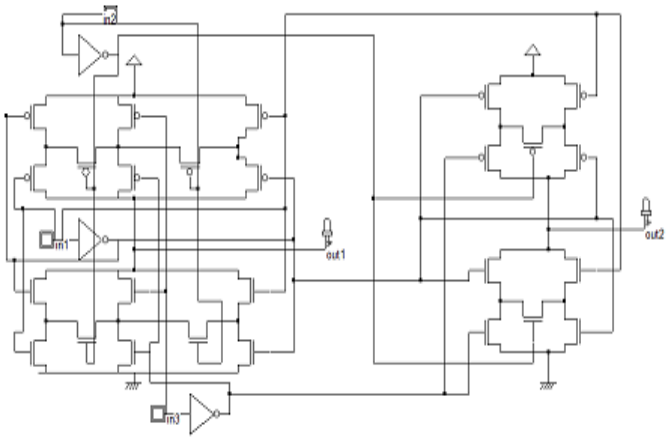

Figure 3. Bridge style adder

B. *Transmission gate adder*

A transmission gate adder is constructed with the help of just 12 transistors (excluding the 8 transistors used for negating the inputs). This circuit is viewed as an extended version of pass transistor logic, providing a maximum voltage level at the output [10]. This adder is quite mentioned in the literature many times as it consumes almost half of the power consumed by a conventional full adder. Fig.4 shows the circuit diagram of a transmission gate adder.

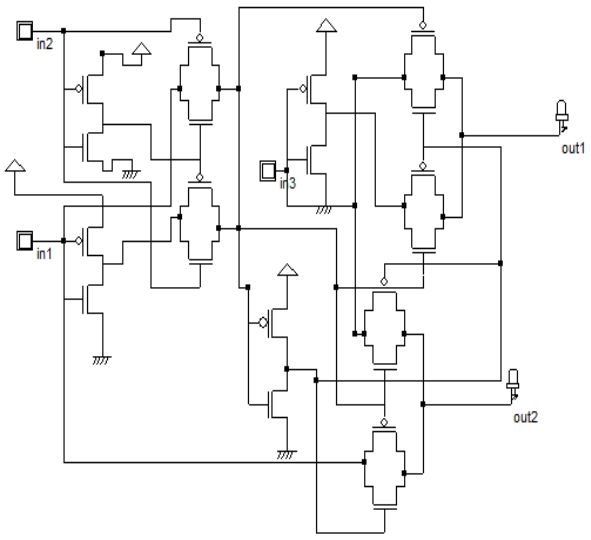

Figure 4.Transmission gate adder

C. *Transmission function adder*

The transmission function adder is based on the transmission function theory. This adder is constructed with the help of just 16 transistors. Thereby we achieve minimum power consumption at its best performance [10]. However when this adder is cascaded in series, it fails to provide a full voltage swing at the output. This is shown in Fig.5.

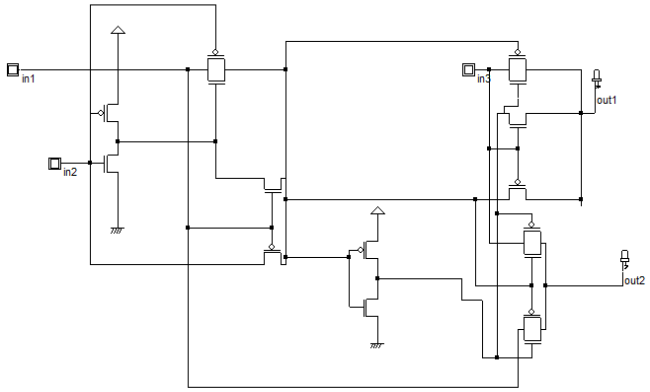

Figure 5.Transmission functional adder

D. *Square-root based adder*

This adder uses the Multiplexing Control Input Technique (MCIT) and Boolean reduction techniques for the sum and carry calculations [8]. This circuit is constructed with the help of 15 transistors including the invertors at the three inputs. Though this adder provides very less power consumption, its output voltage levels and time delays are found to be compromising. Fig.6 shows a square-root based adder which is developed using DSCH tool.

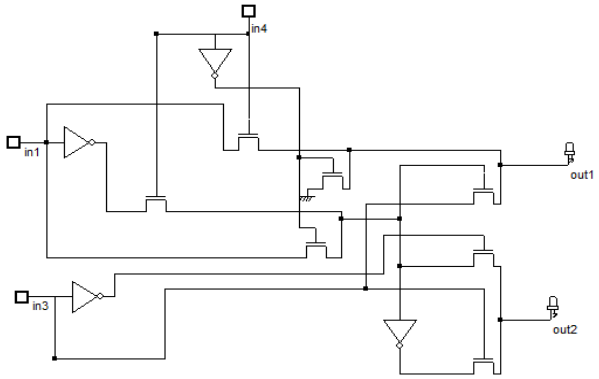

Figure 6.Square-root based adder

E. *SERF- Static Energy Recovery Full adder*

Of all the full adder circuits presented in this paper, SERF is the one which consumes least power. Here the requirement of ground and its corresponding connections are completely eliminated. A low logic level in the circuit substitutes the functionality of ground [11]. This design saves up to 18 transistors when compared with the standard CMOS transistor. The area occupied by its layout has also been recorded to be very less. This style is shown is Fig.7.

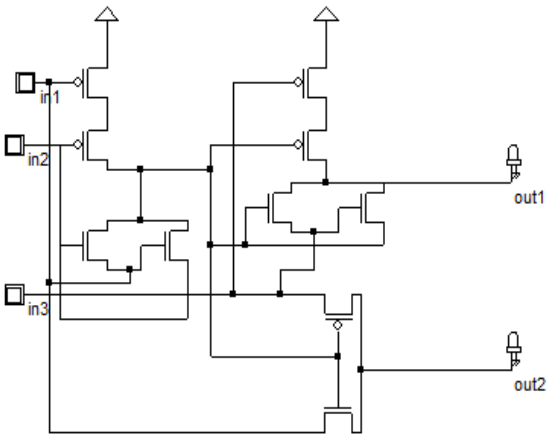

Figure 7.SERF (static energy recovery full adder)

IV. SIMULATION RESULTS

The layouts are generated with the help of Microwind layout editor and the functionalities are verified in each style. Fig.8 and 9 are shown the transmission gate adder layout and the timing diagram results respectively. Transmission function adder layout and functional simulation results are shown in Fig.10 and 11. SERF adder layout and functional simulation results are shown in Fig.12 and 13.

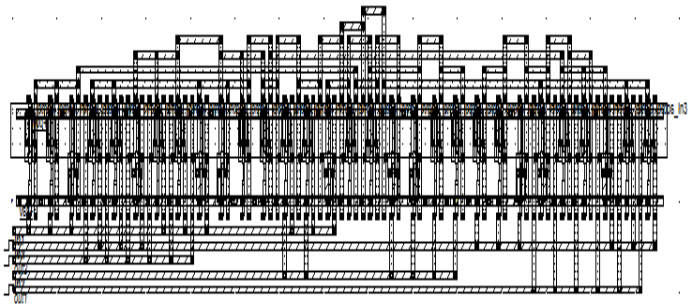

Figure 8.Transmission gate adder layout

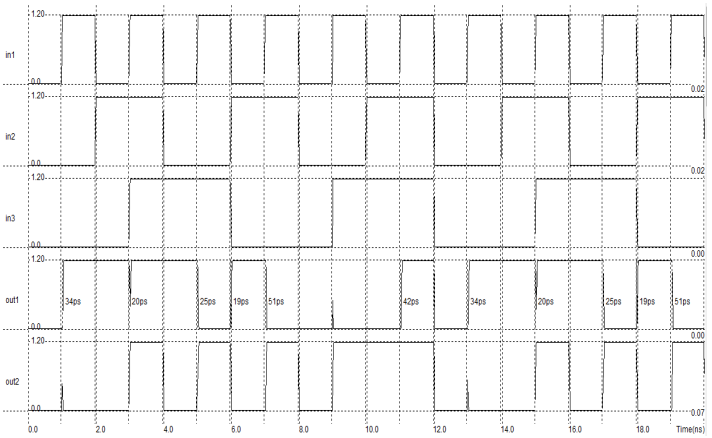

Figure 9.Simulation result of transmission gate adder

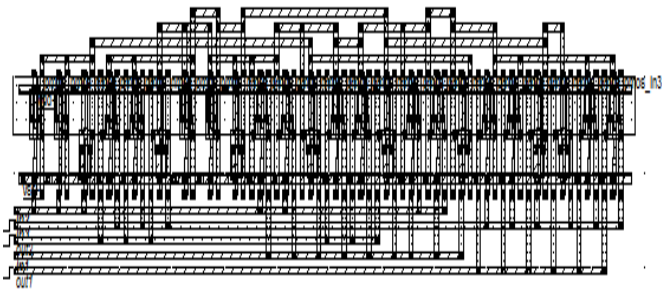

Figure 10.Transmission function adder layout

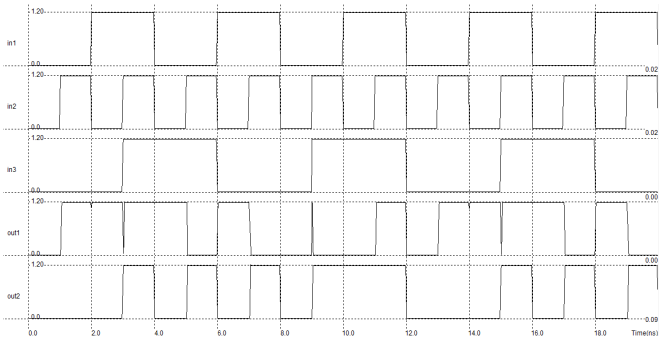

Figure 11.Simulation result of transmission function adder

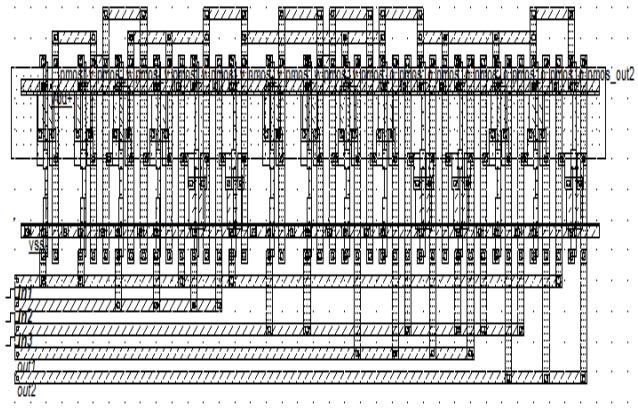

Figure 12. SERF adder layout

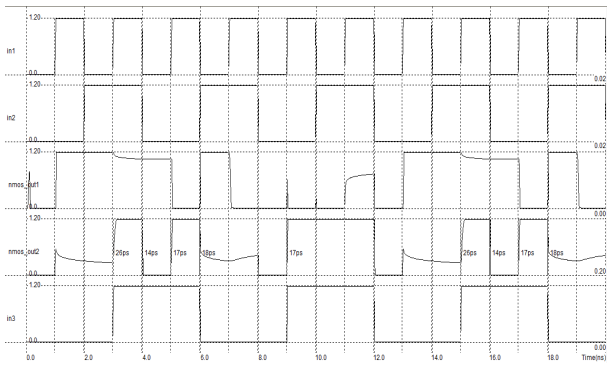

Figure 13. Simulation result of SERF adder

Dynamic power dissipation results for each adder style are obtained in the Table I. SERF adders are better compared with others in terms of power saving. Table II contains the number of transistors used for each style. Again SERF style adder shows better results compared with others. These simulation results are obtained using Microwind layout editor tool.

Table I. Comparison of adders – Power Dissipation

Design	50nm	90 nm	120 nm
Standard CMOS adder	1.771µW	14.97 µW	18.75 µW
Bridge style adder	2.520µW	22.39 µW	29.79 µW
Transmission gate adder	1.303µW	10.252µW	13.272µW
Transmission functional adder	0.648µW	5.706µW	7.39µW
Square root based adder	0.516µW	4.22µW	6.731µW
Static energy recovery full adder	0.345µW	4.553µW	4.291µW

Table II. Layout Area of Adders.

Design	Layout Area	Number of transistors
Standard CMOS adder	517.1 μm^2	28
Bridge style adder	649.3 μm^2	32
Transmission gate adder	414.5 μm^2	20
Transmission functional adder	299.4 μm^2	16
Square-root based adder	133.2μm^2	15
Static energy recovery full adder	168.7 μm^2	10

V. CONCLUSIONS

This study presents many important points that are frequently sought out while selecting a suitable low power adder. The simulation results show no significant difference between a traditional CMOS adder and the set of TGA,TFA adders in terms of their output response, making them a suitable choice for replacing the conventional adder. While the Bridge style adder leaves no advantage in terms of power consumption, it is definitely a good choice for circuits operating at high frequencies. The remaining two adders consume very less power but are compromising in their output voltage levels.

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