Reduced Area Multipliers

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Abstract

As developed by Wallace and Dadda, a high-speed method for the parallel multiplication of two binary numbers is to reduce their partial products to two numbers whose sum is equal to the product. The resulting two numbers are then summed using a fast carry-propagate adder. This paper presents a multiplier, the Reduced Area multiplier, with a novel reduction scheme which results in fewer components and less interconnect overhead than either Wallace or Dadda multipliers. This reduction scheme is especially useful for pipelined multipliers, because it minimizes the number of latches required in the reduction of the partial products. Equations are given for determining the number of components and a method is presented for estimating the interconnect overhead for Wallace, Dadda and Reduced Area multipliers. Area estimates indicate that pipelined Reduced Area multipliers require 3 to 8 percent less area than equivalent Wallace multipliers and 15 to 25 percent less area than equivalent Dadda multipliers.

1: Introduction

The demand for high-performance, application-specific processors has generated the need for maximum speed multipliers. A method for fast multiplication was originally proposed by Wallace [1] and later refined by Dadda [2,3]. Another implementation of a high-speed multiplier is Braun's carry-save scheme [4]. Braun's method is compared by Habibi and Wintz [5] to multipliers by Wallace and Dadda on the basis of speed, complexity and cost. Habibi's analysis indicates that while both Wallace's and Dadda's schemes offer the fastest multiplication, the issues of cost and complexity merit further attention.

Wallace [1] developed a method for fast multiplication based on parallel counters. By Wallace's method, the multiplication of two numbers is performed in the following sequence:

(1) Form all partial products in parallel.
(2) Reduce the matrix of partial products through a series of reduction stages to two numbers by strategically applying pseudo adders.
(3) Sum the two numbers produced in step 2 using a carry-propagate adder to generate the final product.

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Dadda [2,3] refined Wallace's method by recognizing that pseudo adders are (3,2) and (2,2) counters and defining a counter placement strategy that requires fewer counters at the cost of a larger carry-propagate adder. Both methods yield multipliers with total delays proportional to the logarithm of the operand word size, which is faster than array multipliers [6] or sequential multipliers (e.g., those employing Booth's algorithm [7]). Because of their short delay, Wallace and Dadda multipliers have been implemented in a number of existing systems [12-14].

The Reduced Area (RA) multiplier defined herein is a refinement of Wallace's and Dadda's methods. The reduction scheme of the RA multiplier differs from Wallace's and Dadda's methods in that the maximum number of (3,2) counters is used as early as possible, and (2,2) counters are carefully placed to reduce the word size of the carry-propagate adder. Employing (3,2) counters as early as possible minimizes the number of bits passing between successive stages in the reduction. This decreases the amount of interconnect and reduces the number of latches required by pipelined multipliers. Our area analysis indicates that for a given size multiplication, RA multipliers require less area than either Wallace or Dadda multipliers.

2: Reduction schemes

The multiplication of an M-bit multiplicand by an N-bit multiplier yields an N by M matrix of partial products. The reduction of this partial product matrix through the parallel application of (3,2) and (2,2) counters results in a matrix with a height of two. Each (3,2) counter accepts three inputs from a given column and produces a sum bit which remains in that column and a carry bit which goes into the next more significant column. A (2,2) counter accepts two inputs from a column and produces a sum bit in the same column and a carry bit in the next more significant column. In this section, the matrix reduction schemes for Dadda, Wallace, and RA multipliers are detailed with accompanying dot diagrams [2]. These three reduction schemes differ in the number and placement of (3,2) and (2,2) counters and the size of the carry-propagate adder.

2.1: Dadda multipliers

For the parallel application of (3,2) and (2,2) counters, Dadda [2] introduces a sequence of intermediate matrix heights that provides the minimum number of reduction stages for a given size multiplier. This sequence, determined by working back from the final two row matrix, limits the height of each intermediate matrix to the largest integer that is no more than 1.5 times the height of its successor. Table 1 lists the number of stages needed for partial product reduction based on the number of bits in the multiplier. For example, a 16 by 16 Dadda multiplier requires six reduction stages with intermediate matrix heights of 13, 9, 6, 4, 3, and finally 2. Although the heights of the intermediate matrices are not always the same for Wallace, Dadda, and RA multipliers, all three schemes require the same number of stages in the reduction.

Dadda's reduction scheme uses the following algorithm [11]:

(1) Let $d_1 = 2$ and $d_{j+1} = \lfloor 3 \cdot d_j / 2 \rfloor$, where d_j is the matrix height for the j-th stage from the end. Find the largest j such that at least one column of the bit matrix has more than d_j bits.

(2) Employ (3,2) and (2,2) counters to obtain a reduced matrix with no more than d_j elements in any column.

(3) Until a matrix with only two rows is generated, let j = j-1 and repeat step 2.

The dot diagram of a 12 by 12 Dadda multiplier is shown in Figure 1. This multiplier requires five stages (matrix heights of 9, 6, 4 3, 2) and uses 99 (3,2) counters, 11 (2,2) counters, and a 22 bit carry-propagate adder.

Table 1: Number of reduction stages.

Bits in multiplier (N)	Number of stages
3	1
4	2
$5 \le N \le 6$	3
$7 \le N \le 9$	4
$10 \le N \le 13$	5
$14 \le N \le 19$	6
$20 \le N \le 28$	7
$29 \le N \le 42$	8
$43 \le N \le 63$	9
$63 \le N \le 94$	10

2.2: Wallace multipliers

The dot diagram of a 12 by 12 Wallace multiplier is shown in Figure 2. In each stage of the reduction, Wallace performs a preliminary grouping of rows into sets of three. Within each three row set, (3,2) counters are employed to reduce columns with three bits to two bits. (2,2) counters are employed to reduce columns with only two bits. Rows which are not part of a three row set are transferred to the next stage without modification. The bits of these rows will be reduced in later stages. For example, in the second stage of the reduction for the 12 by 12 multiplier, the last two rows are left over and are not reduced until the following stage. The height of the matrix in the j-th reduction stage, w_j, is defined by the recursive equations.

$$w_0 = N$$

$$w_{j+1} = 2 \cdot \lfloor w_j / 3 \rfloor + (w_j \bmod 3)$$

The 12 by 12 Wallace multiplier requires five stages (matrix heights of 8, 6, 4, 3, 2) and uses 102 (3,2) counters, 34 (2,2) counters, and an 18 bit carry-propagate adder.

2.3: RA multipliers

The dot diagram for a 12 by 12 RA multiplier is shown in Figure 3. The RA multiplier performs the reduction as follows:

(1) For each stage, the number of (3,2) counters used in each column is $\lfloor b_i / 3 \rfloor$, where b_i is the number of bits in column i. This provides the maximum reduction in the number of bits entering the next stage.
(2) (2,2) counters are used only (a) when required to reduce the number of bits in a column to the number of bits specified by the Dadda series, or (b) to reduced the rightmost column containing exactly two bits.

In Figure 3, rule (2a) dictates that in stage 3 of the reduction two half adders are used to reduce the number of bits in columns 11 and 12 to four. Rule (2b) adds one (2,2) counter to each stage of the reduction. This has the advantage of decreasing the word length of the carry-propagate adder by an amount equal to the number of stages used in the reduction. The 12 by 12 RA multiplier requires five stages (matrix heights of 8, 6, 4, 3, 2) and uses 104 (3,2) counters, 11 (2,2) counters, and a 17 bit carry-propagate adder.

2.4: 8 by 8 multipliers

As a second example of the reduction schemes, dot diagrams are shown in Figure 4 for 8 by 8 Dadda, Wallace, and RA multipliers. A summary of the hardware requirements for 8 by 8 and 12 by 12 multipliers is given in Table 2. Dadda's method always uses the fewest (3,2) counters and has the largest carry-propagate adder. The RA method uses the most (3,2) counters, but has the smallest carry-propagate adder.

Table 2: Hardware requirements for various multipliers.

Reduction Scheme	(3,2) counters	(2,2) counters	Adder Length
Dadda (12 by 12)	99	11	22
Wallace (12 by 12)	102	34	18
RA (12 by 12)	104	11	17
Dadda (8 by 8)	35	7	14
Wallace (8 by 8)	38	15	11
RA (8 by 8)	39	7	10

3: Multiplier comparisons

This section gives algebraic expressions for the number of (3,2) and (2,2) counters used in the reduction, and the word-length of the carry-propagate adder. It also compares the interconnection overhead for the various reduction schemes and describes advantages that RA multipliers have over Wallace and Dadda multipliers. In the discussion to follow, the multipliers are N by M ($M \geq N \geq 3$). The number of AND gates needed for the partial product generation is the same for all schemes and is equal to N·M. The total number of reduction stages is S.

3.1: Dadda multipliers

The number of (3,2) counters required for the partial product reduction is determined by subtracting the number of bits in the final two row matrix from the number of bits in the original matrix. This is because each (3,2) counter reduces

the number of bits in the matrix by one. For Dadda multipliers, there are N·M bits in the original matrix and 2·(N + M) - 3 bits in the final two row matrix. Thus, the total number of (3,2) counters needed for an N by M Dadda multiplier is

$$N \cdot M - 2 \cdot (N + M) + 3$$

The word-length of the carry-propagate adder is N + M - 2.

To determine the number of (2,2) counters required in the Dadda reduction scheme, the following observations are made:

(1) The number of (2,2) counters required in the first stage of reduction is $(N - d_s + 1)$, where d_j is the number of bits specified by the Dadda sequence for the j-th reduction stage from the end and S is the number of reduction stages.

(2) The number of (2,2) counters required in the j-th reduction stage from the end (for $2 \le j \le s$) is $(d_j - d_{j-1})$.

Thus, the total number of (2,2) counters needed is

$$(N - d_s + 1) + (d_s - d_{s-1}) + \ldots + (4 - 3) + (3 - 2) = N - 1$$

Habibi and Wintz [5] established that Dadda's method of reduction is optimum in the sense that it uses the minimum number of (3,2) counters. In addition, (N-1) is the minimum number of (2,2) counters for any scheme which minimizes the number of (3,2) counters. A scheme with fewer (2,2) counters can be developed, but it will require an increase in the number of (3,2) counters.

3.2: Wallace multipliers

The hardware requirements for Wallace multipliers are determined in a similar manner. The number of bits in the final two row matrix of a Wallace multiplier is

$2 \cdot (N + M) - 3 - S$ $\quad (3 \le N < 6)$

$2 \cdot (N + M) - 2 - S$ or $2 \cdot (N + M) - 1 - S$ $\quad (N \ge 6)$

For $N \ge 6$, there will be either one or two bits in the most significant column of the two row matrix, depending on the values of N and M. The number of (3,2) counters and the word length of the carry-propagate adder are

$$(3 \le N < 6)$$

$$\#(3,2) = N \cdot M - 2 \cdot (N + M) + 3 + S \quad \text{Adder length} = N + M - 2 - S$$

$$(6 \ge N)$$

$$\#(3,2) = N \cdot M - 2 \cdot (N + M) + 2 + S \quad \text{Adder length} = N + M - 1 - S$$

or

$$\#(3,2) = N \cdot M - 2 \cdot (N + M) + 1 + S \quad \text{Adder length} = N + M - 1 - S$$

The number of (2,2) counters is at least N - 1, and is often much greater than N. For example, for multiplier sizes of 16 by 16, 32 by 32, and 64 by 64, the number of (2,2) counters needed are 54, 171, and 459, respectively.

3.3: RA multipliers

The hardware requirements for RA multipliers are

$$\#(3,2) = N \cdot M - 2 \cdot (N + M) + 3 + S$$

$$\#(2,2) = N - 1$$

$$\text{Adder length} = N + M - 2 - S$$

Compared to Dadda multipliers, RA multipliers use the same number of (2,2) counters and S more (3,2) counters. However, the word length of the carry-propagate adder is S bits less. Since, in general, one bit in a carry-propagate adder requires more hardware than a (3,2) counter, this will result in a net hardware advantage for the RA multiplier. The smaller size of the carry-propagate adder may also result in a modest speed advantage, depending on the values of N and M, and the implementation of the carry-propagate adder. Wallace multipliers and RA multipliers use approximately the same number of (3,2) counters and have approximately the same size carry-propagate adders. RA multipliers, however, use significantly fewer (2,2) counters than Wallace multipliers, especially when N and M are large.

3.4: Reduced interconnection

Another advantage of the RA reduction scheme is the decrease in the number of bits in the partial product matrix as early as possible. This results from the usage of the maximum number of (3,2) counters in each reduction stage. The RA reduction scheme also limits the number of bits that are passed between successive stages without being summed. These two features are advantageous since they reduce the interconnect overhead which occurs due to the routing of partial product bits.

To compare the interconnection overhead due to bits passing between successive reduction stages, the number of bits going into stage i is defined to be g_i. The sum of all bits passing between successive stages is

$$G = \sum_{i=1}^{S+1} g_i$$

where g_{s+1} is the number of bits going into the carry-propagate adder. The value of g_i is

$$g_i = N^2 \qquad \text{(for } i = 1\text{)}$$

$$g_{i+1} = g_i - (3,2)_i \qquad \text{(for } 2 \le i \le S\text{)}$$

where $(n,m)_i$ is the number of (n,m) counters in stage i. Similarly, the number of bits which pass through stage i without being summed by a (3,2) counter or (2,2) counter is defined as p_i. Their sum is

$$P = \sum_{i=1}^{S} p_i$$

with

$$p_i = g_i - 3\cdot(3,2)_i - 2\cdot(2,2)_i$$

The values of P and G for 12 by 12 and 8 by 8 multipliers are given in Table 3.

Table 3: Interconnection estimates for various multipliers.

Reduction Method	G	P
Dadda (12 by 12)	594	213
Wallace (12 by 12)	491	75
RA (12 by 12)	473	95
Dadda (8 by 8)	243	100
Wallace (8 by 8)	241	45
RA (8 by 8)	204	39

For given values of M and N, RA multipliers always have the lowest value of G, while Dadda multipliers have the highest. Dadda multipliers only employ (3,2) counters (i.e., reduce the number of bits in the matrix) when their use is required to reduce the number of bits in a column to the next value in the Dadda series. Reducing the maximum number of bits in the earlier stages is especially desirable for pipelined implementations, because latches that are used to store bit values between stages are eliminated. Either Wallace multipliers or RA multipliers will have the lowest value of P, depending on the values of M and N.

As an example of the decrease in number of bits passing between successive stages of the reduction, consider the first reduction stage, with N = M. For Dadda multipliers, the reduction in the number of bits (i.e., the number of (3,2) counters) in the first stage is

$$(N - d_s)^2 - 1 < N^2 / 9.$$

For Dadda multipliers with N close to d_s, the reduction in the number of bits in the first stage will be very small. In comparison, the reduction in the number of bits in the first stage for RA multipliers is

$$2 \cdot N \cdot x - 3 \cdot x^2 - 2 \cdot x$$

where $x = \lfloor N / 3 \rfloor$. Since $x \approx N / 3$, this reduction can be approximated as

$$\frac{N^2 - 2 \cdot N}{3}$$

For Wallace multipliers, the number of bits reduced in the first stage is

$$\lfloor N / 3 \rfloor \cdot (N - 2)$$

which is less than or equal to the reduction in the first stage for RA multipliers. For example, with 32 by 32 bit multipliers, the number of bits reduced in the first stage is:

Dadda: 15 Wallace: 300 RA: 320

4: Area estimates

Estimations of the total relative area required by Dadda, Wallace, and RA multipliers are listed in Tables 4 and 5 for several values of N, with M = N. The relative areas for each of the components are based on data from the LSI Logic standard cell data book [8]. The relative interconnection areas come from the examination of interconnection areas of existing multipliers. The relative areas of the AND gates, (2,2) counters, and (3,2) counters are 8, 26, and 52, respectively. The relative area of the interconnect of each bit entering a stage in the matrix is 1 if the bit is summed within the stage and 2 if it is not. The carry-propagate adder is assumed to be implemented as a carry look-ahead adder (CLA) which employs 4-bit carry look-ahead modules (including modified full adders and carry look-ahead logic) with a relative area of 420 at the first level, and 4-bit carry look-ahead blocks with a relative area of 250 at higher levels. For the pipelined multipliers the relative area of a 1-bit latch is 26. Each stage of the reduction is assumed to be pipelined, as is the CLA. The number of latches required for the reduction is equal to G, the total number of bits passing between stages. The number of latches for a k-bit CLA is estimated from [9] as

$$8 \cdot \lceil k / 4 \rceil + 21 \cdot \lceil k / 4 \rceil \cdot \lceil \log_4(k) - 1 \rceil$$

Table 4: Area comparisons for non-pipelined multipliers

		Dadda		Wallace	
n	RA Area	Area	% Increase	Area	% Increase
8	4511	4809	6.6	4681	3.8
16	17269	18349	6.3	18728	8.4
24	38215	40067	4.8	40318	5.5
32	67351	70859	5.2	70880	5.3
40	104789	108621	3.7	109301	4.3
48	150185	157933	5.2	156727	4.3
56	203292	211604	4.1	211326	4.0
64	264548	281016	6.2	276044	4.3

Table 5: Area comparisons for pipelined multipliers

		Dadda		Wallace	
n	RA Area	Area	% Increase	Area	% Increase
8	11873	13900	17.1	12293	3.5
16	46594	57024	22.4	50778	9.0
24	99065	120542	21.7	103393	4.4
32	170415	215360	26.4	178230	4.6
40	267316	317240	18.7	275104	2.9
48	378448	481862	27.3	391764	3.5
56	503114	614116	22.1	521872	3.7
64	649332	867714	33.6	679248	4.6

RA multipliers have the lowest total area for all multiplier sizes examined. For non-pipelined multipliers, the increase in area compared to the RA multiplier varied from 3.7 to 6.6 percent for Dadda multipliers, and from 3.8 to 8.4 percent for Wallace multipliers. For pipelined multipliers, the increase in area for Dadda multipliers ranged from 17.1 percent to 33.6 percent, and from 2.9 to 9.0 percent for Wallace multipliers. The large increase in area for pipelined Dadda multipliers is primarily due to the number of latches that are required for the early stages of the reduction.

5: Two's complement multipliers

The RA reduction scheme also offers an advantage for two's complement multipliers. Figure 5 shows the multiplication matrices for 8 by 8 two's complement Dadda, Wallace, and RA multipliers. For N by N two's complement multipliers, the most significant bit (msb) of the first N-1 partial products and all the bits except the msb of the last partial product are complemented and a one is added to column N-1. The net change in hardware is that 2·N - 1 of the AND gates are changed to NAND gates, and one of the (2,2) counters in column N-1 is changed to a (3,2) counter. For Dadda and Wallace multipliers, the (2,2) counter is changed to a (3,2) counter in the first reduction stage. For RA multipliers, this change occurs in the first reduction stage which requires a half adder to meet the number of bits specified by the Dadda series. Thus, the reduction in area achieved by the RA multiplier for a given value of N is approximately equal for two's

complement and unsigned (or sign-magnitude) numbers. A more detailed discussion of N by M two's complement multipliers is given in [10].

6: Conclusion

In this paper, a novel partial product reduction scheme has been presented. This reduction scheme can be implemented for sign-magnitude or two's complement multipliers. Area estimates demonstrate that RA multipliers offer an advantage over Dadda and Wallace multipliers. They require fewer components and have less interconnect for both pipelined and non-pipelined implementations. RA multipliers may also have a modest speed advantage over Dadda multipliers since they employ a smaller carry-propagate adder.

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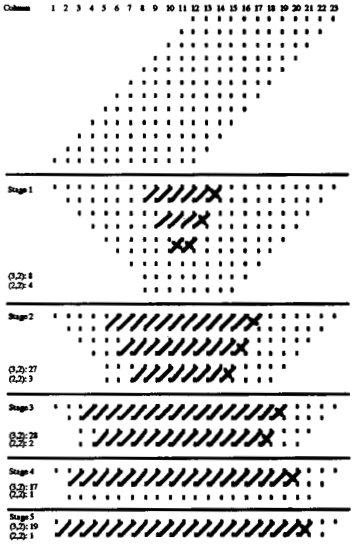

Figure 1: 12 by 12 Dadda Multiplier.

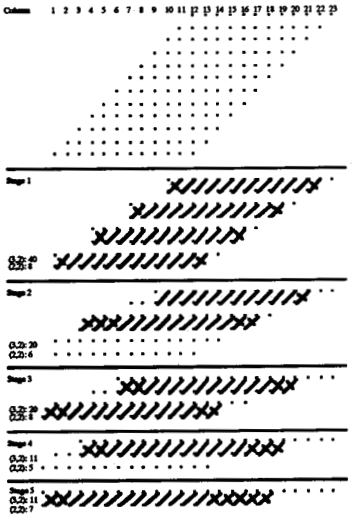

Figure 2: 12 by 12 Wallace Multiplier.

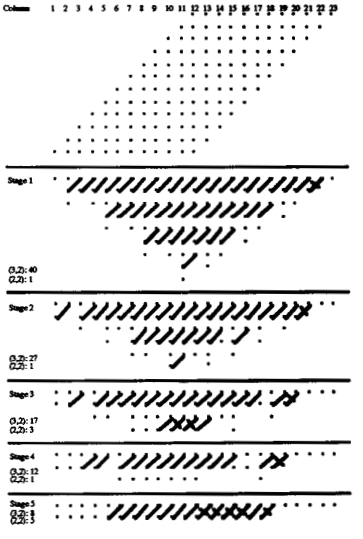

Figure 3: 12 by 12 RA Multiplier.

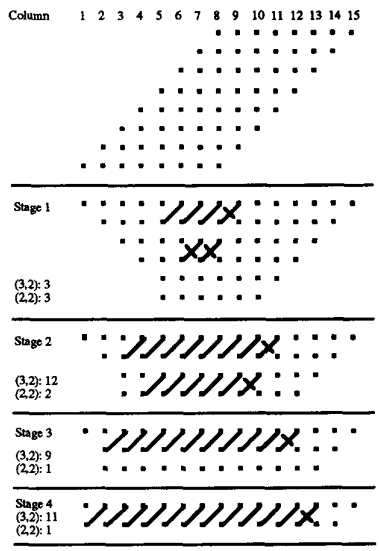

Figure 4a: 8 by 8 Dadda Multiplier.

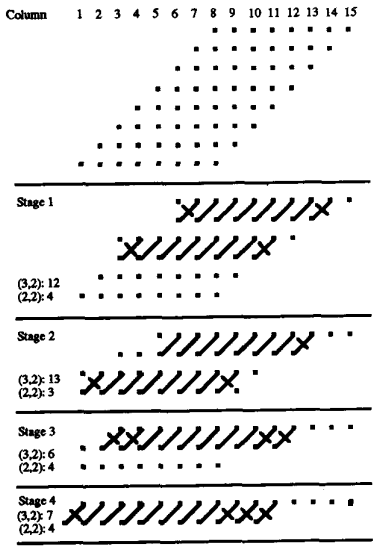

Figure 4b: 8 by 8 Wallace Multiplier.

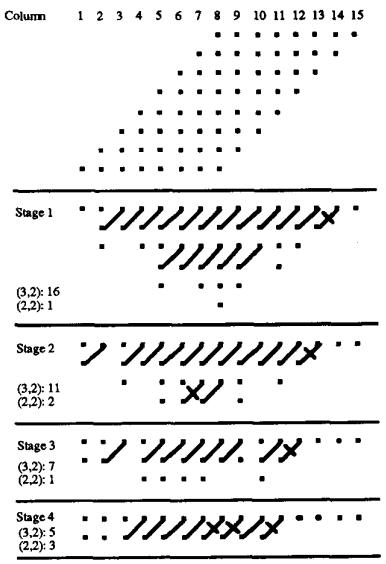

Figure 4c: 8 by 8 RA Multiplier.

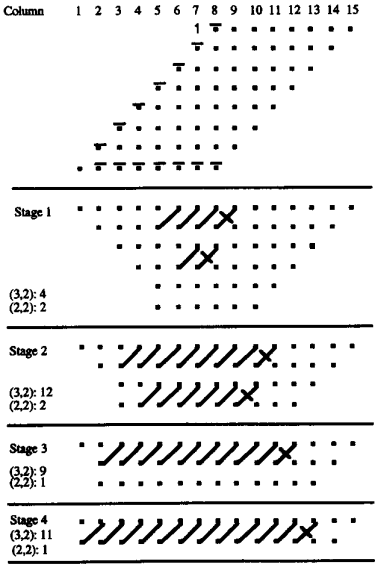

Figure 5a: 2's Comp. Dadda Multiplier.

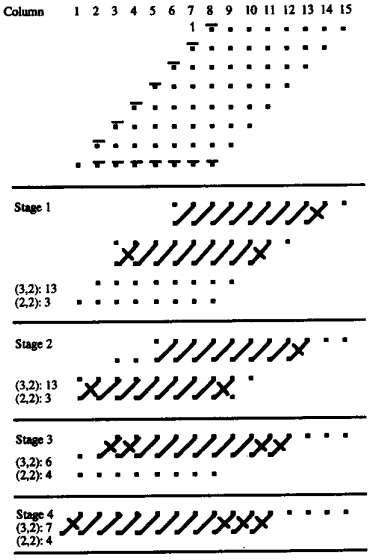

Figure 5b: 2's Comp. Wallace Multiplier.

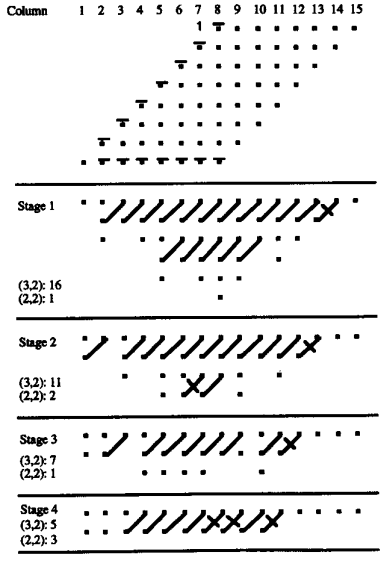

Figure 5c: 2's Comp. RA Multiplier.