ADVD
Assignment 1
EEE F313

Problem set 72

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Problem 1

Design a 4:1 multiplexer using CMOS logic style. Simulate with a 500fF load capacitance

Solution

Schematic design

The schematic design is shown below

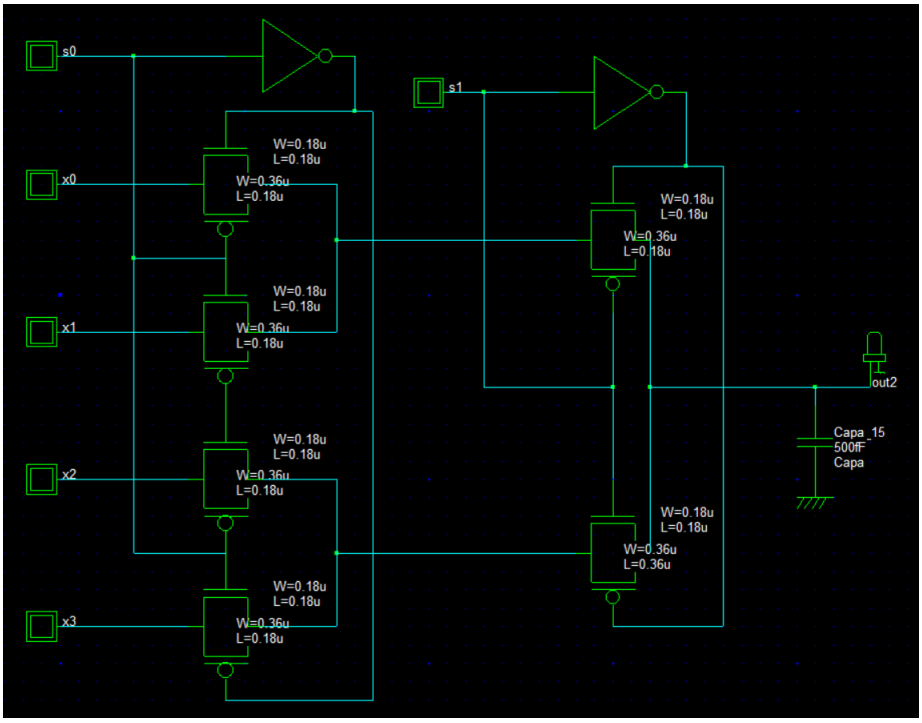

Figure 1: Schematic design for a 4:1 mux using transmission gates

Layout design

Since we're using the cmos018.rul library, we have the value of L as 180nm. We chose the value of W/L as 1 for all NMOS and 2 for all PMOS. This implies the value for W and L for NMOS is 180nm. W and L values for PMOS is 360nm and 180nm respectively. The layout design is shown below.

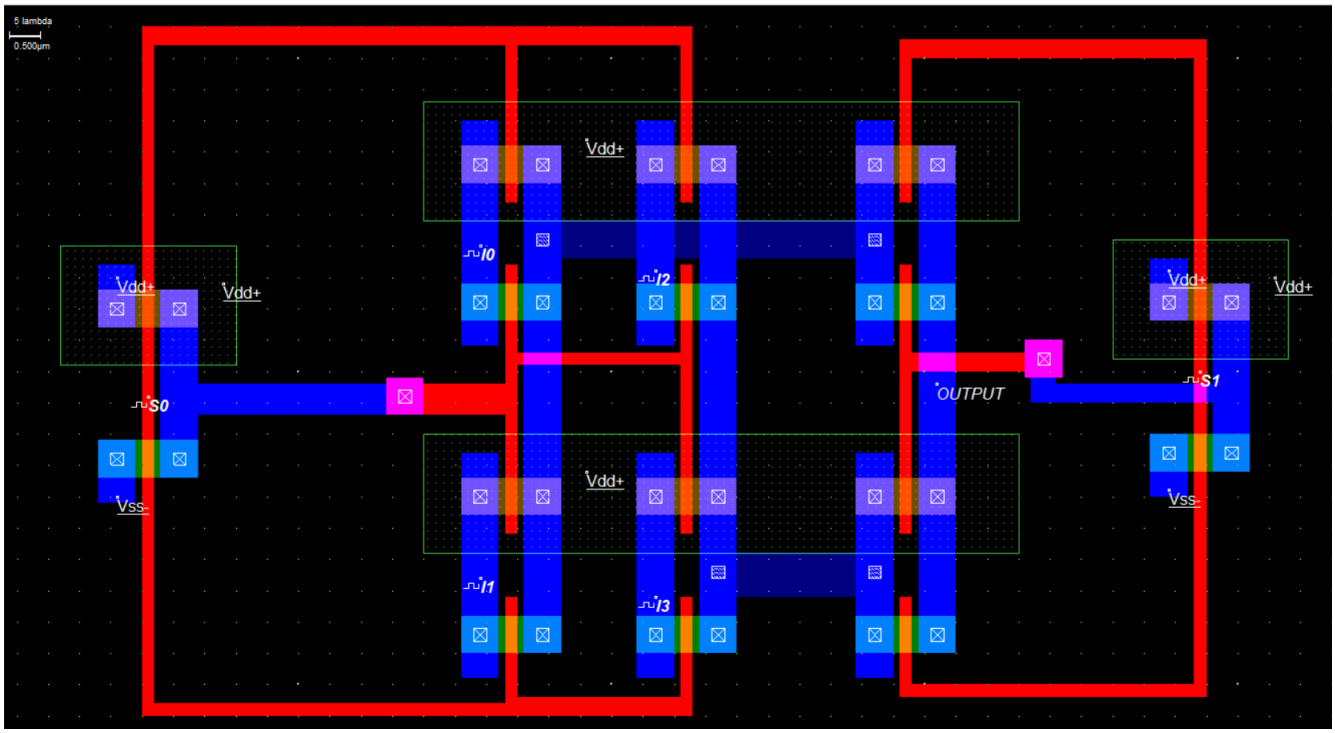

Figure 2: Layout design

Reasoning From the spice netlist of the circuit we found that the value of μ_n and μ_p were 380 and 200 units respectively. Equating $\mu_n C_{ox} \frac{W}{L}$ of NMOS to $\mu_p C_{ox} \frac{W}{L}$ of PMOS and keeping the value of L constant for both PMOS and NMOS at 180nm, we came to the relation of $\frac{W_p}{W_n} = 1.9 \approx 2$. This is why the value of W for PMOS is taken to be 360nm and W for NMOS is taken to be 180nm.

Area, power consumption and delays

Area of the layout As per the statistics generated by Microwind, the area of the layout is $23.4\mu\text{m} \times 11.0\mu\text{m} = 257.4\mu\text{m}^2$

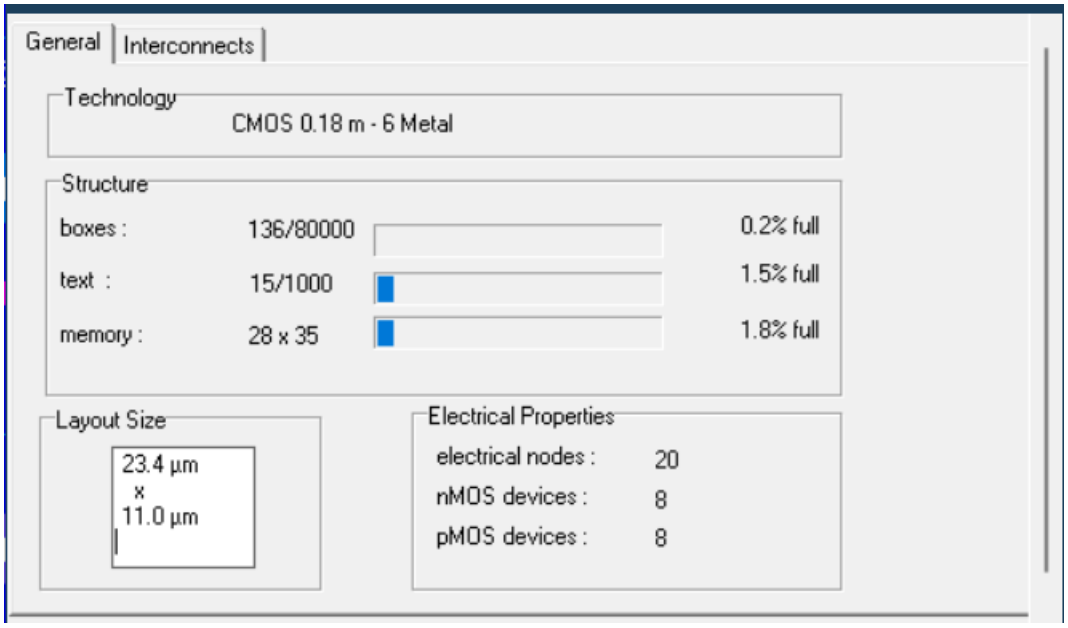

Figure 3: Area of the layout

Power consumption As per the graph below, the power consumed by circuit comes out to be $71.904\mu\text{W}$.

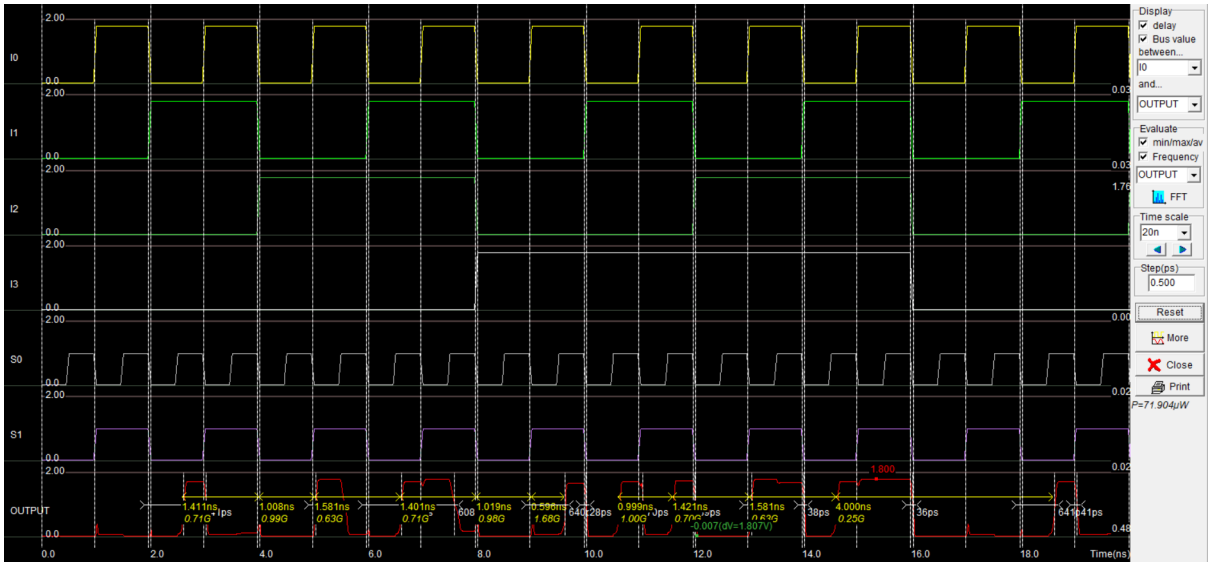

Figure 4: Voltage vs time graph

Delay calculation The average propagation delay calculated is 0.164ns.

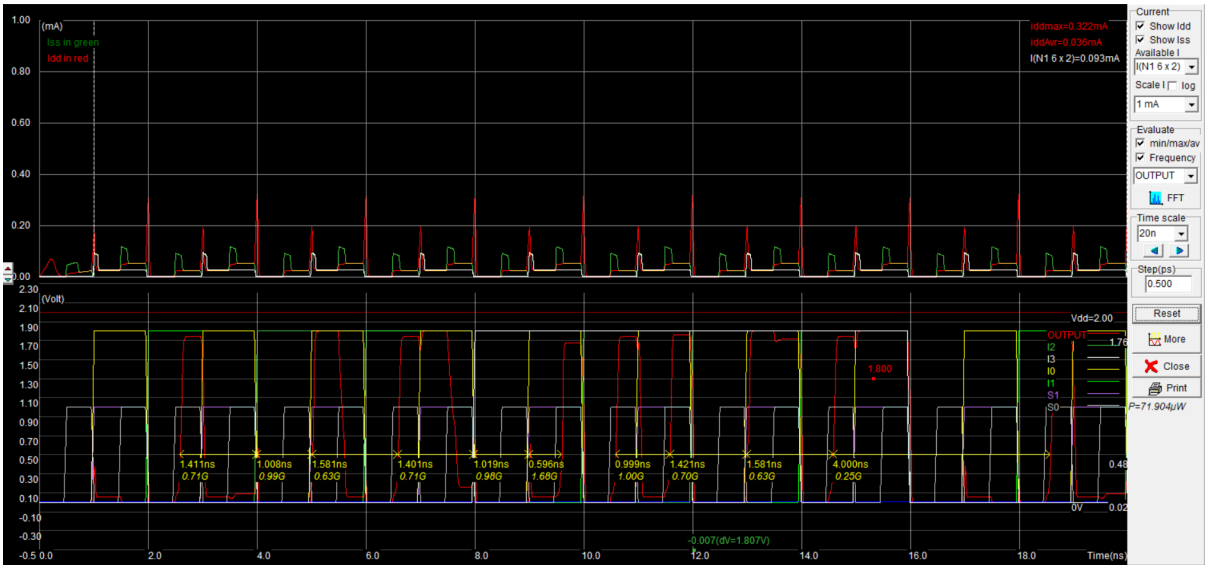

Figure 5: Voltage vs time and current vs time graphs

Layout design generated by Microwind

Corresponding to the verilog file generated for the schematic shown in Figure 1, Microwind has generated the following layout

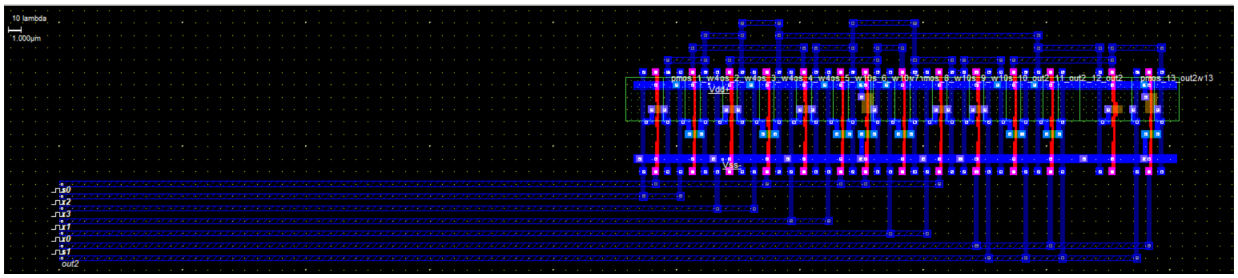

Figure 6: Layout generated by Microwind

The silicon area occupied by this layout is found to be 1777.7 μm^2 which is considerably larger than the area that is occupied by the layout shown in Figure 2. The power consumed is also found to be 0.141mW which is significantly higher than the power consumed by the previous layout design. In addition to this, the output waveform is also seen to incorporate more noise and propagation delay. Considering these factors, we have decided to choose Figure 2 as the final layout design for the given problem statement

Problem 2

Design a modulo-6 counter, which counts in the sequence 0, 1, 2, 3, 4, 5, 0, 1$\cdots$. The counter counts the clock pulses if its enable input, E, is equal to 1. Use D flip-flops in your circuit.

Solution

Schematic design

The schematic design is shown below

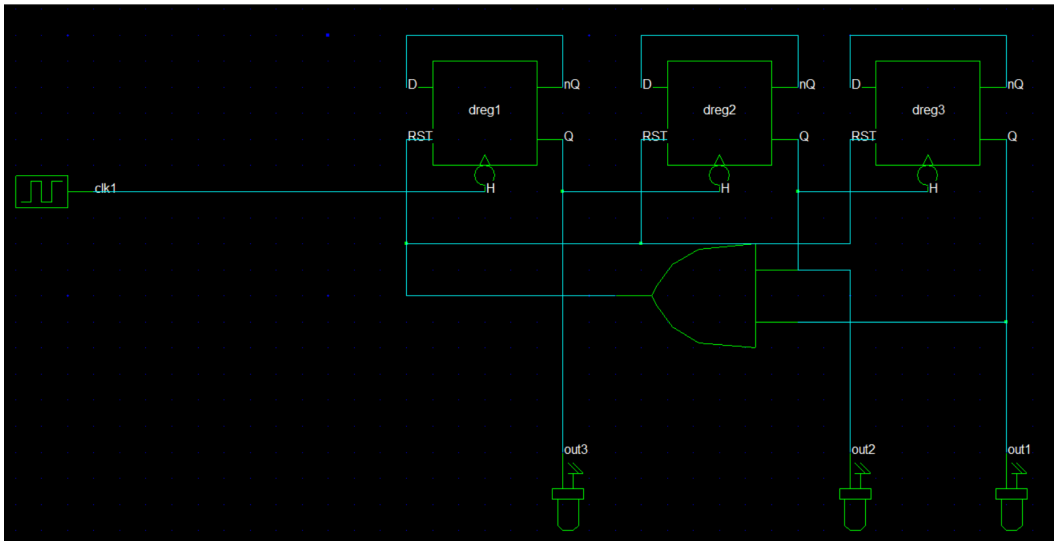

Figure 7: Schematic design for a mod 6 counter

Verilog Code

```
    module counter ( clk ,reset ,dout, enable );

        output reg [2:0] dout ;

        input wire clk ;
        input wire reset ;
        input wire enable;

        initial dout = 0;

        always @ (posedge (clk)) begin
            if (reset)
                dout <= 0;
            else if (dout<5 && enable ==1)
                dout <= dout + 1;
            else
                dout <= 0;
        end
endmodule
```

Testbench

```
    module counter_tb();
    reg clk;
    reg reset;
    wire[2:0] out;
    reg enable;
    counter c1(.clk(clk),.reset(reset),.dout(out),.enable(enable));
    always #10 clk = ~clk;
    initial begin
        enable = 0;
        #50 ; enable  = 1;
        {clk,reset}<=0;
    end
endmodule
```

Output waveform

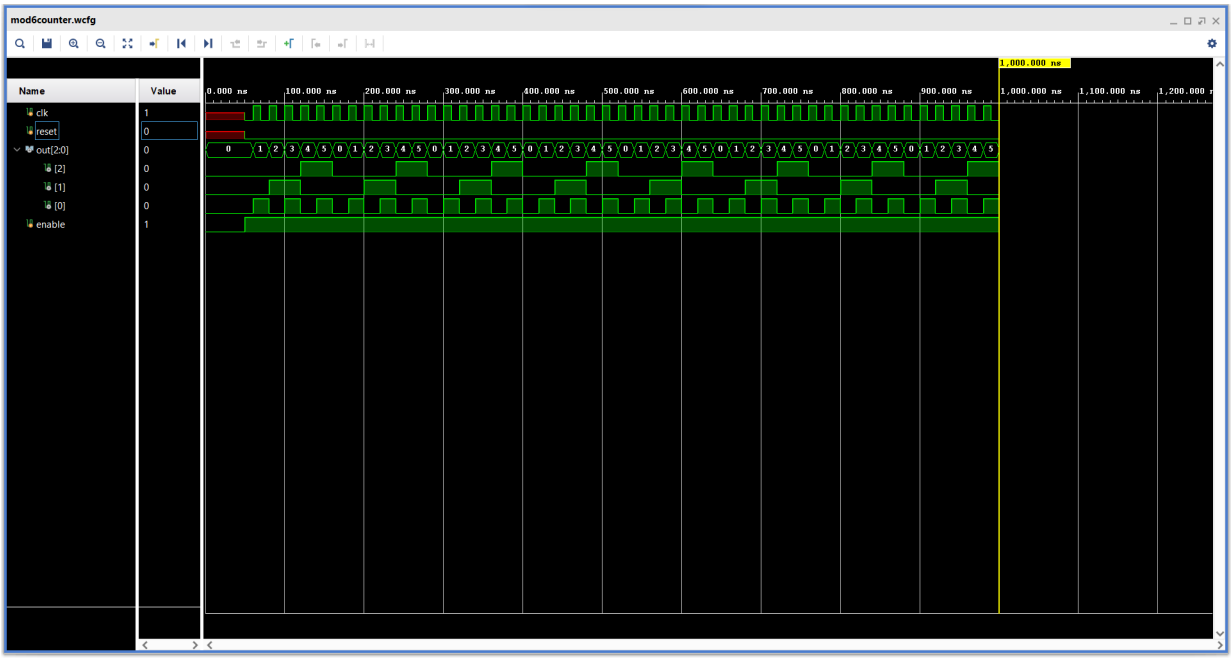

Figure 8: Output waveform of the counter