ADVD
Assignment 2
EEE F313

Problem set 14

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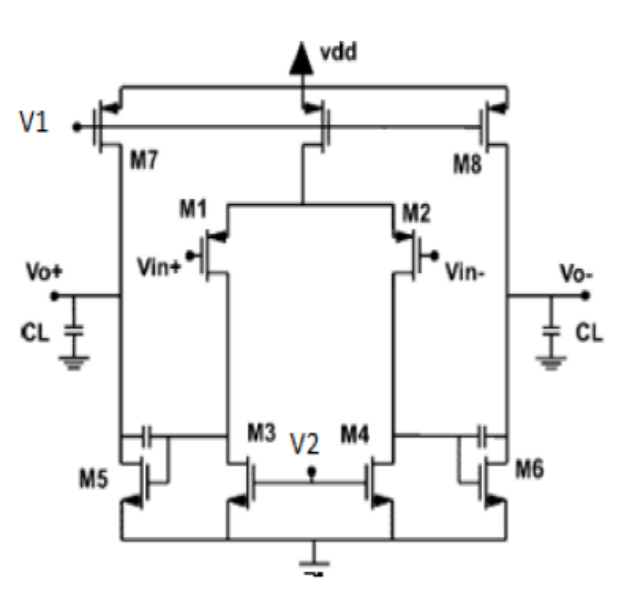
1 Problem statement

Design a two stage CMOS OPAMP as shown in the figure



(a) Analysis of all equations of your design, with a systematic derivation of all transistors W/L ratios and spectre simulation of circuit for the following specifications:

(i) Open loop gain (DC gain) $\geq$ 110dB

(ii) Phase margin $\approx 60^\circ$

(iii) Power dissipation $\leq$ 1mW

(b) Show a biasing circuitry to bias all the voltages in your design (except the input)

(c) Calculate and plot the following parameters for your OPAMP: DC gain, Bode plot for AC gain and phase, ICMR plot, slew rate, Differential Output voltage swing (dc+transient), power consumption, and input and output offset voltage.

2 Design

2.1 Circuit diagram

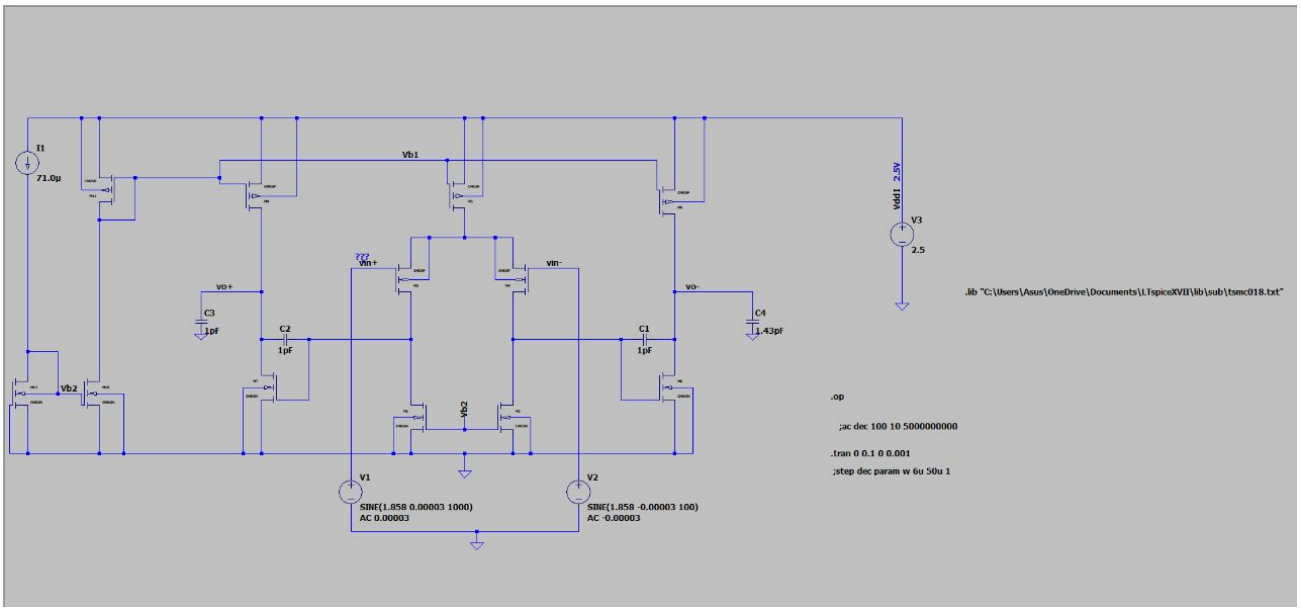


Figure 1: Circuit diagram

2.2 W/L calculations

- Current will be same in all the branches of the circuit. Approximate value of $|V_{DS}|$ was calculated accordingly.
- PMOS overdrive was set at 0.36V and NMOS overdrive at 0.3V because of the lesser mobility of PMOS, which hence needs a higher overdrive voltage.
- To obtain W/L of all the MOSFETs:
  - The MOSFETs were taken to a separate SPICE file.
  - Since the L value is constant, the value for W was found by parametrically sweeping accordingly to match requirements

2.2.1 W/L table

MOSFET	W	W/L
M1 & M2	5.6 μ	16
M3 & M4	5.6 μ	99
M5	65.8 μ	188
M6 & M7 & M10 & M12	2.8 μ	8
M8 &M9	56 μ	160
M11	16.55 μ	47

Table 1: Table for W/L values

3 Plots and results

3.1 Bode plot for AC gain and phase

Figure 2: AC gain at

UGB from the given circuit is 218.776 MHz.
With the current circuitry and number of stages the maximum gain we are able to achieve is 66.48dB at 27 °C. The gain can be increased by adding more stages at the expense of power consumption.

3.2 ICMR plot

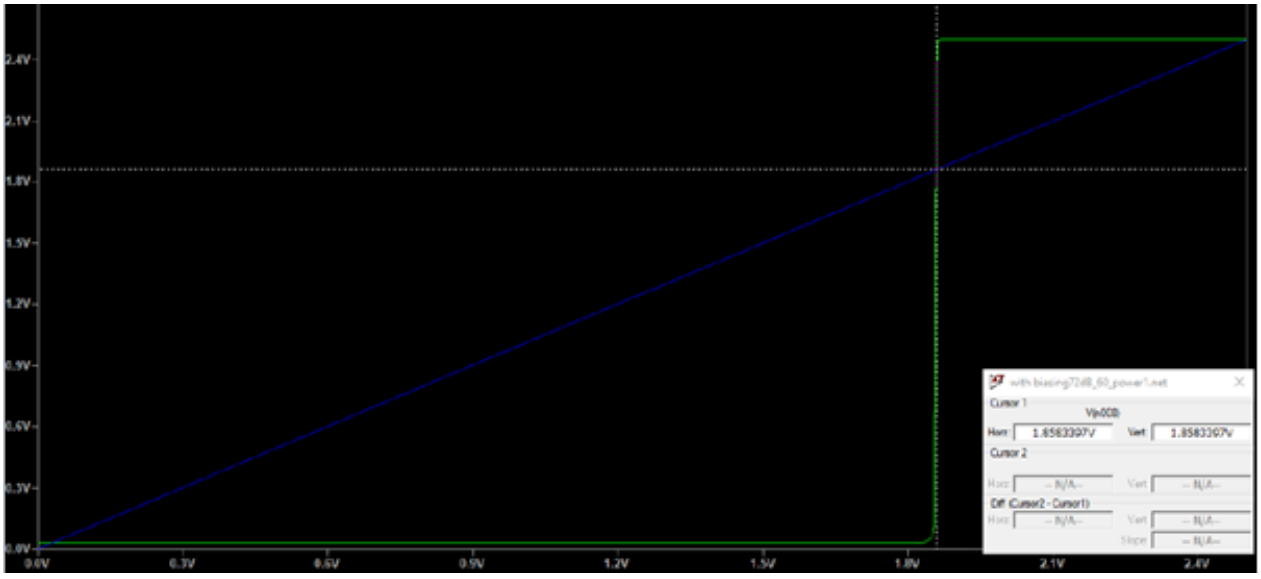


Figure 3: ICMR plot

3.3 Slew rate

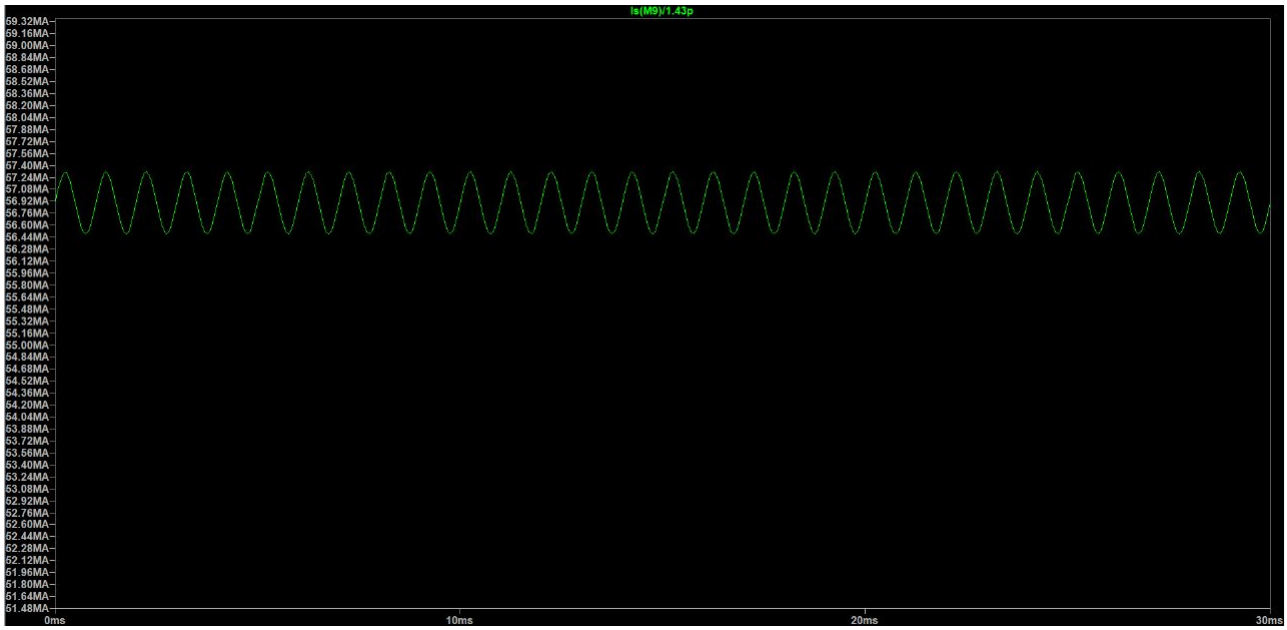


Figure 4: Slew rate

3.4 Differential output voltage swing

Figure 5: Differential output voltage swing

3.5 Power consumption

Power consumed by the circuit is given by the product: Total current drawn $\times$ V_{dd}
From the circuit simulated by LTSpice, we have the total current drawn as $I_{tot} = 329.4\mu A$ and $V_{dd} = 2.5V$.
Hence the total power consumption: $I_{tot} \times V_{dd} = 329.24\mu A \times 2.5V = 0.8321mW \leq 1mW$

3.6 Input and output offset voltage

The input is an AC voltage of 30 μ sinusoid with a frequency of 1kHz. The DC offset voltage given is 1.858V.

3.6.1 Input offset voltage

The input offset voltage is negligible due to the circuit being systematic at the input nodes

3.6.2 Output offset voltage

Output offset voltage(V_{oo}) is defined as follows: Output voltage of the op-amp when both inputs are 0. V_{oo} is due to dissimilarities in the transistors and due to mismatch in resistor values in the internal circuitry in the op-amp. For this particular calculation, input was set as 0 and transient analysis was performed, which gives us the graph below for small time periods. For larger time periods, a steep fall was observed

The output offset voltage is determined to be 38.089 mV.

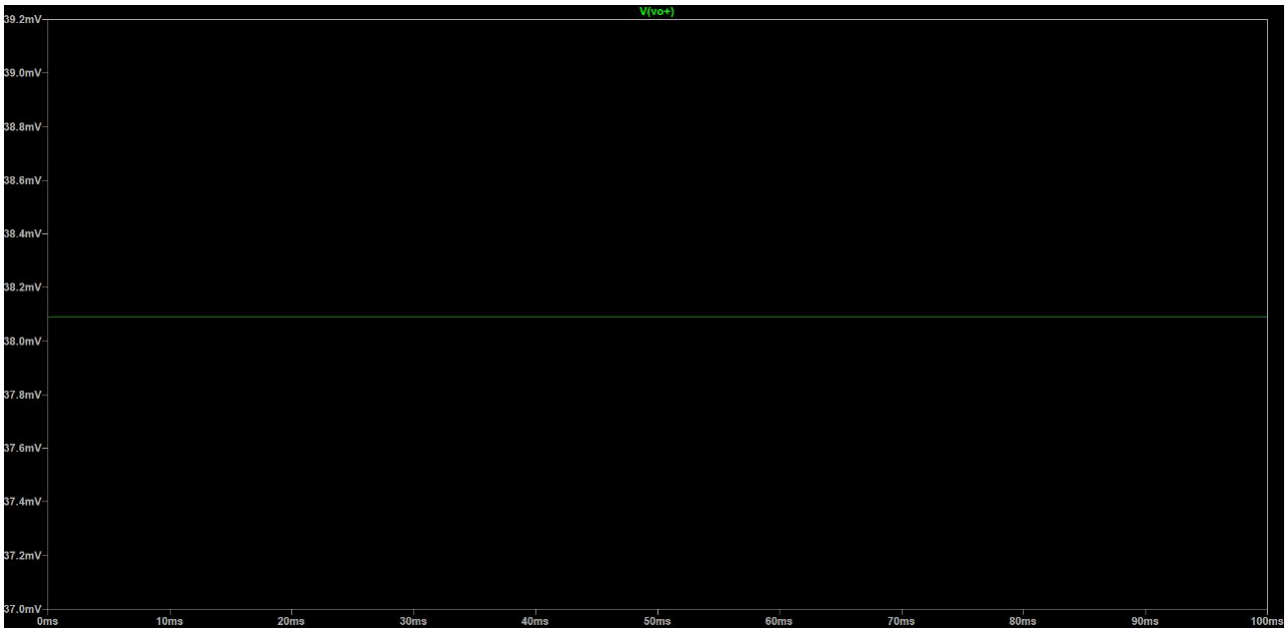


Figure 6: Output offset voltage

4 Design Challenges

1. It was very tedious to match the W/L values from both hand calculations and SPICE simulations. Trial and error was used to eventually reach an optimal value of W/L for each transistor.

2. Obtaining parameters for a 2-stage op-amp was very tricky because of various factors like intermediate poles and separate biasing voltages of all stages

3. No option of a pole and zero plot is available in LTSpice. Individual bode plots had to be used.