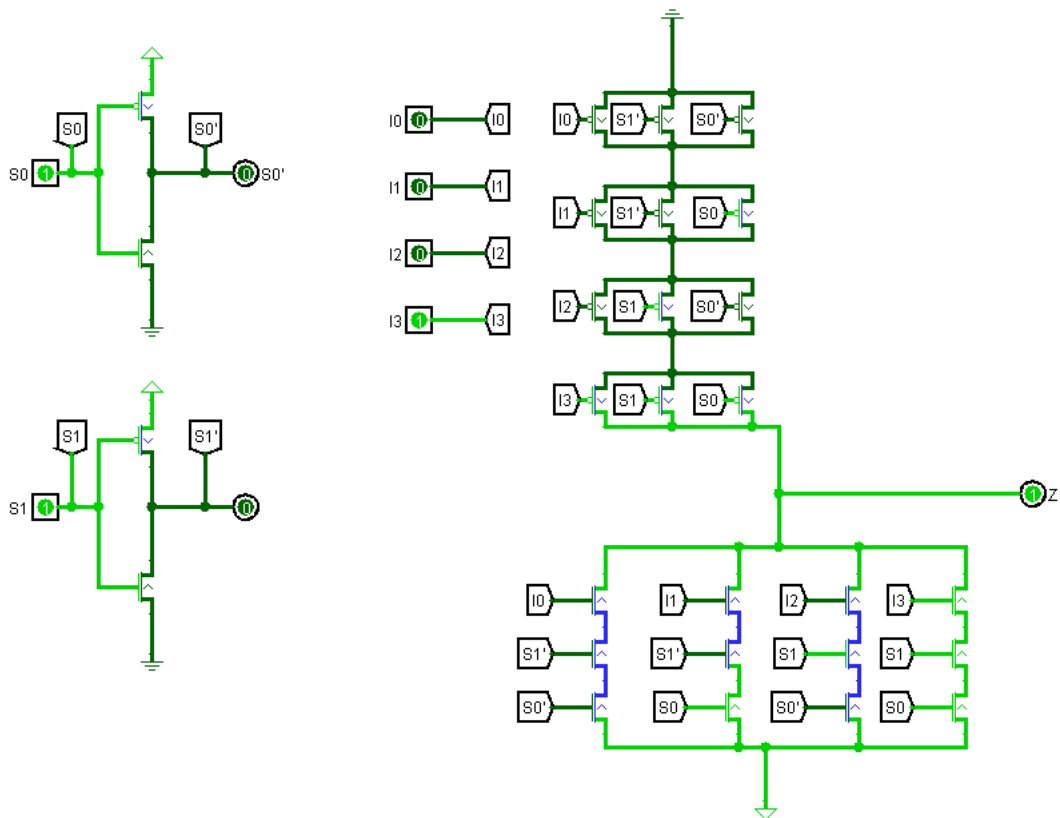


DD Lab 6 Assignment

Sai Kartik
2020A3PS0435P

October 16, 2021

1 4:1 Mux using CMOS logic



2 4:1 Mux using TG and NOT gates

