DD Lab 4 Assignment

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7 Segment display

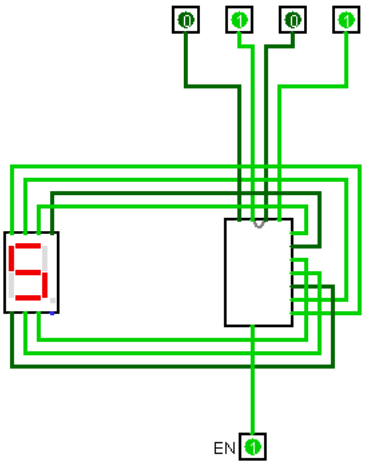
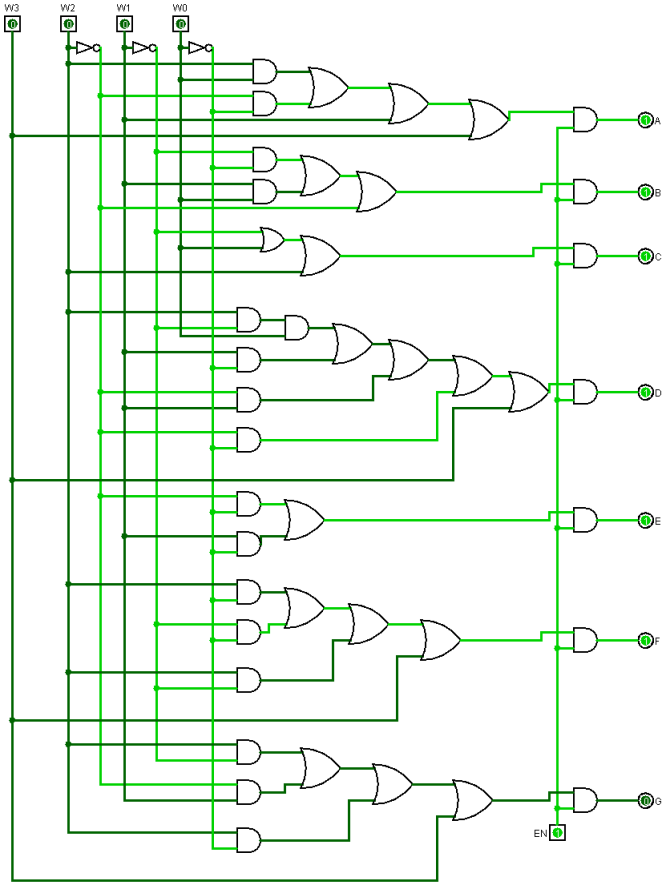


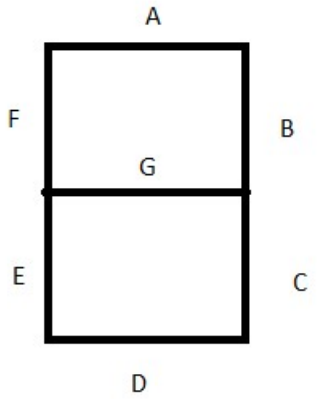
Figure 1: The seven segment display

Decoder circuit



Truth Table used to design the decoder

The convention used for the 7 segment display labelling:



Truth table:

W_3	W_2	W_1	W_0	A	B	C	D	E	F	G
0	0	0	0	1	1	1	1	1	1	0
0	0	0	1	0	1	1	0	0	0	0
0	0	1	0	1	1	0	1	1	0	1
0	0	1	1	1	1	1	1	0	0	1
0	1	0	0	0	1	1	0	0	1	1
0	1	0	1	1	0	1	1	0	1	1
0	1	1	0	1	0	1	1	1	1	1
0	1	1	1	1	1	1	0	0	0	0
1	0	0	0	1	1	1	1	1	1	1
1	0	0	1	1	1	1	1	0	1	1

The expressions realised from the above truth table:

$$
\begin{aligned}
A &= W_3 + W_1 + W_2W_0 + \bar{W}_2\bar{W}_0 \\
B &= \bar{W}_2 + \bar{W}_1\bar{W}_0 + W_1W_0 \\
C &= \bar{W}_1 + W_0 + W_2 \\
D &= W_3 + \bar{W}_2\bar{W}_0 + \bar{W}_2W_1 + W_1\bar{W}_0 + W_2\bar{W}_1W_0 \\
E &= \bar{W}_2\bar{W}_0 + W_1\bar{W}_0 \\
F &= W_3 + W_2\bar{W}_1 + \bar{W}_1\bar{W}_0 + W_1\bar{W}_0 \\
G &= W_3 + W_2\bar{W}_0 + \bar{W}_2W_1 + W_2\bar{W}_1
\end{aligned}
$$