

DD Lab 1 Assignment

Sai Kartik
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Canonical SOP form

Given Equation: $\bar{A} \cdot (B + \bar{C}) + D$

Canonical SOP Form:

$$ABCD + \bar{A}BCD + A\bar{B}CD + AB\bar{C}D + \bar{A}\bar{B}CD + \bar{A}B\bar{C}D + \bar{A}BC\bar{D} \\ + A\bar{B}\bar{C}D + \bar{A}B\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}D + \bar{A}\bar{B}\bar{C}\bar{D}$$

Truth table

(Same obtained for both realisations of the circuit)

a	b	c	d	x
0	0	0	0	1
0	0	0	1	1
0	0	1	0	0
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	0
1	1	1	1	1

Simple gates realisation

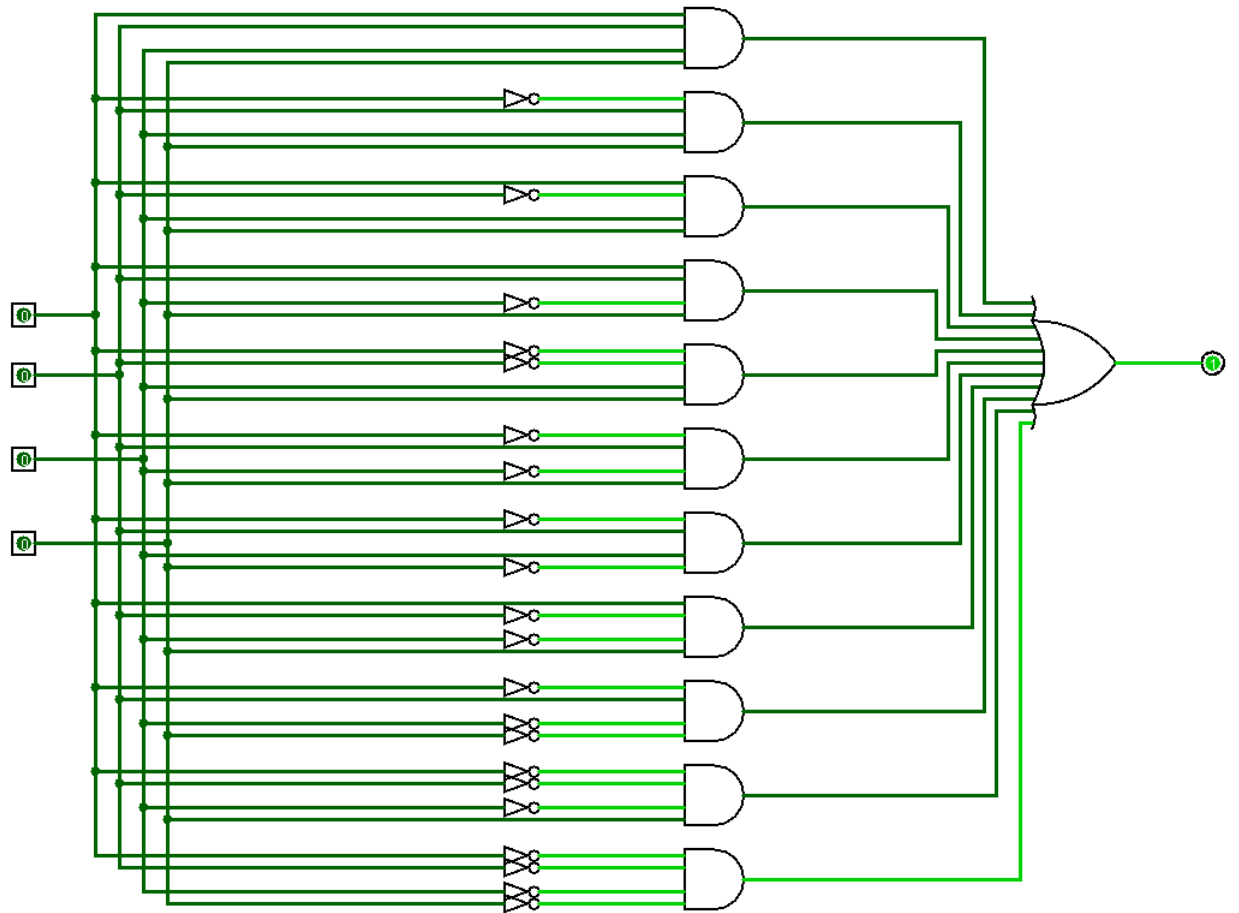


Figure 1: Basic gates realisation of SOP form

NAND Gate realisation

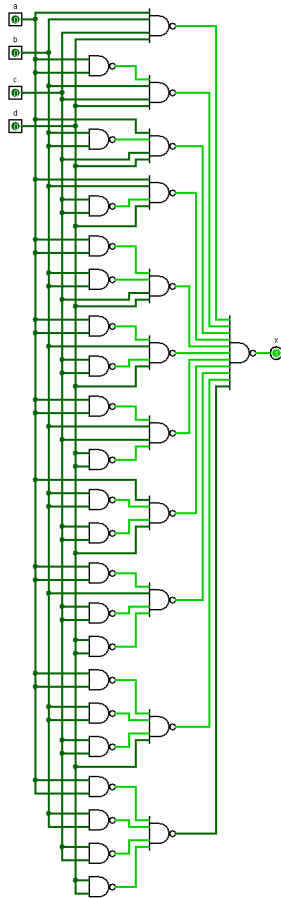


Figure 2: NAND Gate realisation of SOP form

Expression for NAND gate realisation

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a b c d a a b c d a b b c d a b c c d a a b b c d a a b c c d d a b b c c d a a b c c d d a a b b c c d a a b b c c d d

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Canonical POS form

Given Equation: $\bar{A} \cdot (B + \bar{C}) + D$

Canonical POS form:

$$(A+B+\bar{C}+D) \cdot (\bar{A}+B+C+D) \cdot (\bar{A}+B+\bar{C}+D) \cdot (\bar{A}+\bar{B}+C+D) \cdot (\bar{A}+\bar{B}+\bar{C}+D)$$

Truth table

(Same obtained for both realisations of the circuit)

a	b	c	d	x
0	0	0	0	1
0	0	0	1	1
0	0	1	0	0
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	0
1	1	1	1	1

Simple gates realisation

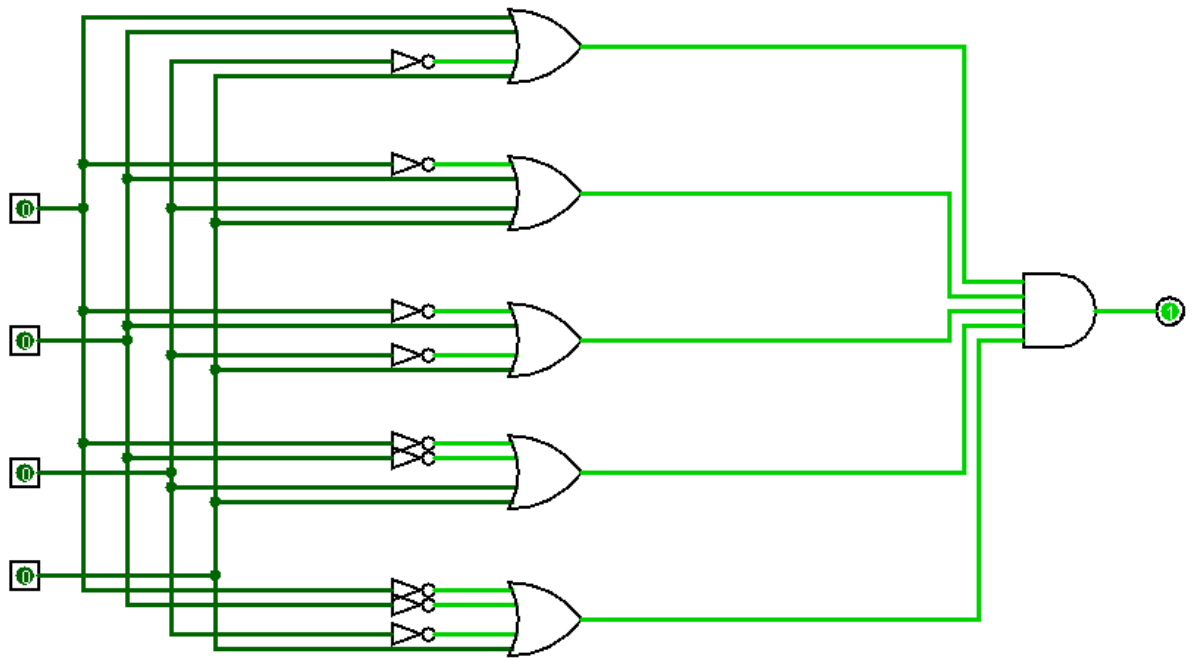


Figure 3: Basic gates realisation of POS form

NOR Gate realisation

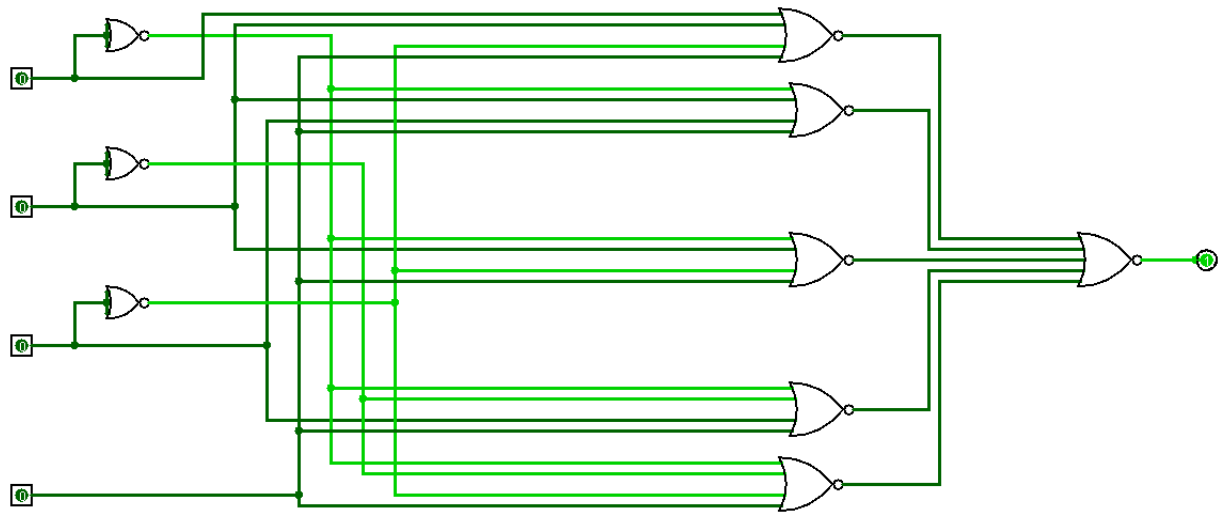


Figure 4: NOR Gate realisation of POS form

Expression for NOR gate realisation

$$\overline{a+b+c+d+a+a+b+c+d+a+a+b+c+c+d+a+a+b+b+c+d+a+a+b+b+c+c+d}$$