DD Lab 2 Assignment

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1 Realisation with multi-input NAND gates

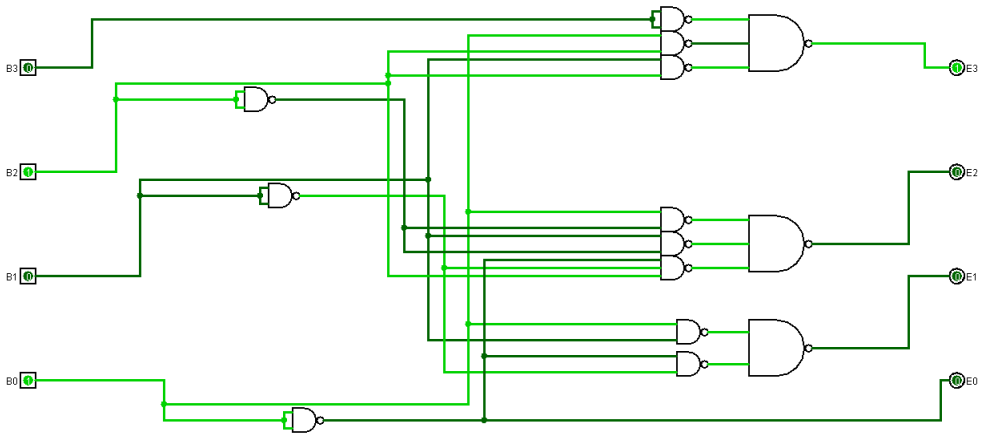

Figure 1: BCD to Excess 3 converter realised with only NAND gates (multiple-input gates)

1.1 Truth Table generated

B3	B2	B1	B0	E3	E2	E1	E0
0	0	0	0	0	0	1	1
0	0	0	1	0	1	0	0
0	0	1	0	0	1	0	1
0	0	1	1	0	1	1	0
0	1	0	0	0	1	1	1
0	1	0	1	1	0	0	0
0	1	1	0	1	0	0	1
0	1	1	1	1	0	1	0
1	0	0	0	1	0	1	1
1	0	0	1	1	1	0	0
1	0	1	0	1	1	0	1
1	0	1	1	1	1	1	0
1	1	0	0	1	1	1	1
1	1	0	1	1	0	0	0
1	1	1	0	1	0	0	1
1	1	1	1	1	0	1	0

Figure 2: Truth table for the above realisation

1.2 Simplified expressions for this realisation

$$E_0 = \bar{B}_0$$

$$E_1 = B_0 B_1 + \bar{B}_0 \bar{B}_1$$

$$E_2 = B_0 \bar{B}_2 + B_1 \bar{B}_2 + \bar{B}_0 \bar{B}_1 B_2$$

$$E_3 = B_3 + B_0 B_2 + B_1 B_2$$

2 Realisation with only 2-input NAND gates

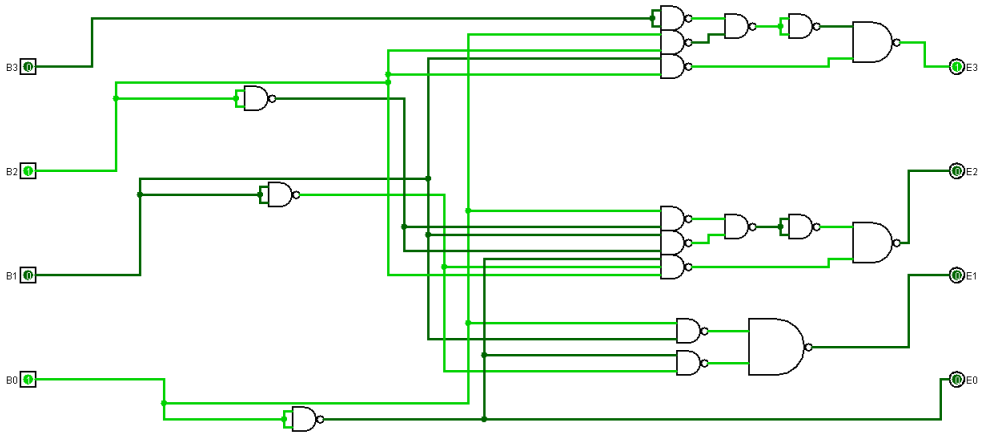

Figure 3: BCD to Excess 3 converter realised with only NAND gates (only 2-input gates)

2.1 Truth Table generated

B3	B2	B1	B0	E3	E2	E1	E0
0	0	0	0	0	0	1	1
0	0	0	1	0	1	0	0
0	0	1	0	0	1	0	1
0	0	1	1	0	1	1	0
0	1	0	0	0	1	1	1
0	1	0	1	1	0	0	0
0	1	1	0	1	0	0	1
0	1	1	1	1	0	1	0
1	0	0	0	1	0	1	1
1	0	0	1	1	1	0	0
1	0	1	0	1	1	0	1
1	0	1	1	1	1	1	0
1	1	0	0	1	1	1	1
1	1	0	1	1	0	0	0
1	1	1	0	1	0	0	1
1	1	1	1	1	0	1	0

Figure 4: Truth table for the above realisation

3 Realisation with multi-input NOR gates

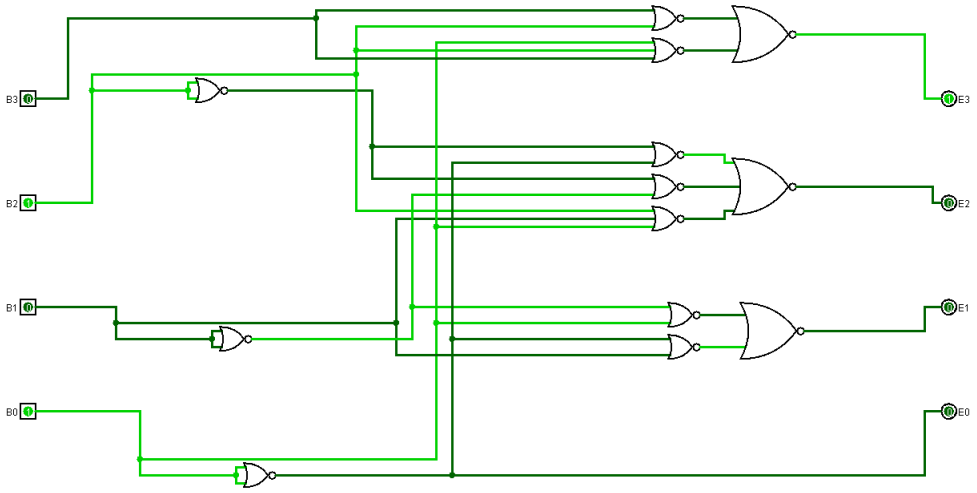

Figure 5: BCD to Excess 3 converter realised with only NOR gates (multiple-input gates)

3.1 Truth Table generated

B3	B2	B1	B0	E3	E2	E1	E0
0	0	0	0	0	0	1	1
0	0	0	1	0	1	0	0
0	0	1	0	0	1	0	1
0	0	1	1	0	1	1	0
0	1	0	0	1	1	1	1
0	1	0	1	1	0	0	0
0	1	1	0	1	0	0	1
0	1	1	1	1	0	1	0
1	0	0	0	1	0	1	1
1	0	0	1	1	1	0	0
1	0	1	0	1	1	0	1
1	0	1	1	1	1	1	0
1	1	0	0	1	1	1	1
1	1	0	1	1	0	0	0
1	1	1	0	1	0	0	1
1	1	1	1	1	0	1	0

Figure 6: Truth table for the above realisation

3.2 Simplified expressions for this realisation

$$E_0 = \bar{B}_0$$

$$E_1 = (\bar{B}_0 + B_1)(B_0 + \bar{B}_1)$$

$$E_2 = (\bar{B}_0 + \bar{B}_2)(\bar{B}_1 + \bar{B}_2)(B_0 + B_1 + B_2)$$

$$E_3 = (B_0 + B_1 + B_3)(B_2 + B_3)$$

4 Realisation with only 2-input NOR gates

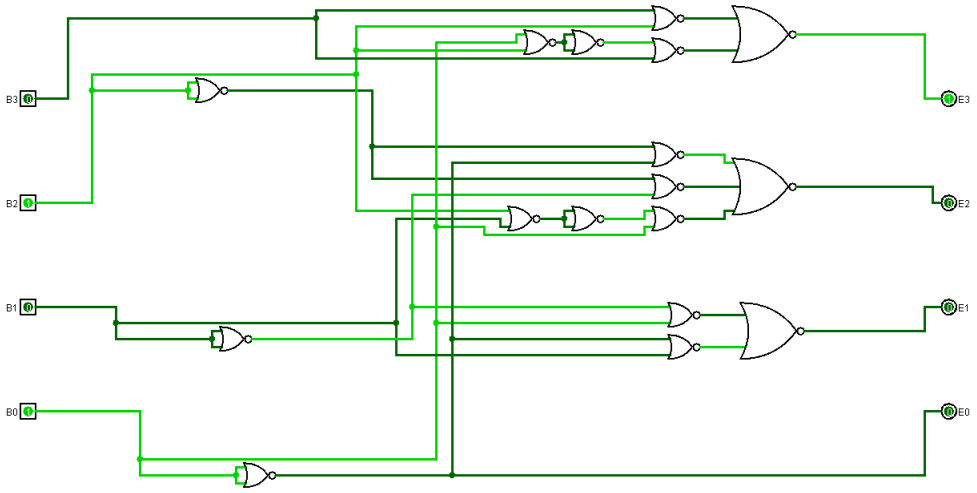

Figure 7: BCD to Excess 3 converter realised with only NOR gates (only 2-input gates)

4.1 Truth Table generated

B3	B2	B1	B0	E3	E2	E1	E0
0	0	0	0	0	0	1	1
0	0	0	1	0	1	0	0
0	0	1	0	0	1	0	1
0	0	1	1	0	1	1	0
0	1	0	0	1	1	1	1
0	1	0	1	1	0	0	0
0	1	1	0	1	0	0	1
0	1	1	1	1	0	1	0
1	0	0	0	1	0	1	1
1	0	0	1	1	1	0	0
1	0	1	0	1	1	0	1
1	0	1	1	1	1	1	0
1	1	0	0	1	1	1	1
1	1	0	1	1	0	0	0
1	1	1	0	1	0	0	1
1	1	1	1	1	0	1	0

Figure 8: Truth table for the above realisation