# DD Lab 6 Assignment

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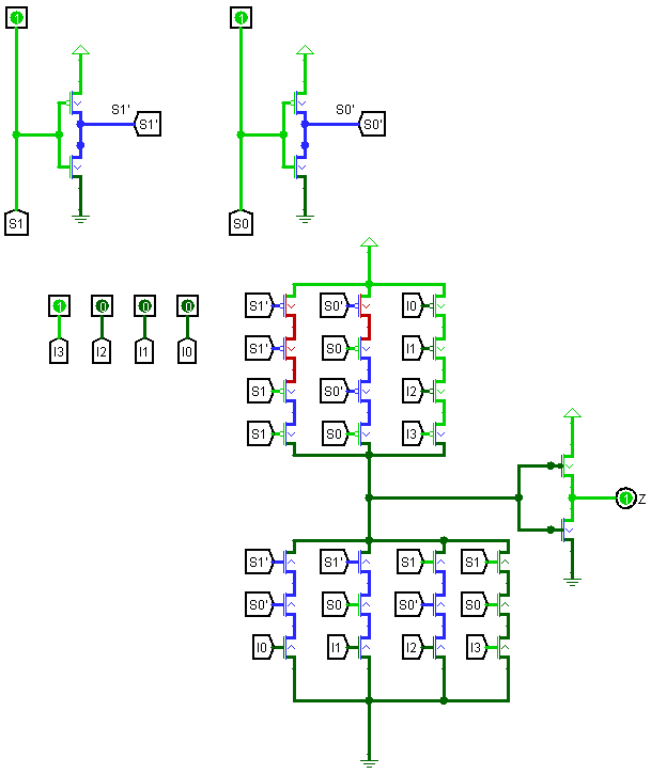
## 1 4:1 Mux using CMOS logic



## 2 4:1 Mux using TG and NOT gates