8-BIT COMPUTER

CIRCUIT DIAGRAMS

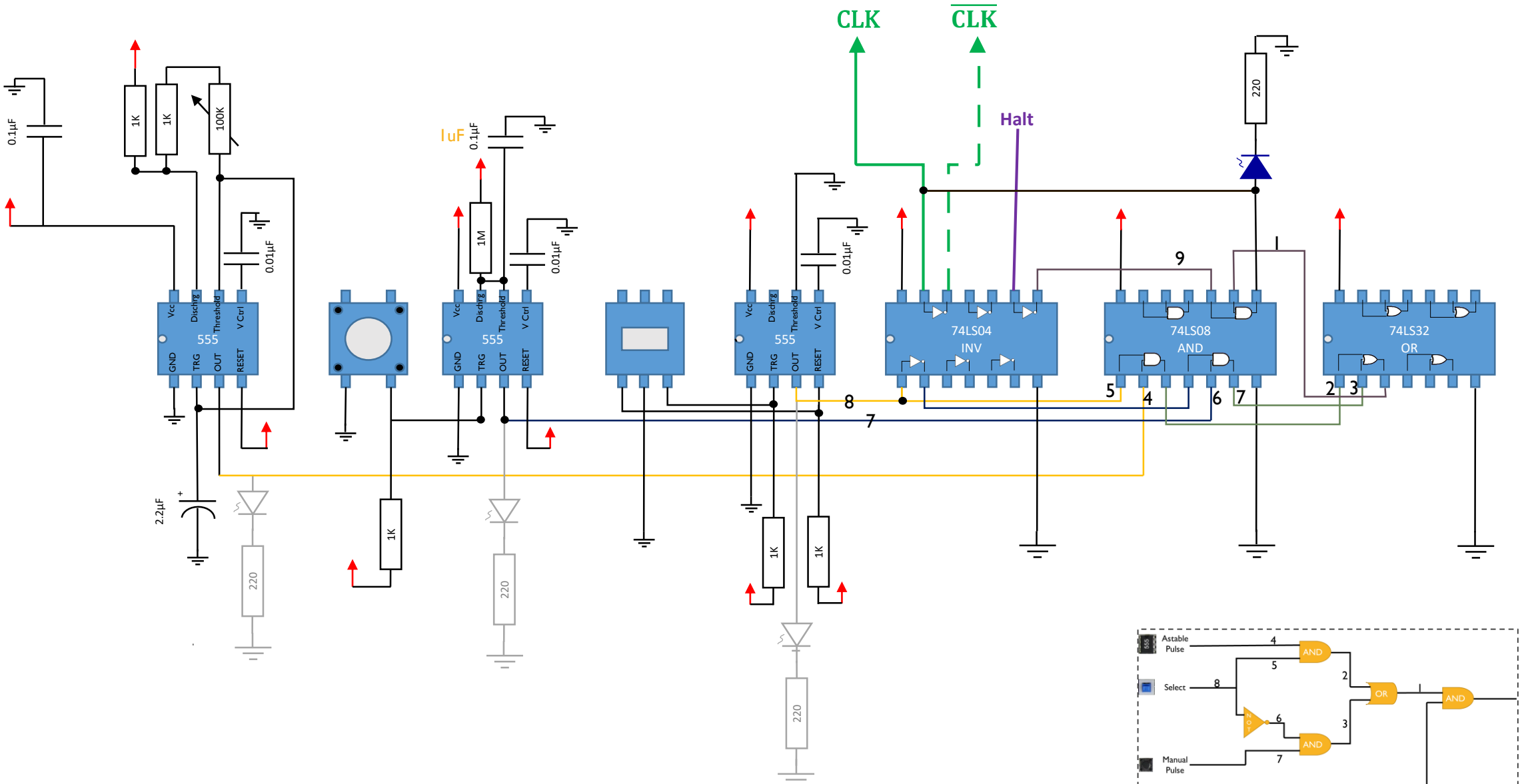
SKETCHED BY ODED

BASED ON BEN EATER'S WORK AT HTTPS://EATER.NET/

COMMENTS

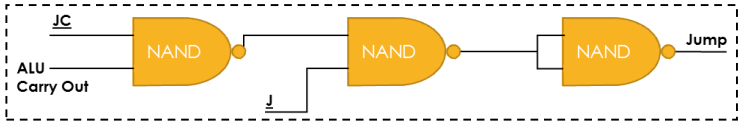
- The following diagrams are based on the great Ben Eater's videos describing the design and build of an 8-bit computer for educational purposed.
- These sketches are not official circuit schematics (which may be harder for most people to interpret) but logical breadboard views of each of the computer's components.
- Originally, I created these sketches for my personal use (to build my own version of the computer) but then decided to share them with the community after seeing so many requests on Ben's site for the schematics.
- If you find a mistake, please send me an email (oded.8bit@gmail.com) and I will make the required changes.
- You can share these sketches in any way you want.

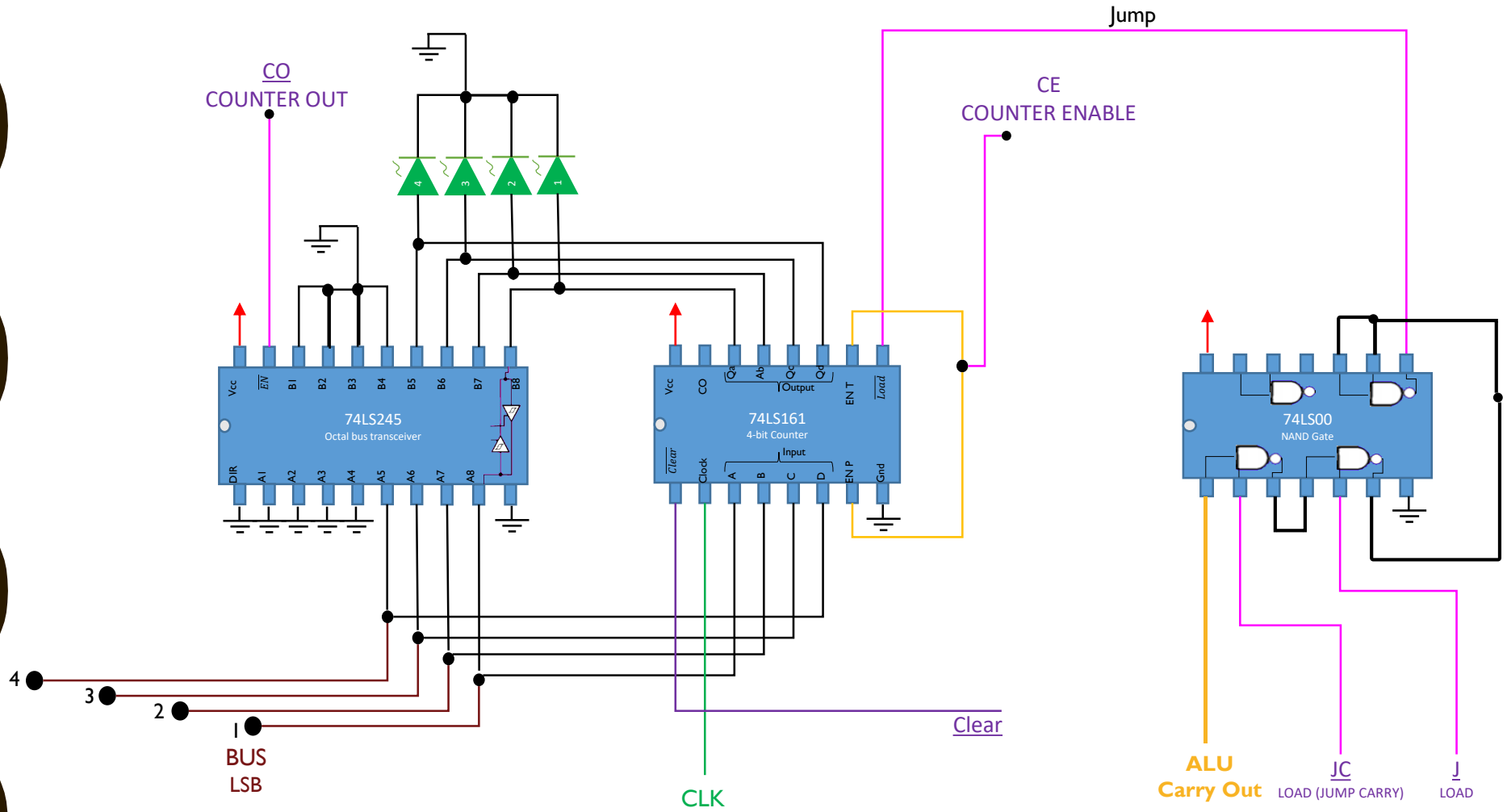
CLOCK


CLK
CLK
Halt
1K
1K
100K
0.1µF
0.01µF
1uF
0.1µF
1M
0.01µF
0.01µF
220
555
74LS04
INV
74LS08
AND
74LS32
OR
2.2µF
1K
1K
1K
220
220
220
Vcc
Discharge
Threshold
V Ctrl
GND
TRG
OUT
RESET

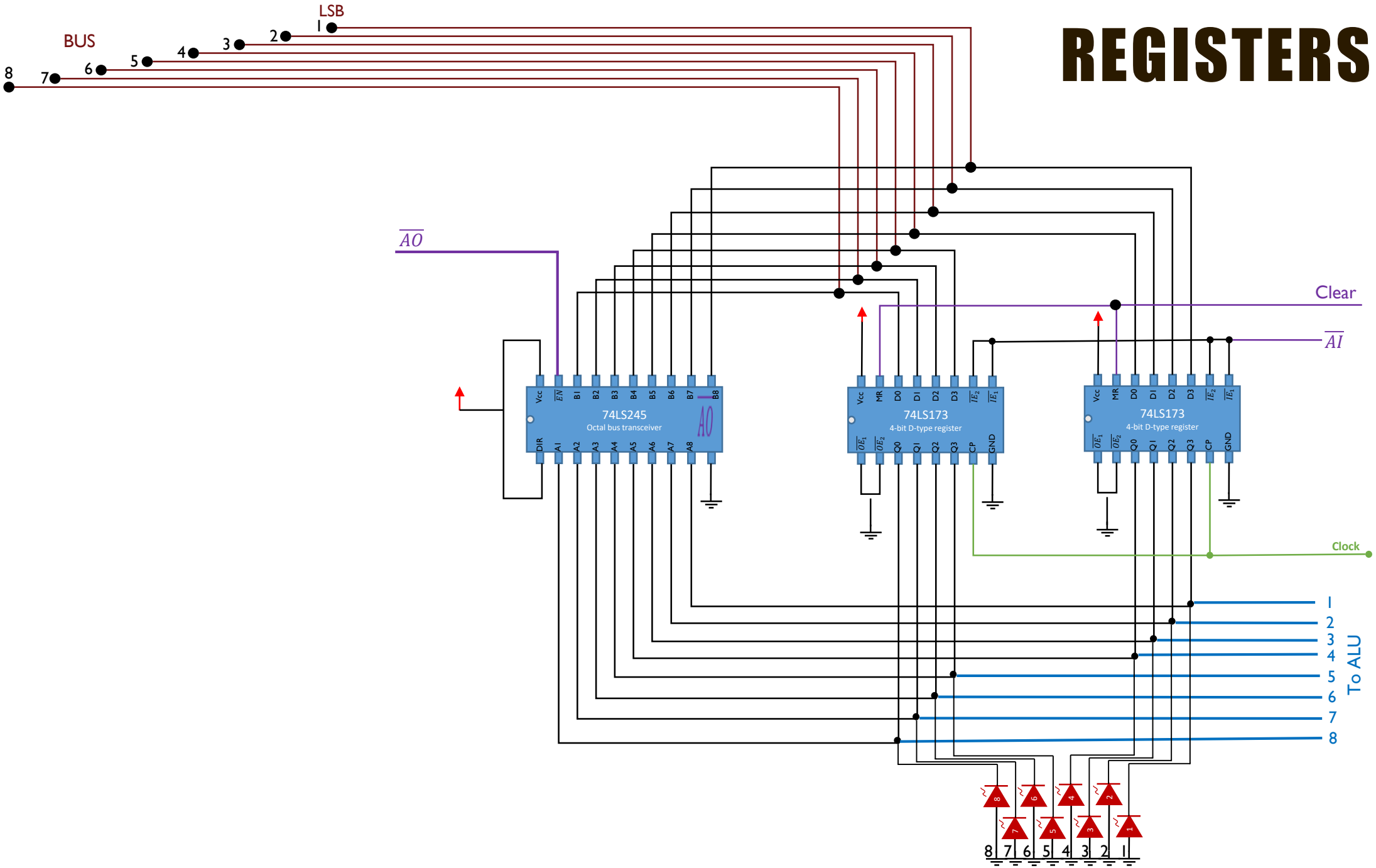
Astable Pulse
Select
Manual Pulse
HLT
AND
AND
AND
OR
NOT
NOT

PROGRAM COUNTER

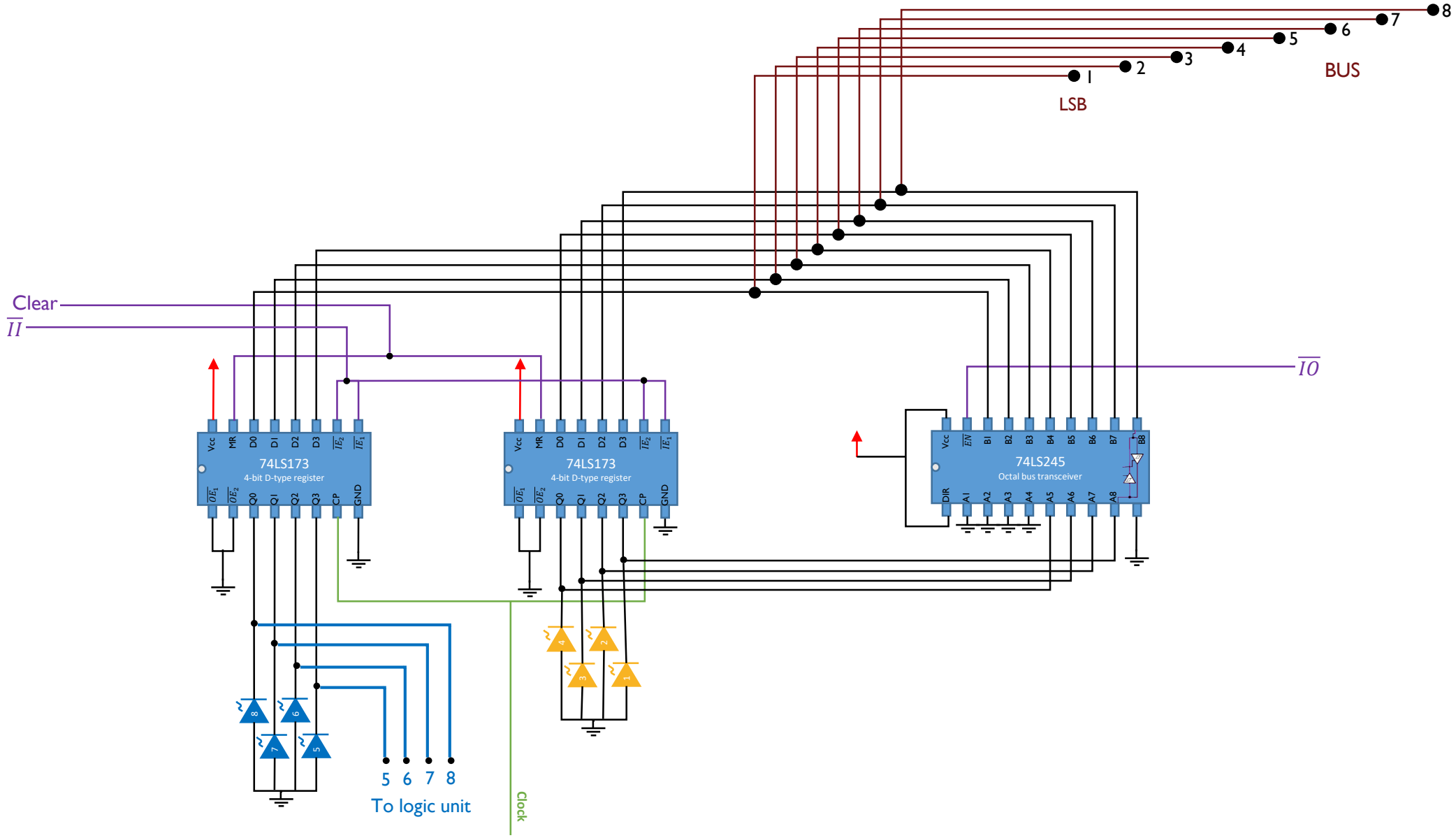




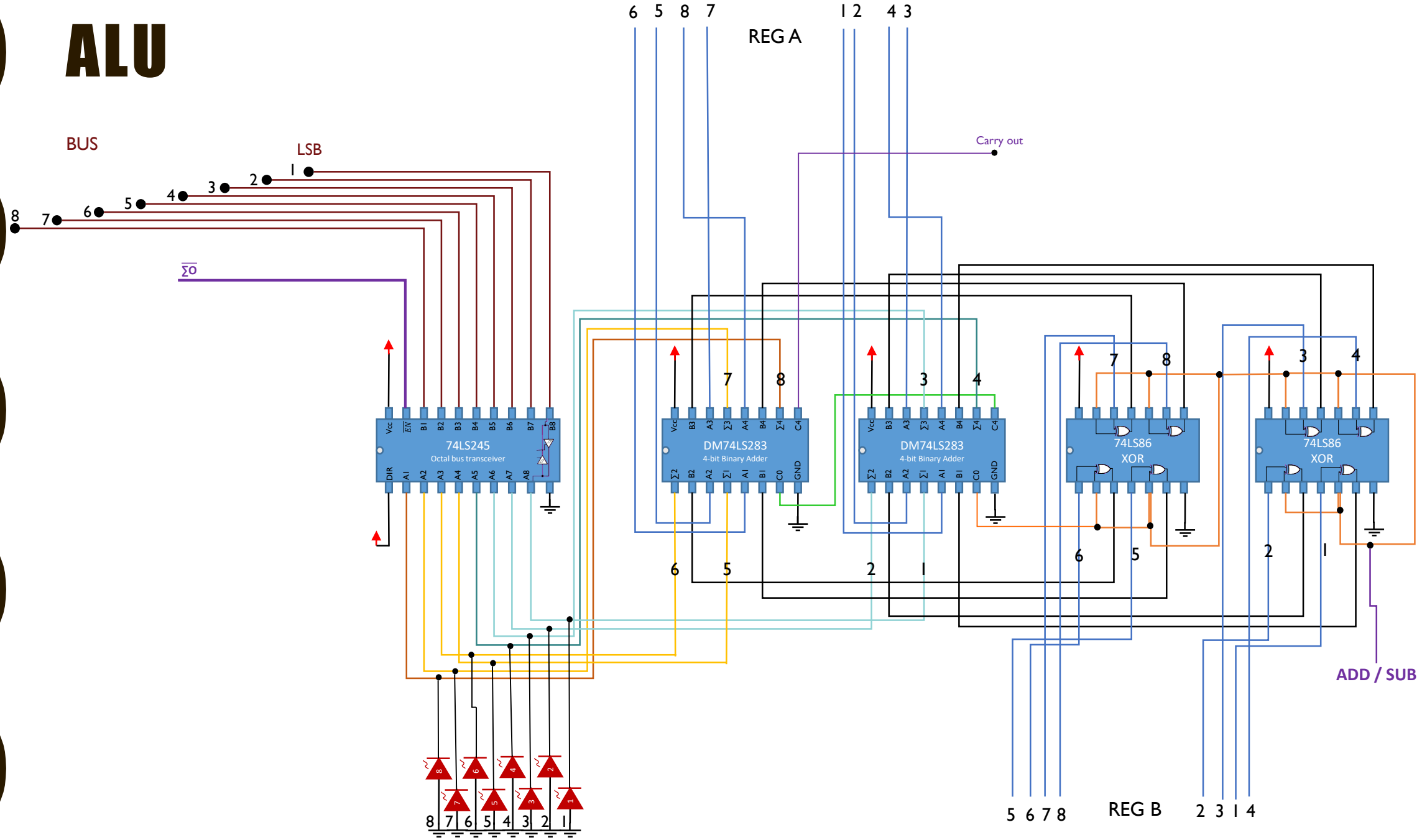
REGISTERS


LSB
BUS
1
2
3
4
5
6
7
8
$\overline{AO}$
Clear
$\overline{AI}$
74LS245
Octal bus transceiver
74LS173
4-bit D-type register
74LS173
4-bit D-type register
Clock
To ALU
1
2
3
4
5
6
7
8

INSTRUCTION REGISTER



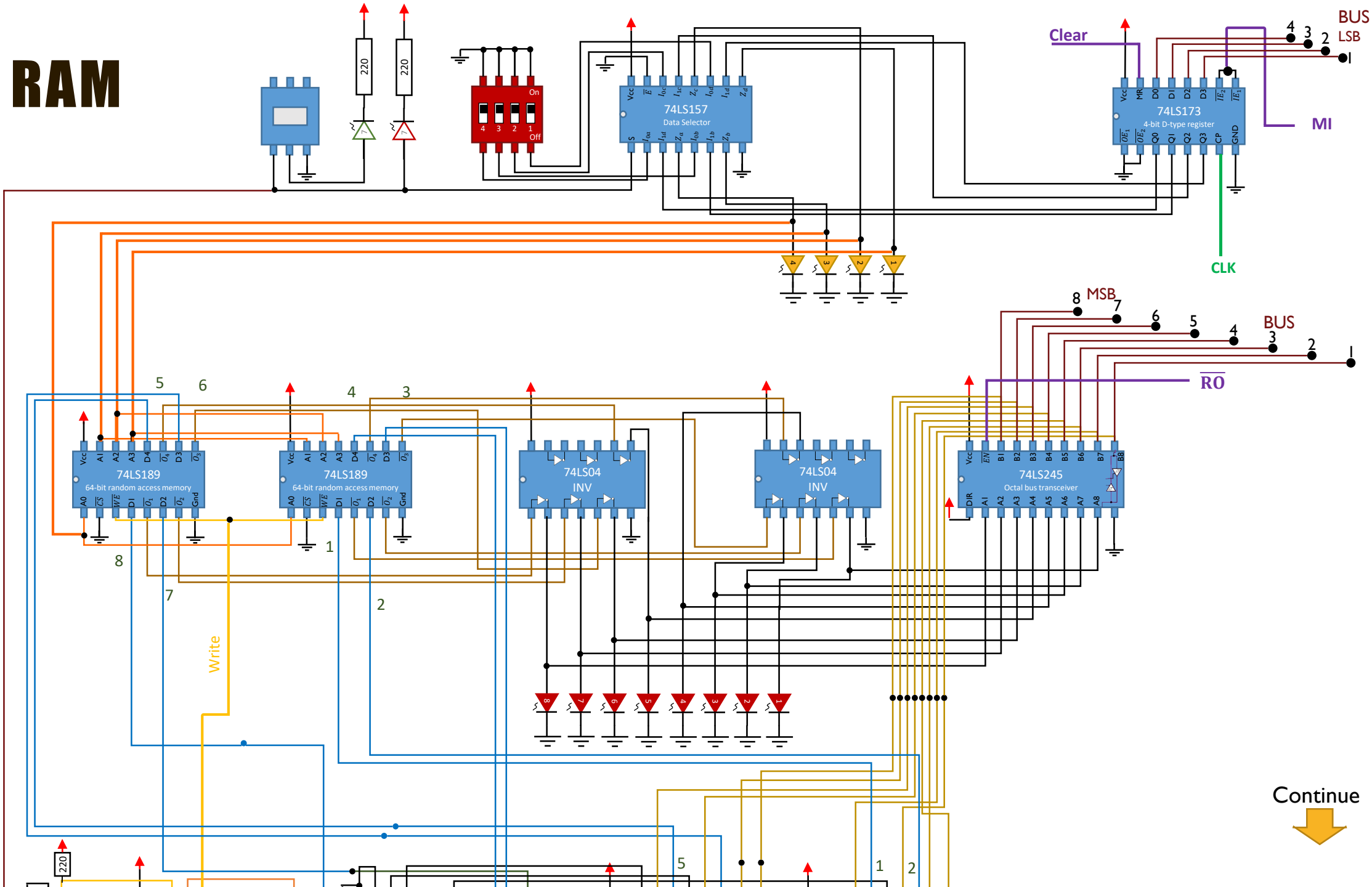
ALU


6 5 8 7
REG A
1 2 4 3
Carry out
BUS
LSB
8 7 6 5 4 3 2 1
Σ̄O
74LS245
Octal bus transceiver
DM74LS283
4-bit Binary Adder
DM74LS283
4-bit Binary Adder
74LS86
XOR
74LS86
XOR
ADD / SUB
5 6 7 8
REG B
2 3 1 4

ADDRESS REGISTER

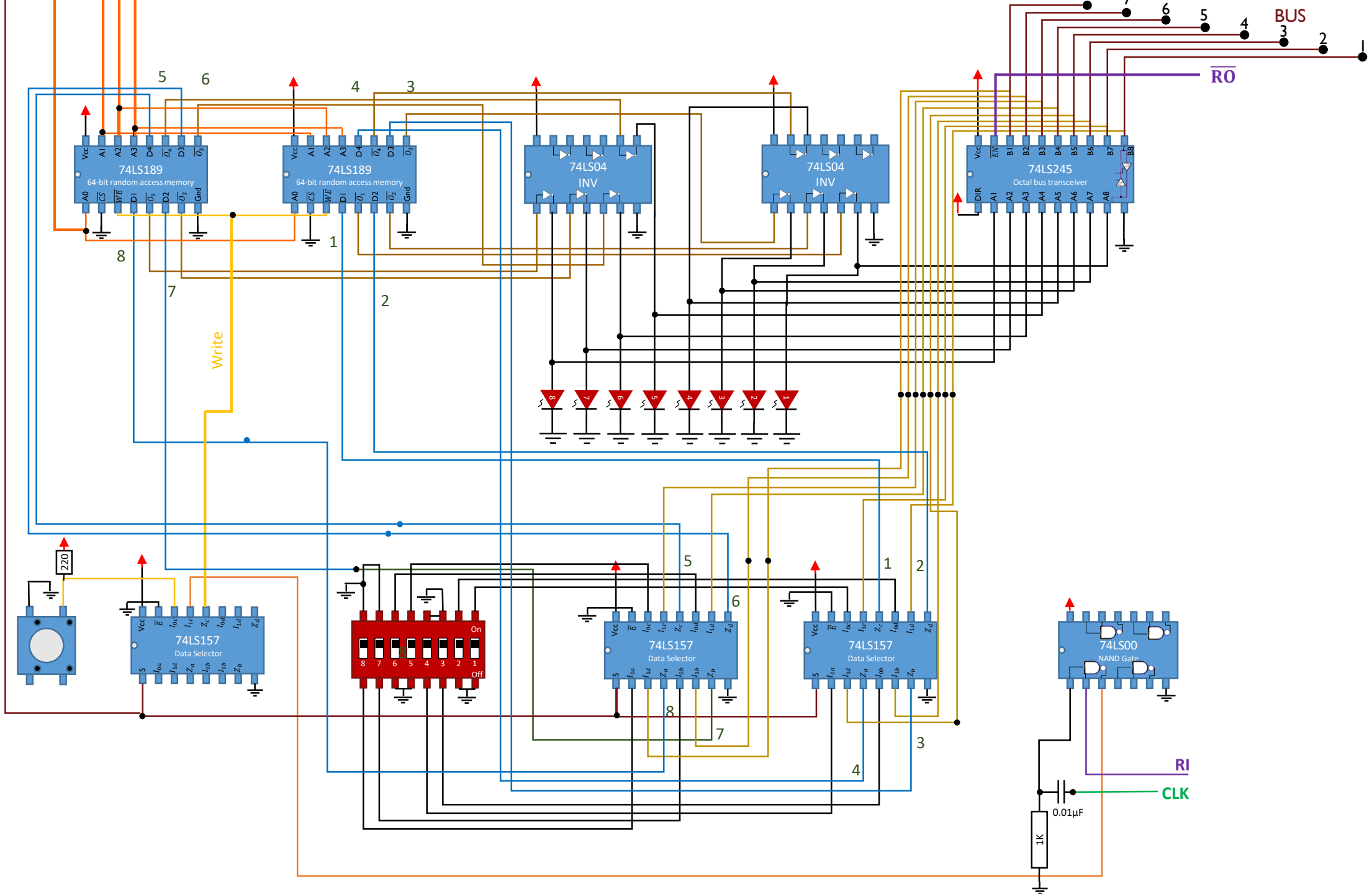
RAM

RAM

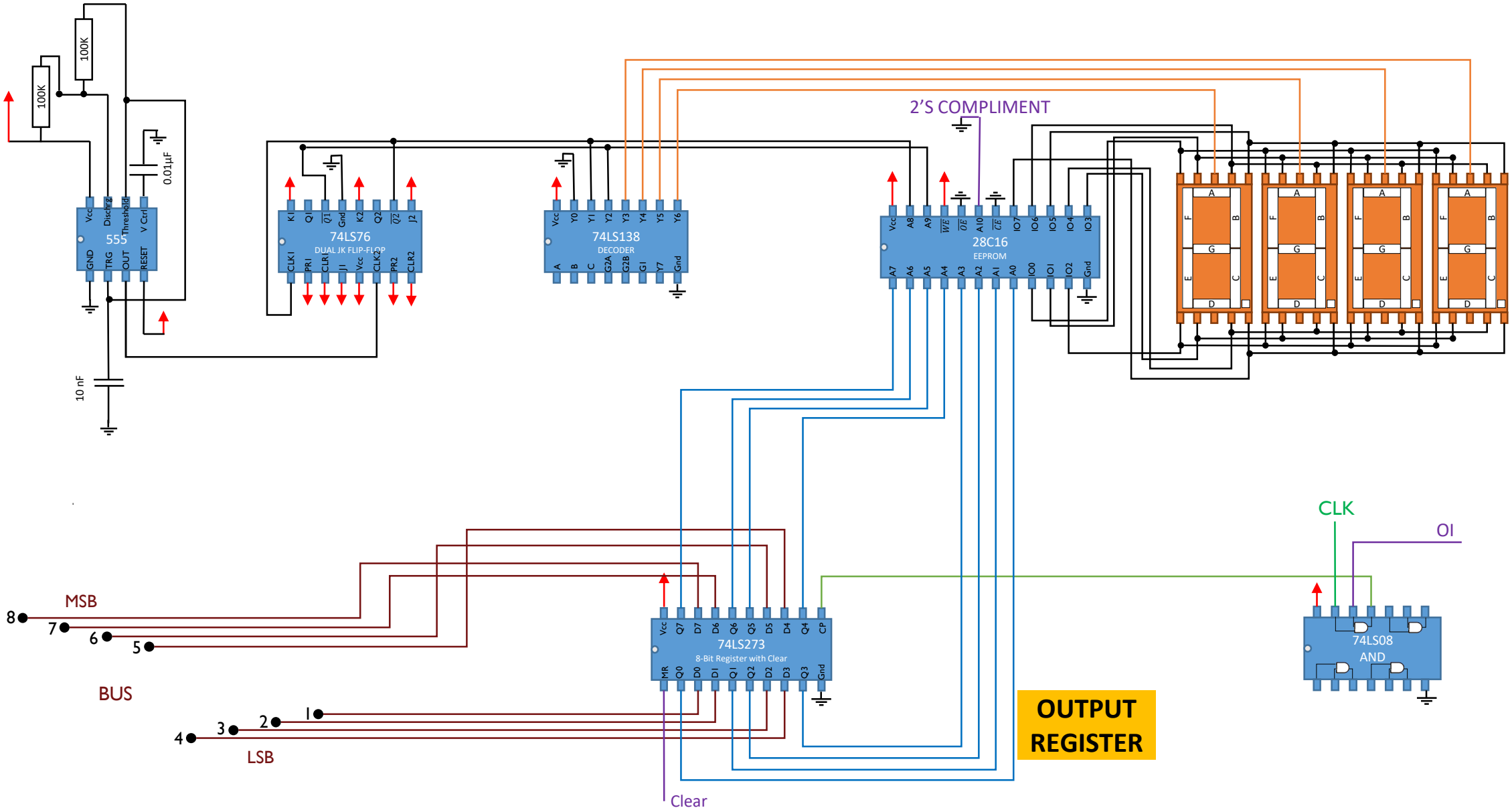


RAM

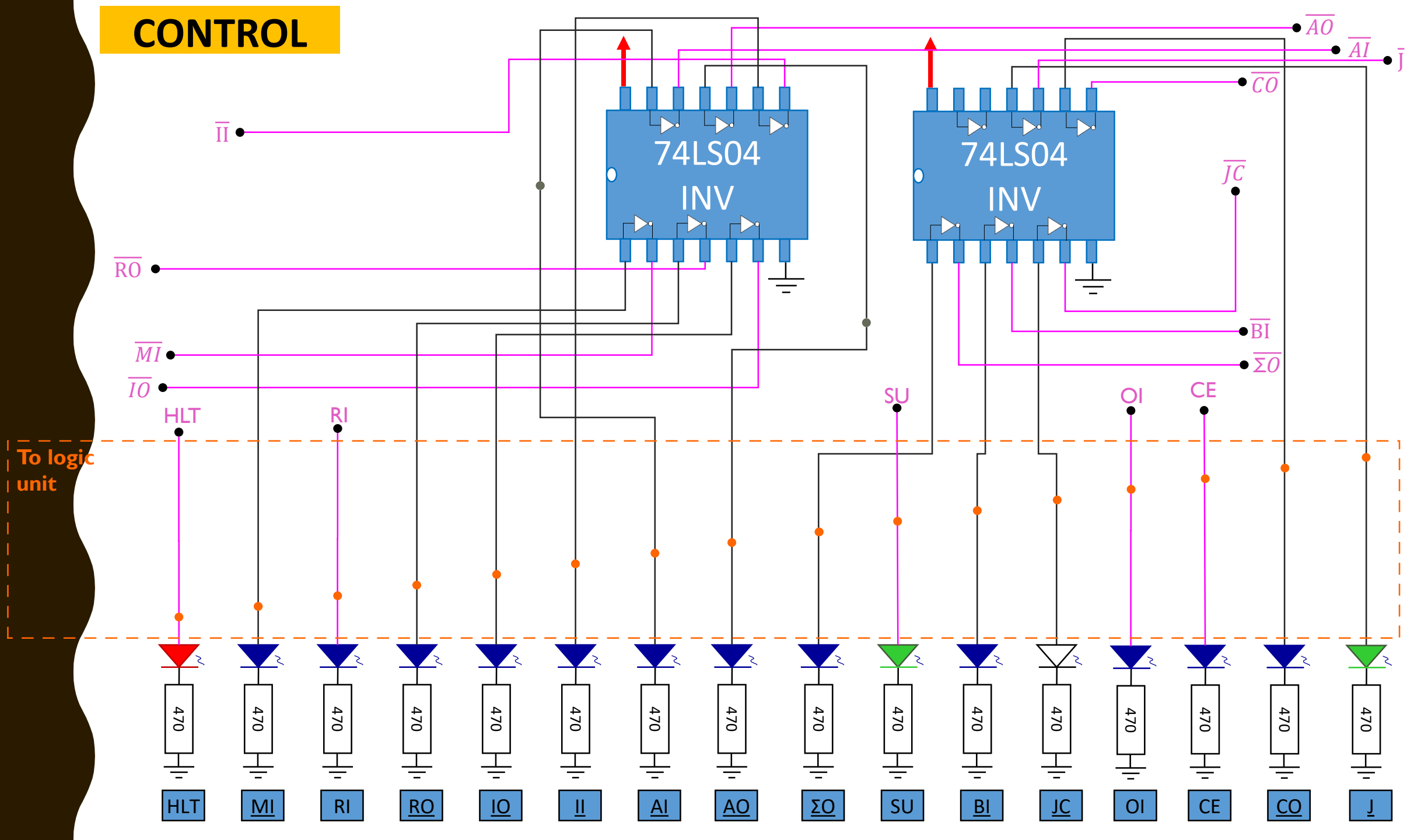
MEMORY CONTENTS



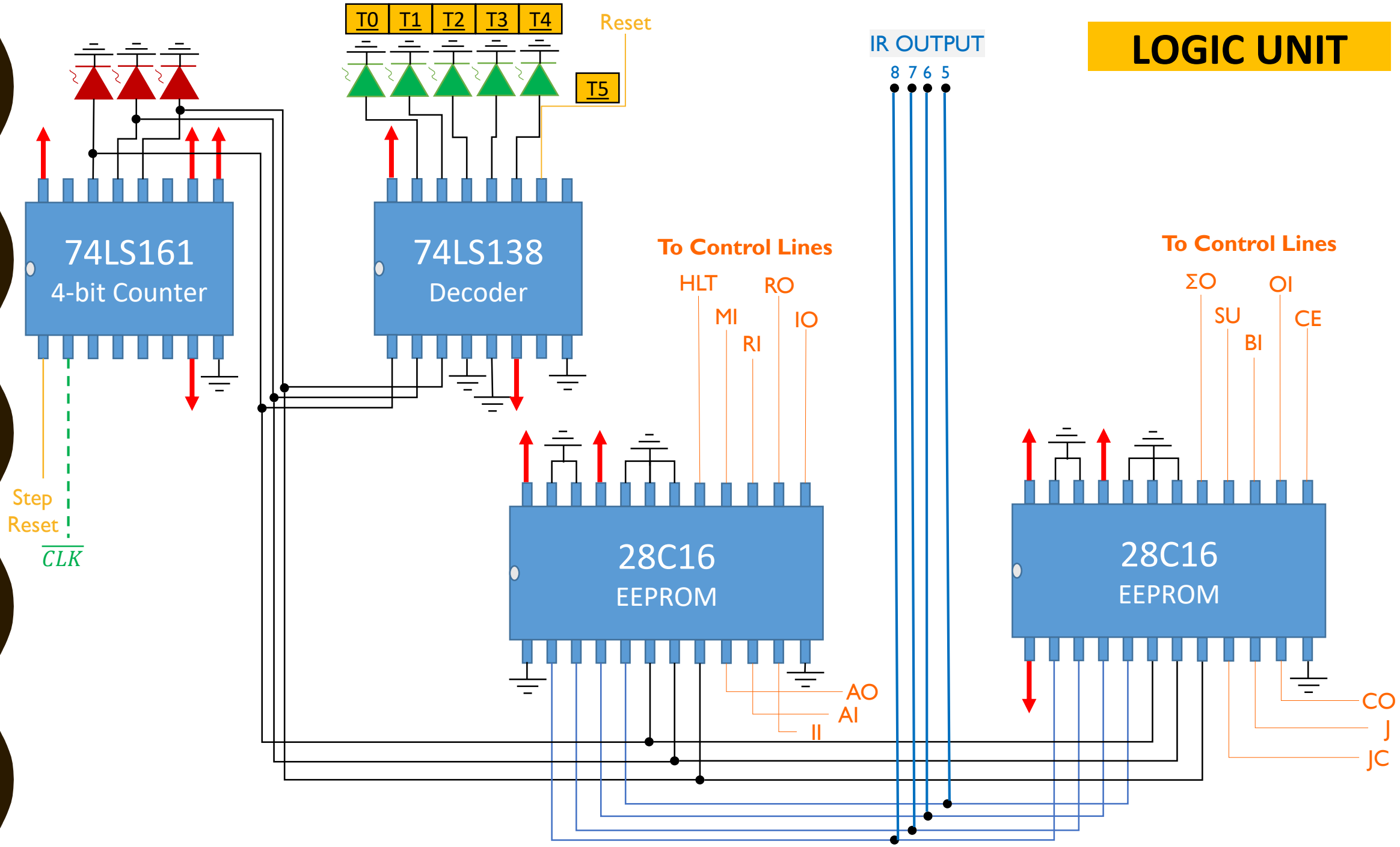
OUTPUT (4X1 DIGIT)



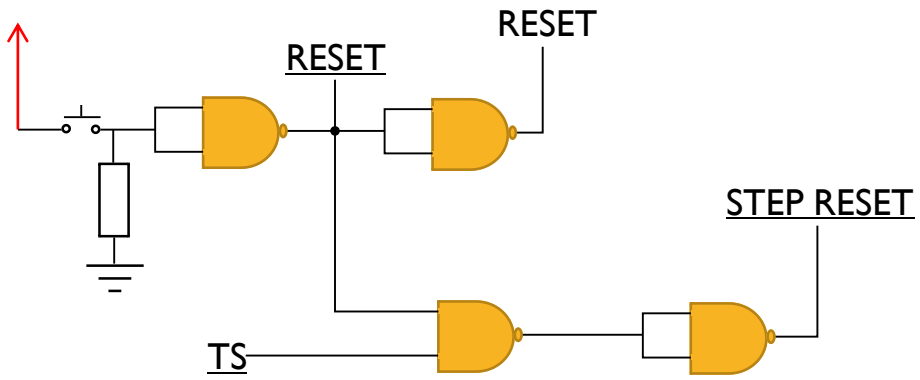
CONTROL

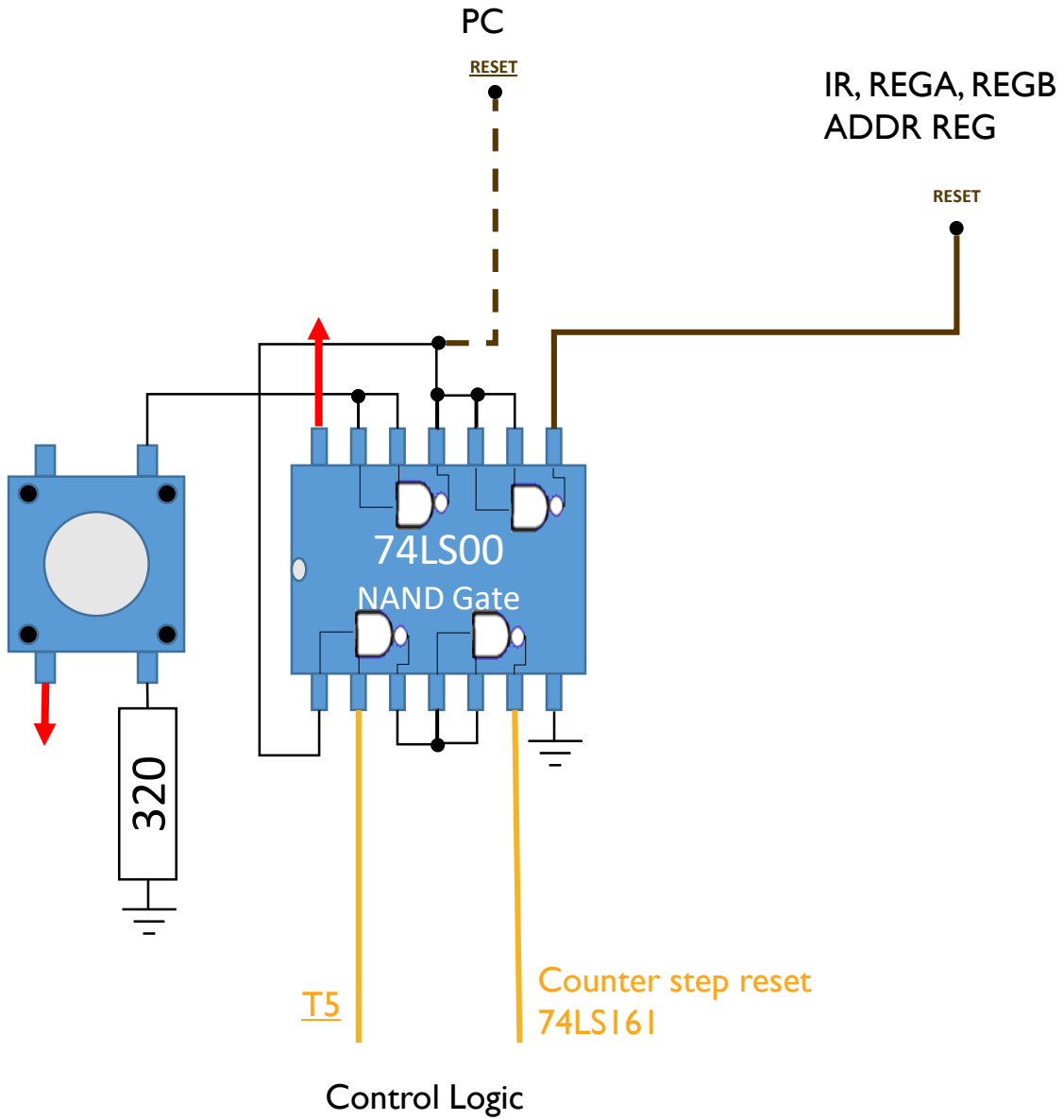

74LS04
INV
74LS04
INV
$\overline{II}$
$\overline{RO}$
$\overline{MI}$
$\overline{IO}$
HLT
RI
SU
OI
CE
$\overline{AO}$
$\overline{AI}$
$\overline{J}$
$\overline{CO}$
$\overline{JC}$
$\overline{BI}$
$\overline{\Sigma O}$
To logic unit
470
HLT
MI
RI
RO
IO
II
AI
AO
ΣO
SU
BI
JC
OI
CE
CO
J

LOGIC UNIT

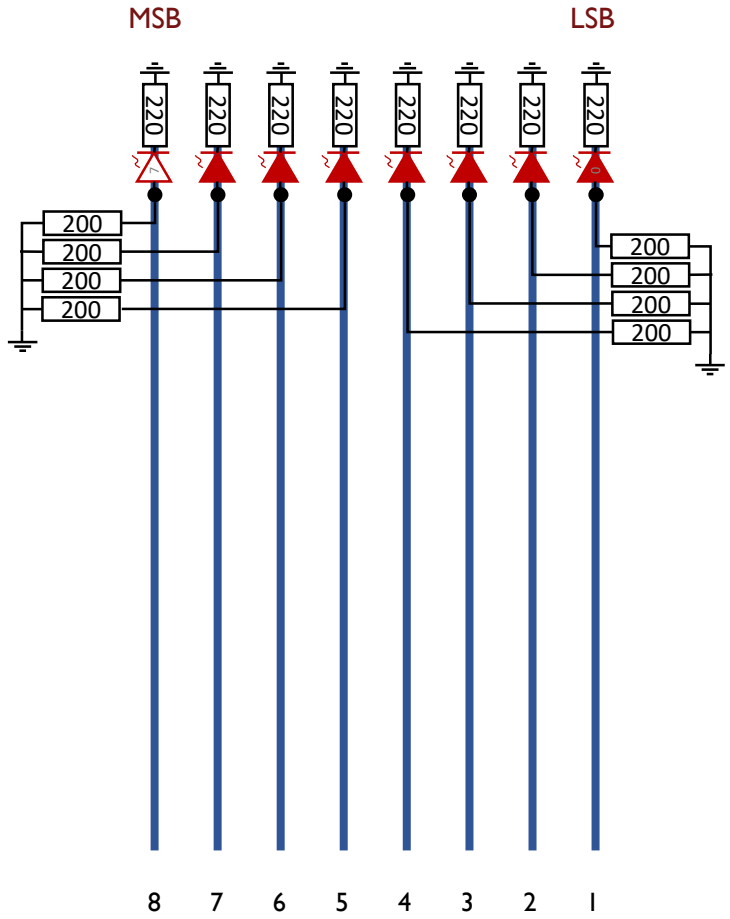

T0
T1
T2
T3
T4
T5
Reset
IR OUTPUT
8 7 6 5
74LS161
4-bit Counter
74LS138
Decoder
To Control Lines
HLT
MI
RI
RO
IO
To Control Lines
ΣO
SU
BI
OI
CE
Step
Reset
$\overline{CLK}$
28C16
EEPROM
28C16
EEPROM
AO
AI
II
CO
J
JC

MASTER RESET



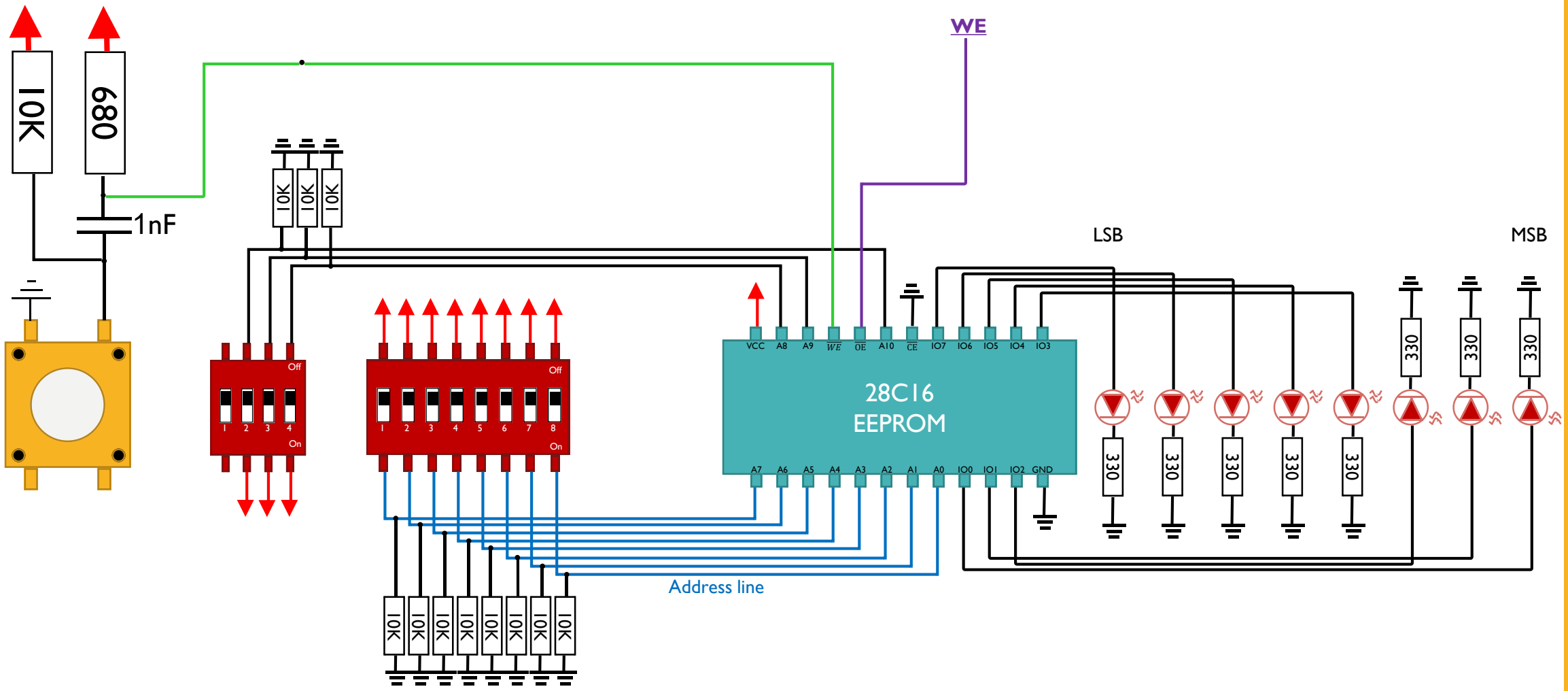


THE BUS

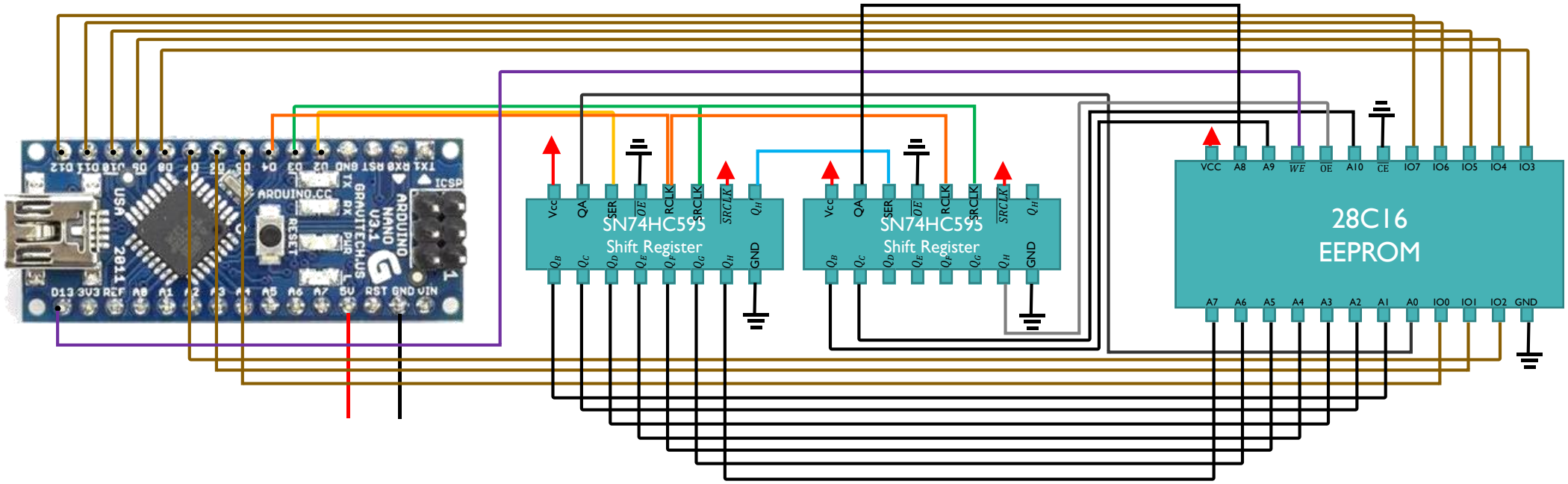

MSB
LSB
220
220
220
220
220
220
220
220
200
200
200
200
200
200
200
200
8
7
6
5
4
3
2
1

PROGRAMMING

EEPROM PROGRAMING WITH DIP SWITCH



EEPROM PROGRAMING WITH ARDUINO



BINARY TO DECIMAL DISPLAY