Technische Informatik: Abgabe 6

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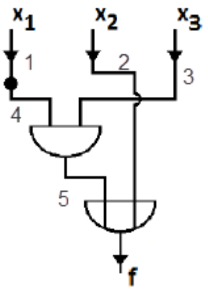
Exercise 6.1 (Circuit jam)

$f(x_1, x_2, x_3) = \bar{x}_1 x_3 + x_2$



$f_1, \ldots, f_5$ are 0-jams	$f_6, \ldots, f_a$ are 1-jams.
$f_1(x_1, x_2, x_3) = \bar{0}x_3 + x_2 = x_3 + x_2$	$f_6(x_1, x_2, x_3) = \bar{1}x_3 + x_2 = x_2$
$f_2(x_1, x_2, x_3) = \bar{x}_1 x_3 + 0 = \bar{x}_1 x_3$	$f_7(x_1, x_2, x_3) = \bar{x}_1 x_3 + 1 = 1$
$f_3(x_1, x_2, x_3) = \bar{x}_1 0 + x_2 = x_2$	$f_8(x_1, x_2, x_3) = \bar{x}_1 1 + x_2 = \bar{x}_1 + x_2$
$f_4(x_1, x_2, x_3) = 0x_3 + x_2 = x_2$	$f_9(x_1, x_2, x_3) = 1x_3 + x_2 = x_3 + x_2$
$f_5(x_1, x_2, x_3) = 0 + x_2 = x_2$	$f_a(x_1, x_2, x_3) = 1 + x_2 = 1$

Ausfalltafel:

#	x_1	x_2	x_3	f_1	f_2	f_3	f_4	f_5	f_6	f_7	f_8	f_9	f_a	f
0	0	0	0	0	0	0	0	0	0	1	1	0	1	0
1	0	0	1	1	1	0	0	0	0	1	1	1	1	1
2	0	1	0	1	0	1	1	1	1	1	1	1	1	1
3	0	1	1	1	1	1	1	1	1	1	1	1	1	1
4	1	0	0	0	0	0	0	0	0	1	0	0	1	0
5	1	0	1	1	0	0	0	0	0	1	0	1	1	0
6	1	1	0	1	0	1	1	1	1	1	1	1	1	1
7	1	1	1	1	0	1	1	1	1	1	1	1	1	1

$\Longrightarrow f_1 = f_9; f_2; f_3 = f_4 = f_5 = f_6; f_7 = f_a; f_8$

Ausfallmatrix:

#	x_1	x_2	x_3	f_1	f_2	f_3	f_7	f_8	f
0	0	0	0	0	0	0	1	1	0
1	0	0	1	1	1	0	1	1	1
2	0	1	0	1	0	1	1	1	1
3	0	1	1	1	1	1	1	1	1
4	1	0	0	0	0	0	1	0	0
5	1	0	1	1	0	0	1	0	0
6	1	1	0	1	0	1	1	1	1
7	1	1	1	1	0	1	1	1	1

Fehlermatrix:

#	x_1	x_2	x_3	$f \nleftrightarrow f_1$	$f \nleftrightarrow f_2$	$f \nleftrightarrow f_3$	$f \nleftrightarrow f_7$	$f \nleftrightarrow f_8$	Test
0	0	0	0	0	0	0	1	1	$\star$
1	0	0	1	0	0	1	0	0	$\star$
2	0	1	0	0	1	0	0	0	$\star$
3	0	1	1	0	0	0	0	0	
4	1	0	0	0	0	0	1	0	
5	1	0	1	1	0	0	1	0	$\star$
6	1	1	0	0	1	0	0	0	
7	1	1	1	0	1	0	0	0	

$\Longrightarrow$ Testvector: $\{(0,0,0),(0,0,1),(0,1,0),(1,0,1)\}$

Exercise 6.2 (Unshortenable DNF's fail fast)

Let $f : \mathbb{B}^n \to \mathbb{B}$ be a boolean function in disjunctive form *containing only prime implicants* [1], that is $f = \bigvee_{i \in I} f_i$ with $f_i = \bigwedge_{k \in K_i} \mathrm{op}_k^i(x_k)$ prime implicants, for $K_i \in \mathfrak{P}\{1, \dots, n\}$ and $\mathrm{op}_k^i \in \{x \mapsto x, x \mapsto \neg x\}$. We call a representation $f = \bigvee_{i \in I} f_i$ *shortenable* if there exists a subset $\tilde{I} \subsetneq I$ such that $f = \bigvee_{i \in \tilde{I}} f_i$, otherwise we call the representation $f = \bigvee_{i \in I} f_i$ *unshortenable*. Now suppose that a function f with the representation $f = \bigvee_{i \in I} f_i$ is implemented by a two-layered circuit with $|I|$ AND-gates in the first layer and one OR-gate (with fan-in $|I|$) in the second layer.

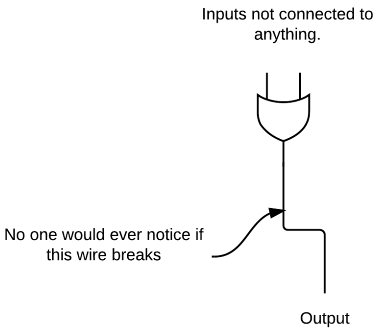
Claim: The following two statements are equivalent:

(1) Every broken connection changes the function of the circuit

(2) The corresponding representation $f = \bigvee_{i \in I} f_i \neq 0$ is unshortenable

Remark: We have to exclude the degenerate case $f = 0$, because otherwise the standard construction yields 0 AND-gates, one single OR-gate without any inputs, and a wire between the OR-gate and the output. This wire can be removed without changing the function.

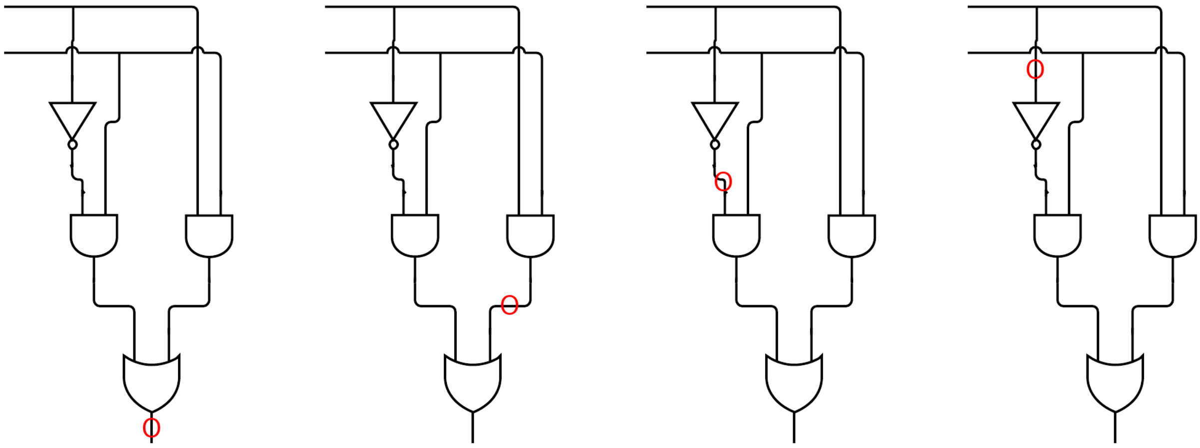
[1] The original statement is either wrong or conflicting with the definition from the lecture, see the comment after the proof



Degenerate case $f = 0$ contains a wire that can break without causing any effects.

Proof: We begin with $(1) \Rightarrow (2)$, which is equivalent to $\neg(2) \Rightarrow \neg(1)$. Suppose the representation $f = \bigvee_{i \in I} f_i$ is shortenable, that is, there is $\tilde{I} \subsetneq I$ with $f = \bigvee_{i \in \tilde{I}} f_i$. For each $j \in I \backslash \tilde{I} \neq \emptyset$ we can destroy the entire $j - th$ AND-gate together with all the adjacent wires, without changing the behaviour of the circuit, in particular, there exists at least one wire that can break without affecting the circuit. Therefore $\neg(1)$ holds.

To prove $(2) \Rightarrow (1)$ we consider all the possible cases. Let $f = \bigvee_{i \in I} f_i$ be unshortenable and suppose one connection breaks. Let $\check{f}$ denote the function implemented by the broken circuit. Furthermore, let $b_j \in \mathbb{B}^n$ be the boolean vectors such that $m_j(b_j) = 1$ for the j-th minterm.



Case 1:
Broken output wire.

Case 2:
Broken AND-gate output.

Case 3:
Broken AND-gate input.

Case 4:
Broken inverter input.

<u>Case 1:</u> Suppose the OR-gate output wire breaks. Then $\check{f} = 0 \neq f$.

<u>Case 2:</u> Suppose the output wire of an AND-gate breaks. If this had no effect on the result, then the conjunction corresponding to this AND-gate could be removed from the representation of f. This would contradict the assumption that the representation is unshortenable. Therefore, a broken output of an AND-gate *has* to affect the circuit.

<u>Case 3:</u> Suppose an input of an AND-gate breaks (if there is an inverter on the wire, we mean that the wire breaks right between the inverter and the AND-gate). Then one input of the AND-gate is stuck at 0, and the output of the whole AND-gate becomes constant 0, that is, a broken input of an AND-gate has the same effect as a broken output in the case 2. Again, this has to affect the whole circuit, because otherwise it

would contradict the assumption that the representation is unshortenable.

Case 4: Finally, suppose that an *input* wire of an inverter breaks. Then one input of the AND-gate is stuck at 1, and the whole AND-gate behaves as if we removed one variable from the corresponding term. This has to change the behavior of the whole circuit, because otherwise we would get a contradiction to the assumed primality of the term (we cannot remove variables from prime implicants). ■

The last case also shows why the original claim is invalid. Consider the circuit used in the illustrations as a simple counterexample for the original claim. It corresponds to the representation $f = m_1 + m_3 = \bar{x}y + xy$. It is already in the normal form, so the minterms are m_1, m_3. If we take m_1, m_3 as implicants, we obtain the implication table:

implicants \minterms	m_1	m_3
$\bar{x}y$	1	0
xy	0	1

Obviously, both rows are required to cover all columns, therefore (according to the definition given in the solution for the lecture 5) this implication matrix is unshortenable. However, breaking the input of the inverter (as on the figure for the case 4) does not affect the resulting circuit: it still represents just $y = f$. This is why we had to strengthen the assumption and require that all implicants in the SOP are prime.

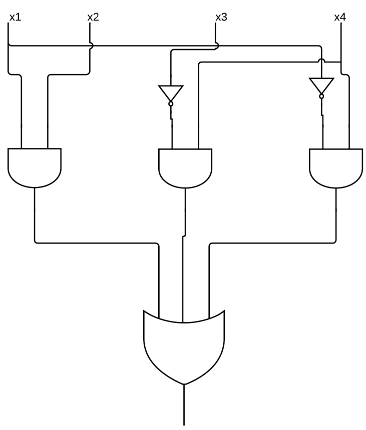
Exercise 6.3 (Hazards)

a) We use a Karnaugh-diagram to derive an optimal SOP-representation:

x_3x_4 \ x_1x_2	00	01	11	10
00			1	
01	1	1	1	1
11	1	1	1	
10			1	

which yields: $f = \bar{x}_3x_4 + x_1x_2 + \bar{x}_1x_4$.

The corresponding two-layer circuit is as follows:



b) Here are example hazards for $k = 1$ and $k = 2$ (k is number of variables that keep their value):

$$\begin{array}{ccccccc} f(1100) = 1 & \rightarrow & f(0100) = 0 & \rightarrow & f(0000) = 0 & \rightarrow & f(0001) = 1 \\ & & f(0011) = 1 & \rightarrow & f(1011) = 0 & \rightarrow & f(1111) = 1 \end{array}$$

c) The circuit above has a circuit-hazard $f(1111) = 1 \quad \rightarrow \quad f(0111) = 1$. It can occur as follows. In the beginning, first AND-gate is on, and the other two are off. When x_1 changes it's value to 0, the first AND-gate can change it's value to 0 a little bit earlier than the third AND-gate changes it's value to 1 (because the wire to third gate is longer and contains an additional inverter). This results in all three AND-gates switched off for a short period of time, the output is 0.

This circuit hazard can be seen in the Karnaugh-diagram as change from red to $green$.