Technische Informatik: Abgabe 4
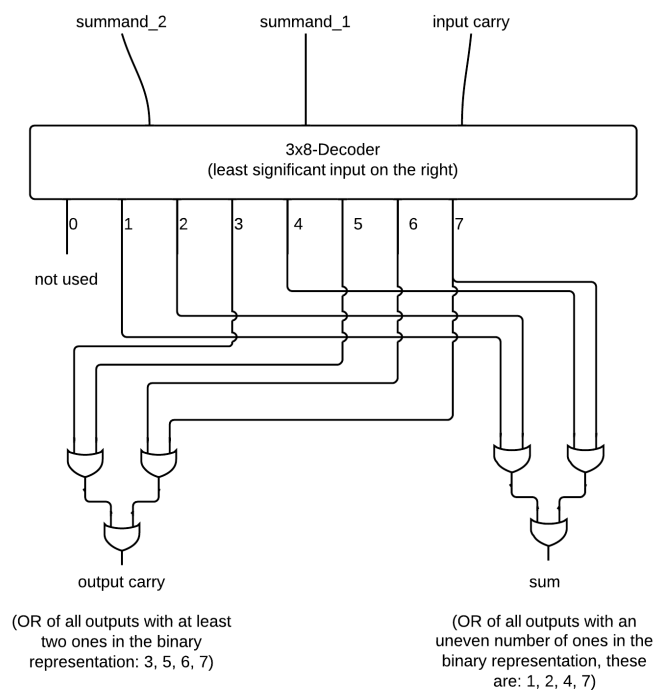
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Exercise 4.1 (Full adder from decoder)

summand_2   summand_1   input carry

3x8-Decoder
(least significant input on the right)

0   1   2   3   4   5   6   7

not used

output carry

(OR of all outputs with at least
two ones in the binary
representation: 3, 5, 6, 7)

sum

(OR of all outputs with an
uneven number of ones in the
binary representation, these
are: 1, 2, 4, 7)

Exercise 4.2 (Subtractors)

a) Here are the tables for the two circuits we wish to implement (namely Half-Subtractor and Full-Subtractor):

minuend	subtrahend	underflow	difference
0	0	0	0
0	1	1	1
1	0	0	1
1	1	0	0

minuend	subtrahend	underflow	underflow	difference
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	1	0
1	0	0	0	1
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

b) More or less compact symbolic representations of these two circuits are as follows (first component is always the resulting underflow, second is the actual difference):

$$HalfSubtractor(m, s) = (\bar{m}s, m \not\leftrightarrow s)$$

$$FullSubtractor(m, s, u) = (\bar{m} \not\leftrightarrow su, m \not\leftrightarrow s \not\leftrightarrow u)$$

c) Now we want to simplify both components (difference and undeflow) of the full subtractor using Karnaugh diagrams. We begin with the difference:

		minuend / subtrahend			
		00	01	11	10
underflow	0	?	?	?	?
	1	?	?	?	?

d)

Exercise 4.3 (TODO)

a) TODO **b)**

summand_2 summand_1 input carry

3x8-Decoder
(least significant input on the right)

0 1 2 3 4 5 6 7

not used

output carry

(OR of all outputs with at least
two ones in the binary
representation: 3, 5, 6, 7)

sum

(OR of all outputs with an
uneven number of ones in the
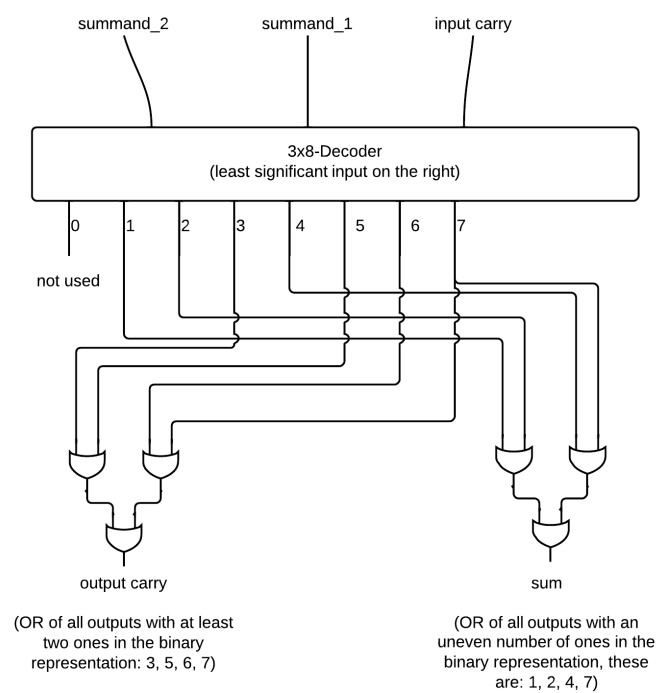binary representation, these
are: 1, 2, 4, 7)

Abbildung 1: Full subtractor. Notice that both outputs share some of the AND gates.