

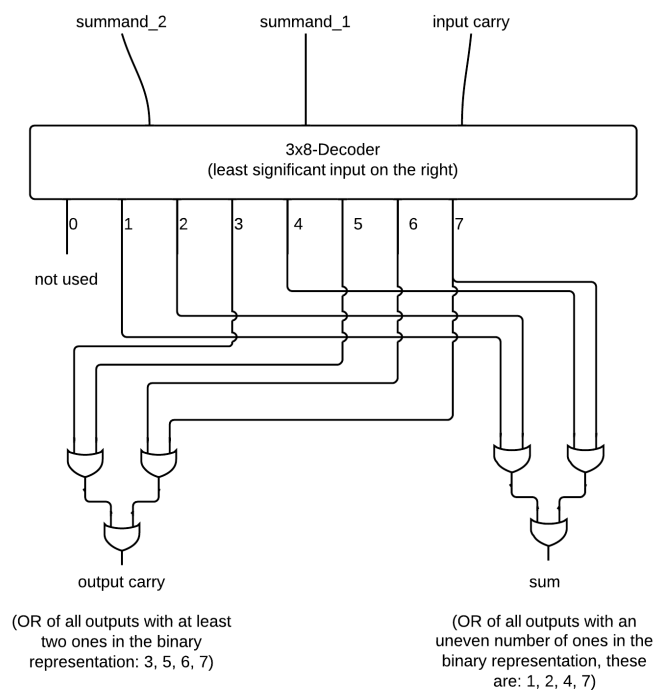
# Technische Informatik: Abgabe 4

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## Exercise 4.1 (Full adder from decoder)



## Exercise 4.2 (Subtractors)

**a)** Here are the tables for the two circuits we wish to implement (namely Half-Subtractor and Full-Subtractor):

minuend	subtrahend	underflow	difference
0	0	0	0
0	1	1	1
1	0	0	1
1	1	0	0

minuend	subtrahend	underflow	underflow	difference
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	1	0
1	0	0	0	1
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

**b)** More or less compact symbolic representations of these two circuits are as follows (first component is always the resulting underflow, second is the actual difference):

$$HalfSubtractor(m, s) = (\bar{m}s, m \nrightarrow s)$$

$$FullSubtractor(m, s, u) = (\bar{m} \nrightarrow su, m \nrightarrow s \nrightarrow u)$$

**c)** Now we want to simplify both components (difference and underflow) of the full subtractor using Karnaugh diagrams. We begin with the difference:

		minuend / subtrahend			
		00	01	11	10
underflow	0	?	?	?	?
	1	?	?	?	?

**d)**

## Exercise 4.3 (TODO)

**a) b)**

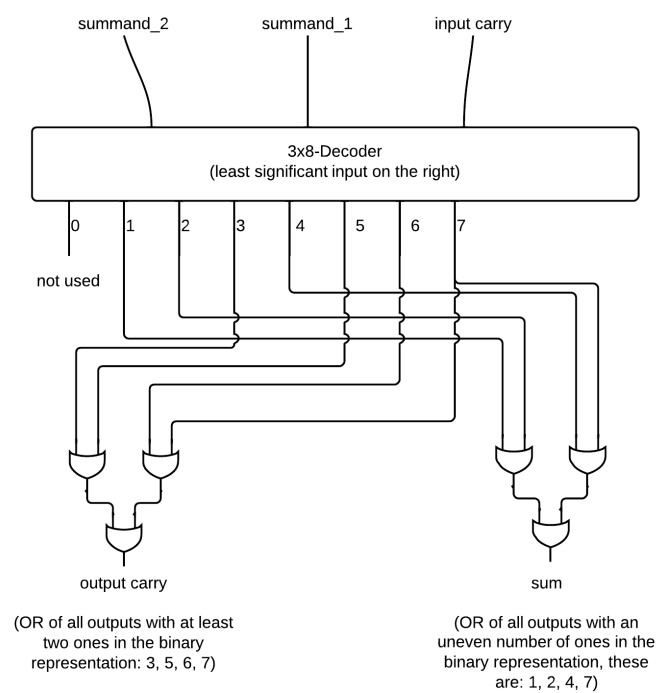


Abbildung 1: Full subtractor. Notice that both outputs share some of the AND gates.