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PCIe-Mini-Synchro

16-BIT TRACKING RESOLVER-TO-DIGITAL CONVERTER

PCIexpress Mini

928-10-000-4000

REFERENCE MANUAL

Revision 1.0
July 2020

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Manual update

Release Rev.10 7/2/2020

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GENERAL DESCRIPTION

1.1. INTRODUCTION

The PCIe-Mini-SYNCHRO module provides One Channel Resolver to digital converter. The configuration ordered can support a 11.8V and 90V
The PCIe-Mini-SYNCHRO is designed based on the DDC integrated Circuits RDC 19231.

The PCIe-Mini form factor provides easy installation.

The PCIe-Mini-SYNCHRO is installed with the following resources:

- One channel Synchro/Resolver Input Channel
- Accuracy to 1 Arc Minute
- Programmable Resolution and Bandwidth
- Internal Synthesized Reference
- Configuration available for 11.8V 90V Synchro and Resolver
- 4 Channels 16 Bits D/A , 10µs settling time
- 30mA output drive
- Extended temperature ranges

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1.2. FUNCTIONAL DESCRIPTION

A functional block diagram of the PCIexpress Mini module is depicted below in Figure 1. The PCIe-Mini-SYNCHRO is designed around the DDC RDC 19231 that is used to measure the motion feedback solutions and provide high accuracy positioning, direction and speed data for high reliability applications Via x1 lane Pciexpress Bridge.
As well a Four Channels Digital to Analog converter with settling time of 10us was implemented to provide 16 Bits Controls with 30ma output drive.

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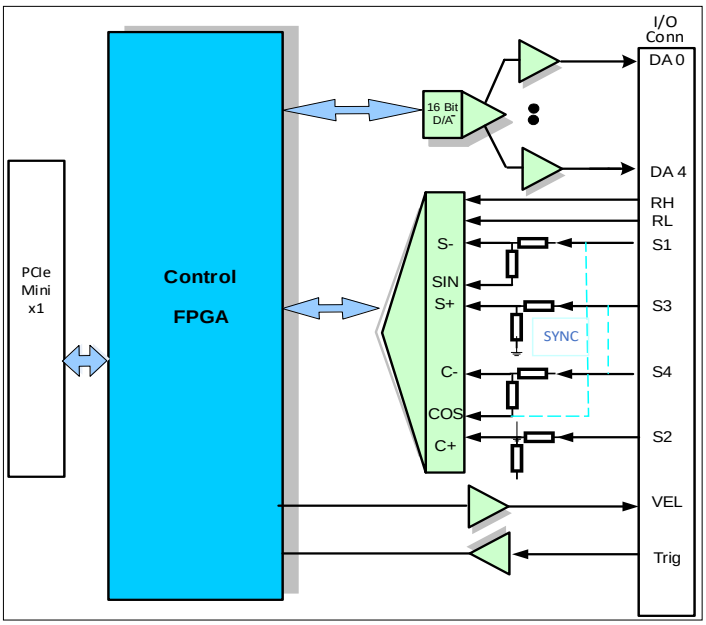

Figure 1.0: PCIe-Mini-SYNCHRO **Block Diagram**

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1.3. REFERENCE MATERIALS LIST

The reader should refer to the “RDC-19231 Data sheet”, from DDC , that provides detailed descriptions about the RDC-19231 registers and capabilities.

https://www.ddc-web.com/ddc/public/en/motioncontrol/motionfeedbacksynchroresolver/synchroresolvertodigital-1/components-3/16-bit-resolver-to-digital-converter?partNumber=RD-19231

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WWW Home Page:
http://www.DDC-Web.com

The reader should refer to the PCIe Local Bus Specification for a detailed explanation of the PCIe bus architecture and timing requirements.

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2. HOST (PCIe-Mini) SIDE

2.1. Interface to HOST (PCIe-Mini)

All PCIe-Mini) devices contain a set of registers in Configuration Space which allow for determining the manufacturer and model of the device, determining the resources necessary for the correct operation of the device, and other configuration information. Configuration space is decoded on a per slot / device basis via a mechanism described in the Mini-PCI specification.

All PCIe-Mini devices can be relocated in physical memory by means of several Base Address Registers. These registers contain the high address bits, which must be matched for any access to the card to be successful. Part of the protocol of programming the Base Address Registers allows for the transfer of information regarding the size of the regions.

The actual Base Address Registers are located in Configuration Space.
Normally, configuring the card is performed by the system controller and some form of firmware or BIOS. Unfortunately, determining Base Addresses and other configuration information in Configuration Space is operating system dependent. One of the primary functions of the device driver under Windows NT/XP/WIN7 is to map these resources to the user application.

The card is actually accessed through the decoded base address registers.

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2.2. PCIe-Mini Configuration Space

PCI Address: *CONFIG:0x00 – 0x3C*
Mode of Access: *Read/Write*
Reset By *Mini-PCI Hardware Reset*

The card has the following registers available to PCIe-Mini Configuration Space. They are implemented in the FPGA chip.

Offset Into PCI CFG	31 – 24	23 – 16	15 – 8	7 – 0
0x00	Device ID		Vendor ID	
0x04	Status		Command	
0x08	Class Code			Revision ID
0x0C	BIST	Header Type	PCI Latency Timer	Cache Line Size
0x10	PCI Base Address 0 (Memory Access to PLX Registers)			
0x14	PCI Base Address 1 (I/O Access to PLX Registers)			
0x18	PCI Base Address 2 (Memory Access to DSP SRAM and card registers)			
0x1C	PCI Base Address 3 (Not Used for this card)			
0x20	Unused PCI Base Address 4			
0x24	Unused PCI Base Address 5			
0x28	Cardbus CIS Pointer (Not Supported)			
0x2C	Subsystem ID		Subsystem Vendor ID	
0x30	PCI Base Address for Expansion ROM			
0x34	Reserved			
0x38	Reserved			
0x3C	Max Latency	Min Grant	Interrupt Pin	Interrupt Line

Table 2.1: PCIe-Mini Configuration Space

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The card presents the following initial configuration values to the PCIe-Mini system, based on the values stored in the device.

Register	Value (Meaning)
Vendor ID	0x13C5 (Alphi technology Corporation)
Device ID	0x0508 (PCIe-Mini-Synchro)
Revision ID	0x00
Class Code	0xff0000 (Device does not fit into defined class codes)
Interrupt Line	0xff
Interrupt Pin	A
Multifunction Device	No
Build In Self Test	No
Latency Timer	0x00
Minimum Grant	0x00
Maximum Latency	0x00
Base Address 0 Size	16K Bytes Allocated
Base Address 1 Size	Not used
Base Address 2 Size	4K Bytes Allocated
Base Address 3 Size	No used
Expansion ROM Size	None

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Table 2.2: PCIe-Mini-Synchro Default Configuration

2.3. PCIe-Mini Base Address Regions

HOST Address	WIDTH USED	Description	TYPE
BAR0	16 K bytes	PCIexpress Control Register	I/O
BAR2	4 K bytes	Mini-Synchro IO Space	
BAR3	Not used		
BAR4	Not used		
BAR5	Not used		

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Table 2.3: PCIe-Mini-Synchro Base Address Regions

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1 Register Description

1.1 BAR2 Address Map

Address Offset	Module	R/W	Size	Description
0x0000	System ID	R	32-bit	System Identification
0x0004	FPGA Version	R		Time stamp corresponding to the FPGA version
0x0010	Control Register	R/W	32-bit	General Purpose Outputs
0x0020	GP Input	R	32-bit	General Purpose Inputs
0x0040	Synchro Position	R	32-bit	Synchro Position Data
0x004C	Encoder Counter	R	32-bit	Encoder Counter Data
0x0080	S1 Gain	R/W	32-bit	Simulator amplitude channel 1
0x0084	S2 Gain	R/W	32-bit	Simulator amplitude channel 2
0x0088	S3 Gain	R/W	32-bit	Simulator amplitude channel 3
0x0090	Ref Angular Velocity	R/W	32-bit	Simulator angular velocity of the references, used to calculate frequency
0x00c0	D/A SPI interface	R/W	32-bit	SPI interface used when the D/A are used as general purpose D/As

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Figure 1: Bar 2 Address Map

1.2 0x00 – System ID -- RO

Bit	31-0
	System ID

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System ID: 0x00000101

1.3 0x04 – Timestamp -- RO

Bit	31-0
	Timestamp

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FPGA Version:

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1.4 0x10 – Control Register – R/W

Bit	9:7	6	5	4	3	2	1:0
	DAC_Span	DAC_RSTn	DSRn	A_Q_Bn	DN_UPn	Shift	Res

Bit	31:12	11	10
	Unused	DAC ldac_n signal	Simulator/DA

These outputs are connected directly to the corresponding input of the RD19231. Refer to the chip datasheet for further details.
Res: Resolver resolution. 11 = 16 bits (default), 10 = 14 bits, 01 = 12 bits, 00 = 10 bits
Shift: ~~1~~Connected to the RD19231 **Shift** pin. A '1' Selects VEL1 components (default), ~~0~~'0' selects VEL2 components.
DN_UPn: Connected to the RD19231 **UP/DN** pin. Only '0'and '1' are supported. Selects the gain of the amplifier driving the de-selected set of bandwidth components (default 0 – pre-set resolution to increase).
A_Q_B: Enables encoder emulation (default 0). Do not change
DSR: Disables synthesized reference (default 0). Do not change
DAC_RST: Sets DAC channels to midrange (default 0).
DAC_Span: 000 = +/- 10V (11.6 V inputs), 010 = +/- 2.5V (direct inputs)
Simulator/DA: When 0, the D/A are used by the synchro simulator, when 1 they are used as general purpose D/A, and accessible through the SPI interface.
LDAC_n: When in general purpose D/A mode, this bit reflects the state of the LDAC_n signal of the DA interface. Refer to the DA manual.

1.5 0x20 -- GP Input -- RO

Bit	31-4	3	1	0
	Unused	B_U	A	BITn

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BITn: Built-In-Test. Active low signal indicates a loss of signal or a large error in the tracking of the converter
A: Encoder output A. There is an up/down counter that tracks the encoder, or its current state can be read here.
B_U: Encoder output B. There is an up/down counter that tracks the encoder, or its current state can be read here.

1.6 0x40 – Synchro Position -- RO

Bit	31-16	15-0
	Last Synchro Position	Synchro Position

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Synchro Position: 2*PI / 2^16 = 1 LSB current resolver angle.
Last Synchro Position: resolver angle from the previous busy cycle.

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1.7 0x4C – Encoder Counter -- RO

Bit	31-16	15-0
	Encoder Error	Counter

Counter: Count of the number of A and B up steps minus the down steps.
Encoder Error: A and B pins are not counting in a gray code manner.

1.8 0x80 – S1 Gain -- RW

Bit	31-16	15-0
	Unused	S1 Gain

S1 Gain: Signed 2's complement number. 32767 = %100, -32768 = -%100.
This value is multiplied by the sine of the current angular position, and sent to the D/A converter every microsecond, to generate a sinewave of the proper amplitude to simulate the synchro position.
Unused: Reads 0.

1.9 0x84 – S2 Gain -- RW

Bit	31-16	15-0
	Unused	S2 Gain

S1 Gain: Signed 2's complement number. 32767 = %100, -32768 = -%100.
This value is multiplied by the sine of the current angular position, and sent to the D/A converter every microsecond, to generate a sinewave of the proper amplitude to simulate the synchro position.
Unused: Reads 0.

1.10 0x88 – S3 Gain -- RW

Bit	31-16	15-0
	Unused	S3 Gain

S1 Gain: Signed 2's complement number. 32767 = %100, -32768 = -%100.
This value is multiplied by the sine of the current angular position, and sent to the D/A converter every microsecond, to generate a sinewave of the proper amplitude to simulate the synchro position.
Unused: Reads 0.

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1.11 0x90 – Simulator Ref Angular velocity -- RW

Bit	31-17	16-0
	Unused	Ref DDS Speed

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Angular velocity: It is expressed in radian/microsecond. The simulator D/As update every microsecond, and it is the angle that is added to the angular position every 1MHz.
The angle is 1 bit of sign, 2 bits of whole number and 14 bits of fraction. It has a range of +PI to -PI.
Unused: Reads 0.

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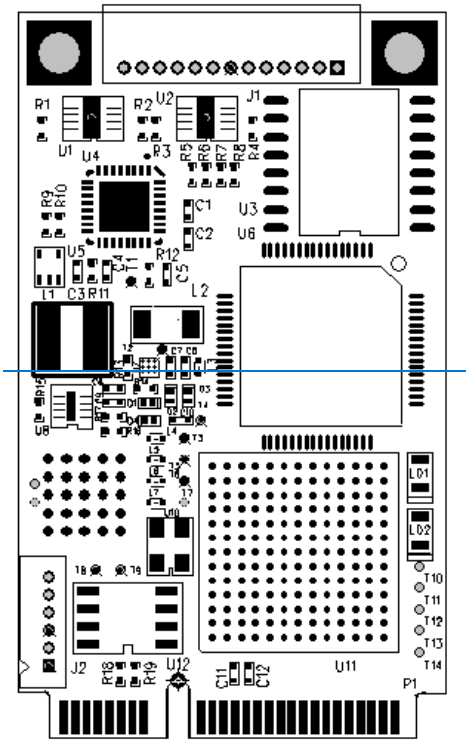
2 CONNECTORS LOCATION



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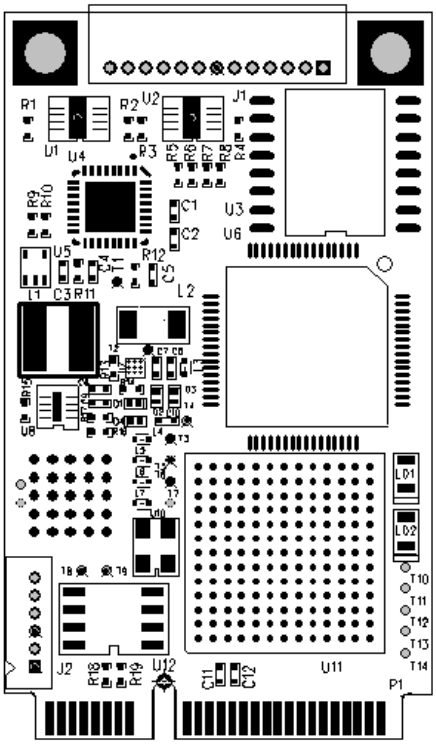

Figure 2.1: **Connector LOCATION**

2.4. Jumpers Description

None

2.5. Connectors Description

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1.1.1 Connector Descriptions

J1 Connector are manufactured by Molex and the style is Pico-blade

Use	Model
On PC Board	53048-1310
Suggested Plug	51021-1300
Suggested Contact	50125-8100

Table 2.1: J1 I/O Connector Model Numbers

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1.1.2 External I/O Connector J1

The signals are routed as follow for PCIe-Mini-SYNCHRO

Pin	Connection	Description
1	RH	Reference +
2	RL	Reference -
3	S1	Phase Input 1
4	S2	Phase Input 2
5	S3	Phase Input 3
6	S4	Phase Input 4
7	GND	Converter Ground
8	VOUT1	D2A Channel 1
9	VOUT2	D2A Channel 2
10	VOUT3	D2A Channel 3
11	VOUT4	D2A Channel 4
12	VEL	Analog Velocity (REV B)
13	TRIG	Trigger Input

Table 4.1: J1 external I/O connector PCIe-Mini-SYNCHRO

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2.6. P1 PCiexpress Mini Connections

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P4	Signal	P4	Signal
1	NC	2	3.3V
3	NC	4	GND
5	NC	6	1.5V
7	GND: CLKreq	8	NC
9	GND	10	NC
11	REF CLK+	12	NC
13	REF CLK+	14	NC
15	GND	16	NC
17	NC	18	GND
19	NC	20	NC
21	GND	22	PCIe reset
23	PCIe TX -	24	NC
25	PCIe TX +	26	GND
27	GND	28	1.5V
29	GND	30	NC
31	PCIe RX -	32	NC
33	PCIe RX +	34	GND
35	GND	36	NC
37	GND	38	NC
39	3.3V	40	GND
41	3.3V	42	NC
43	GND	44	NC
45	NC	46	NC
47	NC	48	1.5V
49	NC	50	GND
51	NC	52	3.3V

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NC: No Connection to the board

Table 2.2: PCIepress Connections

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