

16-BIT MONOLITHIC TRACKING RESOLVER-TO-DIGITAL CONVERTER

RD-19231 DATA SHEET

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1 PREFACE

This data sheet uses typographical conventions to assist the reader in understanding the content. This section will define the text formatting used in the rest of the data sheet.

1.1 Text Usage

- **BOLD**—indicates important information and table, figure, and chapter references.
- ***BOLD ITALIC***—designates DDC Part Numbers.
- *Courier New*—indicates code examples.
- <...> - indicates user-entered text or commands.

1.2 Special Handling and Cautions

The **RD-19231** uses state-of-the-art components, and proper care should be used to ensure that the device will not be damaged by Electrical Static Discharge (ESD), physical shock, or improper power surges and that precautions are taken to avoid electrocution.



Warnings: Turn off power to the computer hardware and unplug from wall.

NEVER insert or remove card with power turned on.

Ensure that standard ESD precautions are followed. As a minimum, one hand should be grounded to the power supply in order to equalize the static potential.

Do not store disks in environments exposed to excessive heat, magnetic fields or radiation.

1.3 Trademarks

All trademarks are the property of their respective owners.

1.4 What is included in this data sheet?

This data sheet contains a complete description of hardware installation and use.

1.5 Technical Support

In the event that problems arise beyond the scope of this manual, you can contact DDC by the following:

US Toll Free Technical Support:
1-800-DDC-5757, ext. 7771

Outside of the US Technical Support:
1-631-567-5600, ext. 7771

Fax:
1-631-567-5758 to the attention of SYNCHRO Applications

DDC Website:
www.ddc-web.com/ContactUs/TechSupport.aspx

Please note that the latest revisions of Software and Documentation are available for download at DDC's Web Site, www.ddc-web.com.

2 OVERVIEW

The RD-19231 is a small and versatile, low cost, state-of-the-art 16-bit monolithic Resolver-to-Digital Converter. This single chip converter offers programmable features such as resolution, bandwidth, velocity output scaling and encoder emulation.

Resolution programming allows selection of 10, 12, 14, or 16 bit, with accuracies to 1 minute. The parallel digital data and the internal encoder emulation signals (A QUAD B) have independent resolution control. Internal encoder emulation will permit inhibiting (freezing) the parallel digital data without interrupting the A and B outputs.

The internal Synthesized Reference feature eliminates errors due to quadrature voltage and ensures operation with a rotor-to-stator phase shift of up to 45 degrees. The velocity output (VEL) can be used in place of a tachometer. It has a range of ± 4 V relative to analog ground. The velocity scale factor/tracking rate is programmed with a single resistor. This converter provides the option of using a second set of filter components which can be used in dual bandwidth or switch on the fly applications.

2.1 Features

- Accuracy up to 1 Arc-Minute
- Use to Interpolate Synchro, Resolver, Inductosyn, LVDT, RVDT, and Hall Sensors
- Digital Outputs Configurable to 3.3V or 5V
- DC to 10 kHz
- Internal Synthesized Reference
- Power From Only +5V Option
- Programmable Resolution, Dual Bandwidth, and Tracking Rate
- Internal Encoder Emulation with Independent Resolution Control
- Velocity Output Eliminates Tachometer
- Built-In-Test (BIT) Output, No 180° Hangup with AC Reference
- -40°C to +85°C Operating Temperature
- Lead Free (RoHS Compliant) Option

Applications Include:

- Military Fire Control Systems
- Naval Navigation and Weapon Systems
- Industrial Control
- Motor Control
- Machine Tool Control
- Robotics
- Factory Automation
- Hybrid Electric Vehicles
- Aviation Flight Control Surfaces
- Unmanned Vehicles

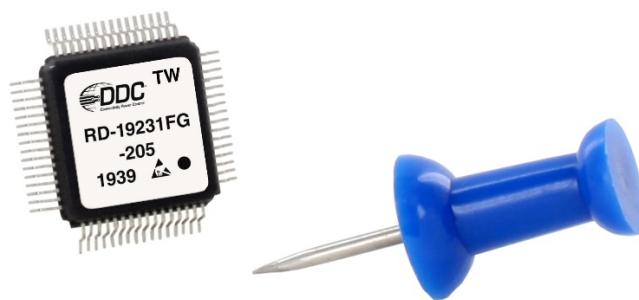


Figure 1. RD-19231 16-Bit Monolithic Tracking Resolver-to-Digital Converter

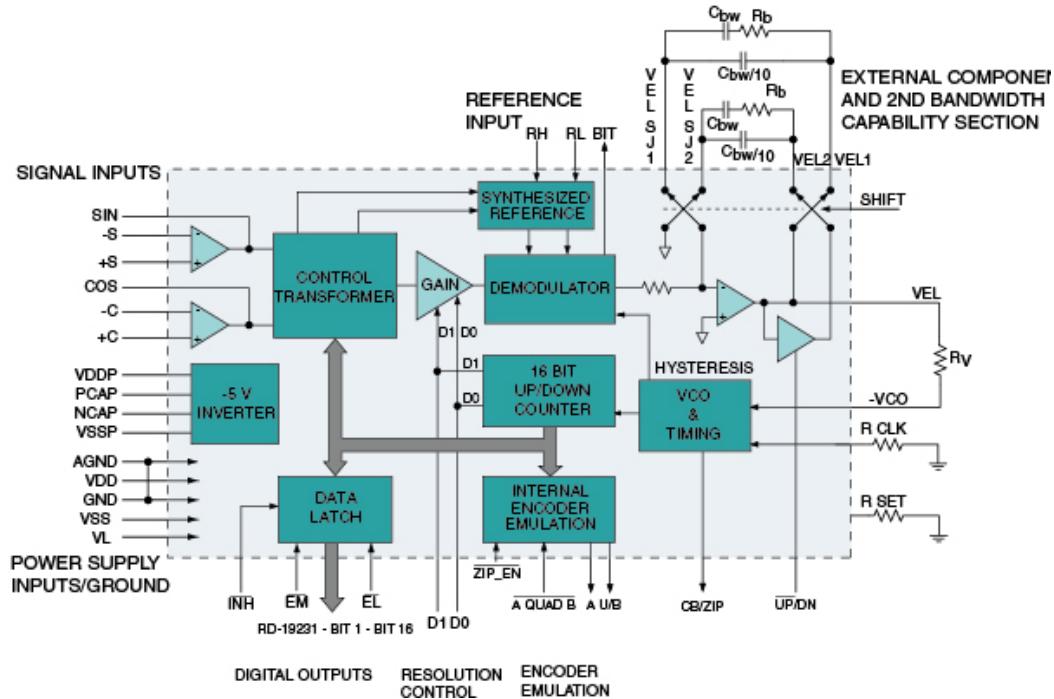


Figure 2. RD-19231 Block Diagram

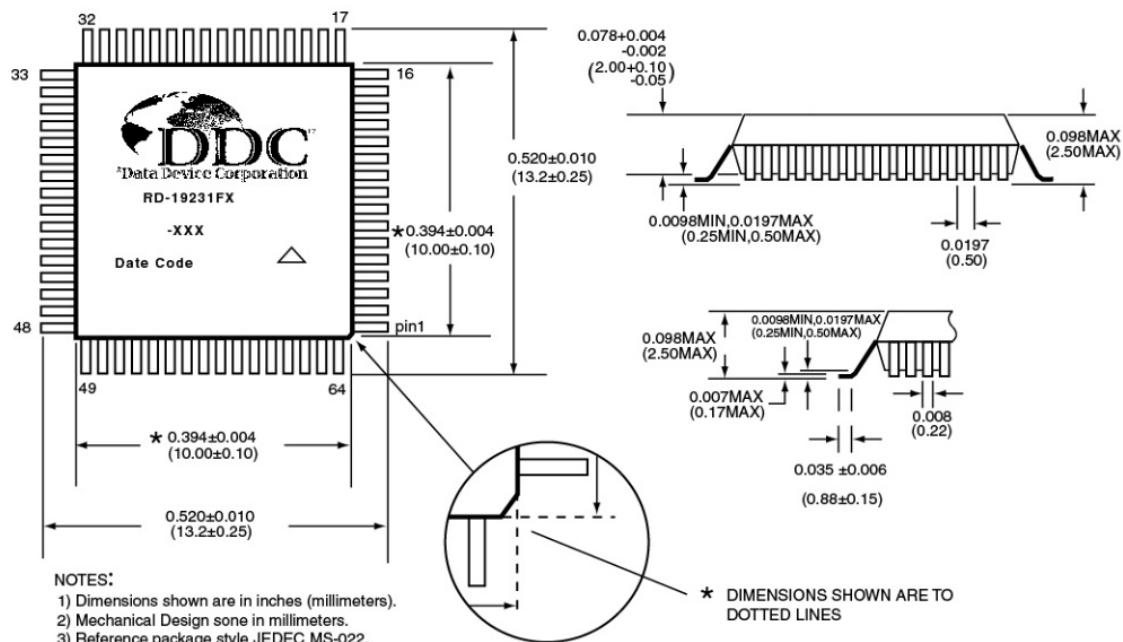


Figure 3. RD-19231 Mechanical Outline (Plastic Package)

Table 1. RD-19231 Specification Table

These specs apply over the rated power supply, temperature, and reference frequency ranges: 10% signal amplitude variation, and 10% harmonic distortion (for values without a tolerance already specified).

PARAMETER	VALUE				UNITS
RESOLUTION (note 1, 2)	10, 12, 14, 16				bits
FREQUENCY RANGE (note 3)	47 – 1k (note 4)	1k – 4k	4k – 7k	7k – 10k	Hz
Accuracy (Tested with Rclk = RSet = 30K)					
• -XX2	4 +1 LSB	4 +1 LSB	4+1 LSB	5 + 1 LSB	minutes
• -XX3	2 +1 LSB	2 +1 LSB	3 +1 LSB	4 + 1 LSB	minutes
• -XX5	1 +1 LSB	1 +1 LSB	3 +1 LSB	3 +1 LSB	minutes
Repeatability	±1	±1	±2	±2	LSB
Differential Linearity	±1	±1	±2	±2	LSB
REFERENCE	(+RH, -RL)				
Type	Differential				
Voltage: differential	10 max. (note 11)				Vp-p
Single Ended	±5 max. (1.5 min.) (note 11)				Vp
Overload	±25 continuous; ±100 transient (note 13)				Vp
Frequency	DC, 47 to 10k (note 4)				Hz
Input Impedance	10M min. 20 pF				Ω
Common Mode Range	3				Vp
SYNTHESIZED REFERENCE (note 5)	45 max. from 400Hz to 10kHz				deg
SIGNAL INPUT	(+S, -S, SIN, +C, -C, COS)				
Type	Resolver, differential, groundbased				
Voltage: operating	2 +/- 15%				Vrms
Overload	±25 continuous (note 13)				Vp
Input Impedance	10M min. 10 pF				Ω
DIGITAL INPUTS (note 10)					
TTL/CMOS Compatible Inputs	Logic 0 = 0.8 V max. Logic 1 = 2.0 V min. Logic -1 = -3.5V min. Loading = 10 µA max P.U. current source to +5V 5 pF max., CMOS transient protected				
Inhibit (<u>INH</u>)	Logic 0 inhibits; Data stable within 150 ns (Logic 1 = Transparent)				
Enable Bits 1 to 8 (<u>EM</u>)	Logic 0 enables; Data stable within 150 ns (Logic 0 = Transparent) Logic 1 = High Impedance; Data High Z within 100 ns (note 8)				
Enable Bits 9 to 16 (<u>EL</u>)					

Table 1. RD-19231 Specification Table

These specs apply over the rated power supply, temperature, and reference frequency ranges: 10% signal amplitude variation, and 10% harmonic distortion (for values without a tolerance already specified).

PARAMETER	VALUE				UNITS
Resolution and Mode Control (D1 & D0) (note 1, 2)	Mode	D1	D0	Resolution	
	Resolver	0	0	10 bits	
	Resolver	0	1	12 bits	
	Resolver	1	0	14 bits	
	Resolver	1	1	16 bits (preset, note 10)	
	LVDT	-1	0	8 bits	
	LVDT	0	-1	10 bits	
	LVDT	1	-1	12 bits	
	LVDT	-1	-1	14 bits	
<u>ZIP_EN</u>	Logic 0 enables ZIP, Logic 1 enables CB				
SHIFT	Logic 1 selects VEL1 components, Logic 0 selects VEL2 components				
<u>UP / DN</u>	Logic 0, precharged components gain 4 Logic 1, precharged components gain is $\frac{1}{4}$				
A QUAD B	Logic 0 enables encoder emulation, Falling edge latches encoder resolution				
<u>DSR</u>	Logic 0 will disable synthesized reference No connect enables synthesized reference (normal mode)				
DIGITAL OUTPUTS					
Drive Capability with VL = 5V					
Logic 0 (at 0.4 Vmax.)	2.1 max mA				
Logic 1 (at 2.8 Vmin.)	6.7 max. mA				
Drive Capability with VL = 3.3V					
Logic 0 (at 0.4 Vmax.)	1.3 max. mA				
Logic 1(at 2.8 Vmin.)	1.4 max. mA				
Parallel Data (1-16) (note 14)	10, 12, 14, or 16 parallel lines; natural binary angle positive logic (note 2)				
Converter Busy (CB)	0.25 to 0.75 μ s positive pulse leading edge initiates counter update. (CB functions with <u>ZIP_EN</u> pin tied to +5V or NC), Logic 1 at all 0's				
Zero Index Pulse (ZIP)	This output is active when the <u>ZIP_EN</u> pin is tied to GND (Logic 0)				
Built-In Test (<u>BIT</u>)	The <u>BIT</u> error is triggered if any of the following conditions exist: ~ 180 LSBs of positive error, ~ 180 LSBs of negative error, Loss of Signal (LOS), or Loss of Reference (LOR) is less than 500 mVp, or a false null occurs when the phase detect circuitry causes a <u>BIT</u> and corrects the error. Logic 0 for fault condition.				
A, B (note 14)	Incremental Encoder Output				

Table 1. RD-19231 Specification Table

These specs apply over the rated power supply, temperature, and reference frequency ranges: 10% signal amplitude variation, and 10% harmonic distortion (for values without a tolerance already specified).

PARAMETER	VALUE				UNITS
DYNAMIC CHARACTERISTICS	(at maximum bandwidth)				
Resolution	10	12	14	16	bits
Tracking Rate	1152	288	72	18	rps
Bandwidth (Closed Loop)	1200	1200	600	300	Hz
Ka (Acceleration Constant) (note 12)	5.7 M	5.7 M	1.4 M	360 k	1/sec ²
A1	19.5	19.5	4.9	1.2	1/sec
A2	295 k	295 k	295 k	295 k	1/sec
A	2400	2400	1200	600	1/sec
B	1200	1200	600	300	1/sec
Acceleration (1 LSB lag)	2 M	500 k	30 k	2 k	deg/sec ²
Settling Time (179° step)	2	8	20	50	msec
VELOCITY CHARACTERISTICS					
Polarity	Positive for increasing angle				
Voltage Range (Full Scale)(note 14)	±4 (at nominal power supply)				
Scale Factor Error	10 typ	20 max			%
Scale Factor TC	100 typ	200 max			PPM/°C
Reversal Error	0.75 typ	1.3 max			%
Linearity	0.25 typ	1.0 max			%
Zero Offset	5 typ	10 max			mV
Zero Offset TC	15 typ	30 max			µV/°C
Load	8 min				
POWER SUPPLIES (note 6)					
Nominal Voltage	+5 (VDD)	-5 (VSS)			V
Voltage Range	±5	±5			%
Max Volt. w/o Damage	+7	-7			V
Current	25 max. (each), 17 typ.* (*Typical current is when a 30K resistor is used for the current set.)				
VL Logic Supply	Set to 3.3V = 3.3V logic outputs Set to 5V = 5V logic outputs				
TEMPERATURE RANGE					
Operating (case)					
-30X	0 to +70				
-20X	-40 to +85				
Storage	-65 to +150				
Junction-to-Case	20				
Junction-to-Ambient	50				
Junction Temp Max	150				

Table 1. RD-19231 Specification Table

These specs apply over the rated power supply, temperature, and reference frequency ranges: 10% signal amplitude variation, and 10% harmonic distortion (for values without a tolerance already specified).

PARAMETER	VALUE	UNITS
MOISTURE SENSITIVITY LEVEL	Level 2 Tested in accordance with JEDEC SPEC J-STD-020	
PHYSICAL CHARACTERISTICS		
Size: 64-pin Quad Flat Pack	0.52 x 0.52 (13.2 x 13.2)	in. (mm)
Weight	0.018 0.5	oz. (g)

Notes:

1. As parallel resolution is reduced, pairs of bits are disabled. (Unused bits are set to a logic "0.")
 - 14 bit resolution: 15/16 disabled,
 - 12 bit resolution: 13/14, 15/16 disabled,
 - 10 bit resolution: 11/12, 13/14, 15/16 disabled
2. In LVDT mode, Bit 3 is the MSB and resolution is programmable to 8, 10, 12, and 14 bits.
3. Accuracy calculation for LVDT mode is described in Section 17.1
4. In the frequency range of 47Hz to 1kHz, there will be 1 LSB of jitter at quadrant boundaries.
5. The maximum phase shift tolerance will degrade linearly from 45 degrees at 400 Hz to 30 degrees at 60 Hz.
6. When using the -5V inverter, the VDD supply current will double and VSSP can be up to 20% low, or -4V.
7. || = in parallel with.
8. High Z refers to parallel data only.
9. Normal ESD (Electro Static Device) handling precautions should be observed.
10. Any unused pins may be left floating (unconnected). All TTL & CMOS input pins are internally pulled up to +5 Volts.
11. A signal less than 500 mVrms will assert BIT.
12. For Ka definition, see the RD/RDC application manual acceleration lag section.
13. When in overload condition, the converter will not operate to specification and will not be damaged.

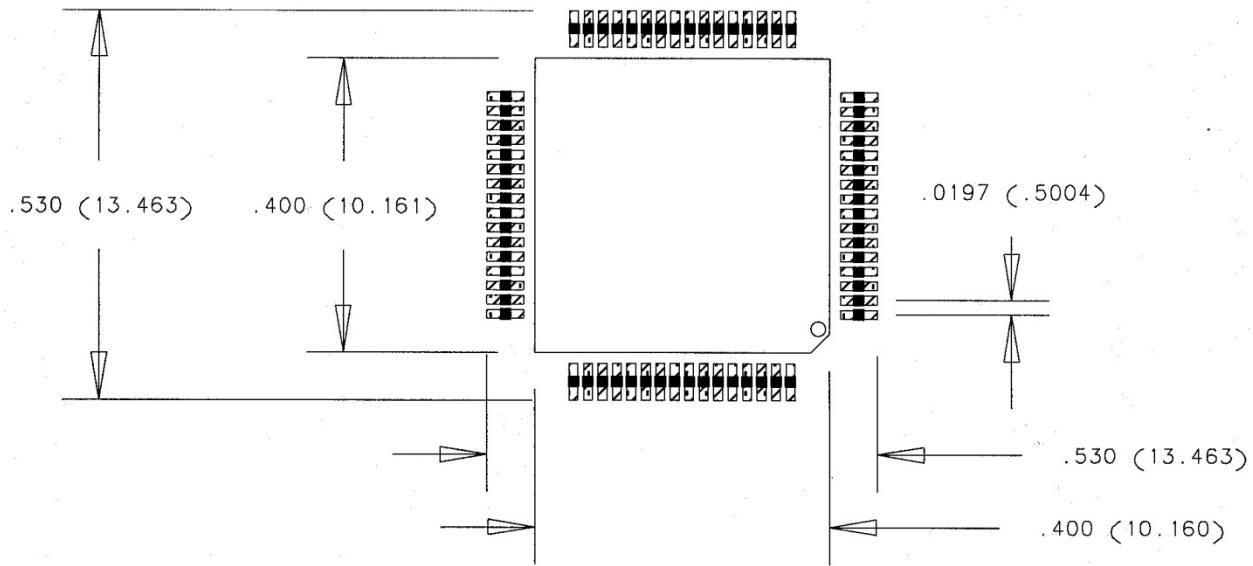
Table 2. RD-19231 Pinouts & Descriptions

#	Name	Description	#	Name	Description
1	VEL	Analog Velocity Output	33	VL	Voltage Logic Set to 3.3V or 5V
2	-VCO	Negative VCO input	34	N/C	No Connect
3	SJ1	Install Bandwidth 1 Components	35	Bit 9	Binary Data Out
4	SJ2	Install Bandwidth 2 Components	36	Bit 2	Binary Data Out
5	SHIFT	Selects VEL1 /VEL2 BW Components	37	Bit 10	Binary Data Out
6	VEL2	VEL2 Bandwidth Components	38	Bit 3	Binary Data Out
7	TP1 (Demod)	No Connect	39	Bit 11	Binary Data Out
8	VEL 1	VEL1 Bandwidth Components	40	Bit 4	Binary Data Out
9	TP2 (EDC)	No Connect	41	N/C	No Connect
10	+C	Positive Analog Input of Cosine	42	Bit 12	Binary Data Out
11	COS	Cosine for Gain Setup	43	Bit 5	Binary Data Out
12	-C	Negative Analog Input of Cosine	44	Bit 13	Binary Data Out
13	+S	Positive Analog Input of Sine	45	Bit 6	Binary Data Out
14	SIN	Sine for Gain Setup	46	Bit 14	Binary Data Out
15	-S	Negative Analog Input of Sine	47	Bit 7	Binary Data Out
16	VSS (-5V)	Negative 5V Supply Connection	48	Bit 15	Binary Data Out
17	VSS (-5V)	Negative 5V Supply Connection	49	Bit 8	Binary Data Out
18	TP3 (test point)	No Connect	50	Bit 16 (LSB)	Binary Data Out
19	R CLK	Resistor for Selection of Sample Rate	51	A (LSB +1)	Encoder Output A
20	R SET	Resistor for Selection of Internal Current	52	DSR	Digital Synthesized Reference Disable
21	ENM	Latch Enable of 8 Most Significant Data Bits	53	N/C	No Connect
22	AGND	Analog Ground Connection	54	N/C	No Connect
23	VSSP	Power Setup for Internal -5V Charge Pump	55	ZIP_EN	Select Pin for CB (ZI) Pin 31
24	NCAP	Filter Capacitor for Internal -5V Charge Pump	56	TP4 (test point)	No Connect
25	GND	Digital Ground Connection	57	ENL	Latch Enable of 8 Least Significant Data Bits
26	PCAP	Filter Capacitor for Internal -5V Charge Pump	58	VDD (+5V)	Positive 5V Power Connection
27	VDDP	Power Setup for Internal -5V Charge Pump	59	UP / DN	Programs the gain of pre-charged Bandwidth components
28	BIT	Built-In-Test Output	60	D0	Resolution Control
29	U/B	U indicates direction of encoder output -OR- Encoder Output B	61	D1	Resolution Control
30	A_QUAD_B	Input Enable for Encoder Mode	62	INH	Inhibit Latch
31	CB (ZI)	Converter Busy -OR- Zero Index Pulse	63	RH	Reference High Input
32	Bit 1 (MSB)	Binary Data Out	64	RL	Reference Low Input

Notes:

1. See Figure 9 for -5V only operation.

2. Unless otherwise specified, pins TP1 through TP4 are for factory use only
 3. N/C means no internal wire connection.



PAD SIZE .012X.050 IS IN INCHES
DIMENSION ARE IN INCHES (MM)

Figure 4. RD-19231 Suggested Footprint

3 THEORY OF OPERATION

The RD-19231 is a mixed signal CMOS IC containing analog input and digital output sections. Precision analog circuitry is merged with digital logic to form a complete high-performance tracking resolver-to-digital converter. For user flexibility and convenience, the converter bandwidth, dynamics, and velocity scaling are externally set with passive components.

The RD-19231 Functional Block Diagram is shown in Figure 2. The analog conversion electronics require ± 5 VDC power supplies, and the converter contains a charge pump to provide the user with the option of a single-ended +5 VDC supply. The converter front-end consists of differential sine and cosine input amplifiers which are protected up to ± 25 V with $2\text{ k}\Omega$ resistors and diode clamps to the ± 5 VDC supplies. The reference input is also protected to ± 25 V with $2\text{ k}\Omega$ resistors and diode clamps to the ± 5 V DC supplies. By performing the following trigonometric identity, $\text{SIN}\theta (\text{COS}\phi) - \text{COS}\theta (\text{SIN}\phi) = \text{SIN}(\theta-\phi)$, the Control Transformer (CT) compares the analog input signals (θ) with the digital output (ϕ), resulting in an error signal proportional to the sine of the angular difference. The CT uses a combination of amplifiers, switches, logic and capacitors in precision ratios to perform the calculation.

Note: *The error output of the CT is normally sinusoidal, but in LVDT mode, it is triangular (linear) and can be used to convert any linear transducer output.*

The converter accuracy is limited by the precision of the computing elements in the CT. Instead of a traditional precision resistor network, this converter uses capacitors with precisely controlled ratios. Sampling techniques are used to eliminate errors due to voltage drift and op-amp offsets.

The error processing is performed using the industry standard technique for Type II tracking converters. The DC error is integrated yielding a velocity voltage which in turn drives a voltage controlled oscillator (VCO). This VCO is an incremental integrator (constant voltage input to position rate output) which, together with the velocity integrator, forms a Type II servo feedback loop. A lead in the frequency response is introduced to stabilize the loop and another lag at higher frequency is introduced to reduce the gain and ripple at the carrier frequency and above. The settings of the various error processor gains and break frequencies are done with external resistors and capacitors so that the converter loop dynamics can be easily controlled by the user.

4 TRANSFER FUNCTION AND BODE PLOT

The dynamic performance of the converter can be determined from its Transfer Function Block Diagrams and Bode Plots (open and closed loop). These are shown in Figure 5, Figure 6, and Figure 7.

The open loop transfer function is as follows:

$$\text{Open Loop Transfer Function} = \frac{A^2 \left(\frac{S}{B} + 1 \right)}{S^2 \left(\frac{S}{10B} + 1 \right)}$$

where A is the gain coefficient and $A^2 = A_1 A_2$
and B is the frequency of lead compensation.

The components of gain coefficient are error gradient, integrator gain, and VCO gain. These can be broken down as follows:

- Error Gradient = 0.011 volts per LSB (CT + Error Amp + Demod
with 2 Vrms input)

- Integrator Gain = $\frac{C_s F_s}{1.1 C_{BW}}$ volts per second per volt

- VCO Gain = $\frac{1}{1.25 R_v C_{VCO}}$ LSBs per second per volt

where: $C_s = 10 \text{ pF}$

$F_s = 67 \text{ kHz}$ when $R_{CLK} = 30 \text{ k}\Omega$

$C_{VCO} = 50 \text{ pF}$

R_v , R_B , and C_{BW} are selected by the user to set velocity scaling and bandwidth.

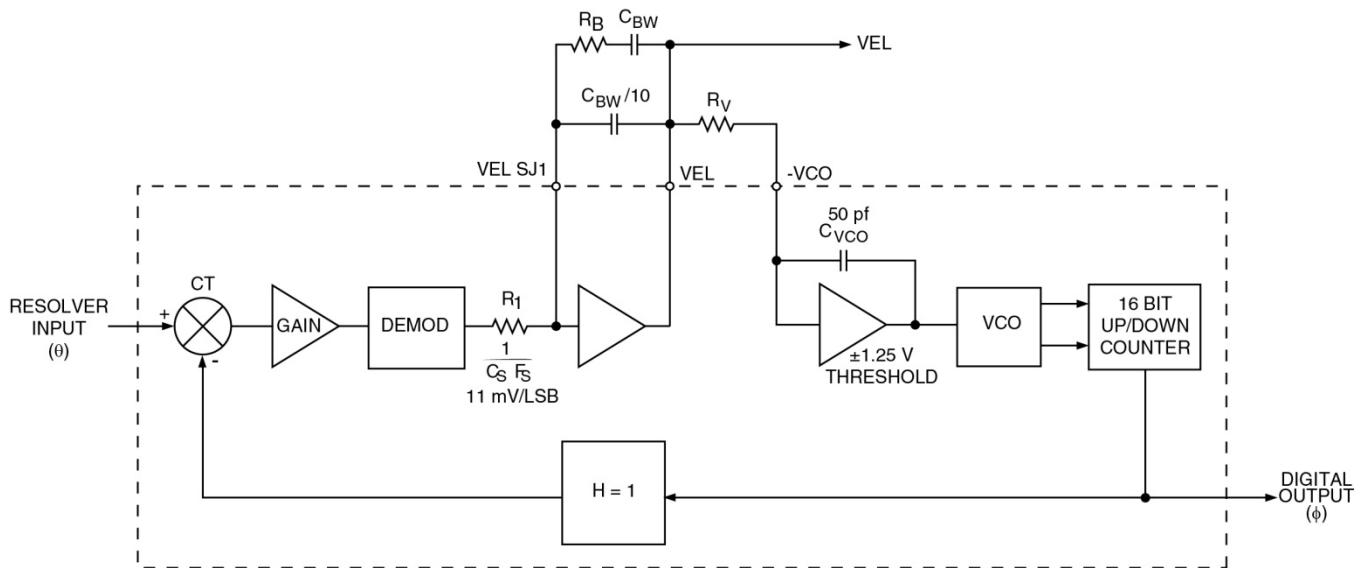


Figure 5. Transfer Function Block Diagram #1

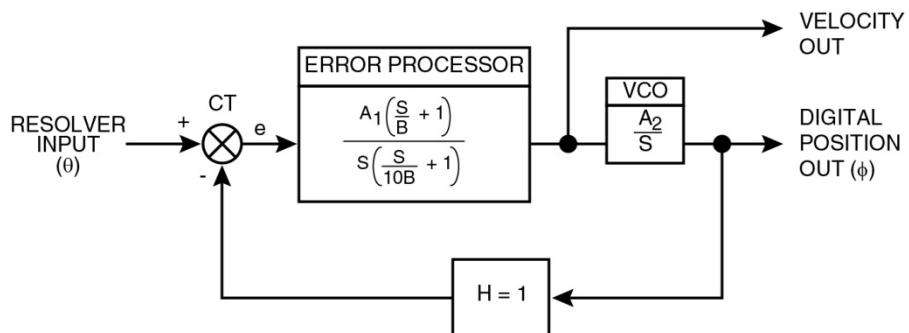


Figure 6. Transfer Function Block Diagram #2

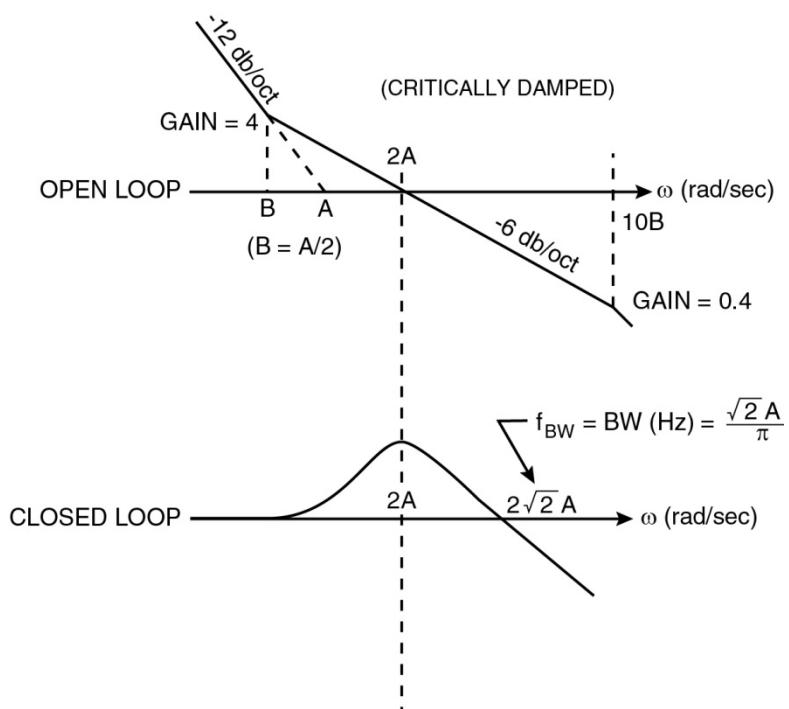


Figure 7. Bode Plots

5 GENERAL SETUP CONDITIONS

Note: For detailed application and technical information see the RD/RDC converter applications manual which is available for download from the DDC web site at www-ddc-web.com.

DDC has external component selection software which considers all the criteria below. In a simple fashion, it asks the key system parameters (carrier frequency, resolution, bandwidth, and tracking rate) needed to derive the external component values.

The following recommendations should be considered when installing the RD-19231 R/D converter:

1) External VDD, VSS & VL Operation:

The RD-19231 requires VDD, VSS and VL supply voltages. Connect the VDD pin to +5 VDC. Connect the VSS pin to -5 VDC. VL is the voltage control for the I/O digital output pins, set pin VL to +5VDC for 5VDC outputs or set VL pin to 3.3VDC for 3.3VDC outputs. For improved supply noise immunity it is recommended that a 0.1 μ F or larger cap be connected from each supply to ground near the converter package. When using an external -5V, VSS supply to power the converter, pins VSSP, NCAP, PCAP and VDDP should be left floating.

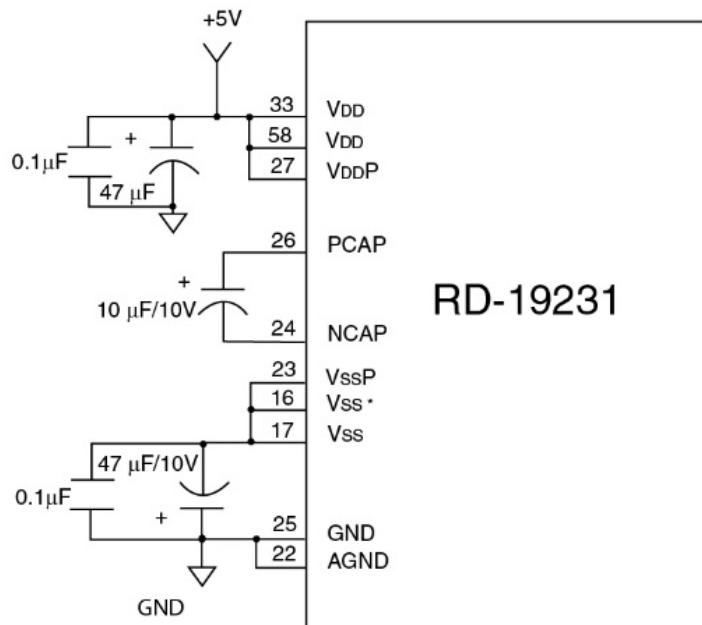
2) External VDD, VL Operation:

The RD-19231 has an -5V inverter. VDDP is the inverter input. VSSP is the inverter output. NCAP and PCAP are the pins that provide connection to the positive and negative terminals of an external switching capacitor.

Using the -5V Inverter will eliminate the need for an external -5V, VSS supply. Capacitor values can be altered to accommodate board space or system noise. Refer to Figure 8 for necessary connections.

The -5V output voltage is dependent on losses due to capacitor ESR and any drops seen at the VDDP input. If the VSSP output is less than 15% of the VSS nominal voltage, the Velocity output scaling may need to be less than the nominal 4V at full scale to avoid saturation.

For example, the maximum tracking rate can be scaled for a full-scale velocity output of 3.5 V max using RV calculation in Step 7 below.



* Pin 16 has been renamed Vss since it will typically be connected to -5 VDC. Applications requiring a differential front-end configuration must connect this pin to Vss. Voltage follower mode should also be implemented with pin 16 tied to Vss by making external connections between the output of the SIN/COS amplifiers and their respective inputs. When left unconnected, the RD-19231 will internally configure the front-end amplifiers in voltage follower mode.

Figure 8. -5V Inverter Connections

3) **Ground PCB Routing :**

The RD-19231 provides separate analog GND (pin 22) and Power GND (Pin 25) to allow for a separate ground current path. The AGND and GND pins must be tied together as close to the package as possible. It is recommended that a low impedance PCB GND plane be used as a common ground.

If the GND plane is not feasible AGND and GND pins must be tied together as close to the package as possible but the returns/grounds for the resolver input should be routed separately to the AGND. This remote sensing of AGND removes any digital or power supply currents from the input signal path and will minimize effects of digital and power supply noise.

4) **Analog Signal Routing**

This device has several high impedance amplifier inputs (+C, -C, +S, -S, -VCO, VEL SJ1, and VEL SJ2) that are sensitive to capacitive coupling through parallel input PCB traces. External components should be connected as close to the converter as possible. The PCB traces that cross these inputs should be kept to a minimum to avoid capacitive coupling via stray capacitance.

5) Sin/Cos Resistor configuration selection:

The analog input error is derived from the trigonometric identity, $\text{SIN}\theta (\text{COS}\phi) - \text{COS}\theta (\text{SIN}\phi) = \text{SIN}(\theta-\phi)$. Any matching errors in the Sin, Cos passive input components will introduce position errors in the converter. DDC has a number of standard input thin films that are designed and tested for .02% tolerance, see Section 18, Thin-Film Resistor Networks for Motion Feedback Products.

6) Tracking Rate and Bandwidth System Considerations:

In selecting the bandwidth (BW) and Tracking Rate (TR), the system requirements need to be considered. The tracking rate is defined as the maximum angular speed for which the converter output will be able to keep track with the input. The tracking rate should be set fast enough to support the system's maximum angular speed, but it should not be set excessively high since it dictates the minimum bandwidth, see Table 3.

Selecting a bandwidth frequency, f_{BW} , which is too low relative to the application's maximum tracking rate can create a spin-around condition in which the converter never settles. The relationship to insure against this condition is detailed in Table 3.

For the greatest noise immunity, select the minimum BW and TR the system will allow.

General rule of thumb is Carrier frequency $\geq 3.5 * \text{selected Bandwidth frequency}$ and the selected tracking rate should not exceed the ratio indicated in Table 3.

Table 3. Tracking/BW Relationship	
RPS (MAX)/BW	Resolution
1	10
0.50	12
0.25	14
0.125	16

7) Bandwidth and Velocity scaling calculation for the optimized critically damped case:

DDC has external component selection software which considers the entered system criteria and indicates warnings if the recommendations or converter capability is exceeded. In a simple fashion, it asks the key system parameters (carrier frequency, resolution, bandwidth, and tracking rate) and calculates the external component values using the equations listed below.

Visit our web site at www.ddc-web.com to download software. The following calculations are provided for reference only.

- Select the desired f_{BW} (closed loop) based on overall system dynamics.
- Select $f_{carrier} \geq 3.5f_{BW}$
- Select the applications tracking rate (in accordance with TABLE 3), and use appropriate values for R_{SET} and R_{CLK}
- Compute $R_v = \frac{\text{Full Scale Velocity Voltage}}{\text{Tracking Rate (rps)} \times 2 \text{ resolution} \times 50 \text{ pF} \times 1.25 \text{ V}}$
- Compute $C_{BW} (\text{pF}) = \frac{3.2 \times F_s (\text{Hz}) \times 10^8}{R_v \times (f_{BW})^2}$
- Where $F_s = 67 \text{ kHz}$ for $R_{CLK} = 30 \text{ k}\Omega$
 100 kHz for $R_{CLK} = 20 \text{ k}\Omega$
 125 kHz for $R_{CLK} = 15 \text{ k}\Omega$
- (F_s = Internal Sample Frequency)
- Compute $R_B = \frac{0.9}{C_{BW} \times f_{BW}}$
- Compute $\frac{C_{BW}}{10}$

As an example:

Calculate component values for a 16-bit converter with 100Hz bandwidth, a tracking rate of 10 RPS and a full scale velocity of 4 Volts.

- $R_v = \frac{4 \text{ V}}{10 \text{ rps} \times 2^{16} \times 50 \text{ pF} \times 1.25 \text{ V}} = 97655 \text{ }\Omega$
- Compute $C_{BW} (\text{pF}) = \frac{3.2 \times 67 \text{ kHz} \times 10^8}{97655 \times 100 \text{ Hz}^2} = 21955 \text{ pF}$
- Compute $R_B = \frac{0.9}{21955 \times 10^{-12} \times 100 \text{ Hz}} = 410 \text{ k}\Omega$

Note: For detailed application and technical information see the RD/RDC converter applications manual which is available for download from the DDC web site at www-ddc-web.com.

6 HIGHER TRACKING RATES AND CARRIER FREQUENCIES

Maximum tracking rate is limited by the velocity voltage saturation (nominally 4 V) and the maximum internal clock rate (nominally 1,333,333 Hz for R CLK = 30k). To achieve higher tracking rates, a higher internal counting rate must be programmed by setting RCLK to a value less than 30k. See Table 4 for the appropriate values.

The Rv resistor and an internal 50pF capacitor are configured as an integrating circuit that resets to zero after a count occurs in either direction. This circuit acts as a VCO with velocity as its input and CB as its output. The Rv resistor and an internal 50pF capacitor determine the maximum rate of the VCO.

Rv must be chosen such that the maximum rate of the VCO is less than the maximum internal clock rate. Choose the tracking rate in accordance with Table 4 to insure this relationship. The rates shown in Table 4 are based on ~90% of the nominal internal clock rate.

The relationship between the velocity voltage and the VCO rate is given by:

$$\frac{\text{Velocity Voltage}}{\text{VCO Frequency}} = \frac{1}{(\text{Rv} \times 50 \text{ pF} \times 1.25)}$$

Table 4. Max Tracking Rate in RPS					
Rset (Ω)	RCLK (Ω)	Resolution			
		10	12	14	16
30k	30k	1152	288	72	18
23k	20k	1728	432	108	27
23k	15k	2176	544	136	34

All dynamic production testing is performed with Rclk = 30K

Maximum tracking rate where Rclk = 20K or 15K are achievable by design, but are not production tested.
Consult DDC for custom screening or setup verification.

The use of 1% or better tolerance resistors is recommended.

6.1 Higher Carrier Frequencies

Select Rclk/Rset to operate at the frequency/resolution indicated in Table 5 then Cross-reference Table 4 for max tracking rate.

		Table 5. Carrier Frequency (max) in KHZ			
Rset (Ω)	RCLK (Ω)	Resolution			
		10	12	14	16
30k	30k	10	10	7	4
23k	20k	10	10	10	7
23k	15k	10	10	10	10

All accuracy testing is performed with Rset = 30k, Rclk = 30k, with carrier frequency = 2.5 kHz.

Maximum operating carrier frequency is achievable by design, but is not tested. Consult DDC for custom screening or setup verification.

The use of 1% or better tolerance resistors is recommended.

7 OPTIONAL BANDWIDTH COMPONENTS

The RD-19231 provides the option of using a second set of bandwidth components. The second set of components can be used for switch-on-the-fly or dual-bandwidth applications. The SHIFT and $\overline{\text{UP}}/\text{DN}$ inputs are used when switching bandwidth components, and their operation is described below. Refer to the block diagram, Figure 2.

7.1 Shift

The SHIFT pin is an input that chooses between the VEL1 and VEL2 bandwidth components. This pin has an internal pull-up to +5V. When the SHIFT pin is left open, or a logic 1 is applied, the VEL1 components are selected. When a Logic 0 is applied, the VEL2 components are selected. The deselected set of bandwidth components are driven by an amplifier, with programmable gain, that follows the velocity amplifier. This amplifier can be used to precharge the deselected set of components to the voltage level that is expected after a change in resolution. (See Section 13.)

7.2 $\overline{\text{UP}}/\text{DN}$

The $\overline{\text{UP}}/\text{DN}$ input selects the gain of the amplifier driving the de-selected set of bandwidth components. $\overline{\text{UP}}/\text{DN}$ has three input states. See Table 6 to relate input to gain.

Table 6. Precharge Amplifier Gain Programming

$\overline{\text{UP}}/\text{DN}$	Gain	Function
Logic 0	4	preset resolution to increase
Logic 1	$\frac{1}{4}$	preset resolution to decrease
-5V	1	dual bandwidth

8 INPUT CONFIGURATIONS

The Sine and Cosine amplifiers should be configured for a full-scale nominal amplitude of 2 VRMS. This amplitude can be measured for Resolver/Synchro applications at the converter's Sine output at position 90° & 270°. The converter bandwidth calculation is derived based on this 2VRMS nominal voltage and will vary linearly with this full scale amplitude. The Sin/Cos amplifier I/O pins are accessible allowing for a multitude of custom input configurations and line to line voltages.

The rated converter accuracy indicated in Table 1, assumes ideal gain matching, ASin/ACos = 1. The implementation of thin film resistor gain or input transformer will contribute error to the converter. DDC provides a selection of thin films that are designed for typical Synchro/Resolver sensors and are optimized for up to 16 bit resolution, see Section 18.

Sin/Cos Gain Error Estimation

1 LSB in 16 bit resolution, ASin/ACos = 1.0002

1 LSB in 14 bit resolution, ASin/ACos = 1.0008

1 LSB in 12 bit resolution, ASin/ACos = 1.0031

1 LSB in 10 bit resolution, ASin/ACos = 1.012

The converter input can be configured using either transformers, 0.1% tolerance resistors or DDC thin film networks per the tables and Figures 12 and Figure 13.

Typical Inputs

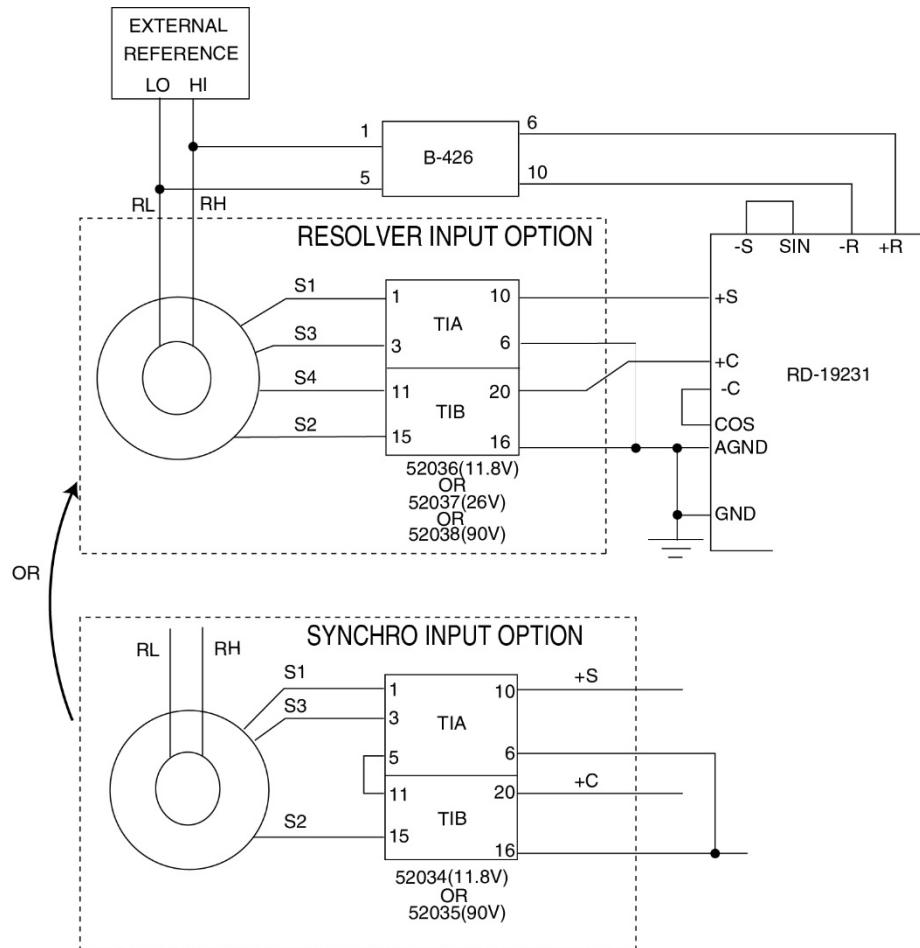
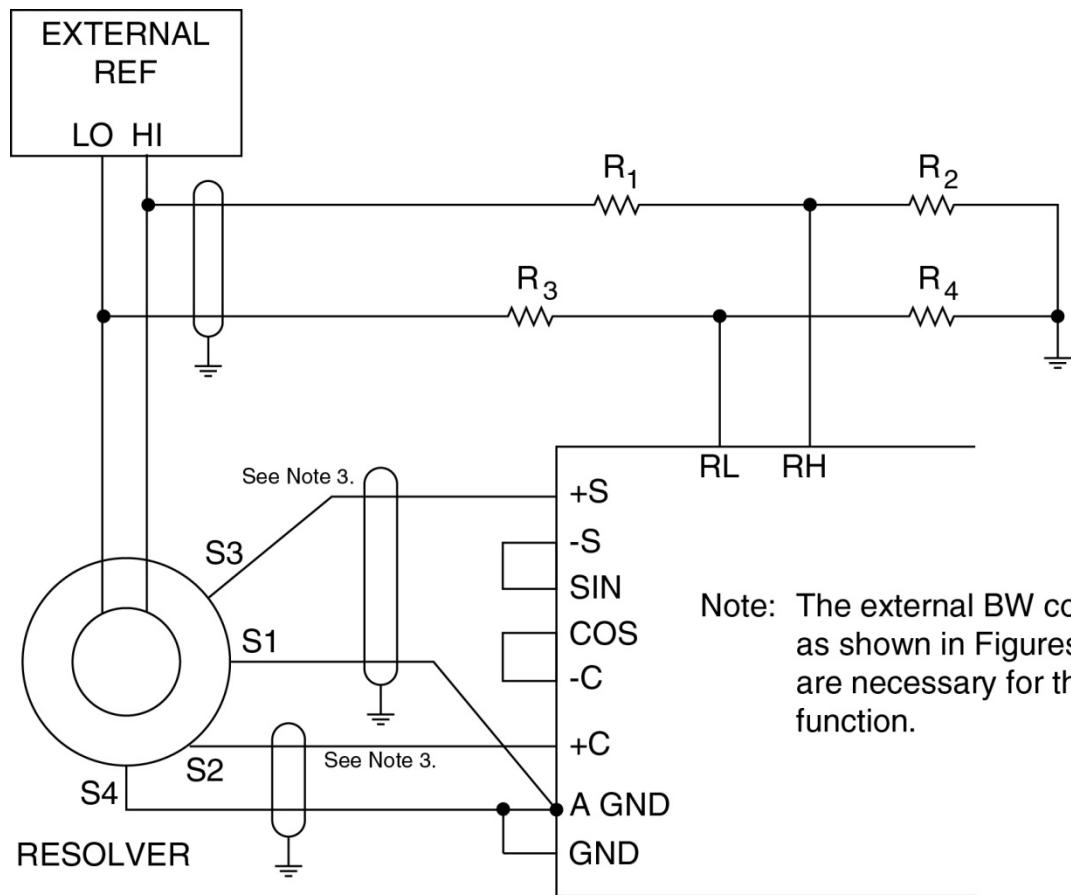


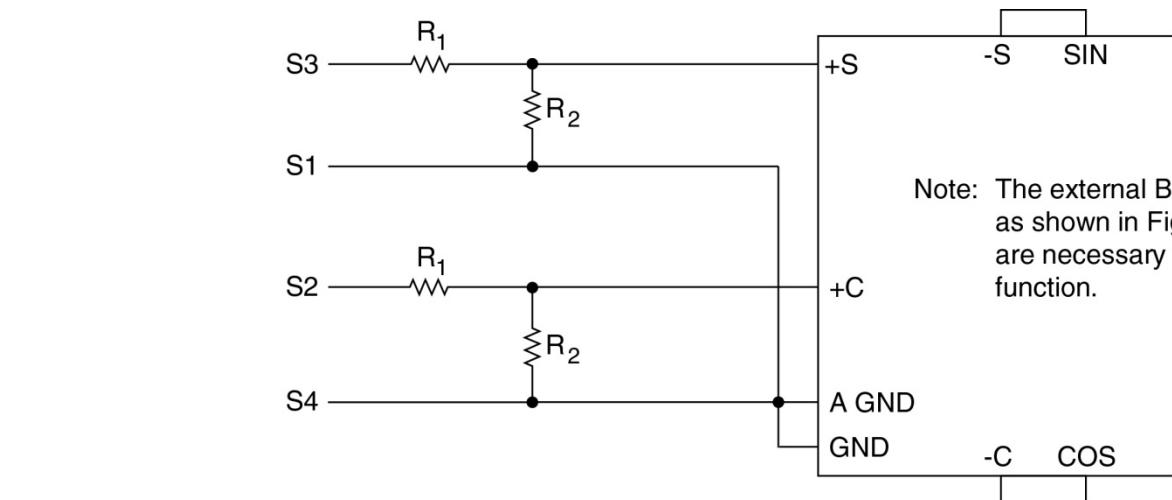
Figure 9 through Figure 13 illustrate typical input configurations.

Figure 9. Typical Transformer Connections



- 1) Resistors selected to limit Vref peak to between 1.5 V and 5 V.
- 2) External reference LO is grounded, then R3 and R4 are not needed, and -R is connected to GND.
- 3) 10k ohms, 1% series current limit resistors are recommended.

Figure 10. Typical Connections, 2V Resolver, Direct Input

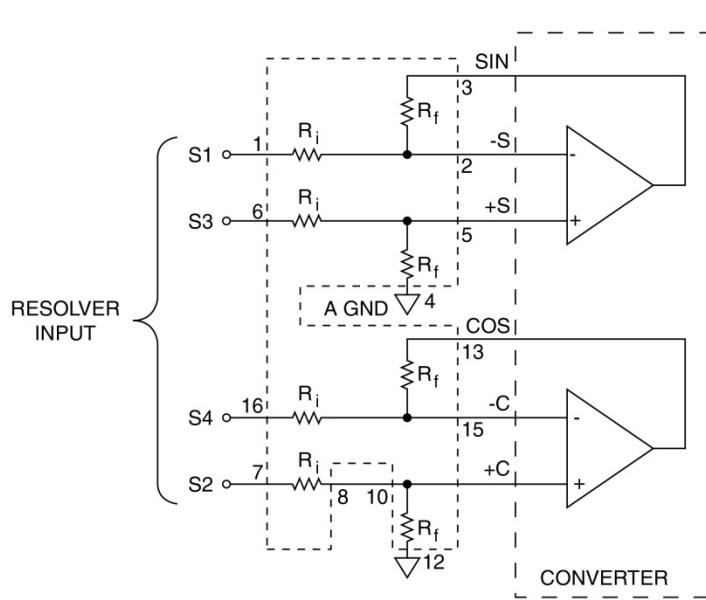


$$\frac{R_2}{R_1 + R_2} = \frac{2}{X \text{ Volt}}$$

$R_1 + R_2$ should not load the Resolver; it is recommended to use an $R_2 = 10 \text{ k}\Omega$

$R_1 + R_2$ Ratio errors will result in Angular errors,
2 cycle, 0.1% Ratio error = 0.029° Peak Error.

Figure 11. Typical Connections, X-Volt Resolver, Direct Input

Examples of Component Calculations:(1) 2V in, need gain of 1, use 10k for R_f & R_i
Gain = $\frac{R_f}{R_i}$ (2) 4V in, need gain of 0.5, $R_i = 20k$, $R_f = 10k$ To Calculate R_i :Select 10k for R_f

$$R_i = R_f \times 0.5 \text{ (input L-L volt)}$$

$$R_i = 10k \times 0.5 \times (L-L \text{ volt})$$

Note: The external BW components as shown in Figures 1 and 2 are necessary for the R/D to function.

See figure 6 for op amp configuration.

S1 and S3, S2 and S4, and RH and RL should be ideally twisted shielded, with the shield tied to GND at the converter.

For DDC-49530: $R_i = 70.8 \text{ k}\Omega$, 11.8 V input, synchro or resolver.

For DDC-49590: $R_i = 270 \text{ k}\Omega$, 90 Volt input, synchro or resolver.

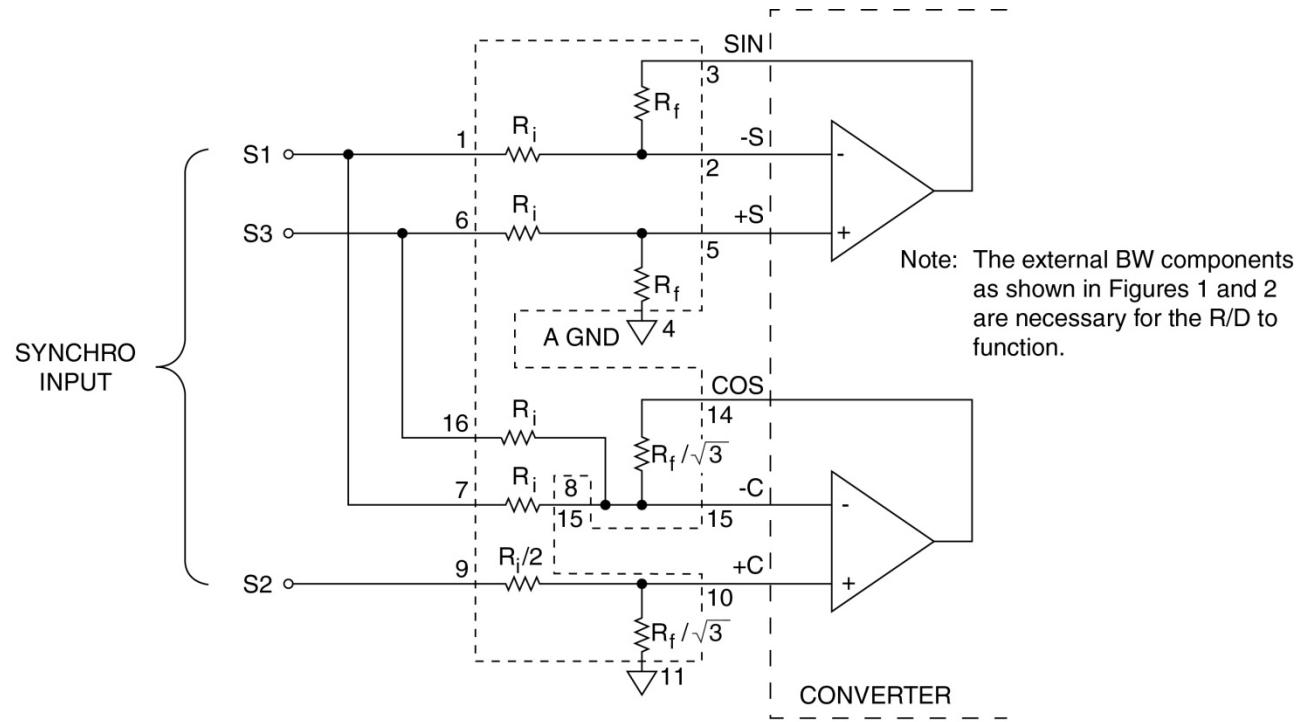
Maximum additional error is 1 LSB using recommended thin film packages.

When using discrete resistors: Resolver L-L voltage = $\frac{R_i}{R_f} \times 2 \text{ Vrms}$, where $R_f \geq 6 \text{ k}\Omega$.

For 2V direct input, use 10kΩ matched resistors for R_i and R_f .

Input options affect DC offset gains and therefore carrier frequency ripple and jitter. Offset gains associated with differential mode (offset gain for differential configuration = $1+R_f/R_i$) and direct mode (offset gain for direct configuration = 1) show differential mode will always be higher. Higher DC offsets cause higher carrier frequency ripple due to the demodulation process. This carrier frequency ripple rides on top of the DC error signal, causing jitter. A higher carrier frequency versus bandwidth ratio will help to decrease ripple and jitter associated with offsets. In summary, R/Ds with differential inputs are more susceptible to offset problems than R/Ds in single-ended mode. R/Ds in higher resolutions, such as 16 bit, will further compound offset issues due to higher internal voltage gains. Although the differential configuration has a higher DC offset gain, the differential configuration's common mode noise rejection makes it the preferred input option. The tradeoffs should be considered on a design to design basis. Also refer to FAQ-GIQ-021.

**Figure 12. Differential Resolver Input
Using DDC-49530/57470 (11.8V) or DDC-49590 (90 V), DDC-82620 (2V)
Using Discrete Resistors**



See figure 5 for op amp configuration.

S1, S2, S3 should be triple twisted shielded; RH and RL should be twisted shielded;

In both cases the shield should be tied to GND at the converter.

11.8 Volt input = DDC-49530: $R_i = 70.8 \text{ k}\Omega$, 11.8 V input, synchro or resolver.

90 Volt input = DDC-49590: $R_i = 270 \text{ k}\Omega$, 90 Volt input, synchro or resolver.

Maximum additional error is 1 LSB using recommended thin film package.

When using discrete resistors: Resolver L-L voltage = $\frac{R_i}{R_f} \times 2 \text{ Vrms}$, where $R_f \geq 6 \text{ k}\Omega$

**Figure 13. Synchro Input
Using DDC-49530-57470 (11.8V), DDC-49590 (90V)**

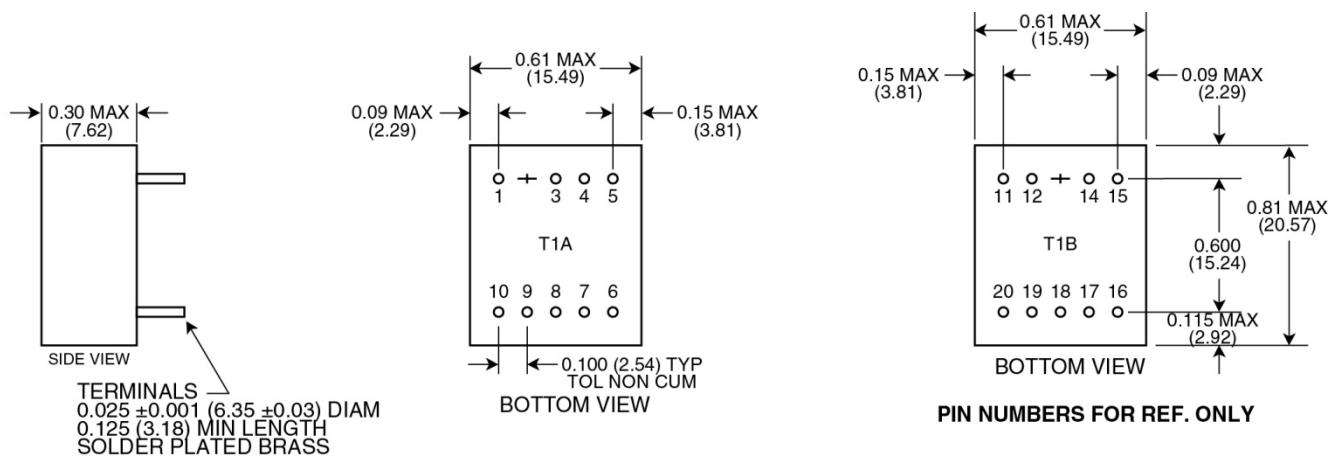
9 INPUT TRANSFORMERS

Refer to Table 7 to select the proper transformer for Reference, Synchro and Resolver inputs.

Table 7. Transformers									
P/N	Type	Frequency (Hz) (note1)	IN (Vrms) (note 1)	OUT (Vrms) (note 2)	Angle Accuracy (note 3)	Length (in)	Width (in)	Height (in)	Figure
52034	S – R	400	11.8	2	1	0.81	0.61	0.3	Figure 14
52035	S – R	400	90	2	1	0.81	0.61	0.3	Figure 14
52036	R – R	400	11.8	2	1	0.81	0.61	0.3	Figure 15
52037	R – R	400	26	2	1	0.81	0.61	0.3	Figure 15
52038	R – R	400	90	2	1	0.81	0.61	0.3	Figure 15
B-426	Reference	400	115	3.4	N/A	0.81	0.61	0.32	Figure 16
24133-X	Reference	60	115	3/6 (note 4)	N/A	1.125	1.125	0.42	Figure 17

Notes:

1. ±10% Frequency (Hz) and Line-to-Line input voltage (Vrms) tolerances
2. 2 Vrms Output Magnitudes are -2 Vrms ±0.5% full scale
3. Angle Accuracy (max minutes)
4. 3 Vrms to ground or 6 Vrms differential (±3% full scale)
5. Dimensions are for each individual main and teaser
6. 60 Hz Synchro transformers are active (requires ±15 Vdc power supplies)
7. 400 Hz transformer temperature range: -55°C to +125°C
8. 60 Hz transformer (24133-X) temperature ranges: add to part number -1 or -3
(-1 = -55°C to +85°C, -3 = 0°C to +70°C)
9. The following transformers can be ordered directly from DDC, Tel (631) 567-5600:
P/N 24133-X
10. The following transformers can be ordered directly from Beta Transformer Technology Corporation (BTTC),
Tel (631) 224-7393:
P/N 52034, 52035, 52036, 52037, 52038, and B-426



Dimensions are shown in inches (mm).

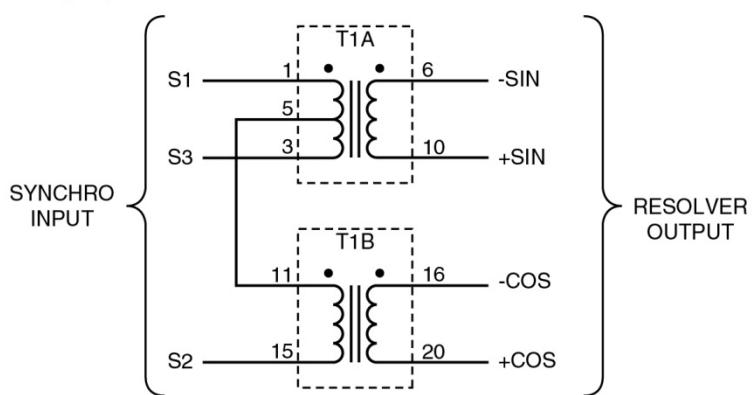
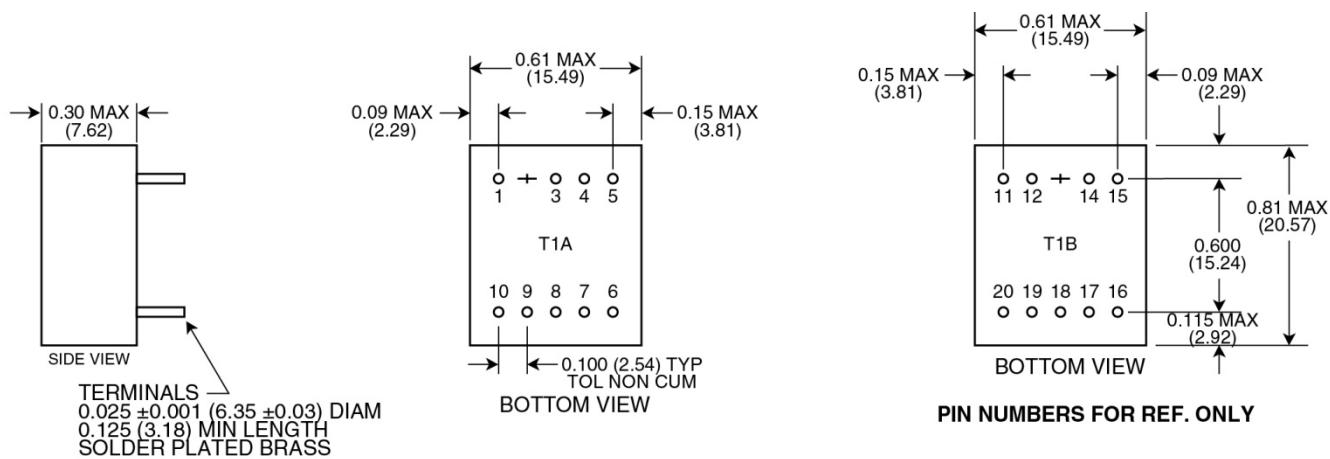


Figure 14. Transformer Layout and Schematic (Synchro Input – 52034/52035)



Dimensions are shown in inches (mm).

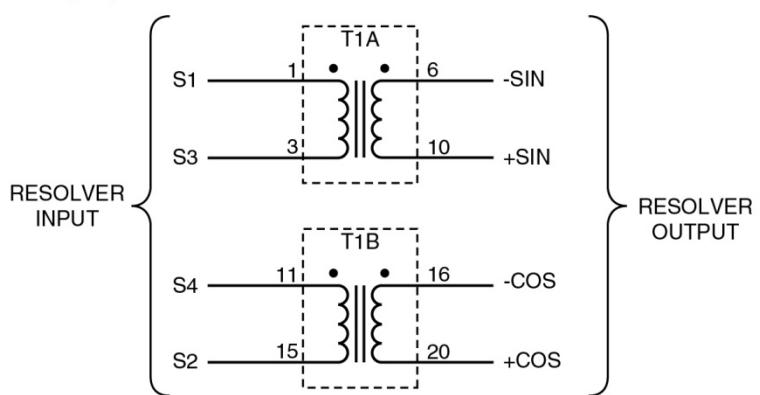
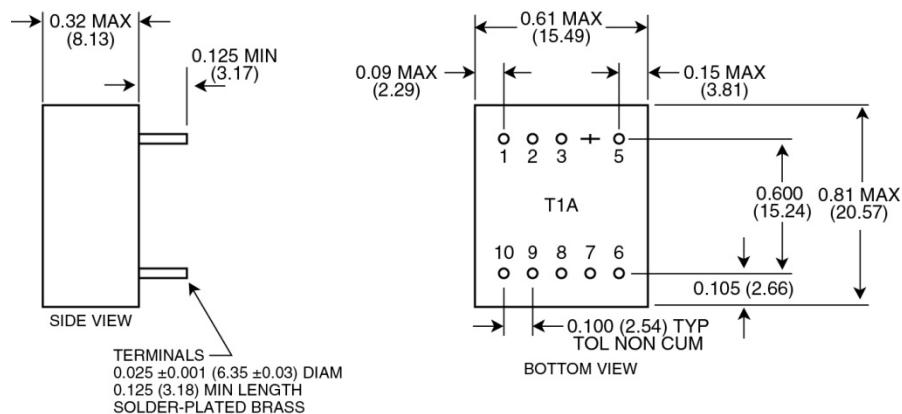


Figure 15. Transformer Layout and Schematic (Resolver Input – 52036/52037/52038)



Dimensions are shown in inches (mm).

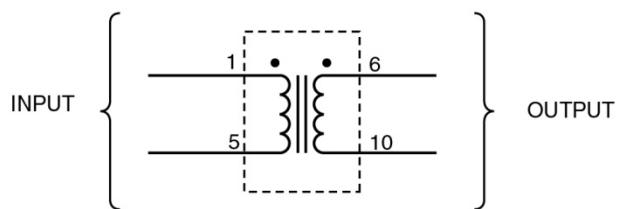


Figure 16. Transformer Layout and Schematic (Reference Input – B-426)

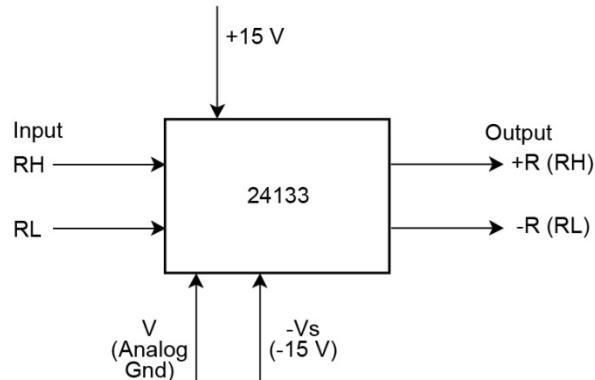
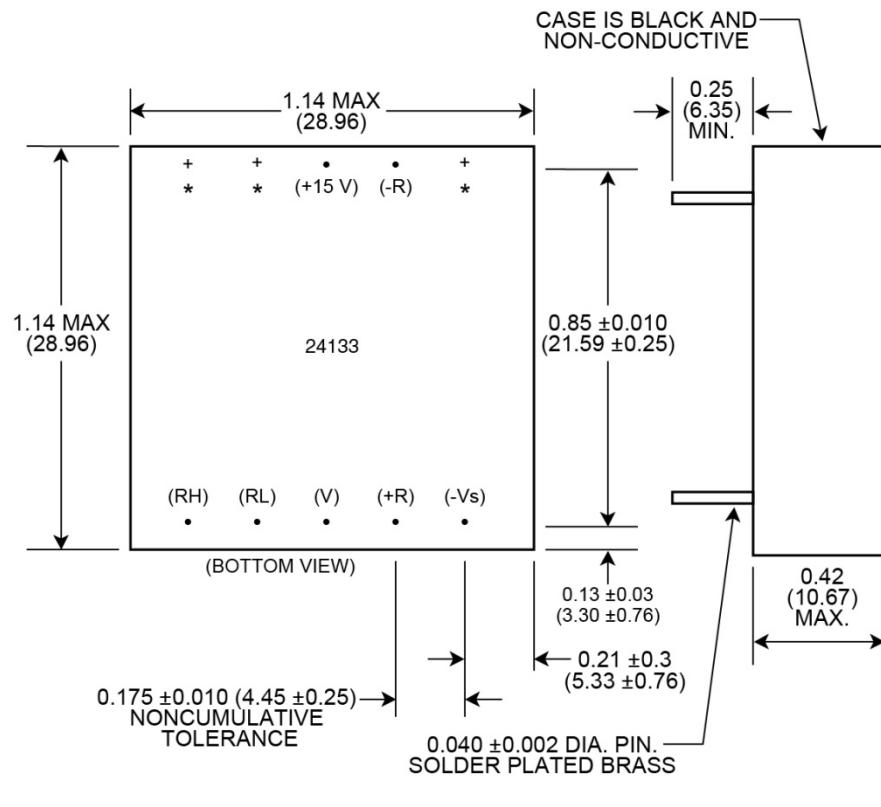
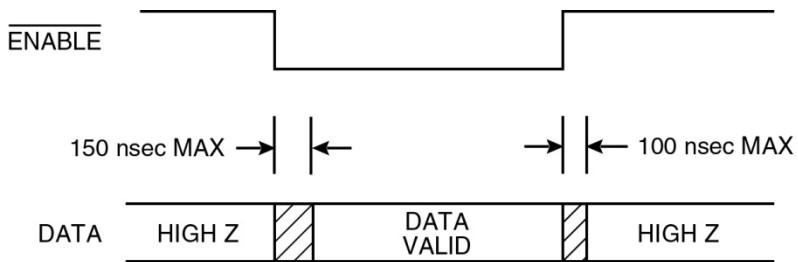


Figure 17. 60 Hz Reference Transformer Diagram (Reference Input – 24133)

10 INHIBIT, ENABLE, AND CB TIMING

The Inhibit (INH) signal is used to freeze the digital output angle in the transparent output data latch while data is being transferred. Application of an Inhibit signal does not interfere with the continuous tracking of the converter.

Output angle data is enabled onto the tri-state data bus in two bytes. Enable MSBs (EM) is used for the most significant 8 bits and Enable LSBs (EL) is used for the least significant 8 bits. As shown in Figure 18, output data is valid 150 ns maximum after the application of a negative enable pulse. The tri-state data bus returns to the high impedance state 100 ns maximum after the rising edge of the enable signal.



For 16-bit bus, EM/EL may be tied to ground for transparent mode, as long as only 1 R/D channel is used on the data bus.

Figure 18. Enable Timing

The Converter Busy (CB) signal indicates that the tracking converter output angle is changing 1 LSB.

10.1 16 Bit Data Read/Timing Setup

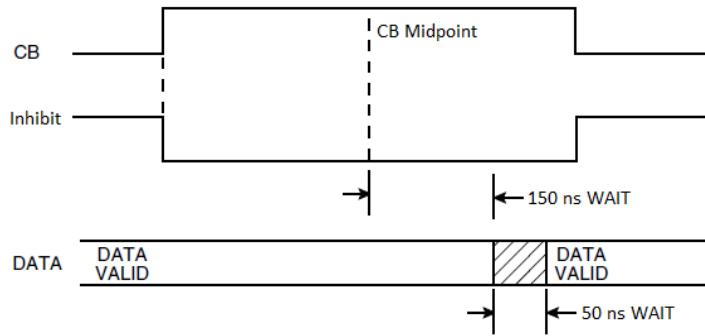


Figure 19. 16 Bit Data Read

For 16 Bit Data Read, EM/EL set low/ground.

Set inhibit low on CB start edge. Calculate inhibit wait time for when a valid data read can be done.

$$\text{Inhibit wait time} = 1 / (40 \times F_s) + 150\text{ns} + 50\text{ns}$$

Fs value for inhibit wait time calculation

<u>RS value used*</u>	<u>Fs value</u>
30Kohms	67,000
20Kohms	100,000
15Kohms	125,000

*Note: RS resistor value is set for max tracking rate and installed as an external component.

Note: The converter INH may be applied regardless of the CB line state. If the CB is busy the converter INH will wait for timing referenced to CB, before setting the INH latch. Therefore when applying an inhibit signal to the converter there is no need to monitor the CB line.

Sample 16-bit Data Read Sequence Using Inhibit Only

To read data in the shortest time duration inhibit must be started on CB start edge, to do a data read without monitoring CB start edge the worst case wait timing is defined below.

Presets: EM and EL must be set low or hard grounded, no need to monitor and trigger inhibit on CB start edge when using this worst case timing sequence:

1. Inhibit (set to Low).
2. Wait 575 ns.
3. Read 16-bit data bus.
4. Inhibit (set to High).
5. Repeat next data read from step 1.

Note: This timing sequence is for worst case timing using the inhibit pin only for control without monitoring the CB start edge. For the shortest data read wait time, CB start edge must be used for initializing an inhibit and a calculation must be performed for best time of inhibit.

11 BUILT-IN-TEST (BIT)

The BIT output is active low, and is triggered if any of the following conditions exist:

1. Loss of Signal (LOS) – The peak voltage of SIN and COS inputs both less than 500mV. The LOS has an internal filter on it to filter out the carrier frequency, to prevent the BIT from toggling between voltage peaks. Since the lowest specified reference frequency is 47 Hz (~21 ms), the filter must have a time constant long enough to filter this out.
2. Loss of Reference (LOR) – The RMS voltage across the Reference Input less than 500 mV.
3. Excessive Error - This error is detected by monitoring the demodulator output, which is proportional to the difference between the analog input and digital output. When it exceeds approximately 180 LSBs of positive error or 180 LSBs of negative error, BIT will be asserted. The demodulator is scaled for approximately 11 mV average per LSB. This condition can occur any time the analog input changes at a rate in excess of the maximum tracking rate. During power up, the converter may see a large difference between the SIN/COS inputs and the digital output angle held in its counter. BIT will be asserted until the converter settles within approximately 180 LSB's of the final result.
4. 180° phase error input signal to reference input (false null) causes a BIT and in addition kickstarts the converter counter to correct the error. All of the BIT conditions previously will disable the synthesized reference which is restored once the BIT is cleared. A 500 μ s dynamic delay occurs before the excessive error BIT becomes active. This dynamic delay is responsive to the active filter loop. The active filter loop is the response of the type II feedback loop to null out the error. This response is a function of the bandwidth components and the magnitude and transient quality of the error False Null 0 – this condition is caused by a meta-stable solution to the error equation when $\theta - \phi = 180^\circ$.

12 VELOCITY TRIMMING

The RD-19231 specifications for velocity scaling, reversal error, and offset are listed in Table 1. Velocity scaling and offset are externally trimmable for applications requiring tighter specifications than those available from the standard unit. Figure 20 shows the setup for trimming these parameters with external pots. It should also be noted that when the resolution is changed, velocity scaling is also changed.

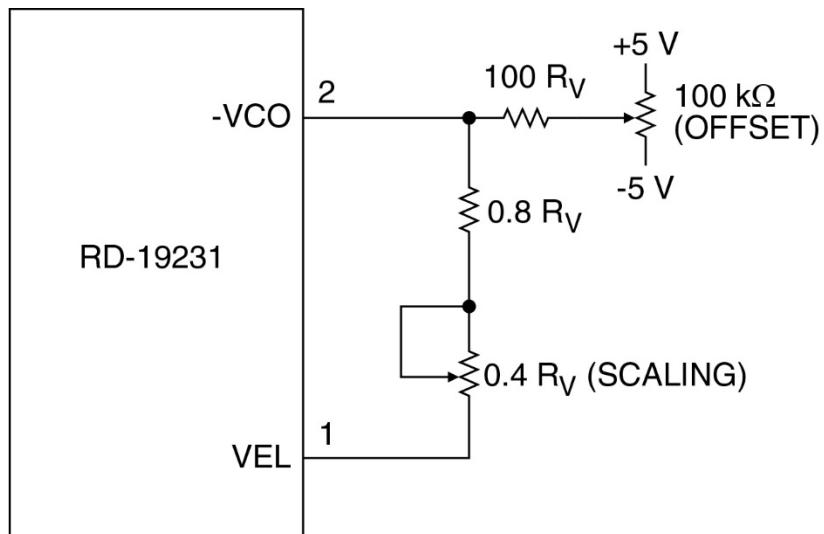


Figure 20. Velocity Trimming

The velocity output of the converter has mandatory timing components on the line which greatly affect the converters function. To use the velocity output line to monitor speed, you must add a buffer to the line as shown below.

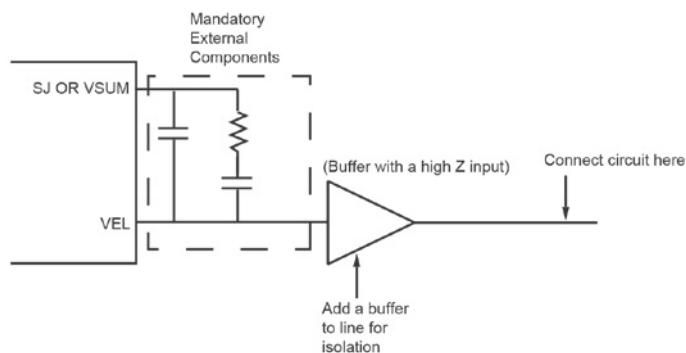


Figure 21. Example of Velocity Output Speed Monitor

13 BENEFIT OF SWITCHING RESOLUTION ON THE FLY

Switching resolution on the fly can be used in applications that require high resolution for accurate position control, and tracking rates or settling times that are faster than the high resolution mode will allow.

The RD-19231 can track four times faster for each step down in resolution (i.e., a step from 16 bits to 14 bits). The velocity output will be scaled down by a factor of four with each step down in resolution. For example, if the velocity output is scaled such that 4 Volts = 10 RPS in 16 bit resolution, then the same converter will output 1 Volt for 10 RPS in 14 bit resolution. To avoid glitches in the velocity output, the second set of bandwidth components can be precharged to the expected voltage, and switched in using the SHIFT input at the same time the resolution is changed. This will allow for a smooth velocity transition, resulting in reduced errors and minimal settling time after the change.

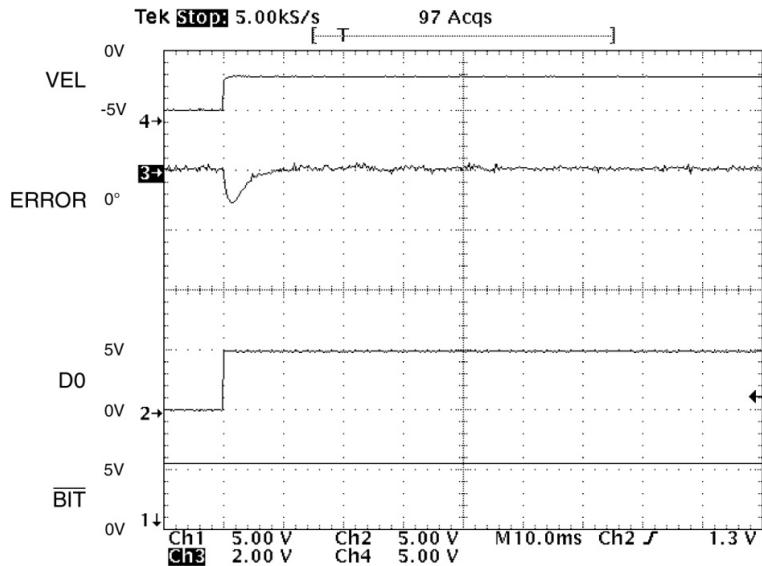
Figure 22 shows the way the converter behaves during a change in resolution while tracking at a constant velocity. The first illustration shows the benefits of switching in precharged components while changing resolution. The second illustration shows the result without the benefits of switching on the fly.

The signals that have been recorded are:

1. VEL: velocity output pin on the RD-19231
2. ERROR: this is the analog representation of the error between the input and the output of the RD-19231
3. D0: an input resolution control line to the RD-19231
4. BIT : built-in-test output pin of the RD-19231

When this system uses the switch resolution on the fly implementation, the velocity signal immediately assumes the precharged level of the second set of components, resulting in small errors and reduced settling times. Notice that the BIT output in Figure 22, does not indicate a fault condition.

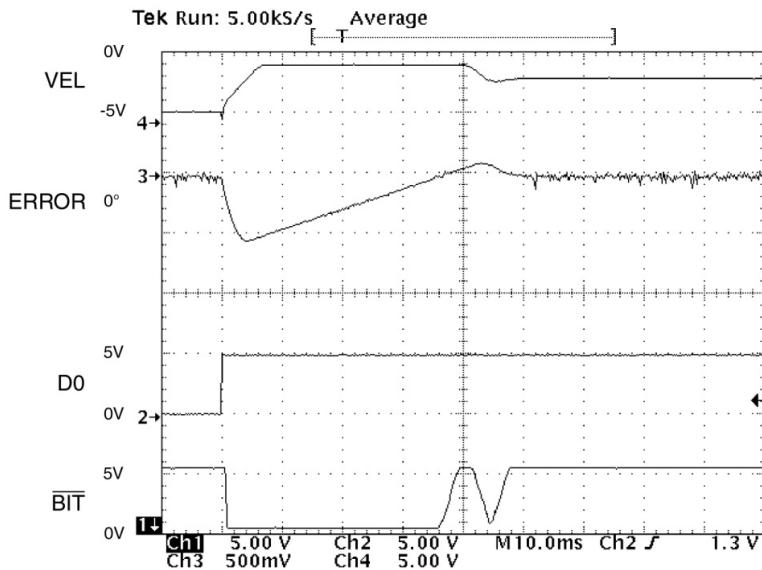
With Switch Resolution on the Fly Implemented:



ERROR = 13.6 LSBs per box

Depending on the bandwidth, the step error may be greater. Also, less velocity / movement will lessen the error glitch. The graphics above shows a worst case condition based on one bandwidth and tracking rate setup. Worst case is when the velocity overshoot hits the saturation point.

Without Switch Resolution on the Fly Implemented:



ERROR = 1500 LSBs per box

Figure 22. Benefit of Switching Resolution of the Fly

13.1 Switch on the Fly Implementation

The following steps detail switching resolution on the fly. For additional information refer to the Application Note #AN/MFT-3 “SWITCHING RESOLUTIONS ON THE FLY” available on the DDC web site at www.ddc-web.com.

1. The SHIFT pin should be controlled synchronously with the change in resolution. When shift is logic high, the VEL1 components will be selected. When shift is logic 0, the VEL2 components will be selected.
2. The second set of BW components (C_{BW2} , R_{B2} , $C_{BW2/10}$) should typically be of the same value as the first set (C_{BW1} , R_{B1} , $C_{BW1/10}$) and should be installed on VEL₂ and VEL SJ₂.

Note: *Each set of bandwidth components must be chosen to insure that the tracking rate to BW ratio (listed in Table 3) is not exceeded for the resolution in which it will be used*

3. The UP /DN line programs the gain of the precharged components/amplifier. If the resolution is increasing (UP /DN logic 0), the gain of the precharge amplifier is set to four. If the resolution is decreasing (UP /DN logic 1), the gain of the precharge amplifier is set to 1/4. The gain of the precharge amplifier should be programmed prior to switching the resolution of the converter, allowing enough time for the components to settle to the precharged level. This time will depend on the time constant of the bandwidth components being charged. If switching is limited to two adjacent resolutions (e.g., 14 and 16) then the precharge amplifier can be set up to continuously maintain the appropriate velocity voltage on the deselected components, resulting in the fastest possible switching times. See Figure 23 for an example of the input wiring connections necessary for switching on the fly between 14 and 16 bit resolution.

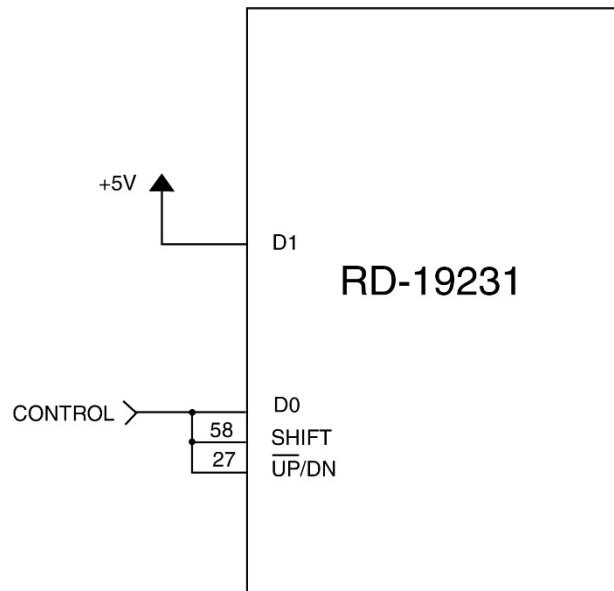


Figure 23. Input Wiring – Switching on the Fly Between 14 and 16 Bit Resolution

13.2 Dual Bandwidths

With the second set of BW component pins, the user can set two bandwidths for the RD-19231 and choose between them. To use two bandwidths, proceed as follows:

1. Tie $\overline{\text{UP}}/\text{DN}$ to pin -5V.
2. Choose the two bandwidths following the guidelines in the General Setup Considerations; the R_V resistor must be the same value for both bandwidths.
3. Use the SHIFT pin to choose between bandwidths. A logic 1 selects the VEL1 components and a logic 0 selects the VEL2 components.

14 SYNTHESIZED REFERENCE

The synthesized reference feature of the RD-19231 eliminates errors due to phase shift between the reference and signal inputs. As shown in the block diagram, Figure 2, the converter synthesizes its own internal reference signal based on the SIN and COS signal inputs. Therefore, the phase of the synthesized (internal) reference is determined by the signal input, resulting in reduced quadrature errors.

The synthesized reference can be disabled by connecting pin 52 DSR to ground through a 10-ohm resistor. Otherwise, the pin should be left as no connect.

Quadrature voltages in a resolver or synchro are by definition the resulting 90° fundamental signal in the nulled out error voltage (e) in the converter. Due to the inductive nature of synchros and resolvers, their output signals lead the reference input signal (RH and RL). When an uncompensated reference signal is used to demodulate the control transformer's output, quadrature voltages are not completely eliminated.

This feature ensures operation with a rotor-to-stator carrier frequency phase shift of up to 45 degrees.

Phase shifts greater than 45 degrees should be avoided to prevent a false BIT, condition 4 in Section 11.

15 DC INPUTS

The RD-19231 can operate with DC Sin, Cos and RH/RL inputs.

The Bit output is undetermined during DC operation and should not be used.

Scale the COS and SIN inputs such that the maximum signal is equal to 1.8VDC. For example, at 90° the SIN input should equal to 1.8VDC. This will keep the BW hysteresis consistent with AC operation.

When applying DC inputs to the Sin/Cos amplifiers, DC Input offsets will contribute error to the input signal. In 12 Bit and 10 Bit resolution, the Sin/Cos amplifiers offsets typically contribute less than 1 LSB of error. If external amplifiers are used to condition the COS and SIN inputs, low offset amplifier should be used.

The reference input is set to DC by tying RH to +5V and RL to ground or -5V.

It is recommended that the synthesized reference option be disabled for DC input operation only.

Disable the synthesized reference by connecting pin 52, DSR, to ground through a 8 to 10 ohm resistor.

In an AC application the phase of the RH/RL reference input is used to demodulate the error signal and provide a reference for position.

When applying DC inputs to RH/RL, the reference phase is undefined. The error signal is already DC so it passes through the demodulator.

Since the reference phase is undefined, DC inputs can result in an unstable false null, i.e., 180° hang-up. The false null condition will only happen on power up or an instantaneous 180° step, therefore once the converter moves it will go to the correct answer.

Considering the mechanical nature of the typical sensor in a real world application, an instantaneous 180° change is very unlikely, although it is theoretically possible. This condition typically arises at power up in real systems or in a test environment where the input is simulated. If the converter powers up at exactly 180° from the applied input, the converter will not move.

The minimum bandwidth should be based on the maximum tracking rate required by the systems. See Tracking Rate/Bandwidth Ratio in Table 3.

16 INTERNAL ENCODER EMULATION

The RD-19231 can be programmed to encoder emulation mode by toggling the A_QUAD_B input to a logic 0. The U/B output pin becomes B (LSB XOR LSB + 1). The A (LSB + 1) and B output signals can be used in control systems that are designed to interface with incremental optical encoders. To enable the Zero Index pulse, ZIP_EN should be tied to a logic 0.

An example circuit to create a low going edge of A_QUAD_B is depicted in Figure 27. If the power supply takes longer than 50ms to start up then the time constant of 50ms set in Figure 27 must be extended. Alternatively a system logic reset signal or internally generated logic ‘load’ pulse can be generated to latch in the encoder resolution.

The resolution of the incremental outputs is latched from the D0 and D1 inputs on the low going edge of A_QUAD_B. The resolution of the parallel data outputs may be changed any time after the encoder resolution is latched (see Figure 26).

When in A_QUAD_B mode, the resolution of the parallel data can be changed to a resolution equal to or greater than the A_QUAD_B resolution setting only. For example if the A_QUAD_B mode is active and the resolution is set to 12 bits, the resolution of the parallel programmed data can be changed from 12 bits to 14- or 16-bits by setting D0 & D1. If 10-bit mode is required for the parallel data, the A_QUAD_B resolution must also be programmed to 10-bits.

Note: The encoder resolution must be less than or equal to the resolution of the parallel data outputs. Refer to Figure 23.

The timing of the A, B and ZIP (or North Reference Pole [NRP]) output is dependent on the rate of change of the synchro/resolver position (rps or degrees per second) and the encoder resolution latched into the RD-19231 (refer to Figure 25). The calculations for the timing are:

$n = \text{resolution of parallel data}$

$t = 1 / (2^n * \text{Velocity(RPS)})$

$T = 1 / (\text{Velocity(RPS)})$

Note: The ZI pulse is high when all the bits of the counter are zero. If the resolution of the counter, (parallel data) is programmed differently than that of the A_QUAD_B then the resolution of the counter will determine the resolution of the ZIP.

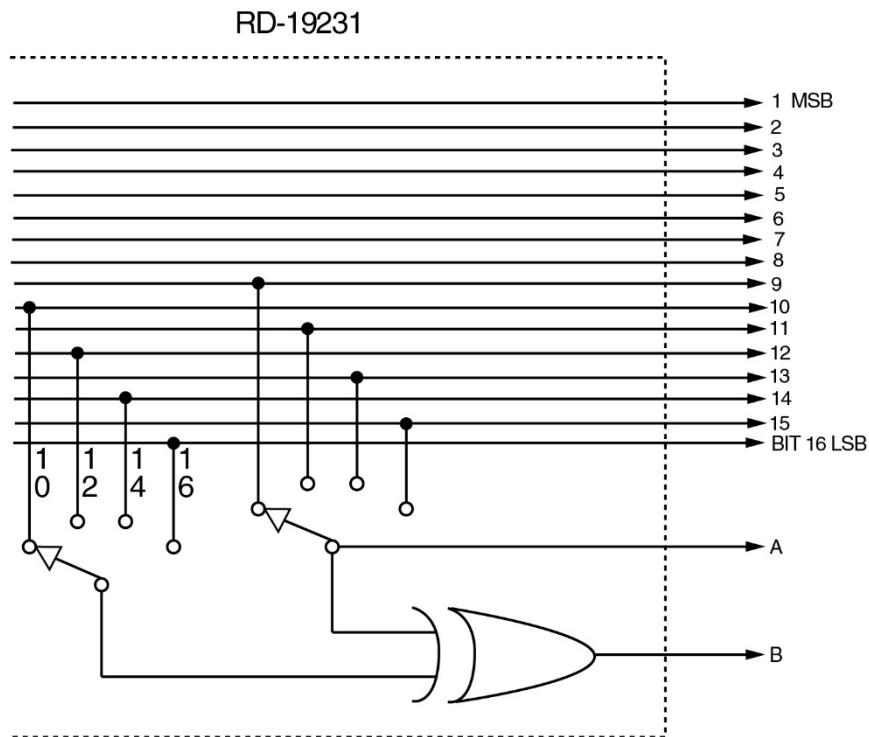


Figure 24. Incremental Encoder Emulation Resolution Control

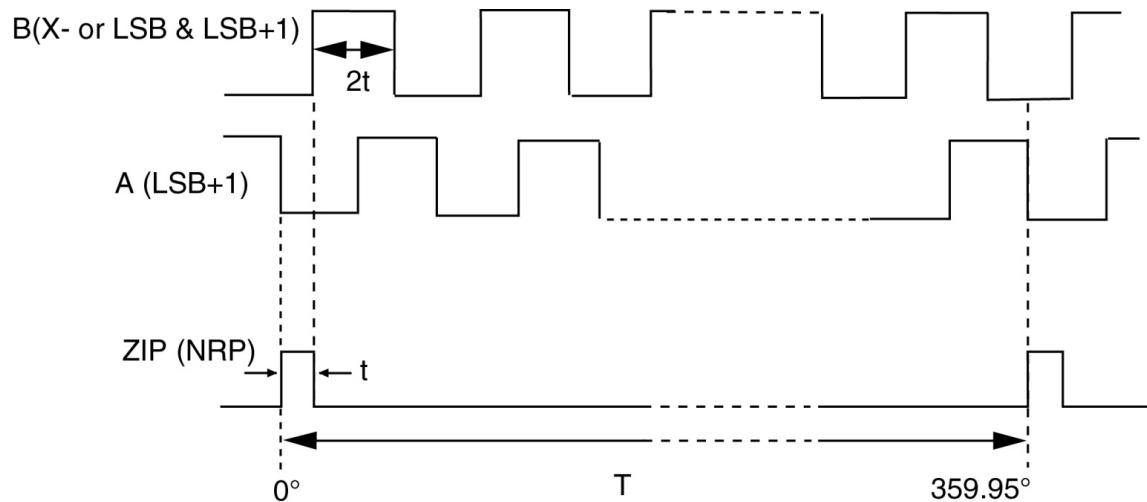


Figure 25. Incremental Encoder Emulation

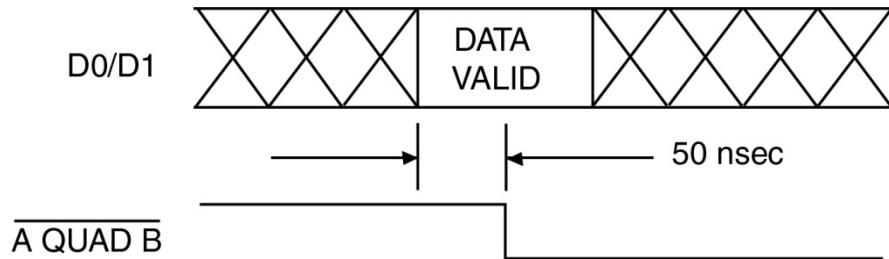
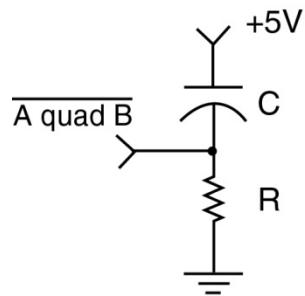


Figure 26. Timing for Incremental Encoder Emulation Resolution Control



$$\tau = RC$$

(ie. $50\text{ms} = 50\text{kOhms} \times 1\mu\text{F}$)

Figure 27. Example Circuit for A Quad B Reset

16.1 Clarification of A_QUAD_B, U/B, and ZIP_EN Functions

The RD-19231 is a tracking converter which is designed with a Type II closed servo loop. The Type II closed servo loop has an internal incremental integrator. This integrator acts as an up-down position counter. An AC error (e) within the RD-19231 represents the difference between θ (current angle to be digitized) and ϕ (the angle stored in digital form in the up-down counter). Because the RD-19231 constitutes in itself a Type II closed loop servomechanism, it continuously attempts to null the error to zero. This is accomplished by counting up or down 1 LSB until ϕ is equal to θ thus having an error of zero.

When A_QUAD_B is logic 0, encoder emulation mode is selected (i.e. The U/B output [Pin 29] is programmed to B). The encoder emulator resolution is set on the falling edge of A_QUAD_B (see Table 8).

Table 8. A_QUAD_B (Pin 30) Function	
A_QUAD_B (Pin 30)	U/B (Pin 29)
0	B
1	U

When A_QUAD_B is logic 1, encoder emulation mode is not selected (i.e. The U/B output is set to U, which indicates the direction of the internal position counter).

Note: *U indicates the “UP” direction of the counter. If the RD-19231 is at a static angle awaiting a new angle θ , U indicates the direction the counter was going to get to the current angle ϕ . As the error is approaching zero, the internal analog circuitry voltage may overshoot before settling - which would then indicate an incorrect direction. Because of this overshoot, the U output should not be relied on after settling to a static state. Only during active resolver movement will the U output state be reliable. U is a logic 1 when going in the positive direction (increasing angle). It is a logic 0 when going in the negative direction (decreasing angle).*

ZIP_EN chooses between the CB and Zero Index pulse outputs and is independent of encoder emulation mode. A logic 1 enables the CB pulse, a logic 0 enables the Zero Index pulse (see Table 9).

Note: *When the RD-19231FX is set for 16-bit mode, the LSB is bit 16. When the RD-19231FX is set for 14-bit mode, the LSB is bit 14 and bits 15 and 16 are set to logic “0”. (See Table 1, Note 1).*

Table 9. ZIP_EN (Pin 55) Function	
ZIP_EN (Pin 55)	CB/ZI (Pin 31)
0	ZI
1	CB

17 LVDT / RVDT MODE

RD-19231 can be configured to operate as an LVDT/RVDT-to-digital converter by programming the resolution control lines D0 & D1. In this mode the RD-19231 functions as a ratiometric tracking linear converter. When linear AC inputs are applied from an LVDT or RVDT the converter operates over one quarter of its range. Bits 1 & 2 are used to indicate over travel, while the remaining bits indicate position. This results in two less bits of resolution for LVDT/RVDT mode than are provided in resolver mode.

LVDT and RVDT sensor output signals need to be scaled to be compatible with the converter input. The value of the scaling constant “a” is selected to provide an input of 2 Vrms at full stroke of the LVDT. The value of scaling constant “b” is selected to provide an input of 1 Vrms at null of the LVDT/RVDT. Data output is binary coded in LVDT/RVDT mode.

17.1 2-Wire Input

By examination of the 2-wire LVDT circuit in Figure 28, the Vref voltage is always 2 Vrms, while Vdis is inverted and varies linearly with the displacement of the sensor.

The Sin output is half the sum of the Vref voltage and Vdis.

The Cos output is half the difference of the Vref and Vdis.

The resistor value R should be selected such that it does not load down the Sensor.

The value of resistor aR should be selected to achieve 2Vrms at Vdis when the output of the LVDT is at maximum voltage, which typically is at full scale or end of the range of the sensor output.

Gain a = 2/LVDT OUT Voltage

The value of resistor bR should be selected to achieve 2Vrms at Vref.

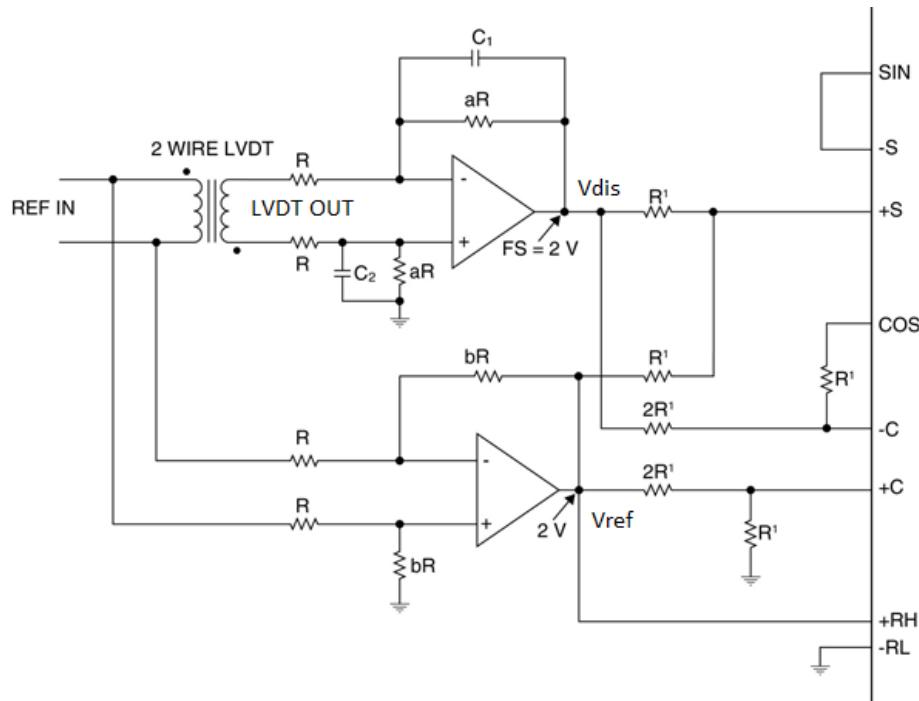
Gain b = 2/REF INPUT VOLTAGE

The Sin = Cos = 1Vrms when the sensor is at the NULL position.

$$(Vref + Vdis)/2 = (Vref - Vdis)/2 = 1Vrms$$

Table 10. 12-Bit 2-Wire LVDT Output Code Example

LVDT Output	Over Range	Data		
		MSB	LSB	
+ over full travel	01	xxxx	xxxx	xxxx
+ full travel -1 LSB	00	1111	1111	1111
+0.5 travel	00	1100	0000	0000
+1 LSB	00	1000	0000	0001
null	00	1000	0000	0000
-1 LSB	00	0111	1111	1111
-0.5 travel	00	0100	0000	0000
- full travel	00	0000	0000	0000
- over full travel	11	xxxx	xxxx	xxxx



$C_1 = C_2$, set for phase lag = phase lead through the LVDT.

Figure 28. 2-Wire LVDT

17.2 3-Wire Input

By examination of the 3-wire LVDT circuit in Figure 29, the Vref voltage is always

-2 Vrms, while Vdis varies linearly with the displacement of the sensor.

The Sin output is half the sum of the Vref voltage and Vdis.

The Cos output is half the difference of the Vref and Vdis.

The resistor value R should be selected such that it does not load down the Sensor.

The value of resistor aR should be selected to achieve 2Vrms at Vdis, when at full stroke end of range.

$$\text{Gain } a = |2/V_a - V_b|$$

The value of resistor bR should be selected to achieve -2Vrms at output Vref.

$$\text{Gain } a = 2/V_a + V_b$$

The Sin = Cos = 1Vrms when the sensor is at the NULL position.

$$(V_{\text{ref}} + V_{\text{dis}})/2 = (V_{\text{ref}} - V_{\text{dis}})/2 = 1\text{Vrms}$$

Table 11. 12-Bit 3-Wire LVDT Output Code Example				
LVDT Output	Over Range	Data		
		MSB	LSB	
+ over full travel	01	xxxx	xxxx	xxxx
+ full travel -1 LSB	00	1111	1111	1111
+0.5 travel	00	1100	0000	0000
+1 LSB	00	1000	0000	0001
null	00	1000	0000	0000
-1 LSB	00	0111	1111	1111
-0.5 travel	00	0100	0000	0000
- full travel	00	0000	0000	0000
- over full travel	11	xxxx	xxxx	xxxx

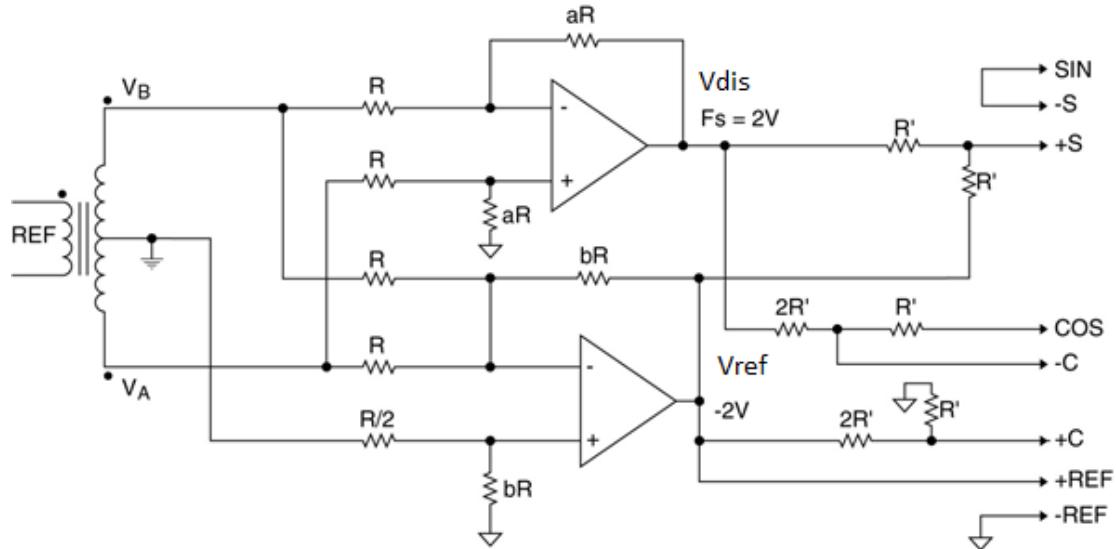


Figure 29. 3-Wire LVDT

LVDT Accuracy - Table 12 translates the accuracy specifications in Table 1 from minutes to % of full scale. It does not include resistor tolerance. Full scale range has been assumed to be NULL to +/-FS.

1 LSB in 14 bit resolution = $1/8192 = .012\%$ of Full Scale

1 LSB in 12 bit resolution = $1/2048 = .049\%$ of Full Scale

1 LSB in 10 bit resolution = $1/512 = .2\%$ of Full Scale

1 LSB in 8 bit resolution = $1/128 = .78\%$ of Full Scale

Table 12. 12-Bit 3-Wire LVDT Output Code Example

Resolution	1K-5Khz	5K-10Khz
12 Bit	8 minutes +1 Bit = .34% of FS	10 minutes +1 Bit = .42% of FS
10 Bit	16 minutes +1Bit = .8% of FS	16 minutes +1Bit = .8% of FS
8 Bit	42 minutes +1Bit = 2.3% of FS	42 minutes +1Bit = 2.3% of FS

18 THIN-FILM RESISTOR NETWORKS FOR MOTION FEEDBACK PRODUCTS

DDC converters such as the RD-19231 require closely matched 2Vrms SIN/COS input voltages to minimize digital error. DDC has custom thin-film resistor networks that provide the correctly matched 2Vrms converter outputs for 11.8Vrms Resolver/Synchro or 90Vrms synchro applications.

Any imbalance of the resistance ratio between the SIN/COS inputs will create errors in the digital output. DDC's custom thin-film resistor networks have very low imbalance percentages. The networks are matched to 0.02%, which equates to 1 LSB of error for a 16-bit application.

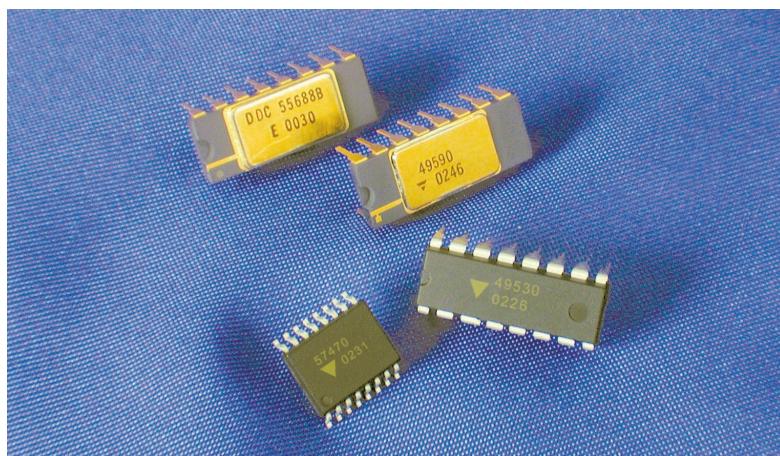


Figure 30. Thin-Film Resistor Networks

Table 13. Thin-Film Resistor Networks

Thin Film Resistor Network	Input Voltage (Vrms)	Output Voltage (Vrms)	Package Type
DDC-55688-1	2 Single Ended	2	Ceramic DIP
DDC-49530	11.8	2	Plastic DIP
DDC-57470	11.8	2	Surface Mount
DDC-49590	90	2	Ceramic DIP
DDC-76037	2 Differential	2	Plastic DIP
DDC-82620	2 Differential	2	Surface Mount
DDC-57471	90	2	Surface Mount

Notes:

1. For thin-film network specifications see the "Thin-Film Network Specifications for Motion Feedback Products" Data Sheet available from the DDC web site.
2. Operating temperature range is -55°C to +125°C

19 ORDERING INFORMATION

RD-19231FX - X 0 X

Accuracy: (note 1)

2 = 4 minutes + 1 LSB

3 = 2 minutes +1 LSB

5 = 1 minute + 1 LSB

Reliability:

0 = Standard DDC Procedures

Operating Temperature Range:

2 = -40°C to + 85°C

3 = 0°C to +70°C

Package Options:

X = Lead (note 2)

G = Lead Free (RoHS Compliant) (note 3)

Notes:

1. See Table 1 for accuracy related to frequency range.
2. Parts are completed by solder dip process over a tin (Sn) plated lead. Final finish is 63/37, 63% tin/37% lead.
3. The lead-free option has a matte tin finish. DDC can provide the reliability and tin whisker growth data associated with these products; however, tin whisker growth is dependent on the application environment and customers should collect their own reliability data and perform a risk assessment based on their individual requirements.

Packaging:

Parts are shipped in JEDEC trays that are acceptable for use with pick and place operation.

Component Selection Software:

Component selection software can be downloaded from our web site at www.ddc-web.com.

Development Kits Available:

P/N RD-19231EX-300 (See the DDC web site for this card's User's Guide)

Standard DDC Processing for Plastic Monolithic Products		
Test	MIL-STD-883	
	Method(s)	Condition(s)
Inspection/Workmanship	2017	—
Electrical Test	DDC ATP	—