PCIe-Mini-CAN-FD

PCIe Mini CAN Controller

PCIexpress Mini

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Software MANUAL

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Hierarchical Index

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Class List

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File List

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Features

CAN Bus

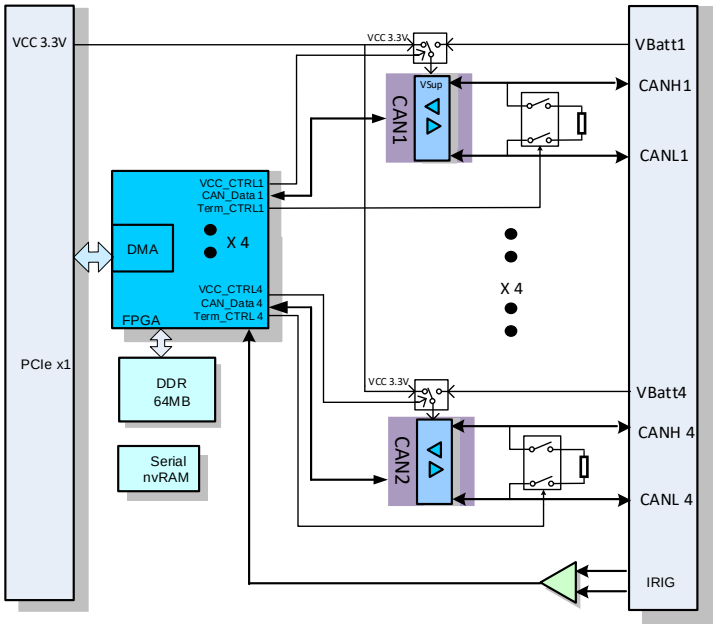
- Four channel CAN controller
- Supports classic CAN and CAN FD
- Complies with
  - ISO11898-1:2015
  - M_CAN Revision 3.2.1.1
- Meets requirements of ISO11898-2:2016
- Data rates from 40Kbps to 8Mbps
- Software programmable speed selection
- Independent Software controlled
  - 120 Ohm Termination
  - Internal External Power Source
- CAN bus robustness
  - ±42V bus fault protection
  - Failsafe mode
  - Internal dominant state timeout
  - Timeout watchdog
- IRIG-B input
- ±15KV ESD protection
- PCI Express x1 interface

Block Diagram and Operational Overview

The ***PCIe-Mini-CAN-FD*** is PCIexpress controller with an integrated CAN FD transceiver supporting data rates up to 8 Mbps. The CAN FD controller meets the specifications of the ISO11898-1:2015 high speed controller area network (CAN) data link layer and meets the physical layer requirements of the ISO11898–2:2016 high speed CAN specification.

The ***PCIe-Mini-CAN-FD*** provides an interface between the CAN bus and the system processor that support both classical CAN and CAN FD
The ***PCIe-Mini-CAN-FD*** provides CAN FD transceiver functionality – differential transmit-receive capability from the bus. It also supports local wake up (LWU) and bus wake up (WUP).

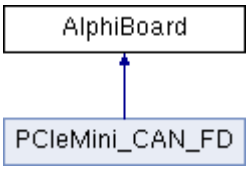
The ***PCIe-Mini-CAN-FD*** device includes many protection features providing device and CAN bus robustness. These features include failsafe mode, internal dominant state timeout, wide bus operating range and a timeout watchdog as examples.



Class Documentation

AlphiBoard Class Reference

Base class implementing a PCIe board and the Jungo driver.
`#include <AlphiBoard.h>`
Inheritance diagram for AlphiBoard:



Public Member Functions

- **AlphiBoard** (UINT16 vendorId, UINT16 deviceId)
- **~AlphiBoard** (void)
  Destructor.

- **HRESULT Open** (int brdNbr)
  Open a board.

- DWORD **reset** ()
  reset some of the board resources

- uint32_t **getFpgaID** ()
  Get the FPGA ID of.

- time_t **getFpgaTimeStamp** ()
  Return the timestamp corresponding to when the FPGA was compiled.

- void **setVerbose** (int **verbose**)
  set the verbose flag

- bool **IsValidDevice** (const CHAR *sFunc)
  Validate a WDC device handle.

- DWORD **hookInterruptServiceRoutine** (uint32_t mask, **MINIPCIE_INT_HANDLER** uicr, void *userData)
  Setup the interrupt of the board.

- DWORD **hookInterruptServiceRoutine** (**MINIPCIE_INT_HANDLER** uicr)
  Set an interrupt handling routine.

- DWORD **getIntResults** (**MINIPCIE_INT_RESULT** *intResult)
- DWORD **unhookInterruptServiceRoutine** ()
  Disable the board interrupt.

- DWORD **enableInterrupts** (uint16_t mask=0xffff)

Enable PCIe interrupts.

- DWORD **disableInterrupts** ()
  Disable PCIe interrupts.

- DWORD **Close** ()
  Close a device handle.

- volatile void * **getBar0Address** (size_t offset)
  Return a pointer to an object in BAR 0.

- volatile void * **getBar2Address** (size_t offset)
  Return a pointer to an object in BAR 2.

- volatile void * **getBar3Address** (size_t offset)
  Return a pointer to an object in BAR 3.

- bool **DMARoutine** (DWORD dwDMABufSize, uint32_t u32LocalAddr, bool fPolling, bool fToDev, **TransferDesc** *tfrDesc)
- **PCIeMini_status DMAOpen** (uint32_t u32LocalAddr, DWORD dwDMABufSize, bool fToDev, **TransferDesc** *tfrDesc)
  Allocates and locks a contiguous DMA buffer.

- void **DMAClose** (bool fPolling)
  Frees a previously allocated contiguous DMA buffer.

- void **DMATransfer** (**TransferDesc** *tfrDesc, bool fPolling)
- virtual void **hwDMAStart** (**TransferDesc** *tfrDesc)
- virtual bool **hwDMAWaitForCompletion** (**TransferDesc** *tfrDesc, bool fPolling)
- virtual bool **hwDMAInterruptEnable** (**MINIPCIE_INT_HANDLER MyDmaIntHandler**, void *pDMA)
- virtual void **hwDMAInterruptDisable** ()
- virtual void **hwDMAProgram** (WD_DMA_PAGE *Page, DWORD dwPages, bool fToDev, uint32_t u32LocalAddr, **TransferDesc** *tfrDesc)

Static Public Member Functions

- static void **MsSleep** (int ms)
  Millisecond Delay Function.

Public Attributes

- **LinearAddress bar0**
  Memory descriptor for the BAR0 in user memory.

- **LinearAddress bar2**
  Memory descriptor for the BAR2 in user memory.

- **LinearAddress bar3**
  Memory descriptor for the BAR3 in user memory.

- **PcieCra * cra**
  PCIe Interface instance.

- **BoardVersion * sysid**
  Board identification.

- WD_DMA * **pDma**
  Jungo DMA structure.

- int **verbose**
  Flag used by various functions to determine the amount of messages to generate.

- DWORD **libStatus**
  Status returned when trying to open the Jungo library. If it is not WD_STATUS_SUCCESS, the initialization failed.

Detailed Description

Base class implementing a PCIe board and the Jungo driver.

Constructor & Destructor Documentation

AlphiBoard::AlphiBoard (UINT16 *vendorId*, UINT16 *deviceId*)

AlphiBoard::~AlphiBoard (void)

Destructor.

Will close the connection to the board if needed.

Member Function Documentation

DWORD AlphiBoard::Close ()

Close a device handle.

Returns

status, a Jungo status code

DWORD AlphiBoard::disableInterrupts ()

Disable PCIe interrupts.

Disable the generation of PCIe interrupts by the PCIe interface, and the reception by the Windows driver.

Return values

Status	code

void AlphiBoard::DMAClose (bool *fPolling*)

Frees a previously allocated contiguous DMA buffer.

PCIeMini_status AlphiBoard::DMAOpen (uint32_t *u32LocalAddr*, DWORD *dwDMABufSize*, bool *fToDev*, TransferDesc * *tfrDesc*)

Allocates and locks a contiguous DMA buffer.

Parameters

fToDev	true means DMA to device, false means DMA from device.
dwDMABufSize	Size of the DMA buffer allocated in user space.
tfrDesc	Pointer to a transfer information structure.
u32LocalAddr	Local FPGA address of the DMA source or destination inside the board.

bool AlphiBoard::DMARoutine (DWORD *dwDMABufSize*, uint32_t *u32LocalAddr*, bool *fPolling*, bool *fToDev*, TransferDesc * *tfrDesc*)

void AlphiBoard::DMATransfer (TransferDesc * *tfrDesc*, bool *fPolling*)

DWORD AlphiBoard::enableInterrupts (uint16_t *mask* = `0xffff`)

Enable PCIe interrupts.

Enable the generation of PCIe interrupts by the board's PCIe interface. Enable the reception of PCIe interrupts by the Windows driver.

Parameters

mask	Optional bit map of which local interrupt line is enabled (board dependent.) If not used, default to 0xffff - all local interrupts allowed.

Return values

Status	code

volatile void * AlphiBoard::getBar0Address (size_t *offset*)

Return a pointer to an object in BAR 0.

Parameters

offset	Offset in BAR0

Return values

Pointer	to the object

volatile void * AlphiBoard::getBar2Address (size_t *offset*)

Return a pointer to an object in BAR 2.

Parameters

offset	Offset in BAR2

Return values

Pointer	to the object

volatile void * AlphiBoard::getBar3Address (size_t *offset*)

Return a pointer to an object in BAR 3.

BAR3 is used on a few board to locate dual-ported RAM.

Parameters

offset	Offset in BAR3

Return values

Pointer	to the object

uint32_t AlphiBoard::getFpgaID ()

Get the FPGA ID of.

Returns

The FPGA ID.

time_t AlphiBoard::getFpgaTimeStamp ()

Return the timestamp corresponding to when the FPGA was compiled.

Returns

a timestamp.

DWORD AlphiBoard::getIntResults (MINIPCIE_INT_RESULT * *intResult*)

DWORD AlphiBoard::hookInterruptServiceRoutine (MINIPCIE_INT_HANDLER *uicr*)

Set an interrupt handling routine.

Parameters

uicr	user callback routine typedef void (__stdcall *UsersIntCompletionRoutine)(void *, uint32_t);

Returns

ERRCODE_NO_ERROR if successful.

DWORD AlphiBoard::hookInterruptServiceRoutine (uint32_t *mask*, MINIPCIE_INT_HANDLER *uicr*, void * *userData*)

Setup the interrupt of the board.

Specify and interrupt service routine and enable the interrupts.

Parameters

mask	board dependent interrupt mask.
uicr	pointer to the interrupt service routine.
userData	Value sent to the interrupt service routine as parameter.

Returns

WD_STATUS_SUCCESS when the operation succeeded WD_INVALID_PARAMETER if the board is not opened WD_OPERATION_FAILED if the board does not have an interrupt resource WD_OPERATION_ALREADY_DONE if there is already an isr active for the interrupt.

void AlphiBoard::hwDMAInterruptDisable () `[virtual]`

Reimplemented in **PCIeMini_CAN_FD** (*p.38*).

bool AlphiBoard::hwDMAInterruptEnable (MINIPCIE_INT_HANDLER *MyDmaIntHandler*, void * *pDMA*) `[virtual]`

Reimplemented in **PCIeMini_CAN_FD** (*p.38*).

void AlphiBoard::hwDMAProgram (WD_DMA_PAGE * *Page*, DWORD *dwPages*, bool *fToDev*, uint32_t *u32LocalAddr*, TransferDesc * *tfrDesc*) `[virtual]`

Reimplemented in **PCIeMini_CAN_FD** (*p.38*).

void AlphiBoard::hwDMAStart (TransferDesc * *tfrDesc*) `[virtual]`

Reimplemented in **PCIeMini_CAN_FD** (*p.38*).

bool AlphiBoard::hwDMAWaitForCompletion (TransferDesc * *tfrDesc*, bool *fPolling*) `[virtual]`

Reimplemented in **PCIeMini_CAN_FD** (*p.39*).

bool AlphiBoard::IsValidDevice (const CHAR * *sFunc*)

Validate a WDC device handle.

Parameters

sFunc	C-string with name of the function e.g. "IntEnable"

Return values

true	if the device context exists.

static void AlphiBoard::MsSleep (int *ms*) `[inline]`, `[static]`

Millisecond Delay Function.

HRESULT AlphiBoard::Open (int *brdNbr*)

Open a board.

Establishes a connection to a board.

Parameters

brdNbr	the board index to open.

Returns

WD_DEVICE_NOT_FOUND if there is no board corresponding to the number

DWORD AlphiBoard::reset () `[inline]`

reset some of the board resources

void AlphiBoard::setVerbose (int *vb*)

set the verbose flag

The verbose value is used to send more information to the log file or console. It is only partially implemented.

Parameters

vb	Verbosity level.

DWORD AlphiBoard::unhookInterruptServiceRoutine ()

Disable the board interrupt.

Parameters

mask	board dependent interrupt mask.
uicr	pointer to the interrupt service routine.

Returns

WD_STATUS_SUCCESS when the operation succeeded WD_INVALID_PARAMETER if the board is not opened WD_OPERATION_FAILED if the board does not have an interrupt resource WD_OPERATION_ALREADY_DONE if there the interrupt is already disabled.

Member Data Documentation

LinearAddress AlphiBoard::bar0

Memory descriptor for the BAR0 in user memory.

LinearAddress AlphiBoard::bar2

Memory descriptor for the BAR2 in user memory.

LinearAddress AlphiBoard::bar3

Memory descriptor for the BAR3 in user memory.

PcieCra* AlphiBoard::cra

PCIe Interface instance.

DWORD AlphiBoard::libStatus

Status returned when trying to open the Jungo library. If it is not WD_STATUS_SUCCESS, the initialization failed.

WD_DMA* AlphiBoard::pDma

Jungo DMA structure.

BoardVersion* AlphiBoard::sysid

Board identification.

int AlphiBoard::verbose

Flag used by various functions to determine the amount of messages to generate.

The documentation for this class was generated from the following files:

- C:/Alphi/PCIeMiniSoftware/include/**AlphiBoard.h**
- C:/Alphi/PCIeMiniSoftware/PCIeMini_lib/**AlphiBoard.cpp**
- C:/Alphi/PCIeMiniSoftware/PCIeMini_lib/**AlphiBoard_dma.cpp**
- C:/Alphi/PCIeMiniSoftware/PCIeMini_lib/**AlphiBoard_irq.cpp**

AlteraDma Class Reference

Low level SPI interface to the SPI hardware.
`#include <AlteraDma.h>`

Public Member Functions

- **AlteraDma** (volatile void *dmaAddress)
  Constructor.

- int **prepare** (void *data, uint32_t len, **alt_rxchan_done** *done, void *handle)
- int **space** ()
- int **send** (const void *from, uint32_t len, **alt_txchan_done** *done, void *handle)
- int **tx_ioctl** (int req, void *arg)
- int **rx_ioctl** (int req, void *arg)
- int **ioctl** (int req, void *arg)
- void **launch_bidir** (**TransferDesc** *t)
- void **launch_txonly** (**TransferDesc** &t)
- void **launch_rxonly** (**TransferDesc** &t)
- void **reset** ()
- char * **statusToString** (char *buffer)
- char * **controlToString** (char *buffer)
- void **print** (const char *title=0)
- void **irq** (void *context, uint32_t id)
- uint32_t **getStatus** ()
- uint32_t **getLength** ()

Detailed Description

Low level SPI interface to the SPI hardware.

Constructor & Destructor Documentation

AlteraDma::AlteraDma (volatile void * *dmaAddress*)

Constructor.

Initialise and register the transmit and receive channels for a given physical DMA device.

Parameters

dmaAddress	Address of the DMA controller in user space.

Member Function Documentation

char* AlteraDma::controlToString (char * *buffer*) `[inline]`

uint32_t AlteraDma::getLength () `[inline]`

uint32_t AlteraDma::getStatus () `[inline]`

int AlteraDma::ioctl (int *req*, void * *arg*)

void AlteraDma::irq (void * *context*, uint32_t *id*)

void AlteraDma::launch_bidir (TransferDesc * *t*)

void AlteraDma::launch_rxonly (TransferDesc & *t*)

void AlteraDma::launch_txonly (TransferDesc & *t*)

int AlteraDma::prepare (void * *data*, uint32_t *len*, alt_rxchan_done * *done*, void * *handle*)

void AlteraDma::print (const char * *title* = `0`) `[inline]`

void AlteraDma::reset () `[inline]`

int AlteraDma::rx_ioctl (int *req*, void * *arg*)

int AlteraDma::send (const void * *from*, uint32_t *len*, alt_txchan_done * *done*, void * *handle*)

int AlteraDma::space ()

char* AlteraDma::statusToString (char * *buffer*) `[inline]`

int AlteraDma::tx_ioctl (int *req*, void * *arg*)

The documentation for this class was generated from the following files:

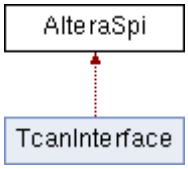
- C:/Alphi/PCIeMiniSoftware/include/**AlteraDma.h**
- C:/Alphi/PCIeMiniSoftware/PCIeMini_lib/**AlteraDma.cpp**

AlteraSpi Class Reference

Low level SPI interface to the SPI hardware.

`#include <AlteraSpi.h>`

Inheritance diagram for AlteraSpi:



Public Member Functions

- **AlteraSpi** (volatile void *addr, uint8_t width=1)
  Constructor.

- int **sendSpiCommand** (uint32_t slave, uint32_t write_length, const uint32_t *write_data, uint32_t read_length, uint32_t *read_data, uint32_t flags)
  Send an SPI command.

- volatile uint32_t **getRxData** ()
  Get the content of the receive data register.

- volatile uint32_t **getStatus** ()
- void **resetStatus** ()
- void **setTxData** (uint32_t data)
- void **setControl** (uint32_t data)
- void **selectSlave** (volatile uint32_t data)

Static Public Attributes

- static const uint32_t **status_ROE_mask** = 0x0008
  Receive - overrun error.

- static const uint32_t **status_TOE_mask** = 0x0010
  Transmitter-overrun error.

- static const uint32_t **status_TMT_mask** = 0x0020
  Transmitter shift-register empty.

- static const uint32_t **status_TRDY_mask** = 0x0040
  Transmitter ready.

- static const uint32_t **status_RRDY_mask** = 0x0080
  Receiver ready.

Protected Attributes

- volatile uint32_t * **base**
- uint8_t **wordSize**
- int **rxData_index** = 0

- int **txData_index** = 1
- int **status_Index** = 2
- int **control_index** = 3
- int **slaveSelect_index** = 5

Detailed Description

Low level SPI interface to the SPI hardware.

Constructor & Destructor Documentation

AlteraSpi::AlteraSpi (volatile void * *addr*, uint8_t *width* = 1)

Constructor.

Called only when the board is opened.

Parameters

addr	Pointer to the device in user space.
width	Word size in byte, default is 1.

Member Function Documentation

volatile uint32_t AlteraSpi::getRxData () [inline]

Get the content of the receive data register.

Return values

Content	of the receive data register

volatile uint32_t AlteraSpi::getStatus () [inline]

void AlteraSpi::resetStatus () [inline]

void AlteraSpi::selectSlave (volatile uint32_t *data*) [inline]

int AlteraSpi::sendSpiCommand (uint32_t *slave*, uint32_t *write_length*, const uint32_t * *write_data*, uint32_t *read_length*, uint32_t * *read_data*, uint32_t *flags*)

Send an SPI command.

This is a very simple routine which performs one SPI master transaction. It would be possible to implement a more efficient version using interrupts and sleeping threads but this is probably not worthwhile initially.

Parameters

slave	Slave number select 0-31
write_length	Number of bytes to send
write_data	A pointer to the buffer containing the data to write
read_length	Number of bytes to receive
read_data	A pointer to the buffer where the received data is going

flags	A bit mask, only ALT_AVALON_SPI_COMMAND_TOGGLE_SS_N is used.

Return values

Number	of bytes read - in SPI read and write are simultaneous so it cannot be 0.

void AlteraSpi::setControl (uint32_t *data*) `[inline]`

void AlteraSpi::setTxData (uint32_t *data*) `[inline]`

Member Data Documentation

volatile uint32_t* AlteraSpi::base `[protected]`

int AlteraSpi::control_index = 3 `[protected]`

int AlteraSpi::rxData_index = 0 `[protected]`

int AlteraSpi::slaveSelect_index = 5 `[protected]`

int AlteraSpi::status_Index = 2 `[protected]`

const uint32_t AlteraSpi::status_ROE_mask = 0x0008 `[static]`

Receive - overrun error.

The ROE bit is set to 1 if new data is received while the rxdata register is full(that is, while the RRDY bit is 1).In this case, the new data overwrites the old. Writing to the status register clears the ROE bit to 0.

const uint32_t AlteraSpi::status_RRDY_mask = 0x0080 `[static]`

Receiver ready.

The RRDY bit is set to 1 when the rxdata register is full.

const uint32_t AlteraSpi::status_TMT_mask = 0x0020 `[static]`

Transmitter shift-register empty.

In master mode, the TMT bit is set to 0 when a transaction is in progress and set to 1 when the shift register is empty.

const uint32_t AlteraSpi::status_TOE_mask = 0x0010 `[static]`

Transmitter-overrun error.

The TOE bit is set to 1 if new data is written to the txdata register while it is still full (that is, while the TRDY bit is 0). In this case, the new data is ignored. Writing to the status register clears the TOE bit to 0.

const uint32_t AlteraSpi::status_TRDY_mask = 0x0040 `[static]`

Transmitter ready.

The TRDY bit is set to 1 when the txdata register is empty.

int AlteraSpi::txData_index = 1 `[protected]`

uint8_t AlteraSpi::wordSize `[protected]`

The documentation for this class was generated from the following files:

- C:/Alphi/PCIeMiniSoftware/include/**AlteraSpi.h**
- C:/Alphi/PCIeMiniSoftware/PCIeMini_lib/**AlteraSpi.cpp**

BoardVersion Class Reference

Board Hardware identification and version.
`#include <AlphiBoard.h>`

Public Member Functions

- **BoardVersion** (volatile uint32_t *addr)
  constructor

- uint32_t **getVersion** ()
  Version, if there is one programmed on the board hardware. Typically 0.

- time_t **getTimeStamp** ()
  Date when the board firmware was compiled.

Detailed Description

Board Hardware identification and version.

Constructor & Destructor Documentation

BoardVersion::BoardVersion (volatile uint32_t * *addr*)

constructor

This constructor reads the chip register to initialize the data. It is called by the open and should not be called by the user.

Parameters

addr	Offset to the sysid controller in the BAR2 address space

---

Member Function Documentation

time_t BoardVersion::getTimeStamp ()

Date when the board firmware was compiled.

Return FPGA time stamp.

Date and time when the board firmware was compiled, it can be used to identify the version of the hardware.

uint32_t BoardVersion::getVersion ()

Version, if there is one programmed on the board hardware. Typically 0.

Return the board type.

The documentation for this class was generated from the following files:

- C:/Alphi/PCIeMiniSoftware/include/**AlphiBoard.h**
- C:/Alphi/PCIeMiniSoftware/PCIeMini_lib/**AlphiBoard.cpp**

IrigDecoder::IrigDate Struct Reference

`#include <IrigDecoder.h>`

Public Attributes

- int **tm_sec**
- int **tm_min**
- int **tm_hour**
- int **tm_yday**
- int **tm_year**

Member Data Documentation

int IrigDecoder::IrigDate::tm_hour

int IrigDecoder::IrigDate::tm_min

int IrigDecoder::IrigDate::tm_sec

int IrigDecoder::IrigDate::tm_yday

int IrigDecoder::IrigDate::tm_year

The documentation for this struct was generated from the following file:

- C:/Alphi/PCIeMiniSoftware/include/**IrigDecoder.h**

IrigDecoder Class Reference

`#include <IrigDecoder.h>`

Classes

- struct **IrigDate**

Public Member Functions

- **IrigDecoder** (volatile void *addr)
- uint32_t **getTimeRaw** ()
- void **getTime** (**IrigDate** *ttm)
- uint32_t **getDayRaw** ()
- void **getDay** (**IrigDate** *ttm)
- uint32_t **getSecond** ()
- void **getIrigDate** (struct tm *t)

Constructor & Destructor Documentation

IrigDecoder::IrigDecoder (volatile void * *addr*) `[inline]`

Member Function Documentation

void IrigDecoder::getDay (IrigDate * *ttm*) `[inline]`

uint32_t IrigDecoder::getDayRaw () `[inline]`

void IrigDecoder::getIrigDate (struct tm * *t*) `[inline]`

uint32_t IrigDecoder::getSecond () `[inline]`

void IrigDecoder::getTime (IrigDate * *ttm*) `[inline]`

uint32_t IrigDecoder::getTimeRaw () `[inline]`

The documentation for this class was generated from the following file:

- C:/Alphi/PCIeMiniSoftware/include/**IrigDecoder.h**

LinearAddress Struct Reference

Memory Segment Descriptor.
`#include <AlphiBoard.h>`

Public Attributes

- void * **Address**
  Linear address.

- size_t **Length**
  Length of the mapping.

Detailed Description

Memory Segment Descriptor.

Member Data Documentation

void* LinearAddress::Address

Linear address.

size_t LinearAddress::Length

Length of the mapping.

The documentation for this struct was generated from the following file:

- C:/Alphi/PCIeMiniSoftware/include/**AlphiBoard.h**

MINIPCIE_DEV_CTX Struct Reference

Minipcie Device Information Structure.
`#include <AlphiBoard.h>`

Public Attributes

- **MINIPCIE_INT_HANDLER funcDiagIntHandler**
  Interrupt handler routine.

- **MINIPCIE_EVENT_HANDLER funcDiagEventHandler**
  Event handler routine.

- void * **userData**
  Data passed to the interrupt routine.

Detailed Description

Minipcie Device Information Structure.

Member Data Documentation

MINIPCIE_EVENT_HANDLER MINIPCIE_DEV_CTX::funcDiagEventHandler

Event handler routine.

MINIPCIE_INT_HANDLER MINIPCIE_DEV_CTX::funcDiagIntHandler

Interrupt handler routine.

void* MINIPCIE_DEV_CTX::userData

Data passed to the interrupt routine.

The documentation for this struct was generated from the following file:

- C:/Alphi/PCIeMiniSoftware/include/**AlphiBoard.h**

MINIPCIE_INT_RESULT Struct Reference

Interrupt result information structure.
`#include <AlphiBoard.h>`

Public Attributes

- DWORD **dwCounter**
  Number of interrupts received.

- DWORD **dwLost**
  Number of interrupts not yet handled.

- WD_INTERRUPT_WAIT_RESULT **waitResult**
  See WD_INTERRUPT_WAIT_RESULT values in windrvr.h.

- DWORD **dwEnabledIntType**
  Interrupt type that was actually enabled (MSI/MSI-X/Level Sensitive/Edge-Triggered)

- DWORD **dwLastMessage**

Detailed Description

Interrupt result information structure.

Member Data Documentation

DWORD MINIPCIE_INT_RESULT::dwCounter

Number of interrupts received.

DWORD MINIPCIE_INT_RESULT::dwEnabledIntType

Interrupt type that was actually enabled (MSI/MSI-X/Level Sensitive/Edge-Triggered)

DWORD MINIPCIE_INT_RESULT::dwLastMessage

Message data of the last received MSI/MSI-X (Windows Vista and higher); N/A to line-based interrupts)

DWORD MINIPCIE_INT_RESULT::dwLost

Number of interrupts not yet handled.

WD_INTERRUPT_WAIT_RESULT MINIPCIE_INT_RESULT::waitResult

See WD_INTERRUPT_WAIT_RESULT values in windrvr.h.

The documentation for this struct was generated from the following file:

- C:/Alphi/PCIeMiniSoftware/include/**AlphiBoard.h**

ParallelInput Class Reference

Alphi Avalon Pio controller class.
`#include <ParallelInput.h>`

Public Member Functions

- **ParallelInput** (volatile void *addr)
- **PCIeMini_status reset** ()
  Reset the PIO.

- uint32_t **getData** ()
- uint32_t **getIrqEnable** ()
  Retrieve the interrupt mask.

- uint32_t **setIrqEnable** (uint32_t mask)
  Enable bits in the interrupt mask.

- uint32_t **setIrqDisable** (uint32_t mask)
  Disable bits in the interrupt mask.

- uint32_t **getIrqStatus** ()
- uint32_t **resetIrq** ()
- **PCIeMini_status clearIrqStatus** (uint32_t mask)

Public Attributes

- volatile uint32_t * **base**
- int **data_index** = 0
- int **polarity_index** = 1
  polarity: when set to 1, the interrupt is requested if the corresponding bit is low.

- int **edgeReg_Index** = 2
  edge register: when a bit is set to 1, the interrupt is generated on an edge

- int **irqStatus_index** = 3
- int **irqEnable_index** = 4
- int **direction_index** = 5
- int **dataOut_index** = 6
- int **irqDelay_index** = 7

Static Public Attributes

- static const uint16_t **CAP_INPUT** = 0x01
- static const uint16_t **CAP_OUTPUT** = 0x02
- static const uint16_t **CAP_INPUT_OUTPUT** = 0x03

Detailed Description

Alphi Avalon Pio controller class.

Constructor & Destructor Documentation

ParallelInput::ParallelInput (volatile void * *addr*) `[inline]`

Member Function Documentation

PCIeMini_status ParallelInput::clearIrqStatus (uint32_t *mask*) `[inline]`

uint32_t ParallelInput::getData () `[inline]`

uint32_t ParallelInput::getIrqEnable () `[inline]`

Retrieve the interrupt mask.

Returns 1 for the bits corresponding to input bits able to generate interrupts. On output-only devices, it will return 0.

Return values

A	32-bit bit map of which bit can generate interrupts.

uint32_t ParallelInput::getIrqStatus () `[inline]`

PCIeMini_status ParallelInput::reset () `[inline]`

Reset the PIO.

Whenever supported, set the direction register to all input, the data register to 0, and disable interrupts.

Return values

Always	success

uint32_t ParallelInput::resetIrq () `[inline]`

uint32_t ParallelInput::setIrqDisable (uint32_t *mask*) `[inline]`

Disable bits in the interrupt mask.

Returns 1 for the bits corresponding to input bits able to generate interrupts. On output-only devices, it will return 0.

Parameters

mask	a bit mask of which bits to disable

Return values

A	32-bit bit map of which bit can generate interrupts.

uint32_t ParallelInput::setIrqEnable (uint32_t *mask*) `[inline]`

Enable bits in the interrupt mask.

Returns 1 for the bits corresponding to input bits able to generate interrupts. On output-only devices, it will return 0.

Parameters

mask	a bit mask of which bits to enable

Return values

A	32-bit bit map of which bit can generate interrupts.

Member Data Documentation

volatile uint32_t* ParallelInput::base

const uint16_t ParallelInput::CAP_INPUT = 0x01 `[static]`

const uint16_t ParallelInput::CAP_INPUT_OUTPUT = 0x03 `[static]`

const uint16_t ParallelInput::CAP_OUTPUT = 0x02 `[static]`

int ParallelInput::data_index = 0

int ParallelInput::dataOut_index = 6

int ParallelInput::direction_index = 5

int ParallelInput::edgeReg_Index = 2

edge register: when a bit is set to 1, the interrupt is generated on an edge

int ParallelInput::irqDelay_index = 7

int ParallelInput::irqEnable_index = 4

int ParallelInput::irqStatus_index = 3

int ParallelInput::polarity_index = 1

polarity: when set to 1, the interrupt is requested if the corresponding bit is low.

The documentation for this class was generated from the following file:

- C:/Alphi/PCIeMiniSoftware/include/**ParallelInput.h**

PcieCra Class Reference

PCIe CRA module controller class.
`#include <PcieCra.h>`

Public Member Functions

- **PcieCra** (volatile void *cra_addr)
  constructor

- void **reset** ()
  Reset the CRA PCIe interface.

- uint32_t **getIrqStatus** ()
  return the interrupt status of the local IRQ lines

- void **setIrqEnableMask** (uint32_t mask)
  Enable/disable the interrupts.

- uint32_t **getIrqEnableMask** ()
  return the interrupt enable mask

- **PCIeMini_status setTxsAvlAddress** (uint32_t txs_addr, uint64_t pageSize, uint16_t nbrOfEntries)
  Set the local Avalon address for the PCIe txs port.

- **PCIeMini_status getMappedAddress** (uint64_t pcieAddress, int tableEntry, uint32_t *localAddress)
  Calculate the DMA address through the txs.

- int **setTrEntry** (int entryNbr, bool is64bitAddress, uint64_t pcieAddress)
  program an entry in the translation table

Detailed Description

PCIe CRA module controller class.

This is a limited software interface to the CRA module of the PCIe adapter that:

- allows to enable/disable the interrupt requests to the PCIe bus and check the status of the local interrupt request lines.
- allows some DMA to/from the PC

Parameters

txs_addr	Address of the txs interface of the PCIe interface chip, in the Avalon address space. It is used to program the DMA controller.

Constructor & Destructor Documentation

PcieCra::PcieCra (volatile void * *cra_addr*)

constructor

This constructor should be only called when the board is opened.

Parameters

cra_addr	Address of the CRA in user space.

Member Function Documentation

uint32_t PcieCra::getIrqEnableMask ()

return the interrupt enable mask

uint32_t PcieCra::getIrqStatus ()

return the interrupt status of the local IRQ lines

In order for the PCIe interface to request an interrupt on the PCIe bus, the bit needs to be set in this register, and the corresponding bit should be set in the interrupt mask register.

PCIeMini_status PcieCra::getMappedAddress (uint64_t *pcieAddress*, int *tableEntry*, uint32_t * *localAddress*)

Calculate the DMA address through the txs.

Parameters

pcieAddress	PCIe address of the PC memory
tableEntry	entry number in the translation table
localAddress	Address to program in the DMA to access the txs port of the PCIe controller

void PcieCra::reset ()

Reset the CRA PCIe interface.

Disable interrupts.

void PcieCra::setIrqEnableMask (uint32_t *mask*)

Enable/disable the interrupts.

Parameters

mask	bit mask of enabled interrupts

int PcieCra::setTrEntry (int *entryNbr*, bool *is64bitAddress*, uint64_t *pcieAddress*)

program an entry in the translation table

Parameters

entryNbr	Index of the entry to set up.
is64bitAddress	True if the address of the target location is a 64-bit address
pcieAddress	Address of the target location

PCIeMini_status PcieCra::setTxsAvlAddress (uint32_t *txs_addr*, uint64_t *pageSize*, uint16_t *nbrOfEntries*)

Set the local Avalon address for the PCIe txs port.

For example, if the core is configured with an address translation table with the following attributes :

- Number of Address Pages—16
  - Size of Address Pages—1 MByte
  - PCI Express Address Size—64 bits then the values in Figure 4–12 are :
- N = 20 (due to the 1 MByte page size)
  - Q = 16 (number of pages)
  - M = 24 (20 + 4 bit page selection)
  - P = 64 In this case, the Avalon address is interpreted as follows :
- Bits[31:24] select the TX slave module port from among other slaves connected to the same master by the system interconnect fabric.The decode is based on the base addresses assigned in Qsys.
  - Bits[23:20] select the address translation table entry.
  - Bits[63:20] of the address translation table entry become PCI Express address bits [63:20].
  - Bits[19:0] are passed throughand become PCI Express address bits[19:0]. The address translation table can be hardwired or dynamically configured at run time.When the IP core is parameterized for dynamic address translation, the address translation table is implemented in memoryand can be accessed through the CRA slave module.This access mode is useful in a typical PCI Express system where address allocation occurs after BIOS initialization.
  - Number of Address Pages—2
  - Size of Address Pages—16 MByte
  - PCI Express Address Size—64 bits then the values in Figure 4–12 are :
- N = 24 (due to the 16 MByte page size)
  - Q = 2 (number of pages)
  - M = 25 (24 + 1 bit page selection)
  - P = 64 In this case, the Avalon address is interpreted as follows :
- Bits[31:24] select the TX slave module port from among other slaves connected to the same master by the system interconnect fabric.The decode is based on the base addresses assigned in Qsys.
  - Bits[24] select the address translation table entry.
  - Bits[63:25] of the address translation table entry become PCI Express address bits [63:20].
  - Bits[23:0] are passed throughand become PCI Express address bits[19:0]. The address translation table can be hardwired or dynamically configured at run time.When the IP core is parameterized for dynamic address translation, the address translation table is implemented in memoryand can be accessed through the CRA slave module.This access mode is useful in a typical PCI Express system where address allocation occurs after BIOS initialization.

Parameters

txs_addr	Local Avalon Address of the txs area
nbrOfEntries	Number of table entries used to calculate the bit pattern
pageSize	size of each translation page (this is currently ignored, hard coded)

The documentation for this class was generated from the following files:

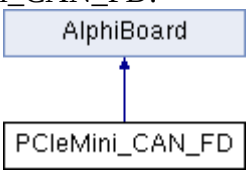
- C:/Alphi/PCIeMiniSoftware/include/**PcieCra.h**
- C:/Alphi/PCIeMiniSoftware/PCIeMini_lib/**PcieCra.cpp**

PCIeMini_CAN_FD Class Reference

PCIeMini_CAN_FD controller board object.

`#include <PCIeMini_CAN_FD.h>`

Inheritance diagram for PCIeMini_CAN_FD:



Public Member Functions

- **PCIeMini_CAN_FD** ()
- **PCIeMini_status open** (int brdNbr)
  Open: connect to an actual board.

- **PCIeMini_status close** ()
  Close the connection to a board object and free the resources.

- **PCIeMini_status reset** ()
  Reset the board controllers.

- void **hwDMAStart** (**TransferDesc** *tfrDesc)
- bool **hwDMAWaitForCompletion** (**TransferDesc** *tfrDesc, bool fPolling)
- bool **hwDMAInterruptEnable** (**MINIPCIE_INT_HANDLER MyDmaIntHandler**, void *pDMA)
- void **hwDMAInterruptDisable** ()
- void **hwDMAProgram** (WD_DMA_PAGE *Page, DWORD dwPages, bool fToDev, uint32_t u32LocalAddr, **TransferDesc** *tfrDesc)
  program the local devices (DMA and CRA) for the DMA

Public Attributes

- **TCAN4550** * **can** [**nbrOfCanInterfaces**]
- CanFdNiosComm * **canNios**
- AlteraPio * **controlRegister**
  Interface to the board control register.

- AlteraPio * **ledPio**
  Interface to the board control register.

- **ParallelInput** * **input0**
- **ParallelInput** * **input1**
- **IrigDecoder** * **irig**
- **AlteraDma** * **dma**
- volatile uint32_t * **dpr**
- volatile uint16_t * **mddr**

Static Public Attributes

- static const uint8_t **nbrOfCanInterfaces** = 4

- static const uint32_t **dpr_offset** = 0x4000
- static const uint32_t **dpr_length** = 0x400

Additional Inherited Members

Detailed Description

PCIeMini_CAN_FD controller board object.

Constructor & Destructor Documentation

PCIeMini_CAN_FD::PCIeMini_CAN_FD ()

The constructor does not take any parameter. The board is not actually usable until the open method connects it to real hardware.

Member Function Documentation

PCIeMini_status PCIeMini_CAN_FD::close ()

Close the connection to a board object and free the resources.

Returns

ERRCODE_NO_ERROR if successful.

void PCIeMini_CAN_FD::hwDMAInterruptDisable () `[virtual]`

Reimplemented from **AlphiBoard** (*p.13*).

bool PCIeMini_CAN_FD::hwDMAInterruptEnable (MINIPCIE_INT_HANDLER *MyDmaIntHandler*, void * *pDMA*) `[virtual]`

Reimplemented from **AlphiBoard** (*p.13*).

void PCIeMini_CAN_FD::hwDMAProgram (WD_DMA_PAGE * *Page*, DWORD *dwPages*, bool *fToDev*, uint32_t *u32LocalAddr*, TransferDesc * *tfrDesc*) `[virtual]`

program the local devices (DMA and CRA) for the DMA

Parameters

fToDev	When true DMA to device, when false DMA from device.

Reimplemented from **AlphiBoard** (*p.13*).

void PCIeMini_CAN_FD::hwDMAStart (TransferDesc * *tfrDesc*) `[virtual]`

Reimplemented from **AlphiBoard** (*p.13*).

bool PCIeMini_CAN_FD::hwDMAWaitForCompletion (TransferDesc * *tfrDesc*, bool *fPolling*) `[virtual]`

Reimplemented from **AlphiBoard** (*p.13*).

PCIeMini_status PCIeMini_CAN_FD::open (int *brdNbr*)

Open: connect to an actual board.

Parameters

brdNbr	The board number is actually system dependent but if you have only one board, it should be 0.

Returns

ERRCODE_NO_ERROR if successful.

PCIeMini_status PCIeMini_CAN_FD::reset ()

Reset the board controllers.

Returns

ERRCODE_NO_ERROR if successful.

Member Data Documentation

TCAN4550* PCIeMini_CAN_FD::can[nbrOfCanInterfaces]

CanFdNiosComm* PCIeMini_CAN_FD::canNios

AlteraPio* PCIeMini_CAN_FD::controlRegister

Interface to the board control register.

AlteraDma* PCIeMini_CAN_FD::dma

volatile uint32_t* PCIeMini_CAN_FD::dpr

const uint32_t PCIeMini_CAN_FD::dpr_length = 0x400 `[static]`

const uint32_t PCIeMini_CAN_FD::dpr_offset = 0x4000 `[static]`

ParallelInput* PCIeMini_CAN_FD::input0

ParallelInput* PCIeMini_CAN_FD::input1

IrigDecoder* PCIeMini_CAN_FD::irig

AlteraPio* PCIeMini_CAN_FD::ledPio

Interface to the board control register.

volatile uint16_t* PCIeMini_CAN_FD::mddr

const uint8_t PCIeMini_CAN_FD::nbrOfCanInterfaces = 4 `[static]`

The documentation for this class was generated from the following files:

- C:/Alphi/PCIeMiniSoftware/include/**PCIeMini_CAN_FD.h**
- **PCIe_Mini_CAN_FD.cpp**

TCAN4550 Class Reference

`#include <TCAN4550.h>`

Public Member Functions

- **TCAN4550** (volatile void *addr, AlteraPio *rstPio, **ParallelInput** *status0, uint8_t nbr)
- void **reset** ()
- void **enableIrq** ()
- void **disableIrq** ()
- bool **MCAN_EnableProtectedRegisters** (void)
  Enable Protected MCAN Registers.

- bool **MCAN_DisableProtectedRegisters** (void)
  Disable Protected MCAN Registers.

- bool **MCAN_ConfigureCCCRRegister** (**TCAN4x5x_MCAN_CCCR_Config** *cccr)
  Configure the MCAN CCCR Register.

- void **MCAN_ReadCCCRRegister** (**TCAN4x5x_MCAN_CCCR_Config** *cccrConfig)
  Read the MCAN CCCR configuration register.

- void **MCAN_ReadDataTimingFD_Simple** (**TCAN4x5x_MCAN_Data_Timing_Simple** *dataTiming)
  Reads the MCAN data time settings, using the simple struct.

- void **MCAN_ReadDataTimingFD_Raw** (**TCAN4x5x_MCAN_Data_Timing_Raw** *dataTiming)
  Reads the MCAN data time settings, using the raw MCAN struct.

- bool **MCAN_ConfigureDataTiming_Simple** (**TCAN4x5x_MCAN_Data_Timing_Simple** *dataTiming)
  Writes the MCAN data time settings, using the simple data timing struct.

- bool **MCAN_ConfigureDataTiming_Raw** (**TCAN4x5x_MCAN_Data_Timing_Raw** *dataTiming)
  Writes the MCAN data time settings, using the raw MCAN data timing struct.

- void **MCAN_ReadNominalTiming_Simple** (**TCAN4x5x_MCAN_Nominal_Timing_Simple** *nomTiming)
  Reads the MCAN nominal/arbitration time settings, using the simple timing struct.

- void **MCAN_ReadNominalTiming_Raw** (**TCAN4x5x_MCAN_Nominal_Timing_Raw** *nomTiming)
  Reads the MCAN nominal/arbitration time settings, using the raw MCAN timing struct.

- bool **MCAN_ConfigureNominalTiming_Simple** (**TCAN4x5x_MCAN_Nominal_Timing_Simple** *nomTiming)
  Writes the MCAN nominal timing settings, using the simple nominal timing struct.

- bool **MCAN_ConfigureNominalTiming_Raw** (**TCAN4x5x_MCAN_Nominal_Timing_Raw** *nomTiming)
  Writes the MCAN nominal timing settings, using the raw MCAN nominal timing struct.

- bool **MRAM_Configure** (**TCAN4x5x_MRAM_Config** *MRAMConfig)
  Configures the MRAM registers.

- void **MRAM_Clear** (void)
  Clear (Zero-fill) the contents of MRAM.

- void **MCAN_ReadInterrupts** (**TCAN4x5x_MCAN_Interrupts** *ir)
  Read the MCAN interrupts.

- void **MCAN_ClearInterrupts** (**TCAN4x5x_MCAN_Interrupts** *ir)
  Clear the MCAN interrupts.

- void **MCAN_ClearInterruptsAll** (void)
  Clear all MCAN interrupts.

- void **MCAN_ReadInterruptEnable** (**TCAN4x5x_MCAN_Interrupt_Enable** *ie)
  Read the MCAN interrupt enable register.

- void **MCAN_ConfigureInterruptEnable** (**TCAN4x5x_MCAN_Interrupt_Enable** *ie)
  Configures the MCAN interrupt enable register.

- uint8_t **MCAN_ReadNextFIFO** (**TCAN4x5x_MCAN_FIFO_Enum** FIFODefine, **TCAN4x5x_MCAN_RX_Header** *header, uint8_t dataPayload[])
  Read the next MCAN FIFO element.

- uint8_t **MCAN_ReadRXBuffer** (uint8_t bufIndex, **TCAN4x5x_MCAN_RX_Header** *header, uint8_t dataPayload[])
  Read the specified RX buffer element.

- uint32_t **MCAN_WriteTXBuffer** (uint8_t bufIndex, **TCAN4x5x_MCAN_TX_Header** *header, uint8_t dataPayload[])
  Write CAN message to the specified TX buffer.

- bool **MCAN_TransmitBufferContents** (uint8_t bufIndex)
  Transmit TX buffer contents of the specified tx buffer.

- bool **MCAN_WriteSIDFilter** (uint8_t filterIndex, **TCAN4x5x_MCAN_SID_Filter** *filter)
  Write MCAN Standard ID filter into MRAM.

- bool **MCAN_WriteXIDFilter** (uint8_t fifoIndex, **TCAN4x5x_MCAN_XID_Filter** *filter)
  Write MCAN Extended ID filter into MRAM.

- uint8_t **MCAN_DLCtoBytes** (uint8_t inputDLC)

Converts the CAN message DLC hex value to the number of bytes it corresponds to.

- uint8_t **MCAN_TXRXESC_DataByteValue** (uint8_t inputESCValue)
  Converts the MCAN ESC (Element Size) value to number of bytes that it corresponds to.

- uint16_t **Device_ReadDeviceVersion** (void)
  Read the TCAN4x5x device version register.

- void **Device_ReadDeviceIdent** (uint32_t *id)
  Read the TCAN4x5x device identification.

- void **Device_ReadInterrupts** (**TCAN4x5x_Device_Interrupts** *ir)
  Read the device interrupts.

- void **Device_ClearInterrupts** (**TCAN4x5x_Device_Interrupts** *ir)
  Clear the device interrupts.

- void **Device_ClearInterruptsAll** (void)
  Clear all device interrupts.

- void **Device_ReadInterruptEnable** (**TCAN4x5x_Device_Interrupt_Enable** *ie)
  Read the device interrupt enable register.

- bool **Device_ConfigureInterruptEnable** (**TCAN4x5x_Device_Interrupt_Enable** *ie)
  Configures the device interrupt enable register.

- bool **Device_SetMode** (**TCAN4x5x_Device_Mode_Enum** modeDefine)
  Sets the TCAN4x5x device mode.

- **TCAN4x5x_Device_Mode_Enum Device_ReadMode** (void)
  Reads the TCAN4x5x device mode.

- bool **Device_EnableTestMode** (**TCAN4x5x_Device_Test_Mode_Enum** modeDefine)
  Sets the TCAN4x5x device test mode.

- bool **Device_DisableTestMode** (void)
  Disables the TCAN4x5x device test mode.

- **TCAN4x5x_Device_Test_Mode_Enum Device_ReadTestMode** (void)
  Reads the TCAN4x5x device test mode.

- bool **WDT_Configure** (**TCAN4x5x_WDT_Timer_Enum** WDTtimeout)
  Configure the watchdog.

- **TCAN4x5x_WDT_Timer_Enum WDT_Read** (void)
  Read the watchdog configuration.

- bool **WDT_Enable** (void)
  Enable the watchdog timer.

- bool **WDT_Disable** (void)
  Disable the watchdog timer.

- void **WDT_Reset** (void)
  Reset the watchdog timer.

Public Attributes

- uint8_t **msgBufferOut** [**BUFF_LEN**]
- uint8_t **msgBufferIn** [**BUFF_LEN**]
- int **msgLength**
- **TcanInterface** * **can**
- **ParallelInput** * **status**
- uint8_t **slaveNbr**

Static Public Attributes

- static const int **BUFF_LEN** = 256

Constructor & Destructor Documentation

TCAN4550::TCAN4550 (volatile void * *addr*, AlteraPio * *rstPio*, ParallelInput * *status0*, uint8_t *nbr*) `[inline]`

Member Function Documentation

void TCAN4550::Device_ClearInterrupts (TCAN4x5x_Device_Interrupts * *ir*)

Clear the device interrupts.

Will attempt to clear any interrupts that are marked as a '1' in the passed **`TCAN4x5x_Device_Interrupts`** struct

Parameters

**ir*	is a pointer to a **`TCAN4x5x_Device_Interrupts`** struct containing the interrupt bit fields that will be updated

void TCAN4550::Device_ClearInterruptsAll (void)

Clear all device interrupts.

Clears all device interrupts

bool TCAN4550::Device_ConfigureInterruptEnable (TCAN4x5x_Device_Interrupt_Enable * *ie*)

Configures the device interrupt enable register.

Configures the device interrupt enable register based on the passed **`TCAN4x5x_Device_Interrupt_Enable`** struct

Parameters

**ie*	is a pointer to a **`TCAN4x5x_Device_Interrupt_Enable`** struct containing the desired enabled interrupt bits

Returns

`true` if configuration successfully done, `false` if not

bool TCAN4550::Device_DisableTestMode (void)

Disables the TCAN4x5x device test mode.

Returns

`true` if disabling test mode was successful, `false` if not

bool TCAN4550::Device_EnableTestMode (TCAN4x5x_Device_Test_Mode_Enum *modeDefine*)

Sets the TCAN4x5x device test mode.

Sets the TCAN4x5x device test mode based on the input `modeDefine` enum

Parameters

modeDefine	is an `TCAN4x5x_Device_Test_Mode_Enum` enum

Returns

`true` if configuration successfully done, `false` if not

void TCAN4550::Device_ReadDeviceIdent (uint32_t * *id*)

Read the TCAN4x5x device identification.

Parameters

id	an array of uint32_t for the results

Returns

The register value for the device version register

uint16_t TCAN4550::Device_ReadDeviceVersion (void)

Read the TCAN4x5x device version register.

Returns

The register value for the device version register

void TCAN4550::Device_ReadInterruptEnable (TCAN4x5x_Device_Interrupt_Enable * *ie*)

Read the device interrupt enable register.

Reads the device interrupt enable register and updates the passed **`TCAN4x5x_Device_Interrupt_Enable`** struct

Parameters

**ie*	is a pointer to a **`TCAN4x5x_Device_Interrupt_Enable`** struct containing the interrupt bit fields that will be updated

void TCAN4550::Device_ReadInterrupts (TCAN4x5x_Device_Interrupts * *ir*)

Read the device interrupts.

Reads the device interrupts and updates a **`TCAN4x5x_Device_Interrupts`** struct that is passed to the function

Parameters

**ir*	is a pointer to a **`TCAN4x5x_Device_Interrupts`** struct containing the interrupt bit fields that will be updated

TCAN4x5x_Device_Mode_Enum TCAN4550::Device_ReadMode (void)

Reads the TCAN4x5x device mode.

Reads the TCAN4x5x device mode and returns a `modeDefine` enum

Returns

A `TCAN4x5x_Device_Mode_Enum` enum of the current state

TCAN4x5x_Device_Test_Mode_Enum TCAN4550::Device_ReadTestMode (void)

Reads the TCAN4x5x device test mode.

Returns

an `TCAN4x5x_Device_Test_Mode_Enum` of the current device test mode

bool TCAN4550::Device_SetMode (TCAN4x5x_Device_Mode_Enum *modeDefine*)

Sets the TCAN4x5x device mode.

Sets the TCAN4x5x device mode based on the input `modeDefine` enum

Parameters

modeDefine	is an `TCAN4x5x_Device_Mode_Enum` enum

Returns

`true` if configuration successfully done, `false` if not

void TCAN4550::disableIrq ()`[inline]`

void TCAN4550::enableIrq ()`[inline]`

void TCAN4550::MCAN_ClearInterrupts (TCAN4x5x_MCAN_Interrupts * *ir*)

Clear the MCAN interrupts.

Will attempt to clear any interrupts that are marked as a '1' in the passed **`TCAN4x5x_MCAN_Interrupts`** struct

Parameters

**ir*	is a pointer to a **`TCAN4x5x_MCAN_Interrupts`** struct containing the interrupt bit fields that will be updated

void TCAN4550::MCAN_ClearInterruptsAll (void)

Clear all MCAN interrupts.

Clears all MCAN interrupts

bool TCAN4550::MCAN_ConfigureCCCRRegister (TCAN4x5x_MCAN_CCCR_Config * *cccrConfig*)

Configure the MCAN CCCR Register.

Configures the bits of the CCCR register to match the CCCR config struct

Warning

This function writes to protected MCAN registers

Note

Requires that protected registers have been unlocked using `TCAN4x5x_MCAN_EnableProtectedRegisters()` and `TCAN4x5x_MCAN_DisableProtectedRegisters()` be used to lock the registers after configuration

Parameters

**cccrConfig*	is a pointer to a **`TCAN4x5x_MCAN_CCCR_Config`** struct containing the configuration bits

Returns

`true` if successfully enabled, otherwise return `false`

bool TCAN4550::MCAN_ConfigureDataTiming_Raw (TCAN4x5x_MCAN_Data_Timing_Raw * *dataTiming*)

Writes the MCAN data time settings, using the raw MCAN data timing struct.

Writes the data timing information to MCAN using the input from the `*dataTiming` pointer

Warning

This function writes to protected MCAN registers

Note

Requires that protected registers have been unlocked using `TCAN4x5x_MCAN_EnableProtectedRegisters()` and `TCAN4x5x_MCAN_DisableProtectedRegisters()` be used to lock the registers after configuration

Parameters

**dataTiming*	is a pointer of a **`TCAN4x5x_MCAN_Data_Timing_Raw`** struct containing the raw data timing information

Returns

`true` if successfully enabled, otherwise return `false`

bool TCAN4550::MCAN_ConfigureDataTiming_Simple (TCAN4x5x_MCAN_Data_Timing_Simple * *dataTiming*)

Writes the MCAN data time settings, using the simple data timing struct.

Writes the data timing information to MCAN using the input from the `*dataTiming` pointer

Warning

This function writes to protected MCAN registers

Note

Requires that protected registers have been unlocked using `TCAN4x5x_MCAN_EnableProtectedRegisters()` and `TCAN4x5x_MCAN_DisableProtectedRegisters()` be used to lock the registers after configuration

Parameters

**dataTiming*	is a pointer of a **`TCAN4x5x_MCAN_Data_Timing_Simple`** struct containing the simplified data timing information

Returns

`true` if successfully enabled, otherwise return `false`

void TCAN4550::MCAN_ConfigureInterruptEnable (TCAN4x5x_MCAN_Interrupt_Enable * *ie*)

Configures the MCAN interrupt enable register.

Configures the MCAN interrupt enable register based on the passed **`TCAN4x5x_MCAN_Interrupt_Enable`** struct Also enables MCAN interrupts out to the INT1 pin.

Parameters

**ie*	is a pointer to a **`TCAN4x5x_MCAN_Interrupt_Enable`** struct containing the desired enabled interrupt bits

bool TCAN4550::MCAN_ConfigureNominalTiming_Raw (TCAN4x5x_MCAN_Nominal_Timing_Raw * *nomTiming*)

Writes the MCAN nominal timing settings, using the raw MCAN nominal timing struct.

Writes the data timing information to MCAN using the input from the `*nomTiming` pointer

Warning

This function writes to protected MCAN registers

Note

Requires that protected registers have been unlocked using `TCAN4x5x_MCAN_EnableProtectedRegisters()` and `TCAN4x5x_MCAN_DisableProtectedRegisters()` be used to lock the registers after configuration

Parameters

**nomTiming*	is a pointer of a **`TCAN4x5x_MCAN_Nominal_Timing_Raw`** struct containing the raw MCAN nominal timing information

Returns

`true` if successfully enabled, otherwise return `false`

bool TCAN4550::MCAN_ConfigureNominalTiming_Simple (TCAN4x5x_MCAN_Nominal_Timing_Simple * *nomTiming*)

Writes the MCAN nominal timing settings, using the simple nominal timing struct.

Writes the data timing information to MCAN using the input from the `*nomTiming` pointer

Warning

This function writes to protected MCAN registers

Note

Requires that protected registers have been unlocked using `TCAN4x5x_MCAN_EnableProtectedRegisters()` and `TCAN4x5x_MCAN_DisableProtectedRegisters()` be used to lock the registers after configuration

Parameters

**nomTiming*	is a pointer of a **`TCAN4x5x_MCAN_Nominal_Timing_Simple`** struct containing the simplified nominal timing information

Returns

`true` if successfully enabled, otherwise return `false`

bool TCAN4550::MCAN_DisableProtectedRegisters (void)

Disable Protected MCAN Registers.

Attempts to disable CCCR.CCE and CCCR.INIT to disallow writes to protected registers

Returns

`true` if successfully enabled, otherwise return `false`

uint8_t TCAN4550::MCAN_DLCtoBytes (uint8_t *inputDLC*)

Converts the CAN message DLC hex value to the number of bytes it corresponds to.

Parameters

inputDLC	is the DLC value from/to a CAN message struct

Returns

The number of bytes of data (0-64 bytes)

bool TCAN4550::MCAN_EnableProtectedRegisters (void)

Enable Protected MCAN Registers.

Attempts to enable CCCR.CCE and CCCR.INIT to allow writes to protected registers, needed for MCAN configuration

Returns

`true` if successfully enabled, otherwise return `false`

void TCAN4550::MCAN_ReadCCCRRegister (TCAN4x5x_MCAN_CCCR_Config * *cccrConfig*)

Read the MCAN CCCR configuration register.

Reads the MCAN CCCR configuration register and updates the passed **`TCAN4x5x_MCAN_CCCR_Config`** struct

Parameters

**cccrConfig*	is a pointer to a **`TCAN4x5x_MCAN_CCCR_Config`** struct containing the CCCR bit fields that will be updated

void TCAN4550::MCAN_ReadDataTimingFD_Raw (TCAN4x5x_MCAN_Data_Timing_Raw * *dataTiming*)

Reads the MCAN data time settings, using the raw MCAN struct.

Reads the MCAN data timing registers and updates the `*dataTiming` struct

Parameters

**dataTiming*	is a pointer of a **`TCAN4x5x_MCAN_Data_Timing_Simple`** struct containing the raw data timing information

void TCAN4550::MCAN_ReadDataTimingFD_Simple (TCAN4x5x_MCAN_Data_Timing_Simple * *dataTiming*)

Reads the MCAN data time settings, using the simple struct.

Reads the MCAN data timing registers and updates the `*dataTiming` struct

Warning

This function writes to protected MCAN registers

Note

Requires that protected registers have been unlocked using `TCAN4x5x_MCAN_EnableProtectedRegisters()` and `TCAN4x5x_MCAN_DisableProtectedRegisters()` be used to lock the registers after configuration

Parameters

**dataTiming*	is a pointer of a **`TCAN4x5x_MCAN_Data_Timing_Simple`** struct containing the simplified data timing information

void TCAN4550::MCAN_ReadInterruptEnable (TCAN4x5x_MCAN_Interrupt_Enable * *ie*)

Read the MCAN interrupt enable register.

Reads the MCAN interrupt enable register and updates the passed **`TCAN4x5x_MCAN_Interrupt_Enable`** struct

Parameters

**ie*	is a pointer to a **`TCAN4x5x_MCAN_Interrupt_Enable`** struct containing the interrupt bit fields that will be updated

void TCAN4550::MCAN_ReadInterrupts (TCAN4x5x_MCAN_Interrupts * *ir*)

Read the MCAN interrupts.

Reads the MCAN interrupts and updates a `MCAN_Interrupts` struct that is passed to the function

Parameters

**ir*	is a pointer to a `MCAN_Interrupts` struct containing the interrupt bit fields that will be updated

uint8_t TCAN4550::MCAN_ReadNextFIFO (TCAN4x5x_MCAN_FIFO_Enum *FIFODefine*, TCAN4x5x_MCAN_RX_Header * *header*, uint8_t *dataPayload*[])

Read the next MCAN FIFO element.

This function will read the next MCAN FIFO element specified and return the corresponding header information and data payload. The start address of the elment is automatically calculated by looking at the MCAN's register that says where the next element to read exists.

Parameters

FIFODefine	is an `TCAN4x5x_MCAN_FIFO_Enum` enum corresponding to either RXFIFO0 or RXFIFO1
**header*	is a pointer to a **`TCAN4x5x_MCAN_RX_Header`** struct containing the CAN-specific header information
dataPayload[]	is a byte array that will be updated with the read data

Warning

`dataPayload` [] must be at least as big as the largest possible data payload, otherwise writing to out of bounds memory may occur

Returns

the number of bytes that were read from the TCAN4x5x and stored into `dataPayload` []

void TCAN4550::MCAN_ReadNominalTiming_Raw (TCAN4x5x_MCAN_Nominal_Timing_Raw * *nomTiming*)

Reads the MCAN nominal/arbitration time settings, using the raw MCAN timing struct.

Reads the MCAN nominal timing registers and updates the `*nomTiming` struct

Parameters

**nomTiming*	is a pointer of a **`TCAN4x5x_MCAN_Nominal_Timing_Raw`** struct containing the raw MCAN nominal timing information

void TCAN4550::MCAN_ReadNominalTiming_Simple (TCAN4x5x_MCAN_Nominal_Timing_Simple * *nomTiming*)

Reads the MCAN nominal/arbitration time settings, using the simple timing struct.

Reads the MCAN nominal timing registers and updates the `*nomTiming` struct

Parameters

**nomTiming*	is a pointer of a **`TCAN4x5x_MCAN_Nominal_Timing_Simple`** struct containing the simplified nominal timing information

uint8_t TCAN4550::MCAN_ReadRXBuffer (uint8_t *bufIndex*, TCAN4x5x_MCAN_RX_Header * *header*, uint8_t *dataPayload*[])

Read the specified RX buffer element.

This function will read the specified MCAN buffer element and return the corresponding header information and data payload. The start address of the element is automatically calculated.

Parameters

bufIndex	is the RX buffer index to read from (starts at 0)
**header*	is a pointer to a **`TCAN4x5x_MCAN_RX_Header`** struct containing the CAN-specific header information
dataPayload[]	is a byte array that will be updated with the read data

Warning

`dataPayload` [] must be at least as big as the largest possible data payload, otherwise writing to out of bounds memory may occur

Returns

the number of bytes that were read from the TCAN4x5x and stored into `dataPayload` []

bool TCAN4550::MCAN_TransmitBufferContents (uint8_t *bufIndex*)

Transmit TX buffer contents of the specified tx buffer.

Writes the specified buffer index bit value into the TXBAR register to request a message to send

Parameters

bufIndex	is the TX buffer index to write to (starts at 0)

Warning

Function does NOT check if the buffer contents are valid

Returns

`true` if the request was queued, `false` if the buffer value was invalid (out of range)

uint8_t TCAN4550::MCAN_TXRXESC_DataByteValue (uint8_t *inputESCValue*)

Converts the MCAN ESC (Element Size) value to number of bytes that it corresponds to.

Parameters

inputESCValue	is the value from an element size configuration register

Returns

The number of bytes of data (8-64 bytes)

bool TCAN4550::MCAN_WriteSIDFilter (uint8_t *filterIndex*, TCAN4x5x_MCAN_SID_Filter * *filter*)

Write MCAN Standard ID filter into MRAM.

This function will write a standard ID MCAN filter to a specified filter element

Parameters

filterIndex	is the SID filter index in MRAM to write to (starts at 0)
**filter*	is a pointer to a `MCAN_SID_Filter` struct containing the MCAN filter information

Returns

`true` if write was successful, `false` if not

uint32_t TCAN4550::MCAN_WriteTXBuffer (uint8_t *bufIndex*, TCAN4x5x_MCAN_TX_Header * *header*, uint8_t *dataPayload*[])

Write CAN message to the specified TX buffer.

This function will write a CAN message to a specified TX buffer that can be transmitted at a later time with the **`MCAN_TransmitBufferContents()`** function

Parameters

bufIndex	is the TX buffer index to write to (starts at 0)
**header*	is a pointer to a `MCAN_TX_Header` struct containing the CAN-specific header information
dataPayload[]	is a byte array that contains the data payload

Warning

`dataPayload` [] must be at least as big as the specified DLC size inside the `*header` struct

Returns

the number of bytes that were read from the TCAN4x5x and stored into `dataPayload` []

bool TCAN4550::MCAN_WriteXIDFilter (uint8_t *filterIndex*, TCAN4x5x_MCAN_XID_Filter * *filter*)

Write MCAN Extended ID filter into MRAM.

This function will write an extended ID MCAN filter to a specified filter element

Parameters

filterIndex	is the XID filter index in MRAM to write to (starts at 0)
**filter*	is a pointer to a `MCAN_XID_Filter` struct containing the MCAN filter information

Returns

`true` if write was successful, `false` if not

void TCAN4550::MRAM_Clear (void)

Clear (Zero-fill) the contents of MRAM.

Write 0s to every address in MRAM. Useful for initializing the MRAM to known values during initial configuration so that accidental ECC errors do not happen

bool TCAN4550::MRAM_Configure (TCAN4x5x_MRAM_Config * *MRAMConfig*)

Configures the MRAM registers.

Uses the `*MRAMConfig` pointer to set up the various sections of the MRAM memory space. There are several different elements that may be configured in the MRAM, including their number of elements, as well as size of elements. This function will automatically generate the start addresses for each of the appropriate MRAM sections, attempting to place them immediately back-to-back. This function will check for over allocated memory conditions, and return `false` if this is found to be the case.

Warning

This function writes to protected MCAN registers

Note

Requires that protected registers have been unlocked using `TCAN4x5x_MCAN_EnableProtectedRegisters()` and `TCAN4x5x_MCAN_DisableProtectedRegisters()` be used to lock the registers after configuration

Parameters

**MRAMConfig*	is a pointer of a **`TCAN4x5x_MRAM_Config`** struct containing the desired MRAM configuration

Returns

`true` if successful, otherwise return `false`

void TCAN4550::reset () `[inline]`

bool TCAN4550::WDT_Configure (TCAN4x5x_WDT_Timer_Enum *WDTtimeout*)

Configure the watchdog.

Parameters

WDTtimeout	is an `TCAN4x5x_WDT_Timer_Enum` enum of different times for the watch dog window

Returns

`true` if successfully configured, or `false` otherwise

bool TCAN4550::WDT_Disable (void)

Disable the watchdog timer.

Returns

`true` if successfully disabled, or `false` otherwise

bool TCAN4550::WDT_Enable (void)

Enable the watchdog timer.

Returns

`true` if successfully enabled, or `false` otherwise

TCAN4x5x_WDT_Timer_Enum TCAN4550::WDT_Read (void)

Read the watchdog configuration.

Returns

an `TCAN4x5x_WDT_Timer_Enum` enum of the currently configured time window

void TCAN4550::WDT_Reset (void)

Reset the watchdog timer.

Member Data Documentation

const int TCAN4550::BUFF_LEN = 256 `[static]`

TcanInterface* TCAN4550::can

uint8_t TCAN4550::msgBufferIn[BUFF_LEN]

uint8_t TCAN4550::msgBufferOut[BUFF_LEN]

int TCAN4550::msgLength

uint8_t TCAN4550::slaveNbr

ParallelInput* TCAN4550::status

The documentation for this class was generated from the following files:

- C:/Alphi/PCIeMiniSoftware/include/**TCAN4550.h**
- **TCAN4550.cpp**

TCAN4x5x_Device_Interrupt_Enable Struct Reference

Struct containing the device interrupt enable bit field.
`#include <TCAN4x5x_Data_Structs.h>`

Public Attributes

- union {
- uint32_t **word**
  Full register as single 32-bit word.

- struct {
- uint8_t **RESERVED1**: 8
  DEV_IE[0:7] : RESERVED.

- uint8_t **CANDOMEN**: 1
  DEV_IE[8] : CANDOM, Can bus stuck dominant.

- uint8_t **RESERVED2**: 1
  DEV_IE[9] : RESERVED.

- uint8_t **CANTOEN**: 1
  DEV_IE[10] : CANTO, CAN Timeout.

- uint8_t **RESERVED3**: 1
  DEV_IE[11] : RESERVED.

- uint8_t **FRAME_OVFEN**: 1
  DEV_IE[12] : FRAME_OVF, Frame Error Overflow (If Selective Wake is equipped)

- uint8_t **WKERREN**: 1
  DEV_IE[13] : WKERR, Wake Error.

- uint8_t **LWUEN**: 1
  DEV_IE[14] : LWU, Local Wake Up.

- uint8_t **CANINTEN**: 1
  DEV_IE[15] : CANINT, CAN Bus Wake Up Interrupt.

- uint8_t **ECCERREN**: 1
  DEV_IE[16] : ECCERR, MRAM ECC Error.

- uint8_t **RESERVED4**: 1
  DEV_IE[17] : Reserved.

- uint8_t **WDTOEN**: 1
  DEV_IE[18] : WDTO, Watchdog Time Out.

- uint8_t **TSDEN**: 1
  DEV_IE[19] : TSD, Thermal Shut Down.

- uint8_t **PWRONEN**: 1
  DEV_IE[20] : PWRON, Power On Interrupt.

- uint8_t **UVIOEN**: 1
  DEV_IE[21] : UVIO, Undervoltage on UVIO.

- uint8_t **UVSUPEN**: 1
  DEV_IE[22] : UVSUP, Undervoltage on VSUP and VCCOUT.

- uint8_t **SMSEN**: 1
  DEV_IE[23] : SMS, Sleep Mode Status Flag. Set when sleep mode is entered due to WKERR, UVIO, or TSD faults.

- uint8_t **CANBUSBATEN**: 1
  DEV_IE[24] : CANBUSBAT, CAN Shorted to VBAT.

- uint8_t **CANBUSGNDEN**: 1
  DEV_IE[25] : CANBUSGND, CAN Shorted to GND.

- uint8_t **CANBUSOPENEN**: 1
  DEV_IE[26] : CANBUSOPEN, CAN Open fault.

- uint8_t **CANLGNDEN**: 1
  DEV_IE[27] : CANLGND, CANL GND.

- uint8_t **CANHBATEN**: 1
  DEV_IE[28] : CANHBAT, CANH to VBAT.

- uint8_t **CANHCANLEN**: 1
  DEV_IE[29] : CANHCANL, CANH and CANL shorted.

- uint8_t **CANBUSTERMOPENEN**: 1
  DEV_IE[30] : CANBUSTERMOPEN, CAN Bus has termination point open.

- uint8_t **CANBUSNORMEN**: 1
  DEV_IE[31] : CANBUSNOM, CAN Bus is normal flag.

- }
- };

Detailed Description

Struct containing the device interrupt enable bit field.

Member Data Documentation

union { ... }

uint8_t TCAN4x5x_Device_Interrupt_Enable::CANBUSBATEN

DEV_IE[24] : CANBUSBAT, CAN Shorted to VBAT.

uint8_t TCAN4x5x_Device_Interrupt_Enable::CANBUSGNDEN

DEV_IE[25] : CANBUSGND, CAN Shorted to GND.

uint8_t TCAN4x5x_Device_Interrupt_Enable::CANBUSNORMEN

DEV_IE[31] : CANBUSNOM, CAN Bus is normal flag.

uint8_t TCAN4x5x_Device_Interrupt_Enable::CANBUSOPENEN

DEV_IE[26] : CANBUSOPEN, CAN Open fault.

uint8_t TCAN4x5x_Device_Interrupt_Enable::CANBUSTERMOPENEN

DEV_IE[30] : CANBUSTERMOPEN, CAN Bus has termination point open.

uint8_t TCAN4x5x_Device_Interrupt_Enable::CANDOMEN

DEV_IE[8] : CANDOM, Can bus stuck dominant.

uint8_t TCAN4x5x_Device_Interrupt_Enable::CANHBATEN

DEV_IE[28] : CANHBAT, CANH to VBAT.

uint8_t TCAN4x5x_Device_Interrupt_Enable::CANHCANLEN

DEV_IE[29] : CANHCANL, CANH and CANL shorted.

uint8_t TCAN4x5x_Device_Interrupt_Enable::CANINTEN

DEV_IE[15] : CANINT, CAN Bus Wake Up Interrupt.

uint8_t TCAN4x5x_Device_Interrupt_Enable::CANLGNDEN

DEV_IE[27] : CANLGND, CANL GND.

uint8_t TCAN4x5x_Device_Interrupt_Enable::CANTOEN

DEV_IE[10] : CANTO, CAN Timeout.

uint8_t TCAN4x5x_Device_Interrupt_Enable::ECCERREN

DEV_IE[16] : ECCERR, MRAM ECC Error.

uint8_t TCAN4x5x_Device_Interrupt_Enable::FRAME_OVFEN

DEV_IE[12] : FRAME_OVF, Frame Error Overflow (If Selective Wake is equipped)

uint8_t TCAN4x5x_Device_Interrupt_Enable::LWUEN

DEV_IE[14] : LWU, Local Wake Up.

uint8_t TCAN4x5x_Device_Interrupt_Enable::PWRONEN

DEV_IE[20] : PWRON, Power On Interrupt.

uint8_t TCAN4x5x_Device_Interrupt_Enable::RESERVED1

DEV_IE[0:7] : RESERVED.

uint8_t TCAN4x5x_Device_Interrupt_Enable::RESERVED2

DEV_IE[9] : RESERVED.

uint8_t TCAN4x5x_Device_Interrupt_Enable::RESERVED3

DEV_IE[11] : RESERVED.

uint8_t TCAN4x5x_Device_Interrupt_Enable::RESERVED4

DEV_IE[17] : Reserved.

uint8_t TCAN4x5x_Device_Interrupt_Enable::SMSEN

DEV_IE[23] : SMS, Sleep Mode Status Flag. Set when sleep mode is entered due to WKERR, UVIO, or TSD faults.

uint8_t TCAN4x5x_Device_Interrupt_Enable::TSDEN

DEV_IE[19] : TSD, Thermal Shut Down.

uint8_t TCAN4x5x_Device_Interrupt_Enable::UVIOEN

DEV_IE[21] : UVIO, Undervoltage on UVIO.

uint8_t TCAN4x5x_Device_Interrupt_Enable::UVSUPEN

DEV_IE[22] : UVSUP, Undervoltage on VSUP and VCCOUT.

uint8_t TCAN4x5x_Device_Interrupt_Enable::WDTOEN

DEV_IE[18] : WDTO, Watchdog Time Out.

uint8_t TCAN4x5x_Device_Interrupt_Enable::WKERREN

DEV_IE[13] : WKERR, Wake Error.

uint32_t TCAN4x5x_Device_Interrupt_Enable::word

Full register as single 32-bit word.

The documentation for this struct was generated from the following file:

- C:/Alphi/PCIeMiniSoftware/include/**TCAN4x5x_Data_Structs.h**

TCAN4x5x_Device_Interrupts Struct Reference

Struct containing the device interrupt bit field.
`#include <TCAN4x5x_Data_Structs.h>`

Public Attributes

- union {
- uint32_t **word**
  Full register as single 32-bit word.

- struct {
- uint8_t **VTWD**: 1
  DEV_IR[0] VTWD: Global Voltage, Temp, or Watchdog (if equipped) Interrupt.

- uint8_t **M_CAN_INT**: 1
  DEV_IR[1] M_CAN_INT: There are MCAN interrupts pending.

- uint8_t **SWERR**: 1
  DEV_IR[2] : Selective Wake Error (If equipped)

- uint8_t **SPIERR**: 1
  DEV_IR[3] : SPI Error.

- uint8_t **CBF**: 1
  DEV_IR[4] : CBF, CAN Bus Fault.

- uint8_t **CANERR**: 1
  DEV_IR[5] : CANERR, CAN Error.

- uint8_t **WKRQ**: 1
  DEV_IR[6] : WKRQ, Wake Request.

- uint8_t **GLOBALERR**: 1
  DEV_IR[7] : GLOBALERR, Global Error. Is the OR output of all interrupts.

- uint8_t **CANDOM**: 1
  DEV_IR[8] : CANDOM, Can bus stuck dominant.

- uint8_t **RESERVED**: 1
  DEV_IR[9] : RESERVED.

- uint8_t **CANTO**: 1
  DEV_IR[10] : CANTO, CAN Timeout.

- uint8_t **RESERVED2**: 1
  DEV_IR[11] : RESERVED.

- uint8_t **FRAME_OVF**: 1
  DEV_IR[12] : FRAME_OVF, Frame Error Overflow (If Selective Wake is equipped)

- uint8_t **WKERR**: 1
  DEV_IR[13] : WKERR, Wake Error.

- uint8_t **LWU**: 1
  DEV_IR[14] : LWU, Local Wake Up.

- uint8_t **CANINT**: 1
  DEV_IR[15] : CANINT, CAN Bus Wake Up Interrupt.

- uint8_t **ECCERR**: 1
  DEV_IR[16] : ECCERR, MRAM ECC Error.

- uint8_t **RESERVED3**: 1
  DEV_IR[17] : Reserved.

- uint8_t **WDTO**: 1
  DEV_IR[18] : WDTO, Watchdog Time Out.

- uint8_t **TSD**: 1
  DEV_IR[19] : TSD, Thermal Shut Down.

- uint8_t **PWRON**: 1
  DEV_IR[20] : PWRON, Power On Interrupt.

- uint8_t **UVIO**: 1
  DEV_IR[21] : UVIO, Undervoltage on UVIO.

- uint8_t **UVSUP**: 1
  DEV_IR[22] : UVSUP, Undervoltage on VSUP and VCCOUT.

- uint8_t **SMS**: 1
  DEV_IR[23] : SMS, Sleep Mode Status Flag. Set when sleep mode is entered due to WKERR, UVIO, or TSD faults.

- uint8_t **CANBUSBAT**: 1
  DEV_IR[24] : CANBUSBAT, CAN Shorted to VBAT.

- uint8_t **CANBUSGND**: 1
  DEV_IR[25] : CANBUSGND, CAN Shorted to GND.

- uint8_t **CANBUSOPEN**: 1
  DEV_IR[26] : CANBUSOPEN, CAN Open fault.

- uint8_t **CANLGND**: 1

DEV_IR[27] : CANLGND, CANL GND.

- uint8_t **CANHBAT**: 1
  DEV_IR[28] : CANHBAT, CANH to VBAT.

- uint8_t **CANHCANL**: 1
  DEV_IR[29] : CANHCANL, CANH and CANL shorted.

- uint8_t **CANBUSTERMOPEN**: 1
  DEV_IR[30] : CANBUSTERMOPEN, CAN Bus has termination point open.

- uint8_t **CANBUSNORM**: 1
  DEV_IR[31] : CANBUSNOM, CAN Bus is normal flag.

- }
- };

Detailed Description

Struct containing the device interrupt bit field.

Member Data Documentation

union { ... }

uint8_t TCAN4x5x_Device_Interrupts::CANBUSBAT

DEV_IR[24] : CANBUSBAT, CAN Shorted to VBAT.

uint8_t TCAN4x5x_Device_Interrupts::CANBUSGND

DEV_IR[25] : CANBUSGND, CAN Shorted to GND.

uint8_t TCAN4x5x_Device_Interrupts::CANBUSNORM

DEV_IR[31] : CANBUSNOM, CAN Bus is normal flag.

uint8_t TCAN4x5x_Device_Interrupts::CANBUSOPEN

DEV_IR[26] : CANBUSOPEN, CAN Open fault.

uint8_t TCAN4x5x_Device_Interrupts::CANBUSTERMOPEN

DEV_IR[30] : CANBUSTERMOPEN, CAN Bus has termination point open.

uint8_t TCAN4x5x_Device_Interrupts::CANDOM

DEV_IR[8] : CANDOM, Can bus stuck dominant.

uint8_t TCAN4x5x_Device_Interrupts::CANERR

DEV_IR[5] : CANERR, CAN Error.

uint8_t TCAN4x5x_Device_Interrupts::CANHBAT

DEV_IR[28] : CANHBAT, CANH to VBAT.

uint8_t TCAN4x5x_Device_Interrupts::CANHCANL

DEV_IR[29] : CANHCANL, CANH and CANL shorted.

uint8_t TCAN4x5x_Device_Interrupts::CANINT

DEV_IR[15] : CANINT, CAN Bus Wake Up Interrupt.

uint8_t TCAN4x5x_Device_Interrupts::CANLGND

DEV_IR[27] : CANLGND, CANL GND.

uint8_t TCAN4x5x_Device_Interrupts::CANTO

DEV_IR[10] : CANTO, CAN Timeout.

uint8_t TCAN4x5x_Device_Interrupts::CBF

DEV_IR[4] : CBF, CAN Bus Fault.

uint8_t TCAN4x5x_Device_Interrupts::ECCERR

DEV_IR[16] : ECCERR, MRAM ECC Error.

uint8_t TCAN4x5x_Device_Interrupts::FRAME_OVF

DEV_IR[12] : FRAME_OVF, Frame Error Overflow (If Selective Wake is equipped)

uint8_t TCAN4x5x_Device_Interrupts::GLOBALERR

DEV_IR[7] : GLOBALERR, Global Error. Is the OR output of all interrupts.

uint8_t TCAN4x5x_Device_Interrupts::LWU

DEV_IR[14] : LWU, Local Wake Up.

uint8_t TCAN4x5x_Device_Interrupts::M_CAN_INT

DEV_IR[1] M_CAN_INT: There are MCAN interrupts pending.

uint8_t TCAN4x5x_Device_Interrupts::PWRON

DEV_IR[20] : PWRON, Power On Interrupt.

uint8_t TCAN4x5x_Device_Interrupts::RESERVED

DEV_IR[9] : RESERVED.

uint8_t TCAN4x5x_Device_Interrupts::RESERVED2

DEV_IR[11] : RESERVED.

uint8_t TCAN4x5x_Device_Interrupts::RESERVED3

DEV_IR[17] : Reserved.

uint8_t TCAN4x5x_Device_Interrupts::SMS

DEV_IR[23] : SMS, Sleep Mode Status Flag. Set when sleep mode is entered due to WKERR, UVIO, or TSD faults.

uint8_t TCAN4x5x_Device_Interrupts::SPIERR

DEV_IR[3] : SPI Error.

uint8_t TCAN4x5x_Device_Interrupts::SWERR

DEV_IR[2] : Selective Wake Error (If equipped)

uint8_t TCAN4x5x_Device_Interrupts::TSD

DEV_IR[19] : TSD, Thermal Shut Down.

uint8_t TCAN4x5x_Device_Interrupts::UVIO

DEV_IR[21] : UVIO, Undervoltage on UVIO.

uint8_t TCAN4x5x_Device_Interrupts::UVSUP

DEV_IR[22] : UVSUP, Undervoltage on VSUP and VCCOUT.

uint8_t TCAN4x5x_Device_Interrupts::VTWD

DEV_IR[0] VTWD: Global Voltage, Temp, or Watchdog (if equipped) Interrupt.

uint8_t TCAN4x5x_Device_Interrupts::WDTO

DEV_IR[18] : WDTO, Watchdog Time Out.

uint8_t TCAN4x5x_Device_Interrupts::WKERR

DEV_IR[13] : WKERR, Wake Error.

uint8_t TCAN4x5x_Device_Interrupts::WKRQ

DEV_IR[6] : WKRQ, Wake Request.

uint32_t TCAN4x5x_Device_Interrupts::word

Full register as single 32-bit word.

The documentation for this struct was generated from the following file:

- C:/Alphi/PCIeMiniSoftware/include/**TCAN4x5x_Data_Structs.h**

TCAN4x5x_MCAN_CCCR_Config Struct Reference

struct containing the bit fields of the MCAN CCCR register
`#include <TCAN4x5x_Data_Structs.h>`

Public Attributes

- union {
- uint32_t **word**
  Full register as single 32-bit word.

- struct {
- uint8_t **reserved**: 2
  Reserved (0)

- uint8_t **ASM**: 1
  ASM: Restricted Operation Mode. The device can only listen to CAN traffic and acknowledge, but not send anything.

- uint8_t **reserved2**: 1
  Reserved (0)

- uint8_t **CSR**: 1
  CSR: Clock stop request.

- uint8_t **MON**: 1
  MON: Bus monitoring mode. The device may only listen to CAN traffic, and is not allowed to acknowledge or send error frames.

- uint8_t **DAR**: 1
  DAR: Disable automatic retransmission. If a transmission errors, gets a NACK, or loses arbitration, the MCAN controller will NOT try to transmit again.

- uint8_t **TEST**: 1
  TEST: MCAN Test mode enable.

- uint8_t **FDOE**: 1
  FDOE: Can FD mode enabled, master enable for CAN FD support.

- uint8_t **BRSE**: 1
  BRSE: Bit rate switch enabled for can FD. Master enable for bit rate switching support.

- uint8_t **reserved3**: 2
  Reserved (0)

- uint8_t **PXHD**: 1
  PXHD: Protocol exception handling disable

  0 = Protocol exception handling enabled [default]

1 = protocol exception handling disabled.

- uint8_t **EFBI**: 1
  EFBI: Edge filtering during bus integration. 0 Disables this [default].

- uint8_t **TXP**: 1
  TXP: Transmit Pause Enable: Pause for 2 can bit times before next transmission.

- uint8_t **NISO**: 1
  NSIO: Non Iso Operation
  0: CAN FD frame format according to ISO 11898-1:2015 [default]
  1: CAN FD frame format according to Bosch CAN FD Spec v1.

- }
- };

Detailed Description

struct containing the bit fields of the MCAN CCCR register

Member Data Documentation

union { ... }

uint8_t TCAN4x5x_MCAN_CCCR_Config::ASM

ASM: Restricted Operation Mode. The device can only listen to CAN traffic and acknowledge, but not send anything.

uint8_t TCAN4x5x_MCAN_CCCR_Config::BRSE

BRSE: Bit rate switch enabled for can FD. Master enable for bit rate switching support.

uint8_t TCAN4x5x_MCAN_CCCR_Config::CSR

CSR: Clock stop request.

uint8_t TCAN4x5x_MCAN_CCCR_Config::DAR

DAR: Disable automatic retransmission. If a transmission errors, gets a NACK, or loses arbitration, the MCAN controller will NOT try to transmit again.

uint8_t TCAN4x5x_MCAN_CCCR_Config::EFBI

EFBI: Edge filtering during bus integration. 0 Disables this [default].

uint8_t TCAN4x5x_MCAN_CCCR_Config::FDOE

FDOE: Can FD mode enabled, master enable for CAN FD support.

uint8_t TCAN4x5x_MCAN_CCCR_Config::MON

MON: Bus monitoring mode. The device may only listen to CAN traffic, and is not allowed to acknowledge or send error frames.

uint8_t TCAN4x5x_MCAN_CCCR_Config::NISO

NSIO: Non Iso Operation

0: CAN FD frame format according to ISO 11898-1:2015 [default]

1: CAN FD frame format according to Bosch CAN FD Spec v1.

uint8_t TCAN4x5x_MCAN_CCCR_Config::PXHD

PXHD: Protocol exception handling disable

0 = Protocol exception handling enabled [default]

1 = protocol exception handling disabled.

uint8_t TCAN4x5x_MCAN_CCCR_Config::reserved

Reserved (0)

uint8_t TCAN4x5x_MCAN_CCCR_Config::reserved2

Reserved (0)

uint8_t TCAN4x5x_MCAN_CCCR_Config::reserved3

Reserved (0)

uint8_t TCAN4x5x_MCAN_CCCR_Config::TEST

TEST: MCAN Test mode enable.

uint8_t TCAN4x5x_MCAN_CCCR_Config::TXP

TXP: Transmit Pause Enable: Pause for 2 can bit times before next transmission.

uint32_t TCAN4x5x_MCAN_CCCR_Config::word

Full register as single 32-bit word.

The documentation for this struct was generated from the following file:

- C:/Alphi/PCIeMiniSoftware/include/**TCAN4x5x_Data_Structs.h**

TCAN4x5x_MCAN_Data_Timing_Raw Struct Reference

Used to setup the timing parameters of the MCAN module This is the raw MCAN form of the struct which takes in the same values as the actual Bosch MCAN core.

```
#include <TCAN4x5x_Data_Structs.h>
```

Public Attributes

- uint8_t **DataBitRatePrescaler**: 5
  DBRP: The prescaler value from the MCAN system clock. Interpreted by MCAN as the value is this field + 1
  Valid range is: 0 to 31.

- uint8_t **DataTimeSeg1andProp**: 5
  DTSEG1: Data time segment 1 + prop segment value. Interpreted by MCAN as the value in this field + 1
  Valid values are: 0 to 31.

- uint8_t **DataTimeSeg2**: 4
  DTSEG2: Data time segment 2. Interpreted by MCAN as the value is this field + 1
  Valid values are: 0 to 15.

- uint8_t **DataSyncJumpWidth**: 4
  DSJW: Data Resynchronization jump width. Interpreted by MCAN as the value is this field + 1
  Valid values are: 0 to 15.

- uint8_t **TDCOffset**: 7
  TDCO: Transmitter delay compensation offset
  Valid values are 0 to 127 mtq.

- uint8_t **TDCFilter**: 7
  TDCFilter: Transmitter delay compensation Filter Window Length
  Valid values are 0 to 127 mtq.

Detailed Description

Used to setup the timing parameters of the MCAN module This is the raw MCAN form of the struct which takes in the same values as the actual Bosch MCAN core.

Member Data Documentation

uint8_t TCAN4x5x_MCAN_Data_Timing_Raw::DataBitRatePrescaler

DBRP: The prescaler value from the MCAN system clock. Interpreted by MCAN as the value is this field + 1

Valid range is: 0 to 31.

uint8_t TCAN4x5x_MCAN_Data_Timing_Raw::DataSyncJumpWidth

DSJW: Data Resynchronization jump width. Interpreted by MCAN as the value is this field + 1

Valid values are: 0 to 15.

uint8_t TCAN4x5x_MCAN_Data_Timing_Raw::DataTimeSeg1andProp

DTSEG1: Data time segment 1 + prop segment value. Interpreted by MCAN as the value in this field + 1

Valid values are: 0 to 31.

uint8_t TCAN4x5x_MCAN_Data_Timing_Raw::DataTimeSeg2

DTSEG2: Data time segment 2. Interpreted by MCAN as the value is this field + 1

Valid values are: 0 to 15.

uint8_t TCAN4x5x_MCAN_Data_Timing_Raw::TDCFilter

TDCFilter: Transmitter delay compensation Filter Window Length

Valid values are 0 to 127 mtq.

uint8_t TCAN4x5x_MCAN_Data_Timing_Raw::TDCOffset

TDCO: Transmitter delay compensation offset

Valid values are 0 to 127 mtq.

The documentation for this struct was generated from the following file:

- C:/Alphi/PCIeMiniSoftware/include/**TCAN4x5x_Data_Structs.h**

TCAN4x5x_MCAN_Data_Timing_Simple Struct Reference

Used to setup the data timing parameters of the MCAN module This is a simplified struct, requiring only the prescaler value (1:x), number of time quanta before and after the sample point.

```
#include <TCAN4x5x_Data_Structs.h>
```

Public Attributes

- uint8_t **DataBitRatePrescaler**: 6
  Prescaler value, interpreted as 1:x
  Valid range is: 1 to 32.

- uint8_t **DataTqBeforeSamplePoint**: 6
  DTQBSP: Number of time quanta before sample point
  Valid values are: 2 to 33.

- uint8_t **DataTqAfterSamplePoint**: 5
  DTQASP: Number of time quanta after sample point
  Valid values are: 1 to 16.

Detailed Description

Used to setup the data timing parameters of the MCAN module This is a simplified struct, requiring only the prescaler value (1:x), number of time quanta before and after the sample point.

Member Data Documentation

uint8_t TCAN4x5x_MCAN_Data_Timing_Simple::DataBitRatePrescaler

Prescaler value, interpreted as 1:x
Valid range is: 1 to 32.

uint8_t TCAN4x5x_MCAN_Data_Timing_Simple::DataTqAfterSamplePoint

DTQASP: Number of time quanta after sample point
Valid values are: 1 to 16.

uint8_t TCAN4x5x_MCAN_Data_Timing_Simple::DataTqBeforeSamplePoint

DTQBSP: Number of time quanta before sample point
Valid values are: 2 to 33.

The documentation for this struct was generated from the following file:

- C:/Alphi/PCIeMiniSoftware/include/**TCAN4x5x_Data_Structs.h**

TCAN4x5x_MCAN_Interrupt_Enable Struct Reference

Struct containing the MCAN interrupt enable bit field.
`#include <TCAN4x5x_Data_Structs.h>`

Public Attributes

- union {
- uint32_t **word**
  Full register as single 32-bit word.

- struct {
- uint8_t **RF0NE**: 1
  IE[0] RF0NE: Rx FIFO 0 new message.

- uint8_t **RF0WE**: 1
  IE[1] RF0WE: Rx FIFO 0 watermark reached.

- uint8_t **RF0FE**: 1
  IE[2] RF0FE: Rx FIFO 0 full.

- uint8_t **RF0LE**: 1
  IE[3] RF0LE: Rx FIFO 0 message lost.

- uint8_t **RF1NE**: 1
  IE[4] RF1NE: Rx FIFO 1 new message.

- uint8_t **RF1WE**: 1
  IE[5] RF1WE: RX FIFO 1 watermark reached.

- uint8_t **RF1FE**: 1
  IE[6] RF1FE: Rx FIFO 1 full.

- uint8_t **RF1LE**: 1
  IE[7] RF1LE: Rx FIFO 1 message lost.

- uint8_t **HPME**: 1
  IE[8] HPME: High priority message.

- uint8_t **TCE**: 1
  IE[9] TCE: Transmission completed.

- uint8_t **TCFE**: 1
  IE[10] TCFE: Transmission cancellation finished.

- uint8_t **TFEE**: 1
  IE[11] TFEE: Tx FIFO Empty.

- uint8_t **TEFNE**: 1
  IE[12] TEFNE: Tx Event FIFO new entry.

- uint8_t **TEFWE**: 1
  IE[13] TEFWE: Tx Event FIFO watermark reached.

- uint8_t **TEFFE**: 1
  IE[14] TEFFE: Tx Event FIFO full.

- uint8_t **TEFLE**: 1
  IE[15] TEFLE: Tx Event FIFO element lost.

- uint8_t **TSWE**: 1
  IE[16] TSWE: Timestamp wraparound.

- uint8_t **MRAFE**: 1
  IE[17] MRAFE: Message RAM access failure.

- uint8_t **TOOE**: 1
  IE[18] TOOE: Time out occured.

- uint8_t **DRXE**: 1
  IE[19] DRXE: Message stored to dedicated RX buffer.

- uint8_t **BECE**: 1
  IE[20] BECE: MRAM Bit error corrected.

- uint8_t **BEUE**: 1
  IE[21] BEUE: MRAM Bit error uncorrected.

- uint8_t **ELOE**: 1
  IE[22] ELOE: Error logging overflow.

- uint8_t **EPE**: 1
  IE[23] EPE: Error_passive status changed.

- uint8_t **EWE**: 1
  IE[24] EWE: Error_warning status changed.

- uint8_t **BOE**: 1
  IE[25] BOE: Bus_off status changed.

- uint8_t **WDIE**: 1
  IE[26] WDIE: MRAM Watchdog Interrupt.

- uint8_t **PEAE**: 1
  IE[27] PEAE Protocol Error in arbitration phase (nominal bit time used)

- uint8_t **PEDE**: 1
  IE[28] PEDE: Protocol error in data phase (data bit time is used)

- uint8_t **ARAE**: 1
  IE[29] ARAE: Access to reserved address.

- uint8_t **reserved**: 2
  IE[30:31] Reserved, not writable.

- }
- };

Detailed Description

Struct containing the MCAN interrupt enable bit field.

Member Data Documentation

union { ... }

uint8_t TCAN4x5x_MCAN_Interrupt_Enable::ARAE

IE[29] ARAE: Access to reserved address.

uint8_t TCAN4x5x_MCAN_Interrupt_Enable::BECE

IE[20] BECE: MRAM Bit error corrected.

uint8_t TCAN4x5x_MCAN_Interrupt_Enable::BEUE

IE[21] BEUE: MRAM Bit error uncorrected.

uint8_t TCAN4x5x_MCAN_Interrupt_Enable::BOE

IE[25] BOE: Bus_off status changed.

uint8_t TCAN4x5x_MCAN_Interrupt_Enable::DRXE

IE[19] DRXE: Message stored to dedicated RX buffer.

uint8_t TCAN4x5x_MCAN_Interrupt_Enable::ELOE

IE[22] ELOE: Error logging overflow.

uint8_t TCAN4x5x_MCAN_Interrupt_Enable::EPE

IE[23] EPE: Error_passive status changed.

uint8_t TCAN4x5x_MCAN_Interrupt_Enable::EWE

IE[24] EWE: Error_warning status changed.

uint8_t TCAN4x5x_MCAN_Interrupt_Enable::HPME

IE[8] HPME: High priority message.

uint8_t TCAN4x5x_MCAN_Interrupt_Enable::MRAFE

IE[17] MRAFE: Message RAM access failure.

uint8_t TCAN4x5x_MCAN_Interrupt_Enable::PEAE

IE[27] PEAE Protocol Error in arbitration phase (nominal bit time used)

uint8_t TCAN4x5x_MCAN_Interrupt_Enable::PEDE

IE[28] PEDE: Protocol error in data phase (data bit time is used)

uint8_t TCAN4x5x_MCAN_Interrupt_Enable::reserved

IE[30:31] Reserved, not writable.

uint8_t TCAN4x5x_MCAN_Interrupt_Enable::RF0FE

IE[2] RF0FE: Rx FIFO 0 full.

uint8_t TCAN4x5x_MCAN_Interrupt_Enable::RF0LE

IE[3] RF0LE: Rx FIFO 0 message lost.

uint8_t TCAN4x5x_MCAN_Interrupt_Enable::RF0NE

IE[0] RF0NE: Rx FIFO 0 new message.

uint8_t TCAN4x5x_MCAN_Interrupt_Enable::RF0WE

IE[1] RF0WE: Rx FIFO 0 watermark reached.

uint8_t TCAN4x5x_MCAN_Interrupt_Enable::RF1FE

IE[6] RF1FE: Rx FIFO 1 full.

uint8_t TCAN4x5x_MCAN_Interrupt_Enable::RF1LE

IE[7] RF1LE: Rx FIFO 1 message lost.

uint8_t TCAN4x5x_MCAN_Interrupt_Enable::RF1NE

IE[4] RF1NE: Rx FIFO 1 new message.

uint8_t TCAN4x5x_MCAN_Interrupt_Enable::RF1WE

IE[5] RF1WE: RX FIFO 1 watermark reached.

uint8_t TCAN4x5x_MCAN_Interrupt_Enable::TCE

IE[9] TCE: Transmission completed.

uint8_t TCAN4x5x_MCAN_Interrupt_Enable::TCFE

IE[10] TCFE: Transmission cancellation finished.

uint8_t TCAN4x5x_MCAN_Interrupt_Enable::TEFFE

IE[14] TEFFE: Tx Event FIFO full.

uint8_t TCAN4x5x_MCAN_Interrupt_Enable::TEFLE

IE[15] TEFLE: Tx Event FIFO element lost.

uint8_t TCAN4x5x_MCAN_Interrupt_Enable::TEFNE

IE[12] TEFNE: Tx Event FIFO new entry.

uint8_t TCAN4x5x_MCAN_Interrupt_Enable::TEFWE

IE[13] TEFWE: Tx Event FIFO watermark reached.

uint8_t TCAN4x5x_MCAN_Interrupt_Enable::TFEE

IE[11] TFEE: Tx FIFO Empty.

uint8_t TCAN4x5x_MCAN_Interrupt_Enable::TOOE

IE[18] TOOE: Time out occured.

uint8_t TCAN4x5x_MCAN_Interrupt_Enable::TSWE

IE[16] TSWE: Timestamp wraparound.

uint8_t TCAN4x5x_MCAN_Interrupt_Enable::WDIE

IE[26] WDIE: MRAM Watchdog Interrupt.

uint32_t TCAN4x5x_MCAN_Interrupt_Enable::word

Full register as single 32-bit word.

The documentation for this struct was generated from the following file:

- C:/Alphi/PCIeMiniSoftware/include/**TCAN4x5x_Data_Structs.h**

TCAN4x5x_MCAN_Interrupts Struct Reference

Struct containing the MCAN interrupt bit field.
`#include <TCAN4x5x_Data_Structs.h>`

Public Attributes

- union {
- uint32_t **word**
  Full register as single 32-bit word.

- struct {
- uint8_t **RF0N**: 1
  IR[0] RF0N: Rx FIFO 0 new message.

- uint8_t **RF0W**: 1
  IR[1] RF0W: Rx FIFO 0 watermark reached.

- uint8_t **RF0F**: 1
  IR[2] RF0F: Rx FIFO 0 full.

- uint8_t **RF0L**: 1
  IR[3] RF0L: Rx FIFO 0 message lost.

- uint8_t **RF1N**: 1
  IR[4] RF1N: Rx FIFO 1 new message.

- uint8_t **RF1W**: 1
  IR[5] RF1W: RX FIFO 1 watermark reached.

- uint8_t **RF1F**: 1
  IR[6] RF1F: Rx FIFO 1 full.

- uint8_t **RF1L**: 1
  IR[7] RF1L: Rx FIFO 1 message lost.

- uint8_t **HPM**: 1
  IR[8] HPM: High priority message.

- uint8_t **TC**: 1
  IR[9] TC: Transmission completed.

- uint8_t **TCF**: 1
  IR[10] TCF: Transmission cancellation finished.

- uint8_t **TFE**: 1
  IR[11] TFE: Tx FIFO Empty.

- uint8_t **TEFN**: 1
  IR[12] TEFN: Tx Event FIFO new entry.

- uint8_t **TEFW**: 1
  IR[13] TEFW: Tx Event FIFO water mark reached.

- uint8_t **TEFF**: 1
  IR[14] TEFF: Tx Event FIFO full.

- uint8_t **TEFL**: 1
  IR[15] TEFL: Tx Event FIFO element lost.

- uint8_t **TSW**: 1
  IR[16] TSW: Timestamp wrapped around.

- uint8_t **MRAF**: 1
  IR[17] MRAF: Message RAM access failure.

- uint8_t **TOO**: 1
  IR[18] TOO: Time out occurred.

- uint8_t **DRX**: 1
  IR[19] DRX: Message stored to dedicated RX buffer.

- uint8_t **BEC**: 1
  IR[20] BEC: MRAM Bit error corrected.

- uint8_t **BEU**: 1
  IR[21] BEU: MRAM Bit error uncorrected.

- uint8_t **ELO**: 1
  IR[22] ELO: Error logging overflow.

- uint8_t **EP**: 1
  IR[23] EP: Error_passive status changed.

- uint8_t **EW**: 1
  IR[24] EW: Error_warning status changed.

- uint8_t **BO**: 1
  IR[25] BO: Bus_off status changed.

- uint8_t **WDI**: 1
  IR[26] WDI: MRAM Watchdog Interrupt.

- uint8_t **PEA**: 1
  IR[27] PEA Protocol Error in arbitration phase (nominal bit time used)

- uint8_t **PED**: 1
  IR[28] PED: Protocol error in data phase (data bit time is used)

- uint8_t **ARA**: 1
  IR[29] ARA: Access to reserved address.

- uint8_t **reserved**: 2
  IR[30:31] Reserved, not writable.

- }
- };

Detailed Description

Struct containing the MCAN interrupt bit field.

Member Data Documentation

union { ... }

uint8_t TCAN4x5x_MCAN_Interrupts::ARA

IR[29] ARA: Access to reserved address.

uint8_t TCAN4x5x_MCAN_Interrupts::BEC

IR[20] BEC: MRAM Bit error corrected.

uint8_t TCAN4x5x_MCAN_Interrupts::BEU

IR[21] BEU: MRAM Bit error uncorrected.

uint8_t TCAN4x5x_MCAN_Interrupts::BO

IR[25] BO: Bus_off status changed.

uint8_t TCAN4x5x_MCAN_Interrupts::DRX

IR[19] DRX: Message stored to dedicated RX buffer.

uint8_t TCAN4x5x_MCAN_Interrupts::ELO

IR[22] ELO: Error logging overflow.

uint8_t TCAN4x5x_MCAN_Interrupts::EP

IR[23] EP: Error_passive status changed.

uint8_t TCAN4x5x_MCAN_Interrupts::EW

IR[24] EW: Error_warning status changed.

uint8_t TCAN4x5x_MCAN_Interrupts::HPM

IR[8] HPM: High priority message.

uint8_t TCAN4x5x_MCAN_Interrupts::MRAF

IR[17] MRAF: Message RAM access failure.

uint8_t TCAN4x5x_MCAN_Interrupts::PEA

IR[27] PEA Protocol Error in arbitration phase (nominal bit time used)

uint8_t TCAN4x5x_MCAN_Interrupts::PED

IR[28] PED: Protocol error in data phase (data bit time is used)

uint8_t TCAN4x5x_MCAN_Interrupts::reserved

IR[30:31] Reserved, not writable.

uint8_t TCAN4x5x_MCAN_Interrupts::RF0F

IR[2] RF0F: Rx FIFO 0 full.

uint8_t TCAN4x5x_MCAN_Interrupts::RF0L

IR[3] RF0L: Rx FIFO 0 message lost.

uint8_t TCAN4x5x_MCAN_Interrupts::RF0N

IR[0] RF0N: Rx FIFO 0 new message.

uint8_t TCAN4x5x_MCAN_Interrupts::RF0W

IR[1] RF0W: Rx FIFO 0 watermark reached.

uint8_t TCAN4x5x_MCAN_Interrupts::RF1F

IR[6] RF1F: Rx FIFO 1 full.

uint8_t TCAN4x5x_MCAN_Interrupts::RF1L

IR[7] RF1L: Rx FIFO 1 message lost.

uint8_t TCAN4x5x_MCAN_Interrupts::RF1N

IR[4] RF1N: Rx FIFO 1 new message.

uint8_t TCAN4x5x_MCAN_Interrupts::RF1W

IR[5] RF1W: RX FIFO 1 watermark reached.

uint8_t TCAN4x5x_MCAN_Interrupts::TC

IR[9] TC: Transmission completed.

uint8_t TCAN4x5x_MCAN_Interrupts::TCF

IR[10] TCF: Transmission cancellation finished.

uint8_t TCAN4x5x_MCAN_Interrupts::TEFF

IR[14] TEFF: Tx Event FIFO full.

uint8_t TCAN4x5x_MCAN_Interrupts::TEFL

IR[15] TEFL: Tx Event FIFO element lost.

uint8_t TCAN4x5x_MCAN_Interrupts::TEFN

IR[12] TEFN: Tx Event FIFO new entry.

uint8_t TCAN4x5x_MCAN_Interrupts::TEFW

IR[13] TEFW: Tx Event FIFO water mark reached.

uint8_t TCAN4x5x_MCAN_Interrupts::TFE

IR[11] TFE: Tx FIFO Empty.

uint8_t TCAN4x5x_MCAN_Interrupts::TOO

IR[18] TOO: Time out occurred.

uint8_t TCAN4x5x_MCAN_Interrupts::TSW

IR[16] TSW: Timestamp wrapped around.

uint8_t TCAN4x5x_MCAN_Interrupts::WDI

IR[26] WDI: MRAM Watchdog Interrupt.

uint32_t TCAN4x5x_MCAN_Interrupts::word

Full register as single 32-bit word.

The documentation for this struct was generated from the following file:

- C:/Alphi/PCIeMiniSoftware/include/**TCAN4x5x_Data_Structs.h**

TCAN4x5x_MCAN_Nominal_Timing_Raw Struct Reference

Used to setup the nominal timing parameters of the MCAN module This is the raw MCAN form of the struct which takes in the same values as the actual Bosch MCAN core.

```
#include <TCAN4x5x_Data_Structs.h>
```

Public Attributes

- uint16_t **NominalBitRatePrescaler**: 9
  NBRP: The prescaler value from the MCAN system clock. Interpreted by MCAN as the value is this field + 1

  Valid range is: 0 to 511.

- uint8_t **NominalTimeSeg1andProp**: 8
  NTSEG1: Data time segment 1 + prop segment value. Interpreted by MCAN as the value is this field + 1

  Valid values are: 0 to 255.

- uint8_t **NominalTimeSeg2**: 7
  NTSEG2: Data time segment 2. Interpreted by MCAN as the value is this field + 1

  Valid values are: 0 to 127.

- uint8_t **NominalSyncJumpWidth**: 7
  NSJW: Nominal time Resynchronization jump width. Interpreted by MCAN as the value is this field + 1

  Valid values are: 0 to 127.

Detailed Description

Used to setup the nominal timing parameters of the MCAN module This is the raw MCAN form of the struct which takes in the same values as the actual Bosch MCAN core.

Member Data Documentation

uint16_t TCAN4x5x_MCAN_Nominal_Timing_Raw::NominalBitRatePrescaler

NBRP: The prescaler value from the MCAN system clock. Interpreted by MCAN as the value is this field + 1

Valid range is: 0 to 511.

uint8_t TCAN4x5x_MCAN_Nominal_Timing_Raw::NominalSyncJumpWidth

NSJW: Nominal time Resynchronization jump width. Interpreted by MCAN as the value is this field + 1

Valid values are: 0 to 127.

uint8_t TCAN4x5x_MCAN_Nominal_Timing_Raw::NominalTimeSeg1andProp

NTSEG1: Data time segment 1 + prop segment value. Interpreted by MCAN as the value is this field + 1

Valid values are: 0 to 255.

uint8_t TCAN4x5x_MCAN_Nominal_Timing_Raw::NominalTimeSeg2

NTSEG2: Data time segment 2. Interpreted by MCAN as the value is this field + 1

Valid values are: 0 to 127.

The documentation for this struct was generated from the following file:

- C:/Alphi/PCIeMiniSoftware/include/**TCAN4x5x_Data_Structs.h**

TCAN4x5x_MCAN_Nominal_Timing_Simple Struct Reference

Used to setup the nominal timing parameters of the MCAN module This is a simplified struct, requiring only the prescaler value (1:x), number of time quanta before and after the sample point.

`#include <TCAN4x5x_Data_Structs.h>`

Public Attributes

- uint16_t **NominalBitRatePrescaler**: 10
  NBRP: The prescaler value from the MCAN system clock. Value interpreted as 1:x
  Valid range is: 1 to 512.

- uint16_t **NominalTqBeforeSamplePoint**: 9
  NTQBSP: The total number of time quanta prior to sample point
  Valid values are: 2 to 257.

- uint8_t **NominalTqAfterSamplePoint**: 8
  NTQASP: The total number of time quanta after the sample point
  Valid values are: 2 to 128.

Detailed Description

Used to setup the nominal timing parameters of the MCAN module This is a simplified struct, requiring only the prescaler value (1:x), number of time quanta before and after the sample point.

Member Data Documentation

uint16_t TCAN4x5x_MCAN_Nominal_Timing_Simple::NominalBitRatePrescaler

NBRP: The prescaler value from the MCAN system clock. Value interpreted as 1:x
Valid range is: 1 to 512.

uint8_t TCAN4x5x_MCAN_Nominal_Timing_Simple::NominalTqAfterSamplePoint

NTQASP: The total number of time quanta after the sample point
Valid values are: 2 to 128.

uint16_t TCAN4x5x_MCAN_Nominal_Timing_Simple::NominalTqBeforeSamplePoint

NTQBSP: The total number of time quanta prior to sample point
Valid values are: 2 to 257.

The documentation for this struct was generated from the following file:

- C:/Alphi/PCIeMiniSoftware/include/**TCAN4x5x_Data_Structs.h**

TCAN4x5x_MCAN_RX_Header Struct Reference

CAN message header.
`#include <TCAN4x5x_Data_Structs.h>`

Public Attributes

- uint32_t **ID**: 29
  CAN ID received.

- uint8_t **RTR**: 1
  Remote Transmission Request flag.

- uint8_t **XTD**: 1
  Extended Identifier flag.

- uint8_t **ESI**: 1
  Error state indicator flag.

- uint16_t **RXTS**: 16
  Receive time stamp.

- uint8_t **DLCode**: 4
  Data length code.

- uint8_t **BRS**: 1
  Bit rate switch used flag.

- uint8_t **FDF**: 1
  CAN FD Format flag.

- uint8_t **reserved**: 2
  Reserved (0)

- uint8_t **FIDX**: 7
  Filter index that this message matched.

- uint8_t **ANMF**: 1
  Accepted non matching frame flag.

Detailed Description

CAN message header.

Member Data Documentation

uint8_t TCAN4x5x_MCAN_RX_Header::ANMF

Accepted non matching frame flag.

uint8_t TCAN4x5x_MCAN_RX_Header::BRS

Bit rate switch used flag.

uint8_t TCAN4x5x_MCAN_RX_Header::DLCode

Data length code.

uint8_t TCAN4x5x_MCAN_RX_Header::ESI

Error state indicator flag.

uint8_t TCAN4x5x_MCAN_RX_Header::FDF

CAN FD Format flag.

uint8_t TCAN4x5x_MCAN_RX_Header::FIDX

Filter index that this message matched.

uint32_t TCAN4x5x_MCAN_RX_Header::ID

CAN ID received.

uint8_t TCAN4x5x_MCAN_RX_Header::reserved

Reserved (0)

uint8_t TCAN4x5x_MCAN_RX_Header::RTR

Remote Transmission Request flag.

uint16_t TCAN4x5x_MCAN_RX_Header::RXTS

Receive time stamp.

uint8_t TCAN4x5x_MCAN_RX_Header::XTD

Extended Identifier flag.

The documentation for this struct was generated from the following file:

- C:/Alphi/PCIeMiniSoftware/include/**TCAN4x5x_Data_Structs.h**

TCAN4x5x_MCAN_SID_Filter Struct Reference

Standard ID filter struct.
`#include <TCAN4x5x_Data_Structs.h>`

Public Attributes

- union {
- uint32_t **word**
  full register as single 32-bit word

- struct {
- uint16_t **SFID2**: 11
  SFID2[10:0].

- uint8_t **reserved**: 5
  Reserved.

- uint16_t **SFID1**: 11
  SFID1[10:0].

- **TCAN4x5x_SID_SFEC_Values SFEC**: 3
  SFEC[2:0] Standard filter element configuration.

- **TCAN4x5x_SID_SFT_Values SFT**: 2
  SFT Standard Filter Type.

- }
- };

Detailed Description

Standard ID filter struct.

Member Data Documentation

union { ... }

uint8_t TCAN4x5x_MCAN_SID_Filter::reserved

Reserved.

TCAN4x5x_SID_SFEC_Values TCAN4x5x_MCAN_SID_Filter::SFEC

SFEC[2:0] Standard filter element configuration.

uint16_t TCAN4x5x_MCAN_SID_Filter::SFID1

SFID1[10:0].

uint16_t TCAN4x5x_MCAN_SID_Filter::SFID2

SFID2[10:0].

TCAN4x5x_SID_SFT_Values TCAN4x5x_MCAN_SID_Filter::SFT

SFT Standard Filter Type.

uint32_t TCAN4x5x_MCAN_SID_Filter::word

full register as single 32-bit word

The documentation for this struct was generated from the following file:

- C:/Alphi/PCIeMiniSoftware/include/**TCAN4x5x_Data_Structs.h**

TCAN4x5x_MCAN_TX_Header Struct Reference

CAN message header for transmitted messages.
`#include <TCAN4x5x_Data_Structs.h>`

Public Attributes

- uint32_t **ID**: 29
  CAN ID to send.

- uint8_t **RTR**: 1
  Remote Transmission Request flag.

- uint8_t **XTD**: 1
  Extended Identifier flag.

- uint8_t **ESI**: 1
  Error state indicator flag.

- uint8_t **DLCode**: 4
  Data length code.

- uint8_t **BRS**: 1
  Bit rate switch used flag.

- uint8_t **FDF**: 1
  CAN FD Format flag.

- uint8_t **reserved**: 1
  Reserved.

- uint8_t **EFC**: 1
  Event FIFO Control flag, to store tx events or not.

- uint8_t **MM**: 8
  Message Marker, used if `EFC` is set to 1.

Detailed Description

CAN message header for transmitted messages.

Member Data Documentation

uint8_t TCAN4x5x_MCAN_TX_Header::BRS

Bit rate switch used flag.

uint8_t TCAN4x5x_MCAN_TX_Header::DLCode

Data length code.

uint8_t TCAN4x5x_MCAN_TX_Header::EFC

Event FIFO Control flag, to store tx events or not.

uint8_t TCAN4x5x_MCAN_TX_Header::ESI

Error state indicator flag.

uint8_t TCAN4x5x_MCAN_TX_Header::FDF

CAN FD Format flag.

uint32_t TCAN4x5x_MCAN_TX_Header::ID

CAN ID to send.

uint8_t TCAN4x5x_MCAN_TX_Header::MM

Message Marker, used if `EFC` is set to 1.

uint8_t TCAN4x5x_MCAN_TX_Header::reserved

Reserved.

uint8_t TCAN4x5x_MCAN_TX_Header::RTR

Remote Transmission Request flag.

uint8_t TCAN4x5x_MCAN_TX_Header::XTD

Extended Identifier flag.

The documentation for this struct was generated from the following file:

- C:/Alphi/PCIeMiniSoftware/include/**TCAN4x5x_Data_Structs.h**

TCAN4x5x_MCAN_XID_Filter Struct Reference

Extended ID filter struct.
`#include <TCAN4x5x_Data_Structs.h>`

Public Attributes

- uint32_t **EFID2**: 29
  EFID2[28:0].

- uint8_t **reserved**: 1
  Reserved.

- **TCAN4x5x_XID_EFT_Values EFT**: 2
  EFT[1:0].

- uint32_t **EFID1**: 29
  EFID1[28:0].

- **TCAN4x5x_XID_EFEC_Values EFEC**: 3
  SFT Standard Filter Type.

Detailed Description

Extended ID filter struct.

Member Data Documentation

TCAN4x5x_XID_EFEC_Values TCAN4x5x_MCAN_XID_Filter::EFEC

SFT Standard Filter Type.

uint32_t TCAN4x5x_MCAN_XID_Filter::EFID1

EFID1[28:0].

uint32_t TCAN4x5x_MCAN_XID_Filter::EFID2

EFID2[28:0].

TCAN4x5x_XID_EFT_Values TCAN4x5x_MCAN_XID_Filter::EFT

EFT[1:0].

uint8_t TCAN4x5x_MCAN_XID_Filter::reserved

Reserved.

The documentation for this struct was generated from the following file:

- C:/Alphi/PCIeMiniSoftware/include/**TCAN4x5x_Data_Structs.h**

TCAN4x5x_MRAM_Config Struct Reference

Defines the number of MRAM elements and the size of the elements.
`#include <TCAN4x5x_Data_Structs.h>`

Public Attributes

- uint8_t **SIDNumElements**: 8
  Standard ID Number of Filter Elements: The number of 11-bit filters the user would like
  Valid range is: 0 to 128.

- uint8_t **XIDNumElements**: 7
  Extended ID Number of Filter Elements: The number of 29-bit filters the user would like
  Valid range is: 0 to 64.

- uint8_t **Rx0NumElements**: 7
  RX FIFO 0 number of elements: The number of elements for the RX FIFO 0
  Valid range is: 0 to 64.

- **TCAN4x5x_MRAM_Element_Data_Size Rx0ElementSize**: 3
  RX FIFO 0 element size: The number of bytes for the RX 0 FIFO (data payload)

- uint8_t **Rx1NumElements**: 7
  RX FIFO 1 number of elements: The number of elements for the RX FIFO 1
  Valid range is: 0 to 64.

- **TCAN4x5x_MRAM_Element_Data_Size Rx1ElementSize**: 3
  RX FIFO 1 element size: The number of bytes for the RX 1 FIFO (data payload)

- uint8_t **RxBufNumElements**: 7
  RX Buffers number of elements: The number of elements for the RX Buffers (Not the FIFO)
  Valid range is: 0 to 64.

- **TCAN4x5x_MRAM_Element_Data_Size RxBufElementSize**: 3
  RX Buffers element size: The number of bytes for the RX Buffers (data payload), not the FIFO.

- uint8_t **TxEventFIFONumElements**: 6
  TX Event FIFO number of elements: The number of elements for the TX Event FIFO
  Valid range is: 0 to 32.

- uint8_t **TxBufferNumElements**: 6
  TX Buffers number of elements: The number of elements for the TX Buffers
  Valid range is: 0 to 32.

- **TCAN4x5x_MRAM_Element_Data_Size TxBufferElementSize**: 3
  TX Buffers element size: The number of bytes for the TX Buffers (data payload)

Detailed Description

Defines the number of MRAM elements and the size of the elements.

Member Data Documentation

TCAN4x5x_MRAM_Element_Data_Size TCAN4x5x_MRAM_Config::Rx0ElementSize

RX FIFO 0 element size: The number of bytes for the RX 0 FIFO (data payload)

uint8_t TCAN4x5x_MRAM_Config::Rx0NumElements

RX FIFO 0 number of elements: The number of elements for the RX FIFO 0
Valid range is: 0 to 64.

TCAN4x5x_MRAM_Element_Data_Size TCAN4x5x_MRAM_Config::Rx1ElementSize

RX FIFO 1 element size: The number of bytes for the RX 1 FIFO (data payload)

uint8_t TCAN4x5x_MRAM_Config::Rx1NumElements

RX FIFO 1 number of elements: The number of elements for the RX FIFO 1
Valid range is: 0 to 64.

TCAN4x5x_MRAM_Element_Data_Size TCAN4x5x_MRAM_Config::RxBufElementSize

RX Buffers element size: The number of bytes for the RX Buffers (data payload), not the FIFO.

uint8_t TCAN4x5x_MRAM_Config::RxBufNumElements

RX Buffers number of elements: The number of elements for the RX Buffers (Not the FIFO)
Valid range is: 0 to 64.

uint8_t TCAN4x5x_MRAM_Config::SIDNumElements

Standard ID Number of Filter Elements: The number of 11-bit filters the user would like
Valid range is: 0 to 128.

TCAN4x5x_MRAM_Element_Data_Size
TCAN4x5x_MRAM_Config::TxBufferElementSize

TX Buffers element size: The number of bytes for the TX Buffers (data payload)

uint8_t TCAN4x5x_MRAM_Config::TxBufferNumElements

TX Buffers number of elements: The number of elements for the TX Buffers
Valid range is: 0 to 32.

uint8_t TCAN4x5x_MRAM_Config::TxEventFIFONumElements

TX Event FIFO number of elements: The number of elements for the TX Event FIFO
Valid range is: 0 to 32.

uint8_t TCAN4x5x_MRAM_Config::XIDNumElements

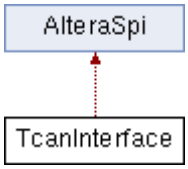
Extended ID Number of Filter Elements: The number of 29-bit filters the user would like
Valid range is: 0 to 64.

The documentation for this struct was generated from the following file:

- C:/Alphi/PCIeMiniSoftware/include/**TCAN4x5x_Data_Structs.h**

TcanInterface Class Reference

This class implements the **TCAN4550** SPI interface.
`#include <TCAN4550.h>`
Inheritance diagram for TcanInterface:



Public Member Functions

- **TcanInterface** (volatile void *spiAddr, AlteraPio *rst, uint8_t nbr)
  Constructor.

- void **reset** ()
  *reset the **TCAN4550** chip*

- uint32_t **getStatus** ()
  Get the SPI interface status.

- volatile void * **getAddress** ()
  Get the address of the SPI controller.

- void **AHB_WRITE_32** (uint16_t address, uint32_t data)
- void **AHB_WRITE_BURST_START** (uint16_t address, uint8_t words)
- void **AHB_WRITE_BURST_WRITE** (uint32_t data)
- void **AHB_WRITE_BURST_END** (void)
- uint32_t **AHB_READ_32** (uint16_t address)
- void **AHB_READ_BURST_START** (uint16_t address, uint8_t words)
- uint32_t **AHB_READ_BURST_READ** (void)
- void **AHB_READ_BURST_END** (void)

Public Attributes

- uint8_t **slave**
  ***TCAN4550** chip select index.*

- AlteraPio * **rstPio**

Detailed Description

This class implements the **TCAN4550** SPI interface.

Constructor & Destructor Documentation

TcanInterface::TcanInterface (volatile void * *spiAddr*, AlteraPio * *rst*, uint8_t *nbr*)`[inline]`

Constructor.

Parameters

spiAddr	Address of the SPI controller
rst	Address of the PIO controlling the reset line
nbr	Chip select line number.

Member Function Documentation

uint32_t TcanInterface::AHB_READ_32 (uint16_t *address*)

void TcanInterface::AHB_READ_BURST_END (void)

uint32_t TcanInterface::AHB_READ_BURST_READ (void)

void TcanInterface::AHB_READ_BURST_START (uint16_t *address*, uint8_t *words*)

void TcanInterface::AHB_WRITE_32 (uint16_t *address*, uint32_t *data*)

void TcanInterface::AHB_WRITE_BURST_END (void)

void TcanInterface::AHB_WRITE_BURST_START (uint16_t *address*, uint8_t *words*)

void TcanInterface::AHB_WRITE_BURST_WRITE (uint32_t *data*)

volatile void* TcanInterface::getAddress () `[inline]`

Get the address of the SPI controller.

Return values

Address	in user space.

uint32_t TcanInterface::getStatus () `[inline]`

Get the SPI interface status.

The bits are defined by the **AlteraSpi** class.

Return values

Status	register content.

void TcanInterface::reset () `[inline]`

reset the **TCAN4550** chip

Member Data Documentation

AlteraPio* TcanInterface::rstPio

uint8_t TcanInterface::slave

TCAN4550 chip select index.

The documentation for this class was generated from the following files:

- C:/Alphi/PCIeMiniSoftware/include/**TCAN4550.h**
- **TCAN4x5x_SPI.cpp**

TransferDesc Class Reference

Structure containing the details of a DMA transaction.
`#include <AlteraDma.h>`

Public Attributes

- volatile uint32_t **dest_offset**
  32-bit FPGA Avalon bus address of destination

- volatile uint32_t **src_offset**
  32-bit FPGA Avalon bus address of source

- uint32_t **tfr_length**
  length of the transfer

- uint32_t **flags**
- uint32_t **txs_offset**
  Offset in the mapping area.

- uint32_t **bufLength**
  Size of the buffer in bytes.

- uint32_t * **userSpaceBuffer**
  PC buffer address as an user-space address.

- bool **fPolling**
  Polling or interrupt for end of transfer (not yet implemented)

Detailed Description

Structure containing the details of a DMA transaction.

Member Data Documentation

uint32_t TransferDesc::bufLength

Size of the buffer in bytes.

volatile uint32_t TransferDesc::dest_offset

32-bit FPGA Avalon bus address of destination

uint32_t TransferDesc::flags

bool TransferDesc::fPolling

Polling or interrupt for end of transfer (not yet implemented)

volatile uint32_t TransferDesc::src_offset

32-bit FPGA Avalon bus address of source

uint32_t TransferDesc::tfr_length

length of the transfer

uint32_t TransferDesc::txs_offset

Offset in the mapping area.

uint32_t* TransferDesc::userSpaceBuffer

PC buffer address as an user-space address.

The documentation for this class was generated from the following file:

- C:/Alphi/PCIeMiniSoftware/include/**AlteraDma.h**

File Documentation

C:/Alphi/PCIeMiniSoftware/include/AlphiBoard.h File Reference

Base PCIe board class with Jungo driver and Altera PCIe hardware.

```
#include <stdint.h>
#include <stdio.h>
#include <Windows.h>
#include "AlphiDll.h"
#include <wdc_defs.h>
#include "PcieCra.h"
#include "AlteraDma.h"
```

Classes

- struct **MINIPCIE_DEV_CTX**
  Minipcie Device Information Structure.
- struct **LinearAddress**
  Memory Segment Descriptor.
- struct **MINIPCIE_INT_RESULT**
  Interrupt result information structure.
- class **BoardVersion**
  Board Hardware identification and version.
- class **AlphiBoard**
  Base class implementing a PCIe board and the Jungo driver.

Macros

- #define **ErrLog** printf
- #define **TraceLog** printf
- #define **CLOCK_REALTIME** 0

Typedefs

- typedef void(* **MINIPCIE_INT_HANDLER**) (void *pIntData)
  minipcie_arinc429 diagnostics interrupt handler function type

- typedef void(* **MINIPCIE_EVENT_HANDLER**) (WDC_DEVICE_HANDLE hDev, DWORD dwAction)
  minipcie_arinc429 diagnostics plug-and-play and power management events handler function type

- typedef struct **MINIPCIE_DEV_CTX** * **PMINIPCIE_DEV_CTX**
- typedef struct **LinearAddress LinearAddress**
  Memory Segment Descriptor.

Functions

- static int **clock_gettime** (int, struct timespec *spec)
  get system time with a nanosecond definition

- static void **usleep** (__int64 usec)
  Sleep for a number of microseconds.

- static void **nanosleep** (struct timespec *t, void *na)

Detailed Description

Base PCIe board class with Jungo driver and Altera PCIe hardware.

Macro Definition Documentation

#define CLOCK_REALTIME 0

#define ErrLog printf

#define TraceLog printf

Typedef Documentation

typedef struct LinearAddress LinearAddress

Memory Segment Descriptor.

typedef void(* MINIPCIE_EVENT_HANDLER) (WDC_DEVICE_HANDLE hDev, DWORD dwAction)

minipcie_arinc429 diagnostics plug-and-play and power management events handler function type

typedef void(* MINIPCIE_INT_HANDLER) (void *pIntData)

minipcie_arinc429 diagnostics interrupt handler function type

typedef struct MINIPCIE_DEV_CTX * PMINIPCIE_DEV_CTX

Function Documentation

static int clock_gettime (int , struct timespec * *spec*) `[inline]`, `[static]`

get system time with a nanosecond definition

static void nanosleep (struct timespec * *t*, void * *na*) `[inline]`, `[static]`

static void usleep (__int64 *usec*) `[inline]`, `[static]`

Sleep for a number of microseconds.

Parameters

usec	Number of microseconds to sleep

C:/Alphi/PCIeMiniSoftware/include/AlphiDll.h File Reference

Utility DLL definitions.
`#include "time.h"`

Macros

- #define **LINUX**
- #define **UNIX**
- #define **FALSE** 0
- #define **TRUE** 1
- #define **ALPHI_S_OK** 0
- #define **Dll** __declspec(dllimport)

Typedefs

- typedef int **HRESULT**

Detailed Description

Utility DLL definitions.

Macro Definition Documentation

#define ALPHI_S_OK 0

#define Dll __declspec(dllimport)

#define FALSE 0

#define LINUX

#define TRUE 1

#define UNIX

Typedef Documentation

typedef int HRESULT

C:/Alphi/PCIeMiniSoftware/include/AlphiErrorCodes.h File Reference

Description of the Error Codes used by the libraries.

```
#include "AlphiDll.h"
```

Macros

- #define **ERRCODE_NO_ERROR** 0
- #define **ERRCODE_SUCCESS** 0
- #define **ERRCODE_INTERNAL_ERROR** 1
- #define **ERRCODE_INVALID_BOARD_NUM** **ERRCODE_INTERNAL_ERROR** + 1
- #define **ERRCODE_BOARD_NOT_PRESENT** **ERRCODE_INTERNAL_ERROR** + 1
- #define **ERRCODE_INVALID_HANDLE** **ERRCODE_INVALID_BOARD_NUM** + 1
- #define **ERRCODE_INVALID_CHANNEL_NUM** **ERRCODE_INVALID_HANDLE** + 1
- #define **ERRCODE_INVALID_SELF_TEST_ENABLE_VAL** **ERRCODE_INVALID_CHANNEL_NUM** + 1
- #define **ERRCODE_INVALID_VALUE** **ERRCODE_INVALID_SELF_TEST_ENABLE_VAL** + 1
- #define **ERRCODE_INPUT_MODE** **ERRCODE_INVALID_VALUE** + 1
- #define **ERRCODE_OUTPUT_MODE** **ERRCODE_INPUT_MODE** + 1
- #define **ERRCODE_INVALID_LOGIC_SEL** **ERRCODE_OUTPUT_MODE** + 1
- #define **ERRCODE_INVALID_STROBE_MODE** **ERRCODE_INVALID_LOGIC_SEL** + 1
- #define **ERRCODE_INVALID_GROUP** **ERRCODE_INVALID_STROBE_MODE** + 1
- #define **ERRCODE_INVALID_FREQUENCY** **ERRCODE_INVALID_GROUP** + 1
- #define **ERRCODE_INVALID_INPUT_MODE** **ERRCODE_INVALID_FREQUENCY** + 1
- #define **ERRCODE_INVALID_MASK_VALUE** **ERRCODE_INVALID_INPUT_MODE** + 1
- #define **ERRCODE_INVALID_MODE** **ERRCODE_INVALID_MASK_VALUE** + 1
- #define **ERRCODE_INVALID_SELF_TEST_DATA** **ERRCODE_INVALID_MODE** + 1
- #define **ERRCODE_SELF_TEST_DISABLE** **ERRCODE_INVALID_SELF_TEST_DATA** + 1
- #define **ERRCODE_FAILED_SELF_TEST** **ERRCODE_SELF_TEST_DISABLE** + 1
- #define **ERRCODE_INVALID_TIME_BOUNCE_VAL** **ERRCODE_FAILED_SELF_TEST** + 1
- #define **ERRCODE_INT_ALREADY_ENABLED** **ERRCODE_INVALID_TIME_BOUNCE_VAL** + 1
- #define **ERRCODE_INT_NOT_ENABLED** **ERRCODE_INT_ALREADY_ENABLED** + 1
- #define **ERRCODE_INVALID_TRANRECVSTS** **ERRCODE_INT_NOT_ENABLED** + 1
- #define **ERRCODE_INVALID_TRANSNUMBER** **ERRCODE_INVALID_TRANRECVSTS** + 1
- #define **ERRCODE_INVALID_RECVNUMBER** **ERRCODE_INVALID_TRANSNUMBER** + 1
- #define **ERRCODE_INVALID_RECVSTATUS** **ERRCODE_INVALID_RECVNUMBER**+1
- #define **ERRCODE_INVALID_TRPAIR** **ERRCODE_INVALID_RECVSTATUS** + 1
- #define **ERRCODE_INVALID_TRANSSTATUS** **ERRCODE_INVALID_TRPAIR** + 1
- #define **ERRCODE_INVALID_LABELNUMBER** **ERRCODE_INVALID_TRANSSTATUS** + 1
- #define **ERRCODE_INVALID_SDI** **ERRCODE_INVALID_LABELNUMBER** + 1
- #define **ERRCODE_INVALID_PARITY** **ERRCODE_INVALID_SDI** + 1
- #define **ERRCODE_INVALID_DATARATE** **ERRCODE_INVALID_PARITY** + 1
- #define **ERRCODE_INVALID_DATALENGTH** **ERRCODE_INVALID_DATARATE** + 1
- #define **ERRCODE_INVALID_SSM** **ERRCODE_INVALID_DATALENGTH** + 1
- #define **ERRCODE_INVALID_EMTINTSTS** **ERRCODE_INVALID_SSM** + 1

- #define **ERRCODE_INVALID_HFINTSTS** **ERRCODE_INVALID_EMTINTSTS** + 1
- #define **ERRCODE_INVALID_FINTSTS** **ERRCODE_INVALID_HFINTSTS** + 1
- #define **ERRCODE_INVALID_COMMAND** **ERRCODE_INVALID_FINTSTS** + 1
- #define **ERRCODE_RX_UNDERFLOW** **ERRCODE_INVALID_COMMAND** + 1
- #define **ERRCODE_TX_OVERFLOW** **ERRCODE_RX_UNDERFLOW** + 1
- #define **ERRCODE_BUSY** **ERRCODE_TX_OVERFLOW** + 1
- #define **ERRCODE_TIMEOUT** **ERRCODE_BUSY** + 1
- #define **ERRCODE_INVALID_ALIGNMENT** **ERRCODE_TIMEOUT** + 1

Typedefs

- typedef int **PCIeMini_status**

Functions

- DLL char * **getAlphiErrorMsg** (**PCIeMini_status** errCode)
  Gives the string description of an error code.

Detailed Description

Description of the Error Codes used by the libraries.

Macro Definition Documentation

#define ERRCODE_BOARD_NOT_PRESENT ERRCODE_INTERNAL_ERROR + 1

#define ERRCODE_BUSY ERRCODE_TX_OVERFLOW + 1

#define ERRCODE_FAILED_SELF_TEST ERRCODE_SELF_TEST_DISABLE + 1

#define ERRCODE_INPUT_MODE ERRCODE_INVALID_VALUE + 1

#define ERRCODE_INT_ALREADY_ENABLED ERRCODE_INVALID_TIME_BOUNCE_VAL + 1

#define ERRCODE_INT_NOT_ENABLED ERRCODE_INT_ALREADY_ENABLED + 1

#define ERRCODE_INTERNAL_ERROR 1

#define ERRCODE_INVALID_ALIGNMENT ERRCODE_TIMEOUT + 1

#define ERRCODE_INVALID_BOARD_NUM ERRCODE_INTERNAL_ERROR + 1

#define ERRCODE_INVALID_CHANNEL_NUM ERRCODE_INVALID_HANDLE + 1

#define ERRCODE_INVALID_COMMAND ERRCODE_INVALID_FINTSTS + 1

#define ERRCODE_INVALID_DATALENGTH ERRCODE_INVALID_DATARATE + 1

#define ERRCODE_INVALID_DATARATE ERRCODE_INVALID_PARITY + 1

#define ERRCODE_INVALID_EMTINTSTS ERRCODE_INVALID_SSM + 1

#define ERRCODE_INVALID_FINTSTS ERRCODE_INVALID_HFINTSTS + 1

#define ERRCODE_INVALID_FREQUENCY ERRCODE_INVALID_GROUP + 1

#define ERRCODE_INVALID_GROUP ERRCODE_INVALID_STROBE_MODE + 1

#define ERRCODE_INVALID_HANDLE ERRCODE_INVALID_BOARD_NUM + 1

#define ERRCODE_INVALID_HFINTSTS ERRCODE_INVALID_EMTINTSTS + 1

#define ERRCODE_INVALID_INPUT_MODE ERRCODE_INVALID_FREQUENCY + 1

#define ERRCODE_INVALID_LABELNUMBER ERRCODE_INVALID_TRANSSTATUS + 1

#define ERRCODE_INVALID_LOGIC_SEL ERRCODE_OUTPUT_MODE + 1

#define ERRCODE_INVALID_MASK_VALUE ERRCODE_INVALID_INPUT_MODE + 1

#define ERRCODE_INVALID_MODE ERRCODE_INVALID_MASK_VALUE + 1

#define ERRCODE_INVALID_PARITY ERRCODE_INVALID_SDI + 1

#define ERRCODE_INVALID_RECVNUMBER ERRCODE_INVALID_TRANSNUMBER + 1

#define ERRCODE_INVALID_RECVSTATUS ERRCODE_INVALID_RECVNUMBER+1

#define ERRCODE_INVALID_SDI ERRCODE_INVALID_LABELNUMBER + 1

#define ERRCODE_INVALID_SELF_TEST_DATA ERRCODE_INVALID_MODE + 1

#define ERRCODE_INVALID_SELF_TEST_ENABLE_VAL ERRCODE_INVALID_CHANNEL_NUM + 1

#define ERRCODE_INVALID_SSM ERRCODE_INVALID_DATALENGTH + 1

#define ERRCODE_INVALID_STROBE_MODE ERRCODE_INVALID_LOGIC_SEL + 1

#define ERRCODE_INVALID_TIME_BOUNCE_VAL ERRCODE_FAILED_SELF_TEST + 1

#define ERRCODE_INVALID_TRANRECVSTS ERRCODE_INT_NOT_ENABLED + 1

#define ERRCODE_INVALID_TRANSNUMBER ERRCODE_INVALID_TRANRECVSTS + 1

#define ERRCODE_INVALID_TRANSSTATUS ERRCODE_INVALID_TRPAIR + 1

#define ERRCODE_INVALID_TRPAIR ERRCODE_INVALID_RECVSTATUS + 1

#define ERRCODE_INVALID_VALUE ERRCODE_INVALID_SELF_TEST_ENABLE_VAL + 1

#define ERRCODE_NO_ERROR 0

#define ERRCODE_OUTPUT_MODE ERRCODE_INPUT_MODE + 1

#define ERRCODE_RX_UNDERFLOW ERRCODE_INVALID_COMMAND + 1

#define ERRCODE_SELF_TEST_DISABLE ERRCODE_INVALID_SELF_TEST_DATA + 1

#define ERRCODE_SUCCESS 0

#define ERRCODE_TIMEOUT ERRCODE_BUSY + 1

#define ERRCODE_TX_OVERFLOW ERRCODE_RX_UNDERFLOW + 1

Typedef Documentation

typedef int PCIeMini_status

Function Documentation

DLL char* getAlphiErrorMsg (PCIeMini_status *errCode*)

Gives the string description of an error code.

Parameters

errCode	Error code returned by a function

Return values

C-string,description	of the error

C:/Alphi/PCIeMiniSoftware/include/AlteraDma.h File Reference

Description of the low-level access routines to the SPI.

```
#include <stddef.h>
#include <stdio.h>
#include <stdint.h>
#include "AlphiDll.h"
```

Classes

- class **TransferDesc**
  Structure containing the details of a DMA transaction.
- class **AlteraDma**
  Low level SPI interface to the SPI hardware.

Macros

- #define **ALT_AVALON_DMA_MODE_MSK** (0xf)
- #define **ALT_AVALON_DMA_MODE_8** (0x0)
- #define **ALT_AVALON_DMA_MODE_16** (0x1)
- #define **ALT_AVALON_DMA_MODE_32** (0x3)
- #define **ALT_AVALON_DMA_MODE_64** (0x7)
- #define **ALT_AVALON_DMA_MODE_128** (0xf)
- #define **ALT_AVALON_DMA_TX_STREAM** (0x20)
- #define **ALT_AVALON_DMA_RX_STREAM** (0x40)
- #define **ALT_DMA_TX_STREAM_ON** (0x1)
- #define **ALT_DMA_TX_STREAM_OFF** (0x2)
- #define **ALT_DMA_RX_STREAM_ON** (0x3)
- #define **ALT_DMA_RX_STREAM_OFF** (0x4)
- #define **ALT_DMA_SET_MODE_8** (0x5)
  Transfer data in units of 8 bits.

- #define **ALT_DMA_SET_MODE_16** (0x6)
  Transfer data in units of 16 bits.

- #define **ALT_DMA_SET_MODE_32** (0x7)
  Transfer data in units of 32 bits.

- #define **ALT_DMA_SET_MODE_64** (0x8)
  Transfer data in units of 64 bits.

- #define **ALT_DMA_SET_MODE_128** (0x9)
  Transfer data in units of 128 bits.

- #define **ALT_DMA_GET_MODE** (0xa)
  Get the current transfer mode.

- #define **ALTERA_AVALON_DMA_CONTROL_BYTE_MSK** (0x1)
- #define **ALTERA_AVALON_DMA_CONTROL_HW_MSK** (0x2)
- #define **ALTERA_AVALON_DMA_CONTROL_WORD_MSK** (0x4)
- #define **ALTERA_AVALON_DMA_CONTROL_GO_MSK** (0x8)
- #define **ALTERA_AVALON_DMA_CONTROL_I_EN_MSK** (0x10)

- #define **ALTERA_AVALON_DMA_CONTROL_REEN_MSK** (0x20)
- #define **ALTERA_AVALON_DMA_CONTROL_WEEN_MSK** (0x40)
- #define **ALTERA_AVALON_DMA_CONTROL_LEEN_MSK** (0x80)
- #define **ALTERA_AVALON_DMA_CONTROL_RCON_MSK** (0x100)
- #define **ALTERA_AVALON_DMA_CONTROL_WCON_MSK** (0x200)
- #define **ALTERA_AVALON_DMA_CONTROL_DWORD_MSK** (0x400)
- #define **ALTERA_AVALON_DMA_CONTROL_QWORD_MSK** (0x800)
- #define **ALTERA_AVALON_DMA_CONTROL_SOFTWARERESET_MSK** (0x1000)
- #define **ALTERA_AVALON_DMA_STATUS_DONE_MSK** (0x1)
- #define **ALTERA_AVALON_DMA_STATUS_BUSY_MSK** (0x2)
- #define **ALTERA_AVALON_DMA_STATUS_REOP_MSK** (0x4)
- #define **ALTERA_AVALON_DMA_STATUS_WEOP_MSK** (0x8)
- #define **ALTERA_AVALON_DMA_STATUS_LEN_MSK** (0x10)
- #define **ALT_AVALON_DMA_NSLOTS** (4)
- #define **ALT_AVALON_DMA_NSLOTS_MSK** (**ALT_AVALON_DMA_NSLOTS** - 1)

Typedefs

- typedef void() **alt_txchan_done**(void *handle)
- typedef void() **alt_rxchan_done**(void *handle, void *data)

Detailed Description

Description of the low-level access routines to the SPI.

Macro Definition Documentation

#define ALT_AVALON_DMA_MODE_128 (0xf)

#define ALT_AVALON_DMA_MODE_16 (0x1)

#define ALT_AVALON_DMA_MODE_32 (0x3)

#define ALT_AVALON_DMA_MODE_64 (0x7)

#define ALT_AVALON_DMA_MODE_8 (0x0)

#define ALT_AVALON_DMA_MODE_MSK (0xf)

#define ALT_AVALON_DMA_NSLOTS (4)

#define ALT_AVALON_DMA_NSLOTS_MSK (ALT_AVALON_DMA_NSLOTS - 1)

#define ALT_AVALON_DMA_RX_STREAM (0x40)

#define ALT_AVALON_DMA_TX_STREAM (0x20)

#define ALT_DMA_GET_MODE (0xa)

Get the current transfer mode.

#define ALT_DMA_RX_STREAM_OFF (0x4)

#define ALT_DMA_RX_STREAM_ON (0x3)

#define ALT_DMA_SET_MODE_128 (0x9)

Transfer data in units of 128 bits.

#define ALT_DMA_SET_MODE_16 (0x6)

Transfer data in units of 16 bits.

#define ALT_DMA_SET_MODE_32 (0x7)

Transfer data in units of 32 bits.

#define ALT_DMA_SET_MODE_64 (0x8)

Transfer data in units of 64 bits.

#define ALT_DMA_SET_MODE_8 (0x5)

Transfer data in units of 8 bits.

#define ALT_DMA_TX_STREAM_OFF (0x2)

#define ALT_DMA_TX_STREAM_ON (0x1)

#define ALTERA_AVALON_DMA_CONTROL_BYTE_MSK (0x1)

#define ALTERA_AVALON_DMA_CONTROL_DWORD_MSK (0x400)

#define ALTERA_AVALON_DMA_CONTROL_GO_MSK (0x8)

#define ALTERA_AVALON_DMA_CONTROL_HW_MSK (0x2)

#define ALTERA_AVALON_DMA_CONTROL_I_EN_MSK (0x10)

#define ALTERA_AVALON_DMA_CONTROL_LEEN_MSK (0x80)

#define ALTERA_AVALON_DMA_CONTROL_QWORD_MSK (0x800)

#define ALTERA_AVALON_DMA_CONTROL_RCON_MSK (0x100)

#define ALTERA_AVALON_DMA_CONTROL_REEN_MSK (0x20)

#define ALTERA_AVALON_DMA_CONTROL_SOFTWARERESET_MSK (0x1000)

#define ALTERA_AVALON_DMA_CONTROL_WCON_MSK (0x200)

#define ALTERA_AVALON_DMA_CONTROL_WEEN_MSK (0x40)

#define ALTERA_AVALON_DMA_CONTROL_WORD_MSK (0x4)

#define ALTERA_AVALON_DMA_STATUS_BUSY_MSK (0x2)

#define ALTERA_AVALON_DMA_STATUS_DONE_MSK (0x1)

#define ALTERA_AVALON_DMA_STATUS_LEN_MSK (0x10)

#define ALTERA_AVALON_DMA_STATUS_REOP_MSK (0x4)

#define ALTERA_AVALON_DMA_STATUS_WEOP_MSK (0x8)

Typedef Documentation

typedef void() alt_rxchan_done(void *handle, void *data)

typedef void() alt_txchan_done(void *handle)

C:/Alphi/PCIeMiniSoftware/include/AlteraSpi.h File Reference

Description of the low-level access routines to the SPI.

```
#include <stddef.h>
#include <stdint.h>
#include "AlphiDll.h"
```

Classes

- class **AlteraSpi**
  Low level SPI interface to the SPI hardware.

Macros

- #define **ALT_AVALON_SPI_COMMAND_MERGE** (0x01)
- #define **ALT_AVALON_SPI_COMMAND_TOGGLE_SS_N** (0x02)
  option: toggle the SS line between words

- #define **ALTERA_AVALON_SPI_STATUS_E_MSK** (0x100)
- #define **ALTERA_AVALON_SPI_STATUS_E_OFST** (8)
- #define **ALTERA_AVALON_SPI_CONTROL_IROE_MSK** (0x8)
- #define **ALTERA_AVALON_SPI_CONTROL_IROE_OFST** (3)
- #define **ALTERA_AVALON_SPI_CONTROL_ITOE_MSK** (0x10)
- #define **ALTERA_AVALON_SPI_CONTROL_ITOE_OFST** (4)
- #define **ALTERA_AVALON_SPI_CONTROL_ITRDY_MSK** (0x40)
- #define **ALTERA_AVALON_SPI_CONTROL_ITRDY_OFS** (6)
- #define **ALTERA_AVALON_SPI_CONTROL_IRRDY_MSK** (0x80)
- #define **ALTERA_AVALON_SPI_CONTROL_IRRDY_OFS** (7)
- #define **ALTERA_AVALON_SPI_CONTROL_IE_MSK** (0x100)
- #define **ALTERA_AVALON_SPI_CONTROL_IE_OFST** (8)
- #define **ALTERA_AVALON_SPI_CONTROL_SSO_MSK** (0x400)
- #define **ALTERA_AVALON_SPI_CONTROL_SSO_OFST** (10)

Detailed Description

Description of the low-level access routines to the SPI.

Macro Definition Documentation

#define ALT_AVALON_SPI_COMMAND_MERGE (0x01)

#define ALT_AVALON_SPI_COMMAND_TOGGLE_SS_N (0x02)

option: toggle the SS line between words

If you need the slave select line to be toggled between words then you should set the toggle bit in the flag.

#define ALTERA_AVALON_SPI_CONTROL_IE_MSK (0x100)

#define ALTERA_AVALON_SPI_CONTROL_IE_OFST (8)

#define ALTERA_AVALON_SPI_CONTROL_IROE_MSK (0x8)

#define ALTERA_AVALON_SPI_CONTROL_IROE_OFST (3)

#define ALTERA_AVALON_SPI_CONTROL_IRRDY_MSK (0x80)

#define ALTERA_AVALON_SPI_CONTROL_IRRDY_OFS (7)

#define ALTERA_AVALON_SPI_CONTROL_ITOE_MSK (0x10)

#define ALTERA_AVALON_SPI_CONTROL_ITOE_OFST (4)

#define ALTERA_AVALON_SPI_CONTROL_ITRDY_MSK (0x40)

#define ALTERA_AVALON_SPI_CONTROL_ITRDY_OFS (6)

#define ALTERA_AVALON_SPI_CONTROL_SSO_MSK (0x400)

#define ALTERA_AVALON_SPI_CONTROL_SSO_OFST (10)

#define ALTERA_AVALON_SPI_STATUS_E_MSK (0x100)

#define ALTERA_AVALON_SPI_STATUS_E_OFST (8)

C:/Alphi/PCIeMiniSoftware/include/IrigDecoder.h File Reference

Irig Decoder class to get time.

```
#include "AlphiDll.h"
#include <stdint.h>
#include <ctime>
```

Classes

- class **IrigDecoder**
- struct **IrigDecoder::IrigDate**

Detailed Description

Irig Decoder class to get time.

C:/Alphi/PCIeMiniSoftware/include/ParallelInput.h File Reference

Description of the Alphi Parallel Input class.

```
#include "AlphiDll.h"
#include <stdint.h>
#include "AlphiErrorCodes.h"
```

Classes

- class **ParallelInput**
  Alphi Avalon Pio controller class.

Detailed Description

Description of the Alphi Parallel Input class.

C:/Alphi/PCIeMiniSoftware/include/PcieCra.h File Reference

PCIe interface CRA class.

```
#include <stdint.h>
#include <stdio.h>
#include <Windows.h>
#include "AlphiDll.h"
#include "AlphiErrorCodes.h"
```

Classes

- class **PcieCra**
  PCIe CRA module controller class.

Detailed Description

PCIe interface CRA class.

C:/Alphi/PCIeMiniSoftware/include/PCIeMini_CAN_FD.h File Reference

Definitition of the **PCIeMini_CAN_FD** board class.

```
#include <stdint.h>
#include <iostream>
#include "AlphiDll.h"
#include "AlphiBoard.h"
#include "AlphiErrorCodes.h"
#include "TCAN4550.h"
#include "IrigDecoder.h"
#include "AlteraPio.h"
#include "ParallelInput.h"
#include "CanFdNiosComm.h"
#include "AlteraDma.h"
#include "PcieCra.h"
```

Classes

- class **PCIeMini_CAN_FD**
  PCIeMini_CAN_FD *controller board object.*

Macros

- #define **PI_nINT_0** 0x0001
- #define **PI_nWAKE_0** 0x0002
- #define **PI_GPIO1_0** 0x0004
- #define **PI_GPO2_0** 0x0008
- #define **PI_nINT_1** 0x0010
- #define **PI_nWAKE_1** 0x0020
- #define **PI_GPIO1_1** 0x0040
- #define **PI_GPO2_1** 0x0080
- #define **PI_nINT_2** 0x0100
- #define **PI_nWAKE_2** 0x0200
- #define **PI_GPIO1_2** 0x0400
- #define **PI_GPO2_2** 0x0800
- #define **PI_nINT_3** 0x1000
- #define **PI_nWAKE_3** 0x2000
- #define **PI_GPIO1_3** 0x4000
- #define **PI_GPO2_3** 0x8000

Detailed Description

Definitition of the **PCIeMini_CAN_FD** board class.

Macro Definition Documentation

#define PI_GPIO1_0 0x0004

#define PI_GPIO1_1 0x0040

#define PI_GPIO1_2 0x0400

#define PI_GPIO1_3 0x4000

#define PI_GPO2_0 0x0008

#define PI_GPO2_1 0x0080

#define PI_GPO2_2 0x0800

#define PI_GPO2_3 0x8000

#define PI_nINT_0 0x0001

#define PI_nINT_1 0x0010

#define PI_nINT_2 0x0100

#define PI_nINT_3 0x1000

#define PI_nWAKE_0 0x0002

#define PI_nWAKE_1 0x0020

#define PI_nWAKE_2 0x0200

#define PI_nWAKE_3 0x2000

C:/Alphi/PCIeMiniSoftware/include/TCAN4550.h File Reference

This file contains **TCAN4550** functions.

```
#include "eusci_b_spi.h"
#include "TCAN4x5x_SPI.h"
#include "TCAN4x5x_Reg.h"
#include "TCAN4x5x_Data_Structs.h"
#include "AlteraPio.h"
#include "ParallelInput.h"
```

Classes

- class **TcanInterface**
  *This class implements the **TCAN4550** SPI interface.*
- class **TCAN4550**

Macros

- #define **TCAN4x5x_MCAN_VERIFY_CONFIGURATION_WRITES**
  If TCAN4x5x_MCAN_VERIFY_CONFIGURATION_WRITES is defined, then each MCAN configuration write will be read and verified for correctness.

- #define **TCAN4x5x_DEVICE_VERIFY_CONFIGURATION_WRITES**
  If TCAN4x5x_DEVICE_VERIFY_CONFIGURATION_WRITES is defined, then each device configuration write will be read and verified for correctness.

Enumerations

- enum **TCAN4x5x_MCAN_FIFO_Enum** { **RXFIFO0**, **RXFIFO1** }
- enum **TCAN4x5x_WDT_Timer_Enum** { **TCAN4x5x_WDT_60MS**, **TCAN4x5x_WDT_600MS**, **TCAN4x5x_WDT_3S**, **TCAN4x5x_WDT_6S** }
- enum **TCAN4x5x_Device_Test_Mode_Enum** { **TCAN4x5x_DEVICE_TEST_MODE_NORMAL**, **TCAN4x5x_DEVICE_TEST_MODE_PHY**, **TCAN4x5x_DEVICE_TEST_MODE_CONTROLLER** }
- enum **TCAN4x5x_Device_Mode_Enum** { **TCAN4x5x_DEVICE_MODE_NORMAL**, **TCAN4x5x_DEVICE_MODE_STANDBY**, **TCAN4x5x_DEVICE_MODE_SLEEP** }

Detailed Description

This file contains **TCAN4550** functions.

It relies on the TCAN4x5x_SPI abstraction functions Additional Feature Sets of **TCAN4550** vs TCAN4x5x:

- Watchdog Timer Functions

Macro Definition Documentation

#define TCAN4x5x_DEVICE_VERIFY_CONFIGURATION_WRITES

If TCAN4x5x_DEVICE_VERIFY_CONFIGURATION_WRITES is defined, then each device configuration write will be read and verified for correctness.

#define TCAN4x5x_MCAN_VERIFY_CONFIGURATION_WRITES

If TCAN4x5x_MCAN_VERIFY_CONFIGURATION_WRITES is defined, then each MCAN configuration write will be read and verified for correctness.

Enumeration Type Documentation

enum TCAN4x5x_Device_Mode_Enum

Enumerator:

TCAN4x5x_DEVICE_MODE_NORMAL	
TCAN4x5x_DEVICE_MODE_STANDBY	
TCAN4x5x_DEVICE_MODE_SLEEP	

enum TCAN4x5x_Device_Test_Mode_Enum

Enumerator:

TCAN4x5x_DEVICE_TEST_MODE_NORMAL	
TCAN4x5x_DEVICE_TEST_MODE_PHY	
TCAN4x5x_DEVICE_TEST_MODE_CONTROLLER	

enum TCAN4x5x_MCAN_FIFO_Enum

Enumerator:

RXFIFO0	
RXFIFO1	

enum TCAN4x5x_WDT_Timer_Enum

Enumerator:

TCAN4x5x_WDT_60MS	
TCAN4x5x_WDT_600MS	
TCAN4x5x_WDT_3S	

TCAN4x5x_WDT_6S	

C:/Alphi/PCIeMiniSoftware/include/TCAN4x5x_Data_Structs.h File Reference

This file contains the TCAN4x5x data structures.
`#include <stdint.h>`

Classes

- struct **TCAN4x5x_MCAN_Data_Timing_Simple**
  Used to setup the data timing parameters of the MCAN module This is a simplified struct, requiring only the prescaler value (1:x), number of time quanta before and after the sample point.
- struct **TCAN4x5x_MCAN_Data_Timing_Raw**
  Used to setup the timing parameters of the MCAN module This is the raw MCAN form of the struct which takes in the same values as the actual Bosch MCAN core.
- struct **TCAN4x5x_MCAN_Nominal_Timing_Simple**
  Used to setup the nominal timing parameters of the MCAN module This is a simplified struct, requiring only the prescaler value (1:x), number of time quanta before and after the sample point.
- struct **TCAN4x5x_MCAN_Nominal_Timing_Raw**
  Used to setup the nominal timing parameters of the MCAN module This is the raw MCAN form of the struct which takes in the same values as the actual Bosch MCAN core.
- struct **TCAN4x5x_MRAM_Config**
  Defines the number of MRAM elements and the size of the elements.
- struct **TCAN4x5x_MCAN_CCCR_Config**
  struct containing the bit fields of the MCAN CCCR register
- struct **TCAN4x5x_MCAN_Interrupts**
  Struct containing the MCAN interrupt bit field.
- struct **TCAN4x5x_MCAN_Interrupt_Enable**
  Struct containing the MCAN interrupt enable bit field.
- struct **TCAN4x5x_MCAN_RX_Header**
  CAN message header.
- struct **TCAN4x5x_MCAN_TX_Header**
  CAN message header for transmitted messages.
- struct **TCAN4x5x_MCAN_SID_Filter**
  Standard ID filter struct.
- struct **TCAN4x5x_MCAN_XID_Filter**
  Extended ID filter struct.
- struct **TCAN4x5x_Device_Interrupts**
  Struct containing the device interrupt bit field.
- struct **TCAN4x5x_Device_Interrupt_Enable**
  Struct containing the device interrupt enable bit field.

Enumerations

- enum **TCAN4x5x_MRAM_Element_Data_Size** { **MRAM_8_Byte_Data** = 0, **MRAM_12_Byte_Data** = 0x1, **MRAM_16_Byte_Data** = 0x2, **MRAM_20_Byte_Data** = 0x3, **MRAM_24_Byte_Data** = 0x4, **MRAM_32_Byte_Data** = 0x5, **MRAM_48_Byte_Data** = 0x6, **MRAM_64_Byte_Data** = 0x7 }
  Data payload defines for the different MRAM sections, used by the ***`TCAN4x5x_MRAM_Config`*** *struct.*
- enum **TCAN4x5x_SID_SFEC_Values** { **TCAN4x5x_SID_SFEC_DISABLED** = 0x0, **TCAN4x5x_SID_SFEC_STORERX0** = 0x1, **TCAN4x5x_SID_SFEC_STORERX1** = 0x2, **TCAN4x5x_SID_SFEC_REJECTMATCH** = 0x3, **TCAN4x5x_SID_SFEC_PRIORITY** =

0x4, **TCAN4x5x_SID_SFEC_PRIORITYSTORERX0** = 0x5, **TCAN4x5x_SID_SFEC_PRIORITYSTORERX1** = 0x6, **TCAN4x5x_SID_SFEC_STORERXBUFORDEBUG** = 0x7 }

- enum **TCAN4x5x_SID_SFT_Values** { **TCAN4x5x_SID_SFT_DISABLED** = 0x3, **TCAN4x5x_SID_SFT_CLASSIC** = 0x2, **TCAN4x5x_SID_SFT_DUALID** = 0x1, **TCAN4x5x_SID_SFT_RANGE** = 0x0 }
- enum **TCAN4x5x_XID_EFEC_Values** { **TCAN4x5x_XID_EFEC_DISABLED** = 0x0, **TCAN4x5x_XID_EFEC_STORERX0** = 0x1, **TCAN4x5x_XID_EFEC_STORERX1** = 0x2, **TCAN4x5x_XID_EFEC_REJECTMATCH** = 0x3, **TCAN4x5x_XID_EFEC_PRIORITY** = 0x4, **TCAN4x5x_XID_EFEC_PRIORITYSTORERX0** = 0x5, **TCAN4x5x_XID_EFEC_PRIORITYSTORERX1** = 0x6, **TCAN4x5x_XID_EFEC_STORERXBUFORDEBUG** = 0x7 }
- enum **TCAN4x5x_XID_EFT_Values** { **TCAN4x5x_XID_EFT_RANGENOMASK** = 0x3, **TCAN4x5x_XID_EFT_CLASSIC** = 0x2, **TCAN4x5x_XID_EFT_DUALID** = 0x1, **TCAN4x5x_XID_EFT_RANGE** = 0x0 }

Detailed Description

This file contains the TCAN4x5x data structures.

It relies on the TCAN4x5x_SPI abstraction functions Additional Feature Sets of **TCAN4550** vs TCAN4x5x:

- Watchdog Timer Functions

Created on: Oct 1, 2017 Author: Texas Instruments

Enumeration Type Documentation

enum TCAN4x5x_MRAM_Element_Data_Size

Data payload defines for the different MRAM sections, used by the **`TCAN4x5x_MRAM_Config`** struct.

Enumerator:

MRAM_8_Byte_Data	8 bytes of data payload
MRAM_12_Byte_Data	12 bytes of data payload
MRAM_16_Byte_Data	16 bytes of data payload
MRAM_20_Byte_Data	20 bytes of data payload
MRAM_24_Byte_Data	24 bytes of data payload
MRAM_32_Byte_Data	32 bytes of data payload
MRAM_48_Byte_Data	48 bytes of data payload
MRAM_64_Byte_Data	64 bytes of data payload

enum TCAN4x5x_SID_SFEC_Values

Enumerator:

TCAN4x5x_SID_SFEC_DISABLED	Disabled filter. This filter will do nothing if it matches a packet.
TCAN4x5x_SID_SFEC_STORERX0	Store in RX FIFO 0 if the filter matches the incoming message.
TCAN4x5x_SID_SFEC_STORERX1	Store in RX FIFO 1 if the filter matches the incoming message.
TCAN4x5x_SID_SFEC_REJECTMATCH	Reject the packet (do not store, do not notify MCU) if the filter matches the incoming message.
TCAN4x5x_SID_SFEC_PRIORITY	Store in default location but set a high priority message interrupt if the filter matches the incoming message.
TCAN4x5x_SID_SFEC_PRIORITYSTORERX0	Store in RX FIFO 0 and set a high priority message interrupt if the filter matches the incoming message.
TCAN4x5x_SID_SFEC_PRIORITYSTORERX1	Store in RX FIFO 1 and set a high priority message interrupt if the filter matches the incoming message.

TCAN4x5x_SID_SFEC_STORERXBUFORDEBUG	Store in RX Buffer for debug if the filter matches the incoming message. SFT is ignored if this is selected.

enum TCAN4x5x_SID_SFT_Values

Enumerator:

TCAN4x5x_SID_SFT_DISABLED	Disabled filter. This filter will match nothing.
TCAN4x5x_SID_SFT_CLASSIC	Classic filter with SFID1 as the ID to match, and SFID2 as the bit mask that applies to SFID1.
TCAN4x5x_SID_SFT_DUALID	Dual ID filter, where both SFID1 and SFID2 hold IDs that can match (must match exactly)
TCAN4x5x_SID_SFT_RANGE	Range Filter. SFID1 holds the start address, and SFID2 holds the end address. Any address in between will match.

enum TCAN4x5x_XID_EFEC_Values

Enumerator:

TCAN4x5x_XID_EFEC_DISABLED	Disabled filter. This filter will do nothing if it matches a packet.
TCAN4x5x_XID_EFEC_STORERX0	Store in RX FIFO 0 if the filter matches the incoming message.
TCAN4x5x_XID_EFEC_STORERX1	Store in RX FIFO 1 if the filter matches the incoming message.
TCAN4x5x_XID_EFEC_REJECTMATCH	Reject the packet (do not store, do not notify MCU) if the filter matches the incoming message.
TCAN4x5x_XID_EFEC_PRIORITY	Store in default location but set a high priority message interrupt if the filter matches the incoming message.
TCAN4x5x_XID_EFEC_PRIORITYSTORERX0	Store in RX FIFO 0 and set a high priority message interrupt if the filter matches the incoming message.
TCAN4x5x_XID_EFEC_PRIORITYSTORERX1	Store in RX FIFO 1 and set a high priority message interrupt if the filter matches the incoming message.
TCAN4x5x_XID_EFEC_STORERXBUFORDEBUG	Store in RX Buffer for debug if the filter matches the incoming message.

enum TCAN4x5x_XID_EFT_Values

Enumerator:

TCAN4x5x_XID_EFT_RANGENOMASK	Range filter from EFID1 to EFID2, The XIDAM mask is not applied.
TCAN4x5x_XID_EFT_CLASSIC	Classic Filter, EFID1 is the ID/filter, and EFID2 is the mask.
TCAN4x5x_XID_EFT_DUALID	Dual ID filter matches if the incoming ID matches EFID1 or EFID2.
TCAN4x5x_XID_EFT_RANGE	Range filter from EFID1 to EFID2.

C:/Alphi/PCIeMiniSoftware/include/TCAN4x5x_Reg.h File Reference

This file contains the register definitions for the TCAN4x5x Family.

Macros

- #define **MRAM_SIZE** 2048
- #define **REG_SPI_CONFIG** 0x0000
- #define **REG_DEV_CONFIG** 0x0800
- #define **REG_MCAN** 0x1000
- #define **REG_MRAM** 0x8000
- #define **REG_SPI_DEVICE_ID0** 0x0000
- #define **REG_SPI_DEVICE_ID1** 0x0004
- #define **REG_SPI_REVISION** 0x0008
- #define **REG_SPI_STATUS** 0x000C
- #define **REG_SPI_ERROR_STATUS_MASK** 0x0010
- #define **REG_DEV_MODES_AND_PINS** 0x0800
- #define **REG_DEV_TIMESTAMP_PRESCALER** 0x0804
- #define **REG_DEV_TEST_REGISTERS** 0x0808
- #define **REG_DEV_IR** 0x0820
- #define **REG_DEV_IE** 0x0830
- #define **REG_MCAN_CREL** 0x1000
- #define **REG_MCAN_ENDN** 0x1004
- #define **REG_MCAN_CUST** 0x1008
- #define **REG_MCAN_DBTP** 0x100C
- #define **REG_MCAN_TEST** 0x1010
- #define **REG_MCAN_RWD** 0x1014
- #define **REG_MCAN_CCCR** 0x1018
- #define **REG_MCAN_NBTP** 0x101C
- #define **REG_MCAN_TSCC** 0x1020
- #define **REG_MCAN_TSCV** 0x1024
- #define **REG_MCAN_TOCC** 0x1028
- #define **REG_MCAN_TOCV** 0x102C
- #define **REG_MCAN_ECR** 0x1040
- #define **REG_MCAN_PSR** 0x1044
- #define **REG_MCAN_TDCR** 0x1048
- #define **REG_MCAN_IR** 0x1050
- #define **REG_MCAN_IE** 0x1054
- #define **REG_MCAN_ILS** 0x1058
- #define **REG_MCAN_ILE** 0x105C
- #define **REG_MCAN_GFC** 0x1080
- #define **REG_MCAN_SIDFC** 0x1084
- #define **REG_MCAN_XIDFC** 0x1088
- #define **REG_MCAN_XIDAM** 0x1090
- #define **REG_MCAN_HPMS** 0x1094
- #define **REG_MCAN_NDAT1** 0x1098
- #define **REG_MCAN_NDAT2** 0x109C
- #define **REG_MCAN_RXF0C** 0x10A0
- #define **REG_MCAN_RXF0S** 0x10A4
- #define **REG_MCAN_RXF0A** 0x10A8
- #define **REG_MCAN_RXBC** 0x10AC
- #define **REG_MCAN_RXF1C** 0x10B0
- #define **REG_MCAN_RXF1S** 0x10B4
- #define **REG_MCAN_RXF1A** 0x10B8

- #define **REG_MCAN_RXESC** 0x10BC
- #define **REG_MCAN_TXBC** 0x10C0
- #define **REG_MCAN_TXFQS** 0x10C4
- #define **REG_MCAN_TXESC** 0x10C8
- #define **REG_MCAN_TXBRP** 0x10CC
- #define **REG_MCAN_TXBAR** 0x10D0
- #define **REG_MCAN_TXBCR** 0x10D4
- #define **REG_MCAN_TXBTO** 0x10D8
- #define **REG_MCAN_TXBCF** 0x10DC
- #define **REG_MCAN_TXBTIE** 0x10E0
- #define **REG_MCAN_TXBCIE** 0x10E4
- #define **REG_MCAN_TXEFC** 0x10F0
- #define **REG_MCAN_TXEFS** 0x10F4
- #define **REG_MCAN_TXEFA** 0x10F8
- #define **MCAN_DLC_0B** 0x00000000
- #define **MCAN_DLC_1B** 0x00000001
- #define **MCAN_DLC_2B** 0x00000002
- #define **MCAN_DLC_3B** 0x00000003
- #define **MCAN_DLC_4B** 0x00000004
- #define **MCAN_DLC_5B** 0x00000005
- #define **MCAN_DLC_6B** 0x00000006
- #define **MCAN_DLC_7B** 0x00000007
- #define **MCAN_DLC_8B** 0x00000008
- #define **MCAN_DLC_12B** 0x00000009
- #define **MCAN_DLC_16B** 0x0000000A
- #define **MCAN_DLC_20B** 0x0000000B
- #define **MCAN_DLC_24B** 0x0000000C
- #define **MCAN_DLC_32B** 0x0000000D
- #define **MCAN_DLC_48B** 0x0000000E
- #define **MCAN_DLC_64B** 0x0000000F
- #define **REG_BITS_MCAN_DBTP_TDC_EN** 0x00800000
- #define **REG_BITS_MCAN_TEST_RX_DOM** 0x00000000
- #define **REG_BITS_MCAN_TEST_RX_REC** 0x00000080
- #define **REG_BITS_MCAN_TEST_TX_SP** 0x00000020
- #define **REG_BITS_MCAN_TEST_TX_DOM** 0x00000040
- #define **REG_BITS_MCAN_TEST_TX_REC** 0x00000060
- #define **REG_BITS_MCAN_TEST_LOOP_BACK** 0x00000010
- #define **REG_BITS_MCAN_CCCR_RESERVED_MASK** 0xFFFF0C00
- #define **REG_BITS_MCAN_CCCR_NISO_ISO** 0x00000000
- #define **REG_BITS_MCAN_CCCR_NISO_BOSCH** 0x00008000
- #define **REG_BITS_MCAN_CCCR_TXP** 0x00004000
- #define **REG_BITS_MCAN_CCCR_EFBI** 0x00002000
- #define **REG_BITS_MCAN_CCCR_PXHD_DIS** 0x00001000
- #define **REG_BITS_MCAN_CCCR_BRSE** 0x00000200
- #define **REG_BITS_MCAN_CCCR_FDOE** 0x00000100
- #define **REG_BITS_MCAN_CCCR_TEST** 0x00000080
- #define **REG_BITS_MCAN_CCCR_DAR_DIS** 0x00000040
- #define **REG_BITS_MCAN_CCCR_MON** 0x00000020
- #define **REG_BITS_MCAN_CCCR_CSR** 0x00000010
- #define **REG_BITS_MCAN_CCCR_CSA** 0x00000008
- #define **REG_BITS_MCAN_CCCR_ASM** 0x00000004
- #define **REG_BITS_MCAN_CCCR_CCE** 0x00000002
- #define **REG_BITS_MCAN_CCCR_INIT** 0x00000001
- #define **REG_BITS_MCAN_IE_ARAE** 0x20000000
- #define **REG_BITS_MCAN_IE_PEDE** 0x10000000
- #define **REG_BITS_MCAN_IE_PEAE** 0x08000000
- #define **REG_BITS_MCAN_IE_WDIE** 0x04000000

- #define **REG_BITS_MCAN_IE_BOE** 0x02000000
- #define **REG_BITS_MCAN_IE_EWE** 0x01000000
- #define **REG_BITS_MCAN_IE_EPE** 0x00800000
- #define **REG_BITS_MCAN_IE_ELOE** 0x00400000
- #define **REG_BITS_MCAN_IE_BEUE** 0x00200000
- #define **REG_BITS_MCAN_IE_BECE** 0x00100000
- #define **REG_BITS_MCAN_IE_DRXE** 0x00080000
- #define **REG_BITS_MCAN_IE_TOOE** 0x00040000
- #define **REG_BITS_MCAN_IE_MRAFE** 0x00020000
- #define **REG_BITS_MCAN_IE_TSWE** 0x00010000
- #define **REG_BITS_MCAN_IE_TEFLE** 0x00008000
- #define **REG_BITS_MCAN_IE_TEFFE** 0x00004000
- #define **REG_BITS_MCAN_IE_TEFWE** 0x00002000
- #define **REG_BITS_MCAN_IE_TEFNE** 0x00001000
- #define **REG_BITS_MCAN_IE_TFEE** 0x00000800
- #define **REG_BITS_MCAN_IE_TCFE** 0x00000400
- #define **REG_BITS_MCAN_IE_TCE** 0x00000200
- #define **REG_BITS_MCAN_IE_HPME** 0x00000100
- #define **REG_BITS_MCAN_IE_RF1LE** 0x00000080
- #define **REG_BITS_MCAN_IE_RF1FE** 0x00000040
- #define **REG_BITS_MCAN_IE_RF1WE** 0x00000020
- #define **REG_BITS_MCAN_IE_RF1NE** 0x00000010
- #define **REG_BITS_MCAN_IE_RF0LE** 0x00000008
- #define **REG_BITS_MCAN_IE_RF0FE** 0x00000004
- #define **REG_BITS_MCAN_IE_RF0WE** 0x00000002
- #define **REG_BITS_MCAN_IE_RF0NE** 0x00000001
- #define **REG_BITS_MCAN_IR_ARA** 0x20000000
- #define **REG_BITS_MCAN_IR_PED** 0x10000000
- #define **REG_BITS_MCAN_IR_PEA** 0x08000000
- #define **REG_BITS_MCAN_IR_WDI** 0x04000000
- #define **REG_BITS_MCAN_IR_BO** 0x02000000
- #define **REG_BITS_MCAN_IR_EW** 0x01000000
- #define **REG_BITS_MCAN_IR_EP** 0x00800000
- #define **REG_BITS_MCAN_IR_ELO** 0x00400000
- #define **REG_BITS_MCAN_IR_BEU** 0x00200000
- #define **REG_BITS_MCAN_IR_BEC** 0x00100000
- #define **REG_BITS_MCAN_IR_DRX** 0x00080000
- #define **REG_BITS_MCAN_IR_TOO** 0x00040000
- #define **REG_BITS_MCAN_IR_MRAF** 0x00020000
- #define **REG_BITS_MCAN_IR_TSW** 0x00010000
- #define **REG_BITS_MCAN_IR_TEFL** 0x00008000
- #define **REG_BITS_MCAN_IR_TEFF** 0x00004000
- #define **REG_BITS_MCAN_IR_TEFW** 0x00002000
- #define **REG_BITS_MCAN_IR_TEFN** 0x00001000
- #define **REG_BITS_MCAN_IR_TFE** 0x00000800
- #define **REG_BITS_MCAN_IR_TCF** 0x00000400
- #define **REG_BITS_MCAN_IR_TC** 0x00000200
- #define **REG_BITS_MCAN_IR_HPM** 0x00000100
- #define **REG_BITS_MCAN_IR_RF1L** 0x00000080
- #define **REG_BITS_MCAN_IR_RF1F** 0x00000040
- #define **REG_BITS_MCAN_IR_RF1W** 0x00000020
- #define **REG_BITS_MCAN_IR_RF1N** 0x00000010
- #define **REG_BITS_MCAN_IR_RF0L** 0x00000008
- #define **REG_BITS_MCAN_IR_RF0F** 0x00000004
- #define **REG_BITS_MCAN_IR_RF0W** 0x00000002
- #define **REG_BITS_MCAN_IR_RF0N** 0x00000001
- #define **REG_BITS_MCAN_IE_ARAL** 0x20000000

- #define **REG_BITS_MCAN_IE_PEDL** 0x10000000
- #define **REG_BITS_MCAN_IE_PEAL** 0x08000000
- #define **REG_BITS_MCAN_IE_WDIL** 0x04000000
- #define **REG_BITS_MCAN_IE_BOL** 0x02000000
- #define **REG_BITS_MCAN_IE_EWL** 0x01000000
- #define **REG_BITS_MCAN_IE_EPL** 0x00800000
- #define **REG_BITS_MCAN_IE_ELOL** 0x00400000
- #define **REG_BITS_MCAN_IE_BEUL** 0x00200000
- #define **REG_BITS_MCAN_IE_BECL** 0x00100000
- #define **REG_BITS_MCAN_IE_DRXL** 0x00080000
- #define **REG_BITS_MCAN_IE_TOOL** 0x00040000
- #define **REG_BITS_MCAN_IE_MRAFL** 0x00020000
- #define **REG_BITS_MCAN_IE_TSWL** 0x00010000
- #define **REG_BITS_MCAN_IE_TEFLL** 0x00008000
- #define **REG_BITS_MCAN_IE_TEFFL** 0x00004000
- #define **REG_BITS_MCAN_IE_TEFWL** 0x00002000
- #define **REG_BITS_MCAN_IE_TEFNL** 0x00001000
- #define **REG_BITS_MCAN_IE_TFEL** 0x00000800
- #define **REG_BITS_MCAN_IE_TCFL** 0x00000400
- #define **REG_BITS_MCAN_IE_TCL** 0x00000200
- #define **REG_BITS_MCAN_IE_HPML** 0x00000100
- #define **REG_BITS_MCAN_IE_RF1LL** 0x00000080
- #define **REG_BITS_MCAN_IE_RF1FL** 0x00000040
- #define **REG_BITS_MCAN_IE_RF1WL** 0x00000020
- #define **REG_BITS_MCAN_IE_RF1NL** 0x00000010
- #define **REG_BITS_MCAN_IE_RF0LL** 0x00000008
- #define **REG_BITS_MCAN_IE_RF0FL** 0x00000004
- #define **REG_BITS_MCAN_IE_RF0WL** 0x00000002
- #define **REG_BITS_MCAN_IE_RF0NL** 0x00000001
- #define **REG_BITS_MCAN_ILE_EINT1** 0x00000002
- #define **REG_BITS_MCAN_ILE_EINT0** 0x00000001
- #define **REG_BITS_MCAN_GFC_ANFS_FIFO0** 0x00000000
- #define **REG_BITS_MCAN_GFC_ANFS_FIFO1** 0x00000010
- #define **REG_BITS_MCAN_GFC_ANFE_FIFO0** 0x00000000
- #define **REG_BITS_MCAN_GFC_ANFE_FIFO1** 0x00000004
- #define **REG_BITS_MCAN_GFC_RRFS** 0x00000002
- #define **REG_BITS_MCAN_GFC_RRFE** 0x00000001
- #define **REG_BITS_MCAN_RXF0C_F0OM_OVERWRITE** 0x80000000
- #define **REG_BITS_MCAN_RXESC_RBDS_8B** 0x00000000
- #define **REG_BITS_MCAN_RXESC_RBDS_12B** 0x00000100
- #define **REG_BITS_MCAN_RXESC_RBDS_16B** 0x00000200
- #define **REG_BITS_MCAN_RXESC_RBDS_20B** 0x00000300
- #define **REG_BITS_MCAN_RXESC_RBDS_24B** 0x00000400
- #define **REG_BITS_MCAN_RXESC_RBDS_32B** 0x00000500
- #define **REG_BITS_MCAN_RXESC_RBDS_48B** 0x00000600
- #define **REG_BITS_MCAN_RXESC_RBDS_64B** 0x00000700
- #define **REG_BITS_MCAN_RXESC_F1DS_8B** 0x00000000
- #define **REG_BITS_MCAN_RXESC_F1DS_12B** 0x00000010
- #define **REG_BITS_MCAN_RXESC_F1DS_16B** 0x00000020
- #define **REG_BITS_MCAN_RXESC_F1DS_20B** 0x00000030
- #define **REG_BITS_MCAN_RXESC_F1DS_24B** 0x00000040
- #define **REG_BITS_MCAN_RXESC_F1DS_32B** 0x00000050
- #define **REG_BITS_MCAN_RXESC_F1DS_48B** 0x00000060
- #define **REG_BITS_MCAN_RXESC_F1DS_64B** 0x00000070
- #define **REG_BITS_MCAN_RXESC_F0DS_8B** 0x00000000
- #define **REG_BITS_MCAN_RXESC_F0DS_12B** 0x00000001
- #define **REG_BITS_MCAN_RXESC_F0DS_16B** 0x00000002

- #define **REG_BITS_MCAN_RXESC_F0DS_20B** 0x00000003
- #define **REG_BITS_MCAN_RXESC_F0DS_24B** 0x00000004
- #define **REG_BITS_MCAN_RXESC_F0DS_32B** 0x00000005
- #define **REG_BITS_MCAN_RXESC_F0DS_48B** 0x00000006
- #define **REG_BITS_MCAN_RXESC_F0DS_64B** 0x00000007
- #define **REG_BITS_MCAN_TXBC_TFQM** 0x40000000
- #define **REG_BITS_MCAN_TXESC_TBDS_8** 0x00000000
- #define **REG_BITS_MCAN_TXESC_TBDS_12** 0x00000001
- #define **REG_BITS_MCAN_TXESC_TBDS_16** 0x00000002
- #define **REG_BITS_MCAN_TXESC_TBDS_20** 0x00000003
- #define **REG_BITS_MCAN_TXESC_TBDS_24** 0x00000004
- #define **REG_BITS_MCAN_TXESC_TBDS_32** 0x00000005
- #define **REG_BITS_MCAN_TXESC_TBDS_48** 0x00000006
- #define **REG_BITS_MCAN_TXESC_TBDS_64** 0x00000007
- #define **REG_BITS_MCAN_TSCC_PRESCALER_MASK** 0x000F0000
- #define **REG_BITS_MCAN_TSCC_COUNTER_ALWAYS_0** 0x00000000
- #define **REG_BITS_MCAN_TSCC_COUNTER_USE_TCP** 0x00000001
- #define **REG_BITS_MCAN_TSCC_COUNTER_EXTERNAL** 0x00000002
- #define **REG_BITS_MCAN_TXBAR_AR31** 0x80000000
- #define **REG_BITS_MCAN_TXBAR_AR30** 0x40000000
- #define **REG_BITS_MCAN_TXBAR_AR29** 0x20000000
- #define **REG_BITS_MCAN_TXBAR_AR28** 0x10000000
- #define **REG_BITS_MCAN_TXBAR_AR27** 0x08000000
- #define **REG_BITS_MCAN_TXBAR_AR26** 0x04000000
- #define **REG_BITS_MCAN_TXBAR_AR25** 0x02000000
- #define **REG_BITS_MCAN_TXBAR_AR24** 0x01000000
- #define **REG_BITS_MCAN_TXBAR_AR23** 0x00800000
- #define **REG_BITS_MCAN_TXBAR_AR22** 0x00400000
- #define **REG_BITS_MCAN_TXBAR_AR21** 0x00200000
- #define **REG_BITS_MCAN_TXBAR_AR20** 0x00100000
- #define **REG_BITS_MCAN_TXBAR_AR19** 0x00080000
- #define **REG_BITS_MCAN_TXBAR_AR18** 0x00040000
- #define **REG_BITS_MCAN_TXBAR_AR17** 0x00020000
- #define **REG_BITS_MCAN_TXBAR_AR16** 0x00010000
- #define **REG_BITS_MCAN_TXBAR_AR15** 0x00008000
- #define **REG_BITS_MCAN_TXBAR_AR14** 0x00004000
- #define **REG_BITS_MCAN_TXBAR_AR13** 0x00002000
- #define **REG_BITS_MCAN_TXBAR_AR12** 0x00001000
- #define **REG_BITS_MCAN_TXBAR_AR11** 0x00000800
- #define **REG_BITS_MCAN_TXBAR_AR10** 0x00000400
- #define **REG_BITS_MCAN_TXBAR_AR9** 0x00000200
- #define **REG_BITS_MCAN_TXBAR_AR8** 0x00000100
- #define **REG_BITS_MCAN_TXBAR_AR7** 0x00000080
- #define **REG_BITS_MCAN_TXBAR_AR6** 0x00000040
- #define **REG_BITS_MCAN_TXBAR_AR5** 0x00000020
- #define **REG_BITS_MCAN_TXBAR_AR4** 0x00000010
- #define **REG_BITS_MCAN_TXBAR_AR3** 0x00000008
- #define **REG_BITS_MCAN_TXBAR_AR2** 0x00000004
- #define **REG_BITS_MCAN_TXBAR_AR1** 0x00000002
- #define **REG_BITS_MCAN_TXBAR_AR0** 0x00000001
- #define **REG_BITS_MCAN_TXBCR_CR31** 0x80000000
- #define **REG_BITS_MCAN_TXBCR_CR30** 0x40000000
- #define **REG_BITS_MCAN_TXBCR_CR29** 0x20000000
- #define **REG_BITS_MCAN_TXBCR_CR28** 0x10000000
- #define **REG_BITS_MCAN_TXBCR_CR27** 0x08000000
- #define **REG_BITS_MCAN_TXBCR_CR26** 0x04000000
- #define **REG_BITS_MCAN_TXBCR_CR25** 0x02000000

- #define **REG_BITS_MCAN_TXBCR_CR24** 0x01000000
- #define **REG_BITS_MCAN_TXBCR_CR23** 0x00800000
- #define **REG_BITS_MCAN_TXBCR_CR22** 0x00400000
- #define **REG_BITS_MCAN_TXBCR_CR21** 0x00200000
- #define **REG_BITS_MCAN_TXBCR_CR20** 0x00100000
- #define **REG_BITS_MCAN_TXBCR_CR19** 0x00080000
- #define **REG_BITS_MCAN_TXBCR_CR18** 0x00040000
- #define **REG_BITS_MCAN_TXBCR_CR17** 0x00020000
- #define **REG_BITS_MCAN_TXBCR_CR16** 0x00010000
- #define **REG_BITS_MCAN_TXBCR_CR15** 0x00008000
- #define **REG_BITS_MCAN_TXBCR_CR14** 0x00004000
- #define **REG_BITS_MCAN_TXBCR_CR13** 0x00002000
- #define **REG_BITS_MCAN_TXBCR_CR12** 0x00001000
- #define **REG_BITS_MCAN_TXBCR_CR11** 0x00000800
- #define **REG_BITS_MCAN_TXBCR_CR10** 0x00000400
- #define **REG_BITS_MCAN_TXBCR_CR9** 0x00000200
- #define **REG_BITS_MCAN_TXBCR_CR8** 0x00000100
- #define **REG_BITS_MCAN_TXBCR_CR7** 0x00000080
- #define **REG_BITS_MCAN_TXBCR_CR6** 0x00000040
- #define **REG_BITS_MCAN_TXBCR_CR5** 0x00000020
- #define **REG_BITS_MCAN_TXBCR_CR4** 0x00000010
- #define **REG_BITS_MCAN_TXBCR_CR3** 0x00000008
- #define **REG_BITS_MCAN_TXBCR_CR2** 0x00000004
- #define **REG_BITS_MCAN_TXBCR_CR1** 0x00000002
- #define **REG_BITS_MCAN_TXBCR_CR0** 0x00000001
- #define **REG_BITS_MCAN_TXBTIE_TIE31** 0x80000000
- #define **REG_BITS_MCAN_TXBTIE_TIE30** 0x40000000
- #define **REG_BITS_MCAN_TXBTIE_TIE29** 0x20000000
- #define **REG_BITS_MCAN_TXBTIE_TIE28** 0x10000000
- #define **REG_BITS_MCAN_TXBTIE_TIE27** 0x08000000
- #define **REG_BITS_MCAN_TXBTIE_TIE26** 0x04000000
- #define **REG_BITS_MCAN_TXBTIE_TIE25** 0x02000000
- #define **REG_BITS_MCAN_TXBTIE_TIE24** 0x01000000
- #define **REG_BITS_MCAN_TXBTIE_TIE23** 0x00800000
- #define **REG_BITS_MCAN_TXBTIE_TIE22** 0x00400000
- #define **REG_BITS_MCAN_TXBTIE_TIE21** 0x00200000
- #define **REG_BITS_MCAN_TXBTIE_TIE20** 0x00100000
- #define **REG_BITS_MCAN_TXBTIE_TIE19** 0x00080000
- #define **REG_BITS_MCAN_TXBTIE_TIE18** 0x00040000
- #define **REG_BITS_MCAN_TXBTIE_TIE17** 0x00020000
- #define **REG_BITS_MCAN_TXBTIE_TIE16** 0x00010000
- #define **REG_BITS_MCAN_TXBTIE_TIE15** 0x00008000
- #define **REG_BITS_MCAN_TXBTIE_TIE14** 0x00004000
- #define **REG_BITS_MCAN_TXBTIE_TIE13** 0x00002000
- #define **REG_BITS_MCAN_TXBTIE_TIE12** 0x00001000
- #define **REG_BITS_MCAN_TXBTIE_TIE11** 0x00000800
- #define **REG_BITS_MCAN_TXBTIE_TIE10** 0x00000400
- #define **REG_BITS_MCAN_TXBTIE_TIE9** 0x00000200
- #define **REG_BITS_MCAN_TXBTIE_TIE8** 0x00000100
- #define **REG_BITS_MCAN_TXBTIE_TIE7** 0x00000080
- #define **REG_BITS_MCAN_TXBTIE_TIE6** 0x00000040
- #define **REG_BITS_MCAN_TXBTIE_TIE5** 0x00000020
- #define **REG_BITS_MCAN_TXBTIE_TIE4** 0x00000010
- #define **REG_BITS_MCAN_TXBTIE_TIE3** 0x00000008
- #define **REG_BITS_MCAN_TXBTIE_TIE2** 0x00000004
- #define **REG_BITS_MCAN_TXBTIE_TIE1** 0x00000002
- #define **REG_BITS_MCAN_TXBTIE_TIE0** 0x00000001

- #define **REG_BITS_MCAN_TXBCIE_CFIE31** 0x80000000
- #define **REG_BITS_MCAN_TXBCIE_CFIE30** 0x40000000
- #define **REG_BITS_MCAN_TXBCIE_CFIE29** 0x20000000
- #define **REG_BITS_MCAN_TXBCIE_CFIE28** 0x10000000
- #define **REG_BITS_MCAN_TXBCIE_CFIE27** 0x08000000
- #define **REG_BITS_MCAN_TXBCIE_CFIE26** 0x04000000
- #define **REG_BITS_MCAN_TXBCIE_CFIE25** 0x02000000
- #define **REG_BITS_MCAN_TXBCIE_CFIE24** 0x01000000
- #define **REG_BITS_MCAN_TXBCIE_CFIE23** 0x00800000
- #define **REG_BITS_MCAN_TXBCIE_CFIE22** 0x00400000
- #define **REG_BITS_MCAN_TXBCIE_CFIE21** 0x00200000
- #define **REG_BITS_MCAN_TXBCIE_CFIE20** 0x00100000
- #define **REG_BITS_MCAN_TXBCIE_CFIE19** 0x00080000
- #define **REG_BITS_MCAN_TXBCIE_CFIE18** 0x00040000
- #define **REG_BITS_MCAN_TXBCIE_CFIE17** 0x00020000
- #define **REG_BITS_MCAN_TXBCIE_CFIE16** 0x00010000
- #define **REG_BITS_MCAN_TXBCIE_CFIE15** 0x00008000
- #define **REG_BITS_MCAN_TXBCIE_CFIE14** 0x00004000
- #define **REG_BITS_MCAN_TXBCIE_CFIE13** 0x00002000
- #define **REG_BITS_MCAN_TXBCIE_CFIE12** 0x00001000
- #define **REG_BITS_MCAN_TXBCIE_CFIE11** 0x00000800
- #define **REG_BITS_MCAN_TXBCIE_CFIE10** 0x00000400
- #define **REG_BITS_MCAN_TXBCIE_CFIE9** 0x00000200
- #define **REG_BITS_MCAN_TXBCIE_CFIE8** 0x00000100
- #define **REG_BITS_MCAN_TXBCIE_CFIE7** 0x00000080
- #define **REG_BITS_MCAN_TXBCIE_CFIE6** 0x00000040
- #define **REG_BITS_MCAN_TXBCIE_CFIE5** 0x00000020
- #define **REG_BITS_MCAN_TXBCIE_CFIE4** 0x00000010
- #define **REG_BITS_MCAN_TXBCIE_CFIE3** 0x00000008
- #define **REG_BITS_MCAN_TXBCIE_CFIE2** 0x00000004
- #define **REG_BITS_MCAN_TXBCIE_CFIE1** 0x00000002
- #define **REG_BITS_MCAN_TXBCIE_CFIE0** 0x00000001
- #define **REG_BITS_DEVICE_MODE_WAKE_PIN_MASK** 0xC0000000
- #define **REG_BITS_DEVICE_MODE_WAKE_PIN_DIS** 0x00000000
- #define **REG_BITS_DEVICE_MODE_WAKE_PIN_RISING** 0x40000000
- #define **REG_BITS_DEVICE_MODE_WAKE_PIN_FALLING** 0x80000000
- #define **REG_BITS_DEVICE_MODE_WAKE_PIN_BOTHEDGES** 0xC0000000
- #define **REG_BITS_DEVICE_MODE_WD_TIMER_MASK** 0x30000000
- #define **REG_BITS_DEVICE_MODE_WD_TIMER_60MS** 0x00000000
- #define **REG_BITS_DEVICE_MODE_WD_TIMER_600MS** 0x10000000
- #define **REG_BITS_DEVICE_MODE_WD_TIMER_3S** 0x20000000
- #define **REG_BITS_DEVICE_MODE_WD_TIMER_6S** 0x30000000
- #define **REG_BITS_DEVICE_MODE_WD_CLK_MASK** 0x08000000
- #define **REG_BITS_DEVICE_MODE_WD_CLK_20MHZ** 0x00000000
- #define **REG_BITS_DEVICE_MODE_WD_CLK_40MHZ** 0x08000000
- #define **REG_BITS_DEVICE_MODE_GPO2_MASK** 0x00C00000
- #define **REG_BITS_DEVICE_MODE_GPO2_CAN_FAULT** 0x00000000
- #define **REG_BITS_DEVICE_MODE_GPO2_MCAN_INT0** 0x00400000
- #define **REG_BITS_DEVICE_MODE_GPO2_WDT** 0x00800000
- #define **REG_BITS_DEVICE_MODE_GPO2_NINT** 0x00C00000
- #define **REG_BITS_DEVICE_MODE_TESTMODE_ENMASK** 0x00200000
- #define **REG_BITS_DEVICE_MODE_TESTMODE_EN** 0x00200000
- #define **REG_BITS_DEVICE_MODE_TESTMODE_DIS** 0x00000000
- #define **REG_BITS_DEVICE_MODE_NWKRQ_VOLT_MASK** 0x00080000
- #define **REG_BITS_DEVICE_MODE_NWKRQ_VOLT_INTERNAL** 0x00000000
- #define **REG_BITS_DEVICE_MODE_NWKRQ_VOLT_VIO** 0x00080000
- #define **REG_BITS_DEVICE_MODE_WDT_RESET_BIT** 0x00040000

- #define **REG_BITS_DEVICE_MODE_WDT_ACTION_MASK** 0x00020000
- #define **REG_BITS_DEVICE_MODE_WDT_ACTION_INT** 0x00000000
- #define **REG_BITS_DEVICE_MODE_WDT_ACTION_INH_PULSE** 0x00010000
- #define **REG_BITS_DEVICE_MODE_WDT_ACTION_WDT_PULSE** 0x00020000
- #define **REG_BITS_DEVICE_MODE_GPO1_MODE_MASK** 0x0000C000
- #define **REG_BITS_DEVICE_MODE_GPO1_MODE_GPO** 0x00000000
- #define **REG_BITS_DEVICE_MODE_GPO1_MODE_CLKOUT** 0x00004000
- #define **REG_BITS_DEVICE_MODE_GPO1_MODE_GPI** 0x00008000
- #define **REG_BITS_DEVICE_MODE_FAIL_SAFE_MASK** 0x00002000
- #define **REG_BITS_DEVICE_MODE_FAIL_SAFE_EN** 0x00002000
- #define **REG_BITS_DEVICE_MODE_FAIL_SAFE_DIS** 0x00000000
- #define **REG_BITS_DEVICE_MODE_CLKOUT_MASK** 0x00001000
- #define **REG_BITS_DEVICE_MODE_CLKOUT_DIV1** 0x00000000
- #define **REG_BITS_DEVICE_MODE_CLKOUT_DIV2** 0x00001000
- #define **REG_BITS_DEVICE_MODE_GPO1_FUNC_MASK** 0x00000C00
- #define **REG_BITS_DEVICE_MODE_GPO1_FUNC_SPI_INT** 0x00000000
- #define **REG_BITS_DEVICE_MODE_GPO1_FUNC_MCAN_INT1** 0x00000400
- #define **REG_BITS_DEVICE_MODE_GPO1_FUNC_UVLO_THERM** 0x00000800
- #define **REG_BITS_DEVICE_MODE_INH_MASK** 0x00000200
- #define **REG_BITS_DEVICE_MODE_INH_DIS** 0x00000200
- #define **REG_BITS_DEVICE_MODE_INH_EN** 0x00000000
- #define **REG_BITS_DEVICE_MODE_NWKRQ_CONFIG_MASK** 0x00000100
- #define **REG_BITS_DEVICE_MODE_NWKRQ_CONFIG_INH** 0x00000000
- #define **REG_BITS_DEVICE_MODE_NWKRQ_CONFIG_WKRQ** 0x00000100
- #define **REG_BITS_DEVICE_MODE_DEVICEMODE_MASK** 0x000000C0
- #define **REG_BITS_DEVICE_MODE_DEVICEMODE_SLEEP** 0x00000000
- #define **REG_BITS_DEVICE_MODE_DEVICEMODE_STANDBY** 0x00000040
- #define **REG_BITS_DEVICE_MODE_DEVICEMODE_NORMAL** 0x00000080
- #define **REG_BITS_DEVICE_MODE_WDT_MASK** 0x00000008
- #define **REG_BITS_DEVICE_MODE_WDT_EN** 0x00000008
- #define **REG_BITS_DEVICE_MODE_WDT_DIS** 0x00000000
- #define **REG_BITS_DEVICE_MODE_DEVICE_RESET** 0x00000004
- #define **REG_BITS_DEVICE_MODE_SWE_MASK** 0x00000002
- #define **REG_BITS_DEVICE_MODE_SWE_DIS** 0x00000002
- #define **REG_BITS_DEVICE_MODE_SWE_EN** 0x00000000
- #define **REG_BITS_DEVICE_MODE_TESTMODE_MASK** 0x00000001
- #define **REG_BITS_DEVICE_MODE_TESTMODE_PHY** 0x00000000
- #define **REG_BITS_DEVICE_MODE_TESTMODE_CONTROLLER** 0x00000001
- #define **REG_BITS_DEVICE_IR_CANBUSNOM** 0x80000000
- #define **REG_BITS_DEVICE_IR_CANBUSTERMOPEN** 0x40000000
- #define **REG_BITS_DEVICE_IR_CANHCANL** 0x20000000
- #define **REG_BITS_DEVICE_IR_CANHBAT** 0x10000000
- #define **REG_BITS_DEVICE_IR_CANLGND** 0x08000000
- #define **REG_BITS_DEVICE_IR_CANBUSOPEN** 0x04000000
- #define **REG_BITS_DEVICE_IR_CANBUSGND** 0x02000000
- #define **REG_BITS_DEVICE_IR_CANBUSBAT** 0x01000000
- #define **REG_BITS_DEVICE_IR_UVSUP** 0x00400000
- #define **REG_BITS_DEVICE_IR_UVIO** 0x00200000
- #define **REG_BITS_DEVICE_IR_PWRON** 0x00100000
- #define **REG_BITS_DEVICE_IR_TSD** 0x00080000
- #define **REG_BITS_DEVICE_IR_WDTO** 0x00040000
- #define **REG_BITS_DEVICE_IR_ECCERR** 0x00010000
- #define **REG_BITS_DEVICE_IR_CANINT** 0x00008000
- #define **REG_BITS_DEVICE_IR_LWU** 0x00004000
- #define **REG_BITS_DEVICE_IR_WKERR** 0x00002000
- #define **REG_BITS_DEVICE_IR_FRAME_OVF** 0x00001000
- #define **REG_BITS_DEVICE_IR_CANSLNT** 0x00000400

- #define **REG_BITS_DEVICE_IR_CANDOM** 0x00000100
- #define **REG_BITS_DEVICE_IR_GLOBALERR** 0x00000080
- #define **REG_BITS_DEVICE_IR_nWKRQ** 0x00000040
- #define **REG_BITS_DEVICE_IR_CANERR** 0x00000020
- #define **REG_BITS_DEVICE_IR_CANBUSFAULT** 0x00000010
- #define **REG_BITS_DEVICE_IR_SPIERR** 0x00000008
- #define **REG_BITS_DEVICE_IR_SWERR** 0x00000004
- #define **REG_BITS_DEVICE_IR_M_CAN_INT** 0x00000002
- #define **REG_BITS_DEVICE_IR_VTWD** 0x00000001
- #define **REG_BITS_DEVICE_IE_CANBUSNOM** 0x80000000
- #define **REG_BITS_DEVICE_IE_CANBUSTERMOPEN** 0x40000000
- #define **REG_BITS_DEVICE_IE_CANHCANL** 0x20000000
- #define **REG_BITS_DEVICE_IE_CANHBAT** 0x10000000
- #define **REG_BITS_DEVICE_IE_CANLGND** 0x08000000
- #define **REG_BITS_DEVICE_IE_CANBUSOPEN** 0x04000000
- #define **REG_BITS_DEVICE_IE_CANBUSGND** 0x02000000
- #define **REG_BITS_DEVICE_IE_CANBUSBAT** 0x01000000
- #define **REG_BITS_DEVICE_IE_UVCCOUT** 0x00800000
- #define **REG_BITS_DEVICE_IE_UVSUP** 0x00400000
- #define **REG_BITS_DEVICE_IE_UVIO** 0x00200000
- #define **REG_BITS_DEVICE_IE_PWRON** 0x00100000
- #define **REG_BITS_DEVICE_IE_TSD** 0x00080000
- #define **REG_BITS_DEVICE_IE_WDTO** 0x00040000
- #define **REG_BITS_DEVICE_IE_ECCERR** 0x00010000
- #define **REG_BITS_DEVICE_IE_CANINT** 0x00008000
- #define **REG_BITS_DEVICE_IE_LWU** 0x00004000
- #define **REG_BITS_DEVICE_IE_WKERR** 0x00002000
- #define **REG_BITS_DEVICE_IE_FRAME_OVF** 0x00001000
- #define **REG_BITS_DEVICE_IE_CANSLNT** 0x00000400
- #define **REG_BITS_DEVICE_IE_CANDOM** 0x00000100
- #define **REG_BITS_DEVICE_IE_MASK** 0xFF69D700

Detailed Description

This file contains the register definitions for the TCAN4x5x Family.

There are a few different define domains:

- REG_MCAN_x: MCAN register address defines
- MCAN_DLC_x: DLC values for the RX and TX FIFO element defines
- REG_SPI_x : SPI Controller register address defines
- REG_DEV_x : TCAN4x5x Device-specific register address defines
- REG_BITS_x: Register bit defines in a similar manner as above. EX: REG_BITS_MCAN_CCCR_INIT is the hex value corresponding to the REG_MCAN_CCCR register's INIT bit

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Author

Texas Instruments

Macro Definition Documentation

#define MCAN_DLC_0B 0x00000000

#define MCAN_DLC_12B 0x00000009

#define MCAN_DLC_16B 0x0000000A

#define MCAN_DLC_1B 0x00000001

#define MCAN_DLC_20B 0x0000000B

#define MCAN_DLC_24B 0x0000000C

#define MCAN_DLC_2B 0x00000002

#define MCAN_DLC_32B 0x0000000D

#define MCAN_DLC_3B 0x00000003

#define MCAN_DLC_48B 0x0000000E

#define MCAN_DLC_4B 0x00000004

#define MCAN_DLC_5B 0x00000005

#define MCAN_DLC_64B 0x0000000F

#define MCAN_DLC_6B 0x00000006

#define MCAN_DLC_7B 0x00000007

#define MCAN_DLC_8B 0x00000008

#define MRAM_SIZE 2048

#define REG_BITS_DEVICE_IE_CANBUSBAT 0x01000000

#define REG_BITS_DEVICE_IE_CANBUSGND 0x02000000

#define REG_BITS_DEVICE_IE_CANBUSNOM 0x80000000

#define REG_BITS_DEVICE_IE_CANBUSOPEN 0x04000000

#define REG_BITS_DEVICE_IE_CANBUSTERMOPEN 0x40000000

#define REG_BITS_DEVICE_IE_CANDOM 0x00000100

#define REG_BITS_DEVICE_IE_CANHBAT 0x10000000

#define REG_BITS_DEVICE_IE_CANHCANL 0x20000000

#define REG_BITS_DEVICE_IE_CANINT 0x00008000

#define REG_BITS_DEVICE_IE_CANLGND 0x08000000

#define REG_BITS_DEVICE_IE_CANSLNT 0x00000400

#define REG_BITS_DEVICE_IE_ECCERR 0x00010000

#define REG_BITS_DEVICE_IE_FRAME_OVF 0x00001000

#define REG_BITS_DEVICE_IE_LWU 0x00004000

#define REG_BITS_DEVICE_IE_MASK 0xFF69D700

#define REG_BITS_DEVICE_IE_PWRON 0x00100000

#define REG_BITS_DEVICE_IE_TSD 0x00080000

#define REG_BITS_DEVICE_IE_UVCCOUT 0x00800000

#define REG_BITS_DEVICE_IE_UVIO 0x00200000

#define REG_BITS_DEVICE_IE_UVSUP 0x00400000

#define REG_BITS_DEVICE_IE_WDTO 0x00040000

#define REG_BITS_DEVICE_IE_WKERR 0x00002000

#define REG_BITS_DEVICE_IR_CANBUSBAT 0x01000000

#define REG_BITS_DEVICE_IR_CANBUSFAULT 0x00000010

#define REG_BITS_DEVICE_IR_CANBUSGND 0x02000000

#define REG_BITS_DEVICE_IR_CANBUSNOM 0x80000000

#define REG_BITS_DEVICE_IR_CANBUSOPEN 0x04000000

#define REG_BITS_DEVICE_IR_CANBUSTERMOPEN 0x40000000

#define REG_BITS_DEVICE_IR_CANDOM 0x00000100

#define REG_BITS_DEVICE_IR_CANERR 0x00000020

#define REG_BITS_DEVICE_IR_CANHBAT 0x10000000

#define REG_BITS_DEVICE_IR_CANHCANL 0x20000000

#define REG_BITS_DEVICE_IR_CANINT 0x00008000

#define REG_BITS_DEVICE_IR_CANLGND 0x08000000

#define REG_BITS_DEVICE_IR_CANSLNT 0x00000400

#define REG_BITS_DEVICE_IR_ECCERR 0x00010000

#define REG_BITS_DEVICE_IR_FRAME_OVF 0x00001000

#define REG_BITS_DEVICE_IR_GLOBALERR 0x00000080

#define REG_BITS_DEVICE_IR_LWU 0x00004000

#define REG_BITS_DEVICE_IR_M_CAN_INT 0x00000002

#define REG_BITS_DEVICE_IR_nWKRQ 0x00000040

#define REG_BITS_DEVICE_IR_PWRON 0x00100000

#define REG_BITS_DEVICE_IR_SPIERR 0x00000008

#define REG_BITS_DEVICE_IR_SWERR 0x00000004

#define REG_BITS_DEVICE_IR_TSD 0x00080000

#define REG_BITS_DEVICE_IR_UVIO 0x00200000

#define REG_BITS_DEVICE_IR_UVSUP 0x00400000

#define REG_BITS_DEVICE_IR_VTWD 0x00000001

#define REG_BITS_DEVICE_IR_WDTO 0x00040000

#define REG_BITS_DEVICE_IR_WKERR 0x00002000

#define REG_BITS_DEVICE_MODE_CLKOUT_DIV1 0x00000000

#define REG_BITS_DEVICE_MODE_CLKOUT_DIV2 0x00001000

#define REG_BITS_DEVICE_MODE_CLKOUT_MASK 0x00001000

#define REG_BITS_DEVICE_MODE_DEVICE_RESET 0x00000004

#define REG_BITS_DEVICE_MODE_DEVICEMODE_MASK 0x000000C0

#define REG_BITS_DEVICE_MODE_DEVICEMODE_NORMAL 0x00000080

#define REG_BITS_DEVICE_MODE_DEVICEMODE_SLEEP 0x00000000

#define REG_BITS_DEVICE_MODE_DEVICEMODE_STANDBY 0x00000040

#define REG_BITS_DEVICE_MODE_FAIL_SAFE_DIS 0x00000000

#define REG_BITS_DEVICE_MODE_FAIL_SAFE_EN 0x00002000

#define REG_BITS_DEVICE_MODE_FAIL_SAFE_MASK 0x00002000

#define REG_BITS_DEVICE_MODE_GPO1_FUNC_MASK 0x00000C00

#define REG_BITS_DEVICE_MODE_GPO1_FUNC_MCAN_INT1 0x00000400

#define REG_BITS_DEVICE_MODE_GPO1_FUNC_SPI_INT 0x00000000

#define REG_BITS_DEVICE_MODE_GPO1_FUNC_UVLO_THERM 0x00000800

#define REG_BITS_DEVICE_MODE_GPO1_MODE_CLKOUT 0x00004000

#define REG_BITS_DEVICE_MODE_GPO1_MODE_GPI 0x00008000

#define REG_BITS_DEVICE_MODE_GPO1_MODE_GPO 0x00000000

#define REG_BITS_DEVICE_MODE_GPO1_MODE_MASK 0x0000C000

#define REG_BITS_DEVICE_MODE_GPO2_CAN_FAULT 0x00000000

#define REG_BITS_DEVICE_MODE_GPO2_MASK 0x00C00000

#define REG_BITS_DEVICE_MODE_GPO2_MCAN_INT0 0x00400000

#define REG_BITS_DEVICE_MODE_GPO2_NINT 0x00C00000

#define REG_BITS_DEVICE_MODE_GPO2_WDT 0x00800000

#define REG_BITS_DEVICE_MODE_INH_DIS 0x00000200

#define REG_BITS_DEVICE_MODE_INH_EN 0x00000000

#define REG_BITS_DEVICE_MODE_INH_MASK 0x00000200

#define REG_BITS_DEVICE_MODE_NWKRQ_CONFIG_INH 0x00000000

#define REG_BITS_DEVICE_MODE_NWKRQ_CONFIG_MASK 0x00000100

#define REG_BITS_DEVICE_MODE_NWKRQ_CONFIG_WKRQ 0x00000100

#define REG_BITS_DEVICE_MODE_NWKRQ_VOLT_INTERNAL 0x00000000

#define REG_BITS_DEVICE_MODE_NWKRQ_VOLT_MASK 0x00080000

#define REG_BITS_DEVICE_MODE_NWKRQ_VOLT_VIO 0x00080000

#define REG_BITS_DEVICE_MODE_SWE_DIS 0x00000002

#define REG_BITS_DEVICE_MODE_SWE_EN 0x00000000

#define REG_BITS_DEVICE_MODE_SWE_MASK 0x00000002

#define REG_BITS_DEVICE_MODE_TESTMODE_CONTROLLER 0x00000001

#define REG_BITS_DEVICE_MODE_TESTMODE_DIS 0x00000000

#define REG_BITS_DEVICE_MODE_TESTMODE_EN 0x00200000

#define REG_BITS_DEVICE_MODE_TESTMODE_ENMASK 0x00200000

#define REG_BITS_DEVICE_MODE_TESTMODE_MASK 0x00000001

#define REG_BITS_DEVICE_MODE_TESTMODE_PHY 0x00000000

#define REG_BITS_DEVICE_MODE_WAKE_PIN_BOTHEDGES 0xC0000000

#define REG_BITS_DEVICE_MODE_WAKE_PIN_DIS 0x00000000

#define REG_BITS_DEVICE_MODE_WAKE_PIN_FALLING 0x80000000

#define REG_BITS_DEVICE_MODE_WAKE_PIN_MASK 0xC0000000

#define REG_BITS_DEVICE_MODE_WAKE_PIN_RISING 0x40000000

#define REG_BITS_DEVICE_MODE_WD_CLK_20MHZ 0x00000000

#define REG_BITS_DEVICE_MODE_WD_CLK_40MHZ 0x08000000

#define REG_BITS_DEVICE_MODE_WD_CLK_MASK 0x08000000

#define REG_BITS_DEVICE_MODE_WD_TIMER_3S 0x20000000

#define REG_BITS_DEVICE_MODE_WD_TIMER_600MS 0x10000000

#define REG_BITS_DEVICE_MODE_WD_TIMER_60MS 0x00000000

#define REG_BITS_DEVICE_MODE_WD_TIMER_6S 0x30000000

#define REG_BITS_DEVICE_MODE_WD_TIMER_MASK 0x30000000

#define REG_BITS_DEVICE_MODE_WDT_ACTION_INH_PULSE 0x00010000

#define REG_BITS_DEVICE_MODE_WDT_ACTION_INT 0x00000000

#define REG_BITS_DEVICE_MODE_WDT_ACTION_MASK 0x00020000

#define REG_BITS_DEVICE_MODE_WDT_ACTION_WDT_PULSE 0x00020000

#define REG_BITS_DEVICE_MODE_WDT_DIS 0x00000000

#define REG_BITS_DEVICE_MODE_WDT_EN 0x00000008

#define REG_BITS_DEVICE_MODE_WDT_MASK 0x00000008

#define REG_BITS_DEVICE_MODE_WDT_RESET_BIT 0x00040000

#define REG_BITS_MCAN_CCCR_ASM 0x00000004

#define REG_BITS_MCAN_CCCR_BRSE 0x00000200

#define REG_BITS_MCAN_CCCR_CCE 0x00000002

#define REG_BITS_MCAN_CCCR_CSA 0x00000008

#define REG_BITS_MCAN_CCCR_CSR 0x00000010

#define REG_BITS_MCAN_CCCR_DAR_DIS 0x00000040

#define REG_BITS_MCAN_CCCR_EFBI 0x00002000

#define REG_BITS_MCAN_CCCR_FDOE 0x00000100

#define REG_BITS_MCAN_CCCR_INIT 0x00000001

#define REG_BITS_MCAN_CCCR_MON 0x00000020

#define REG_BITS_MCAN_CCCR_NISO_BOSCH 0x00008000

#define REG_BITS_MCAN_CCCR_NISO_ISO 0x00000000

#define REG_BITS_MCAN_CCCR_PXHD_DIS 0x00001000

#define REG_BITS_MCAN_CCCR_RESERVED_MASK 0xFFFF0C00

#define REG_BITS_MCAN_CCCR_TEST 0x00000080

#define REG_BITS_MCAN_CCCR_TXP 0x00004000

#define REG_BITS_MCAN_DBTP_TDC_EN 0x00800000

#define REG_BITS_MCAN_GFC_ANFE_FIFO0 0x00000000

#define REG_BITS_MCAN_GFC_ANFE_FIFO1 0x00000004

#define REG_BITS_MCAN_GFC_ANFS_FIFO0 0x00000000

#define REG_BITS_MCAN_GFC_ANFS_FIFO1 0x00000010

#define REG_BITS_MCAN_GFC_RRFE 0x00000001

#define REG_BITS_MCAN_GFC_RRFS 0x00000002

#define REG_BITS_MCAN_IE_ARAE 0x20000000

#define REG_BITS_MCAN_IE_ARAL 0x20000000


```
#define REG_BITS_MCAN_IE_BECE   0x00100000

#define REG_BITS_MCAN_IE_BECL   0x00100000

#define REG_BITS_MCAN_IE_BEUE   0x00200000

#define REG_BITS_MCAN_IE_BEUL   0x00200000

#define REG_BITS_MCAN_IE_BOE   0x02000000

#define REG_BITS_MCAN_IE_BOL   0x02000000

#define REG_BITS_MCAN_IE_DRXE   0x00080000

#define REG_BITS_MCAN_IE_DRXL   0x00080000

#define REG_BITS_MCAN_IE_ELOE   0x00400000

#define REG_BITS_MCAN_IE_ELOL   0x00400000

#define REG_BITS_MCAN_IE_EPE   0x00800000

#define REG_BITS_MCAN_IE_EPL   0x00800000

#define REG_BITS_MCAN_IE_EWE   0x01000000

#define REG_BITS_MCAN_IE_EWL   0x01000000

#define REG_BITS_MCAN_IE_HPME   0x00000100

#define REG_BITS_MCAN_IE_HPML   0x00000100

#define REG_BITS_MCAN_IE_MRAFE   0x00020000

#define REG_BITS_MCAN_IE_MRAFL   0x00020000

#define REG_BITS_MCAN_IE_PEAE   0x08000000

#define REG_BITS_MCAN_IE_PEAL   0x08000000

#define REG_BITS_MCAN_IE_PEDE   0x10000000

#define REG_BITS_MCAN_IE_PEDL   0x10000000

#define REG_BITS_MCAN_IE_RF0FE   0x00000004

#define REG_BITS_MCAN_IE_RF0FL   0x00000004

#define REG_BITS_MCAN_IE_RF0LE   0x00000008

#define REG_BITS_MCAN_IE_RF0LL   0x00000008
```


#define REG_BITS_MCAN_IE_RF0NE 0x00000001

#define REG_BITS_MCAN_IE_RF0NL 0x00000001

#define REG_BITS_MCAN_IE_RF0WE 0x00000002

#define REG_BITS_MCAN_IE_RF0WL 0x00000002

#define REG_BITS_MCAN_IE_RF1FE 0x00000040

#define REG_BITS_MCAN_IE_RF1FL 0x00000040

#define REG_BITS_MCAN_IE_RF1LE 0x00000080

#define REG_BITS_MCAN_IE_RF1LL 0x00000080

#define REG_BITS_MCAN_IE_RF1NE 0x00000010

#define REG_BITS_MCAN_IE_RF1NL 0x00000010

#define REG_BITS_MCAN_IE_RF1WE 0x00000020

#define REG_BITS_MCAN_IE_RF1WL 0x00000020

#define REG_BITS_MCAN_IE_TCE 0x00000200

#define REG_BITS_MCAN_IE_TCFE 0x00000400

#define REG_BITS_MCAN_IE_TCFL 0x00000400

#define REG_BITS_MCAN_IE_TCL 0x00000200

#define REG_BITS_MCAN_IE_TEFFE 0x00004000

#define REG_BITS_MCAN_IE_TEFFL 0x00004000

#define REG_BITS_MCAN_IE_TEFLE 0x00008000

#define REG_BITS_MCAN_IE_TEFLL 0x00008000

#define REG_BITS_MCAN_IE_TEFNE 0x00001000

#define REG_BITS_MCAN_IE_TEFNL 0x00001000

#define REG_BITS_MCAN_IE_TEFWE 0x00002000

#define REG_BITS_MCAN_IE_TEFWL 0x00002000

#define REG_BITS_MCAN_IE_TFEE 0x00000800

#define REG_BITS_MCAN_IE_TFEL 0x00000800


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#define REG_BITS_MCAN_IE_TOOE   0x00040000

#define REG_BITS_MCAN_IE_TOOL   0x00040000

#define REG_BITS_MCAN_IE_TSWE   0x00010000

#define REG_BITS_MCAN_IE_TSWL   0x00010000

#define REG_BITS_MCAN_IE_WDIE   0x04000000

#define REG_BITS_MCAN_IE_WDIL   0x04000000

#define REG_BITS_MCAN_ILE_EINT0   0x00000001

#define REG_BITS_MCAN_ILE_EINT1   0x00000002

#define REG_BITS_MCAN_IR_ARA   0x20000000

#define REG_BITS_MCAN_IR_BEC   0x00100000

#define REG_BITS_MCAN_IR_BEU   0x00200000

#define REG_BITS_MCAN_IR_BO   0x02000000

#define REG_BITS_MCAN_IR_DRX   0x00080000

#define REG_BITS_MCAN_IR_ELO   0x00400000

#define REG_BITS_MCAN_IR_EP   0x00800000

#define REG_BITS_MCAN_IR_EW   0x01000000

#define REG_BITS_MCAN_IR_HPM   0x00000100

#define REG_BITS_MCAN_IR_MRAF   0x00020000

#define REG_BITS_MCAN_IR_PEA   0x08000000

#define REG_BITS_MCAN_IR_PED   0x10000000

#define REG_BITS_MCAN_IR_RF0F   0x00000004

#define REG_BITS_MCAN_IR_RF0L   0x00000008

#define REG_BITS_MCAN_IR_RF0N   0x00000001

#define REG_BITS_MCAN_IR_RF0W   0x00000002

#define REG_BITS_MCAN_IR_RF1F   0x00000040

#define REG_BITS_MCAN_IR_RF1L   0x00000080
```



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#define REG_BITS_MCAN_IR_RF1N   0x00000010

#define REG_BITS_MCAN_IR_RF1W   0x00000020

#define REG_BITS_MCAN_IR_TC   0x00000200

#define REG_BITS_MCAN_IR_TCF   0x00000400

#define REG_BITS_MCAN_IR_TEFF   0x00004000

#define REG_BITS_MCAN_IR_TEFL   0x00008000

#define REG_BITS_MCAN_IR_TEFN   0x00001000

#define REG_BITS_MCAN_IR_TEFW   0x00002000

#define REG_BITS_MCAN_IR_TFE   0x00000800

#define REG_BITS_MCAN_IR_TOO   0x00040000

#define REG_BITS_MCAN_IR_TSW   0x00010000

#define REG_BITS_MCAN_IR_WDI   0x04000000

#define REG_BITS_MCAN_RXESC_F0DS_12B   0x00000001

#define REG_BITS_MCAN_RXESC_F0DS_16B   0x00000002

#define REG_BITS_MCAN_RXESC_F0DS_20B   0x00000003

#define REG_BITS_MCAN_RXESC_F0DS_24B   0x00000004

#define REG_BITS_MCAN_RXESC_F0DS_32B   0x00000005

#define REG_BITS_MCAN_RXESC_F0DS_48B   0x00000006

#define REG_BITS_MCAN_RXESC_F0DS_64B   0x00000007

#define REG_BITS_MCAN_RXESC_F0DS_8B   0x00000000

#define REG_BITS_MCAN_RXESC_F1DS_12B   0x00000010

#define REG_BITS_MCAN_RXESC_F1DS_16B   0x00000020

#define REG_BITS_MCAN_RXESC_F1DS_20B   0x00000030

#define REG_BITS_MCAN_RXESC_F1DS_24B   0x00000040

#define REG_BITS_MCAN_RXESC_F1DS_32B   0x00000050

#define REG_BITS_MCAN_RXESC_F1DS_48B   0x00000060
```



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#define REG_BITS_MCAN_RXESC_F1DS_64B   0x00000070

#define REG_BITS_MCAN_RXESC_F1DS_8B   0x00000000

#define REG_BITS_MCAN_RXESC_RBDS_12B   0x00000100

#define REG_BITS_MCAN_RXESC_RBDS_16B   0x00000200

#define REG_BITS_MCAN_RXESC_RBDS_20B   0x00000300

#define REG_BITS_MCAN_RXESC_RBDS_24B   0x00000400

#define REG_BITS_MCAN_RXESC_RBDS_32B   0x00000500

#define REG_BITS_MCAN_RXESC_RBDS_48B   0x00000600

#define REG_BITS_MCAN_RXESC_RBDS_64B   0x00000700

#define REG_BITS_MCAN_RXESC_RBDS_8B   0x00000000

#define REG_BITS_MCAN_RXF0C_F0OM_OVERWRITE   0x80000000

#define REG_BITS_MCAN_TEST_LOOP_BACK   0x00000010

#define REG_BITS_MCAN_TEST_RX_DOM   0x00000000

#define REG_BITS_MCAN_TEST_RX_REC   0x00000080

#define REG_BITS_MCAN_TEST_TX_DOM   0x00000040

#define REG_BITS_MCAN_TEST_TX_REC   0x00000060

#define REG_BITS_MCAN_TEST_TX_SP   0x00000020

#define REG_BITS_MCAN_TSCC_COUNTER_ALWAYS_0   0x00000000

#define REG_BITS_MCAN_TSCC_COUNTER_EXTERNAL   0x00000002

#define REG_BITS_MCAN_TSCC_COUNTER_USE_TCP   0x00000001

#define REG_BITS_MCAN_TSCC_PRESCALER_MASK   0x000F0000

#define REG_BITS_MCAN_TXBAR_AR0   0x00000001

#define REG_BITS_MCAN_TXBAR_AR1   0x00000002

#define REG_BITS_MCAN_TXBAR_AR10   0x00000400

#define REG_BITS_MCAN_TXBAR_AR11   0x00000800

#define REG_BITS_MCAN_TXBAR_AR12   0x00001000
```


#define REG_BITS_MCAN_TXBAR_AR13 0x00002000

#define REG_BITS_MCAN_TXBAR_AR14 0x00004000

#define REG_BITS_MCAN_TXBAR_AR15 0x00008000

#define REG_BITS_MCAN_TXBAR_AR16 0x00010000

#define REG_BITS_MCAN_TXBAR_AR17 0x00020000

#define REG_BITS_MCAN_TXBAR_AR18 0x00040000

#define REG_BITS_MCAN_TXBAR_AR19 0x00080000

#define REG_BITS_MCAN_TXBAR_AR2 0x00000004

#define REG_BITS_MCAN_TXBAR_AR20 0x00100000

#define REG_BITS_MCAN_TXBAR_AR21 0x00200000

#define REG_BITS_MCAN_TXBAR_AR22 0x00400000

#define REG_BITS_MCAN_TXBAR_AR23 0x00800000

#define REG_BITS_MCAN_TXBAR_AR24 0x01000000

#define REG_BITS_MCAN_TXBAR_AR25 0x02000000

#define REG_BITS_MCAN_TXBAR_AR26 0x04000000

#define REG_BITS_MCAN_TXBAR_AR27 0x08000000

#define REG_BITS_MCAN_TXBAR_AR28 0x10000000

#define REG_BITS_MCAN_TXBAR_AR29 0x20000000

#define REG_BITS_MCAN_TXBAR_AR3 0x00000008

#define REG_BITS_MCAN_TXBAR_AR30 0x40000000

#define REG_BITS_MCAN_TXBAR_AR31 0x80000000

#define REG_BITS_MCAN_TXBAR_AR4 0x00000010

#define REG_BITS_MCAN_TXBAR_AR5 0x00000020

#define REG_BITS_MCAN_TXBAR_AR6 0x00000040

#define REG_BITS_MCAN_TXBAR_AR7 0x00000080

#define REG_BITS_MCAN_TXBAR_AR8 0x00000100

#define REG_BITS_MCAN_TXBAR_AR9 0x00000200

#define REG_BITS_MCAN_TXBC_TFQM 0x40000000

#define REG_BITS_MCAN_TXBCIE_CFIE0 0x00000001

#define REG_BITS_MCAN_TXBCIE_CFIE1 0x00000002

#define REG_BITS_MCAN_TXBCIE_CFIE10 0x00000400

#define REG_BITS_MCAN_TXBCIE_CFIE11 0x00000800

#define REG_BITS_MCAN_TXBCIE_CFIE12 0x00001000

#define REG_BITS_MCAN_TXBCIE_CFIE13 0x00002000

#define REG_BITS_MCAN_TXBCIE_CFIE14 0x00004000

#define REG_BITS_MCAN_TXBCIE_CFIE15 0x00008000

#define REG_BITS_MCAN_TXBCIE_CFIE16 0x00010000

#define REG_BITS_MCAN_TXBCIE_CFIE17 0x00020000

#define REG_BITS_MCAN_TXBCIE_CFIE18 0x00040000

#define REG_BITS_MCAN_TXBCIE_CFIE19 0x00080000

#define REG_BITS_MCAN_TXBCIE_CFIE2 0x00000004

#define REG_BITS_MCAN_TXBCIE_CFIE20 0x00100000

#define REG_BITS_MCAN_TXBCIE_CFIE21 0x00200000

#define REG_BITS_MCAN_TXBCIE_CFIE22 0x00400000

#define REG_BITS_MCAN_TXBCIE_CFIE23 0x00800000

#define REG_BITS_MCAN_TXBCIE_CFIE24 0x01000000

#define REG_BITS_MCAN_TXBCIE_CFIE25 0x02000000

#define REG_BITS_MCAN_TXBCIE_CFIE26 0x04000000

#define REG_BITS_MCAN_TXBCIE_CFIE27 0x08000000

#define REG_BITS_MCAN_TXBCIE_CFIE28 0x10000000

#define REG_BITS_MCAN_TXBCIE_CFIE29 0x20000000

#define REG_BITS_MCAN_TXBCIE_CFIE3 0x00000008


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#define REG_BITS_MCAN_TXBCIE_CFIE30   0x40000000

#define REG_BITS_MCAN_TXBCIE_CFIE31   0x80000000

#define REG_BITS_MCAN_TXBCIE_CFIE4   0x00000010

#define REG_BITS_MCAN_TXBCIE_CFIE5   0x00000020

#define REG_BITS_MCAN_TXBCIE_CFIE6   0x00000040

#define REG_BITS_MCAN_TXBCIE_CFIE7   0x00000080

#define REG_BITS_MCAN_TXBCIE_CFIE8   0x00000100

#define REG_BITS_MCAN_TXBCIE_CFIE9   0x00000200

#define REG_BITS_MCAN_TXBCR_CR0   0x00000001

#define REG_BITS_MCAN_TXBCR_CR1   0x00000002

#define REG_BITS_MCAN_TXBCR_CR10   0x00000400

#define REG_BITS_MCAN_TXBCR_CR11   0x00000800

#define REG_BITS_MCAN_TXBCR_CR12   0x00001000

#define REG_BITS_MCAN_TXBCR_CR13   0x00002000

#define REG_BITS_MCAN_TXBCR_CR14   0x00004000

#define REG_BITS_MCAN_TXBCR_CR15   0x00008000

#define REG_BITS_MCAN_TXBCR_CR16   0x00010000

#define REG_BITS_MCAN_TXBCR_CR17   0x00020000

#define REG_BITS_MCAN_TXBCR_CR18   0x00040000

#define REG_BITS_MCAN_TXBCR_CR19   0x00080000

#define REG_BITS_MCAN_TXBCR_CR2   0x00000004

#define REG_BITS_MCAN_TXBCR_CR20   0x00100000

#define REG_BITS_MCAN_TXBCR_CR21   0x00200000

#define REG_BITS_MCAN_TXBCR_CR22   0x00400000

#define REG_BITS_MCAN_TXBCR_CR23   0x00800000

#define REG_BITS_MCAN_TXBCR_CR24   0x01000000
```



```
#define REG_BITS_MCAN_TXBCR_CR25   0x02000000
#define REG_BITS_MCAN_TXBCR_CR26   0x04000000
#define REG_BITS_MCAN_TXBCR_CR27   0x08000000
#define REG_BITS_MCAN_TXBCR_CR28   0x10000000
#define REG_BITS_MCAN_TXBCR_CR29   0x20000000
#define REG_BITS_MCAN_TXBCR_CR3   0x00000008
#define REG_BITS_MCAN_TXBCR_CR30   0x40000000
#define REG_BITS_MCAN_TXBCR_CR31   0x80000000
#define REG_BITS_MCAN_TXBCR_CR4   0x00000010
#define REG_BITS_MCAN_TXBCR_CR5   0x00000020
#define REG_BITS_MCAN_TXBCR_CR6   0x00000040
#define REG_BITS_MCAN_TXBCR_CR7   0x00000080
#define REG_BITS_MCAN_TXBCR_CR8   0x00000100
#define REG_BITS_MCAN_TXBCR_CR9   0x00000200
#define REG_BITS_MCAN_TXBTIE_TIE0   0x00000001
#define REG_BITS_MCAN_TXBTIE_TIE1   0x00000002
#define REG_BITS_MCAN_TXBTIE_TIE10   0x00000400
#define REG_BITS_MCAN_TXBTIE_TIE11   0x00000800
#define REG_BITS_MCAN_TXBTIE_TIE12   0x00001000
#define REG_BITS_MCAN_TXBTIE_TIE13   0x00002000
#define REG_BITS_MCAN_TXBTIE_TIE14   0x00004000
#define REG_BITS_MCAN_TXBTIE_TIE15   0x00008000
#define REG_BITS_MCAN_TXBTIE_TIE16   0x00010000
#define REG_BITS_MCAN_TXBTIE_TIE17   0x00020000
#define REG_BITS_MCAN_TXBTIE_TIE18   0x00040000
#define REG_BITS_MCAN_TXBTIE_TIE19   0x00080000
```



```
#define REG_BITS_MCAN_TXBTIE_TIE2   0x00000004

#define REG_BITS_MCAN_TXBTIE_TIE20   0x00100000

#define REG_BITS_MCAN_TXBTIE_TIE21   0x00200000

#define REG_BITS_MCAN_TXBTIE_TIE22   0x00400000

#define REG_BITS_MCAN_TXBTIE_TIE23   0x00800000

#define REG_BITS_MCAN_TXBTIE_TIE24   0x01000000

#define REG_BITS_MCAN_TXBTIE_TIE25   0x02000000

#define REG_BITS_MCAN_TXBTIE_TIE26   0x04000000

#define REG_BITS_MCAN_TXBTIE_TIE27   0x08000000

#define REG_BITS_MCAN_TXBTIE_TIE28   0x10000000

#define REG_BITS_MCAN_TXBTIE_TIE29   0x20000000

#define REG_BITS_MCAN_TXBTIE_TIE3   0x00000008

#define REG_BITS_MCAN_TXBTIE_TIE30   0x40000000

#define REG_BITS_MCAN_TXBTIE_TIE31   0x80000000

#define REG_BITS_MCAN_TXBTIE_TIE4   0x00000010

#define REG_BITS_MCAN_TXBTIE_TIE5   0x00000020

#define REG_BITS_MCAN_TXBTIE_TIE6   0x00000040

#define REG_BITS_MCAN_TXBTIE_TIE7   0x00000080

#define REG_BITS_MCAN_TXBTIE_TIE8   0x00000100

#define REG_BITS_MCAN_TXBTIE_TIE9   0x00000200

#define REG_BITS_MCAN_TXESC_TBDS_12   0x00000001

#define REG_BITS_MCAN_TXESC_TBDS_16   0x00000002

#define REG_BITS_MCAN_TXESC_TBDS_20   0x00000003

#define REG_BITS_MCAN_TXESC_TBDS_24   0x00000004

#define REG_BITS_MCAN_TXESC_TBDS_32   0x00000005

#define REG_BITS_MCAN_TXESC_TBDS_48   0x00000006
```


#define REG_BITS_MCAN_TXESC_TBDS_64 0x00000007

#define REG_BITS_MCAN_TXESC_TBDS_8 0x00000000

#define REG_DEV_CONFIG 0x0800

#define REG_DEV_IE 0x0830

#define REG_DEV_IR 0x0820

#define REG_DEV_MODES_AND_PINS 0x0800

#define REG_DEV_TEST_REGISTERS 0x0808

#define REG_DEV_TIMESTAMP_PRESCALER 0x0804

#define REG_MCAN 0x1000

#define REG_MCAN_CCCR 0x1018

#define REG_MCAN_CREL 0x1000

#define REG_MCAN_CUST 0x1008

#define REG_MCAN_DBTP 0x100C

#define REG_MCAN_ECR 0x1040

#define REG_MCAN_ENDN 0x1004

#define REG_MCAN_GFC 0x1080

#define REG_MCAN_HPMS 0x1094

#define REG_MCAN_IE 0x1054

#define REG_MCAN_ILE 0x105C

#define REG_MCAN_ILS 0x1058

#define REG_MCAN_IR 0x1050

#define REG_MCAN_NBTP 0x101C

#define REG_MCAN_NDAT1 0x1098

#define REG_MCAN_NDAT2 0x109C

#define REG_MCAN_PSR 0x1044

#define REG_MCAN_RWD 0x1014

#define REG_MCAN_RXBC 0x10AC

#define REG_MCAN_RXESC 0x10BC

#define REG_MCAN_RXF0A 0x10A8

#define REG_MCAN_RXF0C 0x10A0

#define REG_MCAN_RXF0S 0x10A4

#define REG_MCAN_RXF1A 0x10B8

#define REG_MCAN_RXF1C 0x10B0

#define REG_MCAN_RXF1S 0x10B4

#define REG_MCAN_SIDFC 0x1084

#define REG_MCAN_TDCR 0x1048

#define REG_MCAN_TEST 0x1010

#define REG_MCAN_TOCC 0x1028

#define REG_MCAN_TOCV 0x102C

#define REG_MCAN_TSCC 0x1020

#define REG_MCAN_TSCV 0x1024

#define REG_MCAN_TXBAR 0x10D0

#define REG_MCAN_TXBC 0x10C0

#define REG_MCAN_TXBCF 0x10DC

#define REG_MCAN_TXBCIE 0x10E4

#define REG_MCAN_TXBCR 0x10D4

#define REG_MCAN_TXBRP 0x10CC

#define REG_MCAN_TXBTIE 0x10E0

#define REG_MCAN_TXBTO 0x10D8

#define REG_MCAN_TXEFA 0x10F8

#define REG_MCAN_TXEFC 0x10F0

#define REG_MCAN_TXEFS 0x10F4

#define REG_MCAN_TXESC 0x10C8

#define REG_MCAN_TXFQS 0x10C4

#define REG_MCAN_XIDAM 0x1090

#define REG_MCAN_XIDFC 0x1088

#define REG_MRAM 0x8000

#define REG_SPI_CONFIG 0x0000

#define REG_SPI_DEVICE_ID0 0x0000

#define REG_SPI_DEVICE_ID1 0x0004

#define REG_SPI_ERROR_STATUS_MASK 0x0010

#define REG_SPI_REVISION 0x0008

#define REG_SPI_STATUS 0x000C

C:/Alphi/PCIeMiniSoftware/include/TCAN4x5x_SPI.h File Reference

This file is responsible for abstracting the lower-level microcontroller SPI read and write functions.
`#include "AlteraSpi.h"`

Macros

- #define **AHB_WRITE_OPCODE** 0x61
- #define **AHB_READ_OPCODE** 0x41

Detailed Description

This file is responsible for abstracting the lower-level microcontroller SPI read and write functions.

Macro Definition Documentation

#define AHB_READ_OPCODE 0x41

#define AHB_WRITE_OPCODE 0x61

dllmain.cpp File Reference

```
#include "Windows.h"
```

Functions

- BOOL APIENTRY **DllMain** (HMODULE hModule, DWORD ul_reason_for_call, LPVOID lpReserved)

Function Documentation

BOOL APIENTRY DllMain (HMODULE *hModule*, DWORD *ul_reason_for_call*, LPVOID *lpReserved*)

PCIe_Mini_CAN_FD.cpp File Reference

Implementation of the **PCIeMini_CAN_FD** board class.

```
#include <stdio.h>
#include "PCIeMini_CAN_FD.h"
```

Detailed Description

Implementation of the **PCIeMini_CAN_FD** board class.

TCAN4550.cpp File Reference

This file contains **TCAN4550** functions, and relies on the TCAN4x5x_SPI abstraction functions Additional Feature Sets of **TCAN4550** vs TCAN4x5x:

```
#include <stdint.h>
#include <stdio.h>
#include "TCAN4550.h"
```

Detailed Description

This file contains **TCAN4550** functions, and relies on the TCAN4x5x_SPI abstraction functions Additional Feature Sets of **TCAN4550** vs TCAN4x5x:

- Watchdog Timer Functions

TCAN4x5x_SPI.cpp File Reference

This file is responsible for abstracting the lower-level microcontroller SPI read and write functions.

```
#include <stdint.h>
#include "TCAN4550.h"
```

Macros

- #define **USE_AHB_CODE** 1
- #define **WAIT_FOR_IDLE**()

Detailed Description

This file is responsible for abstracting the lower-level microcontroller SPI read and write functions.

Macro Definition Documentation

#define USE_AHB_CODE 1

#define WAIT_FOR_IDLE()

```
Value:do \
{ \
    status = getStatus(); \
    if (status & ALTERA_AVALON_SPI_CONTROL_IE_MSK) resetStatus(); \
} while ((status & status_TRDY_mask) == 0);
```


x64/Debug/PCIeMini_CAN_FD_lib.vcxproj.FileListAbsolute.txt File Reference

C:/Alphi/PCIeMiniSoftware/PCIeMini_lib/AlphiBoard.cpp File Reference

Implementation of the base PCIe board class with Jungo driver and Altera PCIe hardware.

```
#include "wdc_lib.h"
#include "wdc_defs.h"
#include "utils.h"
#include "AlphiErrorCodes.h"
#include "AlphiBoard.h"
#include "status_strings.h"
#include "wdc_diag_lib.h"
#include <iostream>
```

Macros

- #define **QT_CORE_LIB**
- #define **MINIPCIE_ARINC429_DEFAULT_LICENSE_STRING** ((CHAR *)"872759db47d9ae7988a60332b89b6ea9c386010a7656b25cfdb4076053056c6f590d.WD1440_64_NL_Alphi_Technology_Corporation-DIS")
- #define **MINIPCIE_ARINC429_DEFAULT_DRIVER_NAME** WD_DEFAULT_DRIVER_NAME_BASE

Detailed Description

Implementation of the base PCIe board class with Jungo driver and Altera PCIe hardware.

Macro Definition Documentation

#define MINIPCIE_ARINC429_DEFAULT_DRIVER_NAME WD_DEFAULT_DRIVER_NAME_BASE

#define MINIPCIE_ARINC429_DEFAULT_LICENSE_STRING ((CHAR *)"872759db47d9ae7988a60332b89b6ea9c386010a7656b25cfdb4076053056c6f590d.WD1440_64_NL_Alphi_Technology_Corporation-DIS")

#define QT_CORE_LIB

C:/Alphi/PCIeMiniSoftware/PCIeMini_lib/AlphiBoard_dma.cpp File Reference

Implementation of the DMAs for the base PCIe board class with Jungo driver and Altera PCIe hardware.

```
#include "AlphiBoard.h"
#include "wdc_defs.h"
#include "wdc_lib.h"
#include "status_strings.h"
#include "stdio.h"
#include "string.h"
#include "utils.h"
```

Variables

- **MINIPCIE_INT_HANDLER MyDmaIntHandler**

Detailed Description

Implementation of the DMAs for the base PCIe board class with Jungo driver and Altera PCIe hardware.

Variable Documentation

MINIPCIE_INT_HANDLER MyDmaIntHandler

C:/Alphi/PCIeMiniSoftware/PCIeMini_lib/AlphiBoard_irq.cpp File Reference

Implementation of the interrupts for the base PCIe board class with Jungo driver and Altera PCIe hardware.

```
#include "AlphiBoard.h"
#include "wdc_defs.h"
#include "wdc_lib.h"
#include "stdio.h"
#include "string.h"
#include "utils.h"
#include "status_strings.h"
#include "wdc_diag_lib.h"
```

Macros

- #define **NUM_TRANS_CMDS** 0

Functions

- static void **MINIPCIE_ARINC429_IntHandler** (PVOID pData)
- static BOOL **doesItemExists** (PWDC_DEVICE pDev, ITEM_TYPE item)

Detailed Description

Implementation of the interrupts for the base PCIe board class with Jungo driver and Altera PCIe hardware.

Macro Definition Documentation

#define NUM_TRANS_CMDS 0

Function Documentation

static BOOL doesItemExists (PWDC_DEVICE *pDev*, ITEM_TYPE *item*) [static]

Check whether a given device contains an item of the specified type

static void MINIPCIE_ARINC429_IntHandler (PVOID *pData*) [static]

Interrupt handler routine

C:/Alphi/PCIeMiniSoftware/PCIeMini_lib/AlteraDma.cpp File Reference

Implementation of the DMA block controller.

```
#include "AlteraDma.h"
```

Detailed Description

Implementation of the DMA block controller.

C:/Alphi/PCIeMiniSoftware/PCIeMini_lib/AlteraSpi.cpp File Reference

Implementation of the low-level access routines to the SPI.

```
#include "stdint.h"
#include "AlteraSpi.h"
```

Detailed Description

Implementation of the low-level access routines to the SPI.

C:/Alphi/PCIeMiniSoftware/PCIeMini_lib/PcieCra.cpp File Reference

PCIe interface CRA class.
`#include "PcieCra.h"`

Detailed Description

PCIe interface CRA class.

C:/Alphi/PCIeMiniSoftware/PCIeMini_lib/PCIeMini_error.cpp File Reference

Error code to string conversion.

```
#include "stdio.h"
#include <string.h>
#include "AlphiErrorCodes.h"
#include "windrvr.h"
```

Functions

- char * **wdErrorToString** (**PCIeMini_status** errCode)
- DLL char * **getAlphiErrorMsg** (**PCIeMini_status** errCode)
  Gives the string description of an error code.

Detailed Description

Error code to string conversion.

Function Documentation

DLL char* getAlphiErrorMsg (PCIeMini_status *errCode*)

Gives the string description of an error code.

Parameters

errCode	Error code returned by a function

Return values

C-string,description	of the error

char * wdErrorToString (PCIeMini_status *errCode*)

C:/Alphi/PCIeMiniSoftware/PCIeMini_lib/TestProgram.cpp File Reference

Utility program class for the test programs.
`#include "TestProgram.h"`

Detailed Description

Utility program class for the test programs.

C:/Alphi/PCIeMiniSoftware/PCIeMini_lib/x64/Debug/CodeAnalysisResultManifest.txt File Reference

C:/Alphi/PCIeMiniSoftware/PCIeMini_lib/x64/Debug/PCIeMini_lib.vcxproj.FileListAbsolute.txt File Reference

C:/Alphi/PCIeMiniSoftware/PCIeMini_lib/x64/Release/PCIeMini_lib.vcxproj.FileListAbsolute.txt File Reference

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