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# Structural characterization of classical and memristive circuits with purely imaginary eigenvalues

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SUMMARY

The hyperbolicity problem in circuit theory concerns the existence of purely imaginary eigenvalues in the linearization of the time-domain description of the circuit dynamics. In this paper, we characterize the circuit configurations that, in a strictly passive setting, yield purely imaginary eigenvalues for all values of the capacitances and inductances. Our framework is based on branch-oriented, semistate (differential-algebraic) circuit models that capture explicitly the circuit topology, and use several notions and results from digraph theory. So-called *P-structures* arising in the analysis turn out to be the key element supporting our results. The analysis is shown to hold not only for classical (RLC) circuits but also for nonlinear circuits including memristors and other mem-devices. Copyright © 2011 John Wiley & Sons, Ltd.

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## 1. INTRODUCTION

Qualitative theory plays a key role in the analysis of nonlinear electrical and electronic circuits. Qualitative results are related, for example, to the stability properties of equilibria and operating points [5,17,22,28,60], oscillations [11,21,25,44], bifurcations [15,42,55], or chaotic phenomena [3,19,31,34,35,38,40,41,63,65]. These references are just a sample of the huge literature addressing qualitative aspects in electrical and electronic engineering (cf. also Ref. [37] and references therein). Recent approaches are based on the use of semistate (differential-algebraic) circuit models, accommodating both nodal and hybrid techniques for setting up the circuit equations [7,8,16,23,51–53,61,62].

In this context, we extend in the present paper our previous research concerning the qualitative properties of electrical circuits [56,57] by focusing on the hyperbolicity problem. A linear time-invariant VIRLC circuit (i.e. a circuit composed of independent voltage and current sources, and linear time-invariant resistors, inductors, and capacitors) is said to be *hyperbolic* if all the eigenvalues arising in the state-space description of the dynamics are away from the imaginary axis. Non-hyperbolic configurations exhibiting purely imaginary eigenvalues (PIEs) are important in linear circuit theory because they are responsible for proper oscillations. This problem is also relevant in the nonlinear

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context, since PIEs may be responsible for Hopf bifurcations (see, e.g. Example 3 [Subsection 5.4] below) resulting in practice in nonlinear oscillations.

The research here reported is driven by two goals: first, we aim to extend the results of [57] by presenting a full characterization of so-called *topologically non-hyperbolic* configurations, which are those yielding PIEs for all positive values of the capacitances and inductances involved in the circuit. We refer the reader to Subsection 2.3 for a more detailed description of this goal in terms of the equations that govern the circuit dynamics. Our second goal is to extend the hyperbolicity analysis to circuits with memristors and other mem-devices (memcapacitors and meminductors) [13,32,33,36,45,48–50,54,58]; these devices, whose origin can be traced back to the 1971 paper [4] by Leon Chua, are taking a very relevant role in electronics, stemming from the report of the design of a nanometer memristor by HP in 2008 [59].

Our approach is based on the use of time-domain branch-oriented circuit models that capture explicitly the circuit topology; the semistate (differential-algebraic) form of these models drives the spectral study to a matrix pencil setting. We will also make use of several concepts and results coming from digraph theory. All this material is compiled in Section 2. The first goal mentioned earlier is tackled in Section 3, where we extend the scope of the framework introduced in Ref. [57]; note that the results in Ref. [57] are restricted to circuits with one LC-loop or one LC-cutset only. Certain graph-theoretic structures (called *P-structures*) arising in the analysis will make it possible to extend those results to general circuits. Section 4 then revisits some examples from Ref. [57], trying not only to illustrate these notions and results but also to make it easier to read the proof of our main result, stated in Theorem 2. In Section 5, we extend the results to circuits with memristors, memcapacitors, and meminductors, and additional examples are discussed. Finally, concluding remarks are compiled in Section 6.

## 2. DIGRAPHS, CIRCUIT MODELS, AND THE HYPERBOLICITY PROBLEM

### 2.1. Some results from digraph theory

We compile several notions and results from digraph theory, which will be used in our analysis. Proofs and details can be found in Refs. [1,2,18]. We denote by $b$, $n$, and $c$ the number of branches, nodes, and connected components in a digraph $G$, respectively.

*2.1.1. Cutsets and loops.* A subset $K$ of the set of branches of a digraph is a *cutset* if the removal of $K$ increases the number of connected components of the digraph, and it is minimal with respect to this property, that is, the removal of any proper subset of $K$ does not increase the number of components.

Given an orientation in every cutset, the cutset matrix $\overline{Q} = (q_{ij})$ is defined as

$$q_{ij} = \begin{cases} 1 & \text{if branch } j \text{ is in cutset } i \text{ with the same orientation} \\ -1 & \text{if branch } j \text{ is in cutset } i \text{ with the opposite orientation} \\ 0 & \text{if branch } j \text{ is not in cutset } i. \end{cases}$$

The rank of $\overline{Q}$ can be proved to be $n$–$c$; any set of $n$–$c$ linearly independent rows of $\overline{Q}$ defines a *reduced cutset matrix* $Q \in \mathbb{R}^{(n-c)\times b}$. In a connected digraph, any reduced cutset matrix has the order $(n-1)\times b$.

Analogously, given an orientation in every loop, the *loop matrix* $\overline{B}$ is defined as $(b_{ij})$, with

$$b_{ij} = \begin{cases} 1 & \text{if branch } j \text{ is in loop } i \text{ with the same orientation} \\ -1 & \text{if branch } j \text{ is in loop } i \text{ with the opposite orientation} \\ 0 & \text{if branch } j \text{ is not in loop } i. \end{cases}$$

This matrix can be shown to have rank $b-n+c$. A *reduced loop matrix* $B$ is any $((b-n+c)\times b)$ submatrix of $\overline{B}$ with full row rank.



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If the columns of the reduced loop and cutset matrices $B$, $Q$ of a digraph are arranged according to the same order of branches, then $BQ^T=0$, $QB^T=0$. Moreover, the relations $imQ^T=kerB$ and $imB^T=kerQ$ do hold, and therefore the *cut space* $imQ^T$ spanned by the rows of $Q$ can be described as $kerB$, and analogously, the *cycle space* $imB^T$ spanned by the rows of $B$ equals $kerQ$ (see details in Ref. [2]). The cut and cycle spaces are orthogonal to each other.

*Lemma 1*
Let $K$ be a subset of branches of a digraph. Then $kerB_K$ and $kerQ_K$ are spanned by maximal sets of independent $K$-cutsets and independent $K$-loops.

This means that dim $kerB_K$ and dim $kerB_K$ are defined by the number of independent $K$-cutsets and $K$-loops, respectively. In particular, $K$ does not contain cutsets (resp. loops) if and only if $B_K$ (resp. $Q_K$) has full column rank.

*Blocks*
A key role in our analysis will be played by certain subgraphs called *blocks*.

*Definition 1*
A node is said to be an articulation if the removal of it and its incident branches increases the number of connected components of the digraph.

*Definition 2*
A digraph is said to be non-separable if it is connected and has no articulations.

*Definition 3*
A block is a maximal non-separable subgraph.

For our purposes, the main property of blocks is the one stated in Lemma 2.

*Lemma 2*
The branches of a block do not belong to any loop or cutset including branches from outside the block.

Given a distinguished set of branches $K$, we will call a loop or cutset including elements from both $K$ and $G$-$K$ a *hybrid* loop or cutset, respectively. Lemma 2 then says that the branches of a block $K$ do not take part either in hybrid loops or in hybrid cutsets. The absence of hybrid loops can be seen as a direct consequence of the fact that two blocks can have at most one common vertex (see, e.g. Theorem 1.13 of Ref. [1]), whereas the corresponding assertion for cutsets is explicitly stated in Theorem 3.23 of Ref. [1].

### 2.2. Semistate models for nonlinear circuits

We will analyze in Sections 3 and 4 certain properties of (say, classical) electrical circuits composed of resistors, capacitors, inductors, and independent voltage and current sources; circuits with memristors and other mem-devices will be considered in Section 5. Provided that capacitors and resistors are voltage controlled and that inductors are current controlled, the dynamics of a classical circuit can be described by the semistate system

$$C(v_c)v'_c = i_c \tag{1a}$$

$$L(i_l)i'_l = v_l \tag{1b}$$

$$0 = B_c v_c + B_l v_l + B_r v_r + B_j v_j + B_u v_s(t) \tag{1c}$$

$$0 = Q_c i_c + Q_l i_l + Q_r i_r + Q_j i_s(t) + Q_u i_u \tag{1d}$$



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$$0 = i_r - \gamma(v_r), \tag{1e}$$

where $C(v_c)$ and $L(i_l)$ are the incremental capacitance and inductance matrices, respectively. For later use, we denote the incremental conductance matrix $\gamma'(v_r)$ by $G(v_r)$. In system (1), we are splitting the vectors of branch voltages and currents as $v=(v_c, v_l, v_r, v_j, v_s(t))$ and $i=(i_c, i_l, i_r, i_s(t), i_u)$, the subscripts $c$, $l$, $r$, $j$, and $u$ corresponding to capacitors, inductors, resistors, current sources, and voltage sources, respectively. Note that for the voltage and current sources, we use directly the explicit excitation terms $v_s(t)$, $i_s(t)$. Equations (1c) and (1d) express Kirchhoff's voltage and current laws in terms of the reduced loop and cutset matrices $B=(B_c\ B_l\ B_r\ B_j\ B_u)$, $Q=(Q_c\ Q_l\ Q_r\ Q_j\ Q_u)$ introduced earlier.

System (1) combines the differential equations (1a) and (1b) coming from reactive elements with the algebraic (namely, non-differential) relations (1c, 1d, 1e) modeling Kirchhoff laws and the characteristics of resistors. In the electrical circuit literature, these differential-algebraic models are often referred to as *semistate systems*. The word 'semistate', which was proposed by Dziurla (see Ref. [29], p. 31), appeared for the first time in the joint work of Dziurla and Newcomb [14] (see also Ref. [46]). The semistate or differential-algebraic formalism is now widely used in circuit modeling and analysis (cf. Refs. [16,23,24,51–53,61,62] and references therein).

### 2.3. Linearization: the hyperbolicity problem

Let us now assume that all sources are DC (writing the excitation vectors as $V_s$ and $I_s$) and focus on an equilibrium point of (1), that is, a set of values for $v$ and $i$ that annihilates the right-hand side of (1). By letting $C$, $L$, and $G$ stand respectively for the capacitance, inductance, and conductance matrices at equilibrium, the linearization can be understood to govern the dynamics of the linear circuit described by the equations

$$Cv_c^{'} = i_c \tag{2a}$$

$$Li_l^{'} = v_l \tag{2b}$$

$$0 = B_c v_c + B_l v_l + B_r v_r + B_j v_j + B_u V_s \tag{2c}$$

$$0 = Q_c i_c + Q_l i_l + Q_r i_r + Q_j I_s + Q_u i_u \tag{2d}$$

$$0 = i_r - G v_r. \tag{2e}$$

In turn, the eigenvalues characterizing the dynamics of this circuit (and the local dynamics of (1) near equilibrium) are defined by the spectrum of the matrix pencil

$$\begin{pmatrix} \lambda C & 0 & -I & 0 & 0 & 0 & 0 & 0 \\ 0 & -I & 0 & \lambda L & 0 & 0 & 0 & 0 \\ B_c & B_l & 0 & 0 & B_r & 0 & B_j & 0 \\ 0 & 0 & Q_c & Q_l & 0 & Q_r & 0 & Q_u \\ 0 & 0 & 0 & 0 & G & -I & 0 & 0 \end{pmatrix}, \tag{3}$$

that is, the set of values of $\lambda$ that makes the matrix in (11) singular (cf. Refs. [20,53]).

The eigenvalue analysis can be driven to the RLC setting by working with the so-called *reduced* circuit obtained after open-circuiting current sources and short-circuiting voltage sources. For an RLC circuit, the dynamical behavior is defined by the system

$$Cv_c^{'} = i_c \tag{4a}$$



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$$Li_l^{'} = v_l \tag{4b}$$

$$0 = B_c v_c + B_l v_l + B_r v_r \tag{4c}$$

$$0 = Q_c i_c + Q_l i_l + Q_r i_r \tag{4d}$$

$$0 = i_r - G v_r, \tag{4e}$$

the matrix pencil associated with (4) being

$$\begin{pmatrix} \lambda C & 0 & -I & 0 & 0 & 0 \\ 0 & -I & 0 & \lambda L & 0 & 0 \\ B_c & B_l & 0 & 0 & B_r & 0 \\ 0 & 0 & Q_c & Q_l & 0 & Q_r \\ 0 & 0 & 0 & 0 & G & -I \end{pmatrix}. \tag{5}$$

Note that in (4) and (5), $B=(B_c\ B_l\ B_r)$ and $Q=(Q_c\ Q_l\ Q_r)$ are reduced loop and cutset matrices of the digraph that underlies the circuit obtained after open-circuiting current sources and short-circuiting voltage sources.

Pencil (3) or, equivalently, pencil (5), and in turn the linear circuit models (2) and (4), are *hyperbolic* if they do not display PIEs $\lambda=\pm\omega j$.The chance to tackle the problem in the RLC setting is based on the following result, which is proved in Ref. [57].

*Proposition 1*
Assume that a given VIRLC circuit has neither V-loops nor I-cutsets. The spectrum of the matrix pencil (3) coincides with that of pencil (5), provided that the latter is defined by the RLC circuit obtained after open-circuiting current sources and short-circuiting voltage sources.

Our goal in this paper will be to characterize the circuit configurations that lead to PIEs for all positive values of the capacitances and inductances, not only in the classical setting here described (our results in this context extending those presented in Ref. [57]) but also for circuits with mem-devices (cf. Section 5).

## 3. TOPOLOGICALLY NON-HYPERBOLIC CONFIGURATIONS IN CLASSICAL CIRCUITS

In light of (5), the analysis of non-hyperbolic circuit configurations involves looking for solutions $\lambda$ of the form $\pm\omega j$ for the system

$$\lambda C v_c = i_c \tag{6a}$$

$$\lambda L i_l = v_l \tag{6b}$$

$$0 = B_c v_c + B_l v_l + B_r v_r \tag{6c}$$

$$0 = Q_c i_c + Q_l i_l + Q_r i_r \tag{6d}$$

$$0 = i_r - G v_r. \tag{6e}$$

Our results will focus on solution $\lambda=\pm\omega j$ with $\omega\in\mathbb{R}-\{0\}$; see Theorem 1 for the case $\lambda=0$. Note also that, as far as resistors are strictly passive, the actual conductance values are known to be irrelevant (cf. Proposition 2 below). The analysis will be based on the following hypotheses.



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*Working hypotheses*
We will assume throughout Section 3 that the incremental capacitance and inductance matrices $C$ and $L$ are diagonal with positive entries, and that the incremental conductance matrix $G$ is positive definite. Additionally, the circuits will have neither IC-cutsets (i.e. cutsets formed just by current sources and/or capacitors) nor VL-loops (i.e. loops defined by voltage sources and/or inductors only).

A matrix $M$ is positive definite if $u^T M u > 0$ for any non-vanishing real vector $u$; we do not assume $M$ to be symmetric. The assumptions on the circuit matrices mean that there is no coupling among reactive elements, and that all devices are strictly locally passive. In turn, the absence of IC-cutsets and VL-loops rules out zero eigenvalues (cf. Theorem 1). Note that IC-cutsets include in particular C-cutsets, and analogously, L-loops are particular instances of VL-loops; it is also worth remarking that open-circuiting the current sources in an IC-cutset leads to a C-cutset, and similarly, short-circuiting voltage sources within a VL-loop yields an L-loop.

### 3.1. Previous results

IC-cutsets and VL-loops define topologically non-hyperbolic configurations, since (for positive definite matrices $C$, $L$, and $G$) they are known to characterize the existence of zero eigenvalues [26,27,43,56,57].

*Theorem 1*
The matrix pencil (3) has a zero eigenvalue if and only if the circuit has at least one IC-cutset or one VL-loop.

As stated in the working hypotheses, we will preclude these configurations in order to focus the hyperbolicity analysis on the existence of non-zero PIEs.

Eigenvectors associated with PIEs must necessarily have vanishing voltage and current in the resistor branches, as shown in Proposition 6 of Ref. [57] and as stated in Proposition 2.

*Proposition 2*
Any eigenvector associated with a PIE verifies $v_r = i_r = 0$.

### 3.2. LC-blocks lead to PIEs

The following statement expresses a well-known property in circuit theory.

*Proposition 3*
All eigenvalues of an LC-circuit are purely imaginary.

*Proof*
In the absence of resistors, pencil (5) reads

$$\begin{pmatrix} \lambda C & 0 & -I & 0 \\ 0 & -I & 0 & \lambda L \\ B_c & B_l & 0 & 0 \\ 0 & 0 & Q_c & Q_l \end{pmatrix}. \tag{7}$$

Assume that $\left(x_a^T, x_b^T, x_c^T, x_d^T\right) \neq 0$ is a left eigenvector. This means that

$$\lambda x_a^T C + x_c^T B_c = 0 \tag{8a}$$

$$-x_b^T + x_c^T B_l = 0 \tag{8b}$$



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$$-x_a^T + x_d^T Q_c = 0 \tag{8c}$$

$$\lambda x_b^T L + x_d^T Q_l = 0, \tag{8d}$$

and then

$$\lambda x_d^T Q_c C + x_c^T B_c = 0 \tag{9a}$$

$$\lambda x_c^T B_l L + x_d^T Q_l = 0. \tag{9b}$$

Let us multiply (9a) by $Q_c^T \overline{x}_d$; the transpose of the resulting equation, using the symmetry of $C$, is

$$\lambda x_d^* Q_c C Q_c^T x_d + x_d^* Q_c B_c^T x_c = 0. \tag{10}$$

Analogously, multiplying the conjugate of (9b) by $B_l^T x_c$, one gets

$$\overline{\lambda} x_c^* B_l L B_l^T x_c + x_d^* Q_l B_l^T x_c = 0. \tag{11}$$

Since $Q_c B_c^T + Q_l B_l^T = 0$, the sum of (10) and (11) yields

$$\lambda x_d^* Q_c C Q_c^T x_d + \overline{\lambda} x_c^* B_l L B_l^T x_c = 0. \tag{12}$$

The factors multiplying $\lambda$ and $\overline{\lambda}$ are real because both $C$ and $L$ are symmetric. The real part of (12) then reads

$$Re\lambda \left( x_d^* Q_c C Q_c^T x_d + x_c^* B_l L B_l^T x_c \right) = 0. \tag{13}$$

Additionally, due to the fact that $C$ and $L$ are positive definite, the assumption $Re\lambda \neq 0$ would imply $x_d^T Q_c = 0$, $x_c^T B_l = 0$. In turn, this would mean $x_c^T B_c = 0$, $x_d^T Q_l$ because of (9). Since both $(Q_c\ Q_l)$ and $(B_c\ B_l)$ have full row rank, we would derive $x_c^T = 0$, $x_d^T = 0$, which, together with $x_a^T = 0$, $x_b^T = 0$ from (8b) and (8c), lead to a contradiction, since $\left(x_a^T, x_b^T, x_c^T, x_d^T\right)$ was supposed not to vanish.

*Proposition 4*
Consider a VIRLC circuit. If after open-circuiting current sources and short-circuiting voltage sources there exists an LC-block, then the circuit has a PIE.

This is an immediate consequence of Proposition 3 and the decoupled structure of pencil (7) in the presence of a block, since according to Lemma 2, a block displays no hybrid loops or cutsets. Note that an eigenvalue–eigenvector pair of the LC-block can be extended to an eigenvalue–eigenvector pair of the whole circuit just by setting the remaining entries in the eigenvector to zero.

### *3.3. Statement of the main result*

The converse of Proposition 4 is not true. The examples discussed in Ref. [57] (cf. also Section 4) show that there are RLC circuits without LC-blocks displaying PIEs for certain values of the reactances. However, one may conjecture that if a circuit has PIEs for *all* positive values of the reactances, it must be because an LC-block is exhibited after open-circuiting current sources and short-circuiting voltage sources. This is a natural conjecture, but its proof turned out to be more difficult than expected. The remainder of Section 3 is devoted to show that this conjecture (stated as Theorem 2) is actually true.



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*Theorem 2*
A VIRLC circuit has a PIE for all positive values of capacitances and inductances if and only if after open-circuiting current sources and short-circuiting voltage sources, the reduced circuit exhibits an LC-block.

The 'if' part is already stated in Proposition 4. We need to prove that the 'only if' part is true. In the sequel, we work with the reduced RLC circuit (i.e. the circuit obtained after open-circuiting current sources and short-circuiting voltage sources) without further mention; note that the assumed exclusion of IC-cutsets and VL-loops precludes C-cutsets and L-loops in the reduced circuit.

### *3.4. P-structures*

The key aspect in the proof of Theorem 2 emanates from the following remarks. In the light of Proposition 2, the eigenvalue–eigenvector equations (6) read

$$\lambda C v_c = i_c \tag{14a}$$

$$\lambda L i_l = v_l \tag{14b}$$

$$B_c v_c + B_l v_l = 0 \tag{14c}$$

$$Q_c i_c + Q_l i_l = 0, \tag{14d}$$

for which a solution $\lambda=\omega j\neq 0$ is assumed to exist for all positive values of $C$ and $L$. Of course, the actual values of $\lambda$ and $\omega$ will depend on $C$, $L$.

Fix a set of values for $C$ and $L$, and focus on the non-vanishing entries of $v_c$, $v_l$, $i_c$, and $i_l$ within an associated eigenvector. Note that from (14a) and (14b), exactly the same entries vanish in the voltage and the current vector. Additionally, not all $v_l$'s (hence not all $i_l$'s) can vanish since, otherwise, the equation $B_c v_c=0$ resulting from (14c) would indicate the existence of a C-cutset (cf. Lemma 1). Analogously, not all $i_c$'s (hence not all $v_c$'s) may vanish since $Q_l i_l=0$ from (14d) would signal an L-loop, using again Lemma 1.

Let $K$ stand for the set of capacitive and inductive branches with non-vanishing voltage and current in the above-referred eigenvector. Use a subscript $k$ to denote the corresponding (non-vanishing) entries of $v_c$, $v_l$, $i_c$, and $i_l$ and also to specify the submatrices of $B_c$, $B_l$ $Q_c$, and $Q_l$ defined by the columns that correspond to $K$-branches, as well as the capacitances and inductances of the $K$-branches. With this notation, from (14) we get

$$\lambda C_k v_{ck} = i_{ck} \tag{15a}$$

$$\lambda L_k i_{lk} = v_{lk} \tag{15b}$$

$$B_{ck} v_{ck} + B_{lk} v_{lk} = 0 \tag{15c}$$

$$Q_{ck} i_{ck} + Q_{lk} i_{lk} = 0. \tag{15d}$$

The fact that all $v_{ck}$ and $v_{lk}$ within Equation (15c) do not vanish indicate, in the light of Lemma 1, that every $K$-branch forms at least one cutset just with other $K$-branches. Indeed, since $(v_{ck}, v_{lk})\in ker\ (B_{ck}\ B_{lk})$, this vector can be written as a linear combination of vectors describing $K$-cutsets; additionally, every $K$-branch must have a non-vanishing entry in at least one of these vectors since, otherwise, the corresponding entry in $v_{ck}$ or $v_{lk}$ would vanish.



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Proceeding analogously, (15d) indicates that every $K$-branch forms at least one loop just with other $K$-branches.

*Definition 4*
A set $K$ of capacitive and inductive branches, together with their incident nodes, is said to form a P-structure if every branch in $K$ forms at least one cutset and at least one loop just with other branches from $K$.

Examples of P-structures can be found in Figure 2. It is worth clarifying that the cutset and the loop arising in this definition do not need to include all the branches in $K$; nor it must happen that the cutset and the loop involve the same branches. For the sake of terminological simplicity, we will use $K$ also to mean the subgraph defined by the $K$-branches and their incident nodes.

The 'P' within the term 'P-structure' comes from 'PIE'. This term, however, should not be erroneously understood to guarantee the existence of a PIE; it just reflects the fact that these structures are the candidates that may (but not necessarily do) support the existence of a PIE.

In the light of Definition 4, the preceding discussion indicates that the branches corresponding to the non-vanishing entries of an eigenvector associated with a PIE form a P-structure. Briefly, we will say that the PIE-eigenvector arises from this P-structure.

An LC-block that does not amount to a single branch can be checked to be a P-structure (note, incidentally, that the P-structures from which a PIE-eigenvector arises include at least two branches, namely a capacitor and an inductor).

Certainly, the converse is not true. The proof of Theorem 2 is closely related to this fact. The idea of the proof is that the values of the capacitances and inductances of each P-structure, if it is not a block, must satisfy certain restrictions in order to allow for the existence of PIEs. Therefore, in order to have a PIE for all positive values of the capacitances and the inductances, at least one of these P-structures must be an LC-block. This is detailed in Subsection 3.5.

*3.4.1. Some instances of P-structures.* The notion of a P-structure can be illustrated by means of the circuits in Figure 1, already analyzed in Ref. [57]. Both circuits have a unique P-structure, as displayed in Figure 2. In both cases, the P-structure is defined by the four reactances. In the circuit depicted on the left, the four reactances define simultaneously a loop and a cutset. In the circuit on the right, there are two loops (defined by $L_1$, $C_1$ and by $L_2$, $C_2$, respectively) and just one cutset defined by the four reactances.

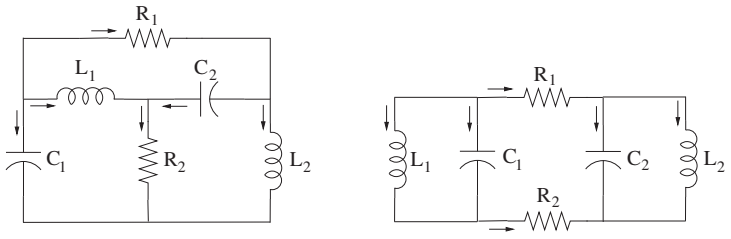


Figure 1. RLC circuits.

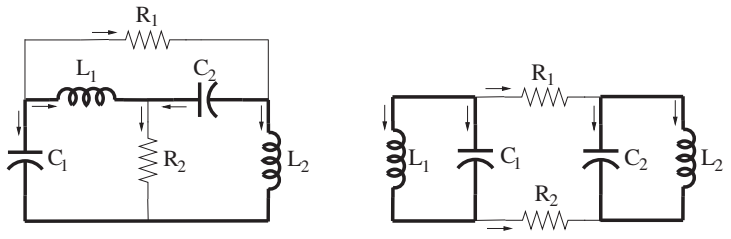


Figure 2. P-structures.



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### 3.5. *Proof of Theorem 2*

Assume that $(v_c, v_l, i_c, i_l)$ is an eigenvector associated with a PIE of an RLC circuit (possibly arising as the reduction of a VIRLC circuit in which current sources are open-circuited and voltage sources short-circuited). Consider the associated P-structure $K$ signaled by the non-vanishing entries of this eigenvector, and recall the relations depicted in (15). Let $b_k$, $n_k$, and $c_k$ stand for the number of branches, nodes, and connected components of $K$, respectively.

*Lemma 3*
If the P-structure $K$ is not a block, then the rank of $B_k=(B_{ck}\ B_{lk})$ is greater than $b_k-n_k+c_k$; if it is a block, then $rk\ B_k=b_k-n_k+c_k$.

*Proof*
Since $K$ is a (sub)circuit, it has $b_k-n_k+c_k$ independent loops. Assume, without loss of generality, that the first rows of the original loop matrix $B$ are defined from these $b_k-n_k+c_k$ independent loops.

Note that $B_k=(B_{ck}\ B_{lk})$ is a submatrix of $B$ including entries from *all* of the rows, and that $B_k$ has at least rank $b_k-n_k+c_k$ since the first $b_k-n_k+c_k$ rows are linearly independent. Write as $\widetilde{B}_k$ the submatrix of $B_k$ defined by the first $b_k-n_k+c_k$ rows, and note that this is a reduced loop matrix of the $K$-subcircuit.

Suppose that $K$ is not a block; this means that there exists a hybrid loop (cf. Lemma 2), namely a loop including some branches from $K$ and some others (label them with $Z$) that are not in $K$. Such a hybrid loop can be used to define a row of $B$ in a way such that the corresponding row of the submatrix $B_k$ is linearly independent of the first $b_k-n_k+c_k$ ones. Assume it is not. Write the hybrid-loop row of $B_k$ as a linear combination of the first $b_k-n_k+c_k$ ones. In the full $B$ matrix, subtract from the hybrid-loop row this linear combination, and note that the $Z$ entries do vanish in the first $b_k-n_k+c_k$ rows. This results in an element of the cycle space that consists only of the $Z$-entries of the hybrid loop, but this is impossible since this would correspond to a 'subloop' of the original hybrid loop.

This means that the existence of a hybrid loop makes the rank of the submatrix $B_k$ greater than $b_k-n_k+c_k$. Hence, if the P-structure is not a block, then the rank is greater than $b_k-n_k+c_k$. Notice also that if $K$ is a block, then the rank of $B_k$ is $b_k-n_k+c_k$ because the remaining rows in $B$ have zeros in the $K$-entries.

Regarding the cutset matrix $Q$, notice that $kerQ_k$ is spanned by linearly independent $K$-loops. Since the $K$-loops are the same in the original circuit and in the $K$-subcircuit, this means that $kerQ_k$ equals $ker\widetilde{Q}_k$, where $\widetilde{Q}_k$ is any (reduced) cutset matrix of the $K$-circuit.

According to the construction in Lemma 3, the first $b_k-n_k+c_k$ rows of (15c) read $\widetilde{B}_k v_k = 0$, where $v_k$ stands for $(v_{ck}, v_{lk})$. Additionally, the aforementioned identity $kerQ_k = ker\widetilde{Q}_k$ means that (15d) can be recast as $\widetilde{Q}_k i_k = 0$, where the vector $i_k$ stands for $(i_{ck}, i_{lk})$. This yields the following result.

*Lemma 4*
A PIE of the original circuit is also a PIE of the corresponding $K$-subcircuit, the non-vanishing entries of the original eigenvector defining an eigenvector of the $K$-subcircuit.

These properties make it possible to prove our main statement.

*Proof of Theorem 2*
The proof is crucially based on the fact that all PIE-eigenvectors must arise from some P-structure, according to Lemma 4.

Fix a P-structure $K$. We can choose the values of capacitances and inductances of the $K$-subcircuit in such a way that all eigenvalues of that subcircuit are simple. Moreover, this is true for parameter values lying on an open dense subset in $\mathbb{R}_+^{b_k}$, where $b_k$ is the number of branches in $K$ (and $\mathbb{R}_+$ is the set of positive real numbers). This is a consequence of the fact that eigenvalues are given by the roots of the polynomial defined by the determinant of (7), which has the form $p(\lambda,C,L)=a_m(C,L)\lambda^m+a_{m-1}(C,L)\lambda^{m-1}+\ldots+a_0(C,L)$. Note that $a_0(C,L)\neq 0$ because the absence of C-cutsets and L-loops rules out



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null eigenvalues. Multiple eigenvalues are defined by the intersection of $p(\lambda,C,L)=0$ and $p_\lambda(\lambda,C,L)=0$ and, therefore, occur only on a lower-dimensional set of the parameter space.

This means that the set of values of $C_k$, $L_k$ for which all eigenvalues are simple is open and dense in $\mathbb{R}_+^{b_k}$, and implies that the corresponding branch equations have generically corank one, namely that the coefficient matrix of

$$\lambda C_k v_{ck} = i_{ck} \tag{16a}$$

$$\lambda L_k i_{lk} = v_{lk} \tag{16b}$$

$$\widetilde{B}_{ck} v_{ck} + \widetilde{B}_{lk} v_{lk} = 0 \tag{16c}$$

$$\widetilde{Q}_{ck} i_{ck} + \widetilde{Q}_{lk} i_{lk} = 0 \tag{16d}$$

has generically corank one when $\lambda=\omega j$ is an eigenvalue of the $K$-subcircuit.

Write the corresponding linear system as

$$\begin{pmatrix} \lambda C_k & 0 & -I & 0 \\ 0 & -I & 0 & \lambda L_k \\ \widetilde{B}_{ck} & \widetilde{B}_{lk} & 0 & 0 \\ 0 & 0 & \widetilde{Q}_{ck} & \widetilde{Q}_{lk} \end{pmatrix} \begin{pmatrix} v_{ck} \\ v_{lk} \\ i_{ck} \\ i_{lk} \end{pmatrix} = 0. \tag{17}$$

Now, for an eigenvalue of the $K$-subcircuit to be an eigenvalue of the original circuit, not only (16c) has to be satisfied, but also the additional conditions coming from (15c). This means that the system

$$\begin{pmatrix} \lambda C_k & 0 & -I & 0 \\ 0 & -I & 0 & \lambda L_k \\ B_{ck} & B_{lk} & 0 & 0 \\ 0 & 0 & \widetilde{Q}_{ck} & \widetilde{Q}_{lk} \end{pmatrix} \begin{pmatrix} v_{ck} \\ v_{lk} \\ i_{ck} \\ i_{lk} \end{pmatrix} = 0 \tag{18}$$

must have a non-trivial solution for the same value of $\lambda$.

The coefficient matrix of (18) is a row-enlargement of that of (17), which as indicated earlier has generically corank one. If (18) has a non-trivial solution, the additional rows in (18) must be linearly dependent on those of (17) (always for generic values of $C$, $L$). Provided that the P-structure $K$ is not a block, there is at least one additional row in the $B_k$ rows of (18) coming from a hybrid loop. We know from the proof of Lemma 3 that this row cannot be expressed as a linear combination of the rows coming from $\widetilde{B}_k$ only. Obviously, it cannot be written just in terms of the $\widetilde{B}_k$ and $\widetilde{Q}_k$ rows, either. Therefore, this linear dependence relation involves (some of) the $C_k$, $L_k$ rows. Hence, if it is at all possible that system (18) has a non-vanishing solution, at least one algebraic restriction on the values of $C_k$ and $L_k$ must necessarily be met. We conclude that reactive values leading to PIEs, if any, must lie on a lower-dimensional set.

Altogether, the foregoing reasoning shows that, for a PIE associated with a given P-structure $K$ which is not a block, either it must happen that the PIE is a multiple eigenvalue of the $K$-subcircuit (and this may happen only for values of $L_k$, $C_k$ lying on a lower-dimensional set), or at least one restriction on the values of these reactances imposed by the existence of a hybrid loop must be met. Since this holds for all P-structures, and there is only a finite number of them, the fact that none of them is a block restricts the possible values of inductances and capacitances to a finite union of lower-dimensional sets, which obviously cannot fill the whole $\mathbb{R}_+^{b_c+b_l}$ space. This completes the proof of Theorem 2.



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## 4. RLC EXAMPLES

Consider the two circuits displayed in Figure 1. None of the P-structures shown in Figure 2 is a block, and therefore, none of these circuits can be topologically non-hyperbolic, according to Theorem 2. In the sequel, we use these circuits to illustrate the reasoning that supports this result. We believe that these examples should be of help for the reader to understand the discussion of Section 3. In particular, by means of the circuit on the left of Figure 1, we show how hybrid loops impose restrictions on the reactive values that yield PIEs, whereas the circuit on the right will be used to illustrate that multiple eigenvalues of the LC-subcircuit associated with a P-structure may lead to PIEs of the original circuit.

### *4.1. Example 1*

Let us focus on the circuit on the left of Figure 1. The LC-subcircuit defined by the P-structure is depicted in Figure 3.

This is a tank circuit, with two capacitors and two inductors connected in series; the corresponding matrix pencil has a zero eigenvalue due to the presence of a C-cutset, an infinite eigenvalue due to the L-cutset, and a unique (hence simple) pair of PIEs given by

$$\lambda = \pm\sqrt{-\frac{C_1 + C_2}{C_1 C_2 (L_1 + L_2)}}. \tag{19}$$

Our aim is to illustrate how the hybrid loops in the full RLC circuit impose additional constraints on the reactive values that keep (19) as a PIE of the original circuit. The matrix arising in (17), which characterizes the eigenvalues of this LC-subcircuit, reads

$$\begin{pmatrix} \lambda C_1 & 0 & 0 & 0 & -1 & 0 & 0 & 0 \\ 0 & \lambda C_2 & 0 & 0 & 0 & -1 & 0 & 0 \\ 0 & 0 & -1 & 0 & 0 & 0 & \lambda L_1 & 0 \\ 0 & 0 & 0 & -1 & 0 & 0 & 0 & \lambda L_2 \\ 1 & 1 & -1 & -1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & 1 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 1 \end{pmatrix}. \tag{20}$$

In particular, the fifth row of this matrix arises from Kirchhoff's voltage law when applied to the LC-loop, whereas the sixth, seventh, and eighth rows correspond to the current equations defined by the $C_1$-$L_1$, $C_2$-$L_2$, and $C_1$-$L_2$ cutsets of the LC-subcircuit.

Now, for the PIE (19) to be an eigenvalue of the original circuit, not only the homogeneous linear equations defined by (20) but also the additional ones arising in (18) must have a non-zero solution. These additional equations stem from the fact that the P-structure is not a block, and hence the hybrid loops will impose additional requirements. Two hybrid loops linearly independent of the LC-loop (cf.

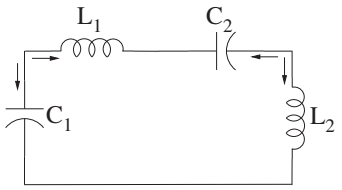


Figure 3. LC-subcircuit.



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Figure 1) are defined by $C_1$, $L_1$, $R_2$ and $C_1$, $L_2$, $R_1$, respectively. They define two extra rows yielding non-zero entries within the $(B_c\ B_l)$ block of the coefficient matrix, namely

$$\begin{pmatrix} 1 & 0 & -1 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & -1 & 0 & 0 & 0 & 0 \end{pmatrix}. \tag{21}$$

All but the fifth row of the matrix in (20) can be easily checked to be linearly independent. Hence, for (19) to be a PIE of the original circuit, the two rows of (21) must be linearly dependent on those seven. Writing down the linear dependence relation for the first row, that is, for the first hybrid loop, and skipping computations for the sake of brevity, one gets the extra relation $\lambda = \pm\sqrt{-(L_1C_1)^{-1}}$. Together with (19), this imposes the algebraic relation $L_1C_1=L_2C_2$ as a necessary restriction for the existence of a PIE in the original circuit. Note that this is already enough to show in practice that the circuit cannot be topologically non-hyperbolic.

Proceeding analogously with the second row of (21), which comes from the second hybrid loop, we get the additional relation $L_1C_2=L_2C_1$, and together with the aforementioned relation, we get $L_1=L_2$, $C_1=C_2$ as necessary relations for the existence of a PIE.

This is of course consistent with the results in Ref. [57]. Notice, however, that the approach in that study makes crucial use of the fact that this circuit has a unique LC-cutset. The use of P-structures overcomes this limitation and therefore extends the scope of Ref. [57].

### *4.2. Example 2*

The circuit on the right of Figure 1 illustrates how multiple eigenvalues of the LC-subcircuit defined by a P-structure may well lead to PIEs in the original circuit. The P-structure depicted on the right of Figure 2 yields an LC-subcircuit defined by two independent tanks, as shown in Figure 4.

Certainly, the eigenvalues of this circuit are given by

$$\lambda_{1,2} = \pm\sqrt{-\frac{1}{L_1C_1}}, \lambda_{3,4} = \pm\sqrt{-\frac{1}{L_2C_2}}, \tag{22}$$

which are simple if $L_1C_1 \neq L_2C_2$, and double if $L_1C_1=L_2C_2$.

Proceeding as in Example 1, the reader can check that, under the assumption $L_1C_1 \neq L_2C_2$, none of these PIEs of the LC-subcircuit yield an eigenvalue of the original RLC circuit. By contrast, the assumption $L_1C_1=L_2C_2$, which makes the PIE of the LC-circuit a double one, indeed leads to a PIE of the original circuit.

In this case, this is a consequence of the fact that the double eigenvalue has index one, and therefore the matrix (17) has corank two. Since no more than one hybrid loop (e.g. the one defined by the two capacitors and the two resistors) can be added to the LC-loops in a linearly independent manner, the matrix (18) will still be rank-deficient, showing that indeed the PIE will be an eigenvalue of the original circuit. As in the foregoing example, the results are consistent with the ones presented in Ref. [57], again without the need to use the fact that the circuit has a unique LC-cutset.

## 5. CIRCUITS WITH MEM-DEVICES

We detail in this section how to extend the results presented in the preceding discussion to circuits including mem-devices, namely memristors, memcapacitors, and meminductors. These devices are the

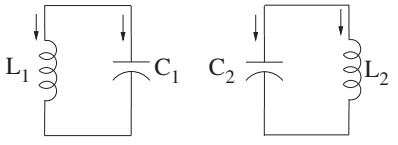


Figure 4. Double tank LC-subcircuit.



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object of much ongoing research in nonlinear circuit theory and electronics, not only from an analytical point of view [4,13,36,45,54,58,59] but also regarding applications in many different fields (see, e.g. Refs. [32,33,48–50] and references therein).

### 5.1. Memristors, memcapacitors, and meminductors

Circuit elements with memory (sometimes referred to as *mem-devices*) have been the object of a great attention in the last three years [13,32,33,36,45,48–50,54,58,59]. The origin of these devices can be found in Chua's 1971 paper [4]. For symmetry reasons, Chua postulated the existence of a nonlinear circuit element with a characteristic relating charge and flux, since resistors, capacitors, and inductors already involved the current–voltage, voltage–charge, and current–flux pairs. The report in 2008 of a nanometer device with a memristive characteristic (cf. Ref. [59]) had a great impact, and much research has been focused on this device since then. Memcapacitors and meminductors, introduced by Di Ventra *et al*. [13], have also received considerable attention.

A memristor can be either charge controlled or flux controlled. The former has a characteristic of the form

$$\varphi = \phi(q),$$

whereas for the latter, the constitutive relation reads as

$$q = \sigma(\varphi). \tag{23}$$

For the sake of simplicity, we will focus on flux-controlled memristors, although the results can be extended without difficulty to circuits including charge-controlled memristors. Differentiating the characteristic (23) and using the identities $q'=i$, $\varphi'=v$, one gets the current–voltage relation

$$i = W(\varphi)v, \tag{24}$$

where $W(\varphi)=\sigma'(\varphi)$ is the so-called *memductance*. This circuit element can be considered as a voltage-controlled resistor in which the conductance depends on $\varphi(t) = \int_{-\infty}^{t} v(\tau)d\tau$, thereby keeping track of the device history (hence the *memory resistor* or *memristor* name). In a charge-controlled setting, the voltage–current relation has the form

$$v = M(q)i, \tag{25}$$

where $M(q)=\varphi'(q)$ is the *memristance*. Note that both $\varphi$ and $\sigma$ must be actually nonlinear since, otherwise, the device would make no difference to a linear resistor.

Reactive elements with memory may be defined in a similar way. Specifically, a memcapacitor is governed by a relation of the form

$$q = C_m(\varphi)v, \tag{26}$$

so that the (mem-)capacitance $C_m$ depends on $\varphi=\int v$. A meminductor is defined by

$$\varphi = L_m(q)i, \tag{27}$$

with the (mem-)inductance $L_m$ now depending on $q=\int i$. See details in Ref. [13].

### 5.2. Circuit model and equilibria

The circuit model (1) may be expanded to accommodate also memristors, memcapacitors, and meminductors, as detailed in what follows. As indicated above, for the sake of simplicity, we assume the memristors to be flux controlled. This yields the differential-algebraic model



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$$C(v_c)\dot{v_c} = i_c \tag{28a}$$

$$L(i_l)\dot{i_l} = v_l \tag{28b}$$

$$\dot{\varphi_{mc}} = v_{mc} \tag{28c}$$

$$\dot{q_{mc}} = i_{mc} \tag{28d}$$

$$\dot{\varphi_{ml}} = v_{ml} \tag{28e}$$

$$\dot{q_{ml}} = i_{ml} \tag{28f}$$

$$\dot{\varphi_m} = v_m \tag{28g}$$

$$0 = B_c v_c + B_l v_l + B_{mc} v_{mc} + B_{ml} v_{ml} + B_r v_r + B_m v_m + B_j v_j + B_u v_s(t) \tag{28h}$$

$$0 = Q_c i_c + Q_l i_l + Q_{mc} i_{mc} + Q_{ml} i_{ml} + Q_r i_r + Q_m i_m + Q_j i_s(t) + Q_u i_u \tag{28i}$$

$$0 = q_{mc} - C_m(\varphi_{mc}) v_{mc} \tag{28j}$$

$$0 = \varphi_{ml} - L_m(q_{ml}) i_{ml} \tag{28k}$$

$$0 = i_r - \gamma(v_r) \tag{28l}$$

$$0 = i_m - W(\varphi_m) v_m, \tag{28m}$$

where the subscripts *m*, *mc*, and *ml* correspond to memristors, memcapacitors, and meminductors, respectively.

Equilibrium points are defined by the vanishing of the right-hand side of (28). It is easy to check that, at equilibrium, all voltages and currents in memristors, memcapacitors, and meminductors are null, and so they are $q_{mc}$ and $\varphi_{ml}$ because of (28j, 28k) In what follows, we show how the results of Section 3 can be extended to the linearization of circuits with mem-devices at equilibria.

### *5.3. Linearization*

In the linearization about any equilibrium point, one can check that the partial derivatives with respect to $\varphi_m$, $\varphi_{mc}$, and $q_{ml}$ of the map defining the right-hand side of (28) do vanish identically, because of the identities $v_m$=0, $v_{mc}$=0, $i_{ml}$=0 at equilibrium. This means that the linearization displays a null eigenvalue whose geometric multiplicity equals the total number of mem-devices. The remaining eigenvalues are defined by the eigenvalue–eigenvector equations

$$\lambda C v_c = i_c \tag{29a}$$

$$\lambda L i_l = v_l \tag{29b}$$



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$$\lambda q_{mc} = i_{mc} \tag{29c}$$

$$\lambda \varphi_{ml} = v_{ml} \tag{29d}$$

$$0 = B_c v_c + B_l v_l + B_{mc} v_{mc} + B_{ml} v_{ml} + B_r v_r + B_m v_m \tag{29e}$$

$$0 = Q_c i_c + Q_l i_l + Q_{mc} i_{mc} + Q_{ml} i_{ml} + Q_r i_r + Q_m i_m \tag{29f}$$

$$0 = q_{mc} - C_m v_{mc} \tag{29g}$$

$$0 = \varphi_{ml} - L_m i_{ml} \tag{29h}$$

$$0 = i_r - G v_r \tag{29i}$$

$$0 = i_m - W v_m, \tag{29j}$$

obtained after short-circuiting voltage sources and open-circuiting current sources. Here, $C$, $L$, $C_m$, $L_m$, $G$, and $W$ are the capacitance, inductance, memcapacitance, meminductance, conductance, and memductance matrices at equilibrium, respectively. By means of a Schur reduction [30,53], we may describe, via (29g)-(29h), the solutions of (29) in terms of those of

$$\lambda C v_c = i_c \tag{30a}$$

$$\lambda C_m v_{mc} = i_{mc} \tag{30b}$$

$$\lambda L i_l = v_l \tag{30c}$$

$$\lambda L_m i_{ml} = v_{ml} \tag{30d}$$

$$0 = B_c v_c + B_{mc} v_{mc} + B_l v_l + B_{ml} v_{ml} + B_r v_r + B_m v_m \tag{30e}$$

$$0 = Q_c i_c + Q_{mc} i_{mc} + Q_l i_l + Q_{ml} i_{ml} + Q_r i_r + Q_m i_m \tag{30f}$$

$$0 = i_r - G v_r \tag{30g}$$

$$0 = i_m - W v_m. \tag{30h}$$

The key remark is that, grouping together capacitors and memcapacitors, inductors and meminductors, and resistors and memristors, system (30) is formally identical to (6), in the understanding that $C$, $L$, and $G$ in (6) correspond in (30) to the block-diagonal matrices defined by $C$ and $C_m$, $L$ and $L_m$, and $G$ and $W$, respectively. This fact supports Theorem 3, which is an analog of Theorem 2 for circuits with memdevices. We denote by $m$ the total number of memristors, memcapacitors, and meminductors.

*Theorem 3*

Assume that, at a given equilibrium, the matrices $C$, $C_m$, $L$, and $L_m$ are diagonal with positive entries, that $G$ and $W$ are positive definite, and that the circuit does not have either cutsets formed just by



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current sources and/or capacitors and/or memcapacitors or loops defined by voltage sources and/or inductors and/or meminductors. Disregarding $m$ null eigenvalues associated with mem-devices, the circuit has a pair of PIEs for all positive values of capacitances, memcapacitances, inductances, and meminductances if and only if after open-circuiting current sources and short-circuiting voltage sources, the reduced circuit exhibits a capacitive-inductive block.

Certainly, a capacitive-inductive block may now be composed of capacitors, memcapacitors, inductors, and/or meminductors. As in the setting of Section 3, the block must include at least one capacitive and one inductive element for a PIE to exist.

### *5.4. Example 3*

The circuit depicted in Figure 5 is proposed in Ref. [50] as a scheme to couple two quantum bits (cf. Refs. [10,12,47,64]). Each qubit is defined by the series connection of a voltage source, a linear capacitor, and a Josephson junction. The use of a memcapacitor is aimed at controlling the interaction between both qubits by pre-setting the value of the memcapacitance $C_m$. In what follows, we examine how the presence of small memristive currents within the Josephson junctions affects the existence of PIEs in this circuit, and address certain related bifurcations.

The Josephson junction, which consists of two superconductors separated by an insulating layer, can be modeled as a nonlinear, flux-controlled inductor with a current-flux characteristic of the form

$$i_l = I_0 sin(k_0 \varphi_l), \tag{31}$$

for physical constants $I_0$, $k_0$ [9]. Provided that $\cos(k_0\varphi_l) \neq 0$, the incremental inductance is

$$L(\varphi_l) = \frac{1}{I_0 k_0 \cos(k_0 \varphi_l)}.$$

However, as detailed in Ref. [6], a small memristive current in parallel should also be taken into account in an accurate model of the Josephson junction. This memristive current is governed by

$$i_m = I_1 \cos(k_1 \varphi_m) v_m, \tag{32}$$

for constants $I_1$, $k_1$. The memductance reads as

$$W(\varphi_m) = I_1 \cos(k_1 \varphi_m).$$

Note that this expression may become negative for certain values of $\varphi_m$. We ignore other parasitic effects that are not relevant to our analysis. Replacing in Figure 5 both junctions by the parallel connection of a nonlinear inductor and a memristor governed by (31) and (32), respectively, we get the circuit depicted in Figure 6.

*5.4.1. The uncoupled case, $C_m$=0.* Let us first consider the dynamics of the circuit displayed in Figure 6 when $C_m$=0, that is, in the absence of the memcapacitor. In this situation, both qubits are

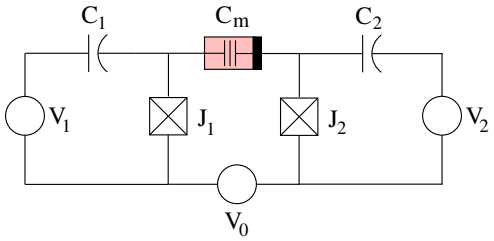


Figure 5. Memcapacitive coupling of two quantum bits.



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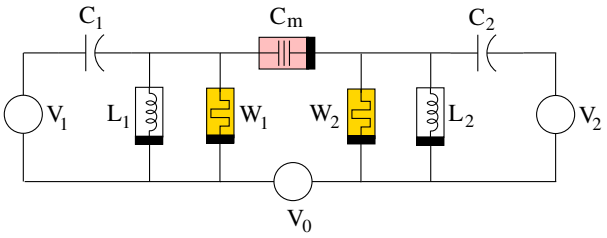


Figure 6. Equivalent circuit.

uncoupled and their dynamics can be analyzed independently. For notational simplicity, denote by $V$, $C$, $L$, and $W$ the DC voltage, capacitance, inductance, and memductance of the (say) left qubit, respectively. The dynamics is defined by the model

$$Cv_c^{'} = I_0 \sin(k_0\varphi_l) + W(\varphi_m)(V - v_c) \tag{33a}$$

$$\varphi_l^{'} = V - v_c \tag{33b}$$

$$\varphi_m^{'} = V - v_c. \tag{33c}$$

Equilibria are defined by $v_c = V$ and $sin(k_0\varphi_l)=0$, without restrictions on $\varphi_m$. Fix, for example, $\varphi_1=0$, which yields a positive incremental inductance $L$ in the Josephson junction. The linearization of (33) at this equilibrium can be easily checked to exhibit a null eigenvalue and a conjugate pair

$$\lambda = \frac{-W}{2C} \pm \sqrt{\left(\frac{W}{2C}\right)^2 - \frac{1}{LC}}. \tag{34}$$

No PIEs are displayed if $W \neq 0$. However, if $W=0$, we get

$$\lambda = \pm j\sqrt{\frac{1}{LC}}. \tag{35}$$

This is a consequence of the fact that, ignoring memristive currents, each uncoupled qubit amounts to a (nonlinear) tank circuit after short-circuiting the voltage source, hence displaying a PIE in the linearized problem, as expected. Noteworthy, (34) can be seen as an unfolding of (35): When $W$ becomes negative, the pair of conjugate eigenvalues crosses the imaginary axis towards the right half-plane, and the equilibrium undergoes a Hopf bifurcation.

Our goal is to examine whether PIEs are also displayed in the presence of the memcapacitor when one memductance vanishes, and if our framework may shed some light in this regard. This task is undertaken in the following subsection.

*5.4.2. Memcapacitive coupling, $C_m \neq 0$.* Let us turn our attention back to the circuit of Figure 6 with $C_m \neq 0$. With the foregoing discussion for the case $C_m=0$, one may conjecture if the vanishing of either $W_1$ or $W_2$ (but not both) is enough to support the existence of a pair of PIEs in the linearized circuit dynamics.

As detailed later, checking whether this conjecture is true or not is by no means a trivial computation; it does not seem to have an easy response without the results discussed in this paper, either.

Assume, for example, that $W_1 > 0$, $W_2=0$. By short-circuiting the voltage sources, one gets the reduced circuit displayed in Figure 7.



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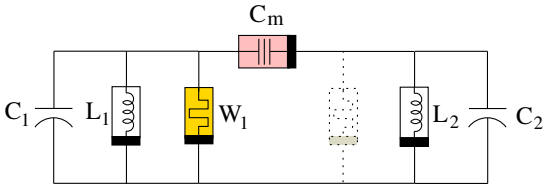


Figure 7. Reduced circuit with $W_2=0$.

Theorem 3 shows that the above conjecture is actually false if we seek for the existence of PIEs for arbitrary (albeit positive) values of $C_m$, $C_i$, $L_i$ ($i=1,2$). This is a consequence of the fact that no capacitive-inductive block (in this case, a block composed of inductors, capacitors and/or the memcapacitor) is displayed in the reduced circuit. However, our framework makes it possible to say more: the circuit has no PIEs for any single set of positive values of $C_m$, $C_i$, $L_i$ if $W_1>0$, $W_2=0$. Indeed, a P-structure is needed for a PIE to be displayed, but the reduced circuit in Figure 7 has no P-structures. This claim can be checked as follows: all cutsets including $C_1$ or $L_1$ include also $W_1$, and therefore both $C_1$ and $L_1$ are precluded in any (tentative) P-structure. Such a P-structure should then involve $L_2$, $C_2$, and/or $C_m$, but the only loop within this set is the one defined by $L_2$ and $C_2$; they do not form a cutset, and the one that they define together with $C_m$ involves the memcapacitor, which in turn does not form a loop just with $C_2$ and/or $L_2$. No P-structure may then support the existence of a PIE in the setting considered above, that is, if $W_1>0$, $W_2=0$; obviously, the same is true by symmetry if $W_1=0$, $W_2>0$.

It is not a simple task to compute the eigenvalues of the linearized dynamics in order to show in practice that no PIEs are displayed. In this case, the determinant of the matrix pencil characterizing the spectrum of the linearized problem can be written, for arbitrary values of $C_m$, $C_i$, $L_i$, $W_i$ ($i=1,2$), as $\lambda^3 p(\lambda,z)$; for the sake of notational simplicity, we group together all the parameters $C_m$, $C_1$, $C_2$, $L_1$, $L_2$, $W_1$, and $W_2$ into a single vector $z$. The triple zero owes to the two memristors and the memcapacitor, each one being responsible for a null eigenvalue. In turn, $p$ can be written as

$$p(\lambda,z)=a_4\lambda^4+a_3\lambda^3+a_2\lambda^2+a_1\lambda+a_0, \tag{36}$$

the coefficients of (36) being

$$\begin{aligned}
a_4&=kL_1L_2(C_1C_2+C_1C_m+C_2C_m)\\
a_3&=kL_1L_2((C_1+C_m)W_2+(C_2+C_m)W_1)\\
a_2&=k(L_1C_1+L_2C_2+(L_1+L_2)C_m+L_1L_2W_1W_2)\\
a_1&=k(L_1W_1+L_2W_2)\\
a_0&=k
\end{aligned}$$

with $k=(L_1L_2C_1C_2)^{-1}$. The fact that a double PIE cannot exist is a simple consequence of the non-vanishing of $a_3$ and $a_1$ when $W_1>0$, $W_2=0$ and all inductances and capacitances are strictly positive. It is more difficult to rule out simple PIEs; we may, in this case, resort to the Routh-Hurwitz criteria for PIEs discussed in Ref. [39]. As detailed in that study, the existence of a simple PIE requires that the relation

$$a_1^2a_4+a_0a_3^2-a_1a_2a_3=0 \tag{37}$$

holds. The expression depicted in (37) can be written as a cubic polynomial in $W_2$ with coefficients depending on $C_m$, $C_i$, $L_i$, and $W_1$; in particular, the independent term (the only one that does not necessarily vanish with $W_2$) is $k^3L_1^3L_2C_m^2W_1^2$. Provided that $W_1>0$, $W_2=0$, and that all inductances and capacitances are strictly positive, this expression cannot vanish, and this confirms that, indeed, there are no simple PIEs.

Note that this kind of computation is not feasible for more complex problems, whereas our theoretical discussion reduces the analysis to a topological check in the circuit. The absence of PIEs if



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both $W_1$ and $W_2$ are strictly positive can be derived from our framework in a similar way. Finally, if both $W_1$ and $W_2$ vanish, then the whole reduced circuit is a capacitive-inductive block, and the existence of PIEs for arbitrary positive values of $C_m$, $C_i$, and $L_i$ follows.

## 6. CONCLUDING REMARKS

In this paper, we have characterized topologically non-hyperbolic configurations in strictly passive circuits, yielding PIEs for *all* values of the capacitances and inductances. Our approach captures explicitly the circuit topology by means of branch-oriented DAE models. The use of so-called P-structures makes it possible to extend the scope of our framework beyond the setting considered in Ref. [57], which only applies to circuits with a unique LC-loop or a unique LC-cutset.

Additionally, we have shown how to accommodate mem-devices (namely, memristors, memcapacitors, and meminductors) in the hyperbolicity analysis. Several examples illustrate our results.

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