

(wileyonlinelibrary.com) DOI: 10.1002/mma.2544
MOS subject classification: 05C50; 15A22; 34A09; 94C05; 94C15

The tractability index of memristive circuits: branch-oriented and tree-based models

Fernando García-Redondo and Ricardo Riaza^{*†}

Communicated by K. P. Haderler

The memory-resistor or memristor is a new electrical element characterized by a nonlinear charge-flux relation. This device poses many challenging problems, in particular from the circuit modeling point of view. In this paper, we address the index analysis of certain differential-algebraic models of memristive circuits; specifically, our attention is focused on so-called branch-oriented models, which include in particular tree-based formulations of the circuit equations. Our approach combines results coming from differential-algebraic equation theory, matrix analysis and theory of digraphs. This framework should be useful in future studies of dynamical aspects of memristive circuits. Copyright © 2012 John Wiley & Sons, Ltd.

Keywords: nonlinear circuit; memristor; differential-algebraic equation; semistate model; index; tree

1. Introduction

The memory-resistor or *memristor* is considered as the fourth basic element in circuit theory, besides resistors, inductors and capacitors. It is defined by a nonlinear charge-flux characteristic, which may have either a charge-controlled form $\varphi = \phi(q)$ or a flux-controlled form $q = \sigma(\varphi)$. The existence of such a device was already postulated for symmetry reasons by Chua in 1971 [1] (see also [2]), and the actual appearance of memristors in nanoscale electronics announced in [3] has raised a renewed interest in these devices. Many analytical aspects of memristors and memristive-based circuits, as well as several applications, have been reported in the last three years (cf. [4–15] and references therein).

Modeling and analyzing memristive circuits pose many challenging mathematical problems. The nonlinear character of memristors naturally leads to the use of time-domain circuit models. These models may be the state-space ones, based on explicit ODEs; nevertheless, in the presence of a high number of devices, the circuit equations are usually set up in terms of *semistate* models on the basis of differential-algebraic equations (DAEs) [16–27]. As detailed below, the analysis of memristive circuit models involves a systematic use of digraph theory and matrix analysis, including matrix pencil theory. This drives the study of modeling aspects of memristive circuits to an interdisciplinary framework.

In this paper, we undertake the analysis of the DAE *index* of the memristive circuit models arising from the so-called branch-oriented approach. These models are closely related to tree-based systems and hybrid analysis [19, 20, 25, 28] and play a key role in the study of many analytical features of circuit theory, not only to set up the network equations but also to address different problems that include, among others, the state formulation problem and several dynamic properties, including stability aspects [22–24].

The above-mentioned index of a differential-algebraic circuit model can be introduced in different ways. The reader is referred to [22, 29–35] for detailed discussions of the different index notions, which include the differentiation, geometric, perturbation, strangeness and tractability indices. The tractability index concept will be of particular interest and is presented in Section 3. All the index concepts can be understood to generalize the Weierstrass–Kronecker index of a matrix pencil [36] to time-varying and/or nonlinear settings. Within the circuit context, the tractability index of different DAE models of classical circuits does not exceed 2 under passivity assumptions [16–18, 22, 26–28]; index 1 configurations are of special interest because they allow for the use of efficient theoretical and numerical tools in their analysis. Some of these results have been recently extended to nodal models of memristive circuits [14]. In the present paper, we address the index analysis of a different family of circuit models, which arise from a branch-oriented approach and require different graph-theoretic techniques. Our results will apply in particular to tree-based formulations, very often used in practice.

Departamento de Matemática Aplicada a las Tecnologías de la Información, Escuela Técnica Superior de Ingenieros de Telecomunicación, Universidad Politécnica de Madrid, 28040 Madrid, Spain

^{*}Correspondence to: Ricardo Riaza, Departamento de Matemática Aplicada a las Tecnologías de la Información, Escuela Técnica Superior de Ingenieros de Telecomunicación, Universidad Politécnica de Madrid, 28040 Madrid, Spain.

[†]E-mail: ricardo.riaza@upm.es

The paper is structured as follows. Section 2 compiles some background on digraph theory and also on memristive circuits. Section 3 introduces the tractability index notion, which supports the index analysis presented in Section 4. Some concluding remarks can be found in Section 5.

2. Background

2.1. Some results from the digraph theory

Some background on digraph theory is necessary before introducing the circuit models. Specifically, we will make systematic use of the loop and cutset matrices introduced below and, occasionally, of the so-called *fundamental* loop and cutset matrices arising from the choice of a spanning tree.

Consider a directed graph with n nodes (vertices), m branches (edges) and k connected components. Chosen an orientation in every loop, the *loop matrix* \tilde{B} is defined as (b_{ij}) , where

$$b_{ij} = \begin{cases} 1 & \text{if branch } j \text{ is in loop } i \text{ with the same orientation} \\ -1 & \text{if branch } j \text{ is in loop } i \text{ with the opposite orientation} \\ 0 & \text{if branch } j \text{ is not in loop } i. \end{cases}$$

The rank of this matrix can be shown to equal $m - n + k$. A *reduced loop matrix* B is any $((m - n + k) \times m)$ -submatrix of \tilde{B} with full row rank.

A subset K of the set of branches of a digraph is a *cutset* if the removal of K increases the number of connected components of the digraph, and it is minimal with respect to this property, that is, the removal of any proper subset of K does not increase the number of components. In a connected digraph, a cutset is just a minimal disconnecting set of branches. The removal of the branches of a cutset increases the number of connected components by exactly 1. Furthermore, all the branches of a cutset may be shown to connect the same pair of connected components of the digraph that results from the deletion of the cutset. This makes it possible to define the orientation of a cutset, say from one of these components toward the other. The cutset matrix $\tilde{D} = (d_{ij})$ is then defined by

$$d_{ij} = \begin{cases} 1 & \text{if branch } j \text{ is in cutset } i \text{ with the same orientation} \\ -1 & \text{if branch } j \text{ is in cutset } i \text{ with the opposite orientation} \\ 0 & \text{if branch } j \text{ is not in cutset } i. \end{cases}$$

The rank of \tilde{D} can be proved to be $n - k$; any set of $n - k$ linearly independent rows of \tilde{D} defines a *reduced cutset matrix* $D \in \mathbb{R}^{(n-k) \times m}$. In a connected digraph, any reduced cutset matrix has order $(n - 1) \times m$.

Certain submatrices of B and D characterize the existence of so-called K -cutsets and K -loops (that is, cutsets or loops just defined by branches belonging to a given set of branches K), as stated below. We denote by B_K (resp. B_{G-K}) the submatrix of B defined by the columns that belong (resp. do not belong) to K ; the same applies to the cutset matrix D . The reader is referred to [22, Sect. 5.1] for explicit proofs of the following assertions.

Lemma 1

Let K be a subset of branches of a given digraph \mathcal{G} . The following assertions are equivalent:

- (a) K does not contain cutsets;
- (b) B_K has full column rank;
- (c) D_{G-K} has full row rank.

Analogously, the following statements are equivalent:

- (d) K does not contain loops;
- (e) D_K has full column rank;
- (f) B_{G-K} has full row rank.

The following digraph analog of Tellegen's theorem will also be useful in our analysis (e.g., see [37, Section 7.4]).

Lemma 2

If the columns of the reduced loop and cutset matrices B and D of a digraph are arranged according to the same order of branches, then $BD^T = 0$, $DB^T = 0$.

Actually, the relations $\text{im } D^T = \ker B$ and $\text{im } B^T = \ker D$ hold true. Hence, the *cut space* $\text{im } D^T$ spanned by the rows of D can be described as $\ker B$, and analogously, the *cycle space* $\text{im } B^T$ spanned by the rows of B equals $\ker D$ [38]. These spaces are orthogonal to each other because $(\text{im } D^T)^\perp = (\ker B)^\perp = \text{im } B^T$.

A particular form of the loop and cutset matrices follows from the choice of a spanning tree in a connected digraph (e.g., see [22, 39]). The branches in the tree are called *twigs*, whereas the remaining ones are called *links*. A well-known property in digraph theory states that every link defines a unique loop together with some twigs, and every twig defines a unique cutset together with some links. Because of this property and Lemma 2, the so-called *fundamental* loop and cutset matrices constructed from a given tree read as

$$B = (F \ I), \quad D = (I - F^T)$$

for a certain submatrix F .

2.2. Memristive circuits

Consider a nonlinear, connected, time-invariant circuit composed of capacitors, inductors, resistors, memristors and independent voltage and current sources. Capacitors and inductors will have C^1 voltage-controlled and current-controlled characteristics $q_c = \psi(v_c)$ and $\varphi_l = \eta(i_l)$, respectively; we denote by $C(v_c)$ and $L(i_l)$ the incremental capacitance and inductance matrices $\psi'(v_c)$, $\eta'(i_l)$.

Memristors will be defined by the C^2 charge-controlled relation $\varphi_m = \phi(q_m)$. The incremental *memristance* is $M(q_m) = \phi'(q_m)$. Note that the relations $\varphi'_m(t) = v_m(t)$ and $q'_m(t) = i_m(t)$ yield $v_m(t) = M(q_m(t))i_m(t)$; the 'memory-resistor' name comes from the fact that the device behaves as a resistor in which the resistance depends on $q_m(t) = \int_{-\infty}^t i_m(\tau) d\tau$. Resistors will be assumed to be current-controlled by a C^1 map of the form $v_r = \rho(i_r)$, and we let $R(i_r)$ stand for the incremental resistance matrix $\rho'(i_r)$. Under a strict passivity assumption on resistors and memristors, the results will be shown to hold also in the presence of voltage-controlled resistors (note that the nonlinear nature allowed for all circuit elements makes, e.g., a diode belong to this class of devices) and/or flux-controlled memristors. Recall that a given set of devices (capacitors, inductors, resistors or memristors) are strictly passive if the corresponding matrix P (standing for $C(v_c)$, $L(i_l)$, $R(i_r)$ or $M(q_m)$, respectively) is positive definite, that is, if the quadratic form $u^T P u = u^T (P + P^T) u / 2$ is positive definite (equivalently, if $u^T P u > 0$ for any non-vanishing vector u). None of these matrices is assumed to be symmetric.

Writing the excitation terms coming from the voltage and current sources, respectively, as $v_s(t)$ and $i_s(t)$, the circuit equations can be written in the form

$$C(v_c)v'_c = i_c \quad (1a)$$

$$L(i_l)i'_l = v_l \quad (1b)$$

$$q'_m = i_m \quad (1c)$$

$$0 = v_m - M(q_m)i_m \quad (1d)$$

$$0 = v_r - \rho(i_r) \quad (1e)$$

$$0 = B_c v_c + B_l v_l + B_m v_m + B_r v_r + B_u v_s(t) + B_j v_j \quad (1f)$$

$$0 = D_c i_c + D_l i_l + D_m i_m + D_r i_r + D_u i_u + D_j i_s(t), \quad (1g)$$

where we are expressing Kirchhoff's laws in terms of the loop and cutset matrices as $Bv = 0$ and $Di = 0$. Note that the loop matrix B is split as $(B_c \ B_l \ B_m \ B_r \ B_u \ B_j)$, where B_c (resp. B_l, B_m, B_r, B_u, B_j) corresponds to the columns accommodating capacitors (resp. inductors, memristors, resistors, voltage sources and current sources). The same applies to the cutset matrix D .

It is worth emphasizing that system (1) covers, in particular, models coming from the choice of a given spanning tree in the circuit; these tree-based models are very often used in circuit theory (cf. for instance [22, 39, 40]). In that case, B and D take the form $B = (F \ I)$ and $D = (I - F^T)$; this means that the voltages of link devices are expressed in terms of twig voltages in (1f) and, analogously, twig currents are written in terms of link currents in (1g). The results will therefore apply in particular to such tree-based models. Although in our analysis, we will not make use of the special form of these fundamental matrices.

The circuit model (1) has the form of a quasilinear (or linearly implicit) DAE, namely

$$A(x)x' = g(x, t), \quad (2)$$

where A stands for a block-diagonal matrix $\text{block-diag}(C, L, I, 0)$ and x comprises all the branch variables entering the model. The right-hand side can be actually written as

$$g(x, t) = f(x) + s(t), \quad (3)$$

because the excitation terms $B_u v_s(t)$ and $D_j i_s(t)$ coming from the voltage and current sources are decoupled from the remaining terms. Section 3 provides some general background on DAEs and their index. In Section 4, we characterize the tractability index of (1) in the light of its linearly implicit form (2).

In the sequel, all circuits will be assumed to be well posed; this means that V-loops (loops just defined by voltage sources) and I-cutsets (cutset defined by current sources only) do not occur.

3. Projector-based analysis of differential-algebraic equation circuit models

Differential-algebraic equations, also known as semistate systems, constrained equations or descriptor systems, arise in different application fields; in addition to circuit theory, these include mechanics, control theory, power systems theory and others [22, 29–32, 34, 35].

Many analytical and numerical properties of DAEs rely on their *index*: we present in this section the tractability index concept, together with some ideas about the decoupling procedure supported on it and some projector-based results that will be useful in the computation of this index.

The characterization of the tractability index of a given DAE model is of major importance, not only because it paves the way for an appropriate numerical treatment in simulation but also because it reduces the description of the dynamical behavior to that of an inherent explicit ODE; this is performed by means of a decoupling of the different solution components [22, 27, 34]. An overview of how this decoupling is performed can be found below for linear time-invariant problems. Note that the tractability index has been already proved to be a very useful tool in circuit theory, especially regarding the analysis of modified nodal analysis models [16, 22, 26, 27, 41]. See also [17, 18, 28, 42]; related results can be found in [21, 25]. The discussion of the tractability index notion will be restricted to cases with index not greater than 2; this is due to the fact that the index of DAEs modeling a very large class of electrical and electronic circuits does not exceed 2 [16, 22, 26, 28]. This way we avoid certain difficulties exhibited in problems with arbitrary index.

In a linear time-invariant setting, several features of the DAE

$$Ax' + Bx = s(t) \quad (4)$$

can be analyzed in terms of the associated *matrix pencil* $\{A, B\}$ (cf. [36]). For time-varying and/or linearly implicit problems, the relation with matrix pencil theory is more involved [22, 29, 35]. In particular, the relation between the tractability index of (2) and the Weierstrass–Kronecker index of the matrix pencil $\{A(x^*), B(x^*)\}$ arising from the linearized problem were thoroughly examined in [30, 43, 44] (recent related results can be found in [34, 45]). In Section 4, we will make use of the fact that a matrix pencil $\{A, B\}$ with singular A is regular with Weierstrass–Kronecker index 1 (or, equivalently, with tractability index 1) if and only if the matrix $A_1 = A + BQ$ is non-singular, Q being any projector onto $\ker A$. Additionally, if A_1 is singular, the pencil can be shown to be regular with Weierstrass–Kronecker (and tractability) index 2 if and only if $A_2 = A_1 + B_1Q_1$ is non-singular, where Q_1 is any projector onto $\ker A_1$ and $B_1 = B(I - Q)$. The index analysis of the circuit model (1) will be crucially supported on these results.

The index 1 and index 2 notions introduced above for linear time-invariant DAEs allow for a relatively simple description of the decoupling procedure based on the projector framework. It is worth emphasizing that this procedure can be also performed for time-varying and/or nonlinear DAEs, including higher index problems, but the discussion is more cumbersome; the reader is referred to [27, 33, 34, 46, 47] for details in this direction. For a linear, time-invariant, index 1 DAE of the form (4), we can premultiply the equation by A_1^{-1} to obtain

$$A_1^{-1}Ax' + A_1^{-1}Bx = A_1^{-1}s(t).$$

Denoting $P = I - Q$ and writing $x = Px + Qx$, we obtain

$$A_1^{-1}Ax' + A_1^{-1}BPx + A_1^{-1}BQx = A_1^{-1}s(t),$$

which by means of the relations $A_1^{-1}A = P$ and $A_1^{-1}BQ = Q$ (cf. [22]) can be recast as

$$Px' + A_1^{-1}BPx + Qx = A_1^{-1}s(t).$$

Premultiplying this equation by P and Q , respectively, we obtain

$$Px' + PA_1^{-1}BPx = PA_1^{-1}s(t) \quad (5)$$

and

$$QA_1^{-1}BPx + Qx = QA_1^{-1}s(t). \quad (6)$$

By denoting $u = Px$, (5) reads as

$$u' + PA_1^{-1}Bu = PA_1^{-1}s(t), \quad (7)$$

which is an *inherent ODE* for which $\text{im } P$ is an invariant space. The solutions of (4) can be decoupled as $x(t) = u(t) + v(t)$, where u is a solution of (7) lying on the invariant space $\text{im } P$, and $v = Qx$ is explicitly given from (6) as

$$v = -QA_1^{-1}Bu + QA_1^{-1}s(t). \quad (8)$$

The importance of this procedure relies on the fact that it reduces the computation of the DAE solutions to the ‘classical’ setting of explicit ODEs, with the additional (explicit) algebraic relation (8).

In the index 2 setting, the decoupling is a bit more complicated; now, the solutions take the form $x(t) = u(t) + v_0(t) + v_1(t)$, where u is a solution of the inherent ODE

$$u' + PP_1A_2^{-1}BPu = PP_1A_2^{-1}s(t), \quad (9)$$

in the invariant space $\text{im } PP_1$ (with $P_1 = I - Q_1$), whereas v_1 and v_0 are given by

$$v_1 = -P_0Q_1A_2^{-1}Bu + P_0Q_1A_2^{-1}s(t), \quad (10a)$$

$$v_0 = -Q_0P_1A_2^{-1}Bu + Q_0Q_1P(Pv_1)' + Q_0P_1A_2^{-1}s(t). \quad (10b)$$

Details can be found in [22]. Again, this procedure reduces the problem to computing the solutions of an explicit ODE (namely (9)), with the additional solution components explicitly given by (10).

In nonlinear cases, this procedure applies locally, although the technical details are more complicated. We refer the reader to [27, 34, 46, 47] and to the forthcoming title [33] for details; for the sake of simplicity, we confine ourselves to presenting the tractability index notion for (2) in index ≤ 2 cases. Let us first remark that the kernel of $A(x)$ in (2) is constant, provided that the capacitance and inductance matrices $C(v_c)$ and $L(i_l)$ in (1) are non-singular. Letting $B(x)$ stand for the Jacobian matrix $-f'(x)$ (cf. (3)) and denoting by Q a constant projector onto $\ker A(x)$ (so that $Q^2 = Q$ with $\text{im } Q = \ker A(x)$), the DAE (2) has tractability index 1 if the matrix

$$A_1(x) = A(x) + B(x)Q \quad (11)$$

is non-singular.

Consider a setting in which $A_1(x)$ is rank-deficient everywhere, in a way such that there exists a continuous projector $Q_1(x)$ onto $\ker A_1(x)$ (forcing $A_1(x)$ to have a constant rank). Let $B_1(x)$ stand for the product $B(x)(I - Q)$. Basing on the special form of the circuit equations (cf. [27, Remark A.18]), system (2) will be said to have tractability index 2 if

$$A_2(x) = A_1(x) + B_1(x)Q_1(x) \quad (12)$$

is non-singular. This definition of the index is simpler than the one for general nonlinear DAEs [27, 34].

4. The index of branch-oriented models of memristive circuits

The main result of this paper is the tractability index characterization of branch-oriented circuit models stated in Theorem 1 below. From a mathematical point of view, the analysis will be based on the results compiled in Sections 2.1 and 3.

4.1. Index analysis of the branch-oriented model

In the proof of Theorem 1, we will make use of the following auxiliary result.

Lemma 3

Let A , C and D be matrices with dimensions $n \times m$, $m \times m$ and $m \times n$, respectively, and let I stand for the identity matrix of order n . Then, the matrix

$$\begin{pmatrix} A & I \\ C & D \end{pmatrix}$$

is non-singular if and only if $C - DA$ is non-singular.

This is a particular case of a *Schur reduction* [48] and can be understood as follows. Consider, in general, a matrix

$$\begin{pmatrix} A & B \\ C & D \end{pmatrix} \quad (13)$$

with A , C and D as above and B non-singular. The non-singularity of the matrix in (13) is equivalent to the unique solvability of the system

$$Ay + Bz = 0 \quad (14a)$$

$$Cy + Dz = 0, \quad (14b)$$

with $y \in \mathbb{R}^m$ and $z \in \mathbb{R}^n$. The non-singularity of B makes it possible to recast (14a) as $z = -B^{-1}Ay$, and the unique solvability of (14) amounts to that of $(C - DB^{-1}A)y = 0$. This means that the matrix in (13) is non-singular if and only if $C - DB^{-1}A$ is so. In particular, with $B = I$, we obtain Lemma 3.

In the statement of Theorem 1 below, a *VC-loop* stands for a loop defined just by voltage sources and/or capacitors, and an *IL-cutset* is a cutset including only current sources and/or inductors. To avoid any confusion in the proof of Theorem 1, recall that the matrices B and D always have $m - n + k$ and $n - k$ rows, respectively, where m , n and k are the numbers of branches, nodes and connected components (cf. subsection 2.1), and that the number of columns in the different blocks is always indicated by the subscript that specifies the type of device involved; for instance, the number of columns of D_c equals the number of capacitors, the number of columns of B_l is defined by the number of inductors and so on.

Theorem 1

Consider a well-posed circuit in which the capacitance and inductance matrices $C(v_c)$ and $L(i_l)$ are non-singular and the resistance and memristance matrices $R(i_r)$ and $M(q_m)$ are positive definite. The following assertions hold.

- The model (1) has tractability index 1 if and only if the circuit has neither VC-loops nor IL-cutsets.
- Suppose, additionally, that $C(v_c)$ and $L(i_l)$ are positive definite. In the presence of VC-loops and/or IL-cutsets, system (1) has tractability index 2.

Proof

The leading matrix $A(x)$ has the structure block-diag($C(v_c), L(i_l), I_m, 0$), whereas $B(x)$ can be written as

$$B(x) = \begin{pmatrix} 0 & 0 & 0 & -I_c & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & -I_l & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & -I_m & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{\partial M(q_m) i_m}{\partial q_m} & 0 & 0 & -M(q_m) & I_m & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & -R(i_r) & I_r & 0 & 0 \\ B_c & 0 & 0 & 0 & B_l & 0 & B_m & 0 & B_r & 0 & B_j \\ 0 & D_l & 0 & D_c & 0 & D_m & 0 & D_r & 0 & D_u & 0 \end{pmatrix}. \quad (15)$$

Note that we have changed the sign of (1d)–(1g) for notational simplicity. A projector Q onto $\ker A(x)$ with the structure block-diag($0, I$) produces a matrix $A_1(x) = A(x) + B(x)Q$ (cf. (11)) with the form

$$A_1(x) = \begin{pmatrix} C(v_c) & 0 & 0 & -I_c & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & L(i_l) & 0 & 0 & -I_l & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & I_m & 0 & 0 & -I_m & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & -M(q_m) & I_m & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & -R(i_r) & I_r & 0 & 0 \\ 0 & 0 & 0 & 0 & B_l & 0 & B_m & 0 & B_r & 0 & B_j \\ 0 & 0 & 0 & D_c & 0 & D_m & 0 & D_r & 0 & D_u & 0 \end{pmatrix}. \quad (16)$$

Proof of Theorem 1(i).

System (1) is index 1 if and only if matrix (16) is non-singular, a condition that relies on the non-singularity of

$$\begin{pmatrix} 0 & 0 & -M(q_m) & I_m & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & -R(i_r) & I_r & 0 & 0 & 0 \\ 0 & B_l & 0 & B_m & 0 & B_r & 0 & B_j & 0 \\ D_c & 0 & D_m & 0 & D_r & 0 & D_u & 0 & 0 \end{pmatrix}. \quad (17)$$

Using Lemma 3, it is not difficult to check that this matrix is non-singular if and only if

$$\begin{pmatrix} 0 & B_l & B_m M(q_m) & B_r R(i_r) & 0 & B_j \\ D_c & 0 & D_m & D_r & D_u & 0 \end{pmatrix} \quad (18)$$

is non-singular. In order to prove the index 1 claim, we then need to show that (18) is non-singular if and only if the circuit has neither VC-loops nor IL-cutsets. Clearly, this is a necessary condition, because otherwise according to Lemma 1 (items (b) and (e)), either $(D_c \ D_u)$ or $(B_l \ B_j)$ would not have a full column rank. \square

Conversely, assume that there are neither VC-loops nor IL-cutsets and suppose that a vector $(x^T \ y^T)$ belongs to the left kernel of (18), that is, suppose that

$$y^T D_c = 0 \quad (19a)$$

$$x^T B_l = 0 \quad (19b)$$

$$x^T B_m M(q_m) + y^T D_m = 0 \quad (19c)$$

$$x^T B_r R(i_r) + y^T D_r = 0 \quad (19d)$$

$$y^T D_u = 0 \quad (19e)$$

$$x^T B_j = 0. \quad (19f)$$

At this point, we make use of the identity

$$B_c D_c^T + B_l D_l^T + B_m D_m^T + B_r D_r^T + B_u D_u^T + B_j D_j^T = 0, \quad (20)$$

which follows from Lemma 2. Multiplying (20) from the left by x^T and from the right by y and using (19a), (19b), (19e) and (19f), we obtain

$$x^T B_m D_m^T y + x^T B_r D_r^T y = 0.$$

Use (19c) and (19d) to replace $D_m^T y$ and $D_r^T y$ and take the transpose to obtain

$$x^T B_m M(q_m) B_m^T x + x^T B_r R(i_r) B_r^T x = 0. \quad (21)$$

Because M and R are positive definite, we conclude that

$$x^T B_m = 0 \quad (22a)$$

$$x^T B_r = 0. \quad (22b)$$

The relations depicted in (19b), (19f), (22a) and (22b), together with the equivalence of items (d) and (f) in Lemma 1 and the absence of VC-loops, imply that $x = 0$.

Similarly, the insertion of (22a) and (22b) into (19c) and (19d) leads to

$$y^T D_m = 0 \quad (23a)$$

$$y^T D_r = 0 \quad (23b)$$

which, together with (19a) and (19e), the equivalence of items (a) and (c) in Lemma 1 and the absence of IL-cutsets, yield $y = 0$. This means that (18) is indeed non-singular and, hence, that (1) is index 1 in the absence of VC-loops and IL-cutsets.

Proof of Theorem 1(ii).

Assume now that the circuit displays VC-loops and/or IL-cutsets. Because of items (b) and (e) of Lemma 1, this implies that $(D_c \ D_u)$ and/or $(B_l \ B_j)$ do not have full column rank, making (17)—and hence the A_1 matrix in (16)—singular. \square

We denote by \hat{Q} a projector onto $\ker(D_c \ D_u)$. Note that $\hat{Q} = 0$ in the absence of VC-loops. Analogously, \tilde{Q} will stand for a projector onto $\ker(B_l \ B_j)$, with $\tilde{Q} = 0$ in problems without IL-cutsets; keep in mind, however, that in the setting of item (ii), both projectors cannot vanish simultaneously. Splitting \hat{Q} and \tilde{Q} in the form

$$\hat{Q} = \begin{pmatrix} \hat{Q}_{11} & \hat{Q}_{12} \\ \hat{Q}_{21} & \hat{Q}_{22} \end{pmatrix}, \quad \tilde{Q} = \begin{pmatrix} \tilde{Q}_{11} & \tilde{Q}_{12} \\ \tilde{Q}_{21} & \tilde{Q}_{22} \end{pmatrix}, \quad (24)$$

a projector onto $A_1(x)$ can be checked to be

$$Q_1 = \begin{pmatrix} 0 & 0 & 0 & C^{-1}\hat{Q}_{11} & 0 & 0 & 0 & 0 & 0 & C^{-1}\hat{Q}_{12} & 0 \\ 0 & 0 & 0 & 0 & L^{-1}\tilde{Q}_{11} & 0 & 0 & 0 & 0 & 0 & L^{-1}\tilde{Q}_{12} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \hat{Q}_{11} & 0 & 0 & 0 & 0 & 0 & \hat{Q}_{12} & 0 \\ 0 & 0 & 0 & 0 & \tilde{Q}_{11} & 0 & 0 & 0 & 0 & 0 & \tilde{Q}_{12} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \hat{Q}_{21} & 0 & 0 & 0 & 0 & 0 & \hat{Q}_{22} & 0 \\ 0 & 0 & 0 & 0 & \tilde{Q}_{21} & 0 & 0 & 0 & 0 & 0 & \tilde{Q}_{22} \end{pmatrix}. \quad (25)$$

Some easy computations show that the matrix $A_2(x)$ (cf. (12)) has the expression

$$\begin{pmatrix} C(v_c) & 0 & 0 & -I_c & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & L(i_l) & 0 & 0 & -I_l & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & I_m & 0 & 0 & -I_m & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & -M(q_m) & I_m & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & -R(i_r) & I_r & 0 & 0 \\ 0 & 0 & 0 & B_c C^{-1} \hat{Q}_{11} & B_l & 0 & B_m & 0 & B_r & B_c C^{-1} \hat{Q}_{12} & B_j \\ 0 & 0 & 0 & D_c & D_l L^{-1} \tilde{Q}_{11} & D_m & 0 & D_r & 0 & D_u & D_l L^{-1} \tilde{Q}_{12} \end{pmatrix},$$

and so it is non-singular if the following matrix is non-singular:

$$\begin{pmatrix} 0 & 0 & -M(q_m) & I_m & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & -R(i_r) & I_r & 0 & 0 \\ B_c C^{-1} \hat{Q}_{11} & B_l & 0 & B_m & 0 & B_r & B_c C^{-1} \hat{Q}_{12} & B_j \\ D_c & D_l L^{-1} \tilde{Q}_{11} & D_m & 0 & D_r & 0 & D_u & D_l L^{-1} \tilde{Q}_{12} \end{pmatrix}.$$

Using again Lemma 3, this matrix is non-singular if and only if

$$\begin{pmatrix} B_c C^{-1} \hat{Q}_{11} & B_l & B_m M(q_m) & B_r R(i_r) & B_c C^{-1} \hat{Q}_{12} & B_j \\ D_c & D_l L^{-1} \tilde{Q}_{11} & D_m & D_r & D_u & D_l L^{-1} \tilde{Q}_{12} \end{pmatrix} \quad (26)$$

is non-singular. Premultiplying (26) by $(x^T \ y^T)$, we obtain the identities

$$x^T B_c C^{-1} \hat{Q}_{11} + y^T D_c = 0 \quad (27a)$$

$$x^T B_l + y^T D_l L^{-1} \tilde{Q}_{11} = 0 \quad (27b)$$

$$x^T B_m M(q_m) + y^T D_m = 0 \quad (27c)$$

$$x^T B_r R(i_r) + y^T D_r = 0 \quad (27d)$$

$$x^T B_c C^{-1} \hat{Q}_{12} + y^T D_u = 0 \quad (27e)$$

$$x^T B_j + y^T D_l L^{-1} \tilde{Q}_{12} = 0, \quad (27f)$$

and we need to show that the unique solution to this system is $x = 0, y = 0$.

Multiply (27a) by \hat{Q}_{11} and (27e) by \hat{Q}_{21} ; adding up the resulting relations, we obtain

$$x^T B_c C^{-1} \hat{Q}_{11} = 0, \quad (28)$$

where we have used the identities $\hat{Q}_{11} \hat{Q}_{11} + \hat{Q}_{12} \hat{Q}_{21} = \hat{Q}_{11}$ and $D_c \hat{Q}_{11} + D_u \hat{Q}_{21} = 0$ that result from the definition of \hat{Q} as a projector onto $\ker(D_c \ D_u)$. From (27a) and (28), it follows that

$$y^T D_c = 0. \quad (29)$$

Proceeding in exactly the same manner with the projectors \hat{Q}_{12} and \hat{Q}_{22} instead of \hat{Q}_{11} and \hat{Q}_{21} , we derive

$$x^T B_c C^{-1} \hat{Q}_{12} = 0 \quad (30)$$

and then

$$y^T D_u = 0. \quad (31)$$

Analogously, working with the projector \tilde{Q} onto $\ker(B_l \ B_j)$, from (27b) and (27f), we obtain

$$x^T B_l = 0 \quad (32)$$

$$x^T B_j = 0. \quad (33)$$

Be aware of the fact that identity (20) is still valid in this setting. Multiplying (20) from the left by x^T and from the right by y and using (27c), (27d), (29), (31), (32) and (33), we now derive

$$x^T B_m M(q_m)^T B_m^T x + x^T B_r R(i_r)^T B_r^T x = 0. \quad (34)$$

Because of the positive definite nature of M and R , this implies that

$$x^T B_m = 0 \quad (35)$$

$$x^T B_r = 0, \quad (36)$$

and in the light of (27c) and (27d),

$$y^T D_m = 0 \quad (37)$$

$$y^T D_r = 0. \quad (38)$$

It still remains to show that the identities $x^T B_c = 0$ and $y^T D_l = 0$ hold true. Premultiplying (20) by x^T and using the relations (32), (33), (35) and (36), it follows that

$$x^T B_c D_c^T + x^T B_u D_u^T = 0.$$

This means that

$$\begin{pmatrix} B_c^T \\ B_u^T \end{pmatrix} x \in \ker(D_c D_u),$$

and because \hat{Q} is a projector onto $\ker(D_c D_u)$ and vectors on $\text{im } \hat{Q}$ remain invariant, this yields

$$\hat{Q} \begin{pmatrix} B_c^T \\ B_u^T \end{pmatrix} x = \begin{pmatrix} B_c^T \\ B_u^T \end{pmatrix} x,$$

in particular

$$\hat{Q}_{11} B_c^T x + \hat{Q}_{12} B_u^T x = B_c^T x. \quad (39)$$

Now, multiplying (28) and (30) by $B_c^T x$ and $B_u^T x$, respectively, and summing up the result, we obtain in the light of (39)

$$x^T B_c C^{-1} B_c^T x = 0,$$

which implies that

$$x^T B_c = 0, \quad (40)$$

because of the positive definiteness assumption on C , which makes C^{-1} positive definite as well.

In exactly the same manner, we may show that the identity

$$y^T D_l = 0 \quad (41)$$

holds because of the positive definite nature of the inductance matrix L .

Finally, the relations (32), (33), (35), (36) and (40), together with the absence of V-loops in well-posed circuits, yield, using items (d) and (f) of Lemma 1, the identity $x = 0$. The relation $y = 0$ follows analogously from (29), (31), (37), (38) and (41), the absence of I-cutsets and items (a) and (c) of Lemma 1. This completes the proof. \square

Theorem 1 extends to the context of memristive circuits the index characterization of nodal models of classical circuits discussed in [16, 26]. Note, however, that the use of a branch-oriented approach, which avoids the introduction of node potentials in the model, requires the use of different graph-theoretic techniques. The present characterization is shown below to hold even without a restriction on the controlling variables for resistors and memristors; in Section 4.3, it will also be shown to apply, in particular, to tree-based models.

4.2. Voltage-controlled resistors and flux-controlled memristors

In strictly passive problems, we can remove the assumption that resistors are current-controlled and memristors are charge-controlled, as shown in Corollary 1.

Corollary 1

The index characterization stated in Theorem 1 applies to circuits with both current-controlled and voltage-controlled resistors, as well as charge-controlled and flux-controlled memristors, provided that all of them are strictly passive.

Indeed, assume that the set of resistors includes both current-controlled and voltage-controlled ones. Use the subscripts 1 and 2 to distinguish both. Current-controlled resistors are governed by

$$v_{r_1} = \rho(i_{r_1}),$$

and the incremental resistance matrix is $R_1(i_{r_1}) = \rho'(i_{r_1})$. Analogously, voltage-controlled resistors are governed by

$$i_{r_2} = \gamma(v_{r_2}),$$

and the incremental conductance matrix is $G_2(v_{r_2}) = \gamma'(v_{r_2})$. The only change in the proof of Theorem 1 involves the block $(-R(i_r) \ I_r)$ in the $B(x)$ matrix (15), which must be split and rewritten in the form

$$\begin{pmatrix} -R_1 & 0 & I_{r_1} & 0 \\ 0 & I_{g_2} & 0 & -G_2 \end{pmatrix}.$$

However, denoting $R_2 = G_2^{-1}$ and premultiplying this block by the non-singular matrix

$$\begin{pmatrix} I_{r_1} & 0 \\ 0 & -R_2 \end{pmatrix},$$

an operation that does not affect the index, we confer the block to the form $(-R \ I)$, and the proof of Theorem 1 is valid because R is positive definite provided that they are R_1 and G_2 . The same reasoning applies in the presence of flux-controlled memristors.

4.3. Tree-based models

Theorem 1 provides, in particular, a characterization of the tractability index of tree-based circuit models. The choice of a tree gives the circuit equations the form

$$C(v_c)v'_c = i_c \quad (42a)$$

$$L(i_l)i'_l = v_l \quad (42b)$$

$$q'_m = i_m \quad (42c)$$

$$0 = v_m - M(q_m)i_m \quad (42d)$$

$$0 = v_r - \rho(i_r) \quad (42e)$$

$$0 = v_{co} + Fv_{tr} \quad (42f)$$

$$0 = i_{tr} - F^T i_{co}, \quad (42g)$$

where v_{co} and v_{tr} (resp. i_{co} and i_{tr}) stand for the link and twig voltages (resp. currents).

In practice, different settings lead to the choice of special trees; in the absence of VC-loops and IL-cutsets, the tree is usually a *proper* one, including all voltage sources and capacitors and neither current sources nor inductors. When VC-loops and/or IL-cutsets are present, it is common to work with a *normal* tree instead, that is, a tree including all voltage sources, the maximum possible number of capacitors, the minimum possible number of inductors and no current source. This stems from the work of Bashkow and Bryant [49–51] and allows for an explicit characterization of the order of complexity (namely the state dimension or dynamical degree of freedom) of the circuit.

Corollary 2

The index characterization in Theorem 1 also applies to the tree-based model (42), regardless of the actual choice of the tree.

This is a straightforward consequence of the fact that (42) is a particular instance of (1) with $B = (F \ I_{co})$ and $D = (I_{tr} \ -F^T)$. Note, incidentally, that the assumptions allowing for the choice of a proper tree correspond to those in the index 1 case considered in item (i) of Theorem 1, whereas the normal tree framework is accommodated in the index 2 context of item (ii).

5. Concluding remarks

In this paper, we have characterized the tractability index of the so-called branch-oriented models of electrical and electronic circuits including memristors. Our approach is based on the use of certain graph-theoretic properties and also on several results coming from projector theory, matrix analysis and matrix pencil theory. The present framework applies under strict passivity assumptions and accommodates in particular circuit models arising from the choice of a spanning tree. The results should be helpful in future analyses of the dynamics of memristive circuits, including qualitative and numerical aspects.

Acknowledgements

This paper was supported by Research Projects MTM2007-62064 of Ministerio de Educación y Ciencia, MTM2010-15102 of Ministerio de Ciencia e Innovación and CCG10-UPM/ESP-5236 of Comunidad de Madrid/UPM, Spain.

References

- Chua LO. Memristor—the missing circuit element. *IEEE Transactions on Circuit Theory* 1971; **18**:507–519.
- Chua LO, Kang SM. Memristive devices and systems. *Proceedings of the IEEE* 1976; **64**:209–223.
- Strukov DB, Snider GS, Stewart DR, Williams RS. The missing memristor found. *Nature* 2008; **453**:80–83.
- Bao B, Ma Z, Xu J, Liu Z, Xu Q. A simple memristor chaotic circuit with complex dynamics. *International Journal of Bifurcation and Chaos in Applied Sciences and Engineering* 2011; **21**:2629–2645.
- Itoh M, Chua LO. Memristor oscillators. *International Journal of Bifurcation and Chaos in Applied Sciences and Engineering* 2008; **18**:3183–3206.
- Itoh M, Chua LO. Memristor cellular automata and memristor discrete-time cellular neural networks. *International Journal of Bifurcation and Chaos in Applied Sciences and Engineering* 2009; **19**:3605–3656.
- Itoh M, Chua LO. Memristor Hamiltonian circuits. *International Journal of Bifurcation and Chaos in Applied Sciences and Engineering* 2011; **21**:2395–2425.
- Messias M, Nespole C, Botta VA. Hopf bifurcation from lines of equilibria without parameters in memristors oscillators. *International Journal of Bifurcation and Chaos in Applied Sciences and Engineering* 2010; **20**:437–450.
- Muthuswamy B. Implementing memristor based chaotic circuits. *International Journal of Bifurcation and Chaos in Applied Sciences and Engineering* 2010; **20**:1335–1350.
- Muthuswamy B, Chua LO. Simplest chaotic circuit. *International Journal of Bifurcation and Chaos in Applied Sciences and Engineering* 2010; **20**:1567–1580.
- Pershin YV, Di Ventra M. Memory effects in complex materials and nanoscale systems. *Advances in Physics* 2011; **60**:145–227.
- Riaza R. Nondegeneracy conditions for active memristive circuits. *IEEE Transactions on Circuits and Systems - II Express Briefs* 2010; **57**:223–227.

13. Riaza R. Explicit ODE reduction of memristive systems. *International Journal of Bifurcation and Chaos in Applied Sciences and Engineering* 2011; **21**:917–930.
14. Riaza R, Tischendorf C. Semistate models of electrical circuits including memristors. *International Journal of Circuit Theory and Applications* 2011; **39**:607–627.
15. Yang JJ, Pickett MD, Li X, Ohlberg DAA, Stewart DR, Williams RS. Memristive switching mechanism for metal/oxide/metal nanodevices. *Nature Nanotechnology* 2008; **3**:429–433.
16. Estévez-Schwarz D, Tischendorf C. Structural analysis of electric circuits and consequences for MNA. *International Journal of Circuit Theory and Applications* 2000; **28**:131–162.
17. Günther M, Feldmann U. CAD-based electric-circuit modeling in industry. I: Mathematical structure and index of network equations. *Surveys on Mathematics for Industry* 1999; **8**:97–129.
18. Günther M, Feldmann U. CAD-based electric-circuit modeling in industry. II: Impact of circuit configurations and parameters. *Surveys on Mathematics for Industry* 1999; **8**:131–157.
19. Hasler M, Neirynck J. *Nonlinear Circuits*. Artech House: Boston, 1986.
20. Iwata S, Takamatsu M, Tischendorf C. Tractability index of hybrid equations for circuit simulation. *Mathematics of Computation* 2012; **81**:923–939.
21. Reis T. Circuit synthesis of passive descriptor systems—a modified nodal approach. *International Journal of Circuit Theory and Applications* 2010; **38**:44–68.
22. Riaza R. *Differential-Algebraic Systems. Analytical Aspects and Circuit Applications*. World Scientific: Singapore, 2008.
23. Riaza R, Tischendorf C. The hyperbolicity problem in electrical circuit theory. *Mathematical Methods in the Applied Sciences* 2010; **33**:2037–2049.
24. Riaza R, Tischendorf C. Structural characterization of classical and memristive circuits with purely imaginary eigenvalues. *International Journal of Circuit Theory and Applications* 2011. in press.
25. Takamatsu M, Iwata S. Index characterization of differential-algebraic equations in hybrid analysis for circuit simulation. *International Journal of Circuit Theory and Applications* 2010; **38**:419–440.
26. Tischendorf C. Topological index calculation of DAEs in circuit simulation. *Surveys on Mathematics for Industry* 1999; **8**:187–199.
27. Tischendorf C. *Coupled Systems of Differential Algebraic and Partial Differential Equations in Circuit and Device Simulation, Modeling and Numerical Analysis*. Habilitationsschrift, Humboldt-Univ: Berlin, 2003.
28. Reisz G. The index of the standard circuit equations of passive RLCTG-networks does not exceed 2. *Proceedings of the 1998 IEEE International Symposium on Circuits and Systems, 1998 (ISCAS'98)* 1998; **3**:419–422.
29. Brenan KE, Campbell SL, Petzold LR. *Numerical Solution of Initial-Value Problems in Differential-Algebraic Equations*. SIAM: Philadelphia, 1996.
30. Griepentrog E, März R. *Differential-Algebraic Equations and Their Numerical Treatment*, Teubner-Texte zur Mathematik 88. Leipzig: Leipzig, 1986.
31. Hairer E, Wanner G. *Solving Ordinary Differential Equations II: Stiff and Differential-Algebraic Problems*. Springer-Verlag: Berlin, 1996.
32. Kunkel P, Mehrmann V. *Differential-Algebraic Equations. Analysis and Numerical Solution*. EMS: Zurich, 2006.
33. Lamour R, März R, Tischendorf C. *Differential-Algebraic Equations: A Projector Based Analysis*: Springer, 2012. (in press).
34. März R. Differential algebraic equations anew. *Applied Numerical Mathematics* 2002; **42**:315–335.
35. Rabier PJ, Rheinboldt WC. Theoretical and numerical analysis of differential-algebraic equations. In *Handbook of Numerical Analysis*, Vol. VIII. North-Holland: Amsterdam, 2002.
36. Gantmacher FR. *The Theory of Matrices*, vols. 1 & 2. AMS Chelsea: New York, 1959.
37. Foulds LR. *Graph Theory Applications*. Springer: Berlin, 1992.
38. Bollobás B. *Modern Graph Theory*. Springer-Verlag: Berlin, 1998.
39. Chua LO, Desoer CA, Kuh ES. *Linear and Nonlinear Circuits*. McGraw-Hill: New York, 1987.
40. Vlach J, Singhal K. *Computer Methods for Circuits Analysis and Design*. Van Nostrand Reinhold ITP: New York, 1983.
41. März R. Differential algebraic systems with properly stated leading term and MNA equations. In *Modeling, Simulation, and Optimization of Integrated Circuits* (Oberwolfach, 2001). *International Series of Numerical Mathematics* 2003; **146**:135–151.
42. Riaza R. Graph-theoretic characterization of bifurcation phenomena in electrical circuit dynamics. *International Journal of Bifurcation and Chaos in Applied Sciences and Engineering* 2010; **20**:451–465.
43. Griepentrog E, März R. Basic properties of some differential-algebraic equations. *Zeitschrift für Analysis und ihre Anwendungen* 1989; **8**:25–40.
44. März R. *A Matrix Chain for Analyzing Differential Algebraic Equations*. Inst. Math., Humboldt University: Berlin, 1987. Preprint 162.
45. März R. The index of linear differential algebraic equations with properly stated leading terms. *Results in Mathematics* 2002; **42**:308–338.
46. Balla K, März R. A unified approach to linear differential-algebraic equations and their adjoint equations. *Zeitschrift für Analysis und ihre Anwendungen* 2002; **21**:783–802.
47. Higuera I, März R. Differential algebraic equations with properly stated leading terms. *Computers and Mathematics with Applications* 2004; **48**:215–235.
48. Horn RA, Johnson C R. *Matrix Analysis*. Cambridge Univ. Press: Cambridge, 1985.
49. Bashkow TR. The A matrix, new network description. *IRE Transactions on Circuit Theory* 1957; **4**:117–119.
50. Bryant PR. The order of complexity of electrical networks. *Proceedings of the IEE, Part C* 1959; **106**:174–188.
51. Bryant PR. The explicit form of Bashkow's A matrix. *IRE Transactions on Circuit Theory* 1962; **9**:303–306.