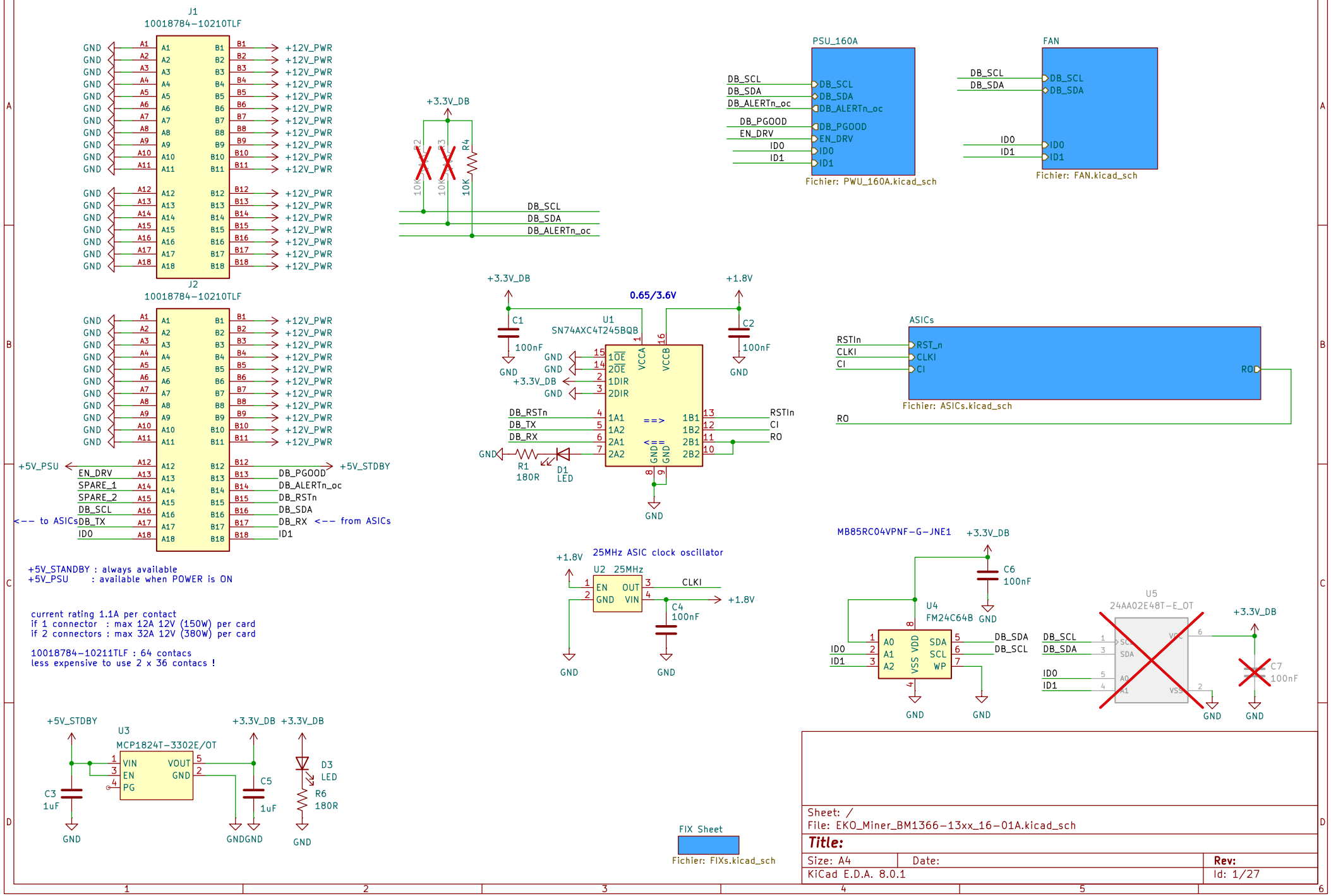
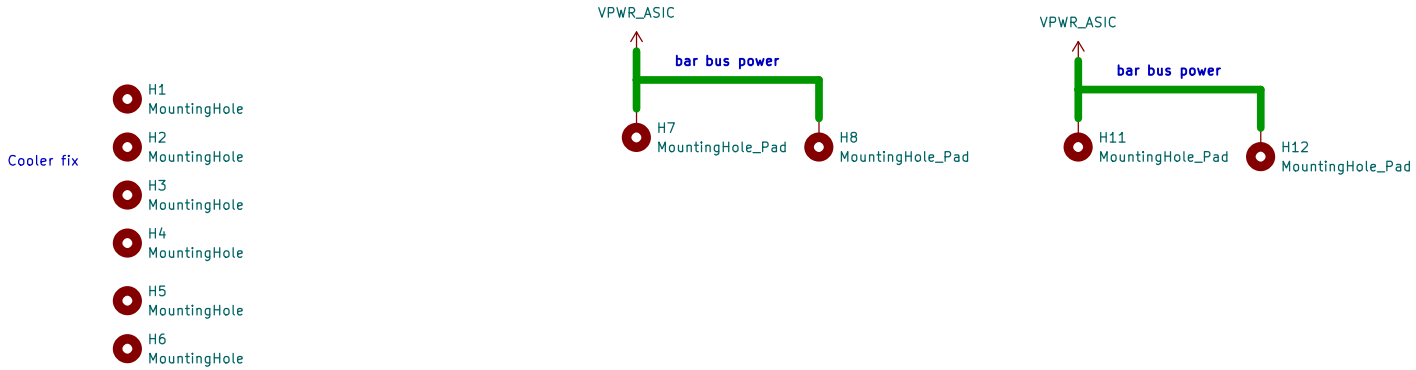

J1
10018784-10210TLF
J2
10018784-10210TLF
+12V_PWR
GND
+5V_PSU
+5V_STDBY
EN_DRV
SPARE_1
SPARE_2
DB_SCL
DB_TX
IDO
DB_PGOOD
DB_ALERTn_oc
DB_RSTn
DB_SDA
DB_RX
ID1
<-- to ASICs
<-- from ASICs
+5V_STANDBY : always available
+5V_PSU : available when POWER is ON
current rating 1.1A per contact
if 1 connector : max 12A 12V (150W) per card
if 2 connectors : max 32A 12V (380W) per card
10018784-10211TLF : 64 contacs
less expensive to use 2 x 36 contacs !
+3.3V_DB
R2
R3
R4
10K
DB_SCL
DB_SDA
DB_ALERTn_oc
PSU_160A
DB_PGOOD
EN_DRV
IDO
ID1
Fichier: PWU_160A.kicad_sch
FAN
Fichier: FAN.kicad_sch
+1.8V
0.65/3.6V
U1
SN74AXC4T245BQB
C1
C2
100nF
GND
DB_RSTn
DB_TX
DB_RX
RSTIn
CI
RO
R1
180R
D1
LED
ASICs
RSTIn
CLKI
CI
RO
Fichier: ASICs.kicad_sch
25MHz ASIC clock oscillator
U2 25MHz
CLKI
C4
MB85RC04VPNF-G-JNE1
U4
FM24C64B
C6
U5
24AA02E48T-E_OT
C7
U3
MCP1824T-3302E/OT
VIN
VOUT
EN
PG
C3
1uF
C5
D3
LED
R6
180R
FIX Sheet
Fichier: FIXs.kicad_sch
Sheet: /
File: EKO_Miner_BM1366-13xx_16-01A.kicad_sch
Title:
Size: A4
Date:
Rev:
KiCad E.D.A. 8.0.1
Id: 1/27



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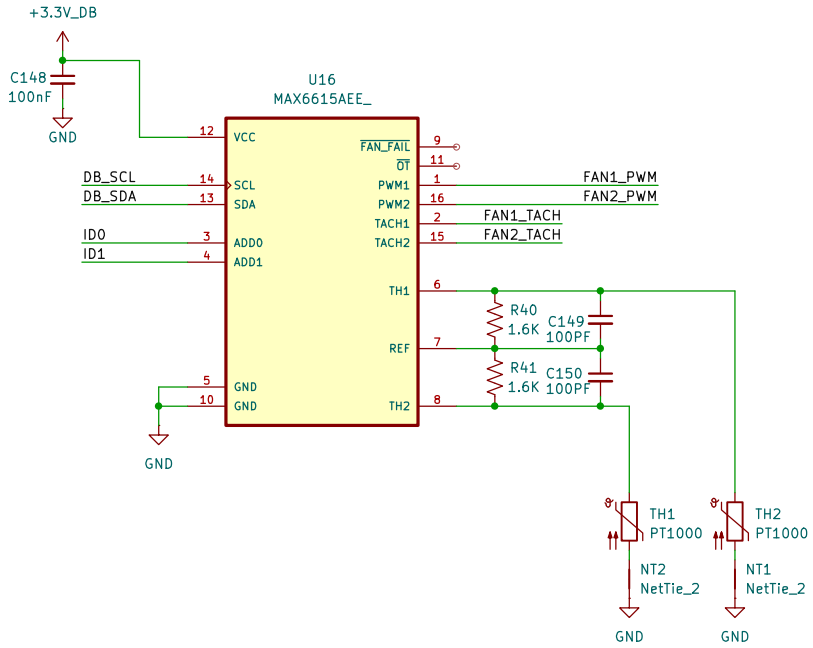
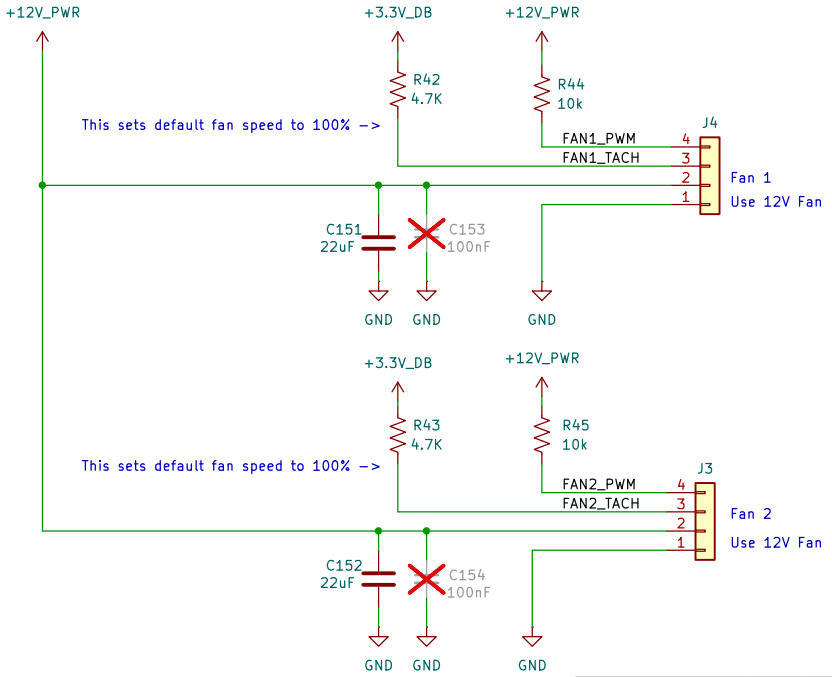
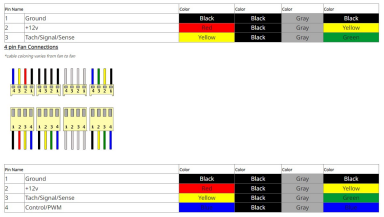
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. 8.0.1		Id: 2/27

MAX6615 : Dual-Channel Temperature Monitors and Fan-Speed Controllers with Thermistor Inputs

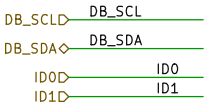
https://forum.hardware.fr/hfr/Hardware/carte-mere/besoin-comprendre-ventilateur-sujet_1027524_1.htm







https://landing.coolermaster.com/faq/3-pin-and-4-pin-fan-wire-diagrams/



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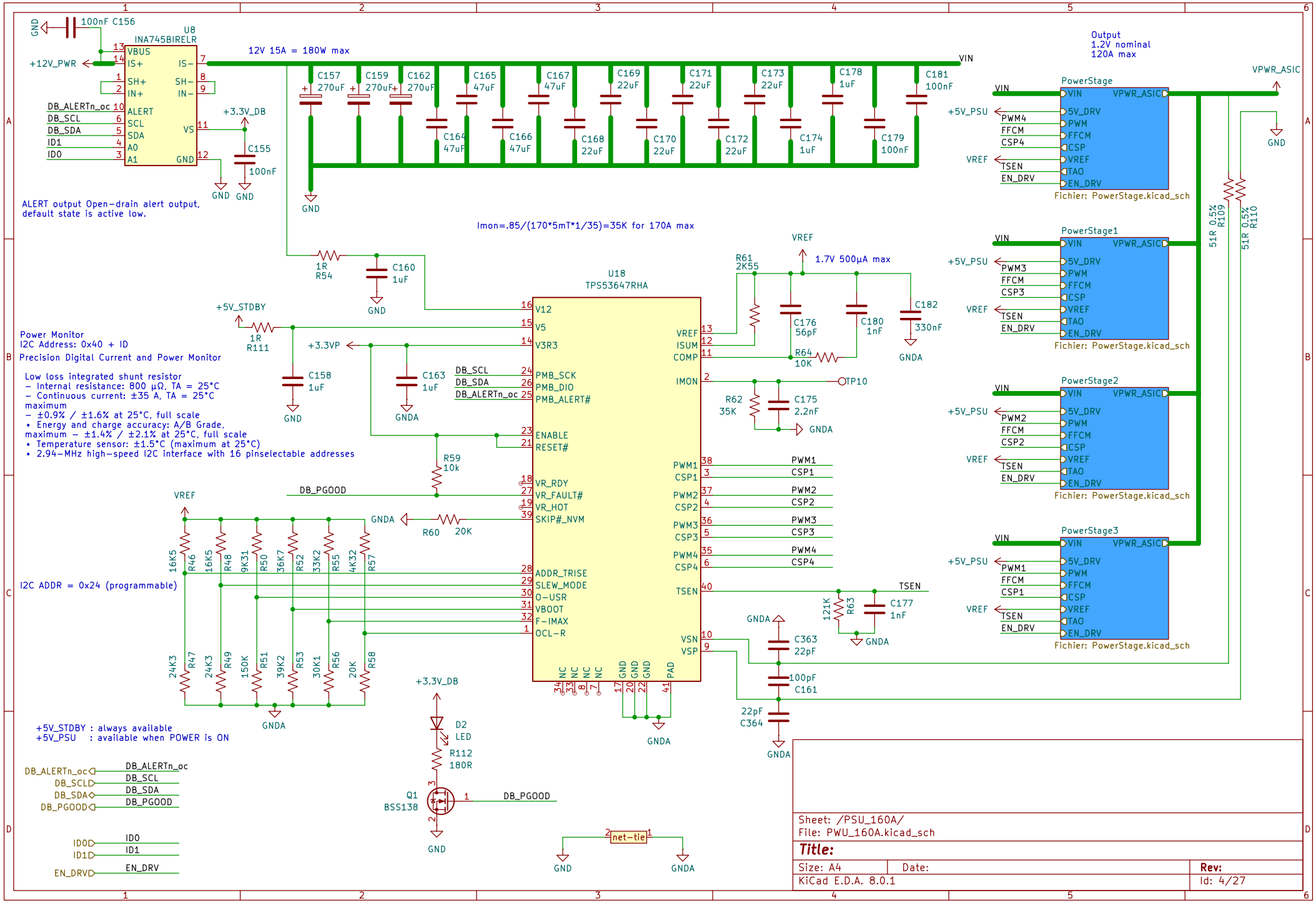
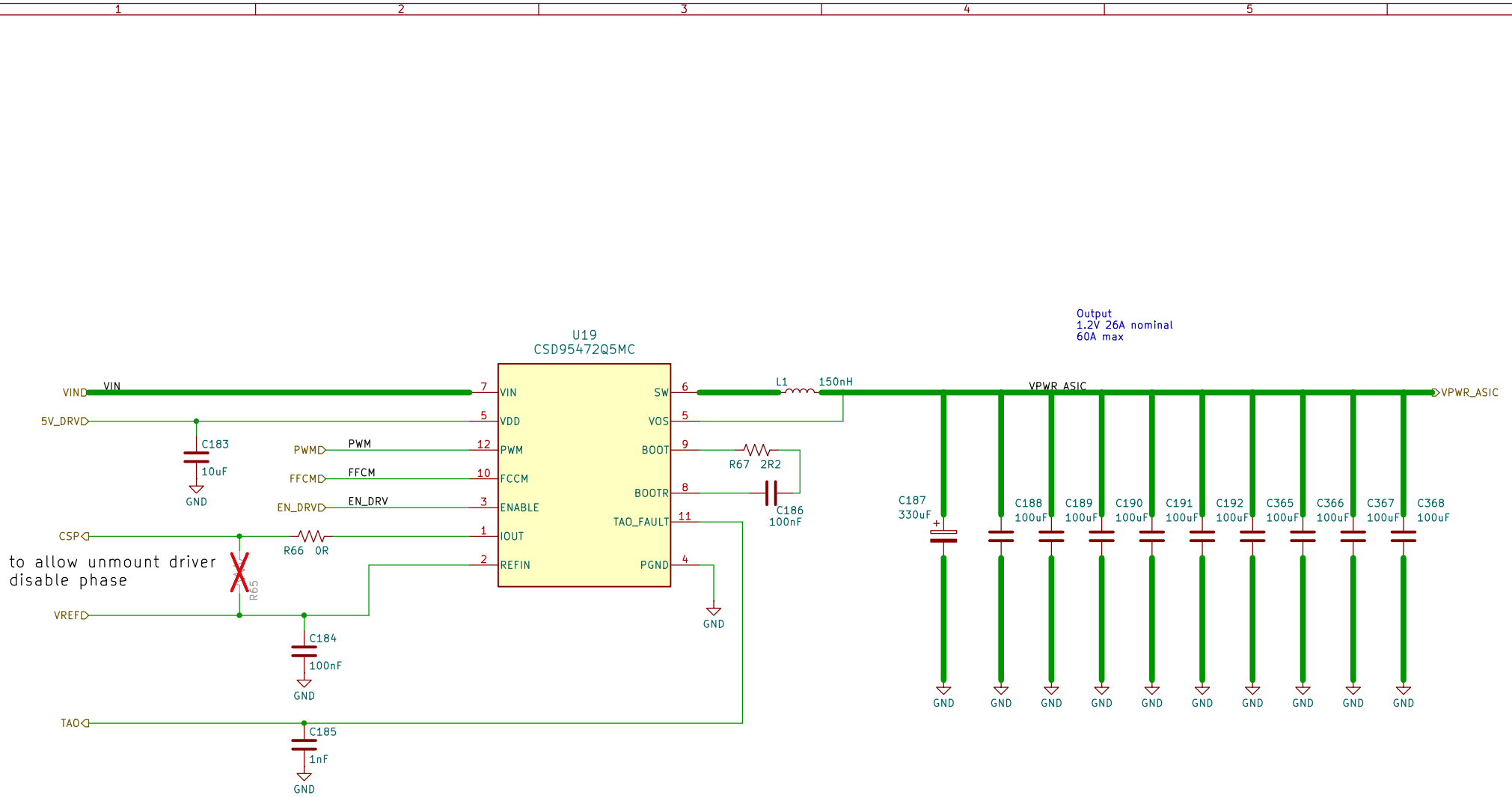
File: FAN.kicad_sch

Title:

Size: A4 | Date: | **Rev:**
KiCad E.D.A. 8.0.1 | Id: 3/27

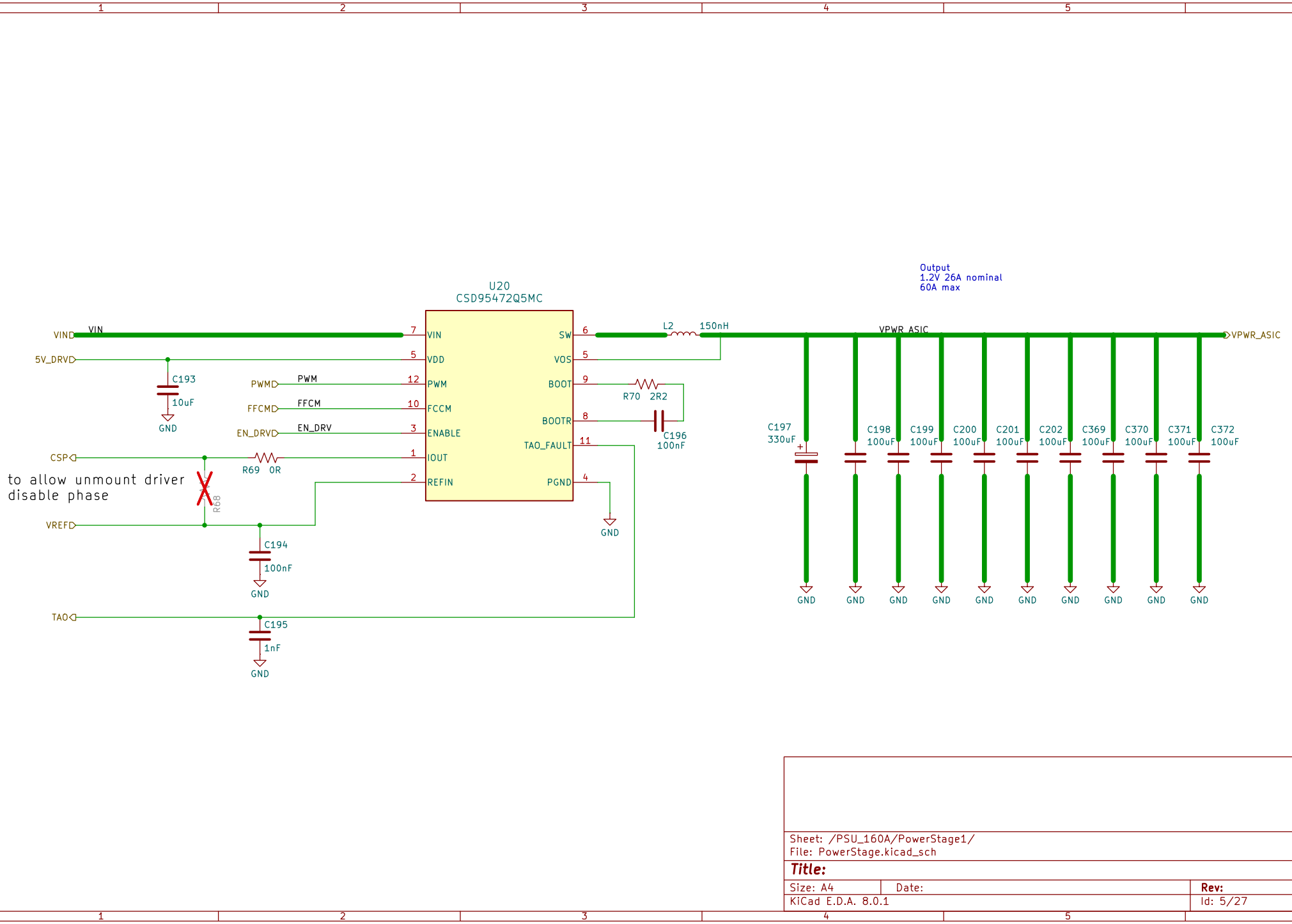

100nF C156
U8
INA745BIRELR
+12V_PWR
12V 15A = 180W max
VIN
Output
1.2V nominal
120A max
VPWR_ASIC
DB_ALERTn_oc
DB_SCL
DB_SDA
ID1
ID0
+3.3V_DB
C155
100nF
ALERT output Open-drain alert output,
default state is active low.
C157 270uF
C159 270uF
C162 270uF
C164 47uF
C165 47uF
C166 47uF
C167 47uF
C168 22uF
C169 22uF
C170 22uF
C171 22uF
C172 22uF
C173 22uF
C174 1uF
C178 1uF
C179 100nF
C181 100nF
PowerStage
PowerStage1
PowerStage2
PowerStage3
Fichier: PowerStage.kicad_sch
+5V_PSU
VREF
PWM4
FFCM
CSP4
TSEN
EN_DRV
51R 0.5% R109
51R 0.5% R110
Imon=.85/(170*5mT*1/35)=35K for 170A max
1R R54
C160 1uF
U18
TPS53647RHA
+5V_STDBY
1R R111
C158 1uF
+3.3VP
C163 1uF
Power Monitor
I2C Address: 0x40 + ID
Precision Digital Current and Power Monitor
Low loss integrated shunt resistor
– Internal resistance: 800 µΩ, TA = 25°C
– Continuous current: ±35 A, TA = 25°C maximum
– ±0.9% / ±1.6% at 25°C, full scale
• Energy and charge accuracy: A/B Grade, maximum – ±1.4% / ±2.1% at 25°C, full scale
• Temperature sensor: ±1.5°C (maximum at 25°C)
• 2.94-MHz high-speed I2C interface with 16 pinselectable addresses
R59 10k
DB_PGOOD
R60 20K
GNDA
R61 2K55
1.7V 500µA max
C176 56pF
C180 1nF
C182 330nF
R64 10K
TP10
R62 35K
C175 2.2nF
R63 121K
C177 1nF
C363 22pF
100pF C161
22pF C364
I2C ADDR = 0x24 (programmable)
16K5 R46
16K5 R48
9K31 R50
36K7 R52
33K2 R55
4K32 R57
24K3 R47
24K3 R49
150K R51
39K2 R53
30K1 R56
20K R58
+5V_STDBY : always available
+5V_PSU : available when POWER is ON
D2 LED
R112 180R
Q1 BSS138
net-tie
Sheet: /PSU_160A/
File: PWU_160A.kicad_sch
Title:
Size: A4
Date:
Rev:
KiCad E.D.A. 8.0.1
Id: 4/27



Sheet: /PSU_160A/PowerStage/
File: PowerStage.kicad_sch

Title:

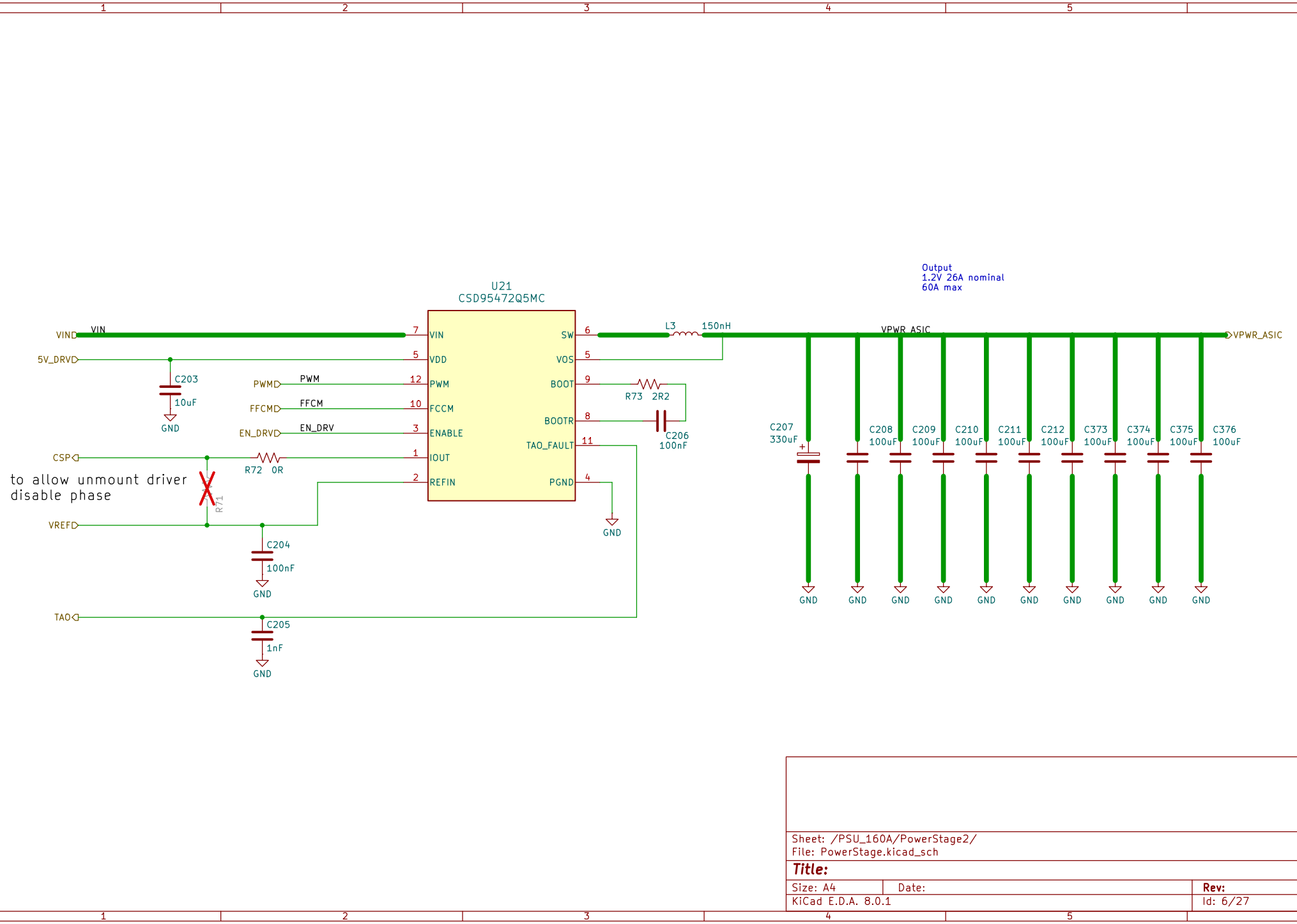
Size: A4	Date:	**Rev:**
KiCad E.D.A. 8.0.1		Id: 1/27



Sheet: /PSU_160A/PowerStage1/
File: PowerStage.kicad_sch

Title:

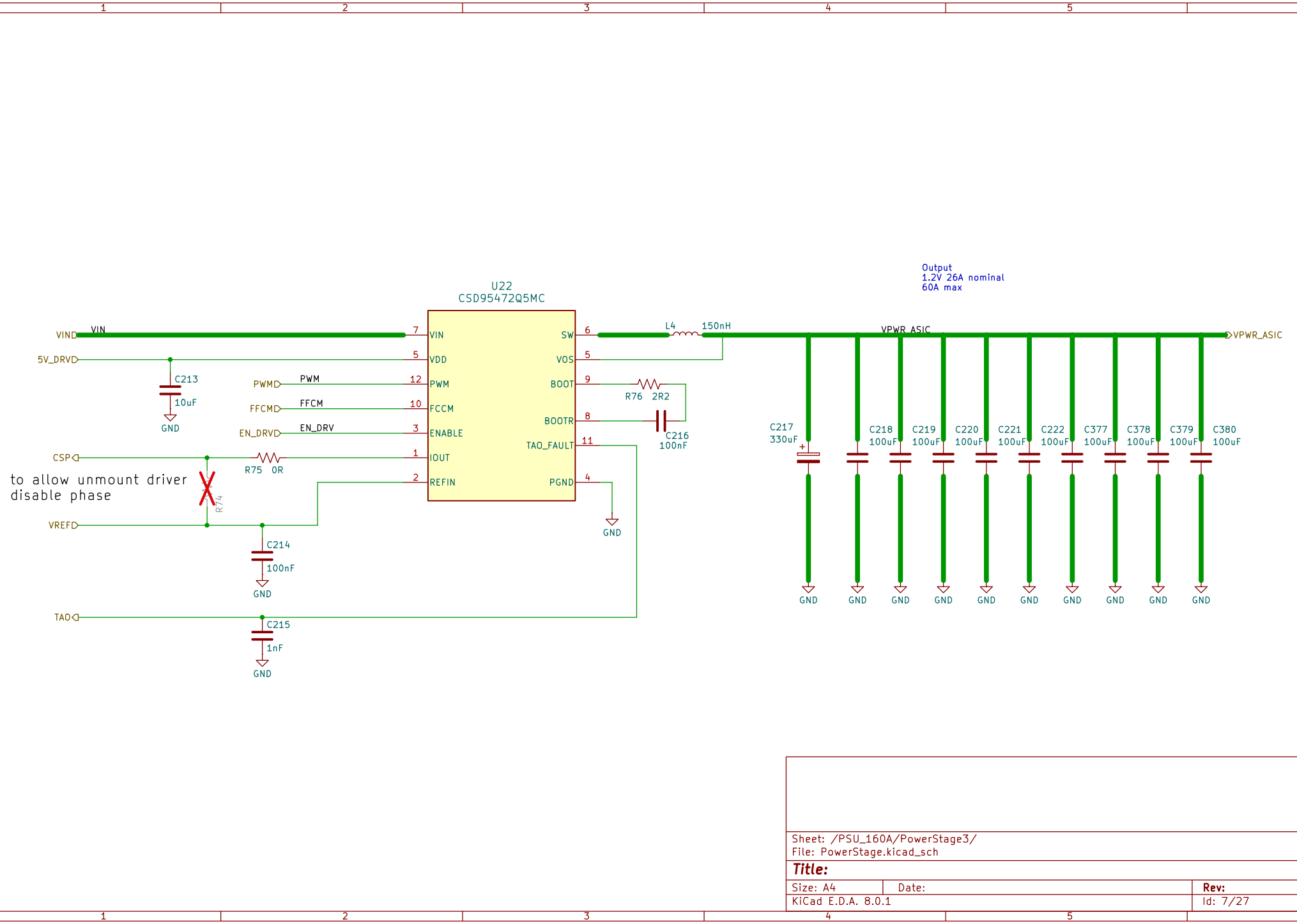
Size: A4	Date:	**Rev:**
KiCad E.D.A. 8.0.1		Id: 5/27

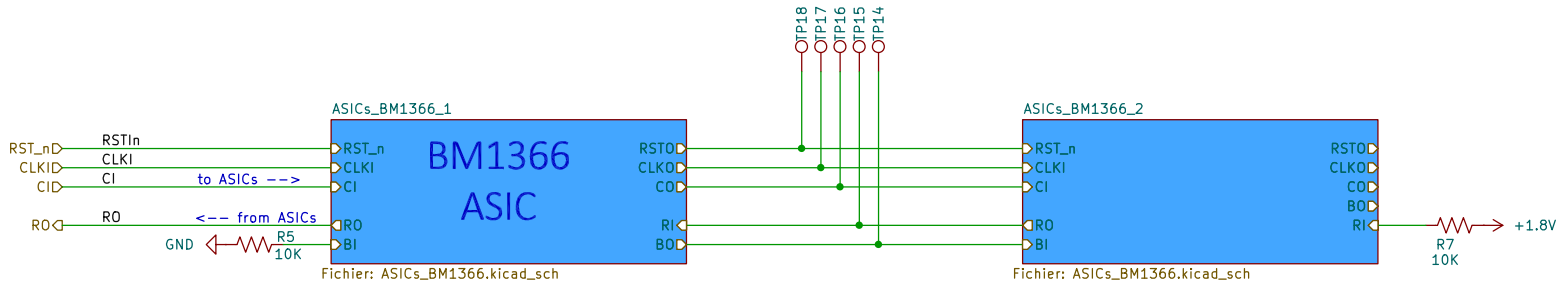


Sheet: /PSU_160A/PowerStage2/
File: PowerStage.kicad_sch

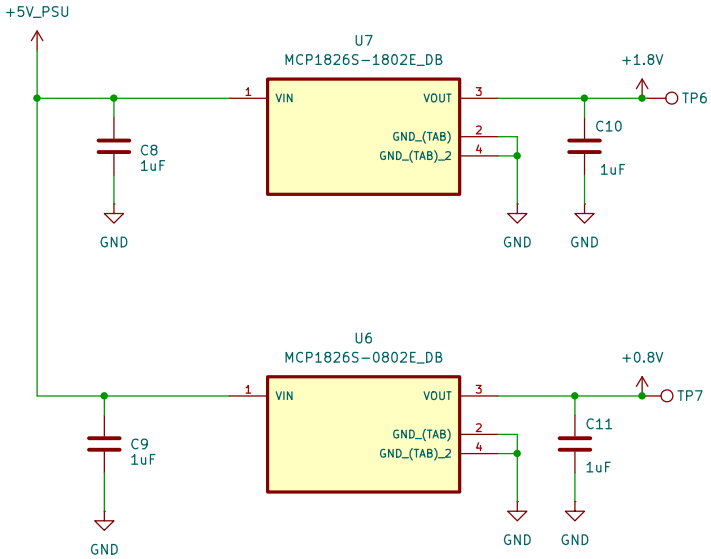
Title:

Size: A4 | Date: | **Rev:**
KiCad E.D.A. 8.0.1 | Id: 6/27


U22
CSD95472Q5MC
VIN
VIN
5V_DRVD
C213
10uF
GND
PWMD
PWM
FFCMD
FFCM
EN_DRVD
EN_DRV
CSP
R75 0R
to allow unmount driver
disable phase
R74
VREFD
C214
100nF
GND
TAO
C215
1nF
GND
7
VIN
5
VDD
12
PWM
10
FCCM
3
ENABLE
1
IOUT
2
REFIN
6
SW
5
VOS
9
BOOT
8
BOOTR
11
TAO_FAULT
4
PGND
GND
L4
150nH
R76 2R2
C216
100nF
VPWR_ASIC
Output
1.2V 26A nominal
60A max
VPWR_ASIC
C217
330uF
C218
100uF
C219
100uF
C220
100uF
C221
100uF
C222
100uF
C377
100uF
C378
100uF
C379
100uF
C380
100uF
GND
GND
GND
GND
GND
GND
GND
GND
GND
GND
Sheet: /PSU_160A/PowerStage3/
File: PowerStage.kicad_sch
Title:
Size: A4
Date:
Rev:
KiCad E.D.A. 8.0.1
Id: 7/27



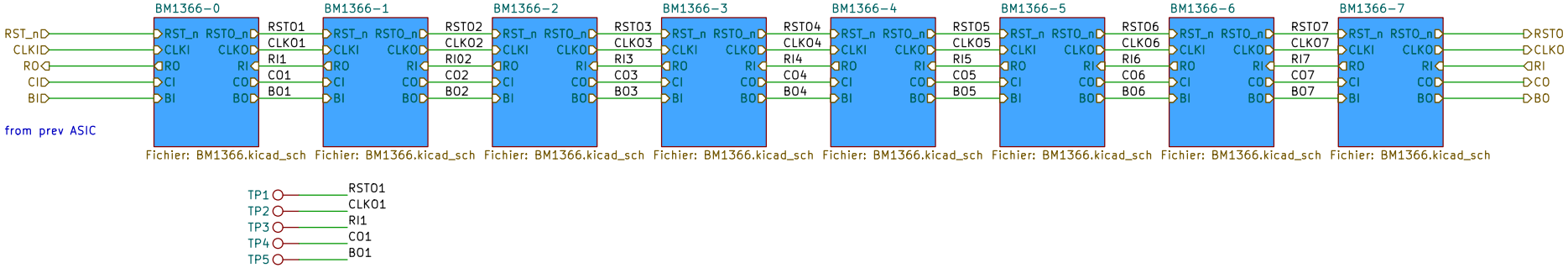
+5V_STDBY : always available
+5V_PSU : available when POWER is ON



Sheet: /ASICs/		
File: ASICs.kicad_sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. 8.0.1		Id: 1/27

voir BM1368 semble compatible pin2pin

radiateur 120x56
https://fr.aliexpress.com/item/1005001368115718.html?spm=a2g0o.productlist.main.41.70b261a4BdkxPV&algo_pvid=cb86c257-5408-49ff-b28b-a15697fb39bc&utparam-url=scene%3Asearch%7Cquery_from%3A
https://fr.aliexpress.com/item/32904595345.html?spm=a2g0o.productlist.main.23.70b261a4BdkxPV&algo_pvid=cb86c257-5408-49ff-b28b-a15697fb39bc&utparam-url=scene%3Asearch%7Cquery_from%3A



BM1380
First of all: the datasheet gives very little information about how this chip actually works
(I imagine that more detailed specification is available for those that buy these in large quantities).
Schematics of S1 reveal information about the functionality of certain pins.

Chips in S1 use UART for communication, settings are 115200, 8N1. Chips communicate within the chain using UART + flow control signals:

CI – Command Input <-> uplink's (like a control board, or so) TXD
RO – Response Output <-> uplink's RXD
CO – Command Ouput <-> connected to CI of the downlink (meaning: next chip in chain)
RI – Response Input <-> connected from downlink's RO

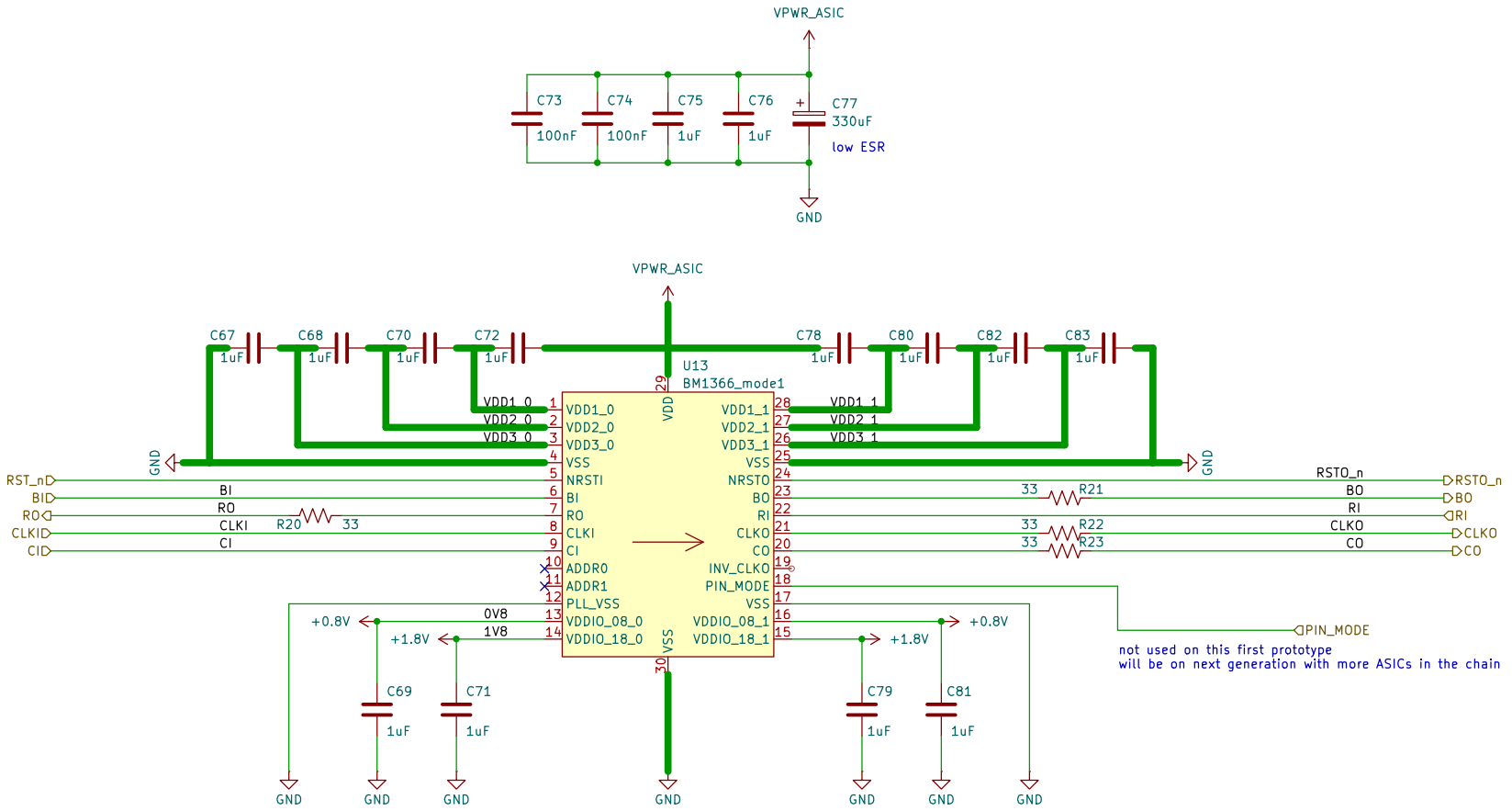
All of the chips are basically sharing the same UART "bus". Flow control/bus arbitration is done using BI (Busy Input)/BO (Busy Output) signals.
Chip that wants to send the data out activates it's Busy Output signal which mutes all chips that are placed further in chain.

Chips have addresses derived from the state of address pins ADDR[7:0] which also determine the MSB value of starting 'nonce'.
S1 has these equally spaced like 0x00, 0x08, 0x10 ... 0xf8, so that each chip covers different (and equal in size, 0x07FFFFFF) area of nocne value search.

Sheet: /ASICs/ASICs_BM1366_1/
File: ASICs_BM1366.kicad_sch

Title:

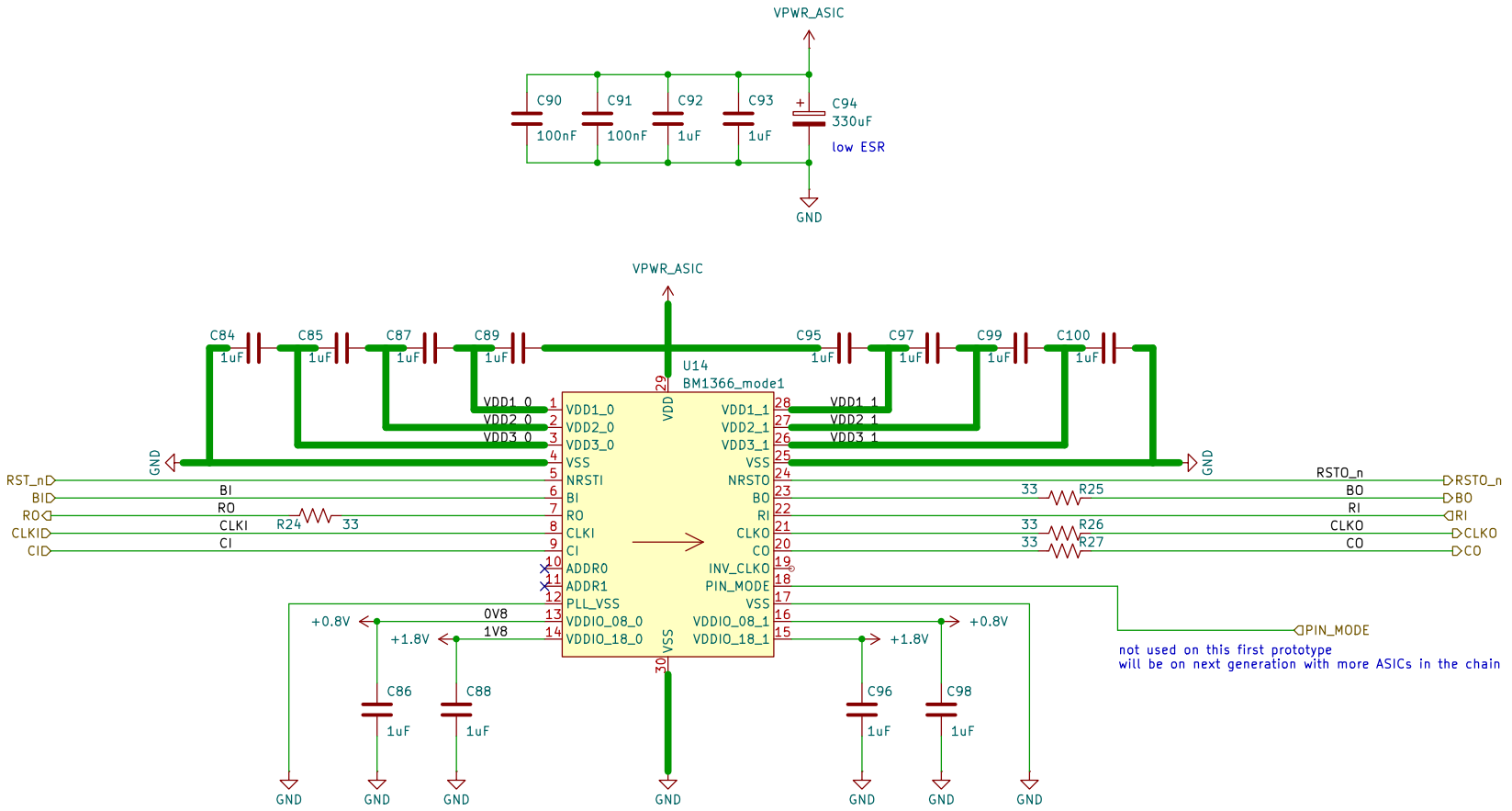
Size: A4	Date:	**Rev:**
KiCad E.D.A. 8.0.1		Id: 1/27



The 17e series I believe use a different chip, BM1396.
The S15 and S17/e chips (BM1391, BM1396, BM1397) are for the most part pin-compatible.
1396 and 1397 have one functional pin difference, but also a different core count and optimal voltage parameters.

The different modes are passing data left to right, or right to left.
There's a Mode pin which gets tied low for one mode, and left floating for the other.
This makes serial power and data in a single copper layer pretty simple to achieve.

Sheet: /ASICs/ASICs_BM1366_1/BM1366-0/		
File: BM1366.kicad_sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. 8.0.1		Id: 27/27



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Sheet: /ASICs/ASICs_BM1366_1/BM1366-1/		
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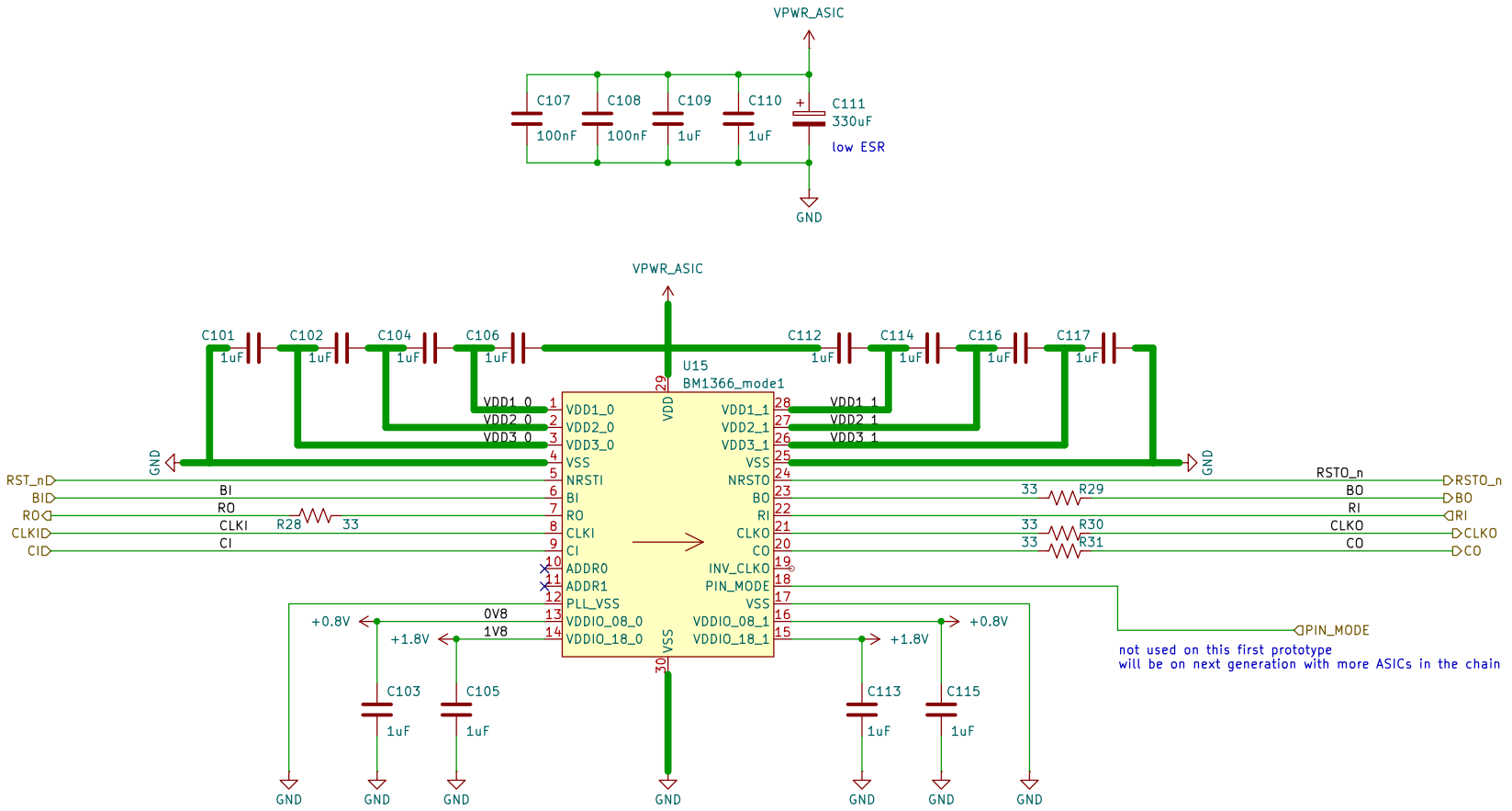
Size: A4	Date:	**Rev:**
KiCad E.D.A. 8.0.1		Id: 11/27



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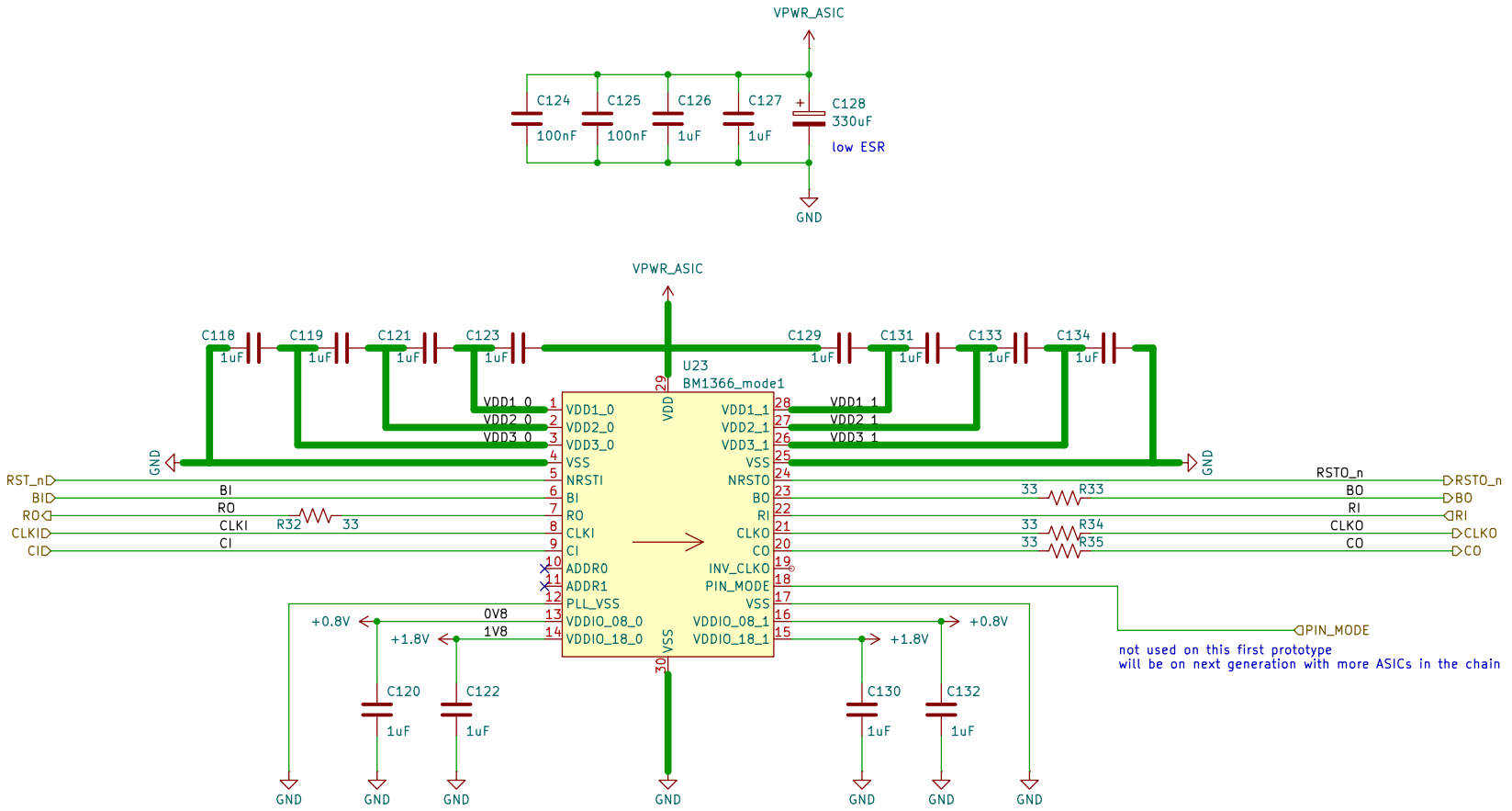
Sheet: /ASICs/ASICs_BM1366_1/BM1366-2/
File: BM1366.kicad_sch

Title:

Size: A4	Date:	**Rev:**
KiCad E.D.A. 8.0.1		Id: 12/27



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Sheet: /ASICs/ASICs_BM1366_1/BM1366-3/		
File: BM1366.kicad_sch		
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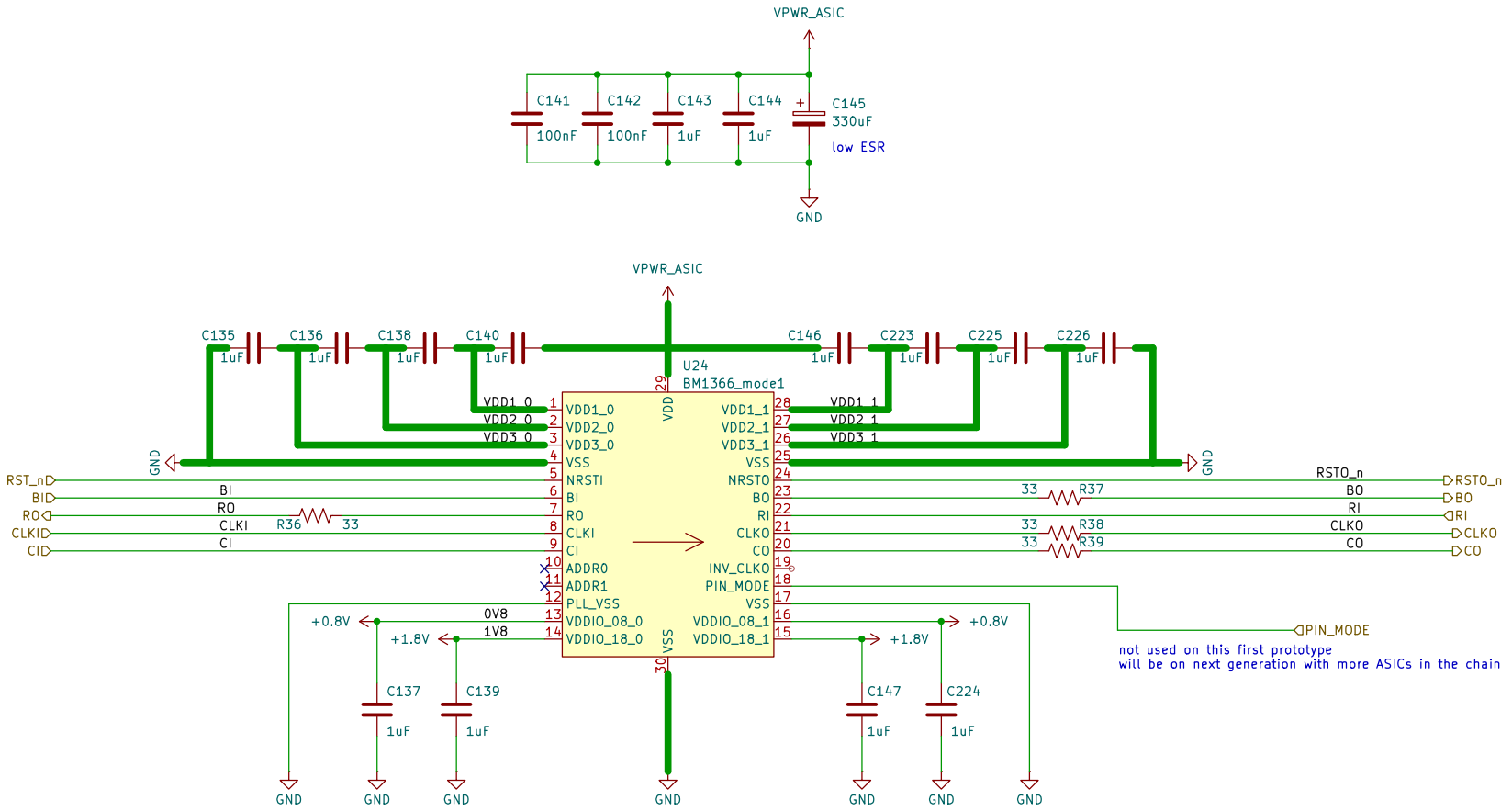
Size: A4	Date:	**Rev:**
KiCad E.D.A. 8.0.1		Id: 13/27



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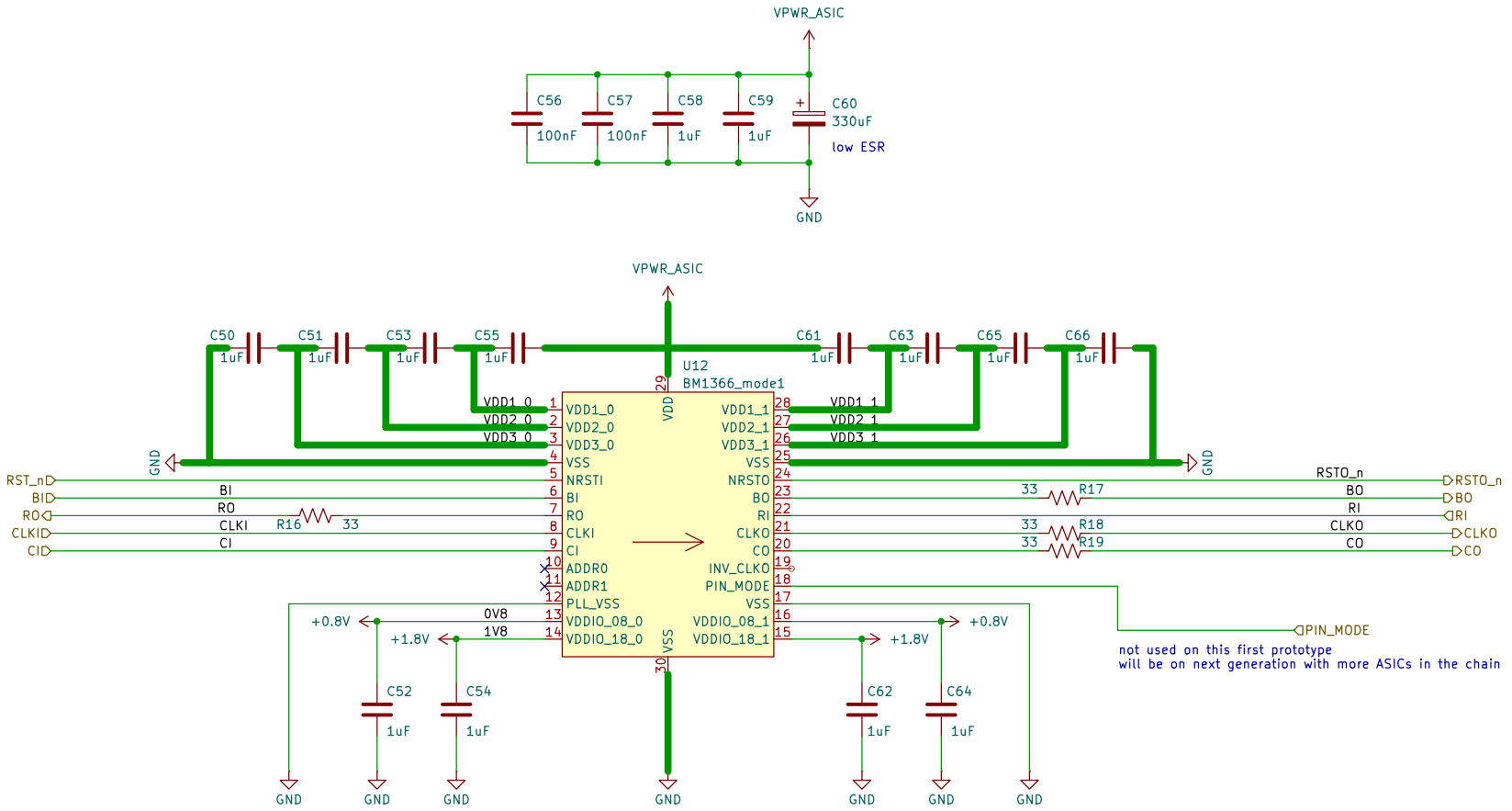
Sheet: /ASICs/ASICs_BM1366_1/BM1366-4/		
File: BM1366.kicad_sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. 8.0.1		Id: 14/27



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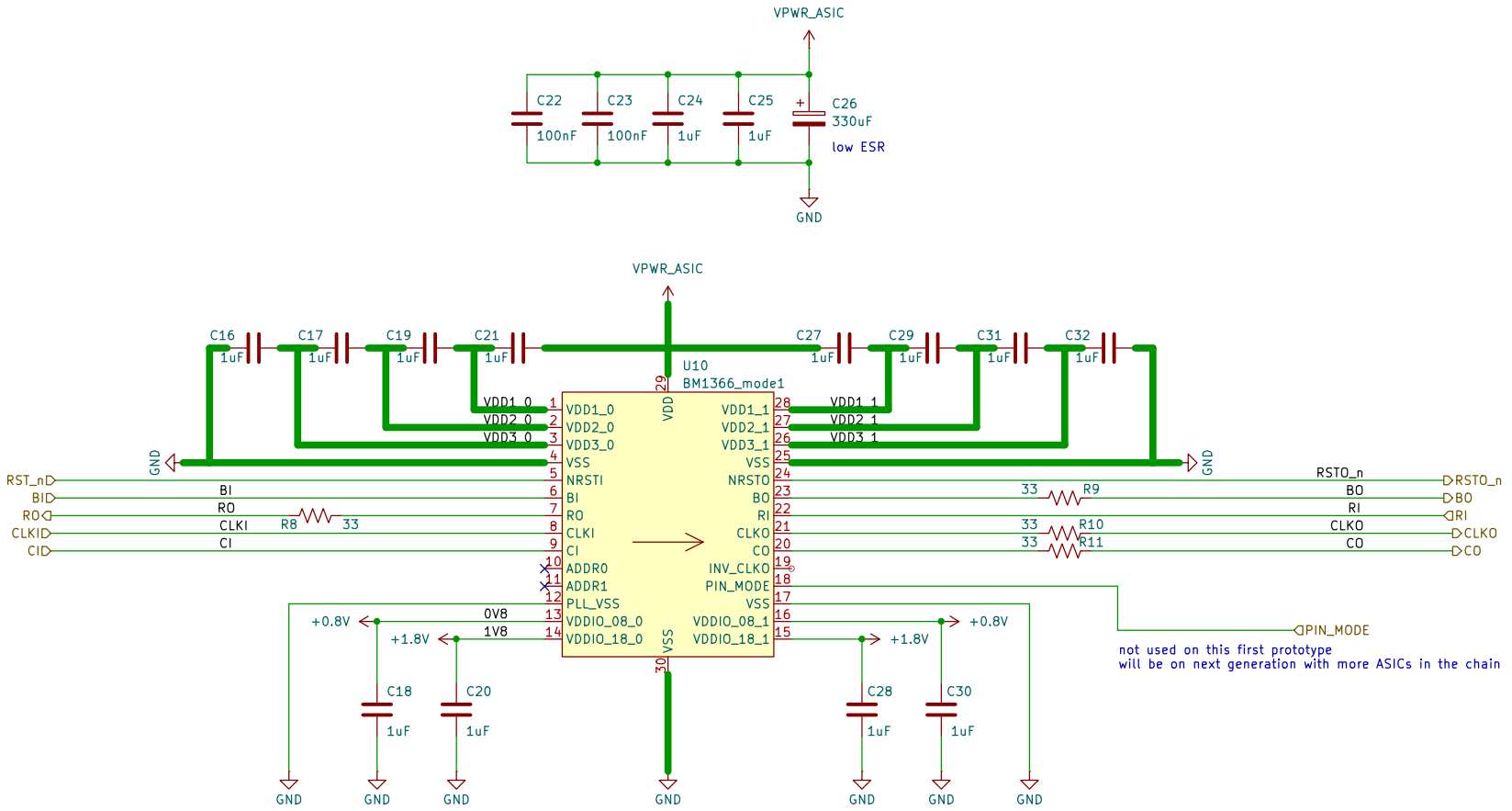
Sheet: /ASICs/ASICs_BM1366_1/BM1366-5/
File: BM1366.kicad_sch

Title:

Size: A4	Date:	**Rev:**
KiCad E.D.A. 8.0.1		Id: 15/27



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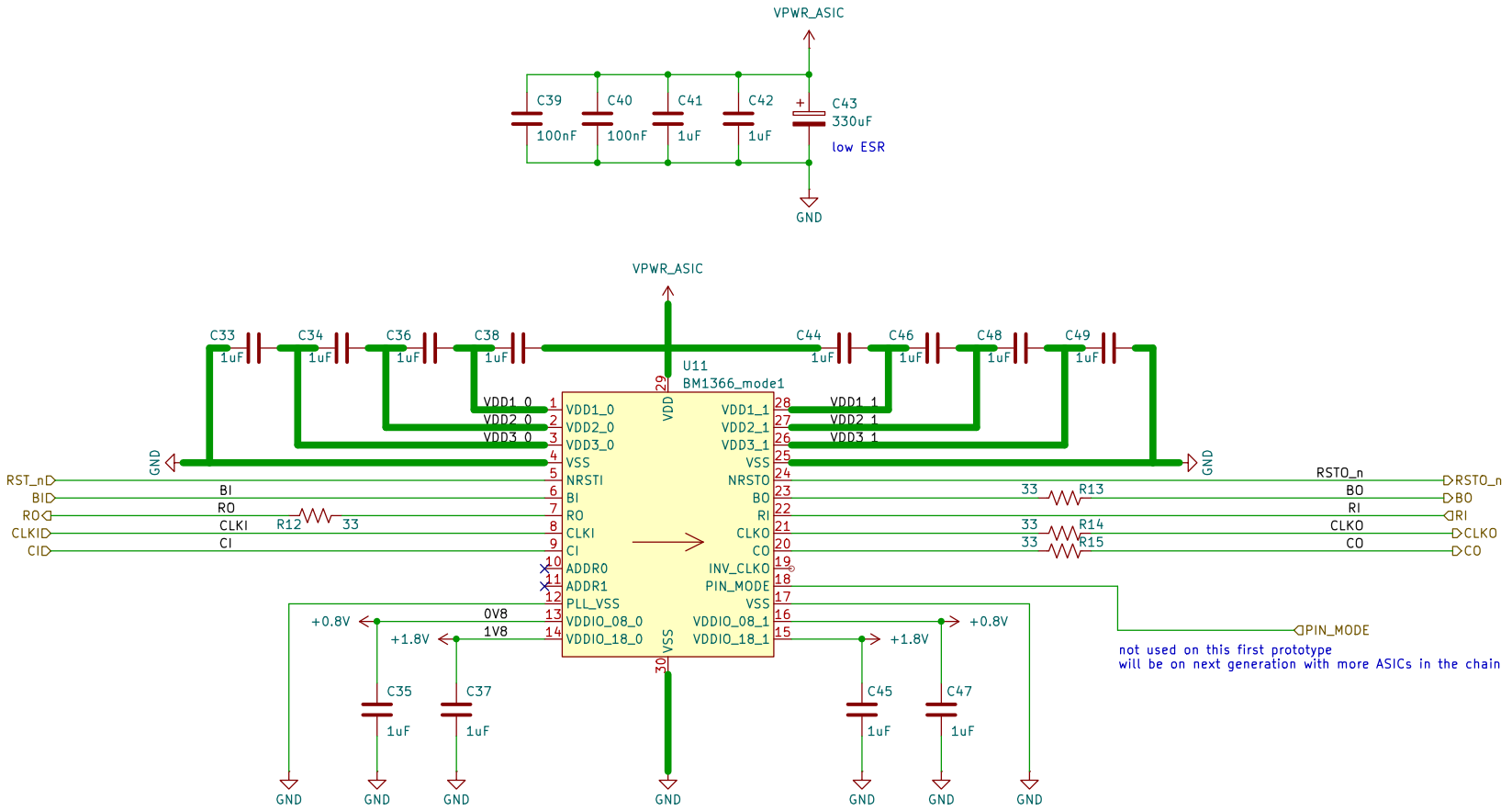
Sheet: /ASICs/ASICs_BM1366_1/BM1366-6/		
File: BM1366.kicad_sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. 8.0.1		Id: 16/27



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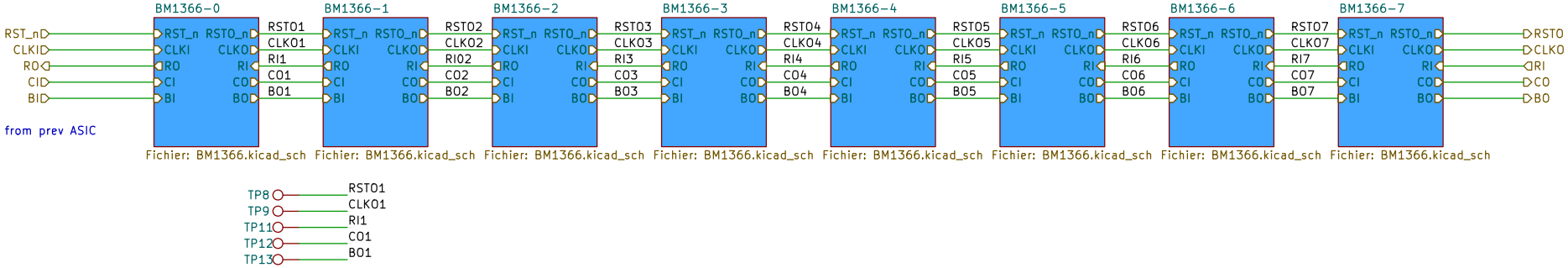
Sheet: /ASICs/ASICs_BM1366_1/BM1366-7/		
File: BM1366.kicad_sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. 8.0.1		Id: 17/27

voir BM1368 semble compatible pin2pin

radiateur 120x56
https://fr.aliexpress.com/item/1005001368115718.html?spm=a2g0o.productlist.main.41.70b261a4BdkxPV&algo_pvid=cb86c257-5408-49ff-b28b-a15697fb39bc&utparam-url=scene%3Asearch%7Cquery_from%3A
https://fr.aliexpress.com/item/32904595345.html?spm=a2g0o.productlist.main.23.70b261a4BdkxPV&algo_pvid=cb86c257-5408-49ff-b28b-a15697fb39bc&utparam-url=scene%3Asearch%7Cquery_from%3A



BM1380
First of all: the datasheet gives very little information about how this chip actually works
(I imagine that more detailed specification is available for those that buy these in large quantities).
Schematics of S1 reveal information about the functionality of certain pins.

Chips in S1 use UART for communication, settings are 115200, 8N1. Chips communicate within the chain using UART + flow control signals:

CI – Command Input <-> uplink's (like a control board, or so) TXD
RO – Response Output <-> uplink's RXD
CO – Command Ouput <-> connected to CI of the downlink (meaning: next chip in chain)
RI – Response Input <-> connected from downlink's RO

All of the chips are basically sharing the same UART "bus". Flow control/bus arbitration is done using BI (Busy Input)/BO (Busy Output) signals.
Chip that wants to send the data out activates it's Busy Output signal which mutes all chips that are placed further in chain.

Chips have addresses derived from the state of address pins ADDR[7:0] which also determine the MSB value of starting 'nonce'.
S1 has these equally spaced like 0x00, 0x08, 0x10 ... 0xf8, so that each chip covers different (and equal in size, 0x07FFFFFF) area of nocne value search.

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Size: A4	Date:	**Rev:**
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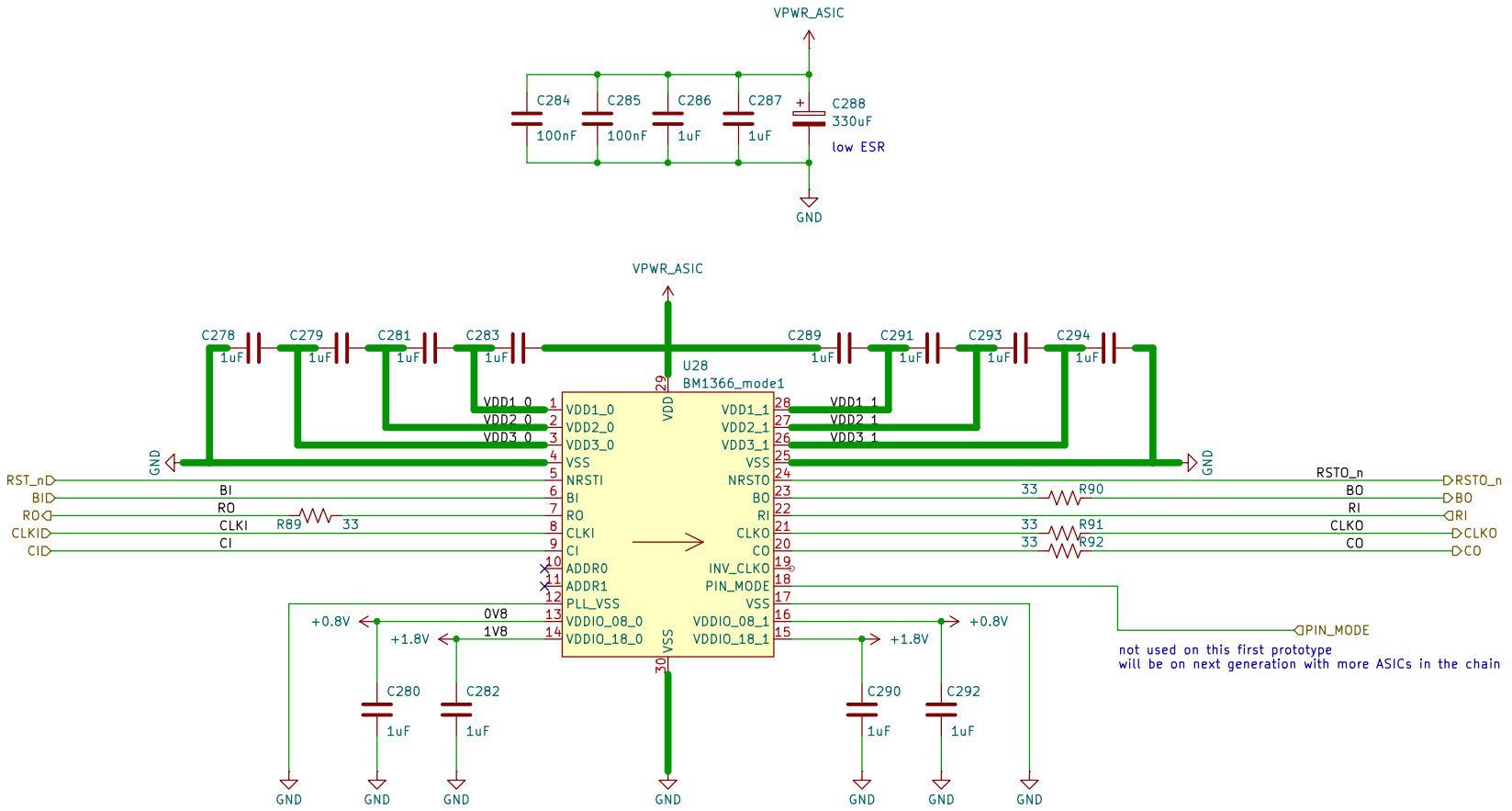

The 17e series I believe use a different chip, BM1396.
The S15 and S17/e chips (BM1391, BM1396, BM1397) are for the most part pin-compatible.
1396 and 1397 have one functional pin difference, but also a different core count and optimal voltage parameters.

The different modes are passing data left to right, or right to left.
There's a Mode pin which gets tied low for one mode, and left floating for the other.
This makes serial power and data in a single copper layer pretty simple to achieve.

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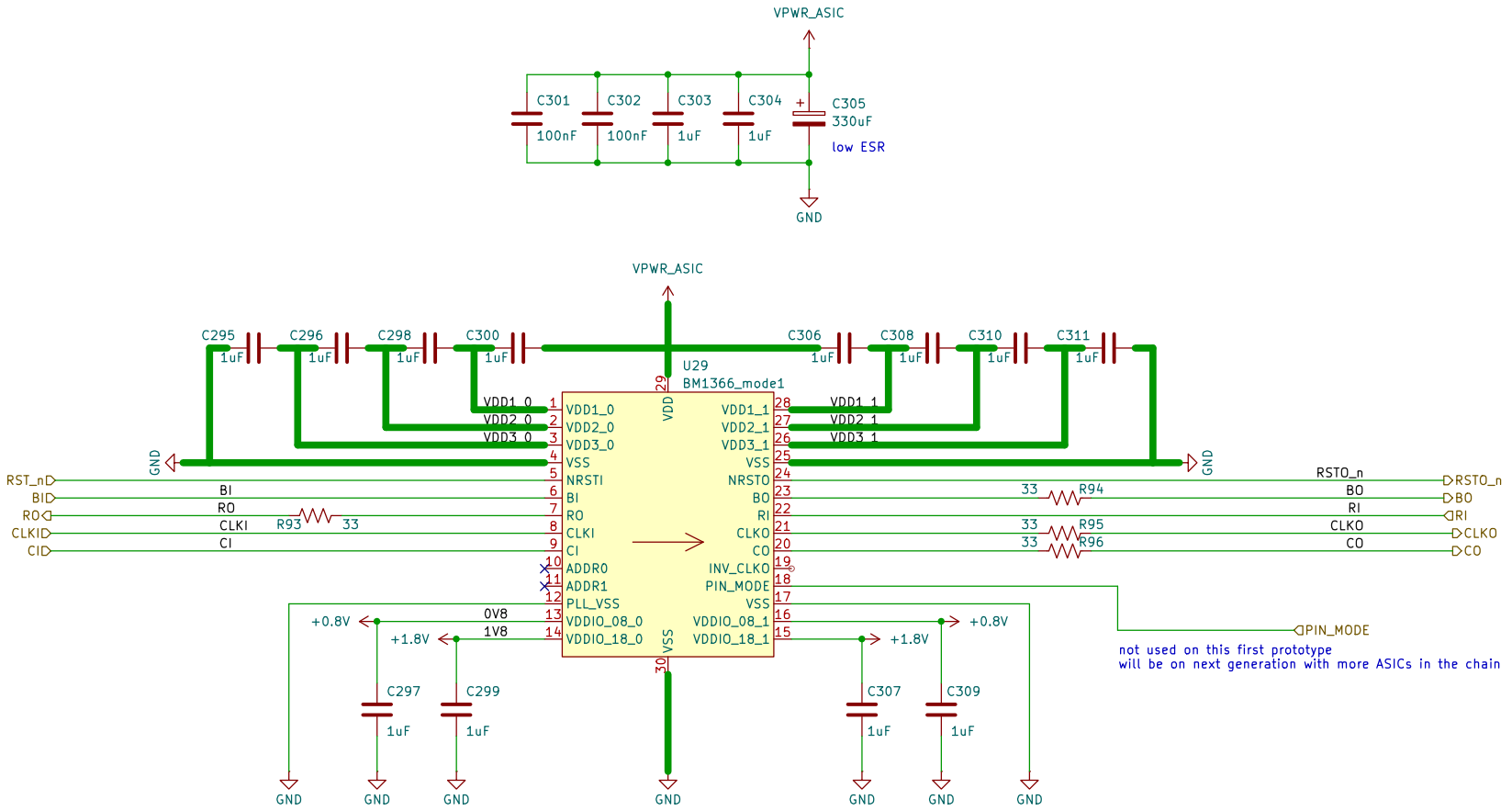
Size: A4	Date:	**Rev:**
KiCad E.D.A. 8.0.1		Id: 18/27



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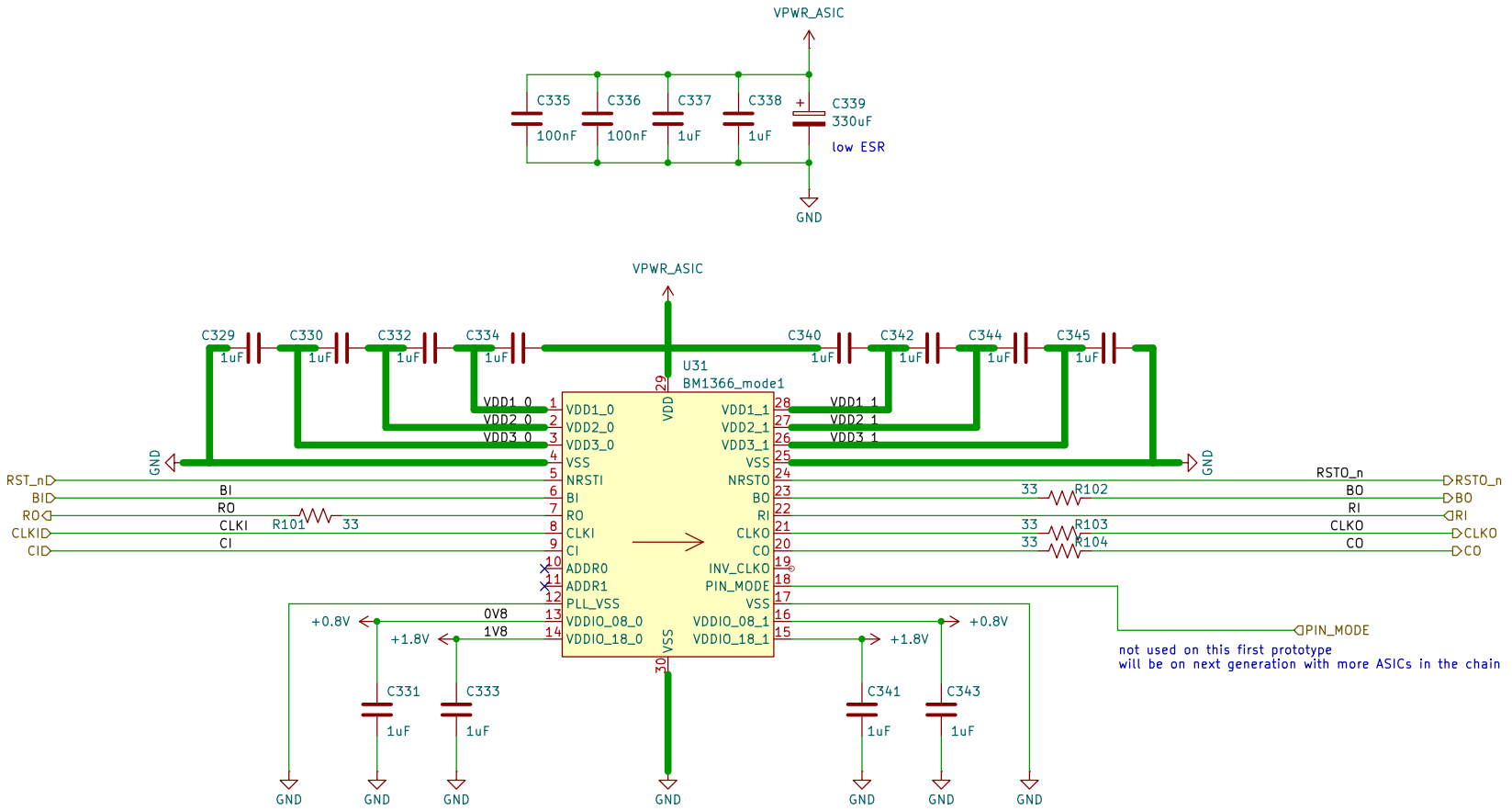

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Size: A4	Date:	**Rev:**
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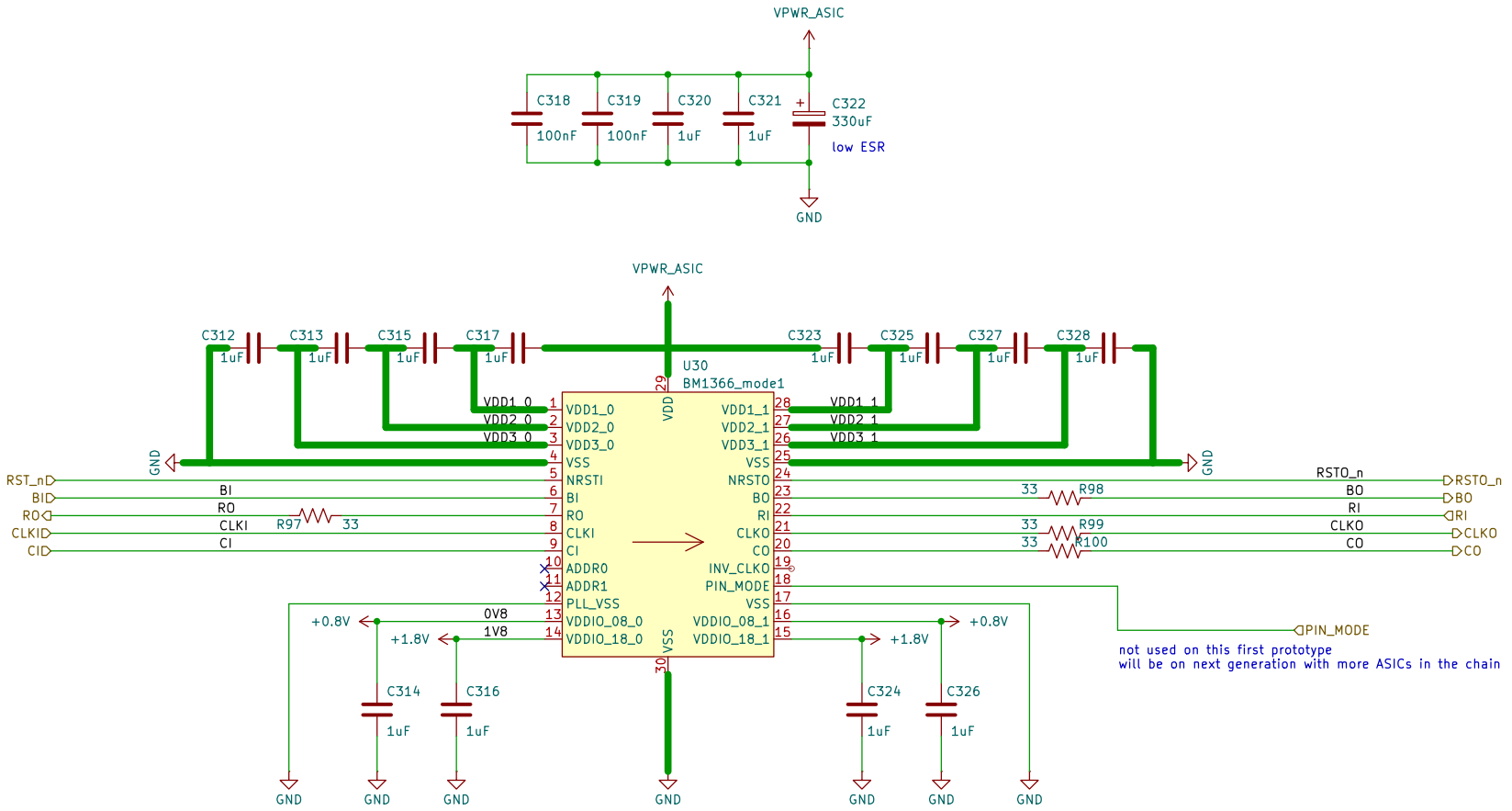

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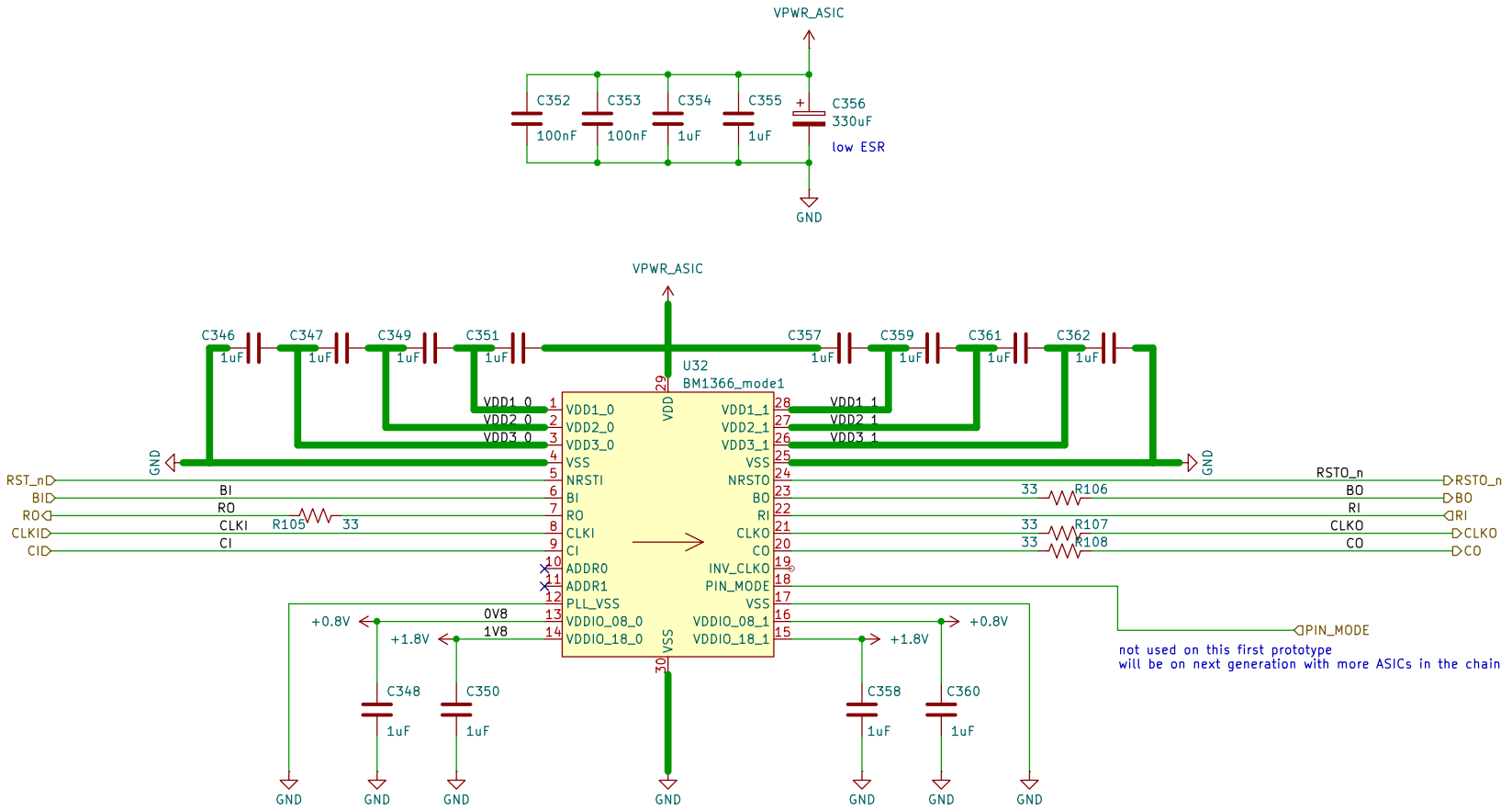

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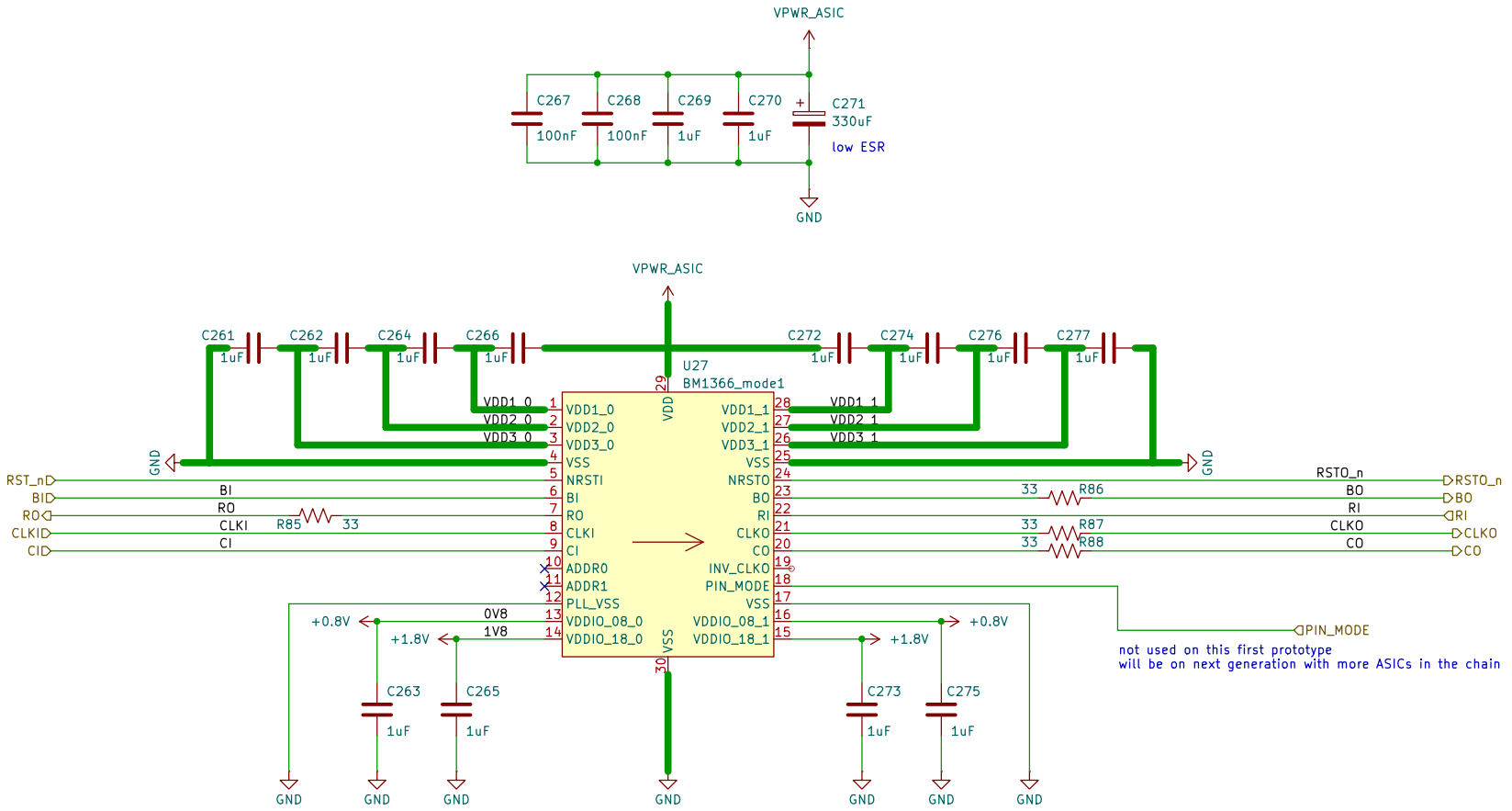

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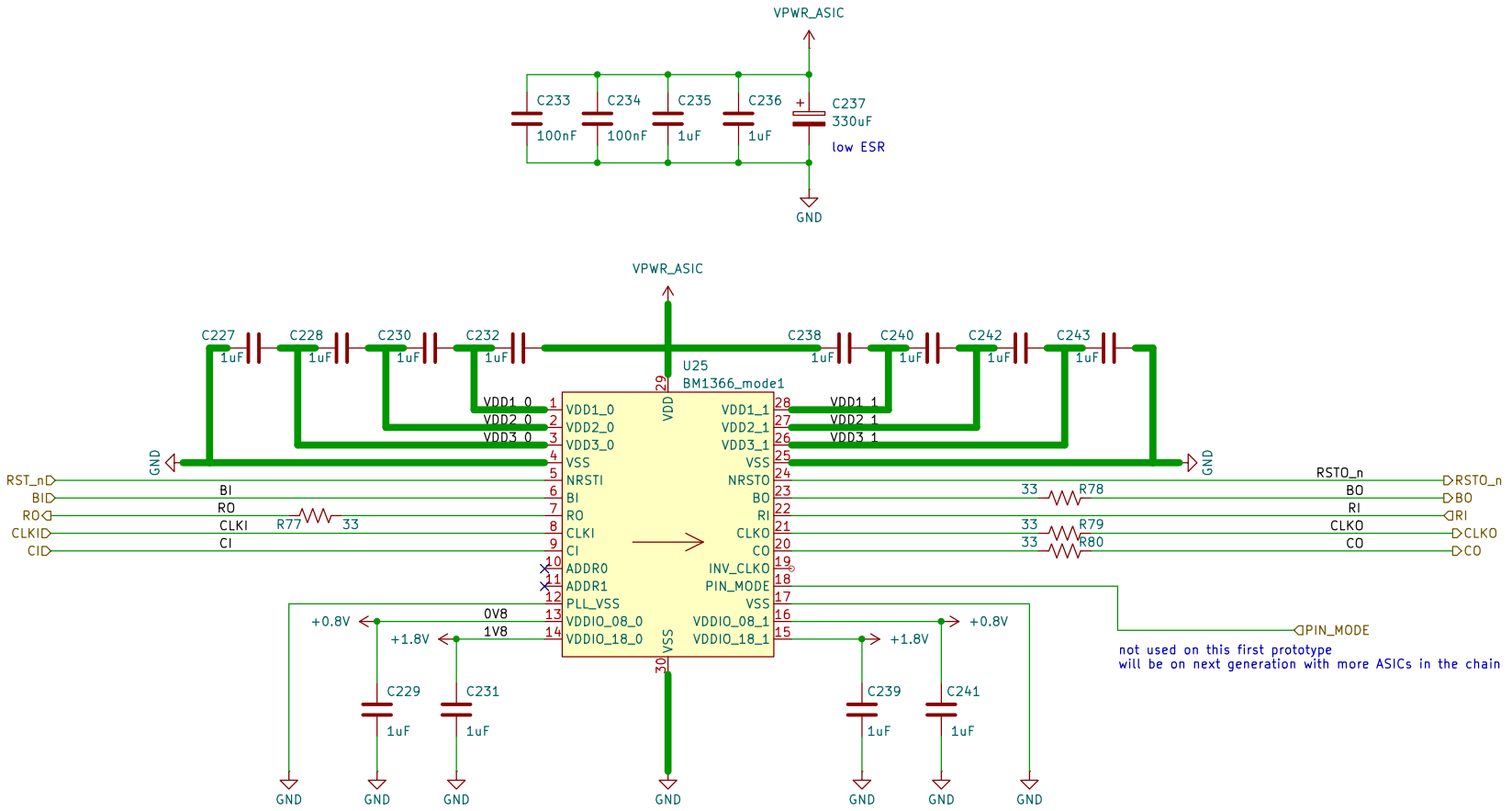

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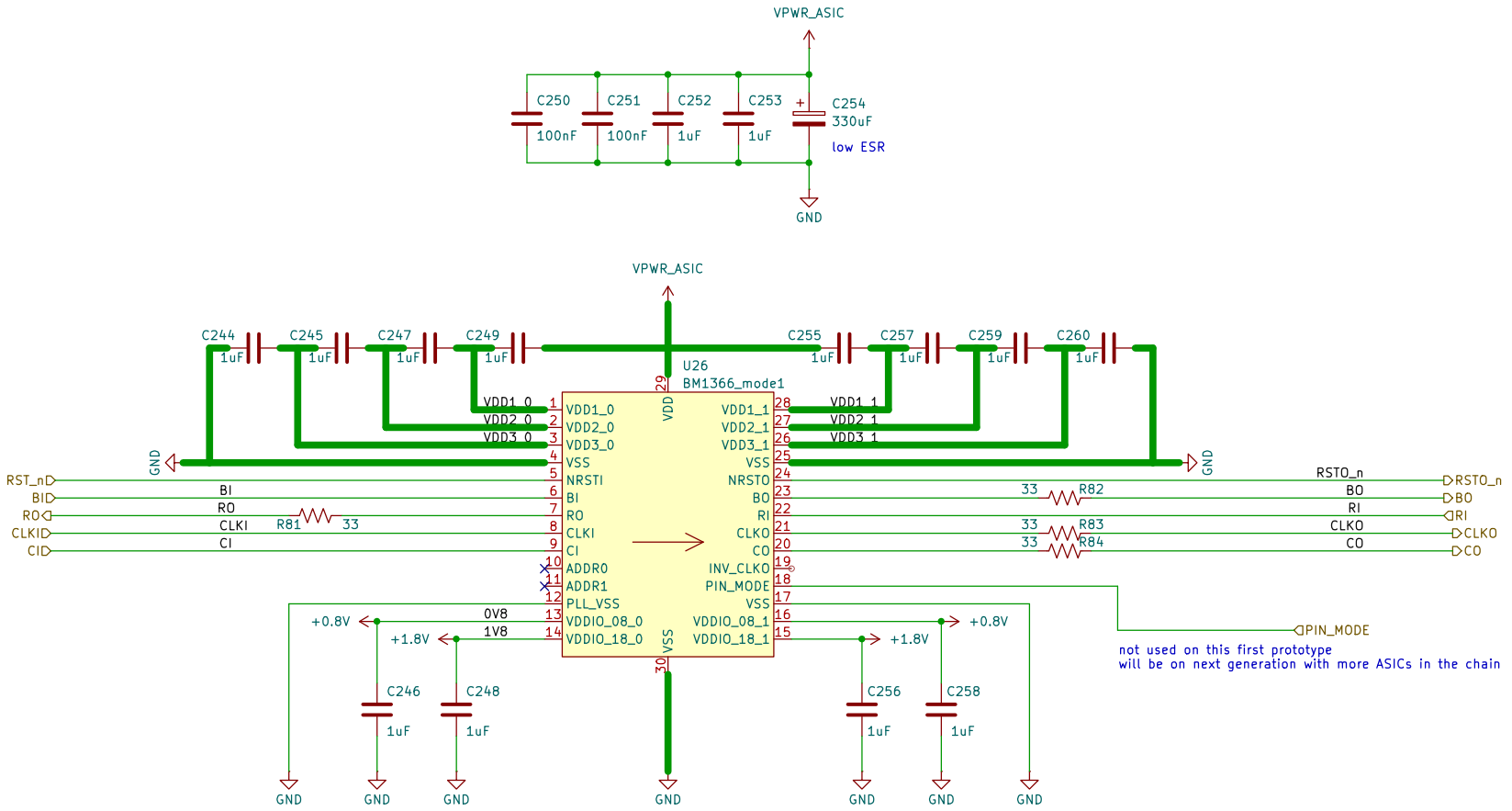

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