## **NUCLEO 144 H7 LEGACY**

MB1364

H753ZI

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U\_mb1364\_Top mb1364\_Top.SchDoc

## Legend

General comment such as function title, configuration, ...

Text to be added to silkscreen.

Warning text.

Notes to generate the board layout.

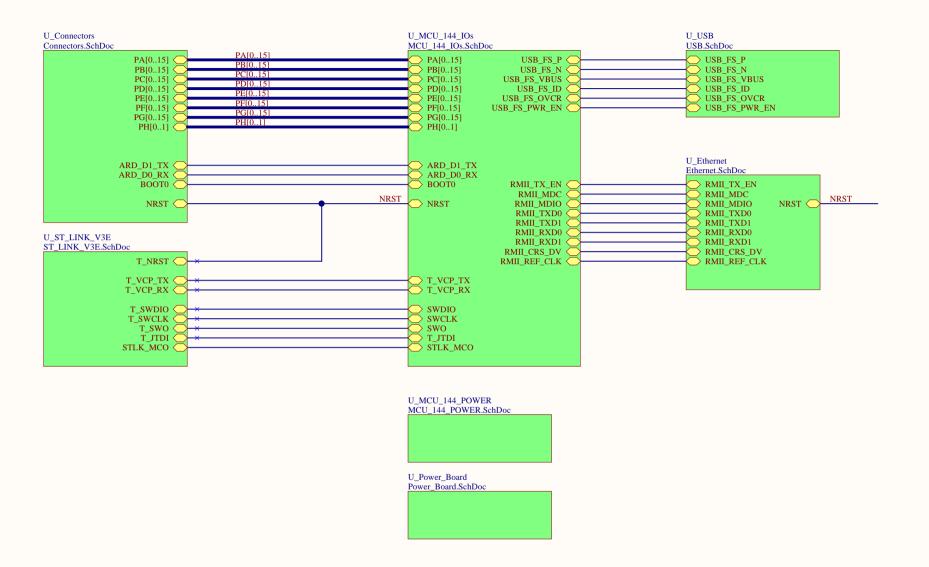
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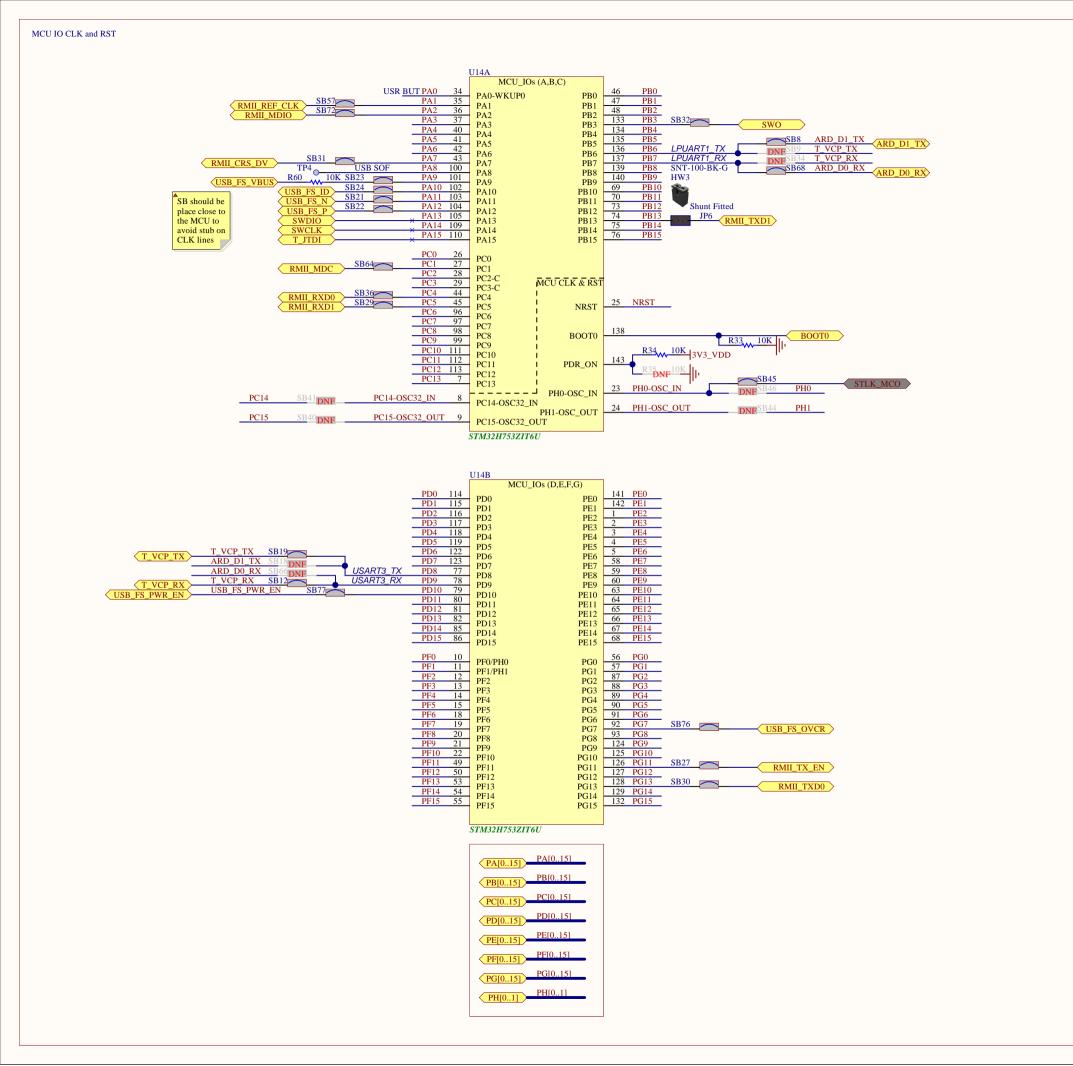
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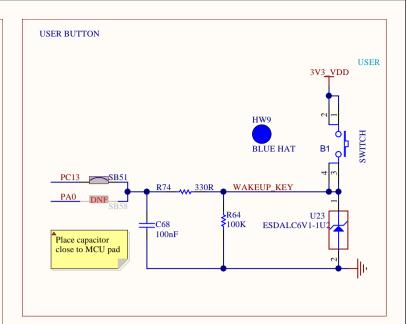
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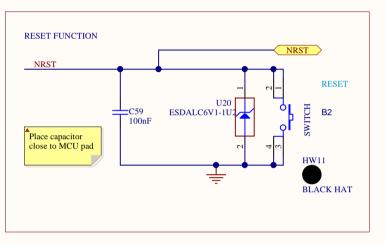
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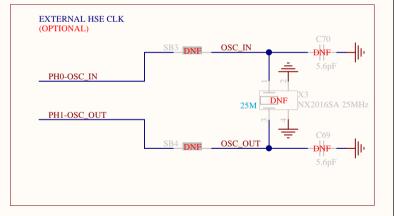


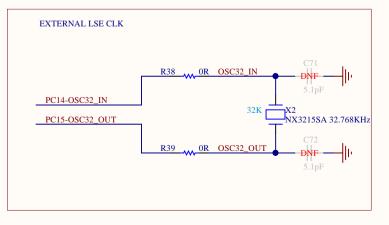
Title: mb1319 Top: hierarchical view			
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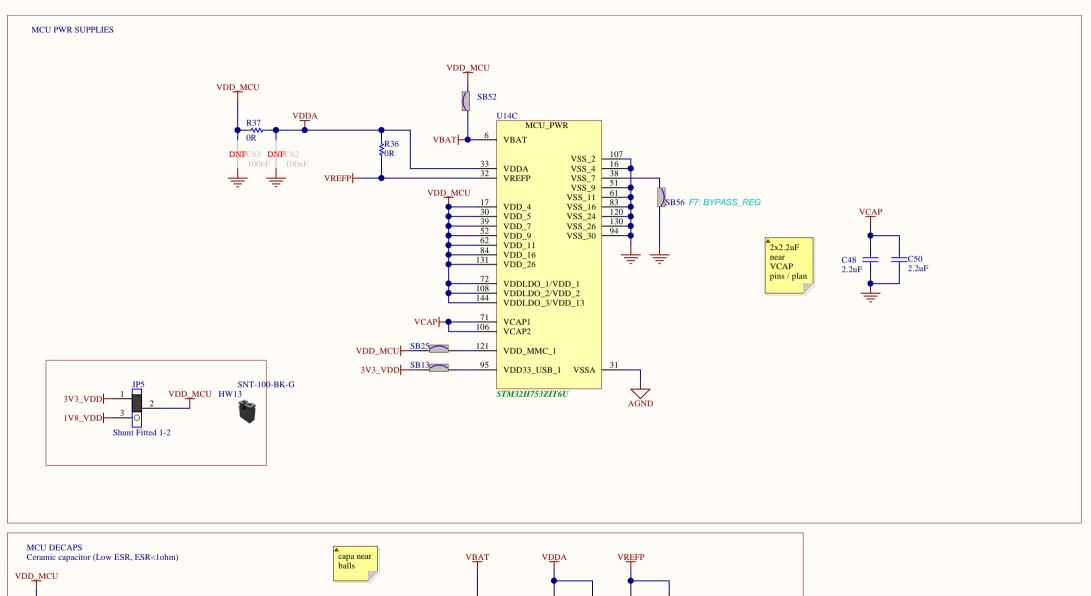


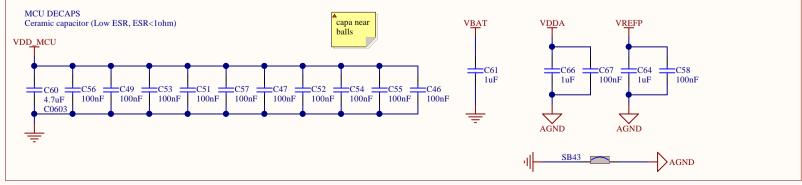






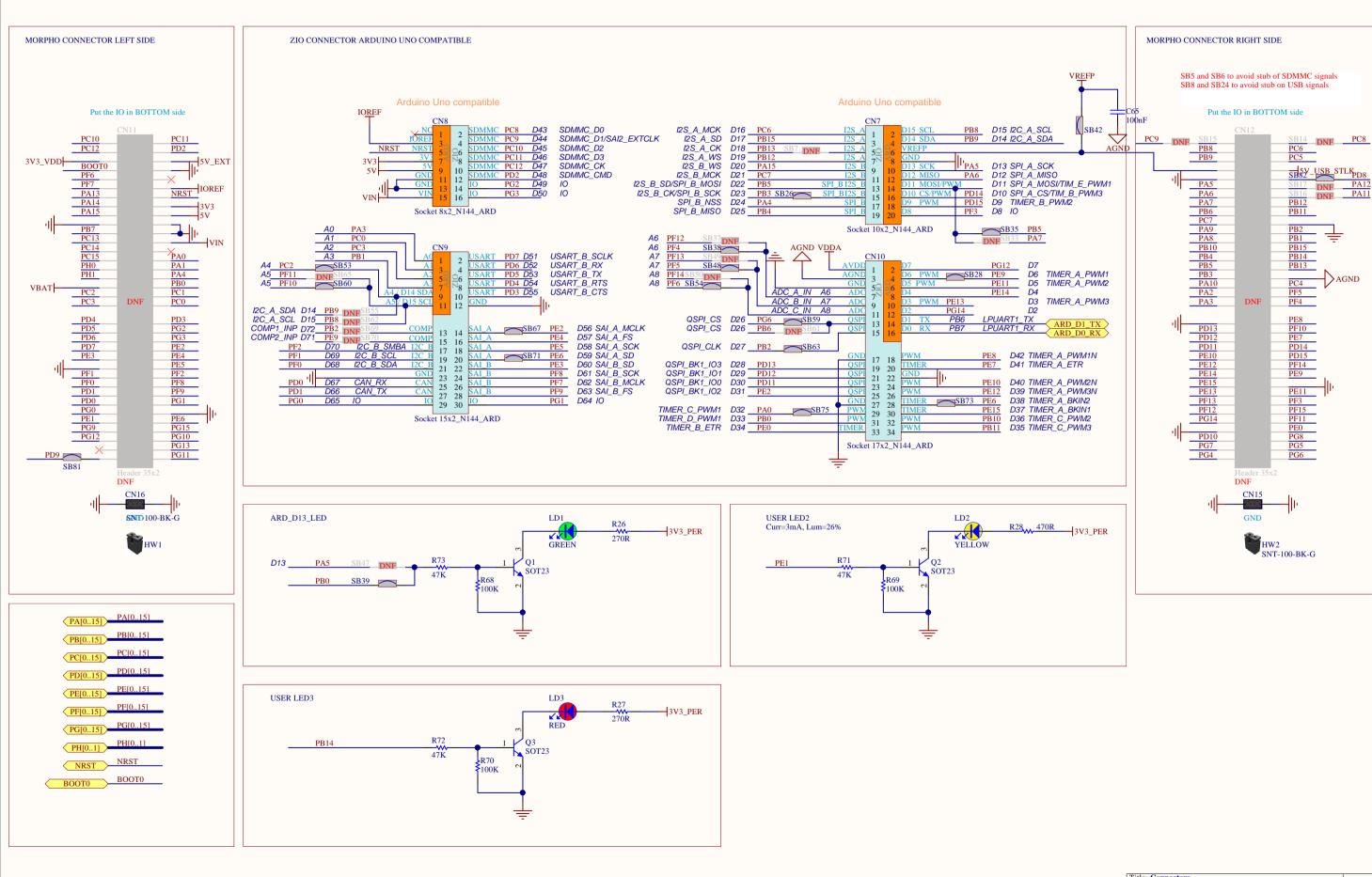
Title: MCU	144 I/Os		
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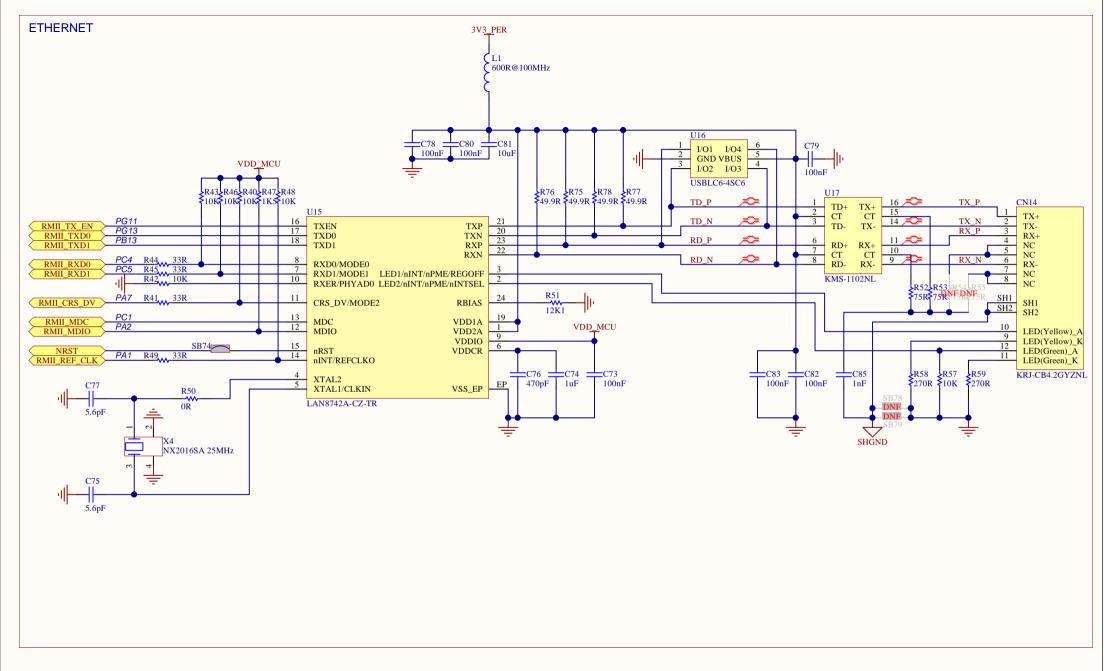


		144 POWER		
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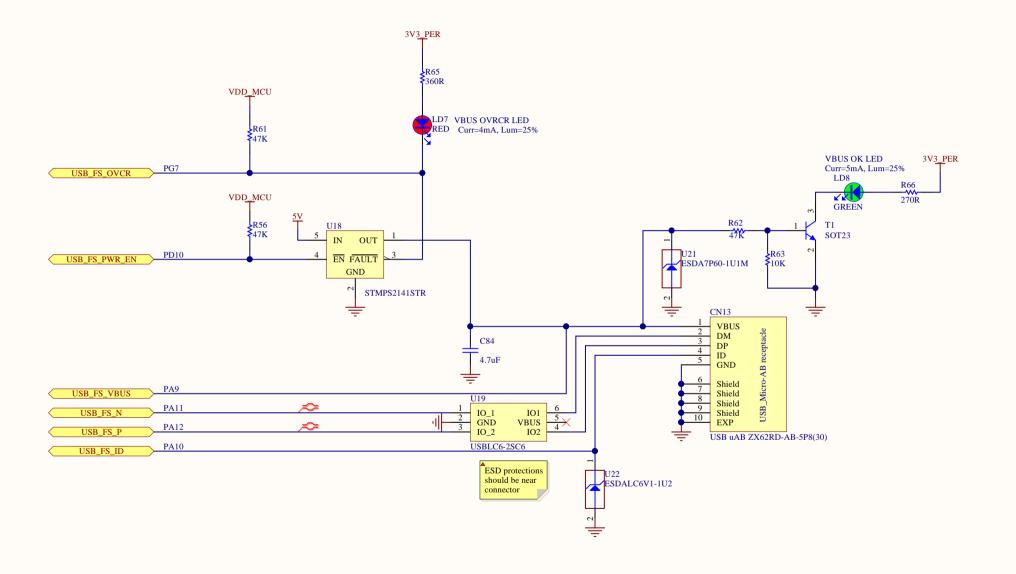


Title: Connectors			
Project: NUCLEO 144 H7 LEGACY			
Variant: H753ZI			
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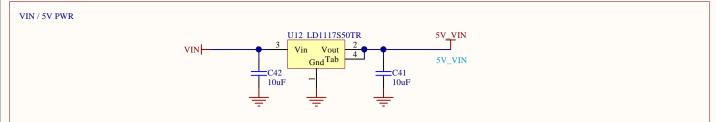


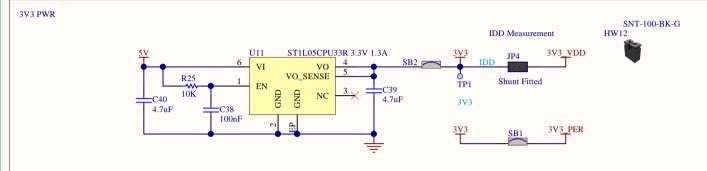
Title: Ethernet PHY with RJ45 connector			
Project: NUCLEO 144 H7 LEGACY			
Variant: H753ZI			
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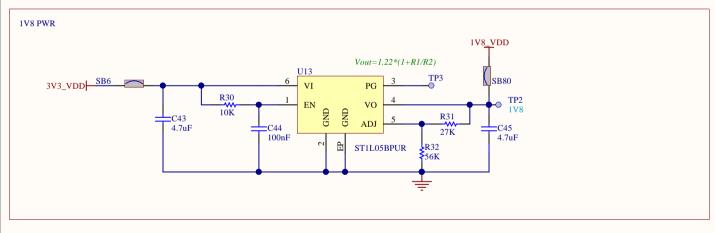


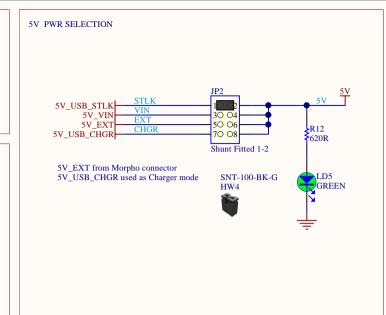


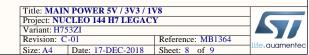
Title: USB			
Project: NUCLEO 144 H7 LEGACY			
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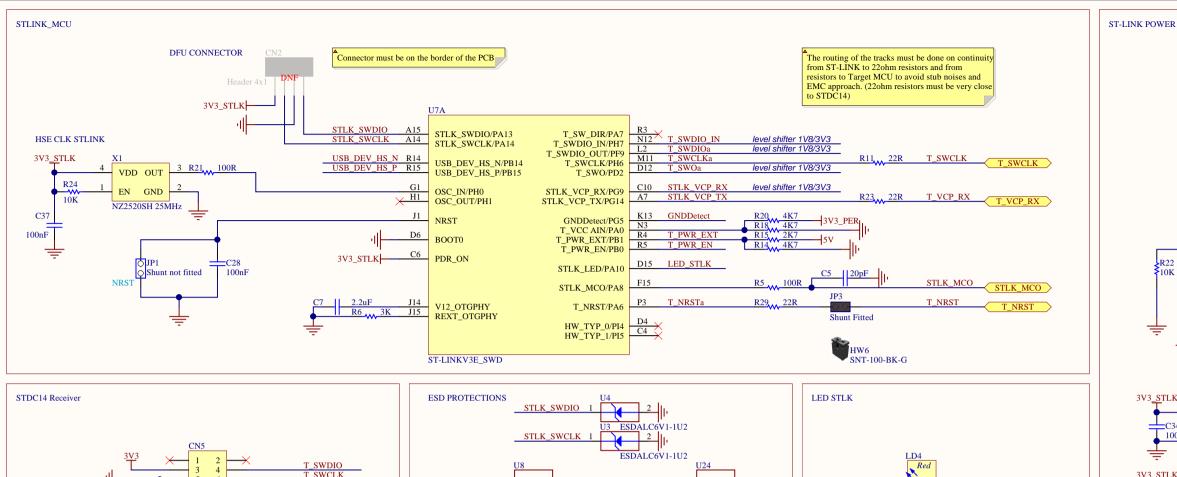












ESDALC6V1W5

T NRST

T\_VCP\_TX

T VCP RX

Pin attributions on ESD can be swapped for layout optimisation

ESDALC6V1W5

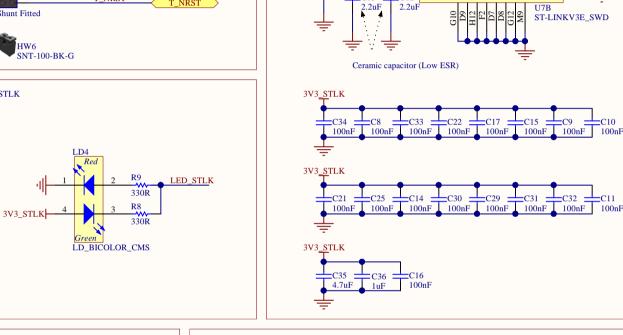
T\_SWDIO

T\_SWCLK

T\_SWO

T\_JTDI

T\_JTDI



3V3\_STLK

G13 C5 K4 G3 N8 N9 J13

VDD VDD

VDD VDD

VDD VDD

L4 BYPASS-REG

VCAP1 F13 VCAP2

7Î2 C9 VDDA VREF+ VBA"

M10

**≤**10K

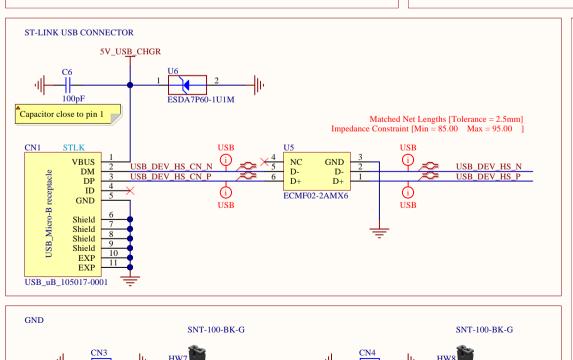
VSS H9
VSS H10

VSS -VSS -VSS -

VSS VSS VSS

VSS VSS VSS VSS VSS VSS VSS

VSS VSSA VREF-

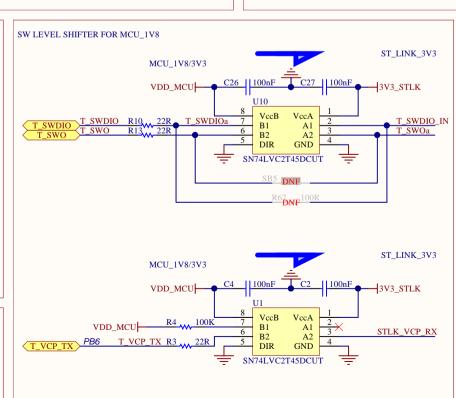


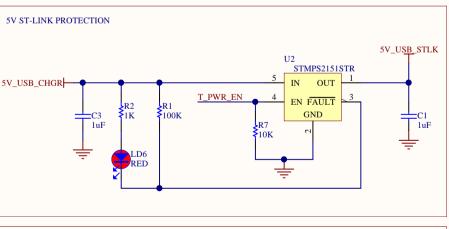
MIPI10 on STDC14 footprint

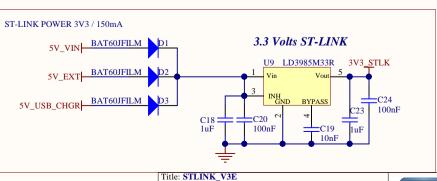
100R

T VCP RX

Specific constraints for T\_SWDIO and T\_SWCLK (must be same length and must be Shielded).







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