Toronto Metropolitan University

Department of Electrical, Computer, & Biomedical Engineering
Faculty of Engineering & Architectural Science

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Instructor:	Dr. Virgilio Valente

Assignment/Lab Number:	7
Assignment/Lab Title:	Design Amplifier Project

Submission Date:	Thursday April 13, 2023
Due Date:	Friday April 14, 2023

Student LAST Name	Student FIRST Name	Student Number	Section	Signature*
Abdalla	Philip	501089429	01	Philip

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Design Project **By: Philip Abdalla**

Date of Submission: Jan 30, 2023

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Table of Content

1. Introduction

The report for Amplifier Design Project, is presented herein. The project was conducted from March 30, 2023 to April 13, 2023. This project will focus on meeting specific requirements that the designed circuit needs to obey. This report will dive deeper on BJT Amplifiers and will explore why chosen amplifiers were used instead of others. This report will explore how resistors and capacitor values affect certain properties of the circuit like the Voltage Gain and will be proved by manual calculations and simulation on Multisim.

2. Objectives

In this design project, the BJT Amplifier circuit needs to meet the following specifications:
(ELE 404 - Amplifier Design Project, 2023)

- Power supply: +10V relative to the ground;
- Quiescent current drawn from the power supply: no larger than 10 mA;
- No-load voltage gain (at 1 kHz): $|A_2| = 50$ (±10%);
- Maximum no-load output voltage swing (at 1 kHz): no smaller than 8 V peak to peak;
- Loaded voltage gain (at 1 kHz and with $R_1 = 1$ kΩ): no smaller than 90% of the no-load voltage gain;
- Maximum loaded output voltage swing (at 1 kHz and $R_1 = 1$ kΩ): no smaller than 4 V peak to peak;
- Input resistance (at 1 kHz): no smaller than 20 k;
- Amplifier type: inverting or non-inverting;
- Frequency response: 20 Hz to 50 kHz (-3dB response);
- Type of transistors: BJT;
- Number of transistors (stages): no more than 3;
- Resistances permitted: values smaller than 220 kΩ from the E24 series;
- Capacitors permitted: 0.1 µF, 1.0 µF, 2.2 µF, 4.7 µF, 10 µF, 47 µF, 100 µF, 220 µF;
- Other components (BJTs, diodes, Zener diodes, etc.): only from your ELE404 lab kit.

Notes:

- The Output Voltage must be from from distortion (clipping, etc.) in all test conditions
- The source resistance, R_S, must be 600 Ω for all tests.

3. Circuit Under Test

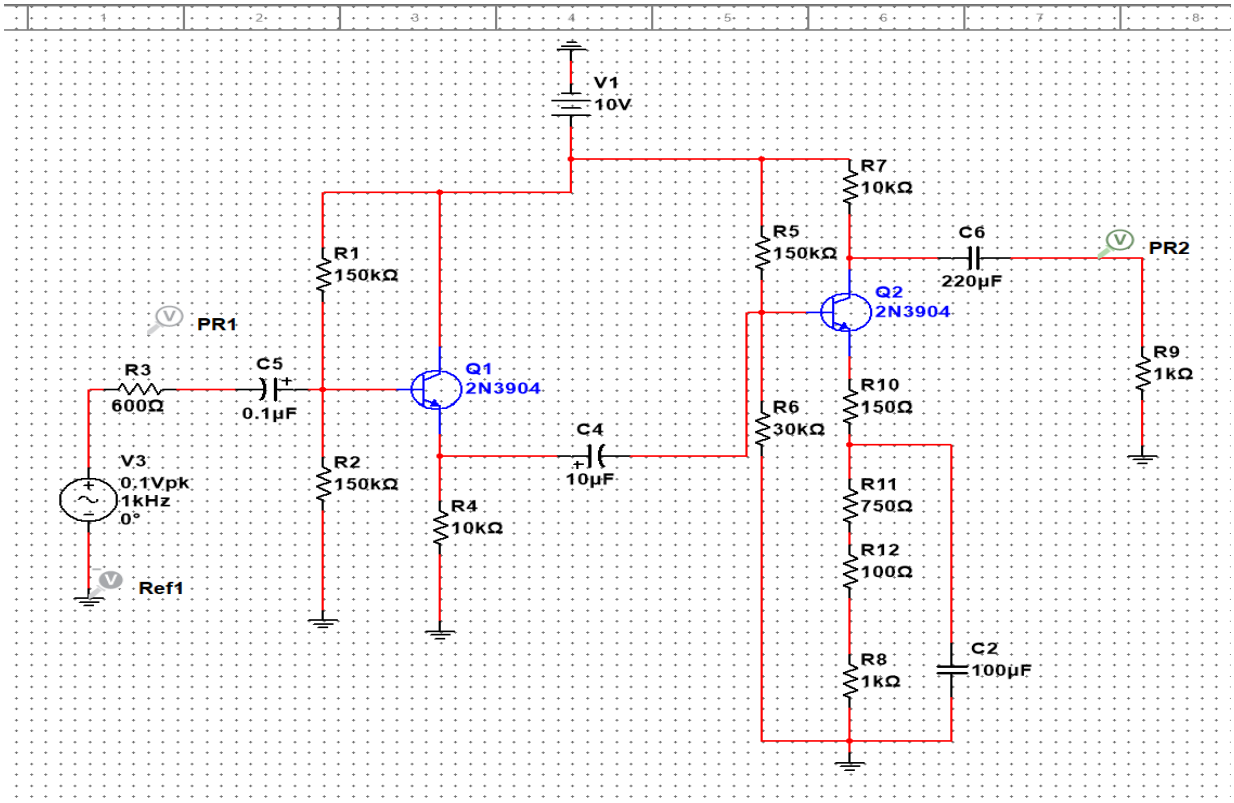

Figure 1: Circuit under test, Stage 1- Common Collector, Stage 2- Common Emitter

IDENTIFY

I chose Common Collector to be my first stage because it has a high input resistance and a very low output resistance which is perfect for “driving” small loads like the 1kΩ.

The problem with the common collector with respect to the specifications of this project is that it can’t amplify an input voltage. The Voltage Gain of a Common Collector is near 1V/V. Because of this issue, I decided to choose a Common Emitter as stage 2 because it has a somewhat low input resistance so that it won’t change the output voltage from stage 1 and its main purpose is to amplify the voltage. The Common Emitter will take the responsibility to amplify and the Common Collector will all accept high input resistances to match the specifications.

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Common Collector Decisions:

DC ANALYSIS

1) I first let I_C= 0.5 mA so that I can half of the current limit (10mA/2)
2) I need to select R_E to "center" my output Voltage (V_E = 5V), $R_E = V_E/I_E$ but I_E is approximately I_C so then R_E = 5V/0.5mA = 10 kΩ. I need to center my output voltage so that when the output voltage is oscillating, the transistor has enough room to change without going into the cutoff or saturation region. This decision will help to get a higher output voltage swing.
3) Now I need to choose R_1 and R_2 to set $V_B = V_E + 0.7 = 5.7$ -> This also helps with maintaining a good output swing and to push the transistor away from the cutoff region. For simplicity we will let R_1 and R_2 to be the same which will divide the 10V source among them equally so that it is near 5.7V. We need to note that $R_2 <= \beta * R_E/10$ -> This is using the reflection rule which helps stabilize the base voltage; With β =150 we can approximate R_2 = 150kΩ which means that R_1 = 150kΩ.

AC ANALYSIS

1) We know that Voltage Gain will be near one => A_v = 1V/V because the it is a Common Collector
2) $R_{in} = R_1//R_2//\beta(r_e + R_E)$ where $r_e = V_T/I_C$. When substituting and doing the parallel calculation we get R_{in} = 71.4 kΩ. This passes the specifications because R_{in} is greater than 20 kΩ.
3) $R_{out} = R_E//(r_e + [R_1//R_2]/150])$, the output resistance will be; R_{out} = 521 Ω
4) In order to find capacitor values, I did a trial and error process and noticed that the capacitor at the input side is "fighting" with the one at the output side. Meaning that as I decrease the input capacitor, the output capacitor takes over and vice versa. I chose that my input capacitor to be 0.1μF and the output capacitor to be 10μF.

Common Emitter Decisions:

DC ANALYSIS

1) I first let I_C= 0.5 mA so that I can get the other half of the current limit (10mA/2) going into the common emitter
2) I need to select R_E to let V_E = 1V, $R_E = V_E/I_E$ but I_E is approximately I_C so then R_E = 1V/0.5mA = 2 kΩ. I need V_E to be 1V so that it stabilizes the operating point of the

device so that it can keep a steady-state DC voltage on all the terminals to keep the transistor active. Also so that the output swing doesn't decrease as much.

3) Now I need to choose R_1 and R_2 to set $V_B = V_E + 0.7 = 1.7$ -> This also helps with maintaining a good output swing and to push the transistor away from the cutoff region. Because of the voltage divider the ratio of R_1 and R_2 will be equal to the ratio of their voltages. $R_1/R_2 = (10-1.7)/1.7 = 8.3/1.7$, again for a better beta stability (stabilizing V_B**)** we note that $R_2 <= \beta * R_E/10$ -> This is using the reflection rule which helps stabilize the base voltage; With $\beta = 150$ we can approximate $R_2 = 20k\Omega$ which means that $R_1 = 220k\Omega$ because of the ratio of R_1 and R_2.
4) We now need V_C to be centered ($V_C = 5V$) due to the oscillations of the output signal around the operation point. We need a 0.3 V across the transistor (V_{CE}) in order to keep the transistor out of saturation mode. Since $V_C = 5 = V_{CC} - I_C R_C \Rightarrow R_C = (10-5)/0.5mA = 10\ k\Omega$

With all these decisions we can ensure a better and bigger output swing since we ideally have the maximum V_{out} as V_{CC} which will make the transistor in the cutoff region and on the other extreme side when V_{out} reaches 1.3V meaning that is at the edge of saturation.

AC ANALYSIS

1) When V_{in} increases the emitter voltage decreases which will increase the collector current which will decrease the output voltage. This can be expressed as $V_{out} = -i_c R_C = -(V_{in} R_C)/R_E = -(R_C/R_E)V_I \Rightarrow$ More accurately $\Rightarrow A_v = -R_C/(r_e + R_E) = -4.878V/V$. But our Voltage is supposed to be 50V/V. We have 3 solution:
    a) Increase R_C: Not a good solution because the output resistance will increase which in not preferred
    b) Decrease R_E: Also not a good solution because we need it for a better operating point stability
    c) Apply Bypass Capacitor: This is the best decision because it doesn't affect any DC analysis and allows the gain to increase without affecting the our operating point
2) By choosing the Bypass Capacitor as the solution we break our 2kΩ emitter resistor into two components, one component will be considered in the voltage gain (R_{E1}) and the other will be bypassed (R_{E2}). Now using the gain voltage equation is the above step, and setting the voltage gain to 50, we can solve for R_{E1}. $R_{E1} = (R_C/A_v) - r_e = 150\Omega$. To find R_{E2} we know that the sum of R_{E1} and R_{E2} will equal out 2kΩ so $R_{E2} = 2k\Omega - 150\Omega = 1850\Omega$.
3) $R_{in} = R_1 // R_2 // \beta(r_e + R_{E1})$ where $r_e = V_T/I_C$. When substituting and doing the parallel calculation we get $R_{in} = 13..6\ k\Omega$. This passes the specifications because R_{in} is greater than 20 kΩ.

4) $R_{out} = R_C$, the output resistance will be; $R_{out} = 1K\Omega$
5) In order to find capacitor values, I did a trial and error process and noticed that the capacitor at the common node needs to be high so that it could have a low impedance at low frequency meaning that it will act as a short circuit at low frequency like 20 Hz which is part of the specifications. The issue is that at the low pass of my frequency response, the -3dB is in the million hertz. The way to solve this is to add a RC Filter but the problem is that the capacitor used needs to be very low like 2nF which I can't create with the specified capacitor values given in the requirements.

Up to this point we can meet most of the requirements but since our R_C is much higher than the 1kΩ load resistor, our voltage $A_v = - (R_C//R_L)/(r_e + R_E)$ will drop to 4.55V/V which is about a 90% drop without the load resistor. In order for this circuit to maintain its gain when a load resistance is present, the load resistance needs to be much larger than $R_C = 10k\Omega$ which is still considered small. If I try to change the R_C to meet the loaded voltage gain requirement then I_C will increase and the 10mA requirement will break.

4. Manual Calculations

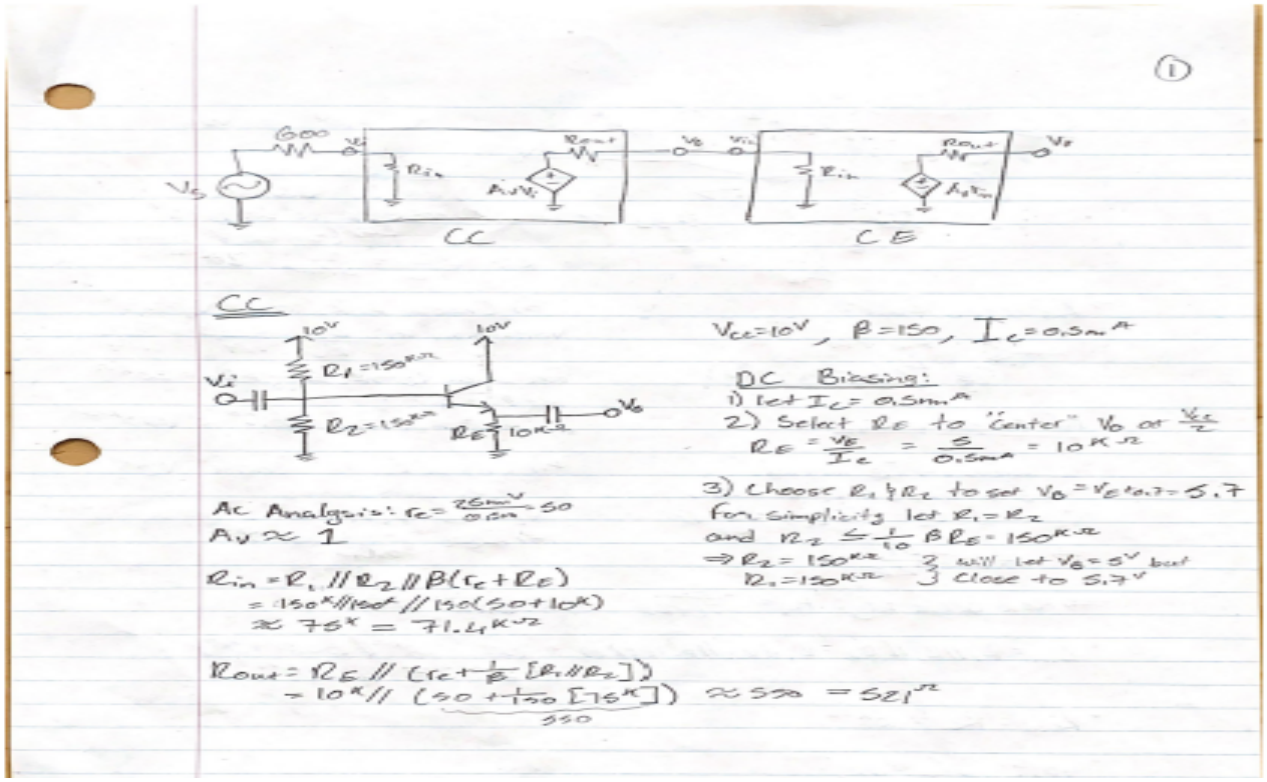


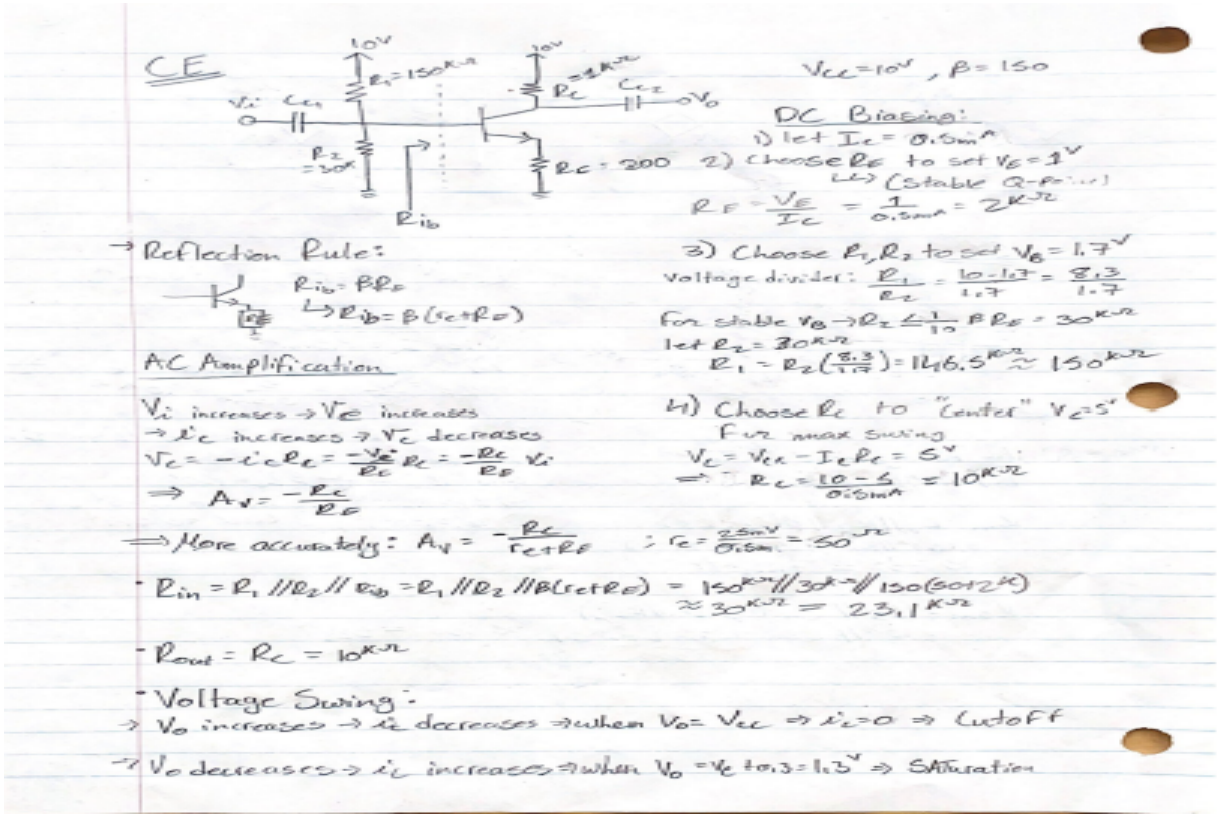
Figure 2: Common Collector Manual Calculations

Table 1: Stage 1- Common Collector DC calculations

V_B	V_C	V_E	I_B	I_C	I_E
5.7V	10V	5V	3.33μA	0.5mA	0.504mA

Table 2: Stage 1- Common Collector AC calculations

R_{in}	R_{out}	g_m	r_e	r_π	A_{vo}	A_v
71.4 kΩ	521Ω	0.019S	50Ω	7.88 kΩ	1 V/V	1 V/V



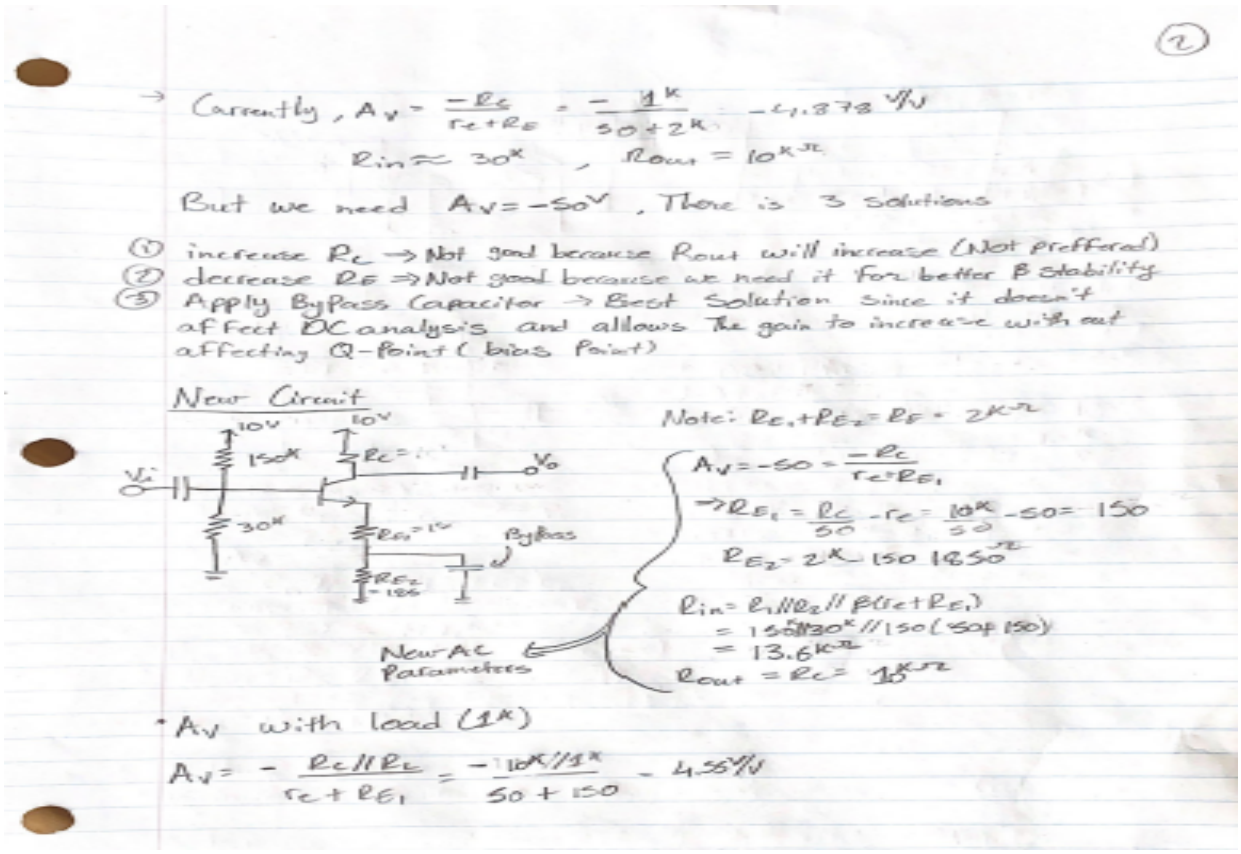


Figure 3: Common EmitterManual Calculations

Table 3: Stage 2- Common Emitter DC calculations

V_B	V_C	V_E	I_B	I_C	I_E
1.7V	5V	1V	3.33μA	0.5mA	0.504mA

Table 4: Stage 1- Common EmitterAC calculations

R_{in}	R_{out}	g_m	r_e	r_π	A_{vo}	A_v
13.6 kΩ	10 kΩ	0.019 mS	50 Ω	7.77 kΩ	-50 V/V	-4.55 V/V

Table 5: Full Circuit

R_{in}	R_{out}	A_{vo}	A_v
71.4 kΩ	10 kΩ	-50 V/V	-4.55 V/V

5. Simulation and Check

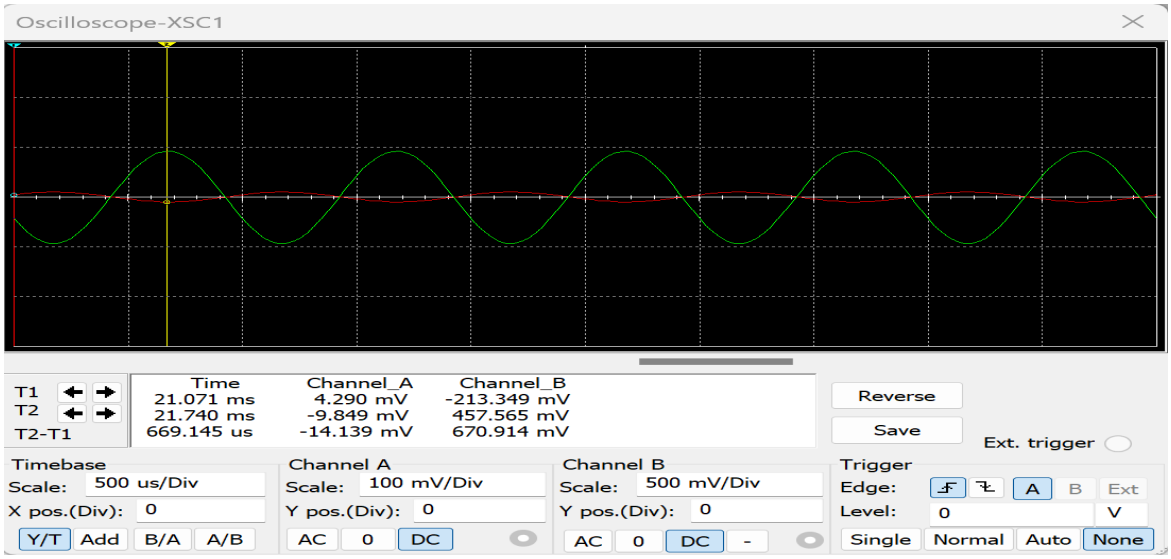


Figure 4: No load Voltage Gain

As shown in Figure 4, the voltage gain is 457.5/-9.849 = -46.6 V/V which is near the unloaded voltage gain of -50V/V that was calculated manually. This also matches the specified requirements.

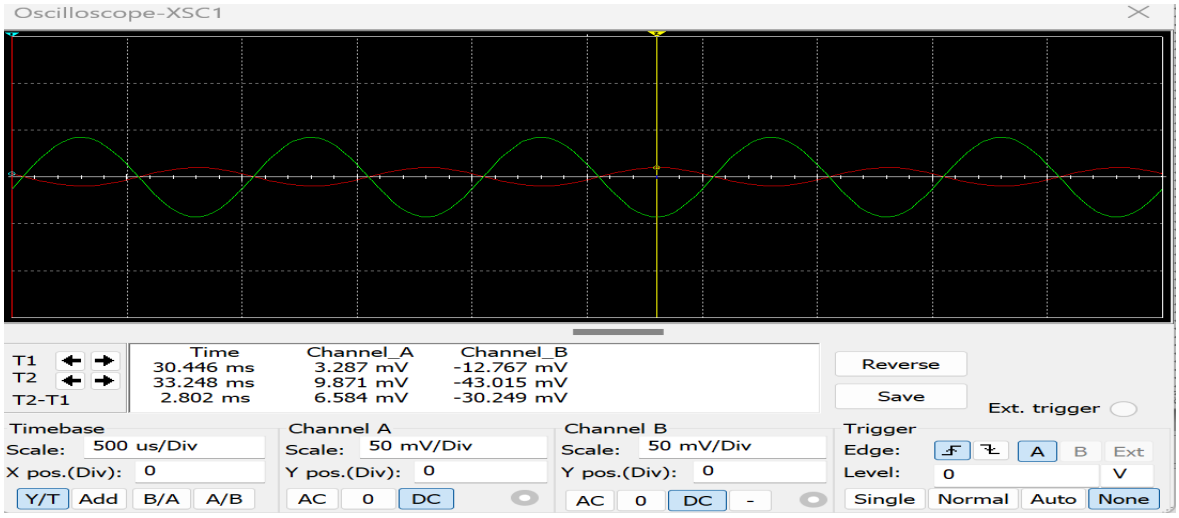


Figure 5: Load Voltage Gain

As shown in Figure 4, the voltage gain is –43/-9.87 = -4.4 V/V which is near the loaded voltage gain of -4.55V/V that was calculated manually. This doesn't match the specified requirements because our output resistance is much larger than the load resistance of 1kΩ

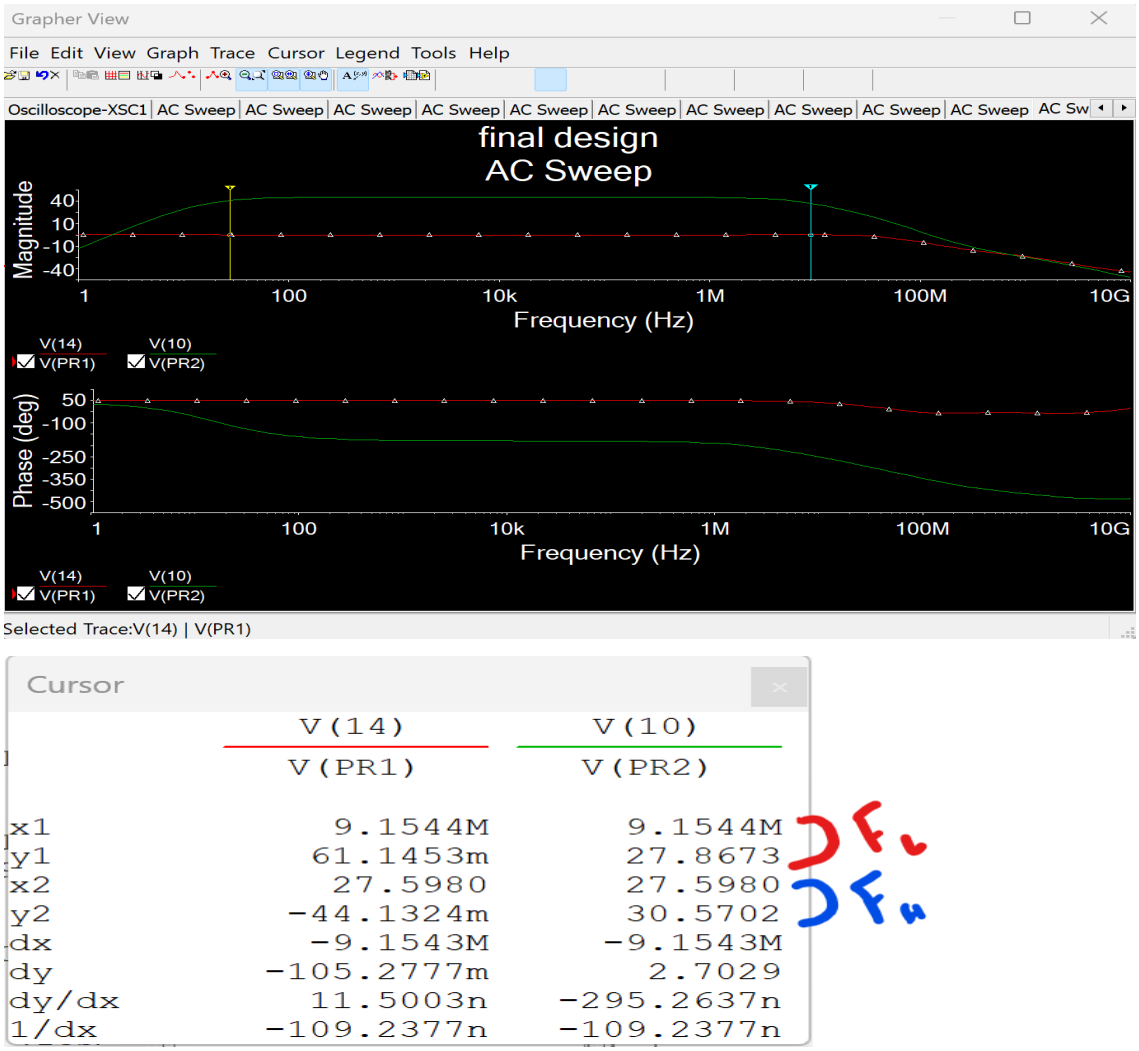


Figure 6: Frequency response

As shown in Figure 6 and explained in the “Identify” section, the bandwidth of the frequency response does start around 20 Hz but it ends as a much higher frequency. This somewhat matches the specified requirements and in order to fix the low pass frequency we can use a RC Filter.

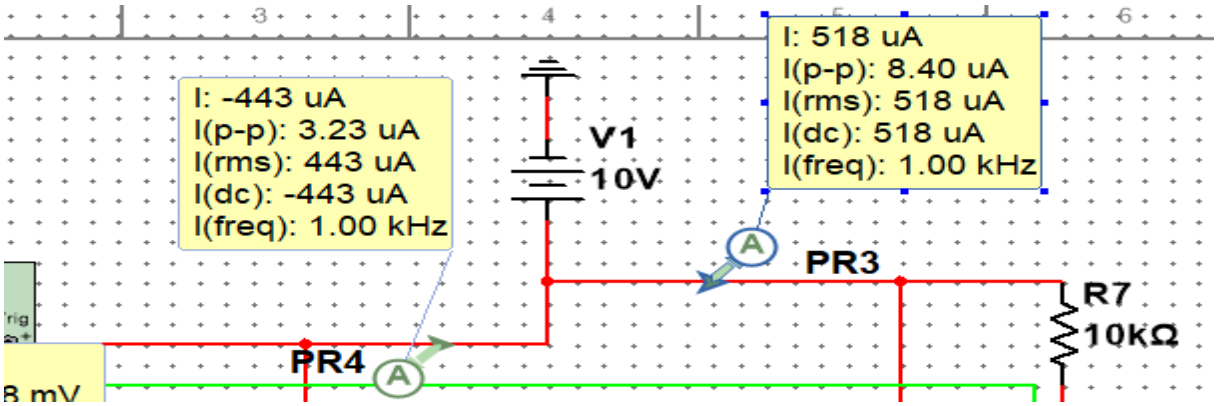


Figure 7: Power Supply Current

As shown in figure 7, the maximum current that is being drawn from the 10V voltage source adds up to 10mA. This matches the required specification mentioned.

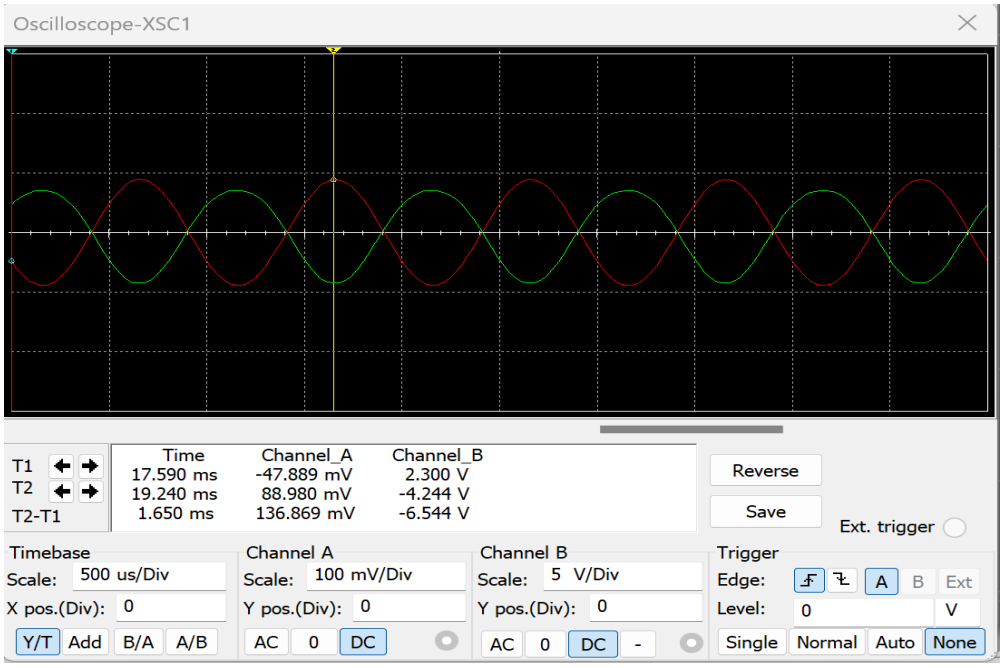


Figure 8: Unloaded output Voltage Swing

As shown in figure 8, the voltage is about 2(-4.2V) = -8.4V which is above a 8V peak to peak voltage. This matches the required specification mentioned.

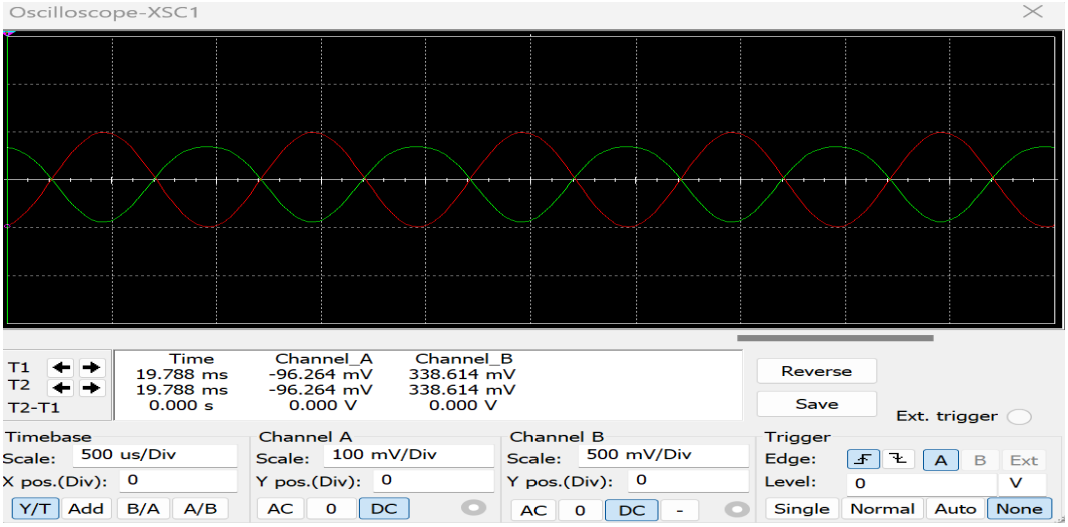


Figure 9: loaded output Voltage Swing

As shown in figure 9, the voltage is about 2(-338mV) = -7mV which is less than 4V peak to peak voltage. This is due to the output resistance being much larger than the loaded resistance of 1kΩ. This doesn't match the required specification mentioned.

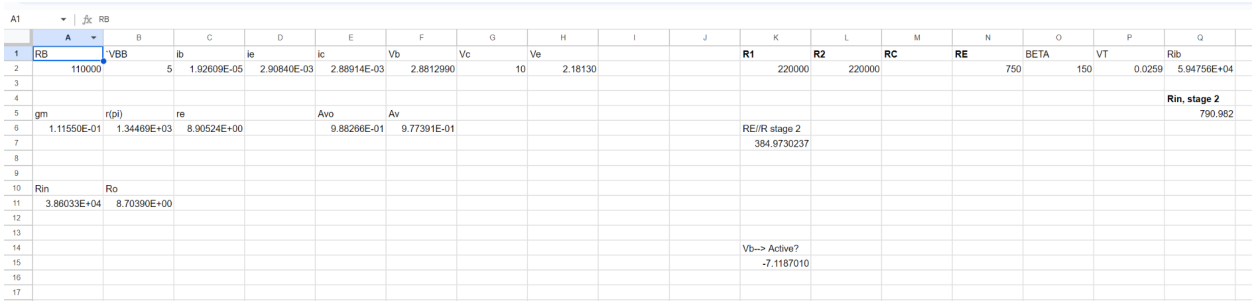
6. Discrepancies

- As shown above the calculated values are not exactly the same. This may occur because of rounding errors or because of how complex the circuit is. I might not have considered all the components that might affect a parameter like the voltage gain.
- The loaded voltage gain doesn't match the required specification because the output resistance of the Common Emitter is 10kΩ which is much higher than the load resistance (1kΩ). Because the Voltage gain is directly proportional to the parallel calculation of the 10kΩ and the 1kΩ, thai will drop the voltage gain significantly. I could try to get the output resistance to be much lower than the 1kΩ but that will change the operation point and will drop the output voltage swing.
- The frequency response (-3dB) goes to millions of hertz instead of the specified 50KHz. The is due to a high capacitance which is needed to be "short circuited" at low frequencies due to its low impedance. We can solve this problem by using a RC Filter with a very low capacitance (capacitance value is in nanos). Since the capacitance value is very low, I can't create it with the limited values given in the required specifications.

7. Conclusion and Remarks

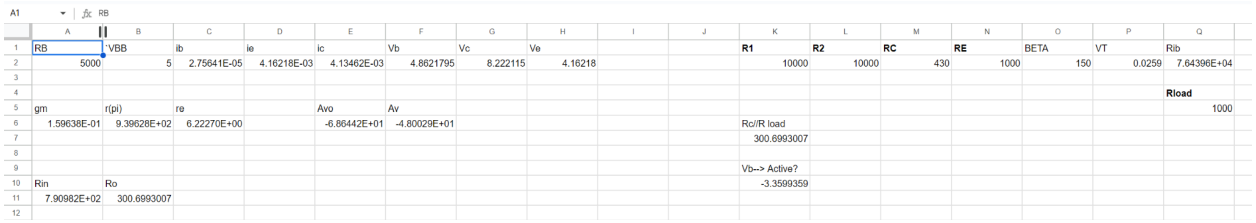
In conclusion, my designed circuit might have not met all the requirements mentioned but it has most of them met with somewhat close values. Creating a circuit with these specifications was very hard since one change in one element will easily break one of the requirements. The process of designing this circuit tried to take the best of all the requirements and the parts it couldn't meet, the specific reason was mentioned on why it happened and a possible solution.

8. Appendix



	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q
1	RB	VBB	ib	ie	ic	Vb	Vc	Ve			**R1**	**R2**	**RC**	**RE**	BETA	VT	Rib
2	110000	5	1.92609E-05	2.90840E-03	2.88914E-03	2.8812990	10	2.18130			220000	220000		750	150	0.0259	5.94756E+04
3																	
4																	**Rin, stage 2**
5	gm	r(pi)	re		Avo	Av											790.982
6	1.11550E-01	1.34469E+03	8.90524E+00		9.88266E-01	9.77391E-01					RE//R stage 2						
7											384.9730237						
8																	
9																	
10	Rin	Ro															
11	3.86033E+04	8.70390E+00															
12																	
13																	
14											Vb--> Active?						
15											-7.1187010						
16																	
17																	

Figure 10: Common Collector Excel Calculator (By: Philip Abdalla)



	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q
1	RB	VBB	ib	ie	ic	Vb	Vc	Ve			**R1**	**R2**	**RC**	**RE**	BETA	VT	Rib
2	5000	5	2.75641E-05	4.16218E-03	4.13462E-03	4.8621795	8.222115	4.16218			10000	10000	430	1000	150	0.0259	7.64396E+04
3																	
4																	**Rload**
5	gm	r(pi)	re		Avo	Av											1000
6	1.59638E-01	9.39628E+02	6.22270E+00		-6.86442E+01	-4.80029E+01					Rc//R load						
7											300.6993007						
8																	
9											Vb--> Active?						
10	Rin	Ro									-3.3599359						
11	7.90982E+02	300.6993007															
12																	

Figure 11: Common Emitter Excel Calculator (By: Philip Abdalla)

- Link of the Excel that refers to figure 10 and 11.

https://docs.google.com/spreadsheets/d/14TOxxpPbHajkU7D2AY5jtvlOETxqBQ9eZhAfSZeG1mw/edit?usp=sharing