Ασκηση 1 VHDL

a	b	c	e	y
0	0	0	1	1
0	0	1	1	1
0	1	0	1	0
1	0	0	0	0
1	0	1	0	0
1	1	0	0	0
0	1	1	0	1
1	1	1	0	0

απλοποιησεις:
E = (-a)(-c)+(-a)(-b)c = (-a)((-b)c+(-c)) = (-a)((-b)+(-c)) = (-a)(-b) + (-a)(-c)

Y = (-a)(-b) + (-a)(-b)c + (-(A + (-C)))=(-a)(-b)+(-a)(-b)c+(-a)(-(-(c)) = (-a)(-b)+(-a)(-b)c+(-a)c=
=(-a)(-b)+(-a)c

VHDL:

```
entity Assign1 is
port(
        a, b, c         : in STD_LOGIC;
        e, y            :out STD_LOGIC
);
end entity Assign1;

 architecture Dataflow of Assign1 is
begin

e <= ((not a) and (not c)) or ((not a) and (not b) and c);
y <= ((not a ) and (not b)) or ((not a) and (not b) and c) or not (a or (not c));

end architecture Dataflow;
```