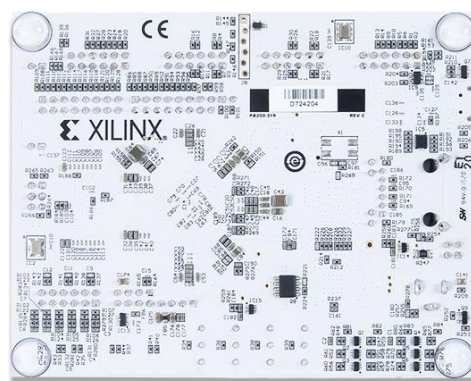
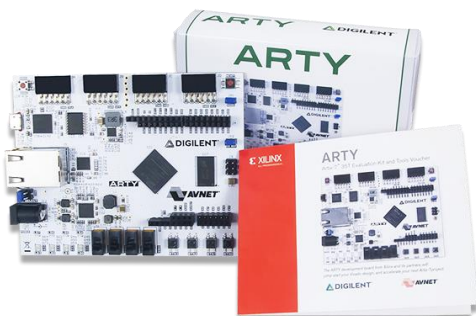
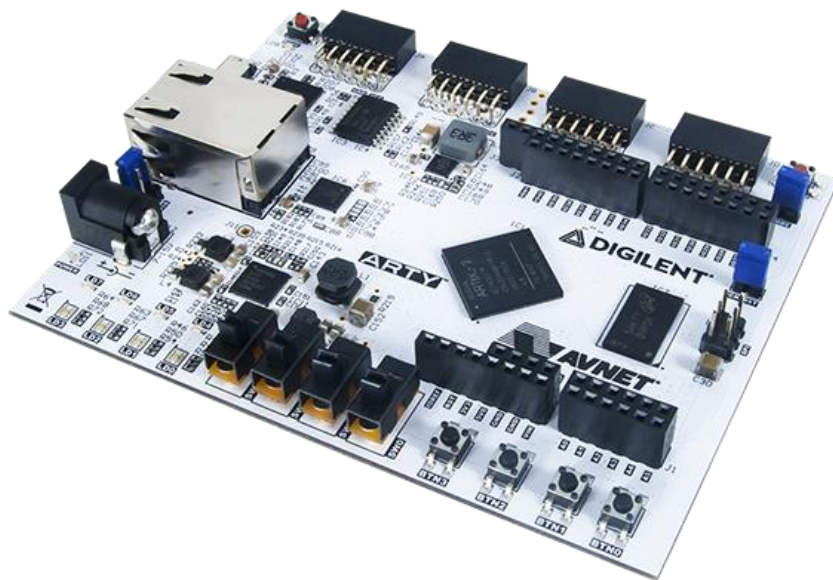


Arty A7 Reference Manual

The Arty A7, formerly known as the Arty, is a ready-to-use development platform designed around the Artix-7™ Field Programmable Gate Array (FPGA) from Xilinx. It was designed specifically for use as a MicroBlaze Soft Processing System. When used in this context, the Arty A7 becomes the most flexible processing platform you could hope to add to your collection, capable of adapting to whatever your project requires. Unlike other Single Board Computers, the Arty A7 isn't bound to a single set of processing peripherals: One moment it's a communication powerhouse chock-full of UARTs, SPIs, IICs, and an Ethernet MAC, and the next it's a meticulous timekeeper with a dozen 32-bit timers.



Features

Xilinx Artix-7 FPGA

5,200 slices containing four 6-input LUTs and 8 flip-flops (15,850 slices)¹⁾

1,800 Kbits of fast block RAM (4,860 Kbits)²⁾

5 clock management tiles (CMTs), each with a phase-locked loop and mixed-mode clock manager (6 CMTs)³⁾

90 DSP slices (240 DSP slices)⁴⁾

Internal clock speeds exceeding 450MHz

On-chip analog-to-digital converter (XADC)

Programmable over JTAG and Quad-SPI Flash

System Features

256MB DDR3L with a 16-bit bus @ 667MHz

16MB Quad-SPI Flash

USB-JTAG Programming circuitry

Powered from USB or any 7V-15V source

System Connectivity

10/100 Mbps Ethernet

USB-UART Bridge

Interaction and Sensory Devices

4 Switches

4 Buttons

1 Reset Button

4 LEDs

4 RGB LEDs

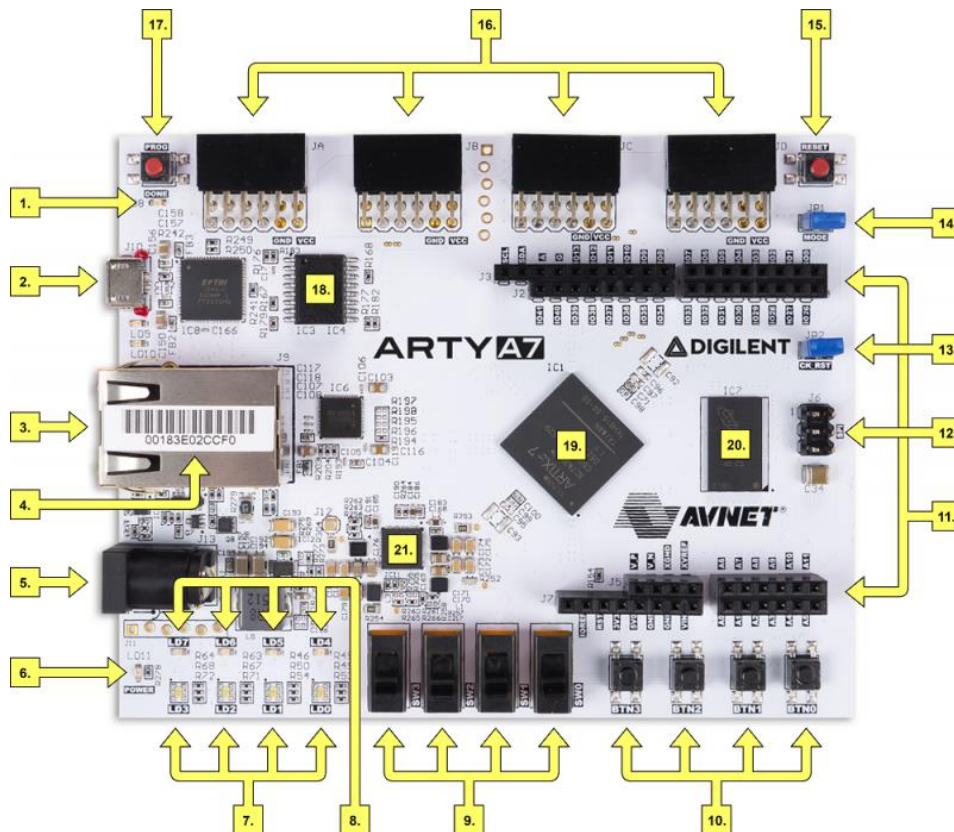
Expansion Connectors

4 Pmod connectors

Arduino/ChipKit Shield connector

1), 2), 3), 4) Arty A7-100 variant value in parentheses where different

The Artix A7 is fully compatible with the high-performance Vivado[®] Design Suite. It is supported under the free WebPACK[™] license, so designs can be implemented at no additional cost. This free license includes the ability to create MicroBlaze[™] soft-core processor designs. Design resources, example projects, and tutorials are available for download at the Artix Resource Center, accessible from reference.digilentinc.com.



Callout	Description	Callout	Description	Callout	Description
1	FPGA programming DONE LED	8	User RGB LEDs	15	chipKIT processor reset
2	Shared USB JTAG / UART port	9	User slide switches	16	Pmod connectors
3	Ethernet connector	10	User push buttons	17	FPGA programming reset button
4	MAC address sticker	11	Arduino/chipKIT shield connectors	18	SPI flash memory
5	Power jack for optional external supply	12	Arduino/chipKIT shield SPI connector	19	Artix FPGA
6	Power good LED	13	chipKIT processor reset jumper	20	Micron DDR3 memory
7	User LEDs	14	FPGA programming mode	21	Dialog Semiconductor DA9062 power supply

1 Purchasing Options

The Arty A7 can be purchased with either a XC7A35 or XC7A100 FPGA loaded. These two Arty A7 product variants are referred to as the Arty A7-35 and Arty A7-100, respectively. When Digilent documentation describes functionality that is common to both of these variants, they are referred to collectively as the “Arty A7”. When describing something that only applies to a specific variant, the variant will be explicitly called out by its name.

The only difference between the Arty A7-35 and Arty A7-100 are the capabilities of the Artix-7 part. The Artix-7 FPGAs both have the same functionality, but the -100 has about a 3 times larger internal FPGA than the -35. The differences between the two variants are summarized below:

Product Variant	Arty A7-35	Arty A7-100
FPGA Part Number	XC7A35TICSG324-1LXC7A100TCSG324-1	
Look-up Tables (LUTs)	5,200	15,850
Flip-Flops	29,200	126,800
Block RAM	225 KB	607.5 KB
Clock Management Tiles	6	

The board is sold standalone, but requires either a micro USB cable or 7-15V external power supply to be powered. The external power supply must have a coaxial, center-positive connector with 2.1 mm or 2.5 mm internal diameter. When purchased from Digilent, a micro USB cable or suitable 12V, 3A power supply can be added at the time of purchase.

2 Designing with the Arty A7

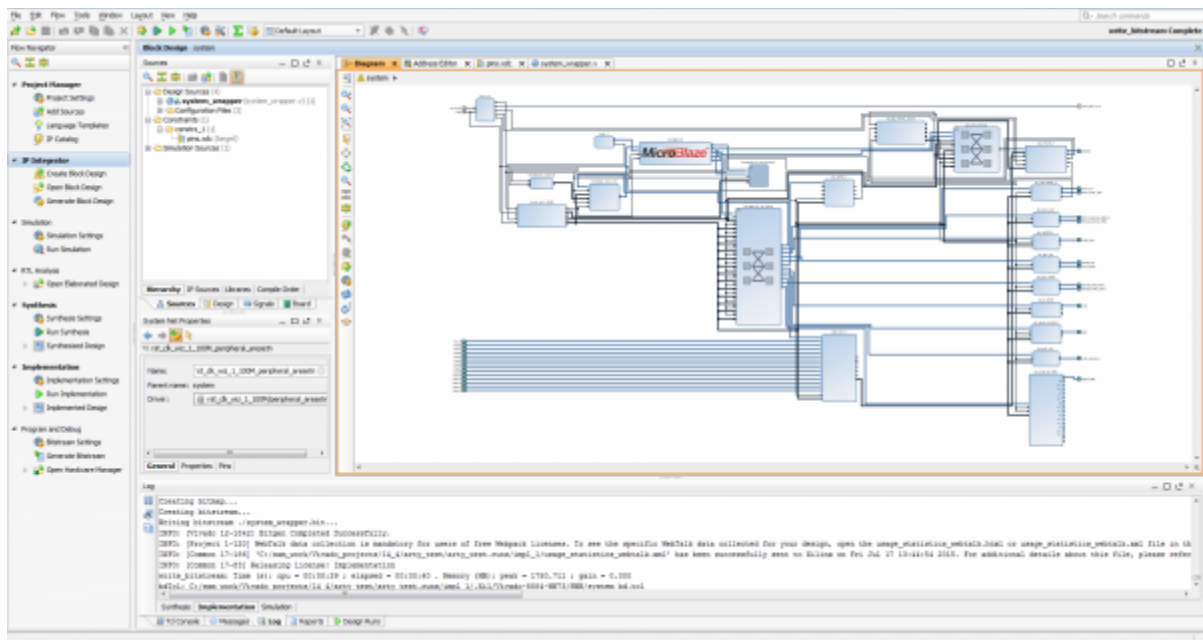


Figure 2.1 Vivado IPI

What makes the Arty A7 so flexible is its FPGA. Among their many features, FPGAs have the ability to transform into a custom software-defined System-on-a-Chip (SoC). These “Soft SoC” FPGA configurations are designed graphically using a tool called Vivado IP Integrator (Vivado IPI). In this tool, pre-built peripheral blocks are dragged from an extensive library and dropped into your processing system as you see fit. These pre-built peripherals include timers, UART/SPI/IIC controllers, and many of the other devices you would typically find in an SoC or microcontroller. Ambitious users will also find that they can create their own peripheral blocks by writing them in a Hardware Definition Language (HDL), specifically Verilog or VHDL. For those with no interest in learning HDL, the Xilinx High Level Synthesis tool can be used to define custom peripheral blocks by writing them in C.

The Arty A7's Soft SoC configurations are powered by MicroBlaze processor cores. MicroBlaze is a 32-bit RISC soft processor core, designed specifically to be used in Xilinx FPGAs. The MicroBlaze processor in an SoC configuration is typically run at 100 MHz, though it is possible to design your SoC so that it can operate at over 200MHz. The Arty A7 supports large MicroBlaze programs with demanding memory requirements by providing 16MB of non-volatile program memory and 256MB of DDR3L RAM.

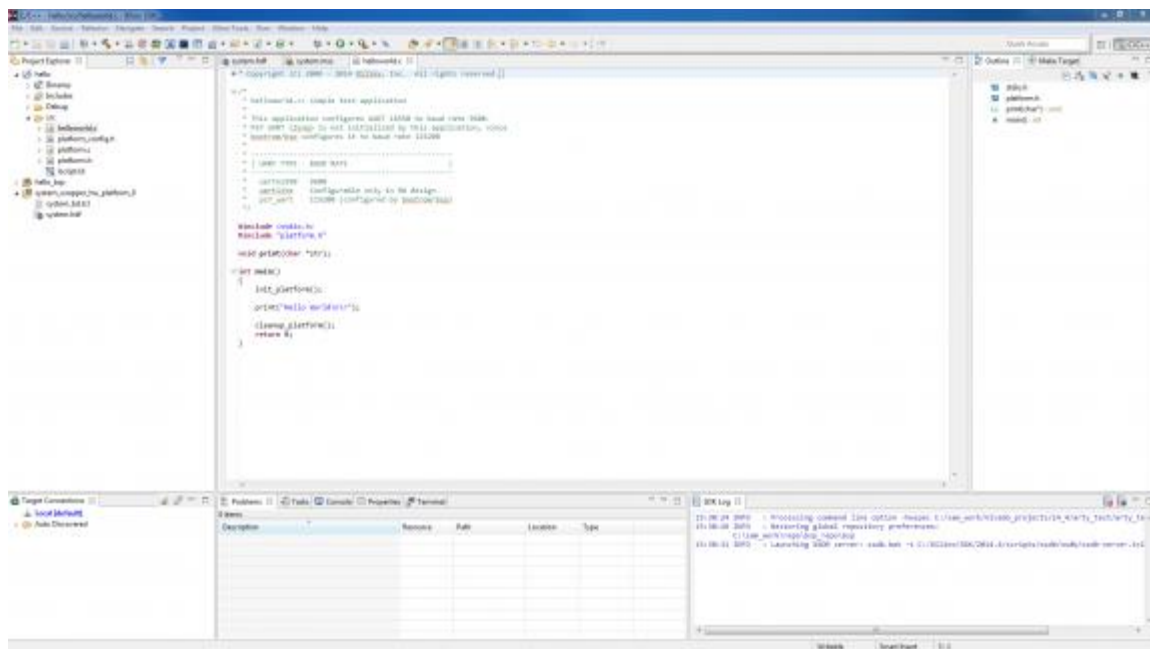


Figure 2.2 Xilinx SDK

After you design your soft SoC configuration for the Arty A7 you can start writing programs for it. This is done by exporting your SoC design out of Vivado IPI and into the Xilinx Software Development Kit (XSDK), an Integrated Development Environment (IDE) for designing/debugging MicroBlaze programs in C. After the IPI to XSDK handoff, XSDK is automatically configured to include libraries and examples for the peripheral blocks you've included in your SoC. At this point, programming the Arty is very similar to programming other SoC or microcontroller platforms: Programs are written in C, programmed into board over USB, and then optionally debugged in hardware. Soft SoC configurations and MicroBlaze programs can also be loaded into the 16MB non-volatile program memory so that they execute immediately after the Arty is powered on.

Although the Arty A7 is particularly well suited for Microblaze Soft SoC designs, it can also be programmed with a Register-Transfer Level (RTL) circuit description like any other FPGA

development platform. This design flow requires that you describe your RTL circuit using an HDL within Vivado, and it does not use the Vivado IPI or XSDK tools. Designing this way has many advantages, but is very unlike programming a single board computer, and instead is used by those familiar with FPGA design or interested in designing and implementing a digital circuit that doesn't contain a processor.

3 Power Supplies

The Arty A7 requires a 5 volt power source to operate. This power source can come from the Digilent USB-JTAG port (J10) or it can be derived from a 7 to 15 Volt DC power supply that's connected to the Power Jack (J13) or Pin 8 of Header J7.

A power-good LED (LD11), driven by the 3.3V output (VCC3V3) of the DA9062 regulator, indicates that the board is receiving power and that the onboard supplies are functioning as expected. If this LED does not illuminate when an acceptable power supply is connected, please contact your distributor or Digilent Support for further help.

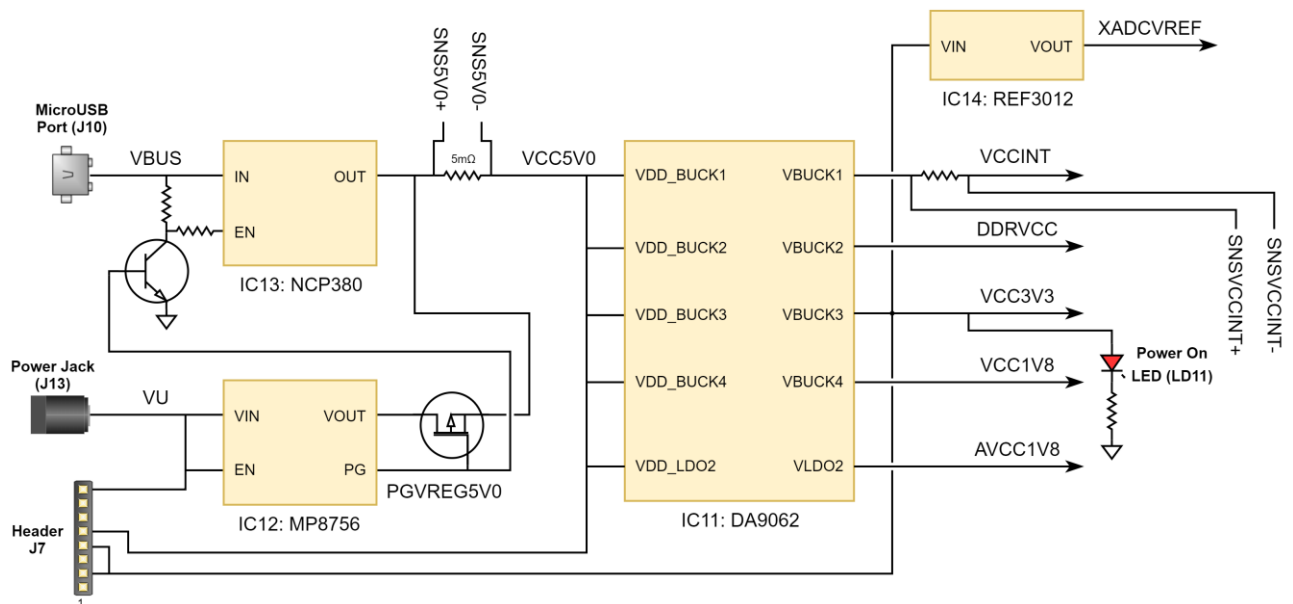


Figure 3.1 Arty A7 Power Circuit

The USB port can deliver enough power for the vast majority of designs. However, a few demanding applications, including any that drive multiple peripheral boards, might require more power than the USB port can provide. Also, some applications may need to run without being connected to a PC's USB port. In these instances an external power supply or battery pack can be used.

An external power supply can be used by plugging into Power Jack J13. The supply must use a coaxial, center-positive 2.1mm (or 2.5mm) internal-diameter plug, and provide a voltage of 7 to 15 Volts DC. The supply should provide a minimum current of 1 amp. Ideally, the supply should be capable of providing 36 Watts of power (12 Volts DC, 3 amps).

An external battery pack can be used by connecting the battery's positive terminal to pin 8 of J7 (labeled VIN) and the negative terminal to pin 7 of J7 (labeled GND), as shown in Figure 3.2. The battery must provide a voltage between 7 and 15 volts DC, and should NOT be installed while there is a supply connected to Power Jack J13.

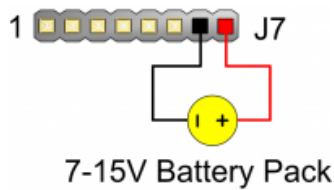


Figure 3.2 Arty A7 Battery Pack Connection

The Arty A7 uses a combination of a USB load switch (IC13), a MOSFET, (Q8), and some additional control circuitry to automatically determine the 5V power source based on the supplies that are plugged into the board. If an external supply is connected to Power Jack J13, it will be used as the input source regardless of whether or not anything is plugged into the USB port (J10). If the Arty A7 is initially powered via USB and an external supply is plugged into J13, then the the 5V power source will automatically switch over to the regulated external supply rail and no brown-out will occur. If the external supply is later disconnected from Power Jack J13 while USB power is still present, then the 5V power source will switch over to USB power, and a brown-out - which can be seen as the power-good LED toggles - will occur.

Voltage regulator circuits from Dialog Semiconductor and Texas Instruments create the required 3.3V, 1.8V, 1.35V, 1.25V, 1.00V, 0.675V supplies from the 5V power source. In the event that an external supply or battery pack is used, the on-board Monolithic Power Systems 5V regulator (IC12) provides the 5V source. Table 3.1 provides additional information (typical currents depend strongly on FPGA configuration and the values provided are typical of medium size/speed designs).

Supply	Circuits	Device	Maximum Current
5.0V	Onboard Regulators, RGB LEDs	IC13: ON Semiconductor NCP380	1.0A (5.0A) ¹⁾
3.3V	FPGA I/O, Clocks, Flash, PMODs, LEDs, Buttons, Switches, USB port, Ethernet	IC11: Dialog Semiconductor DA9062	2.0A
0.95V (1.0V) ²⁾	FPGA Core and Block RAM	IC11: Dialog Semiconductor DA9062	2.5A
1.8V	FPGA Auxiliary	IC11: Dialog Semiconductor DA9062	1.5A
1.35V	DDR3L and associated FPGA bank	IC11: Dialog Semiconductor DA9062	2.5A
0.675V	DDR3L	IC17: Diodes Incorporated AP2303	1.75A
1.25V	XADC Analog Reference	IC14: Texas Instruments REF3012	25mA

Table 3.1. Arty A7 Power Rails.

1) With external power provided via Power Jack J13

2) Arty A7-100 variant value in parentheses

3.1 External Supply Voltage Monitoring

The Arty A7 includes circuitry for monitoring the voltage of an external supply connected to Power Jack J13 or an external battery pack connected to Header J7. A voltage divider is used to scale the unregulated input voltage, VU, to be within the range (0-1V) that the on-chip 12-bit ADC is capable of measuring. The unregulated input voltage, VU, is divided by 16 and then fed into Auxiliary Channel 2 on the XADC of the Artix-7. Applications that wish to monitor the voltage of an external supply may configure Channel 2 of the XADC as a unipolar input and perform a conversion to receive a digital value corresponding to the input voltage. Figure 3.1.1 provides an overview of the circuitry that allows an external supply voltage to be monitored.

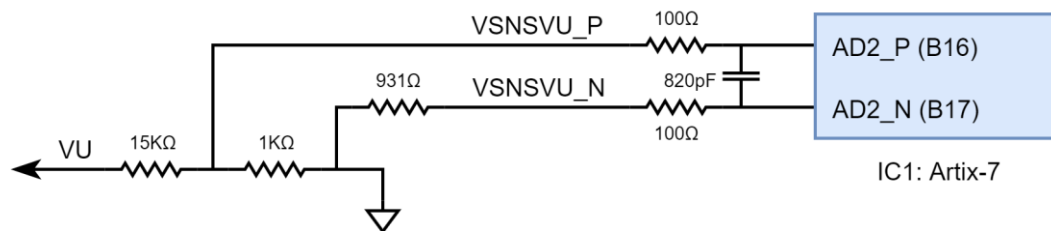


Figure 3.1.1 Monitoring External Supply Voltage

3.2 FPGA Core Supply Current Monitoring

The Arty A7 includes circuitry for monitoring the current consumed by the FPGA core. The current is monitored by measuring the voltage across a 10 milliohm sense resistor that's placed between the output of the DC-DC converter system (IC11, Channel 1) and the VCCINT network. A current sense amplifier (IC16, Texas Instruments INA199A1) connected across the sense resistor provides a gain of 50 and produces an output voltage of 500 millivolts per amp of current. Currents above 2 Amps will not damage the circuit or the FPGA, but will be reported as 2 Amps. The output of the current sense amplifier is fed into Auxiliary Channel 10 on the XADC of the Artix-7 FPGA. Applications that wish to monitor the current consumption of the FPGA Core and Block RAM may configure Channel 10 of the XADC as a unipolar input and perform a conversion to receive a digital value that corresponds to the amplified sense resistor voltage. This current sense circuit is capable of measuring current between 0 and 2 Amps. Figure 3.2.1 provides an overview of the circuitry that allows the FPGA Core Supply current to be monitored.

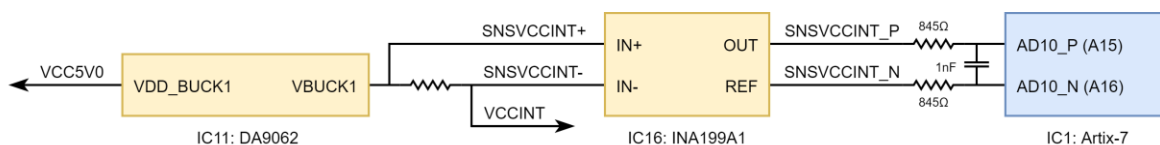


Figure 3.2.1 FPGA Core Supply Current Monitoring

3.3 5V Supply Power Monitoring

The Arty A7 includes circuitry for monitoring the voltage of the 5 Volt supply as well as the current consumed from this supply. A voltage divider is used to scale the 5V input voltage to be within the range (0-1V) that the on-chip 12-bit ADC is capable of measuring. The 5V supply voltage is divided by 5.99 and then fed into Auxiliary Channel 1 on the XADC of the Artix-7 FPGA. A combination of a 5 milliohm current sense resistor and a current sense amplifier (IC15, Texas Instruments INA199A1) are used to produce an output voltage of 250 millivolts per amp of current. This current sense circuit is capable of measuring current between 0 and 2 Amps. Currents above 4 Amps will not damage the circuit or the FPGA, but will be reported as only 4 Amps. The output of the current sense amplifier is

fed into Auxiliary Channel 9 on the XADC of the Artix-7 FPGA. Applications that wish to monitor the instantaneous power consumption of the Arty A7 may configure Channels 1 and 9 of the XADC as unipolar inputs and then perform a simultaneous conversion of the two channels to receive digital values that can be used to compute the instantaneous power consumption. Figure 3.3.1 provides an overview of the circuitry that allows the 5V supply power consumption to be monitored.

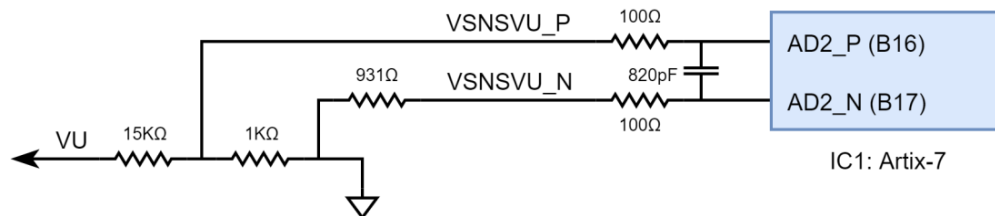


Figure 3.3.1 5V Supply Power Monitoring

4 FPGA Configuration

After power-on, the Artix-7 FPGA must be configured (or programmed) before it can perform any functions. You can configure the FPGA in one of four ways:

A PC can use the Digilent USB-JTAG circuitry (port J10) to program the FPGA any time the power is on.

A file stored in the nonvolatile serial (SPI) flash device can be transferred to the FPGA using the SPI port.

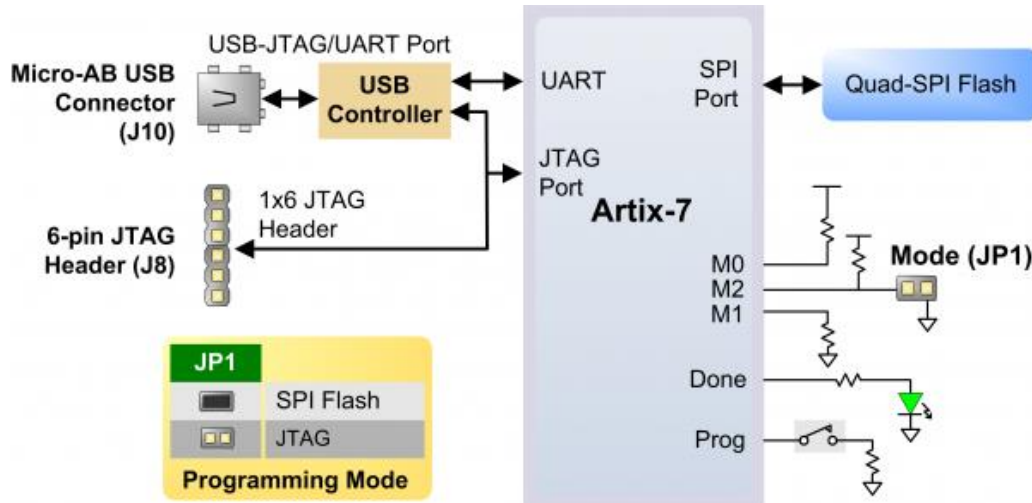


Figure 4.1 Arty A7 Configuration

Figure 4.1 shows the different options available for configuring the FPGA. An on-board “mode” jumper (JP1) selects whether the FPGA will be programmed by the Quad-SPI flash on power up.

The FPGA configuration data is stored in files called bitstreams that have the .bit file extension. The ISE or Vivado software from Xilinx can create bitstreams from VHDL, Verilog®, or schematic-based source files (in the ISE toolset, EDK is used for MicroBlaze™ embedded processor-based designs).

Bitstreams are stored in volatile memory cells within the FPGA. This data defines the FPGA’s logic functions and circuit connections, and it remains valid until it is erased by removing board power, by

pressing the reset button attached to the PROG input, or by writing a new configuration file using the JTAG port.

An Artix-7 35T bitstream is typically 17,536,096 bits. The time it takes to program the Arty A7 can be decreased by compressing the bitstream before programming, and then allowing the FPGA to decompress the bitstream itself during configuration. Depending on design complexity, compression ratios of 10x can be achieved. Bitstream compression can be enabled within the Xilinx tools (ISE or Vivado) to occur during generation. For instructions on how to do this, consult the Xilinx documentation for the toolset being used.

After being successfully programmed, the FPGA will cause the “DONE” LED to illuminate. Pressing the “PROG” button at any time will reset the configuration memory in the FPGA. After being reset, the FPGA will immediately attempt to reprogram itself from whatever method has been selected by the programming mode jumpers.

The following sections provide greater detail about programming the Arty A7 using the different methods available.

4.1 JTAG Configuration

The Xilinx tools typically communicate with FPGAs using the Test Access Port and Boundary-Scan Architecture, commonly referred to as JTAG. During JTAG programming, a .bit file is transferred from the PC to the FPGA using the onboard Digilent USB-JTAG circuitry (port J10) or an external JTAG programmer, such as the Digilent JTAG-HS2, attached to port J8. You can perform JTAG programming any time after the Arty A7 has been powered on, regardless of whether the mode jumper (JP1) is set. If the FPGA is already configured, then the existing configuration is overwritten with the bitstream being transmitted over JTAG. Not setting the mode jumper (seen in Figure 4.1) is useful to prevent the FPGA from being configured from Quad-SPI Flash until a JTAG programming occurs.

Programming the Arty A7 with an uncompressed bitstream using the on-board USB-JTAG circuitry usually takes around 6 seconds. JTAG programming can be done using the hardware manager in Vivado or the iMPACT tool included with ISE.

4.2 Quad-SPI Configuration

Since the FPGA's memory on the Arty A7 is volatile, it relies on the Quad-SPI flash memory to store the configuration between power cycles. This configuration mode is called Master SPI. The blank FPGA takes the role of master and reads the configuration file out of the flash device upon power-up. To that effect, a configuration file needs to be downloaded first to the flash. When programming a nonvolatile flash device, a bitstream file is transferred to the flash in a two-step process. First, the FPGA is programmed with a circuit that can program flash devices, and then data is transferred to the flash device via the FPGA circuit (this complexity is hidden from the user by the Xilinx tools). This is called indirect programming. After the flash device has been programmed, it can automatically configure the FPGA at a subsequent power-on or reset event as determined by the mode jumper setting (see Figure 4.1). Programming files stored in the flash device will remain until they are overwritten, regardless of power-cycle events.

Programming the flash can take as long as four to five minutes, which is mostly due to the lengthy erase process inherent to the memory technology. Once written however, FPGA configuration can be very fast—less than a second. Bitstream compression, SPI bus width, and configuration rate are

factors controlled by the Xilinx tools that can affect configuration speed. The Arty A7 supports x1, x2, and x4 bus widths and data rates of up to 50 MHz for Quad-SPI programming.

Quad-SPI programming can be done using the hardware manager in Vivado or with the iMPACT tool included with ISE.

5 Memory

The Arty A7 contains two external memories: a 256MB DDR3L SDRAM and a 128Mb (16MB) non-volatile serial Flash device. The DDR3L module is connected to the FPGA using the industry standard interface. The serial Flash is on a dedicated quad-mode (x4) SPI bus. The connections and pin assignments between the FPGA and external memories are shown below.

5.1 DDR3L

The Arty includes one MT41K128M16JT-125 memory component, creating a single rank, 16-bit wide interface. It is routed to a 1.35V-powered HR (High Range) FPGA bank with 50 ohm controlled single-ended trace impedance. 50 ohm internal terminations in the FPGA are used to match the trace characteristics. Similarly, on the memory side, on-die terminations (ODT) are used for impedance matching.

For proper operation of the memory, a memory controller and physical layer (PHY) interface needs to be included in the FPGA design. The easiest way to accomplish this on the Arty A7 is to use the Xilinx 7-series memory interface solutions core generated by the MIG (Memory Interface Generator) Wizard. Depending on the tool used (ISE, EDK or Vivado), the MIG Wizard can generate a native FIFO-style or an AXI4 interface to connect to user logic. This workflow allows the customization of several DDR parameters optimized for the particular application. Table 2 below lists the MIG Wizard settings optimized for the Arty.

Table 2. DDR3L settings for the Arty A7.

Setting	Value
Memory type	DDR3 SDRAM
Max. clock period	3000ps (667Mbps data rate)
Memory part	MT41K128M16JT-125
Memory Voltage	1.35V
Data width	16
Data mask	Enabled
Recommended Input Clock Period 6000 ps (166.667 MHz)	
Output Driver Impedance Control	RZQ/6
Controller Chip Select pin	Enabled
Rtt (nominal) – On-die termination	RZQ/6
Internal Vref	Enabled

Internal termination impedance 50ohms

The MIG Wizard will require the fixed pin-out of the memory signals to be entered and validated before generating the IP core. For your convenience, an importable UCF file is provided on the Arty A7 Resource Center to speed up this process. It is included in the “MIG Project” design resource download. This download also includes a .prj file that can be imported into the wizard to automatically configure it with the options found in Table 2.

For more details on the Xilinx MIG, refer to the 7 Series FPGAs Memory Interface Solutions User Guide (ug586).

5.2 Quad-SPI Flash

FPGA configuration files can be written to the Quad-SPI Flash (Spansion part number S25FL128SAGMF100), and setting the mode jumper will cause the FPGA to automatically read a configuration from this device at power on. An Artix-7 35T configuration file requires 17,536,096 bits of memory, leaving about 87% of the flash device (or ~14MB) available for user data. A common use for this extra memory is to store Microblaze programs too big to fit in the onboard Block memory (typically 128 KB). These programs are then loaded and executed using a smaller bootloader program that can fit in the block memory. It is possible to automatically generate this bootloader, roll it into a single file (called an .mcs file) that also contains the bitstream and your custom Microblaze application, and program this file into SPI Flash using Xilinx SDK and Vivado. Xilinx Answer Record 63605 explains how to do this.

The contents of the memory can be manipulated by issuing certain commands on the SPI bus. The implementation of this protocol is outside the scope of this document. All signals in the SPI bus are general-purpose user I/O pins after FPGA configuration. On other boards, SCK is an exception because it remains a dedicated pin even after configuration, however, on the Arty A7 the SCK signal is routed to an additional general purpose pin that can be accessed after configuration (see Figure below). This allows access to this pin without having to instantiate the special FPGA primitive called STARTUPE2.

Xilinx's AXI Quad SPI core can be used to read/write the flash in a Microblaze design. Refer to Xilinx's product guide for this core to learn more about using it, or to Micron's datasheet for the flash device to learn how to implement a custom controller.

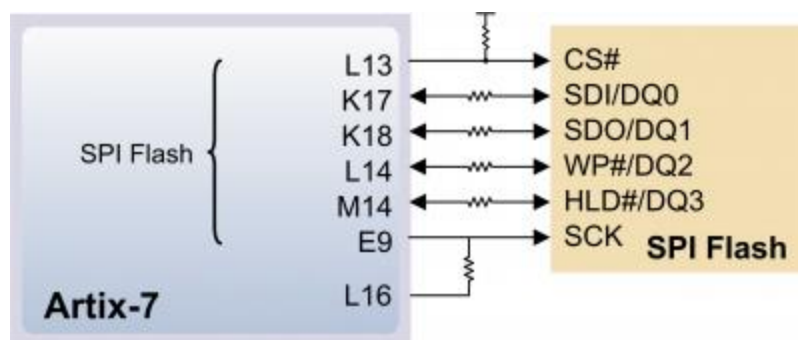


Figure 5.2.1 Arty A7 SPI Flash

The Arty A7 includes a Texas Instruments 10/100 Ethernet PHY (TI part number DP83848J) paired with an RJ-45 Ethernet jack with integrated magnetics and indicator LEDs. The TI PHY uses the MII interface and supports 10/100 Mb/s. Figure 5 illustrates the pin connections between the Artix-7 and the Ethernet PHY. At power-on reset, the PHY is set to the following defaults:

II mode interface

Auto-negotiation enabled, advertising all 10/100 mode capable

PHY address=00001

LED Mode 2

Two LEDs found in the Ethernet connector (J9) are connected to the PHY to provide link status and data activity feedback. See the PHY datasheet for details. Note that it is normal for one LED to be illuminated and one to be off, even when not using the Ethernet PHY.

Vivado IPI based designs can access the PHY using either the AXI EthernetLite IP core, the AXI 1G/2.5G Ethernet Subsystem IP core, or the Tri Mode Ethernet MAC IP core. A 25 MHz clock needs to be generated for the X1 pin of the external PHY, labeled ETH_REF_CLK in the Arty A7 schematic. To learn how to properly use the Ethernet PHY in a Microblaze design on the Arty, refer to the Getting Started with Microblaze Servers tutorial on the Arty A7 Resource Center.

For further information on the Ethernet PHY, refer to the DP83848J data sheet.

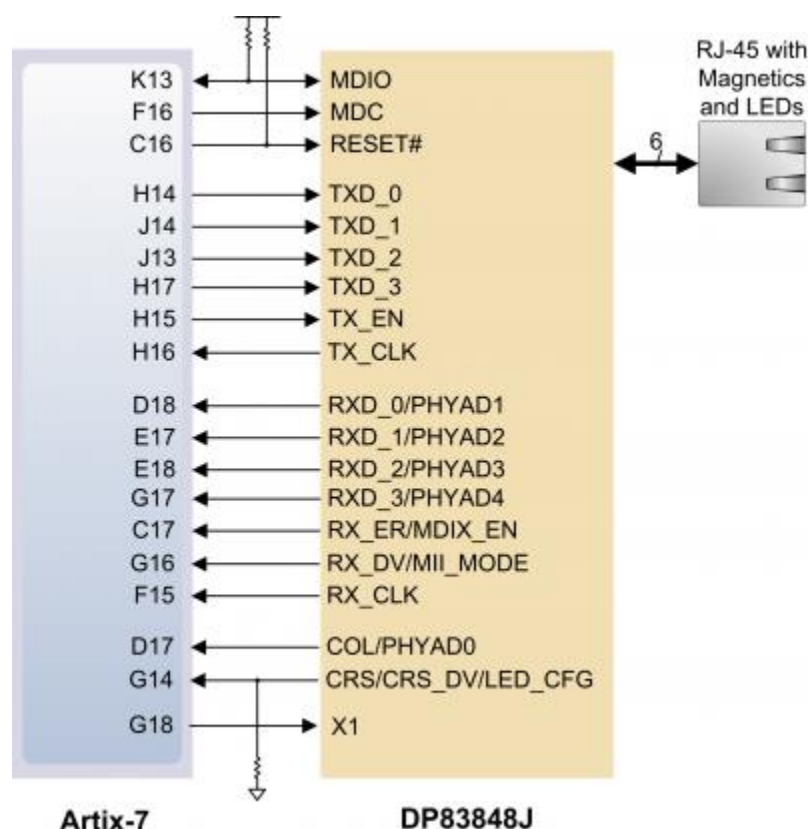


Figure 6.1 Arty A7 Ethernet

The Arty A7 includes a single 100 MHz crystal oscillator connected to pin E3 (E3 is a MRCC input on bank 35). The input clock can drive MMCMs or PLLs to generate clocks of various frequencies and with known phase relationships that may be needed throughout a design. Some rules restrict which MMCMs and PLLs may be driven by the 100 MHz input clock. For a full description of these rules and of the capabilities of the Artix-7 clocking resources, refer to the “7 Series FPGAs Clocking Resources User Guide” available from Xilinx.

Xilinx offers the Clocking Wizard IP core to help users generate the different clocks required for a specific design. This wizard will properly instantiate the needed MMCMs and PLLs based on the desired frequencies and phase relationships specified by the user. The wizard will then output an easy-to-use wrapper component around these clocking resources that can be inserted into the user’s design. The clocking wizard can be accessed from within the Project Navigator or Core Generator tools.

8 USB-UART Bridge (Serial Port)

The Arty A7 includes an FTDI FT2232HQ USB-UART bridge (attached to connector J10) that allows you use PC applications to communicate with the board using standard Windows COM port commands. Free USB-COM port drivers, available from www.ftdichip.com under the “Virtual Com Port” or VCP heading, convert USB packets to UART/serial port data. Serial port data is exchanged with the FPGA using a two-wire serial port (TXD/RXD). After the drivers are installed, I/O commands can be used from the PC directed to the COM port to produce serial data traffic on the A9 and D10 FPGA pins.

Two on-board status LEDs provide visual feedback on traffic flowing through the port: the transmit LED (LD10) and the receive LED (LD9). Signal names that imply direction are from the point-of-view of the DTE (Data Terminal Equipment), in this case the PC.

The FT2232HQ is also used as the controller for the Digilent USB-JTAG circuitry, but the USB-UART and USB-JTAG functions behave entirely independent of one another. Programmers interested in using the UART functionality of the FT2232 within their design do not need to worry about the JTAG circuitry interfering with the UART data transfers, and vice-versa. The combination of these two features into a single device allows the Arty A7 to be programmed, communicated with via UART, and powered from a computer attached with a single Micro USB cable.

The CK_RST signal (see the Arty A7 Schematic) is also connected to the FT2232HQ device via JP2. When JP2 is shorted, the FT2232HQ can trigger a Microblaze reset, mimicking the behavior of Arduino and chipKIT boards when sketches are loaded. Note the CK_RST signal is also connected to the red RESET button and the RST pin of J7 on the shield connector (these connections are not shown in the figure below).

The connections between the FT2232HQ and the Artix-7 are shown in Figure 6.

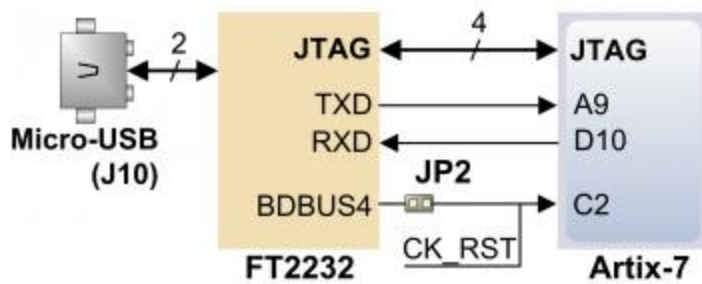


Figure 8.1 Arty A7 UART

9 Basic I/O

The Arty A7 includes four tri-color LEDs, 4 switches, 4 push buttons, 4 individual LEDs, and a reset button, as shown in Figure 16. The push buttons and slide switches are connected to the FPGA via series resistors to prevent damage from inadvertent short circuits (a short circuit could occur if an FPGA pin assigned to a push button or slide switch was inadvertently defined as an output). The four push buttons are “momentary” switches that normally generate a low output when they are at rest, and a high output only when they are pressed. Slide switches generate constant high or low inputs depending on their position.

The red reset button labeled “RESET” generates a high output when at rest and a low output when pressed. The RESET button is intended to be used in Microblaze designs to reset the processor, but you can also use it as a general purpose push button. Note that it is also tied to the RST pin on J7 of the shield connector and to the FT2232 UART device via JP2, though these connections are not shown in the figure below.

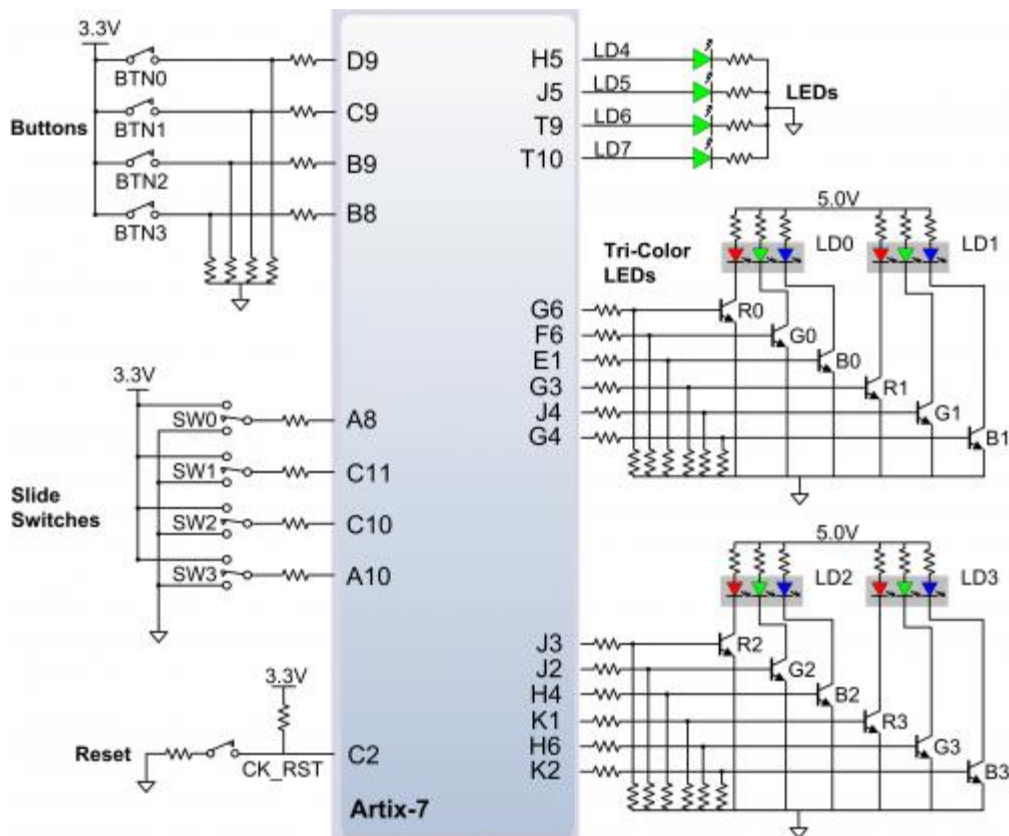


Figure 9.1 Arty A7 GPIO

The four individual high-efficiency LEDs are anode-connected to the FPGA via 330-ohm resistors, so they will turn on when a logic high voltage is applied to their respective I/O pin. Additional LEDs that are not user-accessible indicate power-on, FPGA programming status, and USB and Ethernet port status.

9.1 Tri-Color LEDs

The Arty A7 contains four tri-color LEDs. Each tri-color LED has three input signals that drive the cathodes of three smaller internal LEDs: one red, one blue, and one green. Driving the signal corresponding to one of these colors high will illuminate the internal LED. The input signals are driven by the FPGA through a transistor, which inverts the signals. Therefore, to light up the tri-color LED, the corresponding signals need to be driven high. The tri-color LED will emit a color dependent on the combination of internal LEDs that are currently being illuminated. For example, if the red and blue signals are driven high and green is driven low, the tri-color LED will emit a purple color.

Note: Digilent strongly recommends the use of pulse-width modulation (PWM) when driving the tri-color LEDs. Driving any of the inputs to a steady logic '1' will result in the LED being illuminated at an uncomfortably bright level. You can avoid this by ensuring that none of the tri-color signals are driven with more than a 50% duty cycle. Using PWM also greatly expands the potential color palette of the tri-color led. Individually adjusting the duty cycle of each color between 50% and 0% causes the different colors to be illuminated at different intensities, allowing virtually any color to be displayed.

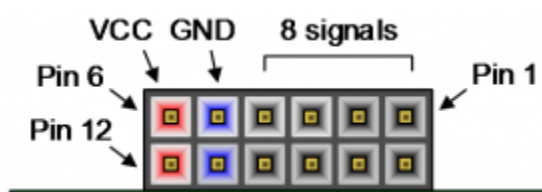
10 Pmod Connectors

Pmod connectors are 2×6, right-angle, 100-mil spaced female connectors that mate with standard 2×6 pin headers. Each 12-pin Pmod connector provides two 3.3V VCC signals (pins 6 and 12), two Ground signals (pins 5 and 11), and eight logic signals, as shown in Fig. 16. The VCC and Ground pins can deliver up to 1A of current, but care must be taken not to exceed any of the power budgets of the onboard regulators or the external power supply (these are described in the “Power supplies” section).

Warning: Since the Pmod pins are connected to Artix-7 FPGA pins using a 3.3V logic standard, care should be taken not to drive these pins over 3.4V.

Digilent produces a large collection of Pmod accessory boards that can attach to the Pmod expansion connectors to add ready-made functions like A/D's, D/A's, motor drivers, sensors, and other functions. See www.digilentinc.com for more information.

The Arty A7 has four Pmod connectors, some of which behave differently than others. Each Pmod connector falls into one of two categories: standard or high-speed. Table 4 specifies which category each Pmod falls into, and also lists the FPGA pins they are connected to. The following sections describe the different types of Pmods.



	Pmod JA	Pmod JB	Pmod JC	Pmod JD
Pmod Type	Standard	High-Speed	High-Speed	Standard
Pin 1	G13	E15	U12	D4
Pin 2	B11	E16	V12	D3
Pin 3	A11	D15	V10	F4
Pin 4	D12	C15	V11	F3
Pin 7	D13	J17	U14	E2
Pin 8	B18	J18	V14	D2
Pin 9	A18	K15	T13	H2
Pin 10	K16	J15	U13	G2

10.1 Standard Pmod

The standard Pmod connectors are connected to the FPGA via 200 Ohm series resistors. The series resistors prevent short circuits that can occur if the user accidentally drives a signal that is supposed to be used as an input. The downside to this added protection is that these resistors can limit the maximum switching speed of the data signals. If the Pmod being used does not require high-speed access, then the standard Pmod connector should be used to help prevent damage to the devices.

10.2 High-Speed Pmod

The High-speed Pmods use the standard Pmod connector, but have their data signals routed as impedance matched differential pairs for maximum switching speeds. They have pads for loading resistors for added protection, but the Arty A7 ships with these loaded as 0-Ohm shunts. With the series resistors shunted, these Pmods offer no protection against short circuits, but allow for much faster switching speeds. The signals are paired to the adjacent signals in the same row: pins 1 and 2, pins 3 and 4, pins 7 and 8, and pins 9 and 10.

Traces are routed 100 ohm (+/- 10%) differential.

These connectors should be used only when high speed differential signaling is required or the other Pmods are all occupied. If used as single-ended, coupled pairs may have significant crosstalk. In applications where this is a concern, the standard Pmod connector shall be used. Another option would be to ground one of the signals (drive it low from the FPGA) and use its pair for the signal-ended signal.

Since the High-Speed Pmods have 0-ohm shunts instead of protection resistors, the operator must take precaution to ensure that they do not cause any shorts.

11 Arduino/chipKIT Shield Connector

The Arty A7 can be connected to standard Arduino and chipKIT shields to add extended functionality. Special care was taken while designing the Arty to make sure it is compatible with the majority of Arduino and chipKIT shields on the market. The shield connector has 49 pins connected to the FPGA for general purpose Digital I/O. Due to the flexibility of FPGAs, it is possible to use these

pins for just about anything including digital read/write, SPI connections, UART connections, I2C connections, and PWM. Six of these pins (labeled AN0-AN5) can also be used as single-ended analog inputs with an input range of 0V-3.3V, and another six (labeled AN6-11) can be used as differential analog inputs.

Warning: The Arty A7 is not compatible with shields that output 5V digital or analog signals. Driving pins on the shield connector above 3.4V may cause damage to the FPGA.

Figure 11.1 diagrams the pins found on the shield connector of the Arty A7.

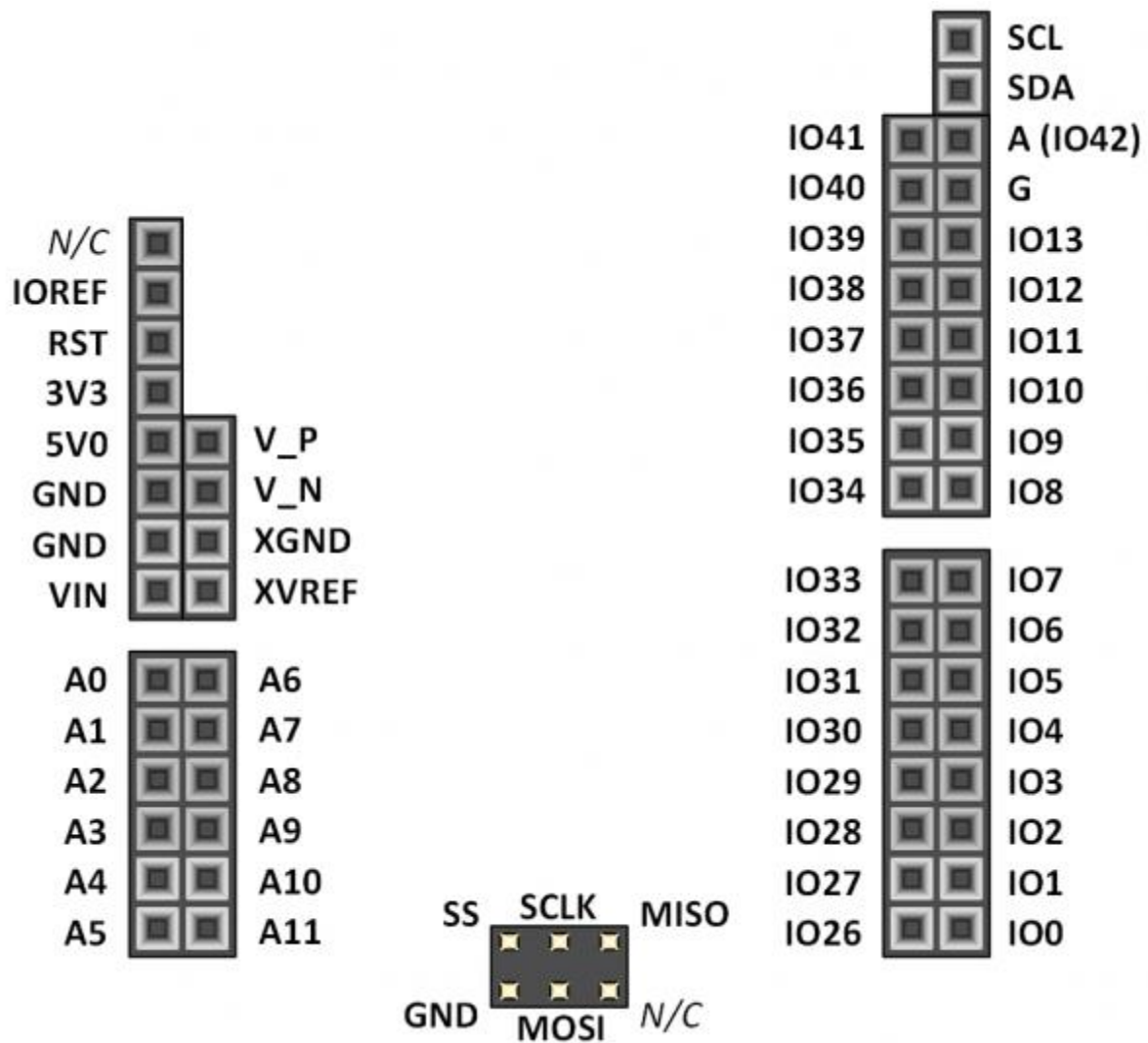


Figure 11.1 Arty A7 Shield Connector Pin Diagram

Pin Name	Shield Function	Arty A7 Connection
IO0-IO13, IO26-IO41, A (IO42)	General purpose I/O pins	See Section titled "Shield Digital I/O"
SCL	I2C Clock	See Section titled "Shield Digital I/O"
SDA	I2C Data	See Section titled "Shield Digital I/O"

Pin Name	Shield Function	Arty A7 Connection
SCLK	SPI Clock	See Section titled “Shield Digital I/O”
MOSI	SPI Data out	See Section titled “Shield Digital I/O”
MISO	SPI Data in	See Section titled “Shield Digital I/O”
SS	SPI Slave Select	See Section titled “Shield Digital I/O”
A0-A5	Single-Ended Analog Input	See Section titled “Shield Analog I/O”
A6-A11	Differential Analog Input	See Section titled “Shield Analog I/O”
V_P, V_N	Dedicated Differential Analog Input	See Section titled “Shield Analog I/O”
XGND	XADC Analog Ground	Connected to net used to drive the XADC ground reference on the FPGA (VREFN)
XVREF	XADC Analog Voltage Reference	Connected to 1.25 V, 25mA rail used to drive the XADC voltage reference on the FPGA (VREFP)
N/C	Not Connected	Not Connected
IOREF	Digital I/O Voltage reference	Connected to the 3.3V Power Rail (See the “Power Supplies” section)
RST	Reset to Shield	Connected to the red “RESET” button and a Digital I/O of the FPGA. When JP2 is shorted, it is also connected to the DTR signal of the FTDI USB-UART bridge.
3V3	3.3V Power Rail	Connected to the 3.3V Power Rail (See the “Power Supplies” section)
5V0	5.0V Power Rail	Connected to the 5.0V Power Rail (See the “Power Supplies” section)
GND, G	Ground	Connected to the ground plane
VIN	Power Input	Connected in parallel with the external power supply connector (J13). See the “Power Supplies” section for information on powering the Arty A7 from this pin.

11.1 Shield Digital I/O

The pins connected directly to the FPGA can be used as general purpose inputs or outputs. These pins include the I2C, SPI, and general purpose I/O pins. There are 200 Ohm series resistors between the FPGA and the digital I/O pins to help provide protection against accidental short circuits. The absolute maximum and recommended operating voltages for these pins are outlined in the table below.

	Absolute Minimum Voltage	Recommended Minimum Operating Voltage	Recommended Maximum Operating Voltage	Absolute Maximum Voltage
Powered	-0.4 V	-0.2 V	3.4 V	3.75 V
Unpowered	-0.4 V	N/A	N/A	0.55 V

For more information on the electrical characteristics of the pins connected to the FPGA, please see the Artix-7 datasheet from Xilinx.

11.2 Shield Analog I/O

The pins labeled A0-A11 and V_P/V_N are used as analog inputs to the XADC module of the FPGA. The FPGA expects that the inputs range from 0-1 V. On the pins labeled A0-A5 we use an external circuit to scale down the input voltage from 3.3V. This circuit is shown in Figure 11.2.1. This circuit allows the XADC module to accurately measure any voltage between 0V and 3.3V (relative to the Arty A7's GND) that is applied to any of these pins. If you wish to use the pins labeled A0-A5 as Digital inputs or outputs, they are also connected directly to the FPGA before the resistor divider circuit (also shown in Figure 11.2.1).

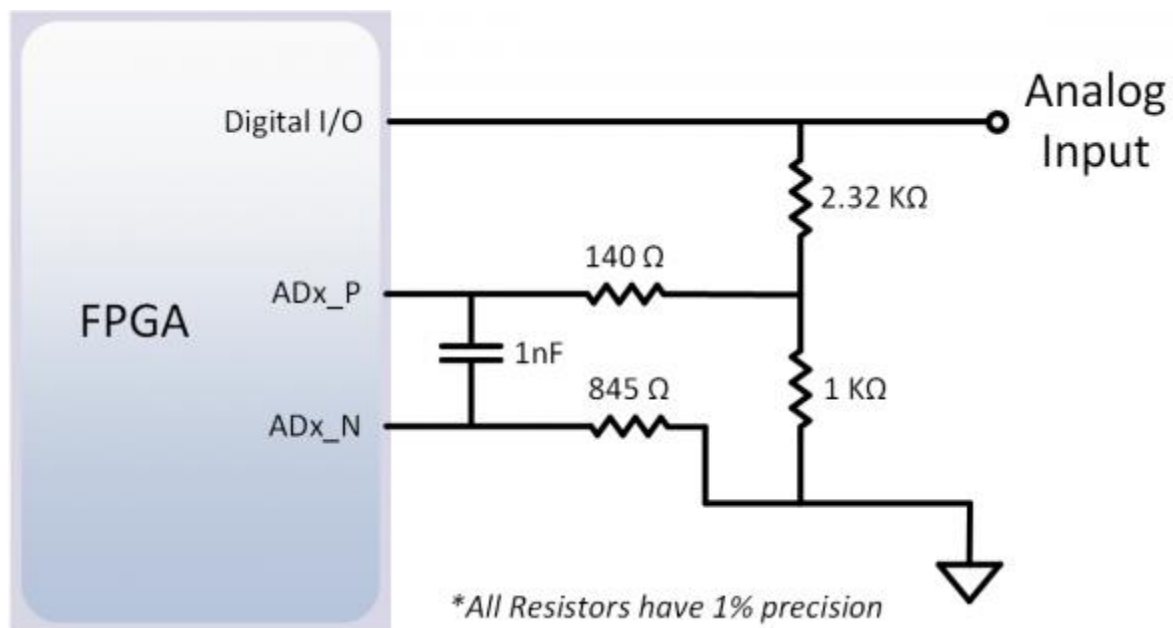


Figure 11.2.1 Arty A7 Single-Ended Analog Inputs

The pins labeled A6-A11 are connected directly to 3 pairs of analog capable pins on the FPGA via an anti-aliasing filter. This circuit is shown in Figure 11.2.2. These pairs of pins can be used as differential analog inputs with a voltage difference between 0-1V. The even numbers are connected to the positive pins of the pair and the odd numbers are connected to the negative pins (so A6 and A7 form an analog input pair with A6 being positive and A7 being negative). Note that though the pads for the capacitor are present, they are not loaded for these pins. Since the analog capable pins of the FPGA can also be used like normal digital FPGA pins, it is also possible to use these pins for Digital I/O.

The pins labeled V_P and V_N are connected to the VP_0 and VN_0 dedicated analog inputs of the FPGA. This pair of pins can also be used as a differential analog input with voltage between 0-1V, but

they cannot be used as Digital I/O. The capacitor in the circuit shown in Figure 11.2.2 for this pair of pins is loaded on the Arty.

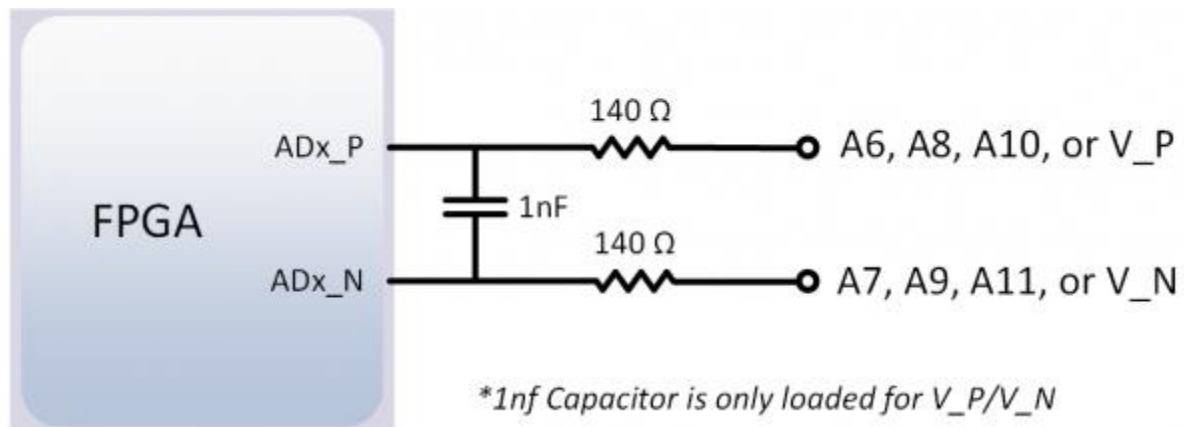


Figure 11.2.2 Arty A7 Differential Analog Inputs

The XADC core within the Artix-7 is a dual channel 12-bit analog-to-digital converter capable of operating at 1 MSPS. Either channel can be driven by any of the analog inputs connected to the shield pins. The XADC core is controlled and accessed from a user design via the Dynamic Reconfiguration Port (DRP). The DRP also provides access to voltage monitors that are present on each of the FPGA's power rails, and a temperature sensor that is internal to the FPGA. For more information on using the XADC core, refer to the Xilinx document titled 7 Series FPGAs and Zynq-7000 All Programmable SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter. A demo that uses the XADC core is available on the Arty A7 Resource Center.

https://reference.digilentinc.com/reference/programmable-logic/arty-a7/reference-manual?_ga=2.245609412.1739733833.1570020700-2034427845.1554910082