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Bachelor Thesis

Development of a PoC for a PCIe based Automotive Zonal Architecture

Computer Science

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I hereby declare that I have written the present thesis titled *Development of a PoC for a PCIe based Automotive Zonal Architecture* independently and have used no sources or aids other than those stated. Furthermore, I confirm that the submitted electronic version corresponds to the printed version.

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Achkowledgement

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Acronyms

BDF	Bus Device Function
CPU	Central Processing Unit
CRC	Cyclic Redundancy Check
DLLP	Data Link Layer Packet
DW	Double Word
ECRC	End-to-End Cyclic Redundancy Check
EISA	Enhanced Industry Standard Architecture
FEC	Forward Error Correction
FLIT	Flow Control Unit
GT/s	Gigatransfers per Second
ISA	Industry Standard Architecture
LCRC	Link Cyclic Redundancy Check
PAM4	Pulse Amplitude Modulation 4-level
PCI	Peripheral Component Interconnect
PCIe	Peripheral Component Interconnect Express
PCI-SIG	PCI Special Interest Group
PCI-X	Peripheral Component Interconnect Extended
QoS	Quality of Service
TLP	Transaction Layer Packet
VESA	Video Electronics Standards Association
VLB	VESA Local Bus

Abstract

1 Introduction

1.1 Motivation

1.2 Problem

1.3 Solution Approach

2 State of the Art

2.1 Peripheral Component Interconnect Express

The following section provides an overview of the PCIe protocol, its architecture, its history, and its role in modern computing systems. Additionally, it will discuss the advancements in PCIe technology and its impact on data transfer rates and system performance.

2.1.1 History and Fundamentals

PCIe is a high-speed serial computer expansion bus standard designed to replace the older Peripheral Component Interconnect (PCI) and Peripheral Component Interconnect Extended (PCI-X) standards. In order to understand the evolution of PCIe, it is essential to first understand the principles of its predecessors, PCI and PCI-X.

The development of modern computer bus architectures has been driven by the growing demand for higher bandwidth, lower latency, and better power efficiency (Budruk et al. 2003). This progression has led to significant advancements in how peripherals communicate with computer systems, culminating in the development of PCIe as a dominant interconnect technology.

Evolution of Computer Bus Architectures

The history of computer expansion bus technology represents a continuous evolution toward greater speeds, wider data paths, and enhanced functionality. Early personal computers utilized the Industry Standard Architecture (ISA) bus, introduced with the IBM PC/AT in 1984 (Messmer n.d.). While functional, ISA operated at just 8MHz with an 8-bit or 16-bit data path, creating a significant bottleneck as processor and peripheral speeds increased.

In response to these limitations, several interim standards emerged, including VESA Local Bus (VLB) and the Enhanced Industry Standard Architecture (EISA) (Abbott 2003, pp. 9-10). However, these solutions were eventually superseded by PCI, which offered a more scalable and processor-independent approach to peripheral connectivity.

PCI and PCI-X

PCI was introduced by Intel in 1992 as a replacement for the Industry Standard Architecture (ISA) bus (Shanley and Anderson 1999). PCI operated as a parallel bus architecture with a 33 MHz clock speed and 32-bit data width, providing a maximum theoretical bandwidth of 133 MB/s (Shanley 2000). This represented a significant improvement over previous standards, enabling more efficient communication between the Central Processing Unit (CPU) and peripheral devices.

The design philosophy behind PCI was revolutionary for its time, introducing several key innovations (Abbott 2003, pp. 11, 92-105, 189):

- **Processor independence**: Unlike earlier buses that were tightly coupled to the CPU's architecture, PCI was designed to be processor-agnostic.
- **Bus mastering**: PCI devices could take control of the bus and initiate transactions without CPU intervention, significantly improving multitasking capabilities.
- **Plug and Play**: PCI introduced automated device configuration, eliminating the need for manual jumper settings that plagued earlier expansion cards.

As computing demands increased, the PCI standard evolved into PCI-X in 1998 (Shanley 2000). PCI-X maintained backward compatibility while increasing the bus frequency to 66 MHz, 133 MHz, and eventually 533 MHz in PCI-X 2.0, enabling theoretical bandwidths of up to 4.3 GB/s. The PCI-X standard was developed specifically to address the growing bandwidth demands of server applications, particularly for high-performance network and storage interfaces (Shanley 2000).

However, both PCI and PCI-X faced inherent limitations due to their parallel bus architecture:

- **Signal integrity issues**: As frequencies increased, maintaining signal integrity across multiple parallel lines became increasingly challenging (Wilen et al. 2003). At higher clock rates, timing skew and cross-talk between adjacent traces created significant signal integrity problems.
- **Shared bandwidth**: All devices on the bus shared the same bandwidth, creating bottlenecks in data-intensive applications (Budruk et al. 2003). This shared resource model meant that a single bandwidth-hungry device could degrade performance for all other components on the same bus.
- **Complex routing**: The parallel architecture required complex routing on motherboards and made high-speed operation difficult beyond short distances (Budruk et al. 2003). The large number of signal traces created challenges for motherboard design and limited practical bus lengths.

- **Limited scalability**: The bus topology placed fundamental limits on clock speeds and the number of supported devices (Shanley and Anderson 1999). Each additional device added electrical load to the bus, constraining maximum achievable frequencies.
- **Voltage issues**: Maintaining consistent voltage levels across multiple devices operating at higher speeds became increasingly difficult (Abbott 2003, pp. 112-115).

These limitations, coupled with the rapidly increasing performance requirements of modern computing systems, necessitated a fundamentally new approach to peripheral connectivity, ultimately leading to the development of PCIe.

Creation of PCIe

The development of PCIe began in the late 1990s under the code name "Arapahoe" as a collaborative effort between several major technology companies, including Intel, Dell, IBM, and HP. In 2001, the technology was transferred to the PCI Special Interest Group (PCI-SIG), the industry organization responsible for specifying the PCI family of standards. The first draft specification was completed in 2002, with the official PCIe 1.0 specification released in 2003 (PCI Special Interest Group 2003). This marked a revolutionary shift in computer architecture, moving from the shared parallel bus paradigm to a serial, point-to-point topology.

The fundamental innovation of PCIe was its adoption of serialized data transmission over differential pairs, which provided several critical advantages (Johnson and Budruk n.d.):

- **Superior signal integrity**: Differential signaling offered much better noise immunity and allowed for higher clock rates.
- **Point-to-point connectivity**: Each device had a dedicated link to either a switch or the root complex, eliminating shared bandwidth bottlenecks.
- **Scalable performance**: The introduction of "lanes" allowed bandwidth to scale linearly with the number of lane pairs allocated to a device.
- **Lower pin count**: Serial transmission drastically reduced the number of physical pins required for connectors.

From its inception, PCIe was designed for backward compatibility at the software level, allowing existing operating systems and drivers to work with PCIe devices with minimal modification (Budruk et al. 2003). This design philosophy ensured rapid industry adoption despite the radical changes in physical implementation.

2.1.2 Generational Evolution of PCIe

Since its introduction, PCIe has undergone several generational advancements, each doubling the bandwidth of its predecessor while maintaining backward compatibility (PCI Special Interest Group 2019). This evolutionary approach has ensured the longevity and widespread adoption of the standard across various computing platforms. Table 2.1 summarizes the key characteristics of each PCIe generation.

Table 2.1: PCIe Generations and Their Specifications

Generation	Year	Data Rate	Encoding	Bandwidth per Lane
PCIe 1.0	2003	2.5 GT/s	8b/10b	250 MB/s
PCIe 2.0	2007	5 GT/s	8b/10b	500 MB/s
PCIe 3.0	2010	8 GT/s	128b/130b	985 MB/s
PCIe 4.0	2017	16 GT/s	128b/130b	1969 MB/s
PCIe 5.0	2019	32 GT/s	128b/130b	3938 MB/s
PCIe 6.0	2022	64 GT/s	PAM4/FLIT	7877 MB/s
PCIe 7.0*	2025*	128 GT/s	PAM4/FLIT	15754 MB/s

* Projected specifications based on PCI-SIG announcements (PCI Special Interest Group 2023)

PCIe 1.0 established the foundation with its 2.5 Gigatransfers per Second (GT/s) data rate and 8b/10b encoding scheme, resulting in 250 MB/s of effective bandwidth per direction per lane (Budruk et al. 2003). While modest by today's standards, this offered a significant improvement over PCI-X for many applications, especially when aggregated across multiple lanes.

PCIe 2.0, introduced in 2007, maintained the same encoding but doubled the transfer rate to 5 GT/s, effectively doubling the bandwidth (PCI Special Interest Group 2007). This generation also introduced improved power management features, reflecting the growing importance of energy efficiency in computing systems (Johnson and Budruk n.d.).

A significant advancement came with PCIe 3.0 in 2010, which not only increased the transfer rate to 8 GT/s but also implemented a more efficient 128b/130b encoding scheme (PCI Special Interest Group 2010). This change reduced the encoding overhead from 20% to approximately 1.5%, resulting in nearly 1 GB/s of bandwidth per lane in each direction. The introduction of this more efficient encoding was a critical innovation that significantly boosted effective throughput.

After a longer development cycle, PCIe 4.0 was released in 2017, continuing the trend of doubling transfer rates to reach 16 GT/s while maintaining the 128b/130b encoding, delivering approximately 2 GB/s per lane (PCI Special Interest Group 2017). This generation was particularly important for high-bandwidth applications such as graphics processing, machine learning acceleration, and high-performance storage.

PCIe 5.0 followed relatively quickly in 2019, with transfer rates reaching 32 GT/s with the same encoding scheme, effectively providing almost 4 GB/s per lane (PCI Special Interest Group 2019). The rapid progression from PCIe 4.0 to 5.0—taking only about two years—reflected the increasing demands of data-intensive applications and the maturation of the development process.

PCIe 6.0, finalized in 2022, represents a more fundamental shift in the standard's approach (PCI Special Interest Group 2022). While maintaining the doubled transfer rate pattern (64 GT/s), it introduced Pulse Amplitude Modulation 4-level (PAM4) signaling and Flow Control Unit (FLIT)-based encoding. PAM4 encodes two bits per symbol instead of one, allowing twice the data rate without increasing the fundamental frequency, which helps address signal integrity challenges at higher speeds. The FLIT encoding scheme further optimizes transmission efficiency and incorporates Forward Error Correction (FEC) to maintain reliability at these higher speeds.

Looking ahead, PCIe 7.0 is currently under development with a projected release around 2025, aiming to continue the trend of doubling bandwidth to 128 GT/s using PAM4 signaling, potentially delivering approximately 15.8 GB/s per lane in each direction (PCI Special Interest Group 2023). These continued advancements demonstrate PCIe's adaptability and its critical role in addressing the ever-increasing bandwidth demands of modern computing systems (Mangla and Pub 2025).

2.1.3 Architectural Foundations

The fundamental architecture of PCIe consists of a layered protocol stack that separates different aspects of the communication process, providing flexibility and extensibility (PCI Special Interest Group 2003, pp. 22-26). This layered approach consists of three primary protocol layers:

- **Transaction Layer**: The uppermost layer responsible for generating and processing Transaction Layer Packet (TLP)s (Budruk et al. 2003). It manages end-to-end communications, credit-based flow control, and quality of service mechanisms.
- **Data Link Layer**: The middle layer ensures reliable data transfer by adding sequence numbers and Cyclic Redundancy Check (CRC) protection to TLPs, forming Data Link Layer Packet (DLLP)s (Wilen et al. 2003). It handles packet acknowledgment, retransmission of failed packets, and link power management.
- **Physical Layer**: The lowest layer deals with the electrical aspects of transmitting and receiving serialized data (Budruk et al. 2003). It manages lane initialization, training, and power management state transitions.

Unlike the shared bus architecture of PCI, PCIe implements a point-to-point topology built around three primary components: endpoints, switches, and root complexes (Solari and Congdon 2005). This topology creates a hierarchical structure that enables more efficient data routing and resource allocation.

The root complex serves as the central connection point between the CPU, memory subsystem, and PCIe fabric, initiating configuration cycles and managing the enumeration process that identifies connected devices during system initialization (Budruk et al. 2003). PCIe switches function as packet routing devices, directing traffic between multiple endpoints and the root complex (Wilen et al. 2003).

The addressing scheme in PCIe uses a three-component system consisting of a bus number, device number, and function number (Bus Device Function (BDF)), similar to PCI but expanded to accommodate the hierarchical topology (Solari and Congdon 2005). This addressing scheme ensures that each function within the PCIe hierarchy has a unique identifier, enabling precise routing of transactions throughout the fabric.

2.2 Zonal Automotive Architecture

3 Concept

3.1 Software Architecture

4 Implementation

4.1 Experimental Setup

4.2 Development of Software

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5.1 Benchmarking

5.2 Reliability and Robustness

6 Conclusion

7 Outlook

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7.2 Long Term Impact

A Appendix

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