XMC1100 AB-Step

Microcontroller Series for Industrial Applications

ARM® Cortex®-M0
32-bit processor core

About this Document

This datasheet is addressed to embedded hardware and software developers. It provides the reader with detailed descriptions about the ordering designations, available features, electrical and physical characteristics of the XMC1100 series devices.

The document describes the characteristics of a superset of the XMC1100 series devices. For simplicity, the various device types are referred to by the collective term XMC1100 throughout this document.

XMC1000 Family User Documentation

The set of user documentation includes:

- **Reference Manual**
    - describes the functionality of the superset of devices.
- **Datasheets**
    - list the complete ordering designations, available features and electrical characteristics of derivative devices.
- **Errata Sheets**
    - list deviations from the specifications given in the related Reference Manual or Datasheets. Errata Sheets are provided for the superset of devices.

Attention: **Please consult all parts of the documentation set to attain consolidated knowledge about your device.**

Application related guidance is provided by **Users Guides** and **Application Notes**.

Please refer to http://www.infineon.com/xmc1000 to get access to the latest versions of those documents.

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1   Summary of Features

The XMC1100 devices are members of the XMC1000 Family of microcontrollers based on the ARM Cortex-M0 processor core. The XMC1100 series devices are designed for general purpose applications.
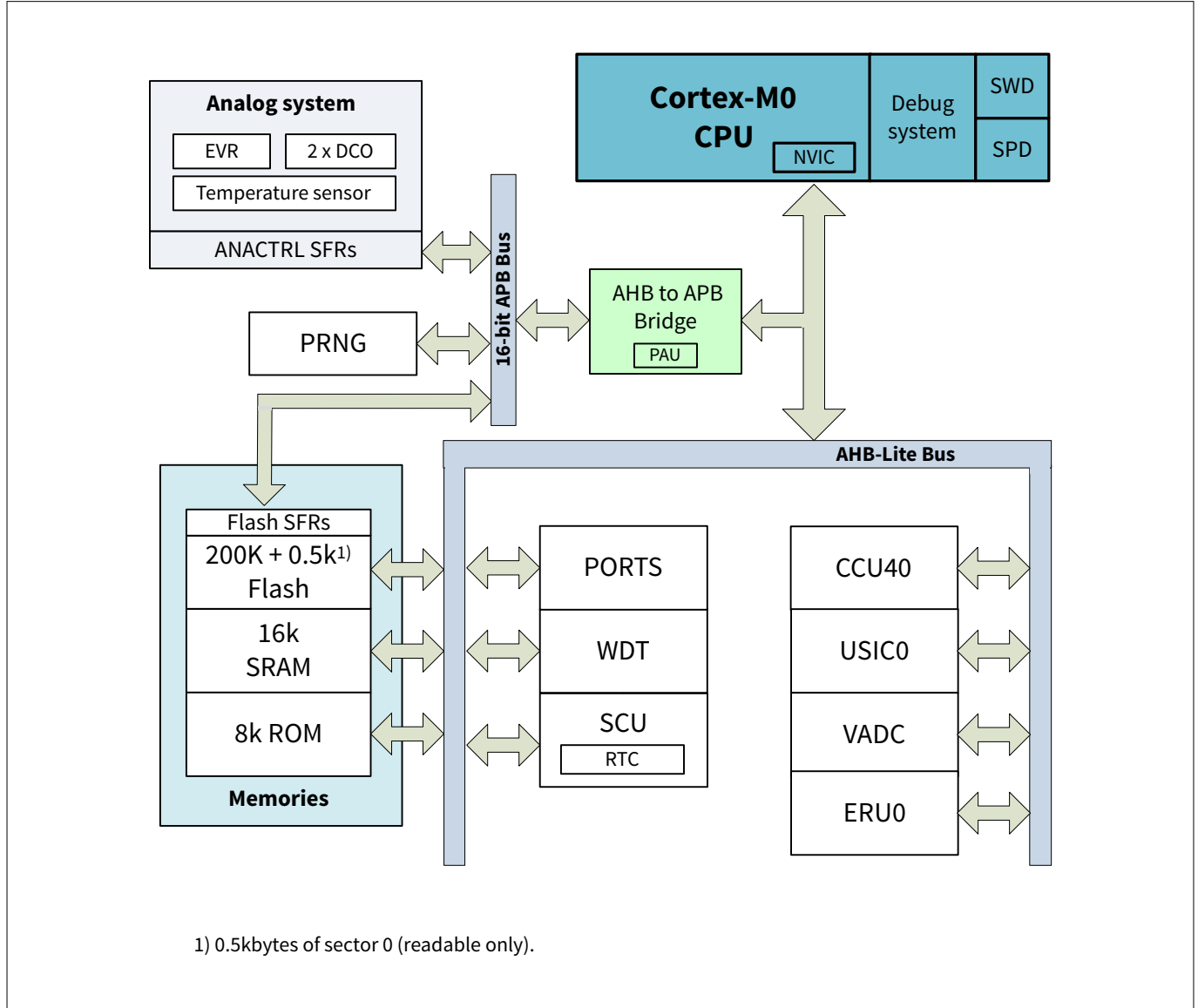
Figure 1   System Block Diagram

CPU Subsystem

- CPU Core
    - High-performance 32-bit ARM Cortex-M0 CPU
    - Most 16-bit Thumb and subset of 32-bit Thumb2 instruction set
    - Single cycle 32-bit hardware multiplier
    - System timer (SysTick) for Operating System support
    - Ultra low power consumption
- Nested Vectored Interrupt Controller (NVIC)
- Event Request Unit (ERU) for processing of external and internal service requests

1 Summary of Features

On-Chip Memories

- 8 kbytes on-chip ROM
- 16 kbytes on-chip high-speed SRAM
- up to 200 KB on-chip Flash program and data memory

On-Chip Peripherals

- Two Universal Serial Interface Channels (USIC), usable as UART, double-SPI, quad-SPI, IIC, IIS and LIN interfaces
- A/D Converters
    - up to 12 analog input pins and channels
    - 12-bit analog to digital converter
- Capture/Compare Units 4 (CCU4) for use as general purpose timers
- Window Watchdog Timer (WDT) for safety sensitive applications
- Real Time Clock module with alarm support (RTC)
- System Control Unit (SCU) for system configuration and control
- Pseudo random number generator (PRNG) for fast random data generation
- Temperature Sensor (TSE)

Input/Output Lines With Individual Bit Controllability

- Tri-stated in input mode
- Push/pull or open drain output mode
- Configurable pad hysteresis

Debug System

- Access through the standard ARM serial wire debug (SWD) or the single pin debug (SPD) interface
- A breakpoint unit (BPU) supporting up to 4 hardware breakpoints
- A watchpoint unit (DWT) supporting up to 2 watchpoints

1.1 Ordering Information

The ordering code for an Infineon microcontroller provides an exact reference to a specific product. The code "XMC1<DDD>-<Z><PPP><T><FFFF>" identifies:

- <DDD> the derivatives function set
- <Z> the package variant
    - T: TSSOP
    - Q: VQFN
- <PPP> package pin count
- <T> the temperature range:
    - F: -40°C to 85°C
    - X: -40°C to 105°C
- <FFFF> the Flash memory size

For ordering codes for the XMC1100 please contact your sales representative or local distributor.

This document describes several derivatives of the XMC1100 series, some descriptions may not apply to a specific product. Please see Table 1.

For simplicity the term **XMC1100** is used for all derivatives throughout this document.

1.2 Device Types

These device types are available and can be ordered through Infineon's direct and/or distribution channels.

Table 1   Synopsis of XMC1100 Device Types

Derivative	Package	Flash Kbytes	SRAM Kbytes
XMC1100-T016F0008	PG-TSSOP-16-8	8	16
XMC1100-T016F0016	PG-TSSOP-16-8	16	16
XMC1100-T016F0032	PG-TSSOP-16-8	32	16
XMC1100-T016F0064	PG-TSSOP-16-8	64	16
XMC1100-T016X0016	PG-TSSOP-16-8	16	16
XMC1100-T016X0032	PG-TSSOP-16-8	32	16
XMC1100-T016X0064	PG-TSSOP-16-8	64	16
XMC1100-T038F0016	PG-TSSOP-38-9	16	16
XMC1100-T038F0032	PG-TSSOP-38-9	32	16
XMC1100-T038F0064	PG-TSSOP-38-9	64	16
XMC1100-T038X0064	PG-TSSOP-38-9	64	16
XMC1100-T038X0128	PG-TSSOP-38-9	128	16
XMC1100-T038X0200	PG-TSSOP-38-9	200	16
XMC1100-Q024F0008	PG-VQFN-24-19	8	16
XMC1100-Q024F0016	PG-VQFN-24-19	16	16
XMC1100-Q024F0032	PG-VQFN-24-19	32	16
XMC1100-Q024F0064	PG-VQFN-24-19	64	16
XMC1100-Q040F0016	PG-VQFN-40-13	16	16
XMC1100-Q040F0032	PG-VQFN-40-13	32	16
XMC1100-Q040F0064	PG-VQFN-40-13	64	16

1.3 Device Type Features

The following table lists the available features per device type.

Table 2   Features of XMC1100 Device Types[1]

Derivative	ADC channel
XMC1100-T016	6
XMC1100-T038	12
XMC1100-Q024	8
XMC1100-Q040	12

1)   Features that are not included in this table are available in all the derivatives.

Table 3 ADC Channels

Package	VADC0 G0	VADC0 G1
PG-TSSOP-16	CH0..CH5	–
PG-TSSOP-38	CH0..CH7	CH1, CH5 .. CH7
PG-VQFN-24	CH0..CH7	–
PG-VQFN-40	CH0..CH7	CH1, CH5 .. CH7

1.4 Chip Identification Number

The Chip Identification Number allows software to identify the marking. It is a 8 words value with the most significant 7 words stored in Flash configuration sector 0 (CS0) at address location: $1000\ 0F00_H$ (MSB) - $1000\ 0F1B_H$ (LSB). The least significant word and most significant word of the Chip Identification Number are the value of registers DBGROMID and IDCHIP, respectively.

Table 4 XMC1100 Chip Identification Number

Derivative	Value	Marking
XMC1100-T016F0008	00011032 01CF00FF 00001F37 00000000 00000C00 00001000 00003000 $201ED083_H$	AB
XMC1100-T016F0016	00011032 01CF00FF 00001F37 00000000 00000C00 00001000 00005000 $201ED083_H$	AB
XMC1100-T016F0032	00011032 01CF00FF 00001F37 00000000 00000C00 00001000 00009000 $201ED083_H$	AB
XMC1100-T016F0064	00011032 01CF00FF 00001F37 00000000 00000C00 00001000 00011000 $201ED083_H$	AB
XMC1100-T016X0016	00011033 01CF00FF 00001F37 00000000 00000C00 00001000 00005000 $201ED083_H$	AB
XMC1100-T016X0032	00011033 01CF00FF 00001F37 00000000 00000C00 00001000 00009000 $201ED083_H$	AB
XMC1100-T016X0064	00011033 01CF00FF 00001F37 00000000 00000C00 00001000 00011000 $201ED083_H$	AB
XMC1100-T038F0016	00011012 01CF00FF 00001F37 00000000 00000C00 00001000 00005000 $201ED083_H$	AB
XMC1100-T038F0032	00011012 01CF00FF 00001F37 00000000 00000C00 00001000 00009000 $201ED083_H$	AB
XMC1100-T038F0064	00011012 01CF00FF 00001F37 00000000 00000C00 00001000 00011000 $201ED083_H$	AB
XMC1100-T038X0064	00011013 01CF00FF 00001F37 00000000 00000C00 00001000 00011000 $201ED083_H$	AB
XMC1100-T038X0128	00011013 01CF00FF 00001F37 00000000 00000C00 00001000 00021000 $201ED083_H$	AB
XMC1100-T038X0200	00011013 01CF00FF 00001F37 00000000 00000C00 00001000 00033000 $201ED083_H$	AB

(table continues…)

Table 4   **(continued) XMC1100 Chip Identification Number**

Derivative	Value	Marking
XMC1100-Q024F0008	00011062 01CF00FF 00001F37 00000000 00000C00 00001000 00003000 201ED083$_H$	AB
XMC1100-Q024F0016	00011062 01CF00FF 00001F37 00000000 00000C00 00001000 00005000 201ED083$_H$	AB
XMC1100-Q024F0032	00011062 01CF00FF 00001F37 00000000 00000C00 00001000 00009000 201ED083$_H$	AB
XMC1100-Q024F0064	00011062 01CF00FF 00001F37 00000000 00000C00 00001000 00011000 201ED083$_H$	AB
XMC1100-Q040F0016	00011042 01CF00FF 00001F37 00000000 00000C00 00001000 00005000 201ED083$_H$	AB
XMC1100-Q040F0032	00011042 01CF00FF 00001F37 00000000 00000C00 00001000 00009000 201ED083$_H$	AB
XMC1100-Q040F0064	00011042 01CF00FF 00001F37 00000000 00000C00 00001000 00011000 201ED083$_H$	AB

2 General Device Information

This section summarizes the logic symbols and package pin configurations with a detailed list of the functional I/O mapping.

2.1 Logic Symbols
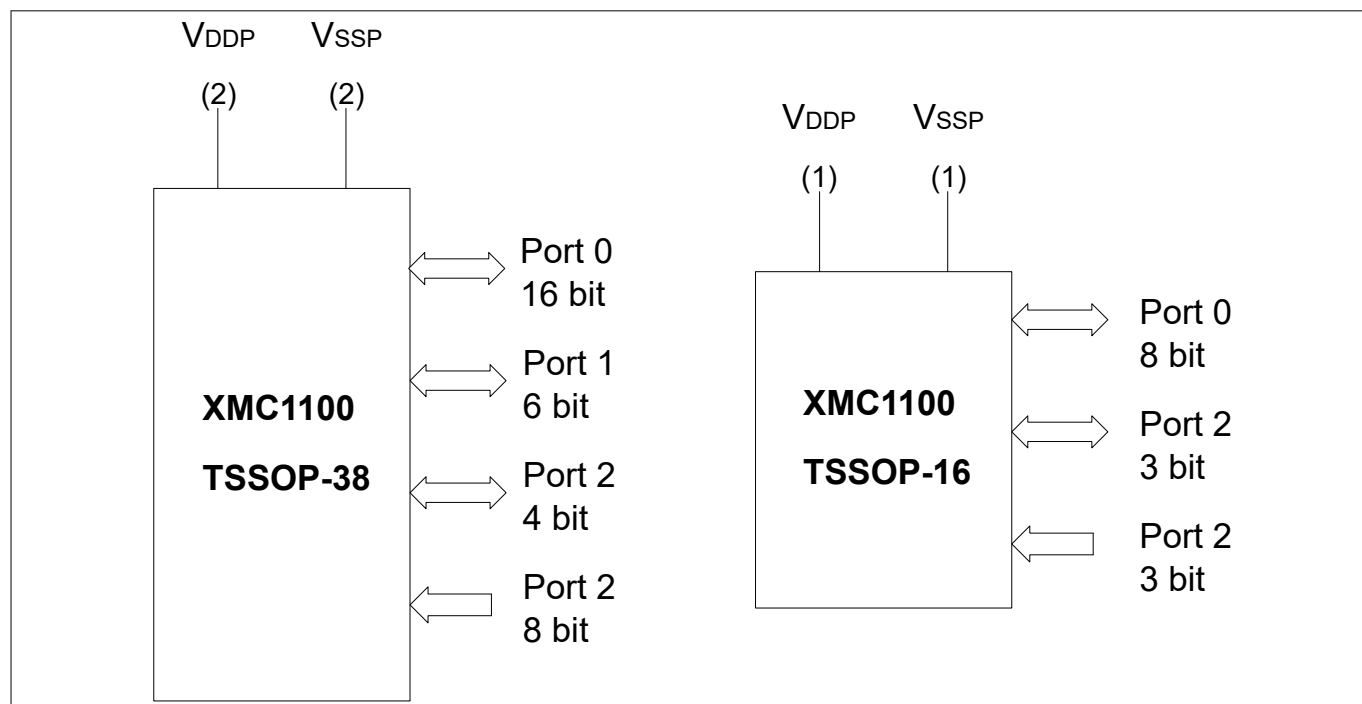
Figure 2   **XMC1100 Logic Symbol for TSSOP-38 and TSSOP-16**
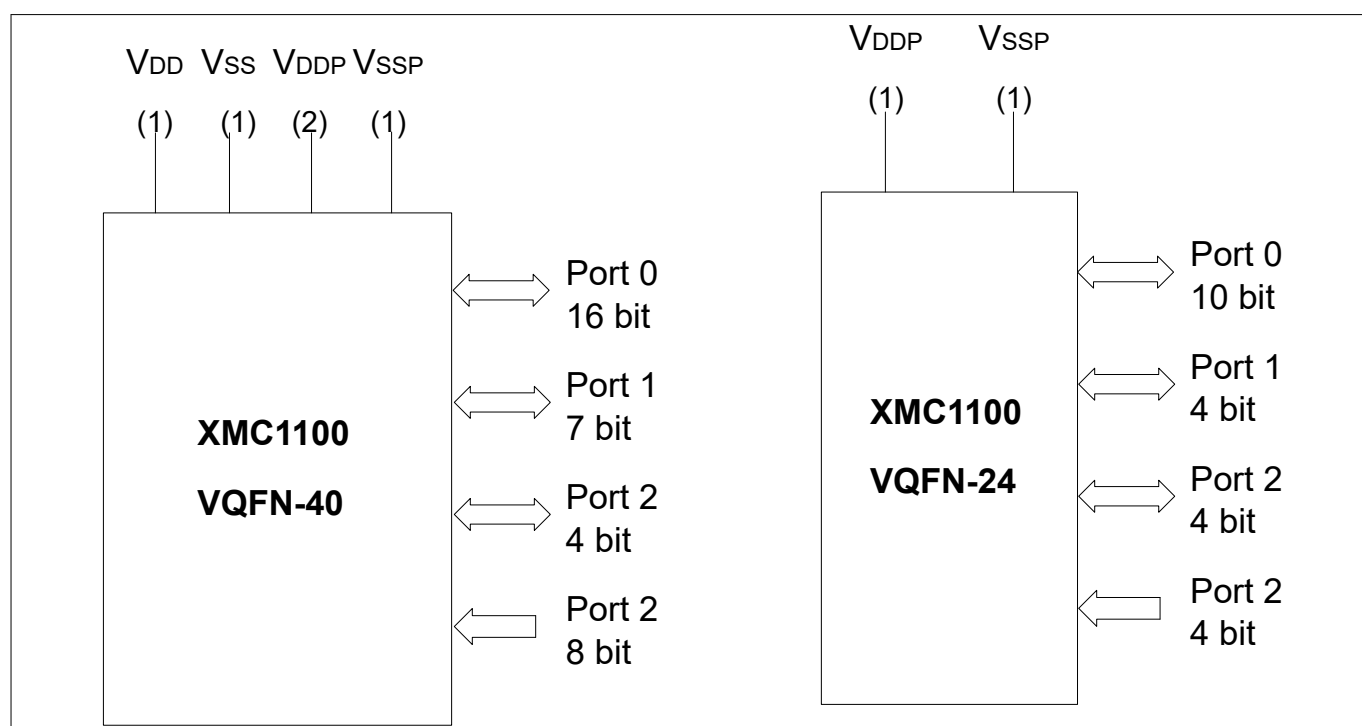
Figure 3   **XMC1100 Logic Symbol for VQFN-24 and VQFN-40**

2.2 Pin Configuration and Definition

The following figures summarize all pins, showing their locations on the different packages.

P2.4	1 ◯ **Top View**	38 P2.3
P2.5	2	37 P2.2
P2.6	3	36 P2.1
P2.7	4	35 P2.0
P2.8	5	34 P0.15
P2.9	6	33 P0.14
P2.10	7	32 P0.13
P2.11	8	31 P0.12
V_{SSP}/V_{SS}	9	30 P0.11
V_{DDP}/V_{DD}	10	29 P0.10
P1.5	11	28 P0.9
P1.4	12	27 P0.8
P1.3	13	26 V_{DDP}
P1.2	14	25 V_{SSP}
P1.1	15	24 P0.7
P1.0	16	23 P0.6
P0.0	17	22 P0.5
P0.1	18	21 P0.4
P0.2	19	20 P0.3
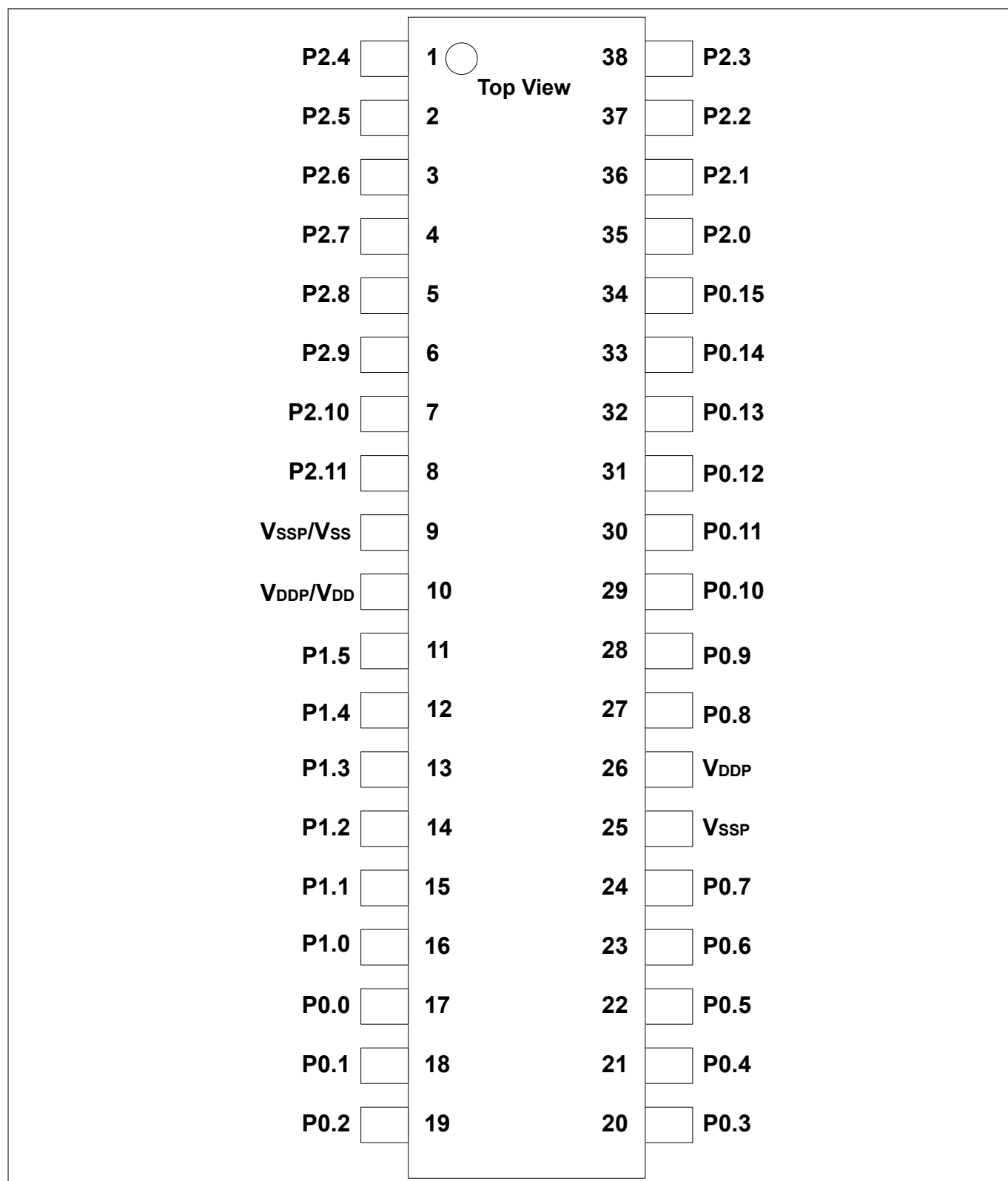
Figure 4 **XMC1100 PG-TSSOP-38 Pin Configuration (top view)**

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P2.7/P2.8	1 ◯	Top View	16	P2.6
P2.9	2		15	P2.0
P2.10	3		14	P0.15
P2.11	4		13	P0.14
V_{SSP}/V_{SS}	5		12	P0.9
V_{DDP}/V_{DD}	6		11	P0.8
P0.0	7		10	P0.7
P0.5	8		9	P0.6
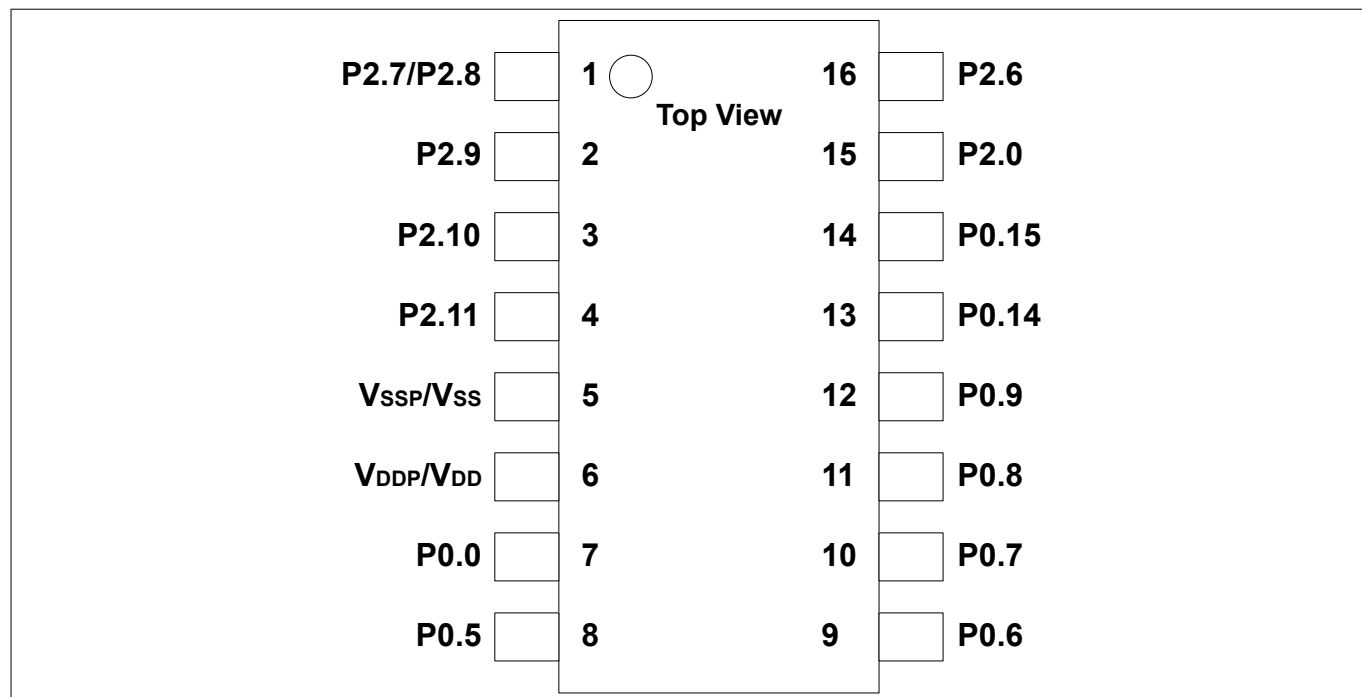
Figure 5   **XMC1100 PG-TSSOP-16 Pin Configuration (top view)**

	P0.7	P0.6	P0.5	P0.0	P1.0	P1.1	
	18	17	16	15	14	13	
P0.8	19					12	P1.2
P0.9	20					11	P1.3
P0.12	21					10	V_{DDP}/V_{DD}
P0.13	22					9	V_{SSP}/V_{SS}
P0.14	23					8	P2.11
P0.15	24 ◯					7	P2.10
	1	2	3	4	5	6	
	P2.0	P2.1	P2.2	P2.6	P2.7/P2.8	P2.9	
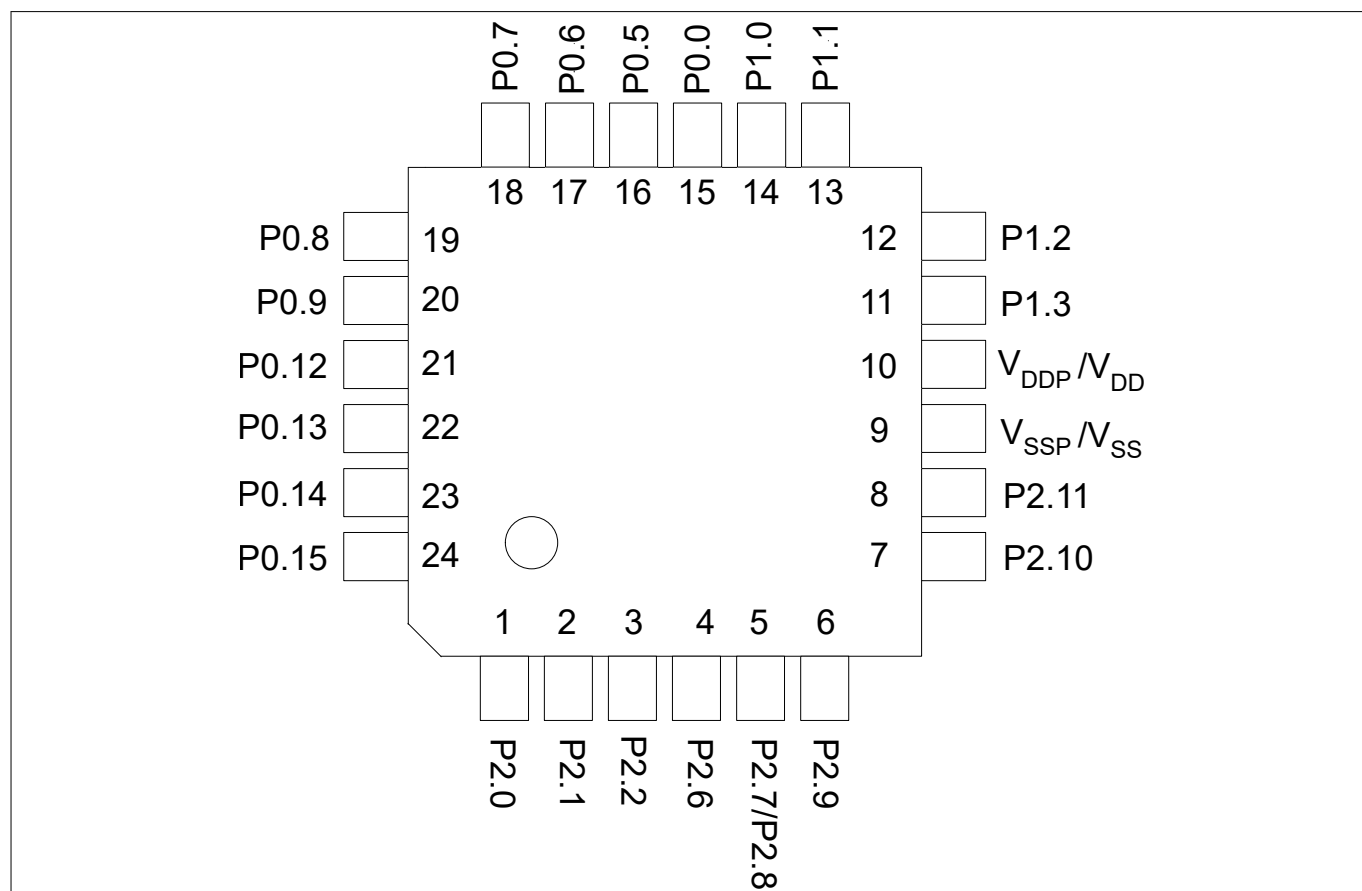
Figure 6   **XMC1100 PG-VQFN-24 Pin Configuration (top view)**

Figure 7   **XMC1100 PG-VQFN-40 Pin Configuration (top view)**

2.2.1   Package Pin Summary

The following general building block is used to describe each pin:

Table 5   **Package Pin Mapping Description**

Function	Package A	Package B	...	Pad Type
Px.y	N	N		Pad Class

The table is sorted by the "Function" column, starting with the regular Port pins (Px.y), followed by the supply pins.

The following columns, titled with the supported package variants, lists the package pin number to which the respective function is mapped in that package.

The "Pad Type" indicates the employed pad type:

- STD_INOUT (standard bi-directional pads)
- STD_INOUT/AN (standard bi-directional pads with analog input)
- High Current (high current bi-directional pads)

2 General Device Information

- STD_IN/AN (standard input pads with analog input)
- Power (power supply)

Details about the pad properties are defined in the Electrical Parameters.

Table 6   **Package Pin Mapping**

Function	VQFN 40	TSSOP 38	VQFN 24	TSSOP 16	Pad Type	Notes
P0.0	23	17	15	7	STD_INOUT	
P0.1	24	18	–	–	STD_INOUT	
P0.2	25	19	–	–	STD_INOUT	
P0.3	26	20	–	–	STD_INOUT	
P0.4	27	21	–	–	STD_INOUT	
P0.5	28	22	16	8	STD_INOUT	
P0.6	29	23	17	9	STD_INOUT	
P0.7	30	24	18	10	STD_INOUT	
P0.8	33	27	19	11	STD_INOUT	
P0.9	34	28	20	12	STD_INOUT	
P0.10	35	29	–	–	STD_INOUT	
P0.11	36	30	–	–	STD_INOUT	
P0.12	37	31	21	–	STD_INOUT	
P0.13	38	32	22	–	STD_INOUT	
P0.14	39	33	23	13	STD_INOUT	
P0.15	40	34	24	14	STD_INOUT	
P1.0	22	16	14	–	High Current	
P1.1	21	15	13	–	High Current	
P1.2	20	14	12	–	High Current	
P1.3	19	13	11	–	High Current	
P1.4	18	12	–	–	High Current	
P1.5	17	11	–	–	High Current	
P1.6	16	–	–	–	STD_INOUT	
P2.0	1	35	1	15	STD_INOUT/AN	
P2.1	2	36	2	–	STD_INOUT/AN	
P2.2	3	37	3	–	STD_IN/AN	
P2.3	4	38	–	–	STD_IN/AN	
P2.4	5	1	–	–	STD_IN/AN	
P2.5	6	2	–	–	STD_IN/AN	
P2.6	7	3	4	16	STD_IN/AN	
P2.7	8	4	5	1	STD_IN/AN	

(table continues...)

Table 6 **(continued) Package Pin Mapping**

| Function	VQFN 40	TSSOP 38	VQFN 24	TSSOP 16	Pad Type	Notes
P2.8	9	5	5	1	STD_IN/AN	
P2.9	10	6	6	2	STD_IN/AN	
P2.10	11	7	7	3	STD_INOUT/AN	
P2.11	12	8	8	4	STD_INOUT/AN	
VSS	13	9	9	5	Power	Supply GND, ADC reference GND
VDD	14	10	10	6	Power	Supply VDD, ADC reference voltage/ORC reference voltage
VDDP	15	10	10	6	Power	When VDD is supplied, VDDP has to be supplied with the same voltage.
VSSP	31	25	–	–	Power	I/O port ground
VDDP	32	26	–	–	Power	I/O port supply
VSSP	Exp. Pad	–	Exp. Pad	–	Power	**Exposed Die Pad** The exposed die pad is connected internally to VSSP. For proper operation, it is mandatory to connect the exposed pad to the board ground. For thermal aspects, please refer to the Package and Reliability chapter.

2.2.2 Port I/O Function Description

The following general building block is used to describe the I/O functions of each PORT pin:

Table 7 **Port I/O Function Description**

Function	Outputs		Inputs	
	ALT1	**ALTn**	**Input**	**Input**
P0.0		MODA.OUT	MODC.INA	
Pn.y	MODA.OUT		MODA.INA	MODC.INB
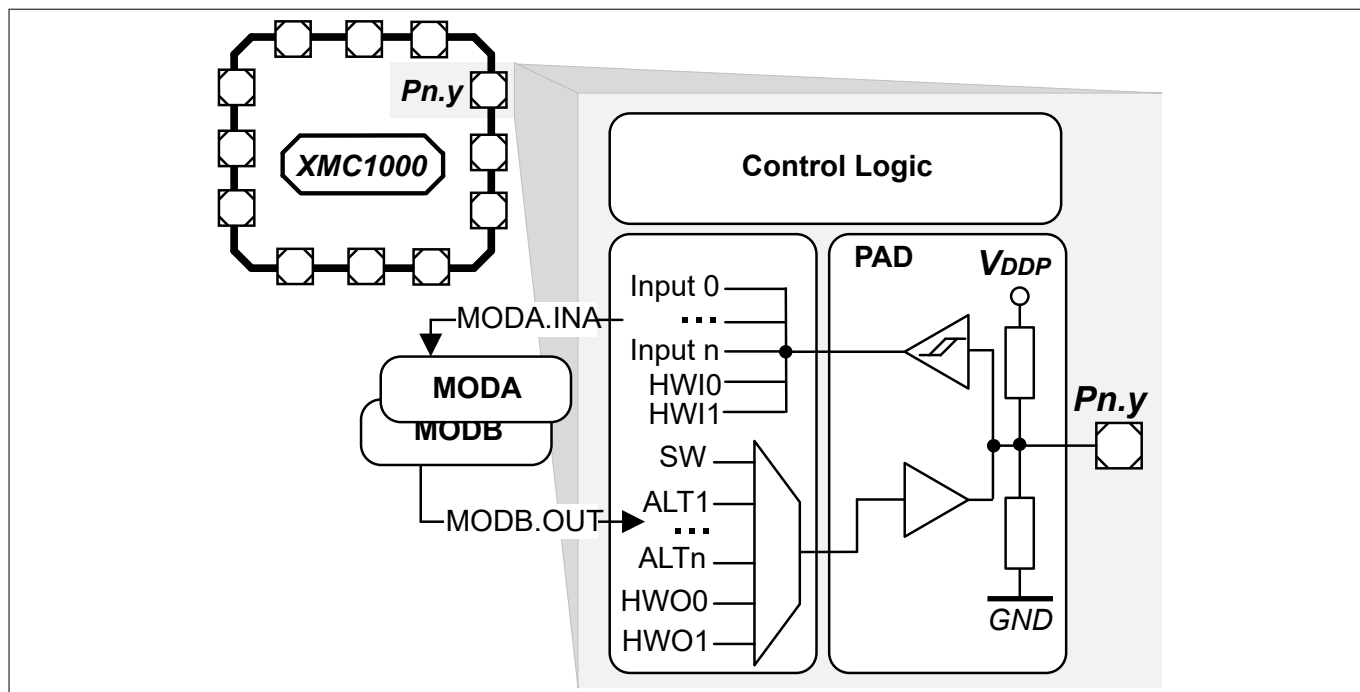
Figure 8   Simplified Port Structure

Pn.y is the port pin name, defining the control and data bits/registers associated with it. As GPIO, the port is under software control. Its input value is read via Pn_IN.y, Pn_OUT defines the output value.

Up to seven alternate output functions (ALT1/2/3/4/5/6/7) can be mapped to a single port pin, selected by Pn_IOCR.PC. The output value is directly driven by the respective module, with the pin characteristics controlled by the port registers (within the limits of the connected pad).

The port pin input can be connected to multiple peripherals. Most peripherals have an input multiplexer to select between different possible input sources.

The input path is also active while the pin is configured as output. This allows to feedback an output to on-chip resources without wasting an additional external pin.

Please refer to Table 9 for the complete Port I/O function mapping.

2.2.3   Hardware Controlled I/O Function Description

The following general building block is used to describe the hardware I/O and pull control functions of each PORT pin:

Table 8   Hardware Controlled I/O Function Description

Function	Outputs	Inputs	Pull Control	
	HWO0	HWI0	HW0_PD	HW0_PU
P0.0	MODB.OUT	MODB.INA		
Pn.y			$\overline{\text{MODC.OUT}}$	MODC.OUT

By Pn_HWSEL, it is possible to select between different hardware "masters" (HWO0/HWI0, HWO1/HWI1). The selected peripheral can take control of the pin(s). Hardware control overrules settings in the respective port pin registers. Additional hardware signals HW0_PD/HW1_PD and HW0_PU/HW1_PU controlled by the peripherals can be used to control the pull devices of the pin.

Please refer to Table 10 for the complete hardware I/O and pull control function mapping.

Table 9   Port I/O Functions

Function	Outputs							Inputs						
	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	Input	Input	Input	Input	Input	Input	Input
P0.0	ERU0.PDOUT0		ERU0.GOUT0	CCU40.OUT0		USIC0_CH0.SELO0	USIC0_CH1.SELO0	CCU40.IN0C				USIC0_CH0.DX2A	USIC0_CH1.DX2A	
P0.1	ERU0.PDOUT1		ERU0.GOUT1	CCU40.OUT1			SCU.VDROP	CCU40.IN1C						
P0.2	ERU0.PDOUT2		ERU0.GOUT2	CCU40.OUT2		VADC0.EMUX02		CCU40.IN2C						
P0.3	ERU0.PDOUT3		ERU0.GOUT3	CCU40.OUT3		VADC0.EMUX01		CCU40.IN3C						
P0.4				CCU40.OUT1		VADC0.EMUX00	WWDT.SERVICE_OUT							
P0.5				CCU40.OUT0										
P0.6				CCU40.OUT0		USIC0_CH1.MCLKOUT	USIC0_CH1.DOUT0	CCU40.IN0B				USIC0_CH1.DX0C		
P0.7				CCU40.OUT1		USIC0_CH0.SCLKOUT	USIC0_CH1.DOUT0	CCU40.IN1B				USIC0_CH0.DX1C	USIC0_CH1.DX0D	USIC0_CH1.DX1C
P0.8				CCU40.OUT2		USIC0_CH0.SCLKOUT	USIC0_CH1.SCLKOUT	CCU40.IN2B				USIC0_CH0.DX1B	USIC0_CH1.DX1B	

(table continues...)

Table 9 (continued) Port I/O Functions

Function	Outputs							Inputs						
	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	Input	Input	Input	Input	Input	Input	Input
P0.9				CCU40.OUT3		USIC0_CH0.SELO0	USIC0_CH1.SELO0	CCU40.IN3B				USIC0_CH0.DX2B	USIC0_CH1.DX2B	
P0.10						USIC0_CH0.SELO1	USIC0_CH1.SELO1					USIC0_CH0.DX2C	USIC0_CH1.DX2C	
P0.11				USIC0_CH0.MCLKOUT		USIC0_CH0.SELO2	USIC0_CH1.SELO2					USIC0_CH0.DX2D	USIC0_CH1.DX2D	
P0.12						USIC0_CH0.SELO3		CCU40.IN0A	CCU40.IN1A	CCU40.IN2A	CCU40.IN3A	USIC0_CH0.DX2E		
P0.13	WWDT.SERVICE_OUT					USIC0_CH0.SELO4						USIC0_CH0.DX2F		
P0.14						USIC0_CH0.DOUT0	USIC0_CH0.SCLKOUT					USIC0_CH0.DX0A	USIC0_CH0.DX1A	
P0.15						USIC0_CH0.DOUT0	USIC0_CH1.MCLKOUT					USIC0_CH0.DX0B		
P1.0		CCU40.OUT0					USIC0_CH0.DOUT0					USIC0_CH0.DX0C		
P1.1	VADC0.EMUX00	CCU40.OUT1				USIC0_CH1.DOUT0	USIC0_CH1.SELO0					USIC0_CH0.DX0D	USIC0_CH1.DX1D	USIC0_CH1.DX2E

(table continues...)

Table 9   (continued) Port I/O Functions

Function	Outputs							Inputs						
	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	Input	Input	Input	Input	Input	Input	Input
P1.2	VADC0.EMUX01	CCU40.OUT2					USIC0_CH1.DOUT0					USIC0_CH1.DX0B		
P1.3	VADC0.EMUX02	CCU40.OUT3				USIC0_CH1.SCLKOUT	USIC0_CH1.DOUT0					USIC0_CH1.DX0A	USIC0_CH1.DX1A	
P1.4	VADC0.EMUX10	USIC0_CH1.SCLKOUT				USIC0_CH0.SELO0	USIC0_CH1.SELO1					USIC0_CH0.DX5E	USIC0_CH1.DX5E	
P1.5	VADC0.EMUX11	USIC0_CH0.DOUT0				USIC0_CH0.SELO1	USIC0_CH1.SELO2					USIC0_CH1.DX5F		
P1.6	VADC0.EMUX12	USIC0_CH1.DOUT0		USIC0_CH0.SCLKOUT		USIC0_CH0.SELO2	USIC0_CH1.SELO3			USIC0_CH0.DX5F				
P2.0	ERU0.PDOUT3	CCU40.OUT0	ERU0.GOUT3			USIC0_CH0.DOUT0	USIC0_CH0.SCLKOUT		VADC0.G0CH5		ERU0.0B0	USIC0_CH0.DX0E	USIC0_CH0.DX1E	USIC0_CH1.DX2F
P2.1	ERU0.PDOUT2	CCU40.OUT1	ERU0.GOUT2			USIC0_CH0.DOUT0	USIC0_CH1.SCLKOUT		VADC0.G0CH6		ERU0.1B0	USIC0_CH0.DX0F	USIC0_CH1.DX3A	USIC0_CH1.DX4A
P2.2									VADC0.G0CH7		ERU0.0B1	USIC0_CH0.DX3A	USIC0_CH0.DX4A	USIC0_CH1.DX5A

(table continues...)

Table 9   (continued) Port I/O Functions

Function	Outputs							Inputs						
	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	Input	Input	Input	Input	Input	Input	Input
P2.3									VADC0.G1CH5		ERU0.1 B1	USIC0_CH0.DX5B	USIC0_CH1.DX3C	USIC0_CH1.DX4C
P2.4									VADC0.G1CH6		ERU0.0 A1	USIC0_CH0.DX3B	USIC0_CH0.DX4B	USIC0_CH1.DX5B
P2.5									VADC0.G1CH7		ERU0.1 A1	USIC0_CH0.DX5D	USIC0_CH1.DX3E	USIC0_CH1.DX4E
P2.6									VADC0.G0CH0		ERU0.2 A1	USIC0_CH0.DX3E	USIC0_CH0.DX4E	USIC0_CH1.DX5D
P2.7									VADC0.G1CH1		ERU0.3 A1	USIC0_CH0.DX5C	USIC0_CH1.DX3D	USIC0_CH1.DX4D
P2.8									VADC0.G0CH1		ERU0.3 B1	USIC0_CH0.DX3D	USIC0_CH0.DX4D	USIC0_CH1.DX5C
P2.9									VADC0.G0CH2		ERU0.3 B0	USIC0_CH0.DX5A	USIC0_CH1.DX3B	USIC0_CH1.DX4B
P2.10	ERU0.PDOUT1	CCU40.OUT2	ERU0.GOUT1				USIC0_CH1.DOUT0		VADC0.G0CH3		ERU0.2 B0	USIC0_CH0.DX3C	USIC0_CH0.DX4C	USIC0_CH1.DX0F
P2.11	ERU0.PDOUT0	CCU40.OUT3	ERU0.GOUT0			USIC0_CH1.SCLKOUT	USIC0_CH1.DOUT0		VADC0.G0CH4		ERU0.2 B1	USIC0_CH1.DX0E	USIC0_CH1.DX1E	

Table 10   Hardware Controlled I/O Functions

Function	Outputs		Inputs		Pull Control			
	HWO0	HWO1	HWI0	HWI1	HW0_PD	HW0_PU	HW1_PD	HW1_PU
P0.0								
P0.1								
P0.2								
P0.3								
P0.4								
P0.5								
P0.6								
P0.7								
P0.8								
P0.9								
P0.10								
P0.11								
P0.12								
P0.13								
P0.14								
P0.15								
P1.0		USIC0_CH0 .DOUT0		USIC0_CH0 .HWIN0				
P1.1		USIC0_CH0 .DOUT1		USIC0_CH0 .HWIN1				
P1.2		USIC0_CH0 .DOUT2		USIC0_CH0 .HWIN2				

(table continues...)

Table 10   **(continued) Hardware Controlled I/O Functions**

Function	Outputs		Inputs		Pull Control			
	HWO0	HWO1	HWI0	HWI1	HW0_PD	HW0_PU	HW1_PD	HW1_PU
P1.3		USIC0_CH0.DOUT3		USIC0_CH0.HWIN3				
P1.4								
P1.5								
P1.6								
P2.0								
P2.1								
P2.2							$\overline{\text{CCU40.OUT3}}$	CCU40.OUT3
P2.3								
P2.4								
P2.5								
P2.6							$\overline{\text{CCU40.OUT3}}$	CCU40.OUT3
P2.7							$\overline{\text{CCU40.OUT3}}$	CCU40.OUT3
P2.8							$\overline{\text{CCU40.OUT2}}$	CCU40.OUT2
P2.9							$\overline{\text{CCU40.OUT2}}$	CCU40.OUT2
P2.10								
P2.11								

3 Electrical Parameters

This section provides the electrical parameters which are implementation-specific for the XMC1100.

3.1 General Parameters

3.1.1 Parameter Interpretation

The parameters listed in this section represent partly the characteristics of the XMC1100 and partly its requirements on the system. To aid interpreting the parameters easily when evaluating them for a design, they are indicated by the abbreviations in the "Symbol" column:

- **CC**

  Such parameters indicate **C**ontroller **C**haracteristics, which are distinctive feature of the XMC1100 and must be regarded for a system design.

- **SR**

  Such parameters indicate **S**ystem **R**equirements, which must be provided by the application system in which the XMC1100 is designed in.

3.1.2 Absolute Maximum Ratings

Stresses above the values listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 11   Absolute Maximum Rating Parameters

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Junction temperature	T_J SR	-40	–	115	°C	–
Storage temperature	T_{ST} SR	-40	–	125	°C	–
Voltage on power supply pin with respect to V_{SSP}	V_{DDP} SR	-0.3	–	6	V	–
Voltage on digital pins with respect to V_{SSP}[1]	V_{IN} SR	-0.5	–	V_{DDP} + 0.5 or max. 6	V	whichever is lower
Voltage on P2 pins with respect to V_{SSP}[2]	V_{INP2} SR	-0.3	–	V_{DDP} + 0.3	V	–
Voltage on analog input pins with respect to V_{SSP}	V_{AIN} V_{AREF} SR	-0.5	–	V_{DDP} + 0.5 or max. 6	V	whichever is lower
Input current on any pin during overload condition	I_{IN} SR	-10	–	10	mA	–
Absolute maximum sum of all input currents during overload condition	ΣI_{IN} SR	-50	–	+50	mA	–

1)   Excluding port pins P2.[1,2,6,7,8,9,11].
2)   Applicable to port pins P2.[1,2,6,7,8,9,11].

3.1.3 Pin Reliability in Overload

When receiving signals from higher voltage devices, low-voltage devices experience overload currents and voltages that go beyond their own IO power supplies specification.

Table 12 defines overload conditions that will not cause any negative reliability impact if all the following conditions are met:

- full operation life-time is not exceeded
- Operating Conditions are met for
  - pad supply levels (V_{DDP})
  - temperature

If a pin current is outside of the Operating Conditions but within the overload conditions, then the parameters of this pin as stated in the Operating Conditions can no longer be guaranteed. Operation is still possible in most cases but with relaxed parameters.

Note: *An overload condition on one or more pins does not require a reset.*

Note: *A series resistor at the pin to limit the current to the maximum permitted overload current is sufficient to handle failure situations like short to battery.*

Table 12   Overload Parameters

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Input current on any port pin during overload condition	I_{OV} SR	-5	–	5	mA	
Absolute sum of all input circuit currents during overload condition	I_{OVS} SR	–	–	25	mA	

Figure 9 shows the path of the input currents during overload via the ESD protection structures. The diodes against V_{DDP} and ground are a simplified representation of these ESD protection structures.
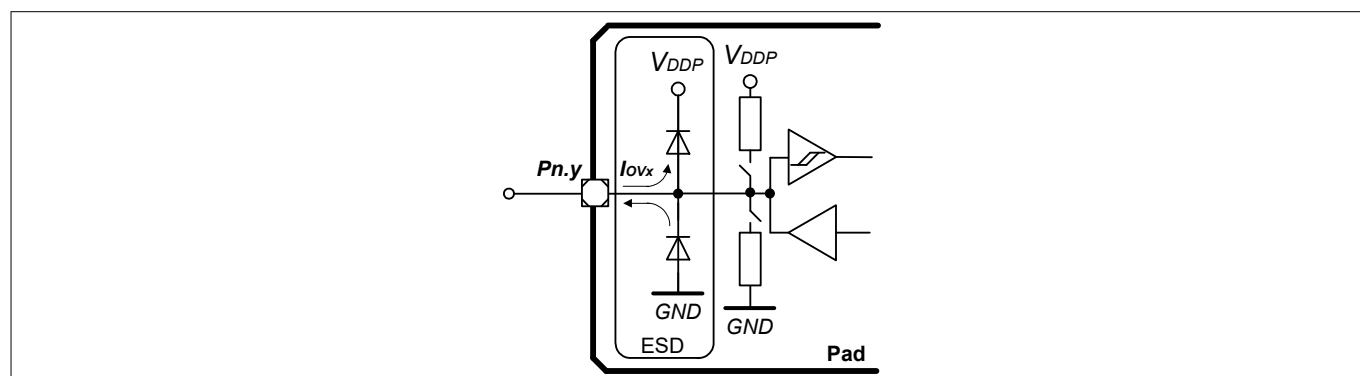
Figure 9   Input Overload Current via ESD structures

Table 13 and Table 14 list input voltages that can be reached under overload conditions. Note that the absolute maximum input voltages as defined in the Absolute Maximum Ratings must not be exceeded during overload.

Table 13   PN-Junction Characteristics for positive Overload

Pad Type	I_{OV} = 5 mA
Standard, High-current, AN/DIG_IN	$V_{IN} = V_{DDP}$ + 0.5 V $V_{AIN} = V_{DDP}$ + 0.5 V $V_{AREF} = V_{DDP}$ + 0.5 V
P2.[1,2,6:9,11]	$V_{INP2} = V_{DDP}$ + 0.3 V

Table 14   PN-Junction Characteristics for negative Overload

Pad Type	I_{OV} = 5 mA
Standard, High-current, AN/DIG_IN	$V_{IN} = V_{SS}$ - 0.5 V $V_{AIN} = V_{SS}$ - 0.5 V $V_{AREF} = V_{SS}$ - 0.5 V
P2.[1,2,6:9,11]	$V_{INP2} = V_{SS}$ - 0.3 V

3.1.4   Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation and reliability of the XMC1100. All parameters specified in the following tables refer to these operating conditions, unless noted otherwise.

Table 15   Operating Conditions Parameters

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Ambient Temperature	T_A SR	-40	–	85	°C	Temp. Range F
		-40	–	105	°C	Temp. Range X
Digital supply voltage[1]	V_{DDP} SR	1.8	–	5.5	V	
MCLK Frequency	f_{MCLK} CC	–	–	33.2	MHz	CPU clock
PCLK Frequency	f_{PCLK} CC	–	–	66.4	MHz	Peripherals clock
Short circuit current of digital outputs	I_{SC} SR	-5	–	5	mA	
Absolute sum of short circuit currents of the device	ΣI_{SC_D} SR	–	–	25	mA	

1)   See also the Supply Monitoring thresholds, Chapter 3.3.2.

3.2 DC Parameters

3.2.1 Input/Output Characteristics

Table 16 provides the characteristics of the input/output pins of the XMC1100.

Note: *These parameters are not subject to production test, but verified by design and/or characterization.*

Note: *Unless otherwise stated, input DC and AC characteristics, including peripheral timings, assume that the input pads operate with the standard hysteresis.*

Table 16 **Input/Output Characteristics (Operating Conditions apply)**

Parameter	Symbol	Limit Values		Unit	Note/Test Condition
		Min.	**Max.**		
Output low voltage on port pins (with standard pads)	V_{OLP} CC	–	1.0	V	I_{OL} = 11 mA (5 V) I_{OL} = 7 mA (3.3 V)
		–	0.4	V	I_{OL} = 5 mA (5 V) I_{OL} = 3.5 mA (3.3 V)
Output low voltage on high current pads	V_{OLP1} CC	–	1.0	V	I_{OL} = 50 mA (5 V) I_{OL} = 25 mA (3.3 V)
		–	0.32	V	I_{OL} = 10 mA (5 V)
		–	0.4	V	I_{OL} = 5 mA (3.3 V)
Output high voltage on port pins (with standard pads)	V_{OHP} CC	V_{DDP} - 1.0	–	V	I_{OH} = -10 mA (5 V) I_{OH} = -7 mA (3.3 V)
		V_{DDP} - 0.4	–	V	I_{OH} = -4.5 mA (5 V) I_{OH} = -2.5 mA (3.3 V)
Output high voltage on high current pads	V_{OHP1} CC	V_{DDP} - 0.32	–	V	I_{OH} = -6 mA (5 V)
		V_{DDP} - 1.0	–	V	I_{OH} = -8 mA (3.3 V)
		V_{DDP} - 0.4	–	V	I_{OH} = -4 mA (3.3 V)
Input low voltage on port pins (Standard Hysteresis)	V_{ILPS} SR	–	0.19 × V_{DDP}	V	CMOS Mode (5 V, 3.3 V & 2.2 V)
Input high voltage on port pins (Standard Hysteresis)	V_{IHPS} SR	0.7 × V_{DDP}	–	V	CMOS Mode (5 V, 3.3 V & 2.2 V)
Input low voltage on port pins (Large Hysteresis)	V_{ILPL} SR	–	0.08 × V_{DDP}	V	CMOS Mode (5 V, 3.3 V & 2.2 V)[10]
Input high voltage on port pins (Large Hysteresis)	V_{IHPL} SR	0.85 × V_{DDP}	–	V	CMOS Mode (5 V, 3.3 V & 2.2 V)[10]

(table continues...)

Table 16   **(continued) Input/Output Characteristics (Operating Conditions apply)**

Parameter	Symbol	Limit Values		Unit	Note/Test Condition
		Min.	Max.		
Rise time on High Current Pad[1]	t_{HCPR} CC	–	9	ns	50 pF @ 5 V[2]
		–	12	ns	50 pF @ 3.3 V[3]
		–	25	ns	50 pF @ 1.8 V[4]
Fall time on High Current Pad[1]	t_{HCPF} CC	–	9	ns	50 pF @ 5 V[2]
		–	12	ns	50 pF @ 3.3 V[3]
		–	25	ns	50 pF @ 1.8 V[4]
Rise time on Standard Pad[1]	t_R CC	–	12	ns	50 pF @ 5 V[5]
		–	15	ns	50 pF @ 3.3 V[6]
		–	31	ns	50 pF @ 1.8 V[7]
Fall time on Standard Pad[1]	t_F CC	–	12	ns	50 pF @ 5 V[5]
		–	15	ns	50 pF @ 3.3 V[6]
		–	31	ns	50 pF @ 1.8 V[7]
Input Hysteresis[8]	HYS CC	$0.08 \times V_{DDP}$	–	V	CMOS Mode (5 V), Standard Hysteresis
		$0.03 \times V_{DDP}$	–	V	CMOS Mode (3.3 V), Standard Hysteresis
		$0.02 \times V_{DDP}$	–	V	CMOS Mode (2.2 V), Standard Hysteresis
		$0.5 \times V_{DDP}$	$0.75 \times V_{DDP}$	V	CMOS Mode(5 V), Large Hysteresis
		$0.4 \times V_{DDP}$	$0.75 \times V_{DDP}$	V	CMOS Mode(3.3 V), Large Hysteresis
		$0.2 \times V_{DDP}$	$0.65 \times V_{DDP}$	V	CMOS Mode(2.2 V), Large Hysteresis
Pin capacitance (digital inputs/outputs)	C_{IO} CC	–	10	pF	
Pull-up resistor on port pins	R_{PUP} CC	20	50	kohm	$V_{IN} = V_{SSP}$
Pull-down resistor on port pins	R_{PDP} CC	20	50	kohm	$V_{IN} = V_{DDP}$
Input leakage current[9]	I_{OZP} CC	-1	1	µA	$0 < V_{IN} < V_{DDP}$, $T_A \leq 105°C$
Voltage on any pin during V_{DDP} power off	V_{PO} SR	–	0.3	V	[10]
Maximum current per pin (excluding P1, V_{DDP} and V_{SS})	I_{MP} SR	-10	11	mA	–

(table continues...)

Table 16 (continued) Input/Output Characteristics (Operating Conditions apply)

Parameter	Symbol	Limit Values		Unit	Note/Test Condition
		Min.	Max.		
Maximum current per high current pins	I_{MP1A} SR	-10	50	mA	–
Maximum current into V_{DDP} (TSSOP28/16, VQFN24)	I_{MVDD1} SR	–	130	mA	[10]
Maximum current into V_{DDP} (TSSOP38, VQFN40)	I_{MVDD2} SR	–	260	mA	[10]
Maximum current out of V_{SS} (TSSOP28/16, VQFN24)	I_{MVSS1} SR	–	130	mA	[10]
Maximum current out of V_{SS} (TSSOP38, VQFN40)	I_{MVSS2} SR	–	260	mA	[10]

1) Rise/Fall time parameters are taken with 10% - 90% of supply.
2) Additional rise/fall time valid for C_L = 50 pF - C_L = 100 pF @ 0.150 ns/pF at 5 V supply voltage.
3) Additional rise/fall time valid for C_L = 50 pF - C_L = 100 pF @ 0.205 ns/pF at 3.3 V supply voltage.
4) Additional rise/fall time valid for C_L = 50 pF - C_L = 100 pF @ 0.445 ns/pF at 1.8 V supply voltage.
5) Additional rise/fall time valid for C_L = 50 pF - C_L = 100 pF @ 0.225 ns/pF at 5 V supply voltage.
6) Additional rise/fall time valid for C_L = 50 pF - C_L = 100 pF @ 0.288 ns/pF at 3.3 V supply voltage.
7) Additional rise/fall time valid for C_L = 50 pF - C_L = 100 pF @ 0.588 ns/pF at 1.8 V supply voltage.
8) Hysteresis is implemented to avoid meta stable states and switching due to internal ground bounce. It cannot be guaranteed that it suppresses switching due to external system noise.
9) An additional error current (I_{INJ}) will flow if an overload current flows through an adjacent pin.
10) However, for applications with strict low power-down current requirements, it is mandatory that no active voltage source is supplied at any GPIO pin when V_{DDP} is powered off.

3.2.2 Analog to Digital Converters (ADC)

Table 17 shows the Analog to Digital Converter (ADC) characteristics.

Note: *These parameters are not subject to production test, but verified by design and/or characterization.*

Table 17 ADC Characteristics (Operating Conditions apply)[1]

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Supply voltage range (internal reference)	V_{DD_int} SR	2.0	–	3.0	V	SHSCFG.AREF = 11_B CALCTR.CALGNSTC = $0C_H$
		3.0	–	5.5	V	SHSCFG.AREF = 10_B
Supply voltage range (external reference)	V_{DD_ext} SR	3.0	–	5.5	V	SHSCFG.AREF = 00_B
Analog input voltage range	V_{AIN} SR	V_{SSP} - 0.05	–	V_{DDP} + 0.05	V	
Auxiliary analog reference ground	V_{REFGND} SR	V_{SSP} - 0.05	–	1.0	V	G0CH0

(table continues...)

Table 17 **(continued) ADC Characteristics (Operating Conditions apply)**[1]

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	**Typ.**	**Max.**		
Internal reference voltage (full scale value)	V_{REFINT} CC	5			V	
Switched capacitance of an analog input	C_{AINS} CC	–	1.2	2	pF	GNCTRxz.GAINy = 00_B (unity gain)
		–	1.2	2	pF	GNCTRxz.GAINy = 01_B (gain g1)
		–	4.5	6	pF	GNCTRxz.GAINy = 10_B (gain g2)
		–	4.5	6	pF	GNCTRxz.GAINy = 11_B (gain g3)
Total capacitance of an analog input	C_{AINT} CC	–	–	10	pF	
Total capacitance of the reference input	C_{AREFT} CC	–	–	10	pF	
Gain settings	G_{IN} CC	1			–	GNCTRxz.GAINy = 00_B (unity gain)
		3			–	GNCTRxz.GAINy = 01_B (gain g1)
		6			–	GNCTRxz.GAINy = 10_B (gain g2)
		12			–	GNCTRxz.GAINy = 11_B (gain g3)
Sample Time	t_{sample} CC	4	–	–	$1/f_{ADC}$	V_{DD} = 5.0 V
		4	–	–	$1/f_{ADC}$	V_{DD} = 3.3 V
		30	–	–	$1/f_{ADC}$	V_{DD} = 2.0 V
Sigma delta loop hold time	t_{SD_hold} CC	20	–	–	µs	Residual charge stored in an active sigma delta loop remains available
Conversion time in fast compare mode	t_{CF} CC	9			$1/f_{ADC}$	[2]
Conversion time in 12-bit mode	t_{C12} CC	20			$1/f_{ADC}$	[2]
Maximum sample rate in 12-bit mode[3]	f_{C12} CC	–	–	$f_{ADC}/43.5$	–	1 sample pending
		–	–	$f_{ADC}/63.5$	–	2 samples pending
Conversion time in 10-bit mode	t_{C10} CC	18			$1/f_{ADC}$	[2]

(table continues...)

Table 17 **(continued) ADC Characteristics (Operating Conditions apply)[1]**

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	**Typ.**	**Max.**		
Maximum sample rate in 10-bit mode[3]	f_{C10} CC	–	–	$f_{ADC}/$41.5	–	1 sample pending
		–	–	$f_{ADC}/$59.5	–	2 samples pending
Conversion time in 8-bit mode	t_{C8} CC	16			$1/f_{ADC}$	[2]
Maximum sample rate in 8-bit mode[3]	f_{C8} CC	–	–	$f_{ADC}/$38.5	–	1 sample pending
		–	–	$f_{ADC}/$54.5	–	2 samples pending
RMS noise[4]	EN_{RMS} CC	–	1.5	–	LSB12	DC input, V_{DD} = 5.0 V, V_{AIN} = 2.5 V, 25°C
DNL error	EA_{DNL} CC	–	±2.0	–	LSB12	
INL error	EA_{INL} CC	–	±4.0	–	LSB12	
Gain error with external reference	EA_{GAIN} CC	–	±0.5	–	%	SHSCFG.AREF = 00$_B$ (calibrated)
Gain error with internal reference[5]	EA_{GAIN} CC	–	±3.6	–	%	SHSCFG.AREF = 1X$_B$ (calibrated), -40°C - 105°C
		–	±2.0	–	%	SHSCFG.AREF = 1X$_B$ (calibrated), 0°C - 85°C
Offset error	EA_{OFF} CC	–	±8.0	–	mV	Calibrated, V_{DD} = 5.0 V

1) The parameters are defined for ADC clock frequency f_{SH} = 32 MHz.
2) No pending samples assumed, excluding sampling time and calibration.
3) Includes synchronization and calibration (average of gain and offset calibration).
4) This parameter can also be defined as an SNR value: SNR[dB] = 20 × log(A_{MAXeff}/N_{RMS}).

   With A_{MAXeff} = 2N/2, SNR[dB] = 20 × log (2048/N_{RMS}) [N = 12].

   N_{RMS} = 1.5 LSB12, therefore, equals SNR = 20 × log (2048/1.5) = 62.7 dB.
5) Includes error from the reference voltage.
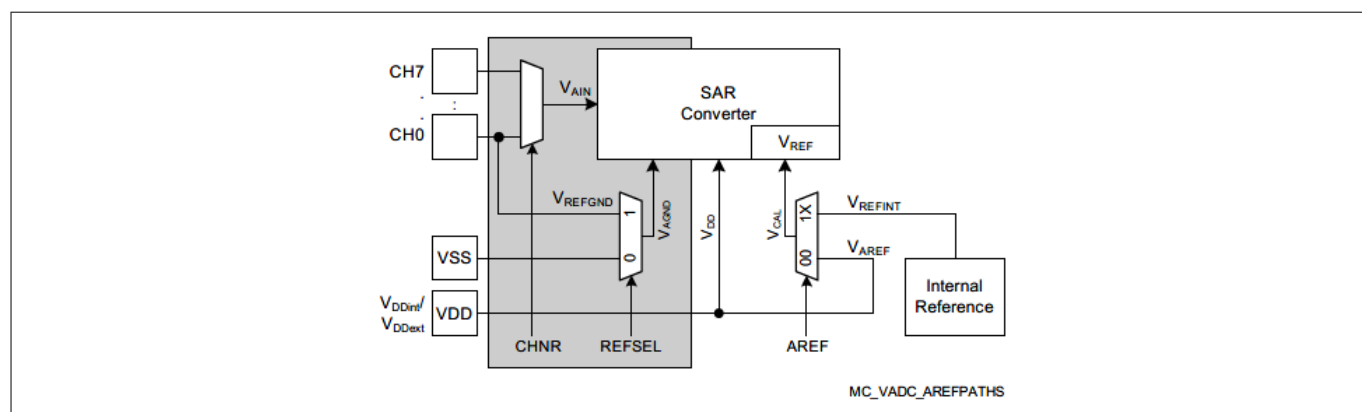
Figure 10 ADC Voltage Supply

3.2.3 Temperature Sensor Characteristics

Note: *These parameters are not subject to production test, but verified by design and/or characterization.*

Table 18 **Temperature Sensor Characteristics**

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Measurement time	t_M CC	–	–	10	ms	
Temperature sensor range	T_{SR} SR	-40	–	115	°C	
Sensor Accuracy[1]	T_{TSAL} CC	-6	–	6	°C	$T_J > 20°C$
		-10	–	10	°C	$0°C \leq T_J \leq 20°C$
		-18	–	18	°C	$-25°C \leq T_J < 0°C$
		-31	–	31	°C	$-40°C \leq T_J < -25°C$
Start-up time after enabling	t_{TSSTE} SR	–	–	15	µs	

1) The temperature sensor accuracy is independent of the supply voltage.

3.2.4 Power Supply Current

The total power supply current defined below consists of a leakage and a switching component.

Application relevant values are typically lower than those given in the following tables, and depend on the customer's system operating conditions (e.g. thermal connection or used application configurations).

Note: *These parameters are not subject to production test, but verified by design and/or characterization.*

Table 19 **Power Supply Parameters; V_{DDP} = 5 V**

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.[1]	Max.		
Active mode current Peripherals enabled f_{MCLK}/f_{PCLK} in MHz[2]	I_{DDPAE} CC	–	8.4	11.0	mA	32/64
		–	7.3	–	mA	24/48
		–	6.1	–	mA	16/32
		–	5.1	–	mA	8/16
		–	3.7	–	mA	1/1
Active mode current Peripherals disabled f_{MCLK}/f_{PCLK} in MHz[3]	I_{DDPAD} CC	–	4.7	–	mA	32/64
		–	4.1	–	mA	24/48
		–	3.3	–	mA	16/32
		–	2.6	–	mA	8/16
		–	1.5	–	mA	1/1
Active mode current Code execution from RAM Flash is powered down f_{MCLK}/f_{PCLK} in MHz	I_{DDPAR} CC	–	6.3	–	mA	32/64
		–	5.4	–	mA	24/48
		–	4.6	–	mA	16/32
		–	3.8	–	mA	8/16
		–	3.0	–	mA	1/1
Sleep mode current Peripherals clock enabled f_{MCLK}/f_{PCLK} in MHz[4]	I_{DDPSE} CC	–	5.9	–	mA	32/64
			5.4	–	mA	24/48
			4.8	–	mA	16/32
			4.3	–	mA	8/16
			3.7	–	mA	1/1
Sleep mode current Peripherals clock disabled Flash active f_{MCLK}/f_{PCLK} in MHz[5]	I_{DDPSD} CC	–	1.8	–	mA	32/64
			1.7	–	mA	24/48
			1.6	–	mA	16/32
			1.5	–	mA	8/16
			1.4	–	mA	1/1

(table continues...)

Table 19   (continued) Power Supply Parameters; V_{DDP} = 5 V

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.[1]	Max.		
Sleep mode current Peripherals clock disabled Flash powered down f_{MCLK}/f_{PCLK} in MHz[6]	I_{DDPSR} CC	–	1.2	–	mA	32/64
			1.1	–	mA	24/48
			1.0	–	mA	16/32
			0.8	–	mA	8/16
			0.7	–	mA	1/1
Deep Sleep mode current[7]	I_{DDPDS} CC	–	0.24	–	mA	
Wake-up time from Sleep to Active mode[8]	t_{SSA} CC	–	6	–	cycles	
Wake-up time from Deep Sleep to Active mode[9]	t_{DSA} CC	–	280	–	μsec	

1) The typical values are measured at T_A = + 25°C and V_{DDP} = 5 V.
2) CPU and all peripherals clock enabled, Flash is in active mode.
3) CPU enabled, all peripherals clock disabled, Flash is in active mode.
4) CPU in sleep, all peripherals clock enabled and Flash is in active mode.
5) CPU in sleep, Flash is in active mode.
6) CPU in sleep, Flash is powered down and code executed from RAM after wake-up.
7) CPU in sleep, peripherals clock disabled, Flash is powered down and code executed from RAM after wake-up.
8) CPU in sleep, Flash is in active mode during sleep mode.
9) CPU in sleep, Flash is in powered down mode during deep sleep mode.

Figure 11 shows typical graphs for active mode supply current for V_{DDP} = 5 V, V_{DDP} = 3.3 V, V_{DDP} = 1.8 V across different clock frequencies.
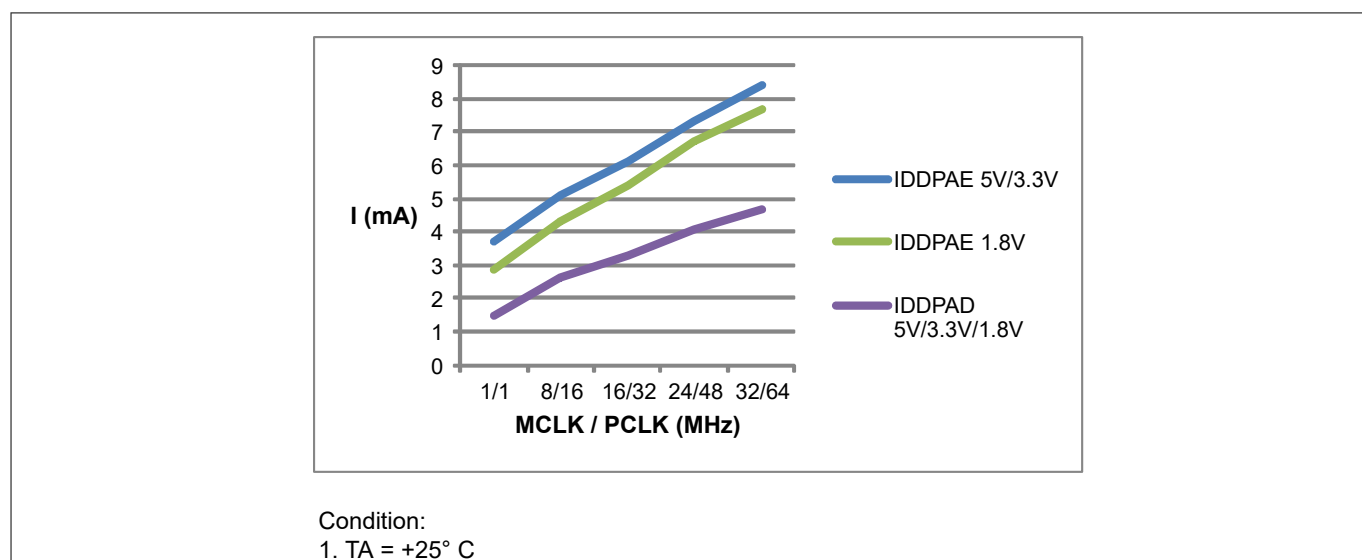
Figure 11   **Active mode, a) peripherals clocks enabled, b) peripherals clocks disabled: Supply current I_{DDPA} over supply voltage V_{DDP} for different clock frequencies**

3 Electrical Parameters

Figure 12 shows typical graphs for sleep mode current for V_{DDP} = 5 V, V_{DDP} = 3.3 V, V_{DDP} = 1.8 V across different clock frequencies.

Condition:
1. TA = +25° C
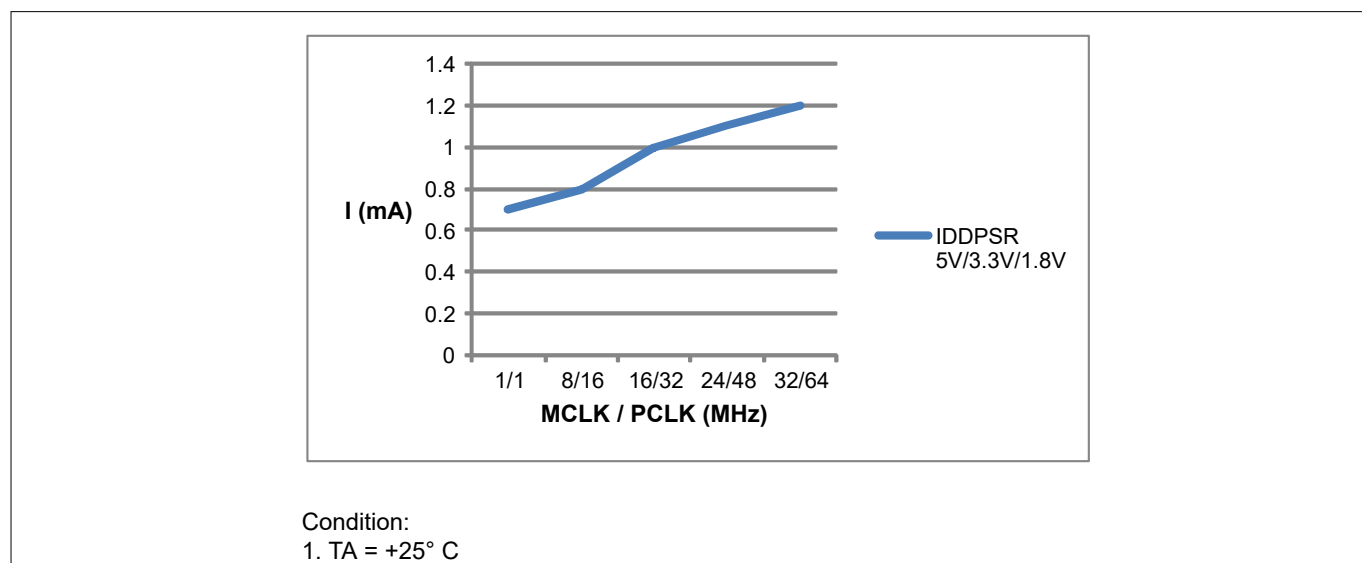
Figure 12   **Sleep mode, peripherals clocks disabled, Flash powered down: Supply current I_{DDPSR} over supply voltage V_{DDP} for different clock frequencies**

Table 20 provides the active current consumption of some modules operating at 5 V power supply at 25°C. The typical values shown are used as a reference guide on the current consumption when these modules are enabled.

Table 20   **Typical Active Current Consumption**

Active Current Consumption	Symbol	Limit Values Typ.	Unit	Note/Test Condition
Baseload current	I_{CPUDDC}	5.04	mA	Modules including Core, SCU, PORT, memories, ANATOP[1]
VADC and SHS	I_{ADCDDC}	3.4	mA	Set CGATCLR0.VADC to 1[2]
USIC0	$I_{USIC0DDC}$	0.87	mA	Set CGATCLR0.USIC0 to 1[3]
CCU40	$I_{CCU40DDC}$	0.94	mA	Set CGATCLR0.CCU40 to 1[4]
WDT	I_{WDTDDC}	0.03	mA	Set CGATCLR0.WDT to 1[5]
RTC	I_{RTCDDC}	0.01	mA	Set CGATCLR0.RTC to 1[6]

1)   Baseload current is measured with device running in user mode, MCLK=PCLK=32 MHz, with an endless loop in the flash memory. The clock to the modules stated in CGATSTAT0 are gated.
2)   Active current is measured with: module enabled, MCLK=32 MHz, running in auto-scan conversion mode.
3)   Active current is measured with: module enabled, alternating messages sent to PC at 57.6 kbaud every 200 ms.
4)   Active current is measured with: module enabled, MCLK=PCLK=32 MHz, 1 CCU4 slice for PWM switching from 1500 Hz and 1000 Hz at regular intervals, 1 CCU4 slice in capture mode for reading period and duty cycle.
5)   Active current is measured with: module enabled, MCLK=32 MHz, time-out mode; WLB = 0, WUB = 0x00008000; WDT serviced every 1 s.
6)   Active current is measured with: module enabled, MCLK=32 MHz, Periodic interrupt enabled.

3.2.5 Flash Memory Parameters

Note: *These parameters are not subject to production test, but verified by design and/or characterization.*

Table 21   Flash Memory Parameters

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Erase Time per page/sector	t_{ERASE} CC	6.8	7.1	7.6	ms	
Program time per block	t_{PSER} CC	102	152	204	µs	
Wake-Up time	t_{WU} CC	–	32.2	–	µs	
Read time per word	t_a CC	–	50	–	ns	
Data Retention Time	t_{RET} CC	10	–	–	years	Max. 100 erase/program cycles
Flash Wait States[1]	$N_{WSFLASH}$ CC	0	0	0		f_{MCLK} = 8 MHz
		0	1	1		f_{MCLK} = 16 MHz
		1	1.3	2		f_{MCLK} = 32 MHz
Fixed Flash Wait States configured in bit NVM_NVMCONF.WS	$N_{FWSFLASH}$ SR	0	0	1		NVM_CONFIG1.FIXWS = 1_B, $f_{MCLK} \leq 16$ MHz
		1	1	1		NVM_CONFIG1.FIXWS = 1_B, 16 MHz < $f_{MCLK} \leq 32$ MHz
Erase Cycles	N_{ECYC} CC	–	–	$5*10^4$	cycles	Sum of page and sector erase cycles
Total Erase Cycles	N_{TECYC} CC	–	–	$2*10^6$	cycles	

1)   Flash wait states are automatically inserted by the Flash module during memory read when needed. Typical values are calculated from the execution of the Dhrystone benchmark program.

3.3 AC Parameters

3.3.1 Testing Waveforms
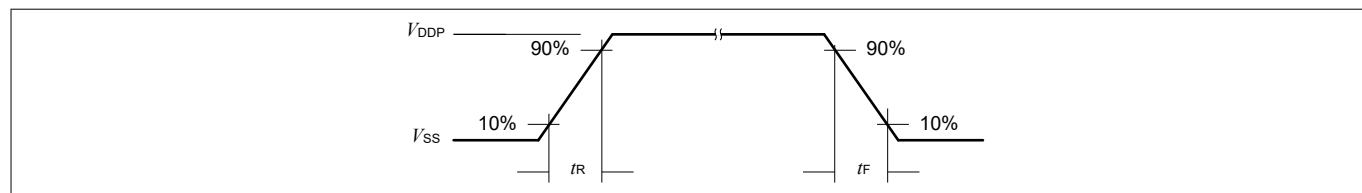
Figure 13 **Rise/Fall Time Parameters**
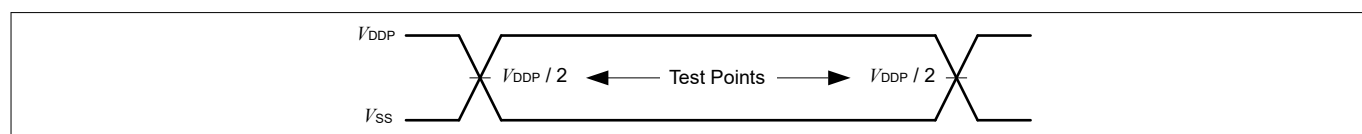
Figure 14 **Testing Waveform, Output Delay**
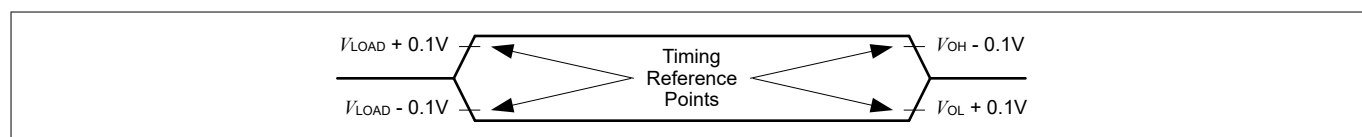
Figure 15 **Testing Waveform, Output High Impedance**

3.3.2 Power-Up and Supply Monitoring Characteristics

Table 22 provides the characteristics of the supply monitoring in XMC1100.

The guard band between the lowest valid operating voltage and the brownout reset threshold provides a margin for noise immunity and hysteresis. The electrical parameters may be violated while V_{DDP} is outside its operating range.

The brownout detection triggers a reset within the defined range. The prewarning detection can be used to trigger an early warning and issue corrective and/or fail-safe actions in case of a critical supply voltage drop.

Note: *These parameters are not subject to production test, but verified by design and/or characterization.*

Table 22   Power-Up and Supply Monitoring Parameters (Operating Conditions apply)[1]

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	**Typ.**	**Max.**		
V_{DDP} ramp-up time	t_{RAMPUP} SR	$V_{DDP}/$ $S_{VDDPrise}$	–	10^7	µs	
V_{DDP} slew rate	S_{VDDPOP} SR	0	–	0.1	V/µs	Slope during normal operation
	S_{VDDP10} SR	0	–	10	V/µs	Slope during fast transient within +/-10% of V_{DDP}
	$S_{VDDPrise}$ SR	0	–	10	V/µs	Slope during power-on or restart after brownout event
	$S_{VDDPfall}$[2] SR	0	–	0.25	V/µs	Slope during supply falling out of the +/-10% limits[3]
V_{DDP} prewarning voltage	V_{DDPPW} CC	2.1	2.25	2.4	V	ANAVDEL.VDEL_SELECT = 00$_B$
		2.85	3	3.15	V	ANAVDEL.VDEL_SELECT = 01$_B$
		4.2	4.4	4.6	V	ANAVDEL.VDEL_SELECT = 10$_B$
V_{DDP} brownout reset voltage	V_{DDPBO} CC	1.55	1.62	1.75	V	calibrated, before user code starts running
V_{DDP} voltage to ensure defined pad states	V_{DDPPA} CC	–	1.0	–	V	
Start-up time from power-on reset	t_{SSW} SR	–	320	–	µs	Time to the first user code instruction in all start-up modes[4]
BMI program time	t_{BMI} SR	–	8.25	–	ms	Time taken from a user-triggered system reset after BMI installation is requested

1)   Not all parameters are 100% tested, but are verified by design/characterization.
2)   A capacitor of at least 100 nF has to be added between V_{DDP} and V_{SSP} to fulfill the requirement as stated for this parameter.
3)   Valid for a 100 nF buffer capacitor connected to supply pin where current from capacitor is forwarded only to the chip. A larger capacitor value has to be chosen if the power source sink a current.
4)   This values does not include the ramp-up time. During start-up firmware execution, MCLK is running at 32 MHz and the clocks to peripheral as specified in register CGATSTAT0 are gated.
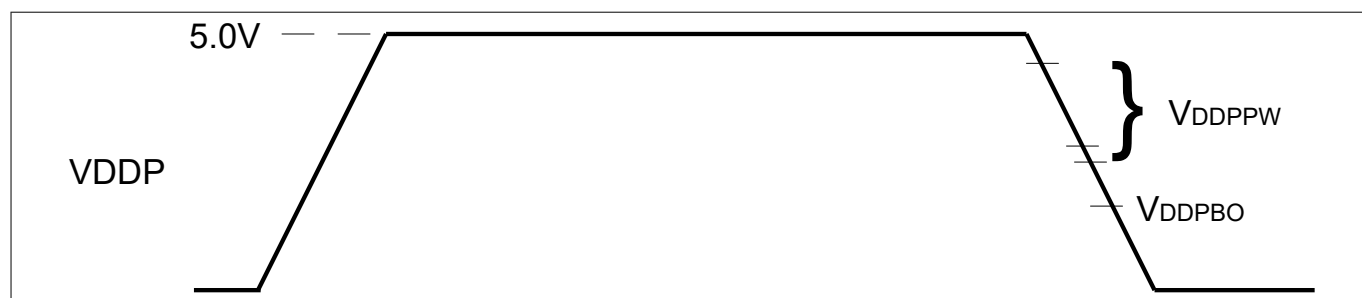
Figure 16   **Supply Threshold Parameters**

3.3.3   On-Chip Oscillator Characteristics

Note: *These parameters are not subject to production test, but verified by design and/or characterization.*

Table 23 provides the characteristics of the 64 MHz clock output from the digital controlled oscillator, DCO1 in XMC1100.
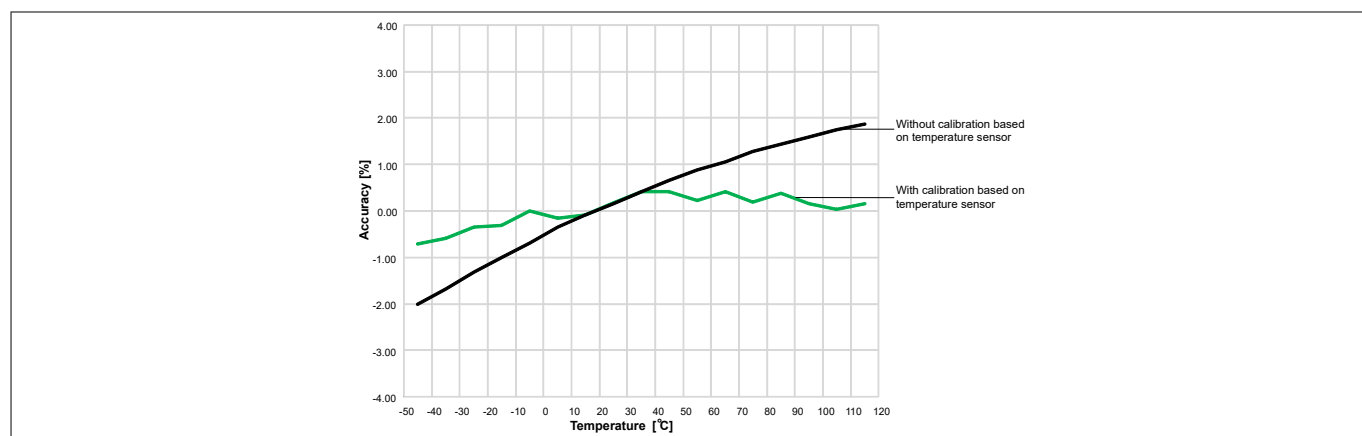
Table 23   **64 MHz DCO1 Characteristics (Operating Conditions apply)**

Parameter	Symbol	Limit Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Nominal frequency	f_{NOM} CC	–	64	–	MHz	under nominal conditions[1] after trimming
Accuracy[2]	Δf_{LT} CC	-1.7	–	3.4	%	with respect to f_{NOM}(typ), over temperature (0°C to 85°C)
		-3.9	–	4.0	%	with respect to f_{NOM}(typ), over temperature (-40°C to 105°C)

1)   The deviation is relative to the factory trimmed frequency at nominal V_{DDC} and T_A = + 25°C.
2)   The accuracy of the DCO1 oscillator can be further improved through alternative methods, refer to XMC1000 Oscillator Handling Application Note.

Figure 17 shows the typical curves for the accuracy of DCO1, with and without calibration based on temperature sensor, respectively.

Figure 17   **Typical DCO1 accuracy over temperature**

Table 24 provides the characteristics of the 32 kHz clock output from digital controlled oscillators, DCO2 in XMC1100.

Table 24   32 kHz DCO2 Characteristics (Operating Conditions apply)

Parameter	Symbol	Limit Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Nominal frequency	f_{NOM} CC	–	32.75	–	kHz	under nominal conditions[1] after trimming
Accuracy	Δf_{LT} CC	-1.7	–	3.4	%	with respect to f_{NOM}(typ), over temperature (0°C to 85°C)
		-3.9	–	4.0	%	with respect to f_{NOM}(typ), over temperature (-40°C to 105°C)

1)   The deviation is relative to the factory trimmed frequency at nominal V_{DDC} and T_A = + 25°C.

3.3.4   Serial Wire Debug Port (SW-DP) Timing

The following parameters are applicable for communication through the SW-DP interface.

Note: *These parameters are not subject to production test, but verified by design and/or characterization.*

Table 25   SWD Interface Timing Parameters (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
SWDCLK high time	t_1 SR	50	–	500000	ns	–
SWDCLK low time	t_2 SR	50	–	500000	ns	–
SWDIO input setup to SWDCLK rising edge	t_3 SR	10	–	–	ns	–
SWDIO input hold after SWDCLK rising edge	t_4 SR	10	–	–	ns	–
SWDIO output valid time after SWDCLK rising edge	t_5 CC	–	–	68	ns	C_L = 50 pF
		–	–	62	ns	C_L = 30 pF
SWDIO output hold time from SWDCLK rising edge	t_6 CC	4	–	–	ns	
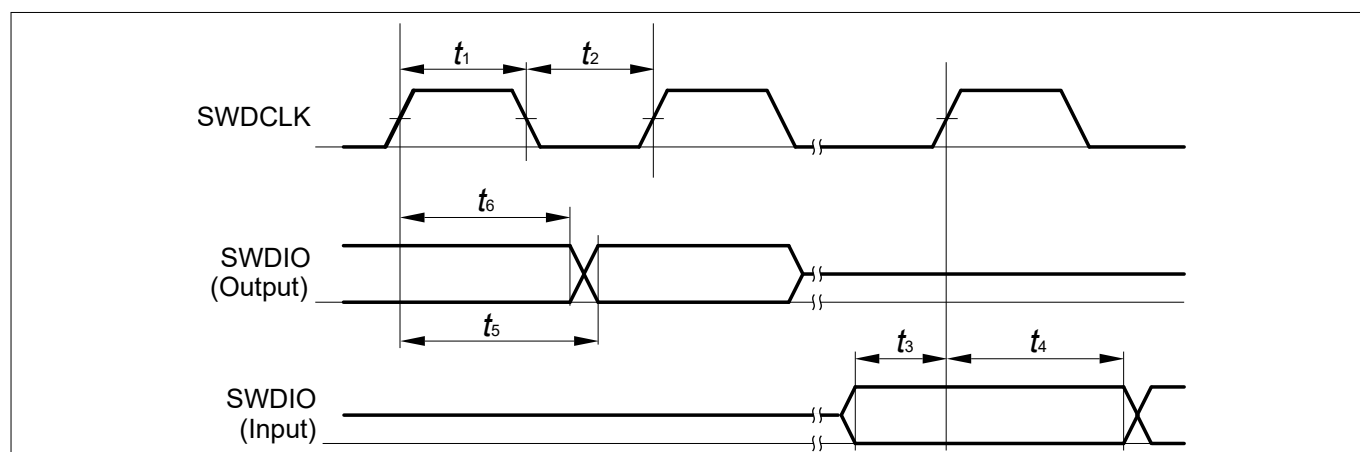
Figure 18   SWD Timing

3.3.5 SPD Timing Requirements

The optimum SPD decision time between 0_B and 1_B is 0.75 µs. With this value the system has maximum robustness against frequency deviations of the sampling clock on tool and on device side. However it is not always possible to exactly match this value with the given constraints for the sample clock. For instance for a oversampling rate of 4, the sample clock will be 8 MHz and in this case the closest possible effective decision time is 5.5 clock cycles (0.69 µs).

Table 26   Optimum Number of Sample Clocks for SPD

Sample Freq.	Sampling Factor	Sample Clocks 0_B	Sample Clocks 1_B	Effective Decision Time[1]	Remark
8 MHz	4	1 to 5	6 to 12	0.69 µs	The other closest option (0.81 µs) for the effective decision time is less robust.

1)   Nominal sample frequency period multiplied with 0.5 + (max. number of 0_B sample clocks).

For a balanced distribution of the timing robustness of SPD between tool and device, the timing requirements for the tool are:

- Frequency deviation of the sample clock is +/- 5%

- Effective decision time is between 0.69 µs and 0.75 µs (calculated with nominal sample frequency)

3.3.6 Peripheral Timings

Note: *These parameters are not subject to production test, but verified by design and/or characterization.*

3.3.6.1 Synchronous Serial Interface (USIC SSC) Timing

The following parameters are applicable for a USIC channel operated in SSC mode.

Note: *Operating Conditions apply.*

Table 27   USIC SSC Master Mode Timing

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	**Typ.**	**Max.**		
SCLKOUT master clock period	t_{CLK} CC	62.5	–	–	ns	
Slave select output SELO active to first SCLKOUT transmit edge	t_1 CC	80	–	–	ns	
Slave select output SELO inactive after last SCLKOUT receive edge	t_2 CC	0	–	–	ns	
Data output DOUT[3:0] valid time	t_3 CC	-10	–	10	ns	
Receive data input DX0/DX[5:3] setup time to SCLKOUT receive edge	t_4 SR	80	–	–	ns	
Data input DX0/DX[5:3] hold time from SCLKOUT receive edge	t_5 SR	0	–	–	ns	

Table 28 **USIC SSC Slave Mode Timing**

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
DX1 slave clock period	t_{CLK} SR	125	–	–	ns	
Select input DX2 setup to first clock input DX1 transmit edge[1]	t_{10} SR	10	–	–	ns	
Select input DX2 hold after last clock input DX1 receive edge[1]	t_{11} SR	10	–	–	ns	
Receive data input DX0/DX[5:3] setup time to shift clock receive edge[1]	t_{12} SR	10	–	–	ns	
Data input DX0/DX[5:3] hold time from clock input DX1 receive edge[1]	t_{13} SR	10	–	–	ns	
Data output DOUT[3:0] valid time	t_{14} CC	–	–	80	ns	

1) These input timings are valid for asynchronous input signal handling of slave select input, shift clock input, and receive data input (bits DXnCR.DSEN = 0).
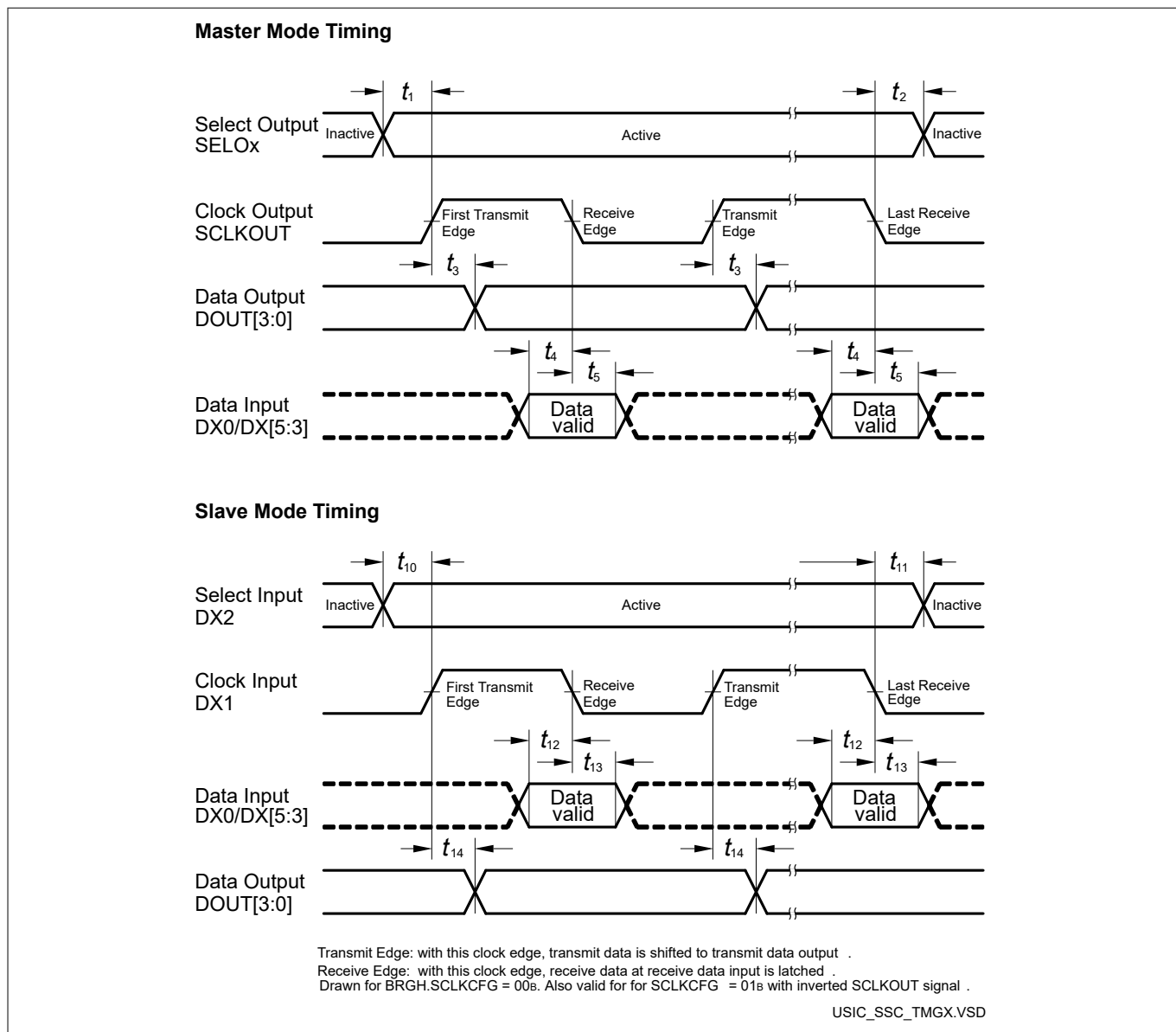
Figure 19   **USIC - SSC Master/Slave Mode Timing**

Note: *This timing diagram shows a standard configuration, for which the slave select signal is low-active, and the serial clock signal is not shifted and not inverted.*

3.3.6.2   Inter-IC (IIC) Interface Timing

The following parameters are applicable for a USIC channel operated in IIC mode.

Note: *Operating Conditions apply.*

Table 29   **USIC IIC Standard Mode Timing**[1)]

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Fall time of both SDA and SCL	t_1 CC/SR	–	–	300	ns	

(table continues...)

3 Electrical Parameters

Table 29 **(continued) USIC IIC Standard Mode Timing**[1]

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Rise time of both SDA and SCL	t_2 CC/SR	–	–	1000	ns	
Data hold time	t_3 CC/SR	0	–	–	µs	
Data set-up time	t_4 CC/SR	250	–	–	ns	
LOW period of SCL clock	t_5 CC/SR	4.7	–	–	µs	
HIGH period of SCL clock	t_6 CC/SR	4.0	–	–	µs	
Hold time for (repeated) START condition	t_7 CC/SR	4.0	–	–	µs	
Set-up time for repeated START condition	t_8 CC/SR	4.7	–	–	µs	
Set-up time for STOP condition	t_9 CC/SR	4.0	–	–	µs	
Bus free time between a STOP and START condition	t_{10} CC/SR	4.7	–	–	µs	
Capacitive load for each bus line	C_b SR	–	–	400	pF	

1) Due to the wired-AND configuration of an IIC bus system, the port drivers of the SCL and SDA signal lines need to operate in open-drain mode. The high level on these lines must be held by an external pull-up device, approximately 10 kOhm for operation at 100 kbit/s, approximately 2 kOhm for operation at 400 kbit/s.

Table 30 **USIC IIC Fast Mode Timing**[1]

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Fall time of both SDA and SCL	t_1 CC/SR	$20 + 0.1{*}C_b$[2]	–	300	ns	
Rise time of both SDA and SCL	t_2 CC/SR	$20 + 0.1{*}C_b$	–	300	ns	
Data hold time	t_3 CC/SR	0	–	–	µs	
Data set-up time	t_4 CC/SR	100	–	–	ns	
LOW period of SCL clock	t_5 CC/SR	1.3	–	–	µs	
HIGH period of SCL clock	t_6 CC/SR	0.6	–	–	µs	
Hold time for (repeated) START condition	t_7 CC/SR	0.6	–	–	µs	
Set-up time for repeated START condition	t_8 CC/SR	0.6	–	–	µs	
Set-up time for STOP condition	t_9 CC/SR	0.6	–	–	µs	
Bus free time between a STOP and START condition	t_{10} CC/SR	1.3	–	–	µs	
Capacitive load for each bus line	C_b SR	–	–	400	pF	

1) Due to the wired-AND configuration of an IIC bus system, the port drivers of the SCL and SDA signal lines need to operate in open-drain mode. The high level on these lines must be held by an external pull-up device, approximately 10 kOhm for operation at 100 kbit/s, approximately 2 kOhm for operation at 400 kbit/s.
2) C_b refers to the total capacitance of one bus line in pF.

3 Electrical Parameters
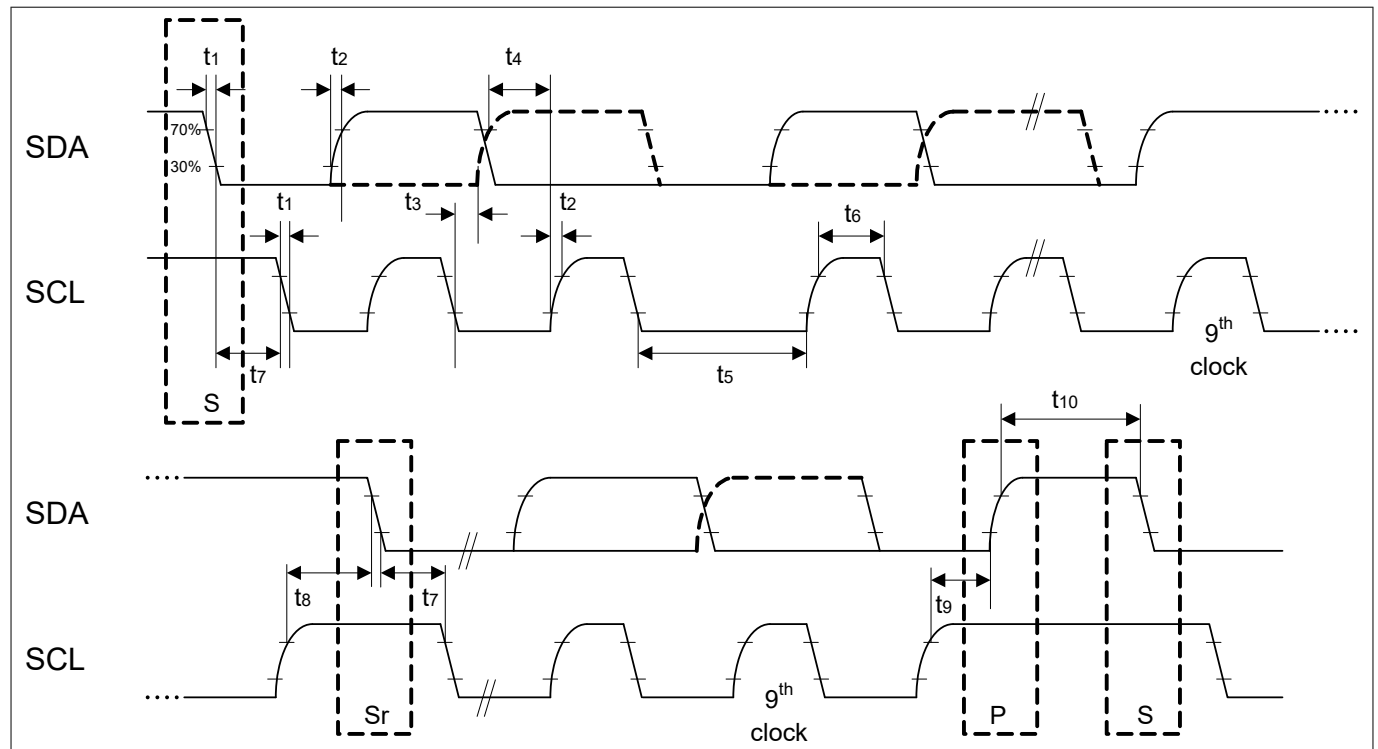
**Figure 20**   **USIC IIC Stand and Fast Mode Timing**

3.3.6.3 Inter-IC Sound (IIS) Interface Timing

The following parameters are applicable for a USIC channel operated in IIS mode.

Note: *Operating Conditions apply.*

Table 31 **USIC IIS Master Transmitter Timing**

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Clock period	t_1 CC	$2/f_{MCLK}$	–	–	ns	$V_{DDP} \geq 3$ V
		$4/f_{MCLK}$	–	–	ns	$V_{DDP} < 3$ V
Clock HIGH	t_2 CC	$0.35 \times t_{1min}$	–	–	ns	
Clock Low	t_3 CC	$0.35 \times t_{1min}$	–	–	ns	
Hold time	t_4 CC	0	–	–	ns	
Clock rise time	t_5 CC	–	–	$0.15 \times t_{1min}$	ns	
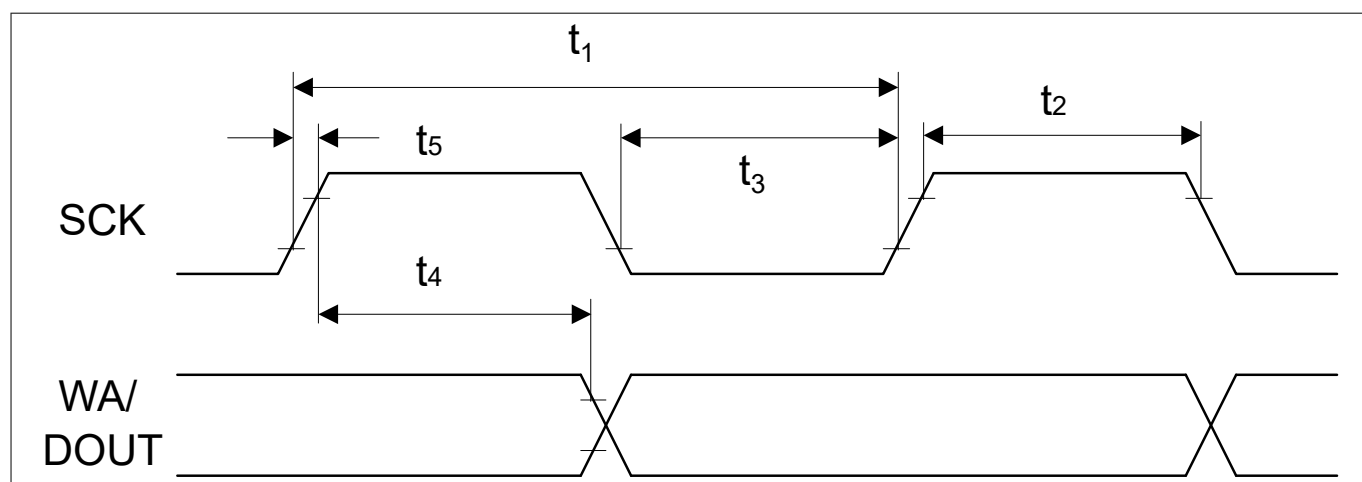
Figure 21 **USIC IIS Master Transmitter Timing**

Table 32   **USIC IIS Slave Receiver Timing**

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	**Typ.**	**Max.**		
Clock period	t_6 SR	$4/f_{MCLK}$	–	–	ns	
Clock HIGH	t_7 SR	$0.35 \times t_{6min}$	–	–	ns	
Clock Low	t_8 SR	$0.35 \times t_{6min}$	–	–	ns	
Set-up time	t_9 SR	$0.2 \times t_{6min}$	–	–	ns	
Hold time	t_{10} SR	10	–	–	ns	
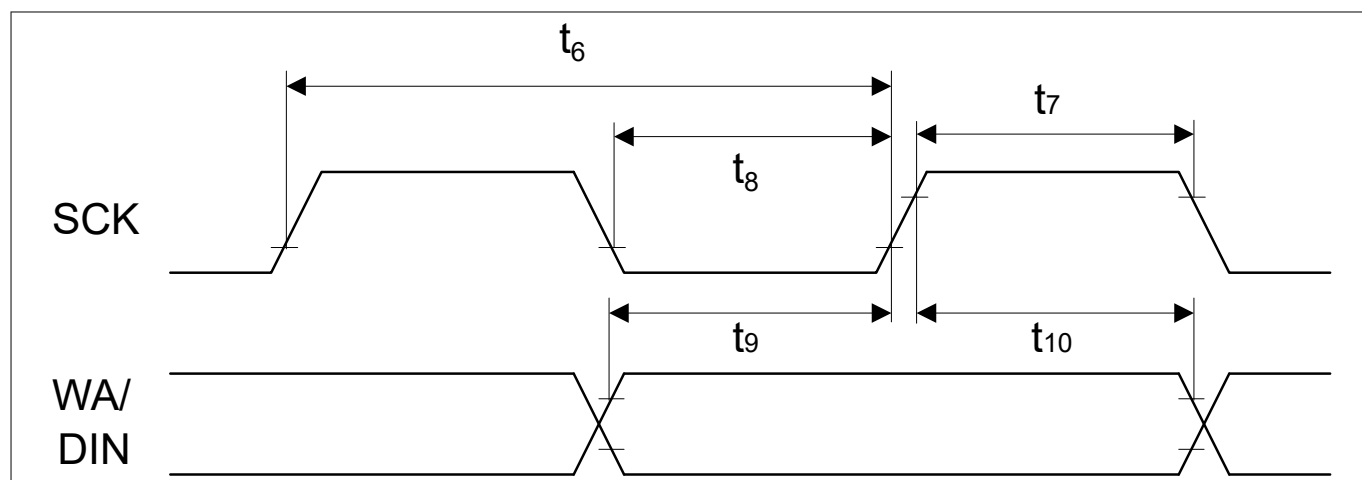
Figure 22   **USIC IIS Slave Receiver Timing**

4 Package and Reliability

The XMC1100 is a member of the XMC1000 Family of microcontrollers. It is also compatible to a certain extent with members of similar families or subfamilies.

Each package is optimized for the device it houses. Therefore, there may be slight differences between packages of the same pin-count but for different device types. In particular, the size of the exposed die pad may vary.

If different device types are considered or planned for an application, it must be ensured that the board layout fits all packages under consideration.

4.1 Package Parameters

Table 33 provides the thermal characteristics of the packages used in XMC1100.

Table 33 **Thermal Characteristics of the Packages**

Parameter	Symbol	Limit Values		Unit	Package Types
		Min.	**Max.**		
Exposed Die Pad Dimensions	Ex × Ey CC	–	2.7 × 2.7	mm	PG-VQFN-24-19
		–	3.7 × 3.7	mm	PG-VQFN-40-13
Thermal resistance Junction-Ambient	$R_{\Theta JA}$ CC	–	104.6	K/W	PG-TSSOP-16-8[1]
		–	70.3	K/W	PG-TSSOP-38-9[1]
		–	46.0	K/W	PG-VQFN-24-19[1]
		–	38.4	K/W	PG-VQFN-40-13[1]

1) Device mounted on a 4-layer JEDEC board (JESD 51-5); exposed pad soldered.

Note: *For electrical reasons, it is required to connect the exposed pad to the board ground V_{SSP}, independent of EMC and thermal requirements.*

4.1.1 Thermal Considerations

When operating the XMC1100 in a system, the total heat generated in the chip must be dissipated to the ambient environment to prevent overheating and the resulting thermal damage.

The maximum heat that can be dissipated depends on the package and its integration into the target board. The "Thermal resistance $R_{\Theta JA}$" quantifies these parameters. The power dissipation must be limited so that the average junction temperature does not exceed 115°C.

The difference between junction temperature and ambient temperature is determined by

$\Delta T = (P_{INT} + P_{IOSTAT} + P_{IODYN}) \times R_{\Theta JA}$

The internal power consumption is defined as

$P_{INT} = V_{DDP} \times I_{DDP}$ (switching current and leakage current).

The static external power consumption caused by the output drivers is defined as

$P_{IOSTAT} = \Sigma((V_{DDP}-V_{OH}) \times I_{OH}) + \Sigma(V_{OL} \times I_{OL})$

The dynamic external power consumption caused by the output drivers (P_{IODYN}) depends on the capacitive load connected to the respective pins and their switching frequencies.

If the total power dissipation for a given system configuration exceeds the defined limit, countermeasures must be taken to ensure proper system operation:

- Reduce V_{DDP}, if possible in the system
- Reduce the system frequency
- Reduce the number of output pins
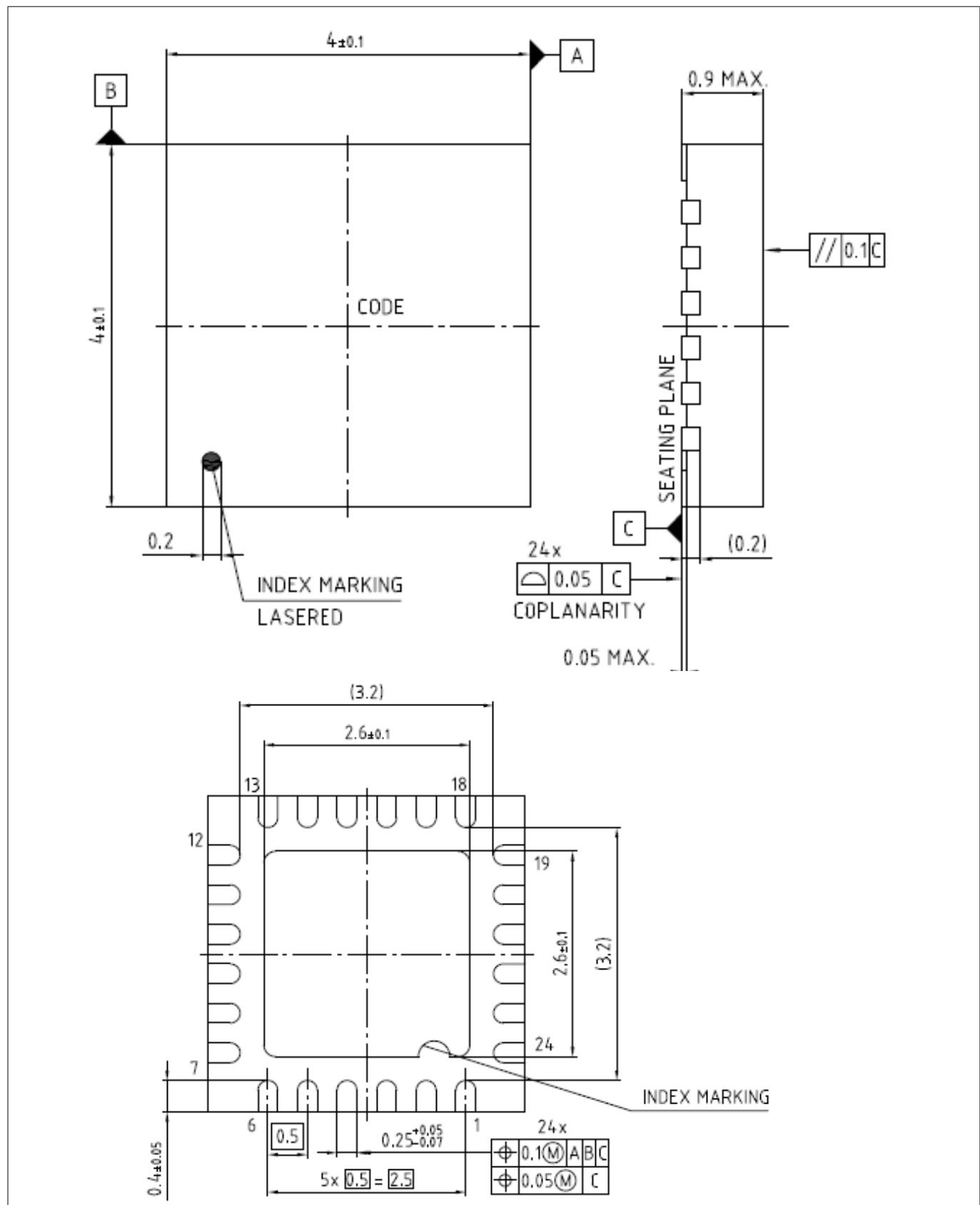- Reduce the load on active output drivers
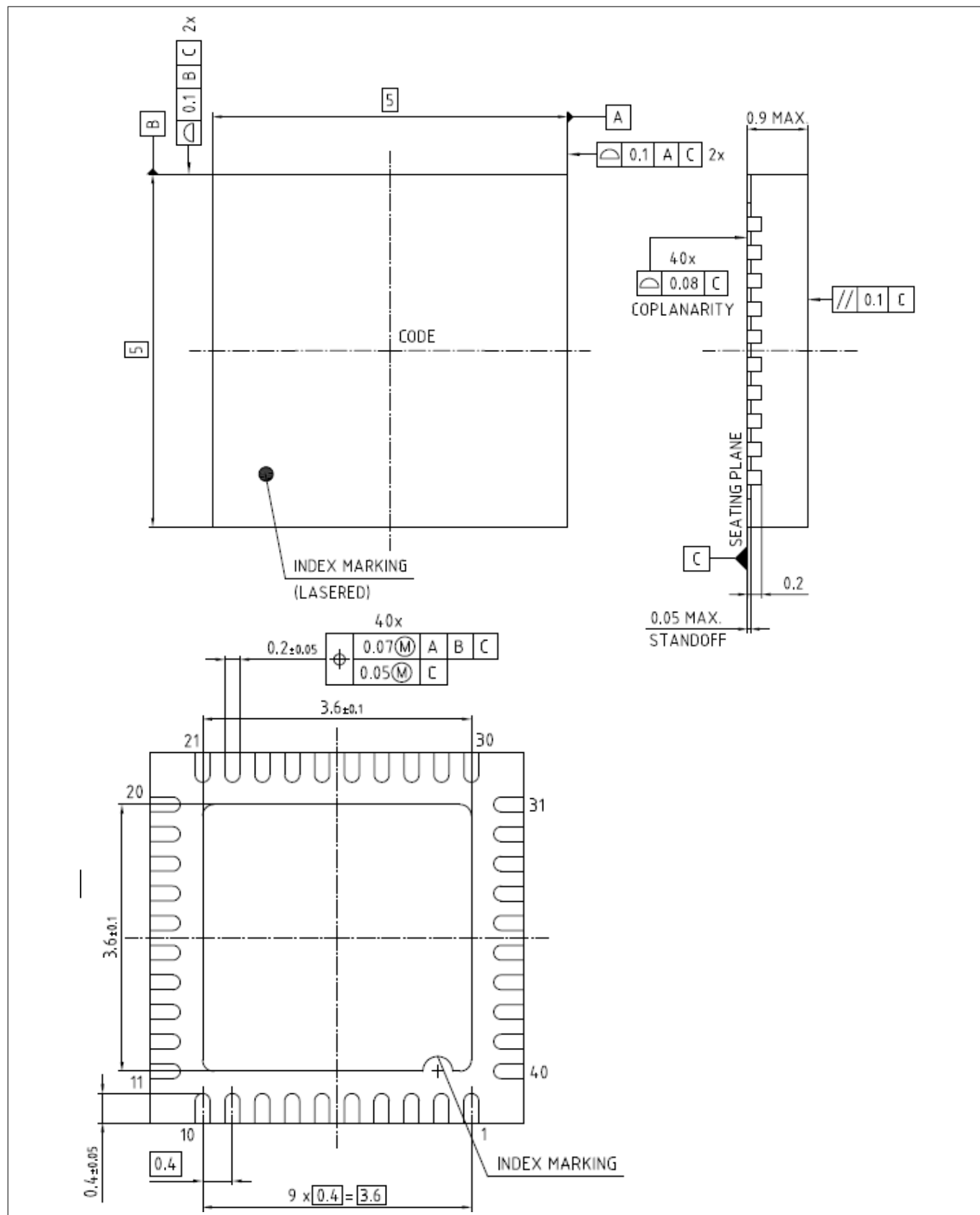
4.2 Package Outlines
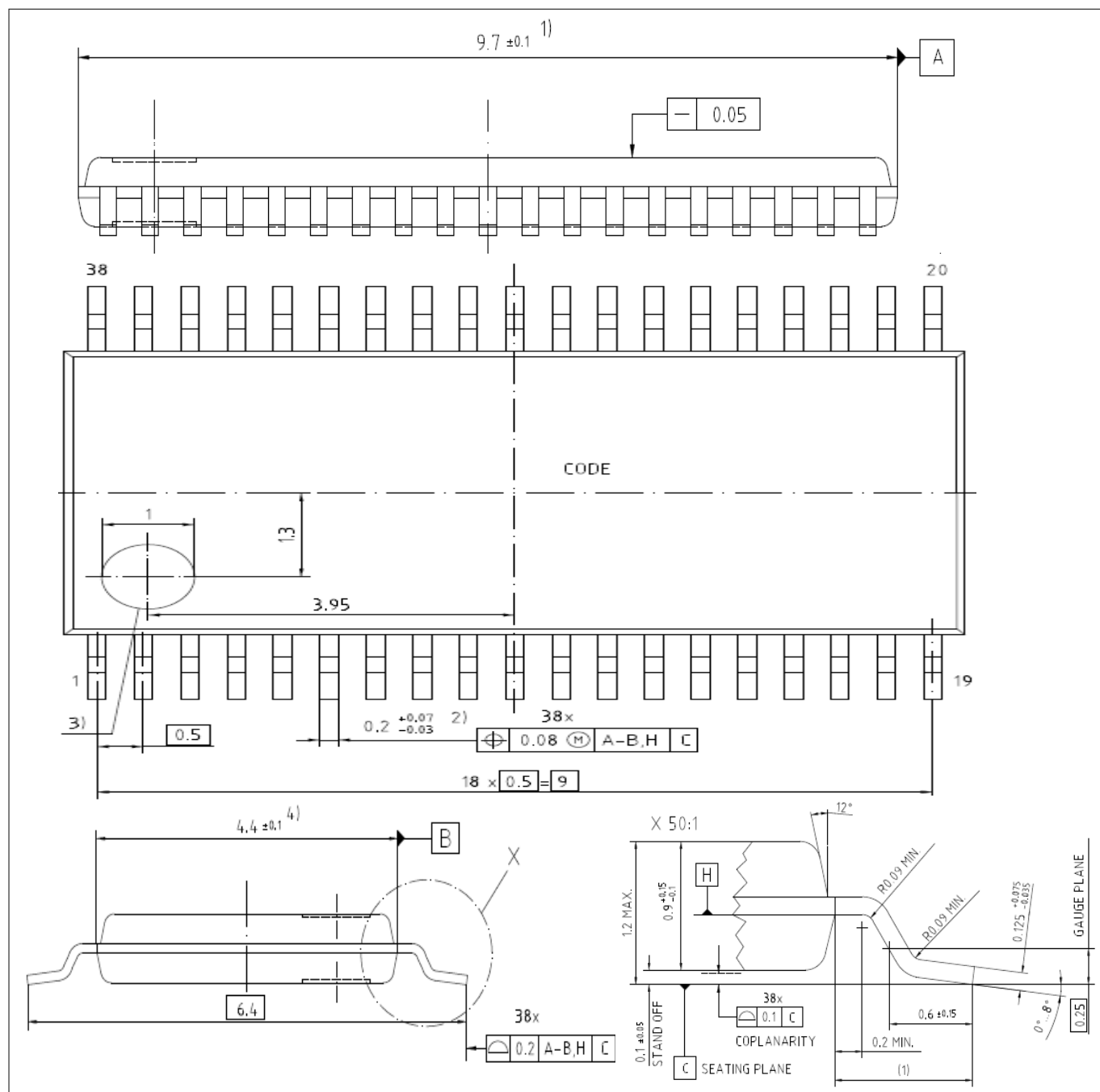
Figure 23 PG-TSSOP-38-9

Figure 24   **PG-TSSOP-16-8**

Figure 25　　　　　**PG-VQFN-24-19**

4 Package and Reliability

Figure 26   **PG-VQFN-40-13**

All dimensions in mm.

5 Quality Declaration

Table 34 shows the characteristics of the quality parameters in the XMC1100.

Table 34   **Quality Parameters**

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	**Max.**		
ESD susceptibility according to Human Body Model (HBM)	V_{HBM} SR	–	4000	V	Conforming to EIA/ JESD22-A114-B
ESD susceptibility according to Charged Device Model (CDM) pins	V_{CDM} SR	–	1000	V	Conforming to JESD22-C101-C
Moisture sensitivity level	*MSL* CC	–	–	–	JEDEC J-STD-020D
• TSSOP-16, TSSOP-38			3		
• VQFN-24, VQFN-40			1		
Soldering temperature	T_{SDR} SR	–	260	°C	Profile according to JEDEC J-STD-020D

6   Revision History

Document revision	Date	Description of changes
V1.8	2016-09	In Absolute Maximum Ratings renamed parameter V_{CM} to V_{INP2}, as the limitation is related to most P2 pins, also if no ACMP is available. Clarified limit to pins P2.[1,2,6:9,11] in Overload specification.
V1.9	2025-01-22	Updated template. Updated Moisture sensitivity level in Quality Declaration section.
V2.0	2025-04-22	Updated On-Chip Memories in Summary of Features section. Added XMC1100-T038X0128 and XMC1100-T038X0200 in Table 1 and Table 4. Updated the block diagram to show 64k to 200K.
V2.1	2025-06-30	Updated ESD ratings in Table 34

Trademarks

All referenced product or service names and trademarks are the property of their respective owners.