overview

FM6124 is a driver IC specially designed for LED modules and displays, with 16 constant current output drive capabilities. FM6124 adopts the "input "out clamping" patented technology, which can effectively eliminate the dark phenomenon of the first row and prevent the lamp beads from being damaged. FM6124 adopts enhanced blanking function design, which has excellent blanking effect. At the same time, FM6124 has excellent anti-interference characteristics , Constant current and low gray effect are not affected by the PCB board. Different external resistors can be selected to adjust the current of the output stage arbitrarily, and the brightness of the LED can be precisely controlled.

FM6124 will cache 16bit display data during the display process (the falling edge of OE), so the system can continue to store in the FM6124 display process 16bit serial data, compared with general constant current source chips, the refresh rate can be increased by more than 50%.

FM6124 internally adopts current precise control technology, which can make the inter-chip error less than ±3.5%, and the inter-channel error less than ±2%.

features

ÿ 16 equal current output channels

ÿ Output current setting range: 0.5ÿ

35mA×16@VDD=5V constant current output 0.5ÿ

25mA×16@VDD=3.3V constant current output ÿ Current accuracy

Current inconsistency between channels: ±1.25% (typical value)

±2% (maximum

value) Current non-uniformity between chips: ±2% (typical

value) ±3.5% (maximum

value) ÿ Fast output current response (Minimum value): 30ns@VDD=5V ÿ I/O

Schmitt trigger trigger input ÿ Data transmission

frequency: fMAX=30MHz (maximum)

ÿ ESD HBM PASS 4KV

ÿPower supply voltage: VDD=3.3ÿ6V

ÿWorking temperature range: Topr=-40ÿ85ÿ

ÿ It has the function of improving lamp bead damage

ÿ Excellent blanking effect

ÿ Effectively eliminate the first row of dark, low gray blocks, low gray color cast and low gray spots ÿ

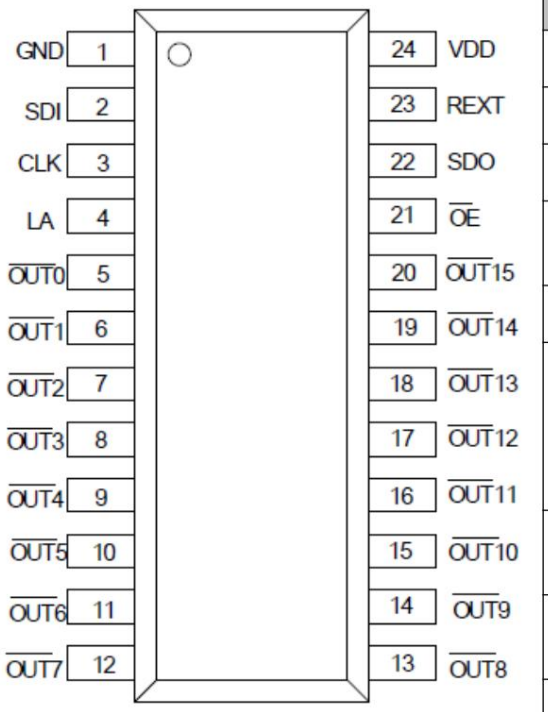
Excellent anti-interference ability and low gray scale effect ÿ

Improve caterpillar phenomenon caused by lamp bead damage

ÿ Integration Double buffering, the refresh rate is more than 50% higher than that of

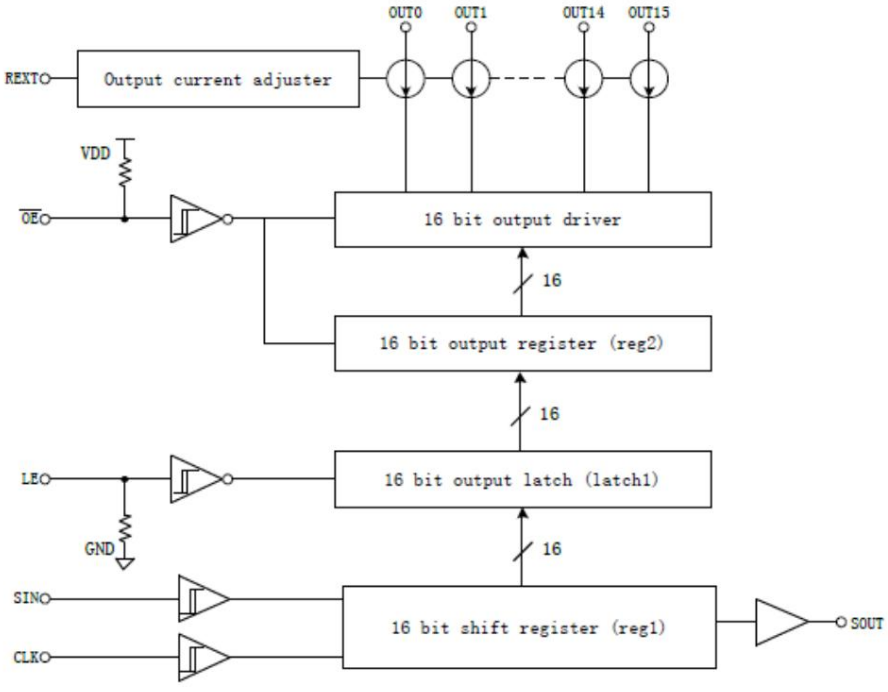
general constant current chips ÿ Package type: SSOP-24

Pin definition and description

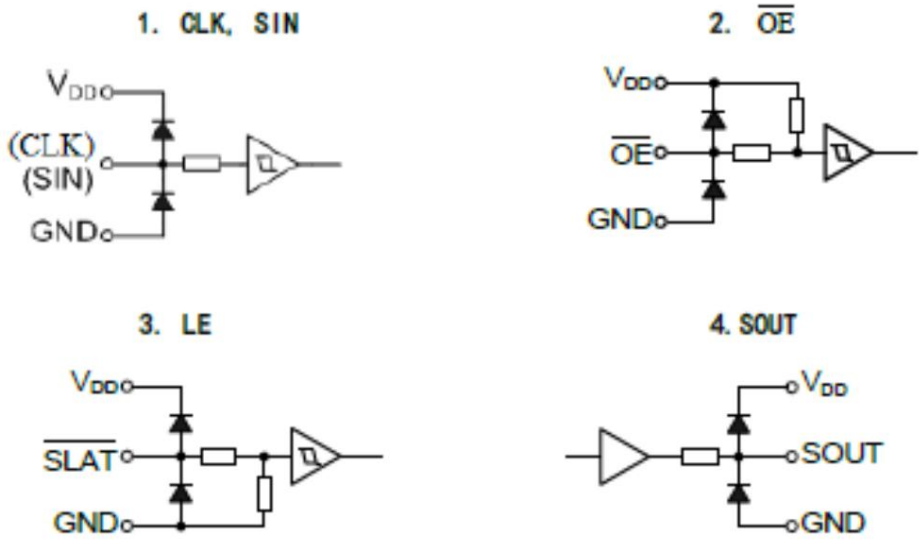


Pin number	Pin definition	pin name
1	GND	chip ground pin
2	SDI	input to the serial data input of the shift register
3	CLK	clock signal input
4	THE	When the data latch input LE is high, the data is transferred to the latch. Constant
5-20	$\overline{OUT0}$—$\overline{OUT15}$	current output
21	$\overline{OE}$	Output enable signal input and buffer data on falling edge When OE is high, turn off OUT0-OUT15 When OE is low level, open the OUT0-OUT15 serial
22	SDO	data output terminal, which can be connected to the next drive chip The SDI
23	RIGHT	terminal is externally connected to the output terminal of the adjustment resistor, which can adjust the output current of all channels
24	VDD	3.3V/5V power input terminal

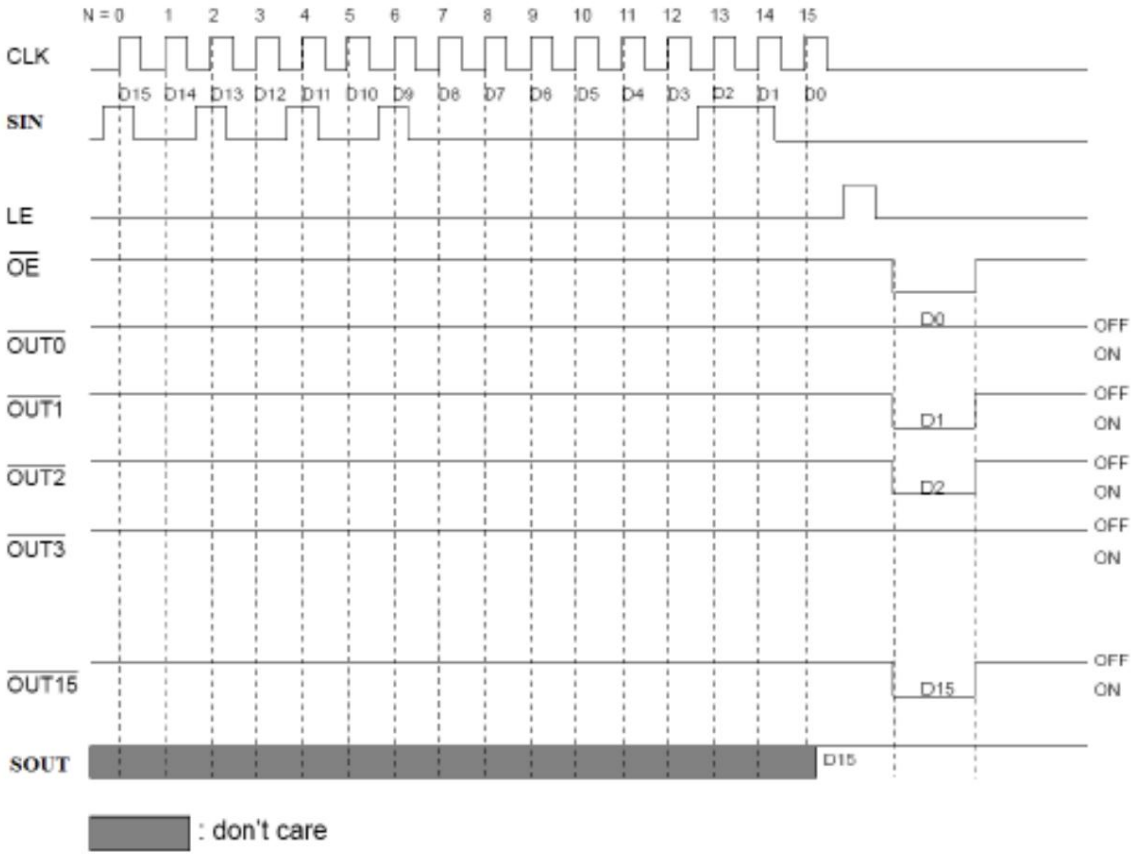
Internal block diagram



I/O equivalent circuit



Timing diagram



truth table

CLK	THE	$\overline{OE}$	SIN	$\overline{OUT0}$ … $\overline{OUT7}$ … $\overline{OUT15}$	SALT
	H	L	Dn	DN`…DN-7…DN-15	DN-15
	L	L	Dn+1	no change	DN-14
	H	L	Dn+2	DN+2…DN-5…DN-13	DN-13
	X	L	Dn+3	DN+2…DN-5…DN-13	DN-13
	X	H	Dn+3	OFF	DN-13

Absolute Maximum Ratings (TA=25ÿ)

characteristic	symbol	Rating unit	
voltage	VDD	0-7.0	IN
Output current	IO	35	mA
Input voltage	COME	-0.4—VDD+0.4 V	
Output withstand voltage	VOUT	30	IN
Clock frequency	FCLK	30	MHZ
ground terminal current	IGND	+600	mA
power consumption	PD	3	IN
thermal resistance	RTH(s)	39.15	ÿ/W
Operating temperature	TOPR	-40—85	ÿ
storage temperature	TSTG	-55—150	ÿ

DC characteristics (if not otherwise stated, TA=40ÿ—85ÿ)

	Symbol Test Condition Min Typ Max Unit					
Characteristics Supply Voltage	VDD	·	3.3	5	6.0	IN
Output voltage VO(ON) when ON		$\overline{OUTn}$	0.6	·	4	IN
High-level logic input voltage VIH Low-level logic		·	0.7*VDD	·	VDD	IN
input voltage VIL		·	GND	·	0.3*VDD V	
SOUT High level output current IOH		VDD=5V	·	-1	·	mA
SOUT low level output current IOL		VDD=5V	·	1	·	mA
Constant current output	IO	$\overline{OUTn}$	0.5	-	35	mA

Dynamic characteristics (if not otherwise stated, VDD=4.5—5.5V, TA=40°C—85°C)

characteristic	Symbol	Test Circuit	Test Conditions	Min	Typ	Max	Unit
Serial data transmission frequency	FCLK	6	·	·	·	30	MHZ
Clock pulse width	TWCLK	6	SCK=H/L	20	·	·	nS
Buffer pulse width	TWLE	6	LE=H	20	·	·	nS
Enable pulse width	TWOE	6	$\overline{OE}$ =H/LÿREXT=890ÿ	30	·	·	nS
hold time	THOLD1	6	·	5	·	·	nS
	THOLD2	6	·	5	·	·	nS
build time	TSETUP1	6	·	5	·	·	nS
	TSETUP2	6	·	5	·	·	nS
Maximum Clock Rise Time	TR	6		·	·	500	nS
Maximum Clock Fall Time	TR	6		·	-	500	nS

electrical characteristics

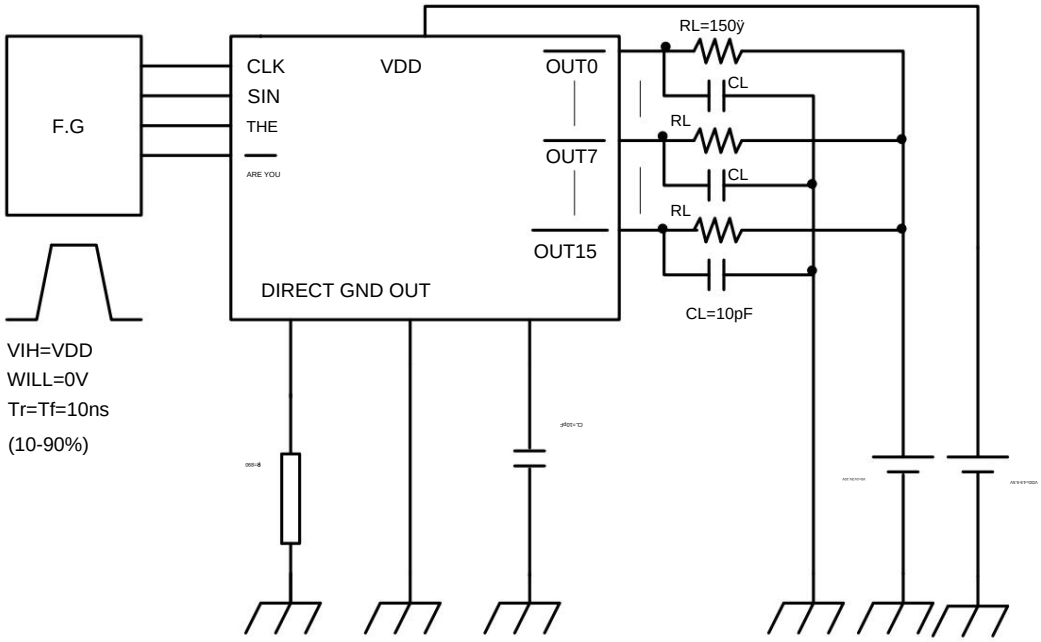
Characteristic	symbol	test circuit	Test Conditions	Min	Typ	Max	Unit
High level logic output voltage	VOH	1	IOH=-1mAÿSOUT	VDD-0.4	·	VDD	V
Low level logic output voltage	VOL	1	IOH=+1mAÿSOUT	·	·	0.4	IN
High level logic input current	IIH	2	VIN=VDD,OE,SIN,CLK	·	·	1	uA
Low level logic input current	IIL	3	VIN=GND,LE,SINÿCLK	·	·	-1	uA
supply current	IDD1	4	REXT=missed, OUT OFF	·	2.0	5.0	mA
	IDD2	4	REXT=1200ÿOUT OFF	·	5.5	9	mA
	IDD3	4	REXT=600ÿOUT OFF	·	6.5	10	mA
	IDD4	4	REXT=1200ÿOUT ON	·	8.2	12	mA
	IDD5	4	REXT=600ÿOUT ON	·	10	15	mA
Constant current output	IO1	5	VDD=5.0VÿVO=2.0VÿREXT=1.19Kÿ	·	15	·	mA
	IO2	5	VDD=5.0VÿVO=2.0VÿREXT=595ÿ	·	30	·	mA
Constant current error	ÿIO	5	VDD=5.0VÿVO=2.0VÿREXT=1.19Kÿ	·	±0.15	±0.37	mA
Constant Current Supply Voltage Regulation	CEOD	5	VDD=4.5-5.5V VO=2.0V,REXT=1.19Kÿ	·	±0.2	-	%/IN

Constant Current Output Voltage Regulation	%VO OUT	5	VDD=5.0V VO=1.0-3.0V,REXT=1.19Kÿ		±0.1		%/IN
Pull-up resistor RUP		3	$\overline{OE}$	200	240	350 Kÿ	
Pull-down resistor	RDO WN	2	THE	250	340	450 Kÿ	

Switching characteristics

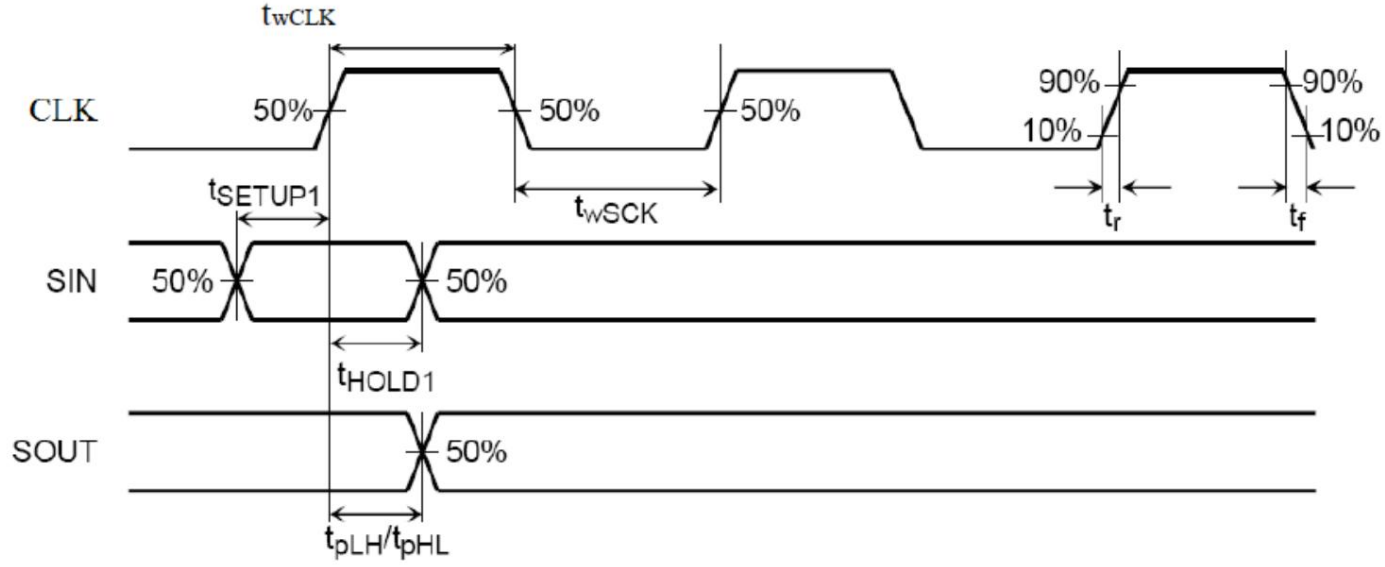
characteristic		Symbol	Test Circuit	Test Condition	Min Value	Typical Value	Max	Unit
transmission delay time	$\overline{OE}$—$\overline{OUT0}$	TPLH3	6	LE=H		25	40	nS
	$\overline{OE}$—$\overline{OUT1}$	TPHL3	6	LE=H		30	50	
	CLK-SOUT TPHL		6			25	30	
Output Rise Time		TOR	6	10-90% of the voltage waveform		15	20	nS
Output fall time		TOR	6	90-10% of the voltage waveform	-	26	31	nS

test circuit

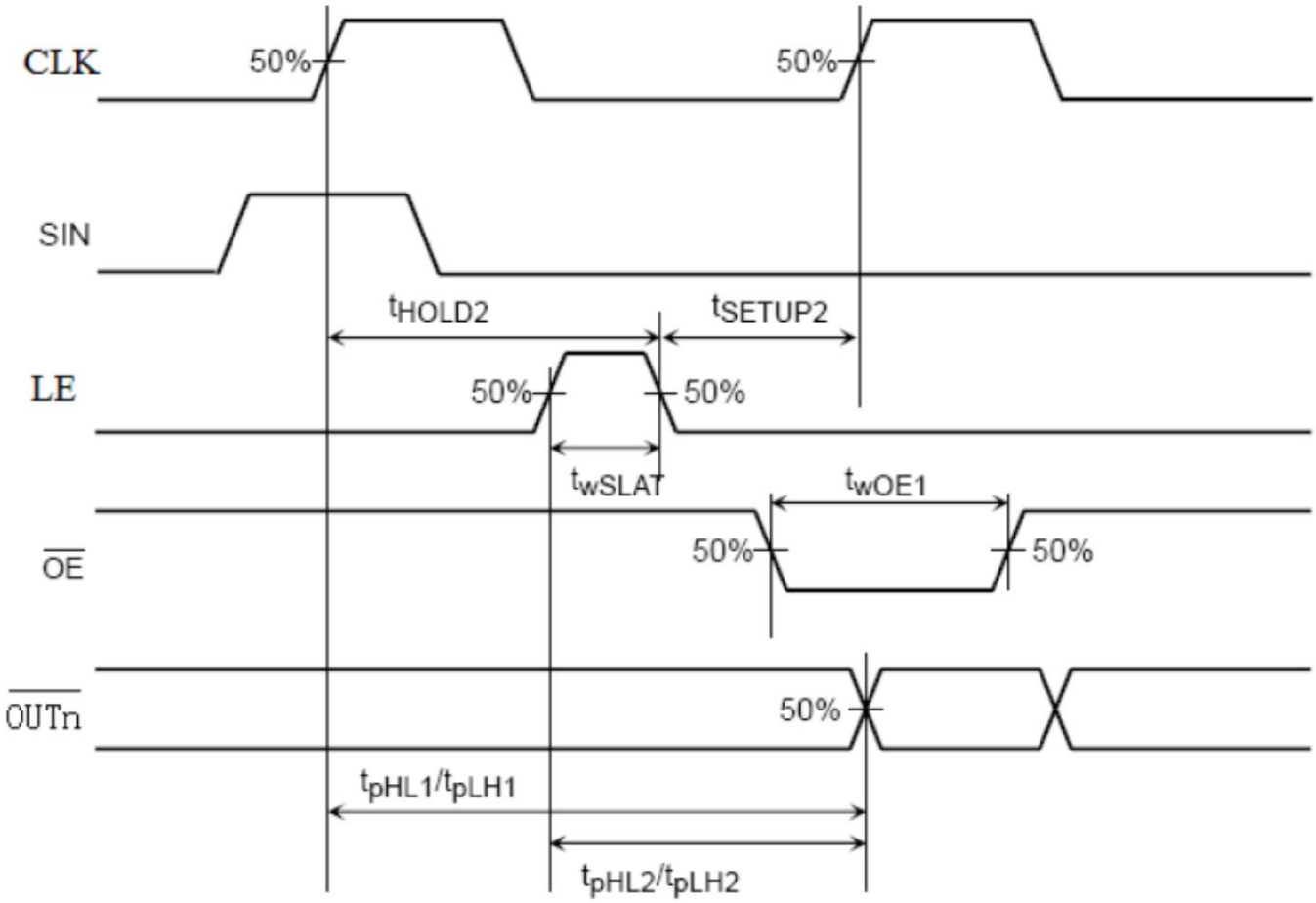


timing waveform

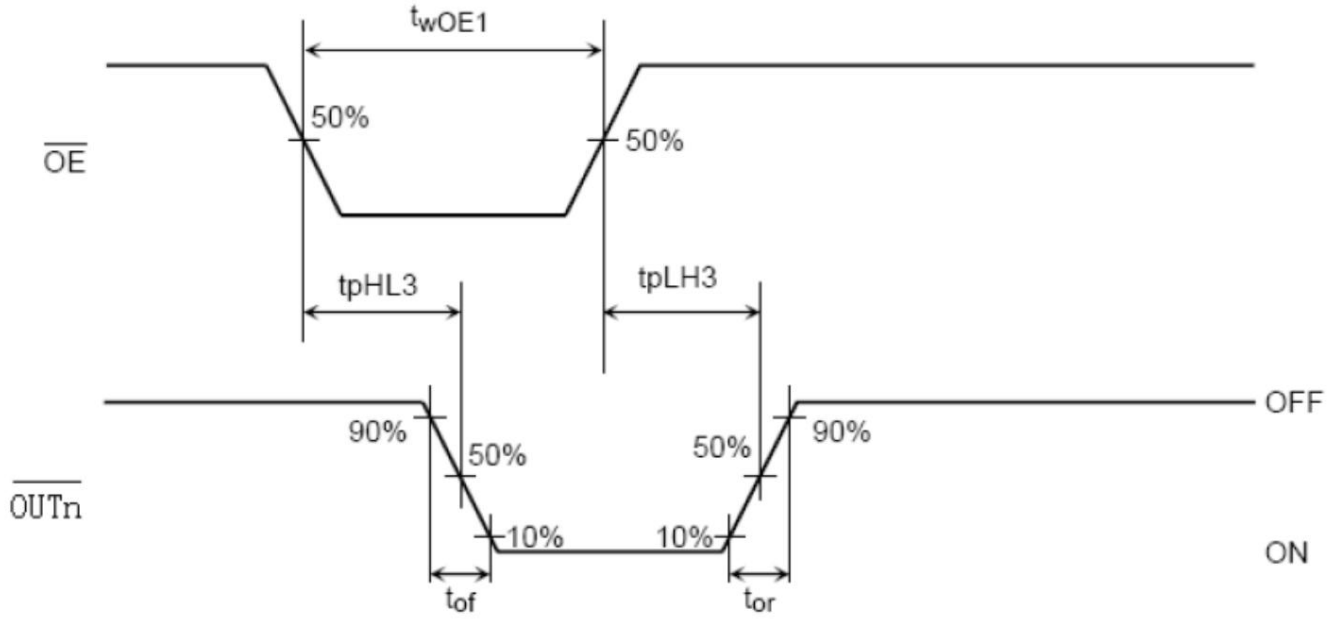
1.CLKÿSINÿSOUT



2.CLKÿSINÿLEÿOEÿOUTN



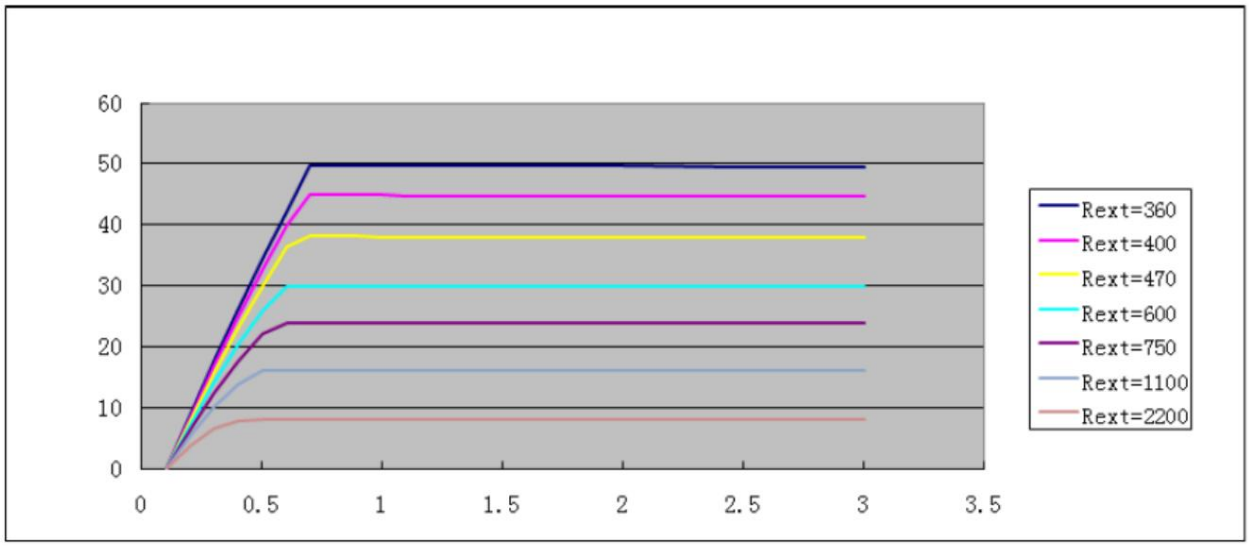
3.OUTN



application information

FM6124 adopts precise current drive control technology, and the current difference between different channels of the same chip and different chips is extremely small. 1) The current difference between channels is <±2%, and the current difference between chips is <±3.5%.

2) It has a current output characteristic that is not affected by the load terminal voltage, as shown in the figure below. The output current will not change with the change of LED forward voltage VF .

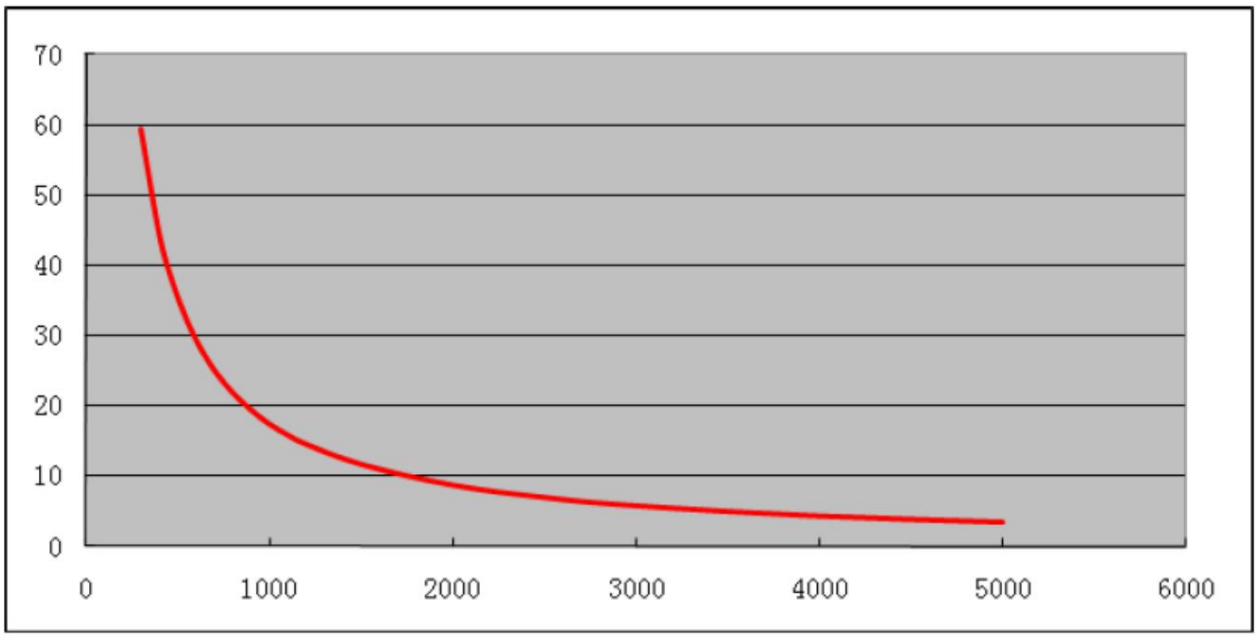


Adjust output current

FM6124 adjusts the output current (Iout) through an external resistor Rext, the calculation formula is:

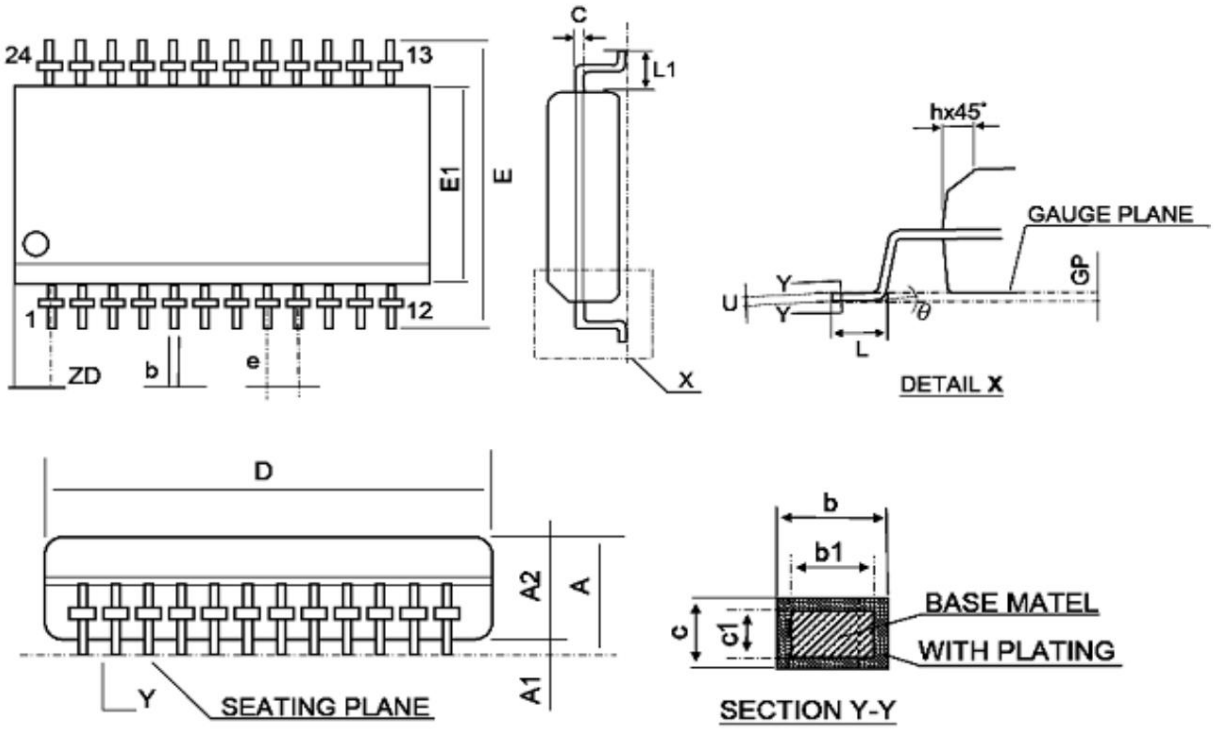
VR-EXT=1.191Vÿ

Iout=(VR-EXT/Right)*15



Package information

SSOP24



SYMBOL	DIMENSION (mm)			DIMENSION (mil)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	1.60	1.75	53	63	69
A1	0.10	0.15	0.25	4	6	10
A2			1.50			59
b	0.20		0.30	8		12
b1	0.20	0.254	0.28	8	10	11
c	0.18		0.25	7		10
c1	0.18	0.203	0.23	7	8	9
D	8.56	8.66	8.74	337	341	344
E	5.80	6.00	6.20	228	236	244
E1	3.80	3.90	4.00	150	154	157
e	0.635 BSC			25 BSC		
h	0.25	0.42	0.50	10	17	20
L	0.40	0.635	1.27	16	25	50
L1	1.00	1.05	1.10	39	41	43
ZD	0.838 REF			33 REF		
Y			0.10			4
θ	0°		8°	0°		8°