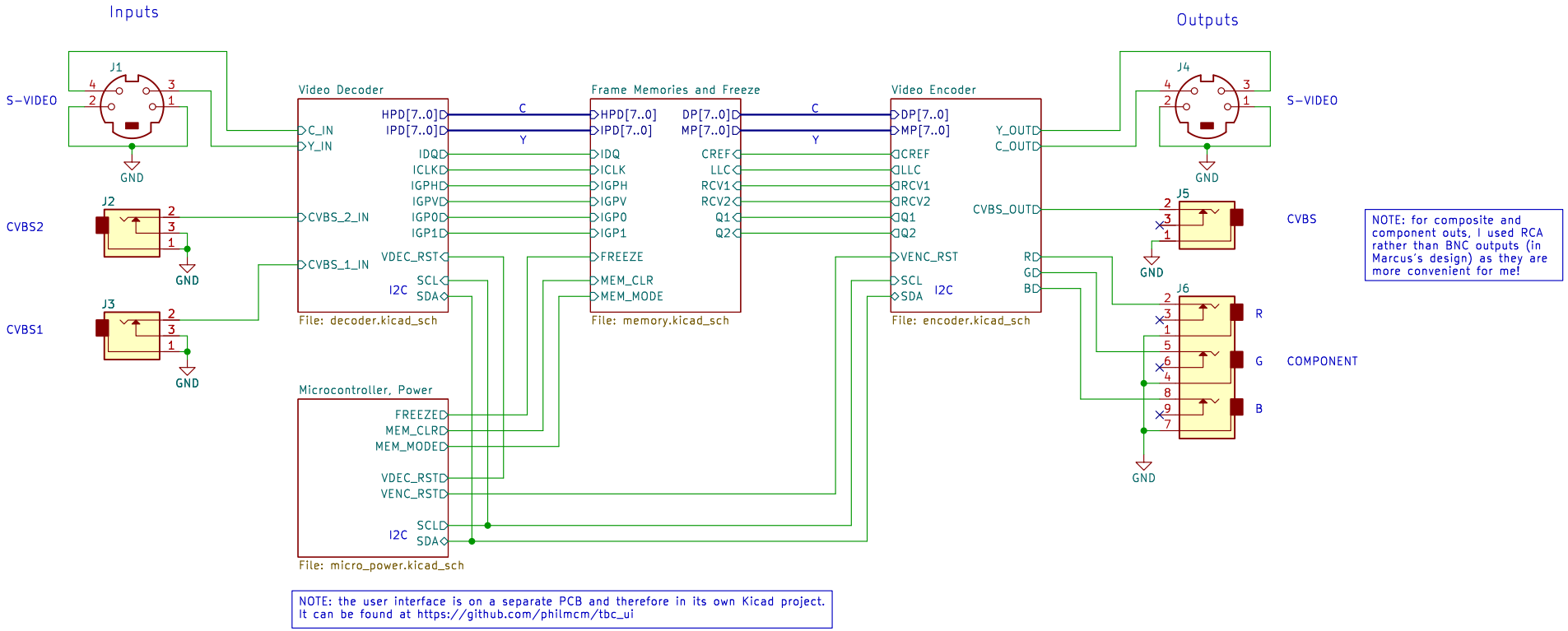

NOTE: Major changes in this design compared to Marcus's original schematic (see below) are the implementation of a modern STM32 microcontroller and 4-line OLED display. Other enhancements have been made, including the addition of RESET circuitry driven by the microcontroller, as well as a rotary encoder and LEDs in the UI.
Otherwise, only minor corrections and enhancements are made to the original circuit. These are noted in the respective schematic sheet to follow.
Links:
https://web.archive.org/web/20181219122351/http://marcusgun.awardspace.com/newvidproc.html
https://web.archive.org/web/20051101234823/http://www.astro.uu.se/~marcus/private/tbcsch.jpg

https://github.com/philmcm/tbc
Wavelet Engineering Pty Ltd (ACN 159 717 665)

Sheet: /
File: tbc.kicad_sch

Title: Time Base Corrector and Video Scaler

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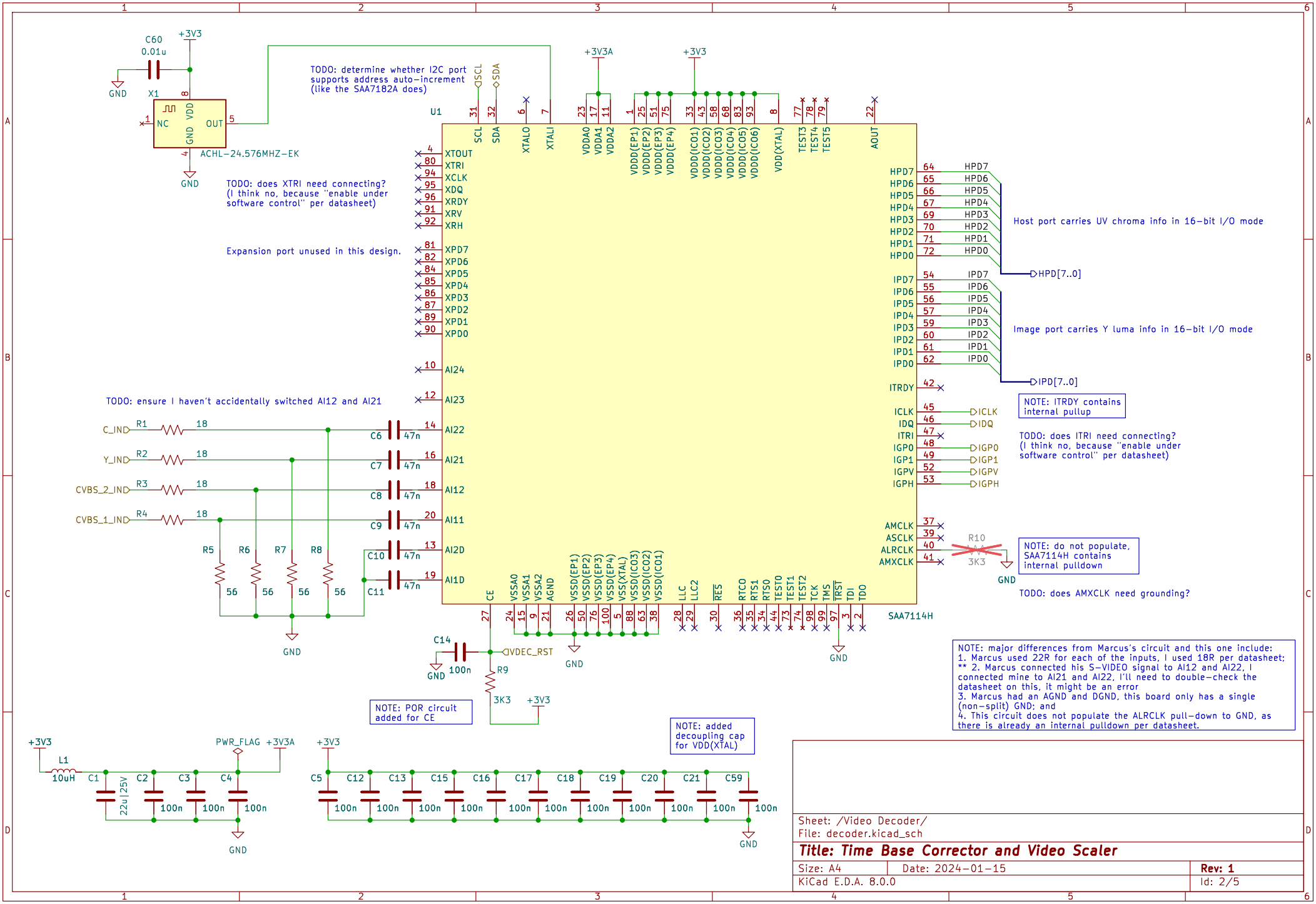
C60
0.01u
+3V3
GND
X1
NC
VDD
GND
OUT
ACHL-24.576MHZ-EK
TODO: determine whether I2C port supports address auto-increment (like the SAA7182A does)
SCL
SDA
+3V3A
+3V3
U1
TODO: does XTRI need connecting? (I think no, because "enable under software control" per datasheet)
Expansion port unused in this design.
XTOUT
XTRI
XCLK
XDQ
XRDY
XRV
XRH
XPD7
XPD6
XPD5
XPD4
XPD3
XPD2
XPD1
XPD0
AI24
AI23
AI22
AI21
AI12
AI11
AI2D
AI1D
TODO: ensure I haven't accidentally switched AI12 and AI21
C_IND
Y_IND
CVBS_2_IND
CVBS_1_IND
R1
R2
R3
R4
18
C6
C7
C8
C9
C10
C11
47n
R5
R6
R7
R8
56
HPD7
HPD6
HPD5
HPD4
HPD3
HPD2
HPD1
HPD0
Host port carries UV chroma info in 16-bit I/O mode
HPD[7..0]
IPD7
IPD6
IPD5
IPD4
IPD3
IPD2
IPD1
IPD0
Image port carries Y luma info in 16-bit I/O mode
IPD[7..0]
ITRDY
NOTE: ITRDY contains internal pullup
ICLK
IDQ
ITRI
IGP0
IGP1
IGPV
IGPH
TODO: does ITRI need connecting? (I think no, because "enable under software control" per datasheet)
AMCLK
ASCLK
ALRCLK
AMXCLK
R10
3K3
NOTE: do not populate, SAA7114H contains internal pulldown
TODO: does AMXCLK need grounding?
SAA7114H
CE
VDEC_RST
C14
100n
R9
3K3
NOTE: POR circuit added for CE
NOTE: major differences from Marcus's circuit and this one include:
1. Marcus used 22R for each of the inputs, I used 18R per datasheet;
** 2. Marcus connected his S-VIDEO signal to AI12 and AI22, I connected mine to AI21 and AI22, I'll need to double-check the datasheet on this, it might be an error
3. Marcus had an AGND and DGND, this board only has a single (non-split) GND; and
4. This circuit does not populate the ALRCLK pull-down to GND, as there is already an internal pulldown per datasheet.
PWR_FLAG
L1
10uH
C1
22u
25V
C2
C3
C4
100n
NOTE: added decoupling cap for VDD(XTAL)
C5
C12
C13
C15
C16
C17
C18
C19
C20
C21
C59
Sheet: /Video Decoder/
File: decoder.kicad_sch
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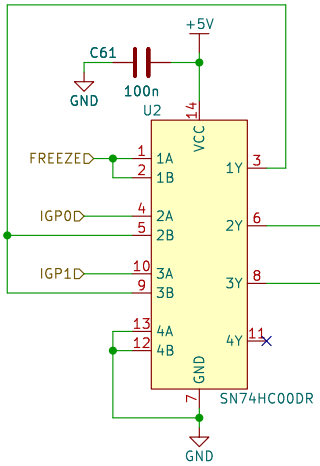
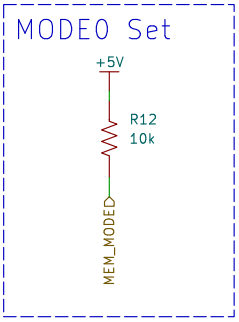
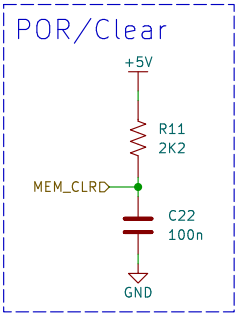
NOTES:
1. I believe Marcus's schematic has $\overline{RRS}$ and $\overline{WRS}$ transposed, and $\overline{RLRS}$ and $\overline{WLRS}$ transposed. I have made the corrections in this design;
2. Marcus doesn't perform the correct power-up sequence identified on pg. 17 on the datasheet. I'm not sure whether I'll actually implement it either, but I have connected the MODE0, $\overline{WCLR}$ and $\overline{RCLR}$ pins to the microcontroller so I can be done if the power-up reset circuit doesn't work as expected.

NOTE:
- when IGP0 is high, $\overline{WE}$ asserted on memories 2 and 4
- when IGP1 is high, $\overline{WE}$ asserted on memories 1 and 3
- when Q1 is high, $\overline{OE}$ asserted on memories 2 and 4
- when Q2 is high, $\overline{OE}$ asserted on memories 1 and 3







Sheet: /Frame Memories and Freeze/		
File: memory.kicad_sch		
Title: Time Base Corrector and Video Scaler		
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NOTES: this circuit differs from Marcus's in the following areas:
1. added the second 75R resistor for each output, similar to the datasheet. This might be an error in Marcus's schematic;
2. added a ferrite and capacitor (LC) to create the analog supply. Marcus's design is not clear on how the separate 3V3A and 3V3D supplies are created, so I used my own judgement on it ;-) ;
3. for the oscillator cicuit, I made a decision to go with a different design, similar to that used for the STM32 microcontroller. Left the pads for the inductor and 1nF capacitor but they are DNP, so that I can revert to Marcus's design same as datasheet) if need be;
4. connected a microcontroller open-drain GPIO to Marcus's POR circuit connecting to the RESET pin.
5. this circuit does not split GND (no separate AGND and DGND);
** 6. I believe RCV1 and RCV2 are reversed on Marcus's schematic, or potentially D and CLK on the LS74 are reversed.
Datasheet states RCV1 contains ON/EVEN, which I think should be the data we want to latch up.

TODO: Unsure on level matching for the LS74, check RCV1 and RCV2 specs and make sure they are ok to drive the flip-flop input and clock.

TODO: determine if RTCI should be connected to ground

+3V3 Analog LC Filter for Encoder

Refer NOTES (item 4) above

Sheet:	/Video Encoder/
File:	encoder.kicad_sch
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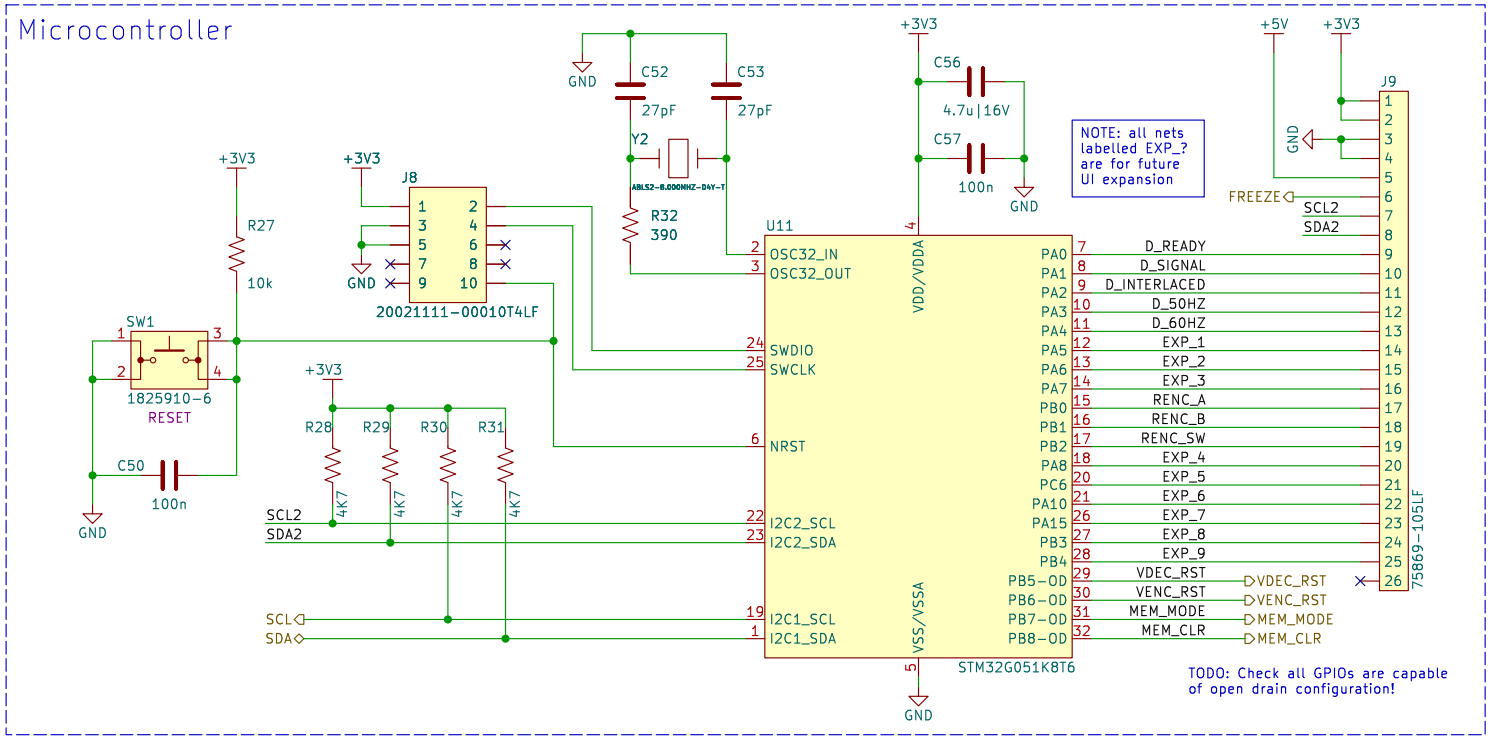

Sheet: /Microcontroller, Power/
File: micro_power.kicad_sch

Title: Time Base Corrector and Video Scaler

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