# Portfolio 3-Boolean Notation for Logic Gates

# Fill in this worksheet and you must upload your worksheet to email [‘a.eleyan@mmu.ac.uk’](mailto:‘a.eleyan@mmu.ac.uk’) by Friday 10th September 10 pm.

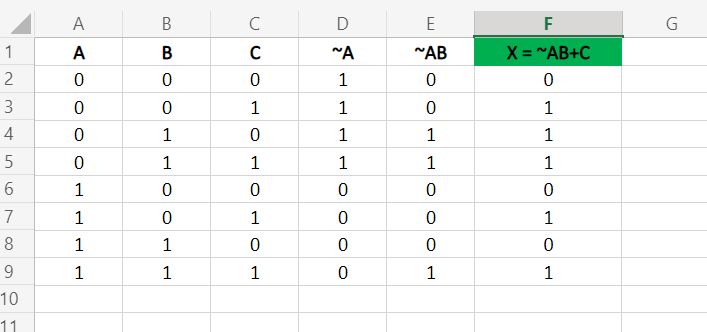
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| --- | --- | --- | --- |
| Name: | PHIL ODONNELL |  |  |

**Boolean Notation**

1. **Give the Boolean expressions and the truth table for the circuits shown below.**

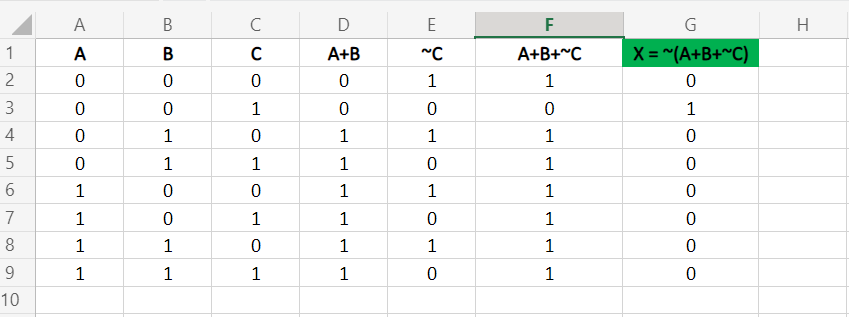
1-1.





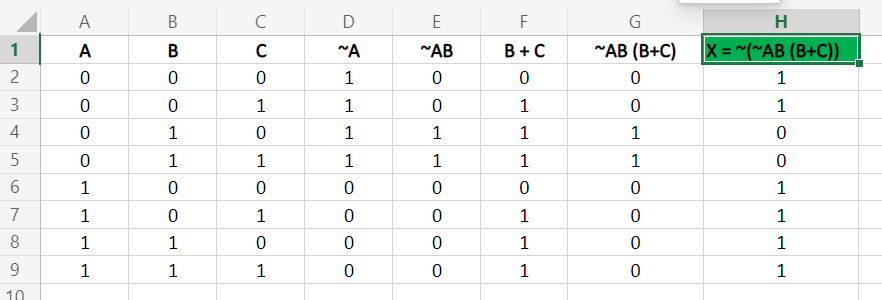
1-2.





1-3.

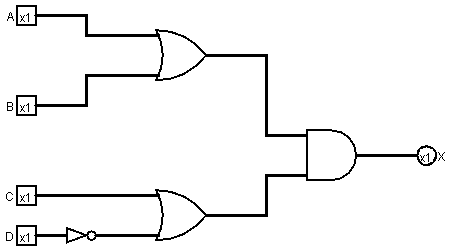




1. In Logisim draw circuit diagrams for the following expressions.

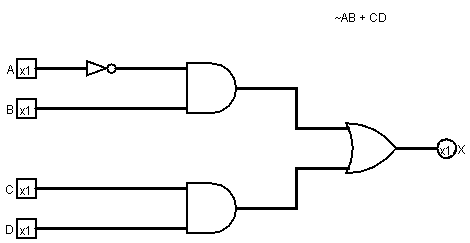
*1.* 

[20 Marks]



1. 

[20 Marks]



Use the “File > Export Image” function in Logisim to save your circuit designs as an image and insert them into the blank page at the end of this document before submitting your work.