Proforma

Description:

Companies open to your department

Company : Intel
Company Name : Intel
Nature Of Business : Core

Designation : Hardware Engineer
Tentative Job Location : Bangalore/ Hyderabad

Hardware Engineer (SoC / IP) JD:

We have roles in Digital and Analog domain

 $\ddot{\text{\i}}, \dot{\text{O}}$ Oversees definition, design, verification, and documentation for SoC (System on a Chip)

development.

- ï, Determines architecture design, logic design, and system simulation.
- i, Defines module interfaces/formats for simulation.
- i, Performs Logic design for integration of cell libraries, functional units and sub-systems

into SoC full chip designs. Register Transfer Level coding, and simulation for SoCs.

 $\ddot{\textbf{i}}, \cdot$ Contributes to the development of multidimensional designs involving the layout of

complex integrated circuits.

 $\ddot{\textbf{i}}, \cdot$ Performs all aspects of the SoC design flow from high-level design to synthesis, place and

route, timing and power to create a design database that is ready for manufacturing.

 $\ddot{\textbf{i}}, \cdot$ Analyzes equipment to establish operation infrastructure, conducts experimental tests,

and evaluates results.

- ï, May also review vendor capability to support development.
- i, He/She should be willing to ramp-up quickly on required areas like RTL, Verification/Validation, Structural Design / Physical Design, Analog, Firmware, Embedded

etc.

Department BT BS MT DoubleMajor dual dualB dualC Mdes MBA Phd MSc MSR

AE	N	-	N	N	N	N	N	-	-	N	-	N
BSBE	N	-	N	N	N	N	N	-	-	N	-	N
CE	N	-	N	N	N	N	N	-	-	N	-	N
CHE	N	-	N	N	N	N	N	-	-	N	-	N
CSE	Y	-	Y	Y	Y	Y	Y	-	-	N	-	Y
EE	Y	-	Y	Y	Y	Y	Y	-	-	N	-	Y
ES	-	N	N	-	N	-	N	-	-	N	-	-
ME	N	-	N	N	N	N	N	-	-	N	-	N
MSE	N	-	N	N	N	N	N	-	-	N	-	N
PHY	-	N	-	N	N	N	N	-	-	N	N	-
CHM	-	N	-	N	N	N	N	-	-	N	N	-
MTH	-	N	-	N	N	N	N	-	-	N	N	-
ECO	-	N	-	N	N	N	N	-	-	N	-	-
DES	-	-	-	-	-	-	N	N	-	N	-	-
IME	-	-	N	-	-	N	N	-	N	N	-	-
CGS	-	-	-	-	-	-	-	-	-	N	-	N
HSS	-	-	-	-	-	-	-	-	-	N	-	-
EEM	-	-	N	-	-	N	-	-	-	N	-	-
MSP	-	-	N	-	-	-	-	-	-	N	-	-
NET	-	-	N	-	-	N	-	-	-	N	-	-
PSE	-	-	Y	-	-	N	-	-	-	N	-	Y
Stats	-	-	-	-	-	-	-	-	-	N	N	-

Eligibilty:

	IITs	
CG Hirig 2020	Btech	Mtech

Cost to Company:

Package Details :

Base	8.55	10.91
Base + Bonus + Retirals + SPP	10.05	12.91
Special Allowance	0.22	0.22
HB (in 2 installments)	3.5	4.5
Relocation (tax protected)	1	1
Other Benefits (Insurance premiums +Transportation)	1.22	1.22
Total CTC	15.99	19.85

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Bond :

False

Medical Requirements :

Resume Shortlist : True

Resume Shortlist Criteria: N/A
Aptitude Test: False
Group Discussion: False
Technical Test: True

Technical Test Duration: 90 mins
Technical Interview: True
Technical Interview Duration: 45

 $Number\ of\ Techincal\ Interview$

Rounds:

2

HR Interview: True HR Interview Duration: 30