Proforma

Companies open to your department

Company :	Marvell Semiconductors
Company Name :	Marvell Semiconductors
Nature Of Business :	R & D
Designation :	Design Engineer
Tentative Job Location :	Bangalore

Hardware JD:

Responsibilities:

As member of theÂ Marvell team,

- You willÂ be involved in the area of Logic Design/Integration, Functional Verification, DesignÂ forÂ Test (DFT), Analog design & Layout, Physical Implementation, Low Power & SignoffÂ for processor systems, ASICs or IPs.
- Opportunity to workÂ forÂ complete SoCÂ design cycle,Â starting fromÂ ArchitectureÂ definition and logic design, feasibility planning/benchmarking for Power/Performance/Area/YieldÂ to end-to-endÂ Design/Implementation/Signoff
- Opportunity to work on challenging design architecture across Networking, Processor,Â Computing,Â Automotive, Switching, Connectivity and Security, in the technology nodes across 5nm/7nm/12nm/14nm and more.

- You will work closely with different functional teams in Marvell and enable successful products for the next generation technology.
- Opportunity to work in multi core ARM sub-system architecture,Â high speed interface designs using Serdes, PCI-e, DDR4, low power design architecture and design/manufacturing for high quality/reliability.
- **Requirements:**

- BE/BTech or ME/MTech in EE/EC/VLSI/InstrumentationÂ with 0-1 years of experience.
- Exposure on Design,Â Verification,Â Test,Â Physical implementation,Â Layout andÂ Semiconductor device/process through previous work/intern experience or course work.
- Experience inÂ one or more of below topics,Â through course work or internshipÂ experience:
- Coding language likeÂ SystemVerilog, Verilog, C/C++ or Assembly language in Test bench development in any of the languages,
- Verification methodology like UVM or VMM or OVM,

- Design for Test and SimulationsÂ using EDA tools,
- Physical design/Implementation using EDA tools,
- Synthesis/STAÂ TimingÂ using EDA tools,
- Low Power Design/Optimization and Reliability signoff using EDA tools,
- Understanding of the fundamentals of circuit design
- Strong intuitive and analytical understanding of transistor-level circuit and layout design
- Should have good knowledge of CMOS process and fabrication
- Custom layout andÂ Physical verificationÂ using EDA tools,

- Scripting/programming usingÂ Tcl/Tk/Perl/Python/Shell
- Detail oriented, self-motivated team worker, good verbal and written communication skills
- Strong Digital Design conceptsÂ and debugging skills

Marvell gives Equal Opportunity Employer and considers applicants for all positions without regard to race, color, creed, religion, ancestry, national origin, age, gender identity, sex, marital status, sexual orientation, physical or mental disability, Be sure to include your name, If you are ready to excel, innovate, and truly enjoy where you work, apply now for the position detailed below.

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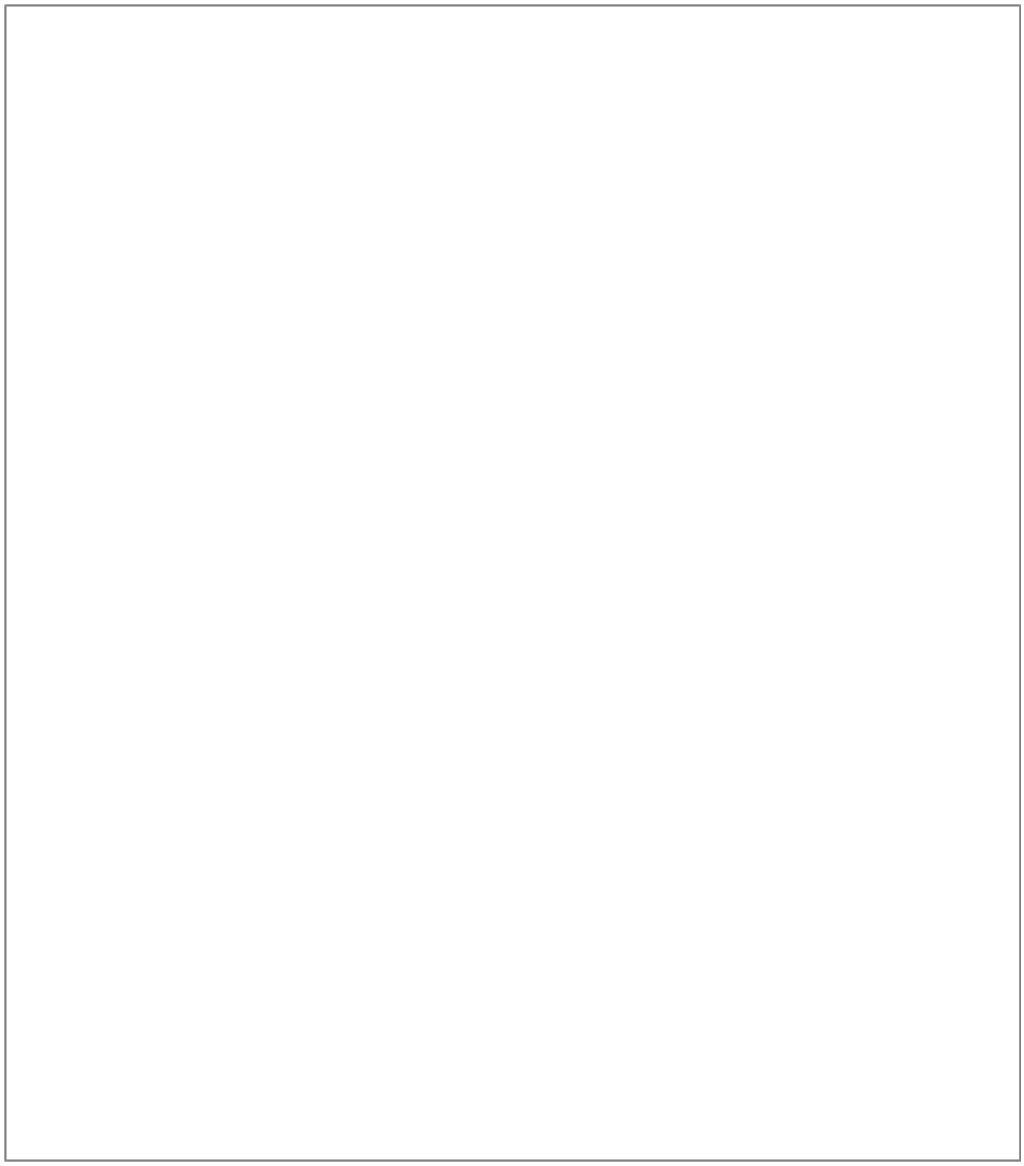

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Eligibilty :

Department	BT	BS	MT	DoubleMajor	dual	dualB	dualC	Mdes	MBA	Phd	MSc	MSR
AE	N	-	N	N	N	N	N	-	-	N	-	N
BSBE	N	-	N	N	N	N	N	-	-	N	-	N
CE	N	-	N	N	N	N	N	-	-	N	-	N
CHE	N	-	N	N	N	N	N	-	-	N	-	N
CSE	N	-	N	N	N	N	N	-	-	N	-	N
EE	N	-	Y	N	Y	Y	Y	-	-	N	-	Y
ES	-	N	N	-	N	-	N	-	-	N	-	-
ME	N	-	N	N	N	N	N	-	-	N	-	N
MSE	N	-	N	N	N	N	N	-	-	N	-	N
PHY	-	N	-	N	N	N	N	-	-	N	N	-
CHM	-	N	-	N	N	N	N	-	-	N	N	-
MTH	-	N	-	N	N	N	N	-	-	N	N	-
ECO	-	N	-	N	N	N	N	-	-	N	-	-
DES	-	-	-	-	-	-	N	N	-	N	-	-
IME	-	-	N	-	-	N	N	-	N	N	-	-
CGS	-	-	-	-	-	-	-	-	-	N	-	N
HSS	-	-	-	-	-	-	-	-	-	N	-	-
EEM	-	-	N	-	-	N	-	-	-	N	-	-
MSP	-	-	N	-	-	-	-	-	-	N	-	-
NET	-	-	N	-	-	N	-	-	-	N	-	-
PSE	-	-	N	-	-	N	-	-	-	N	-	N
Stats	-	-	-	-	-	-	-	-	-	N	N	-

Cost to Company :	CTC - 19.73 LPA
Package Details :	Fixed Salary - 14.09 LPA
Bond :	False
Medical Requirements :	
Resume Shortlist :	True
Resume Shortlist Criteria:	7/10
Aptitude Test:	True
Aptitude Test Duration:	45 Mins
Group Discussion:	False
Technical Test:	True
Technical Test Duration:	45 Mins
Technical Interview:	True
Technical Interview Duration:	60 Mins
Number of Techincal Interview Rounds:	3

HR Interview:	True
HR Interview Duration:	30 Mins