Proforma

Companies open to your department

Company :	GLOBALFOUNDRIES
Company Name :	GLOBALFOUNDRIES
Nature Of Business :	Service Semiconductor Foundry
Designation :	Senior/ Principal Engineer Design Enablement/ Device Modeling:
Tentative Job Location :	Bangalore

Description :

Job Purpose:

To develop FET compact models in Silicon Photonics (SiPh) Semiconductor Technologies for state-of-the-art applications in the growing High Performance, Hyperscale Computing & Wired industries (CWI)

Roles and Responsibilities:

- GLOBALFOUNDRIES is seeking a motivated, self-driven engineer to develop FET compact models which are actively used by clients to design critical CMOS circuits suchs High-Speed IOs and Transimpedance Amplifiers (TIAs) for state-of-the-art monolithic solutions. Familiarity with SOI FET transistor engineering, processing and modeling methodologies, including BSIM and PSP (bulk & SOI), are required to obtain accurate device characteristics suitable for high-frequency applications
- This includes an understanding of how the various model parameters affect the simulation results and how one might extract these parameters from measured data. The role requires a demonstrated background in semiconductor device physics and high-speed circuit design while utilizing automation software for data analysis, parameter extraction & simulation of the device/circuit characteristics.
- Comprehensive knowledge is required of Direct Current (DC), Scattering-parameter, high-frequency measurements for linear and Non-linear characterization, including de-embedding techniques. Experience working with EDA tools, hardware description languages, Electro-Magnetic and integrated circuit simulators are desirable.
- Applicants will be a member of an established technical team, driven by collaborative innovation and creative problem solving. Demonstrated effective communication (written & verbal), analytical thinking, desire to innovate, and people skills are also required

Requirements:

- Master's Degree in Electrical & Electronics, Microelectronics Engineering or Physics; PhD is preferred
- At least 1 years experience in Device/Circuit Design and Compact Modeling; 1+ years is preferred
- English: Proficient.

Eligibilty :

Department	BT	BS	MT	DoubleMajor	dual	dualB	dualC	Mdes	MBA	Phd	MSc	MSR
AE	N	-	N	N	N	N	N	-	-	N	-	N
BSBE	N	-	N	N	N	N	N	-	-	N	-	N
CE	N	-	N	N	N	N	N	-	-	N	-	N
CHE	N	-	N	N	N	N	N	-	-	N	-	N
CSE	N	-	N	N	N	N	N	-	-	N	-	N
EE	N	-	Y	Y	Y	Y	Y	-	-	Y	-	Y
ES	-	N	N	-	N	-	N	-	-	N	-	-
ME	N	-	N	N	N	N	N	-	-	N	-	N
MSE	N	-	Y	N	Y	Y	Y	-	-	Y	-	Y
PHY	-	N	-	N	Y	Y	Y	-	-	Y	Y	-
CHM	-	N	-	N	N	N	N	-	-	N	N	-
MTH	-	N	-	N	N	N	N	-	-	N	N	-
ECO	-	N	-	N	N	N	N	-	-	N	-	-
DES	-	-	-	-	-	-	N	N	-	N	-	-
IME	-	-	N	-	-	N	N	-	N	N	-	-
CGS	-	-	-	-	-	-	-	-	-	N	-	N
HSS	-	-	-	-	-	-	-	-	-	N	-	-
EEM	-	-	N	-	-	N	-	-	-	N	-	-
MSP	-	-	N	-	-	-	-	-	-	N	-	-
NET	-	-	N	-	-	N	-	-	-	N	-	-
PSE	-	-	Y	-	-	Y	-	-	-	Y	-	Y
Stats	-	-	-	-	-	-	-	-	-	N	N	-

Cost to

For **PhDs** - CTC: 2167480 INR

Company :	For **Master's** - CTC: 1288772 INR
Package Details :	Following is the break up for **PhDs** : Base Pay- 1850000, AIP- 185000, Gratuity- 37908, PF- 94572 Following is the break up for **Master's** : Base Pay- 1100000, AIP- 110000, Gratuity- 22540, PF- 56232
Bond :	False
Medical Requirements :	Medical Insurance is provided by the company
Resume Shortlist :	True
Resume Shortlist Criteria:	N/A
Aptitude Test:	False
Group Discussion:	False
Technical Test:	False
Technical Interview:	True
Technical Interview Duration:	N/A
Number of Techincal Interview Rounds:	3
HR Interview:	True
HR Interview Duration:	N/A