VLSI Design Project Report

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2020102037

1. Proposed Structure

2. Topology and Sizing of Blocks

3. Pre-Layout Simulations

3.1 Gates

Gate Testing Code

```
.include ../../TSMC_180nm.txt
.include not.subs
.include and2.subs
.include and3.subs
.include and4.subs
.include and5.subs
.include or2.subs
.include or3.subs
.include or4.subs
.include or5.subs
.include xor2.subs

** Parameters **
.param VSupply=1.8
.param LAMBDA=0.09u
.param width_N=10*LAMBDA
.param width_P=20*LAMBDA
.global vdd gnd

** Input Voltages **
VS vdd gnd VSupply
* V1 in1 gnd pulse VSupply 0 0 100p 100p 10n 20n
* V2 in2 gnd pulse VSupply 0 0 100p 100p 20n 40n
* V3 in3 gnd pulse VSupply 0 0 100p 100p 40n 80n
* V4 in4 gnd pulse VSupply 0 0 100p 100p 80n 160n
* V5 in5 gnd pulse VSupply 0 0 100p 100p 160n 320n

** Circuit Description **
* xnot1 out in1 not
* xand2 out in1 in2 and2
* xand3 out in1 in2 in3 and3
* xand4 out in1 in2 in3 in4 and4
* xand5 out in1 in2 in3 in4 in5 and5
* xor2  out in1 in2 or2
* xor3  out in1 in2 in3 or3
* xor4  out in1 in2 in3 in4 or4
* xor5  out in1 in2 in3 in4 in5 or5
```

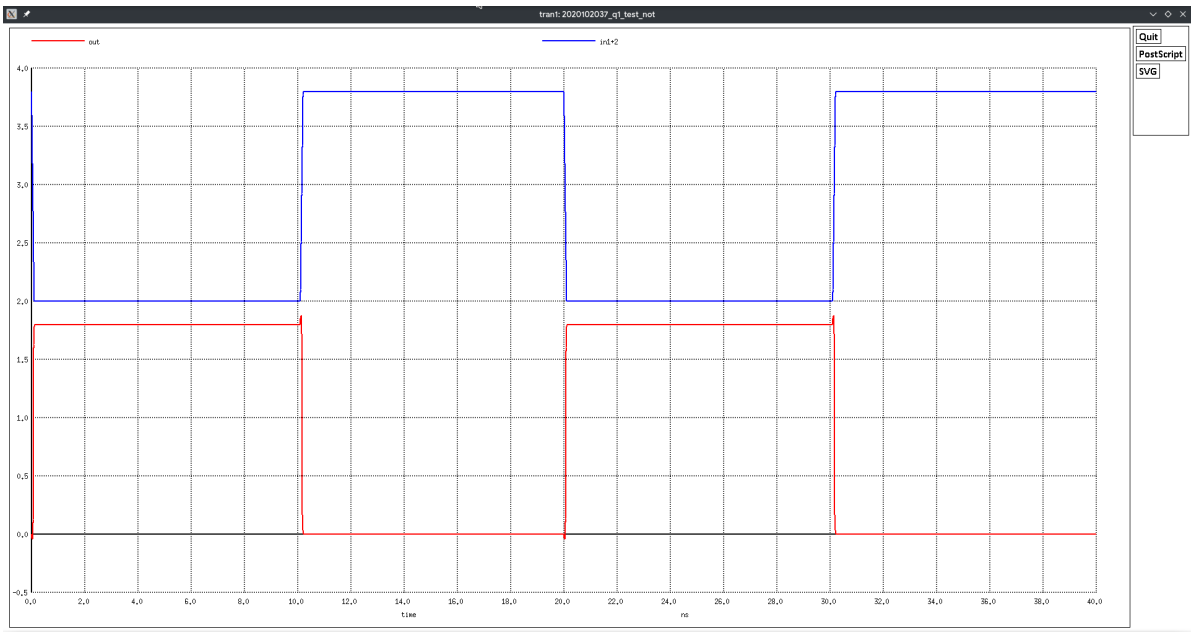
```
* xxor2 out in1 in2 xor2

** Analysis **
* .tran 1p 40n
* .tran 1p 80n
* .tran 1p 160n
* .tran 1p 320n

** Plotting **
.control
set hcopypscolor=1
set color0=white
set color1=black
run
set curplottitle="2020102037_Q1_Test_Gates"
* plot out in1+2
* plot out in1+2 in2+4
* plot out in1+2 in2+4 in3+6
* plot out in1+2 in2+4 in3+6 in4+8
* plot out in1+2 in2+4 in3+6 in4+8 in5+10
.endc

.end
```

3.1.1 NOT Gate

3.1.1.1 Netlist

```
* NOT Gate

.subckt not out in1
MN0 out in1 gnd gnd CMOSN W=width_N L={2*LAMBDA}
MP0 out in1 vdd vdd CMOSP W=width_P L={2*LAMBDA}
.ends
```

3.1.1.2 Simulations Results

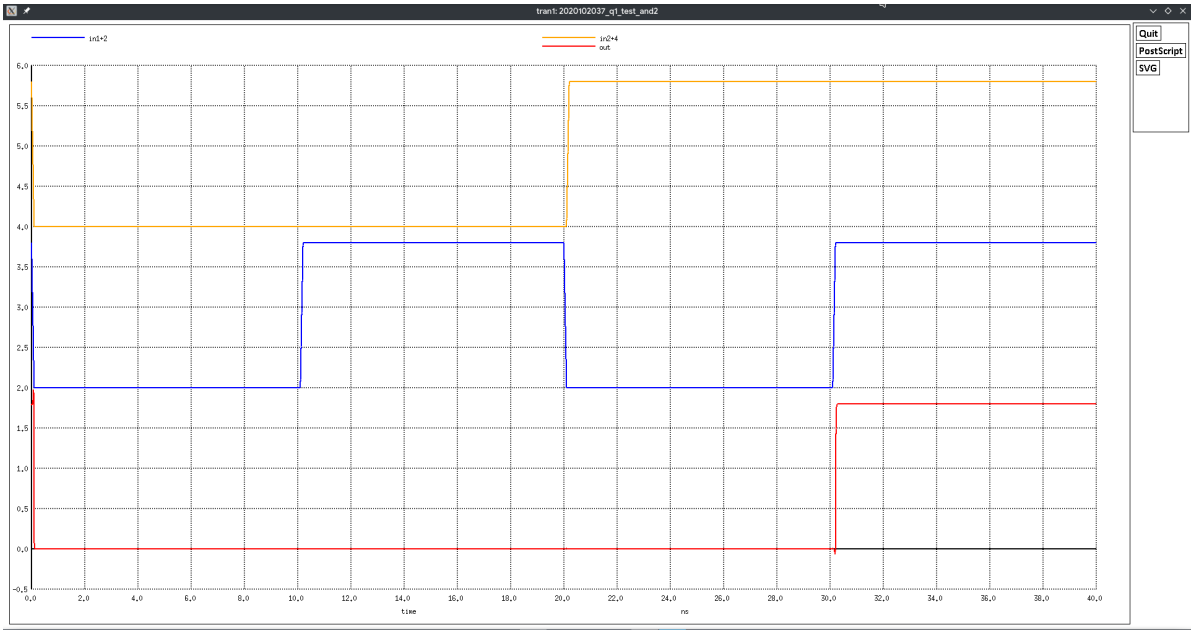


3.1.2 2-Input AND Gate

3.1.2.1 Netlist

```
* 2-Input AND Gate

.subckt and2 out in1 in2
* 2-Input NAND Gate
MN1 n01 in1 n02 n02 CMOSN W=width_N L={2*LAMBDA}
MN2 n02 in2 gnd gnd CMOSN W=width_N L={2*LAMBDA}
MP1 n01 in1 vdd vdd CMOSP W=width_P L={2*LAMBDA}
MP2 n01 in2 vdd vdd CMOSP W=width_P L={2*LAMBDA}

* NOT Gate
MN3 out n01 gnd gnd CMOSN W=width_N L={2*LAMBDA}
MP3 out n01 vdd vdd CMOSP W=width_P L={2*LAMBDA}
.ends
```

3.1.2.2 Simulations Results

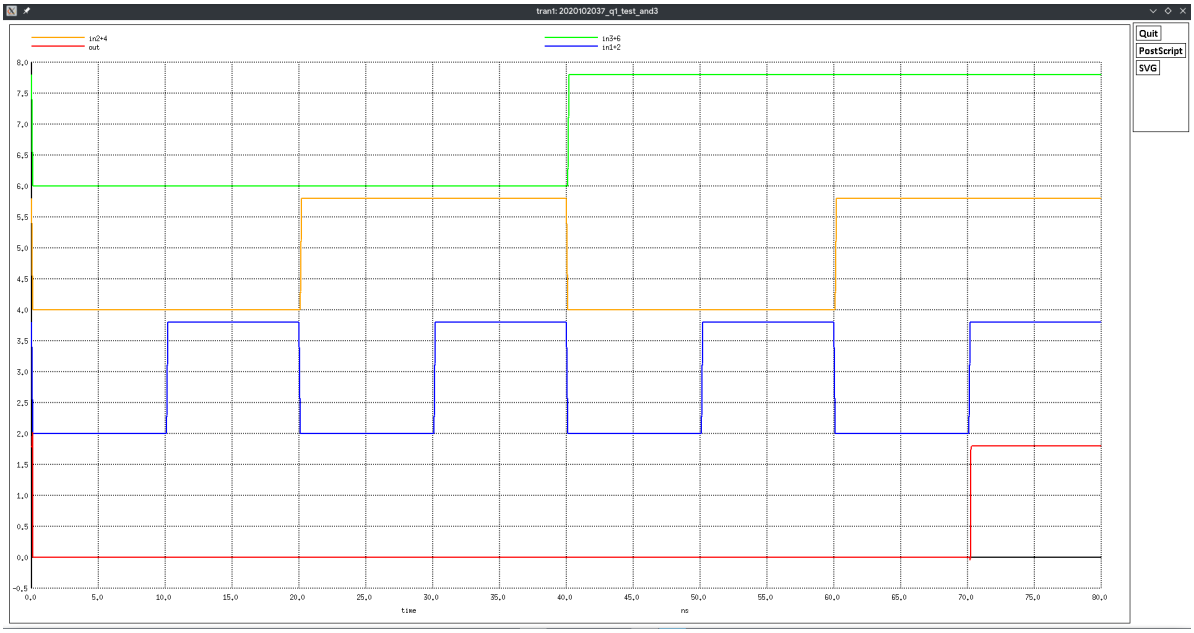


3.1.3 2-Input AND Gate

3.1.3.1 Netlist

```
* 3-Input AND Gate

.subckt and3 out in1 in2 in3
* 3-Input NAND Gate
MN1 n01 in1 n02 n02 CMOSN W=width_N L={2*LAMBDA}
MN2 n02 in2 n03 n03 CMOSN W=width_N L={2*LAMBDA}
MN3 n03 in3 gnd gnd CMOSN W=width_N L={2*LAMBDA}
MP1 n01 in1 vdd vdd CMOSP W=width_P L={2*LAMBDA}
MP2 n01 in2 vdd vdd CMOSP W=width_P L={2*LAMBDA}
MP3 n01 in3 vdd vdd CMOSP W=width_P L={2*LAMBDA}

* NOT Gate
MN4 out n01 gnd gnd CMOSN W=width_N L={2*LAMBDA}
MP4 out n01 vdd vdd CMOSP W=width_P L={2*LAMBDA}
.ends
```

3.1.3.2 Simulations Results

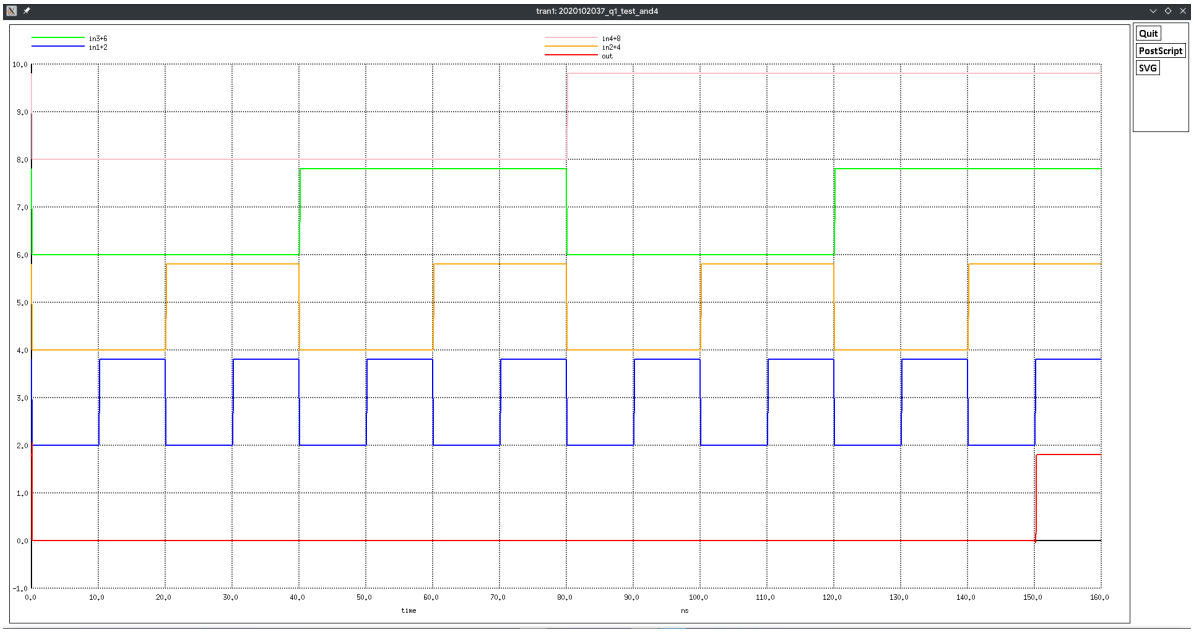


3.1.4 4-Input AND Gate

3.1.4.1 Netlist

```
* 4-Input AND Gate

.subckt and4 out in1 in2 in3 in4
* 4-Input NAND Gate
MN1 n01 in1 n02 n02 CMOSN W=width_N L={2*LAMBDA}
MN2 n02 in2 n03 n03 CMOSN W=width_N L={2*LAMBDA}
MN3 n03 in3 n04 n04 CMOSN W=width_N L={2*LAMBDA}
MN4 n04 in4 gnd gnd CMOSN W=width_N L={2*LAMBDA}
MP1 n01 in1 vdd vdd CMOSP W=width_P L={2*LAMBDA}
MP2 n01 in2 vdd vdd CMOSP W=width_P L={2*LAMBDA}
MP3 n01 in3 vdd vdd CMOSP W=width_P L={2*LAMBDA}
MP4 n01 in4 vdd vdd CMOSP W=width_P L={2*LAMBDA}

* NOT Gate
MN5 out n01 gnd gnd CMOSN W=width_N L={2*LAMBDA}
MP5 out n01 vdd vdd CMOSP W=width_P L={2*LAMBDA}
.ends
```

3.1.4.2 Simulation Results

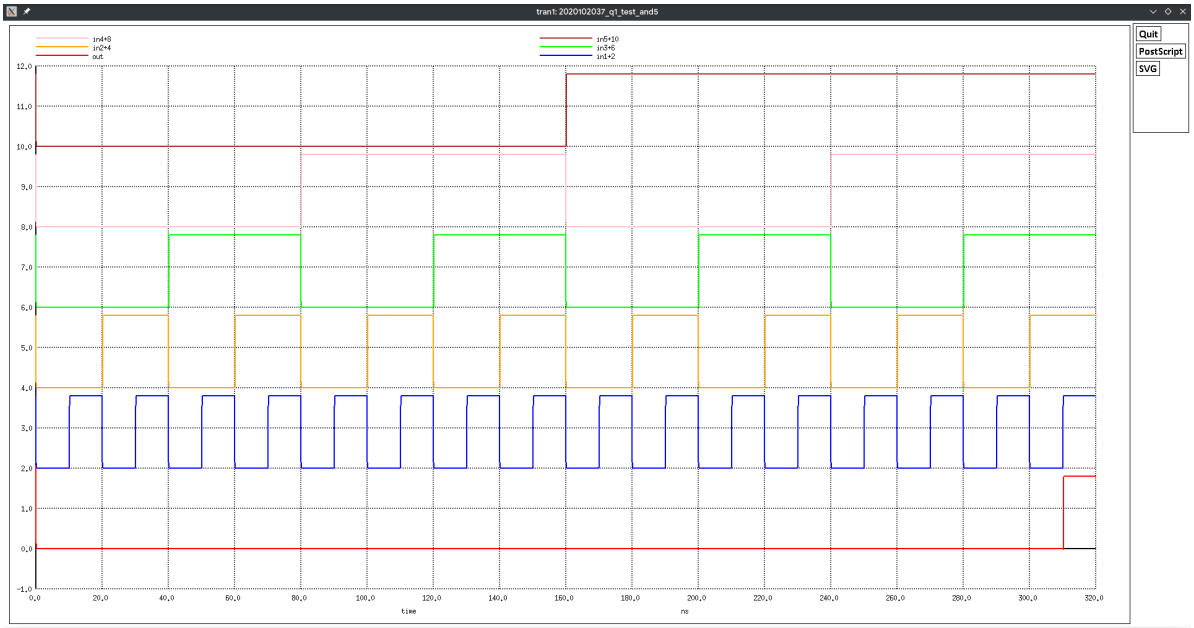


3.1.5 5-Input AND Gate

3.1.5.1 Netlist

```
* 5-Input AND Gate

.subckt and5 out in1 in2 in3 in4 in5
* 5-Input NAND Gate
MN1 n01 in1 n02 n02 CMOSN W=width_N L={2*LAMBDA}
MN2 n02 in2 n03 n03 CMOSN W=width_N L={2*LAMBDA}
MN3 n03 in3 n04 n04 CMOSN W=width_N L={2*LAMBDA}
MN4 n04 in4 n05 n05 CMOSN W=width_N L={2*LAMBDA}
MN5 n05 in4 gnd gnd CMOSN W=width_N L={2*LAMBDA}
MP1 n01 in1 vdd vdd CMOSP W=width_P L={2*LAMBDA}
MP2 n01 in2 vdd vdd CMOSP W=width_P L={2*LAMBDA}
MP3 n01 in3 vdd vdd CMOSP W=width_P L={2*LAMBDA}
MP4 n01 in4 vdd vdd CMOSP W=width_P L={2*LAMBDA}
MP5 n01 in5 vdd vdd CMOSP W=width_P L={2*LAMBDA}

* NOT Gate
MN6 out n01 gnd gnd CMOSN W=width_N L={2*LAMBDA}
MP6 out n01 vdd vdd CMOSP W=width_P L={2*LAMBDA}
.ends
```

3.1.5.2 Simulation Results

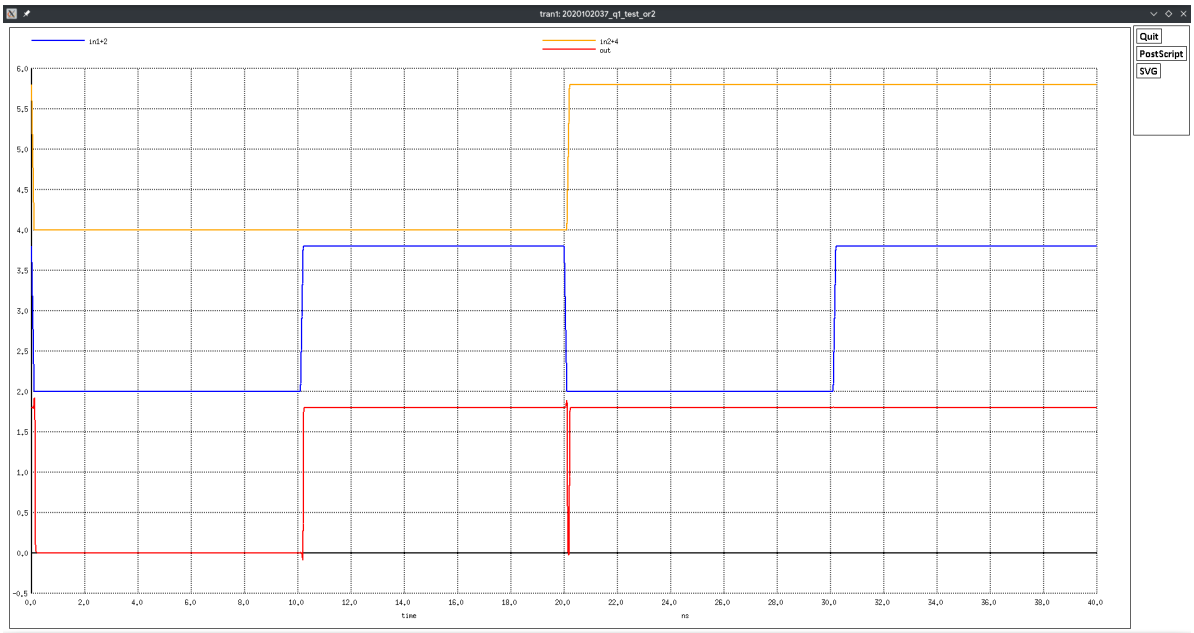


3.1.6 2-Input OR Gate

3.1.6.1 Netlist

```
* 2-Input OR Gate

.subckt or2 out in1 in2
* 2-Input NOR Gate
MN1 n01 in1 gnd gnd CMOSN W=width_N L={2*LAMBDA}
MN2 n01 in2 gnd gnd CMOSN W=width_N L={2*LAMBDA}
MP1 n01 in1 n02 n02 CMOSP W=width_P L={2*LAMBDA}
MP2 n02 in2 vdd vdd CMOSP W=width_P L={2*LAMBDA}

* NOT Gate
MN3 out n01 gnd gnd CMOSN W=width_N L={2*LAMBDA}
MP3 out n01 vdd vdd CMOSP W=width_P L={2*LAMBDA}
.ends
```

3.1.6.2 Simulation Results

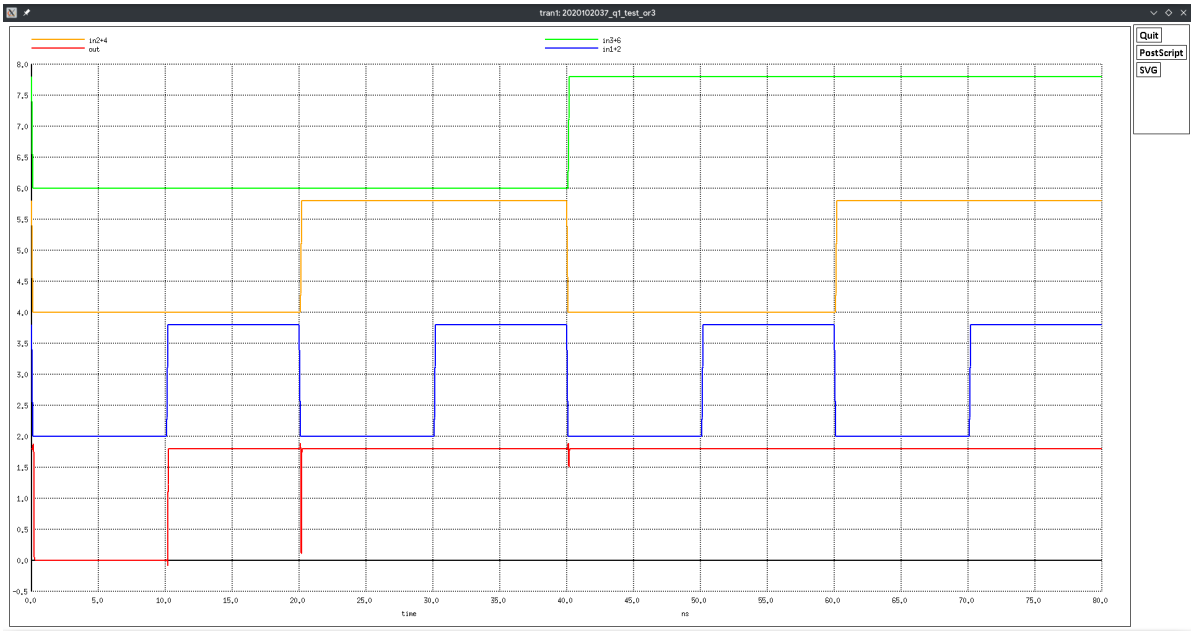


3.1.7 3-Input OR Gate

3.1.7.1 Netlist

```
* 3-Input OR Gate

.subckt or3 out in1 in2 in3
* 3-Input NOR Gate
MN1 n01 in1 gnd gnd CMOSN W=width_N L={2*LAMBDA}
MN2 n01 in2 gnd gnd CMOSN W=width_N L={2*LAMBDA}
MN3 n01 in3 gnd gnd CMOSN W=width_N L={2*LAMBDA}
MP1 n01 in1 n02 n02 CMOSP W=width_P L={2*LAMBDA}
MP2 n02 in2 n03 n03 CMOSP W=width_P L={2*LAMBDA}
MP3 n03 in3 vdd vdd CMOSP W=width_P L={2*LAMBDA}

* NOT Gate
MN4 out n01 gnd gnd CMOSN W=width_N L={2*LAMBDA}
MP4 out n01 vdd vdd CMOSP W=width_P L={2*LAMBDA}
.ends
```

3.1.7.2 Simulation Results



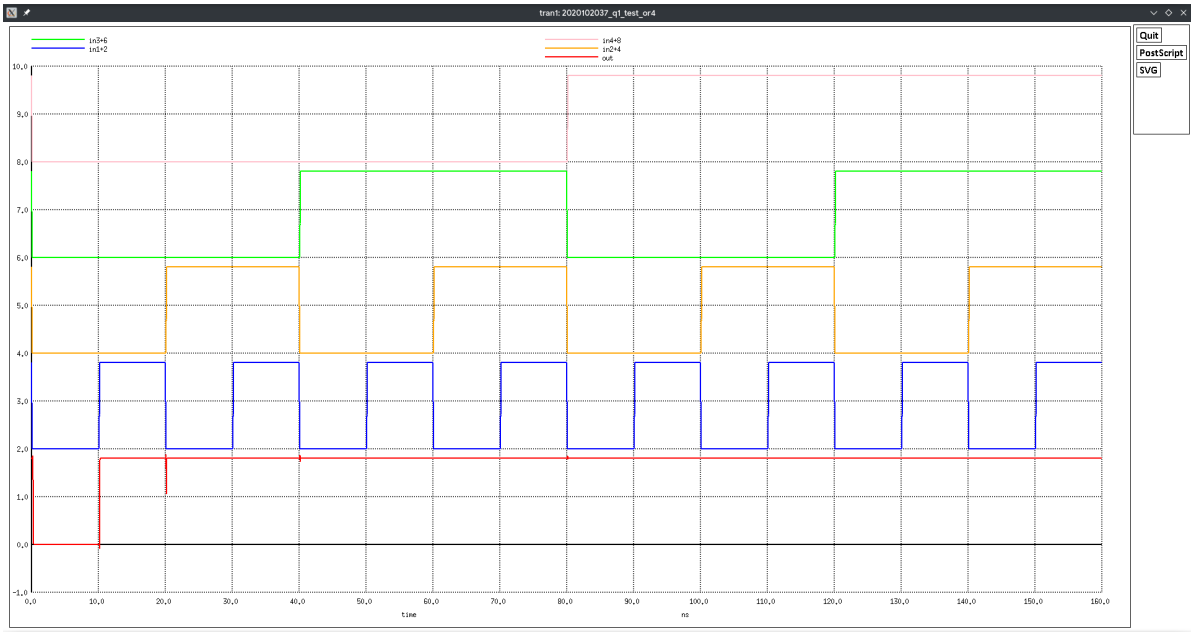
3.1.8 4-Input OR Gate

3.1.8.1 Netlist

```
* 4-Input OR Gate

.subckt or4 out in1 in2 in3 in4
* 4-Input NOR Gate
MN1 n01 in1 gnd gnd CMOSN W=width_N L={2*LAMBDA}
MN2 n01 in2 gnd gnd CMOSN W=width_N L={2*LAMBDA}
MN3 n01 in3 gnd gnd CMOSN W=width_N L={2*LAMBDA}
MN4 n01 in4 gnd gnd CMOSN W=width_N L={2*LAMBDA}
MP1 n01 in1 n02 n02 CMOSP W=width_P L={2*LAMBDA}
MP2 n02 in2 n03 n03 CMOSP W=width_P L={2*LAMBDA}
MP3 n03 in3 n04 n04 CMOSP W=width_P L={2*LAMBDA}
MP4 n04 in4 vdd vdd CMOSP W=width_P L={2*LAMBDA}
```

```
* NOT Gate
MN5 out n01 gnd gnd CMOSN W=width_N L={2*LAMBDA}
MP5 out n01 vdd vdd CMOSP W=width_P L={2*LAMBDA}
.ends
```

3.1.8.2 Simulation Results

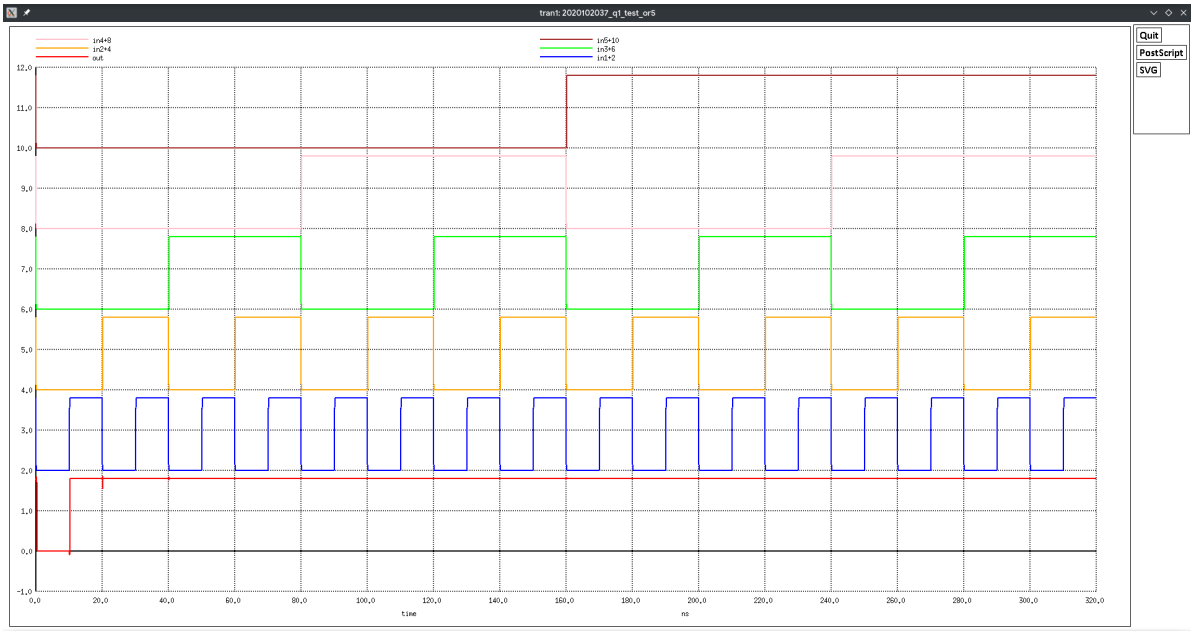


3.1.9 5-Input OR Gate

3.1.9.1 Netlist

```
* 5-Input OR Gate

.subckt or5 out in1 in2 in3 in4 in5
* 5-Input NOR Gate
MN1 n01 in1 gnd gnd CMOSN W=width_N L={2*LAMBDA}
MN2 n01 in2 gnd gnd CMOSN W=width_N L={2*LAMBDA}
MN3 n01 in3 gnd gnd CMOSN W=width_N L={2*LAMBDA}
MN4 n01 in4 gnd gnd CMOSN W=width_N L={2*LAMBDA}
MN5 n01 in5 gnd gnd CMOSN W=width_N L={2*LAMBDA}
MP1 n01 in1 n02 n02 CMOSP W=width_P L={2*LAMBDA}
MP2 n02 in2 n03 n03 CMOSP W=width_P L={2*LAMBDA}
MP3 n03 in3 n04 n04 CMOSP W=width_P L={2*LAMBDA}
MP4 n04 in4 n05 n05 CMOSP W=width_P L={2*LAMBDA}
MP5 n05 in5 vdd vdd CMOSP W=width_P L={2*LAMBDA}

* NOT Gate
MN6 out n01 gnd gnd CMOSN W=width_N L={2*LAMBDA}
MP6 out n01 vdd vdd CMOSP W=width_P L={2*LAMBDA}
.ends
```

3.1.9.2 Simulation Results

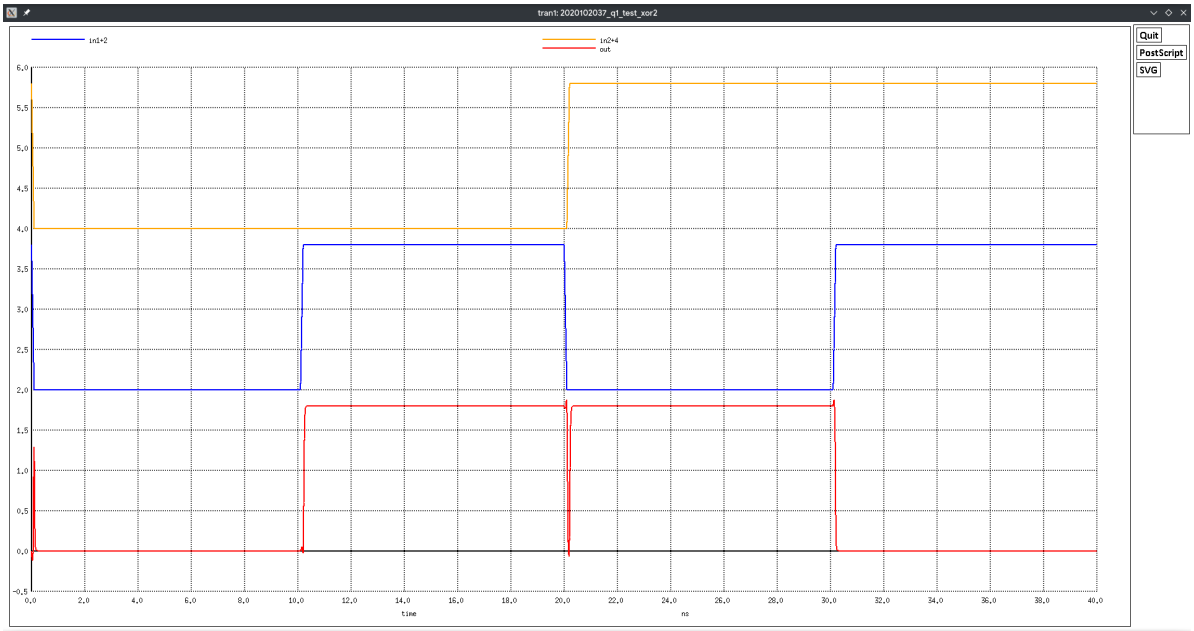


3.1.10 2-Input XOR Gate

3.1.10.1 Netlist

```
* 2-Input XOR Gate

.subckt not out in1
MN1 out in1 gnd gnd CMOSN W=width_N L={2*LAMBDA}
MP1 out in1 vdd vdd CMOSP W=width_P L={2*LAMBDA}
.ends

.subckt twopmos n01 n02 in1 in2
MP1 n03 in1 n01 n01 CMOSP W=width_P L={2*LAMBDA}
MP2 n02 in2 n03 n03 CMOSP W=width_P L={2*LAMBDA}
.ends

.subckt twonmos n01 n02 in1 in2
MP1 n01 in1 n03 n03 CMOSN W=width_N L={2*LAMBDA}
MP2 n03 in2 n02 n02 CMOSN W=width_N L={2*LAMBDA}
.ends

.subckt xor2 out in1 in2
xnot1 nn1 in1 not
xnot2 nn2 in2 not
xtwopmos1 vdd out nn1 in2 twopmos
xtwopmos2 vdd out in1 nn2 twopmos
xtwonmos1 out gnd in1 in2 twonmos
xtwonmos2 out gnd nn1 nn2 twonmos
.ends
```

3.1.10.2 Simulation Results



3.2 Blocks

Block Testing Code

```
.include ../../TSMC_180nm.txt
.include ../Gates/and2.subs
.include ../Gates/and3.subs
.include ../Gates/and4.subs
.include ../Gates/and5.subs
.include ../Gates/or2.subs
.include ../Gates/or3.subs
.include ../Gates/or4.subs
.include ../Gates/or5.subs
.include ../Gates/xor2.subs
.include ../Blocks/propogate-generate.subs
.include ../Blocks/carry-lookahead.subs
.include ../Blocks/sum.subs
.include carry-lookahead-adder.subs

** Parameters **
.param VSupply=1.8
.param LAMBDA=0.09u
.param width_N=10*LAMBDA
.param width_P=20*LAMBDA
.global vdd gnd

** Input Voltages **
VS vdd gnd VSupply

.param HIGH=VSupply
.param LOW=0

* A = a3 a2 a1 a0
VA0 a0 gnd pulse LOW  HIGH 0 100p 100p 40n 80n
VA1 a1 gnd pulse HIGH LOW  0 100p 100p 10n 20n
VA2 a2 gnd pulse HIGH LOW  0 100p 100p 20n 40n
VA3 a3 gnd pulse LOW  HIGH 0 100p 100p 20n 40n

* B = b3 b2 b1 b0
```

```
VB0 b0 gnd pulse HIGH LOW  0 100p 100p 40n 80n
VB1 b1 gnd pulse LOW  HIGH 0 100p 100p 20n 40n
VB2 b2 gnd pulse LOW  HIGH 0 100p 100p 10n 20n
VB3 b3 gnd pulse HIGH LOW  0 100p 100p 10n 20n

* Carry-In = c0
VC0 c0 gnd pulse HIGH LOW  0 100p 100p 20n 40n

** Circuit Description **
* SUM = c4 s3 s2 s1 s0
xpgblock p0 p1 p2 p3 g0 g1 g2 g3 a0 a1 a2 a3 b0 b1 b2 b3 pgblock
xclblock c1 c2 c3 c4 p0 p1 p2 p3 g0 g1 g2 g3 c0 clblock
xsumblock s0 s1 s2 s3 p0 p1 p2 p3 c0 c1 c2 c3 sumblock

** Analysis **
.tran 1p 80n

** Plotting **
.control
set hcopypscolor=1
set color0=white
set color1=black
run
set curplottitle="2020102037_Q3_BlockTest"
plot a0 a1+2 a2+4 a3+6
plot b0 b1+2 b2+4 b3+6
plot p0 p1+2 p2+4 p3+6
plot g0 g1+2 g2+4 g3+6
plot c1 c2+2 c3+4 c4+6
plot s0 s1+2 s2+4 s3+6 c4+8
.endc

.end
```

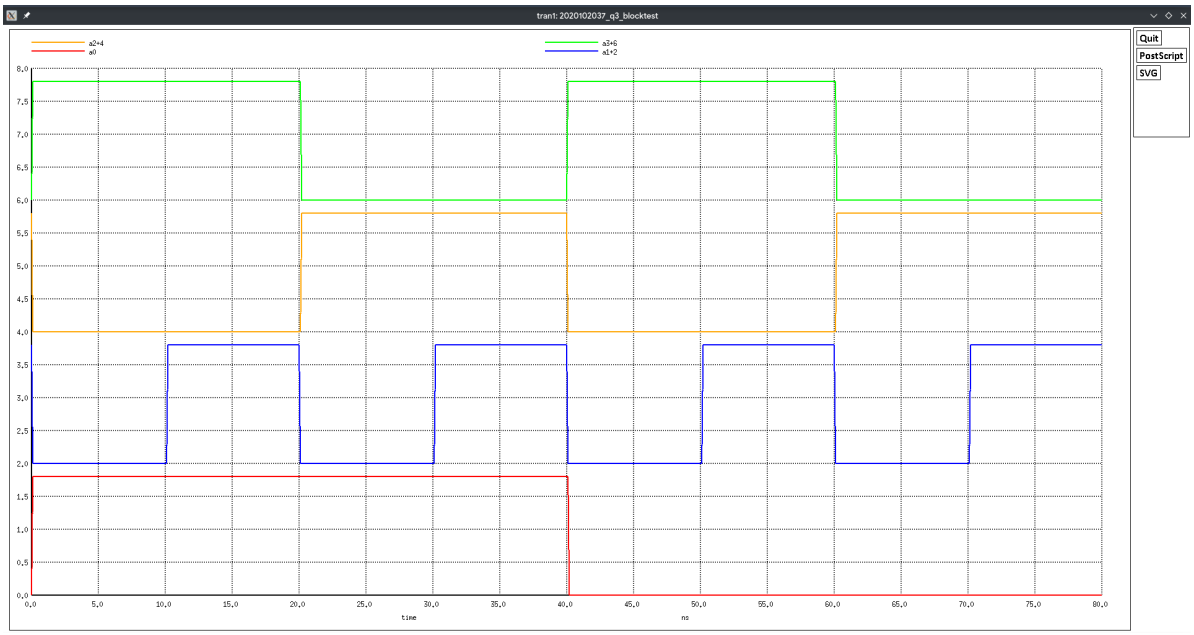
3.2.1 Carry Propogate and Carry Generate Block

3.2.1.1 Netlist

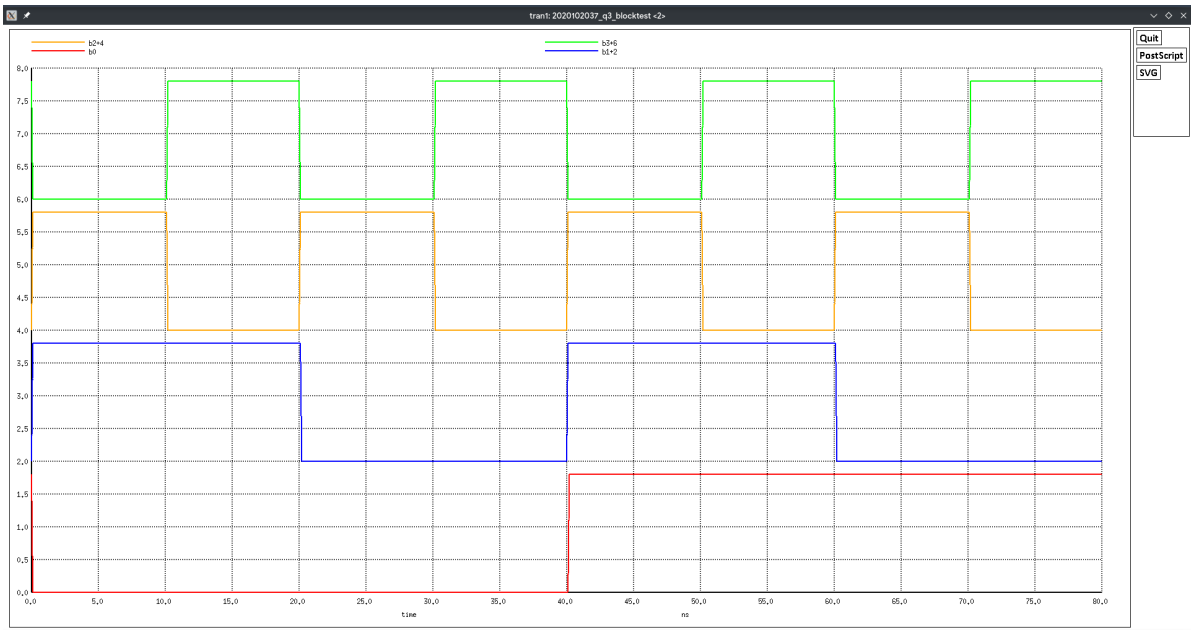
```
* Carry Propogate and Carry Generate Block

.subckt pgsub p g a b
xxor21 p a b xor2
xand21 g a b and2
.ends

.subckt pgblock p0 p1 p2 p3 g0 g1 g2 g3 a0 a1 a2 a3 b0 b1 b2 b3
xpg0 p0 g0 a0 b0 pgsub
xpg1 p1 g1 a1 b1 pgsub
xpg2 p2 g2 a2 b2 pgsub
xpg3 p3 g3 a3 b3 pgsub
.ends
```

3.2.1.2 Simulation Results

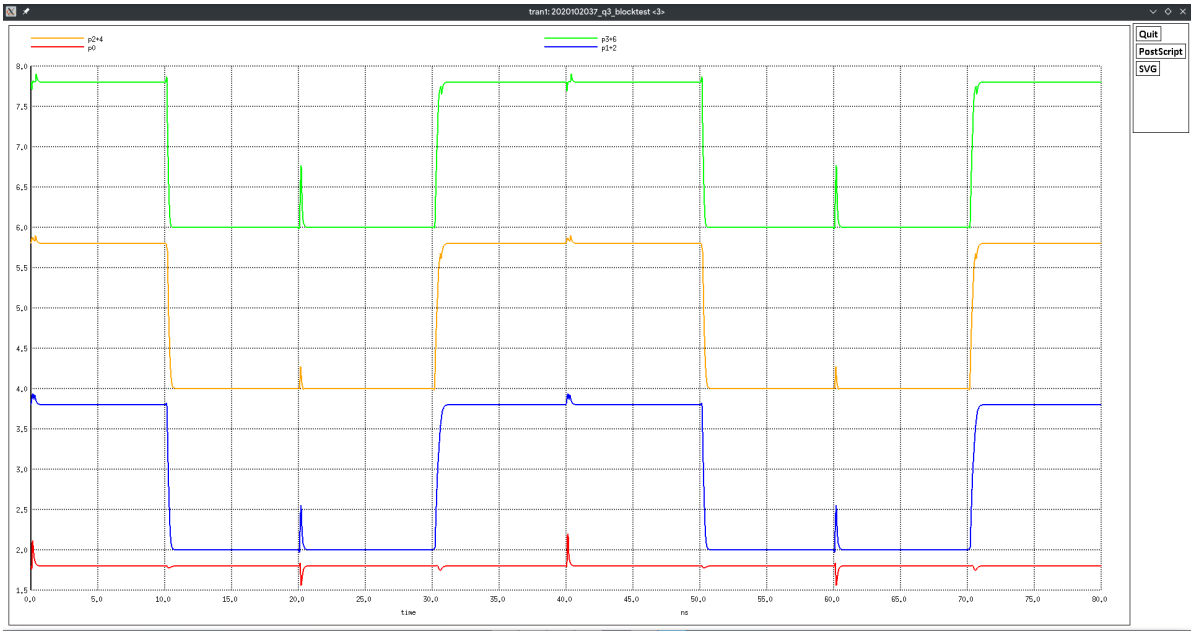
Input A



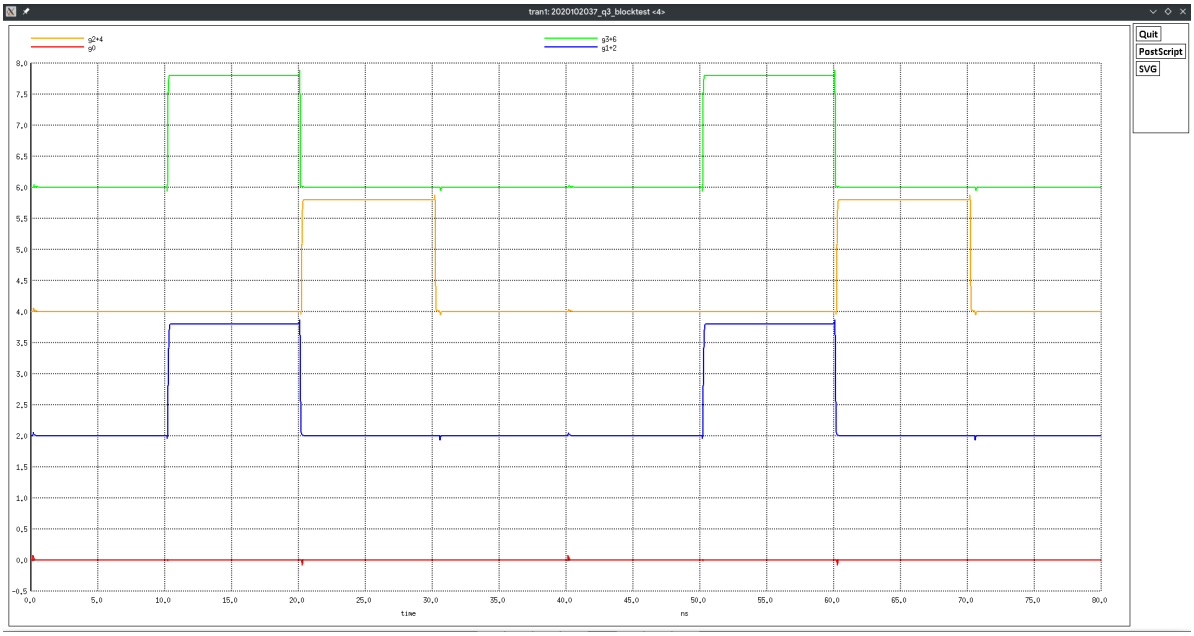
Input B



Output P



Ouput G



3.2.2 Carry Lookahead Block

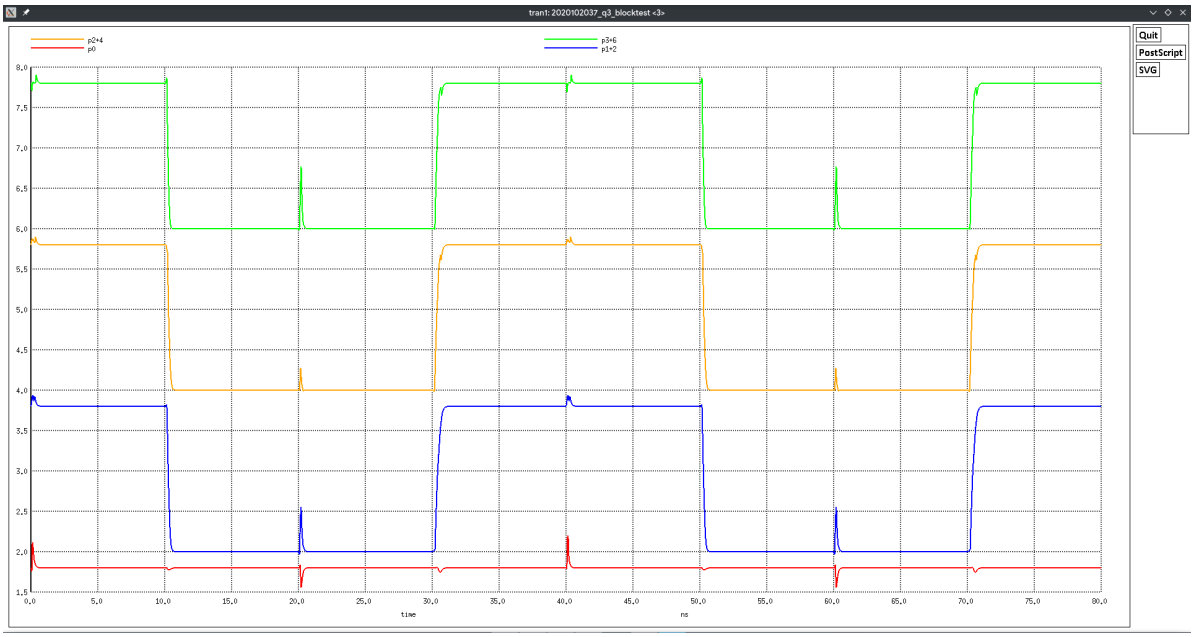
3.2.2.1 Netlist

```
* Carry Lookahead Block

.subckt clblock c1 c2 c3 c4 p0 p1 p2 p3 g0 g1 g2 g3 c0
xand21 a0 p0 c0 and2
xor21  c1 g0 a0 or2

xand22 a1 p1 g0 and2
xand31 a2 p1 p0 c0 and3
xor31  c2 g1 a1 a2 or3

xand23 a3 p2 g1 and2
xand32 a4 p2 p1 g0 and3
xand41 a5 p2 p1 p0 c0 and4
xor41  c3 g2 a3 a4 a5 or4
```

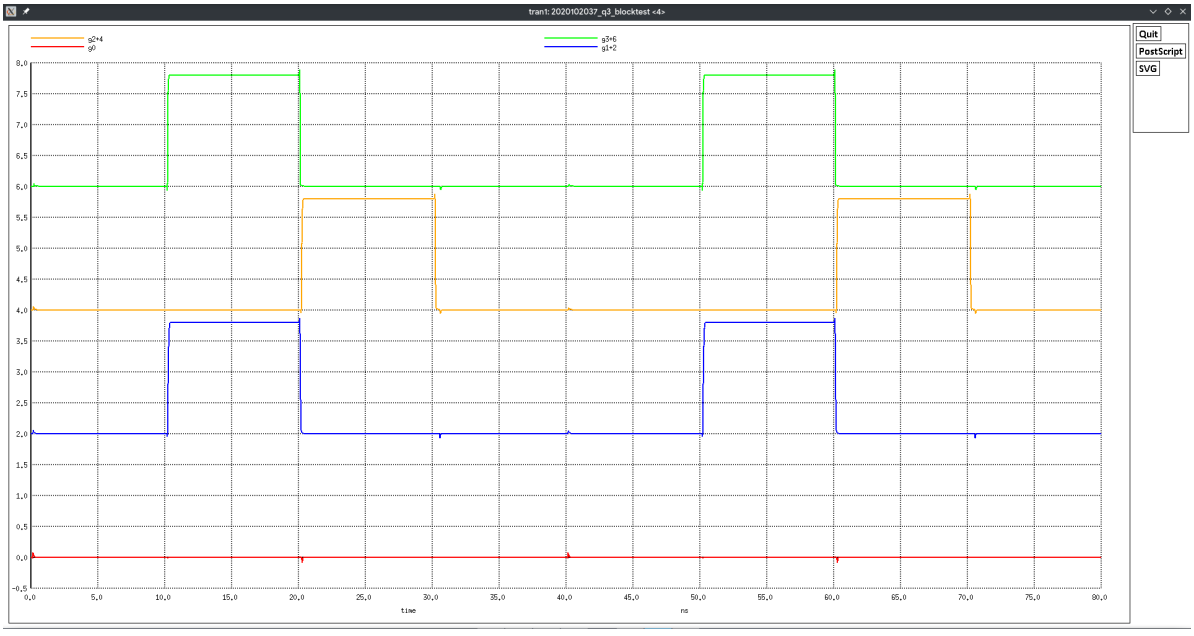
```
xand24 a6 p3 g2 and2
xand33 a7 p3 p2 g1 and3
xand42 a8 p3 p2 p1 g0 and4
xand51 a9 p3 p2 p1 p0 c0 and5
xor51  c4 g3 a6 a7 a8 a9 or5
.ends
```

3.2.2.2 Simulation Results

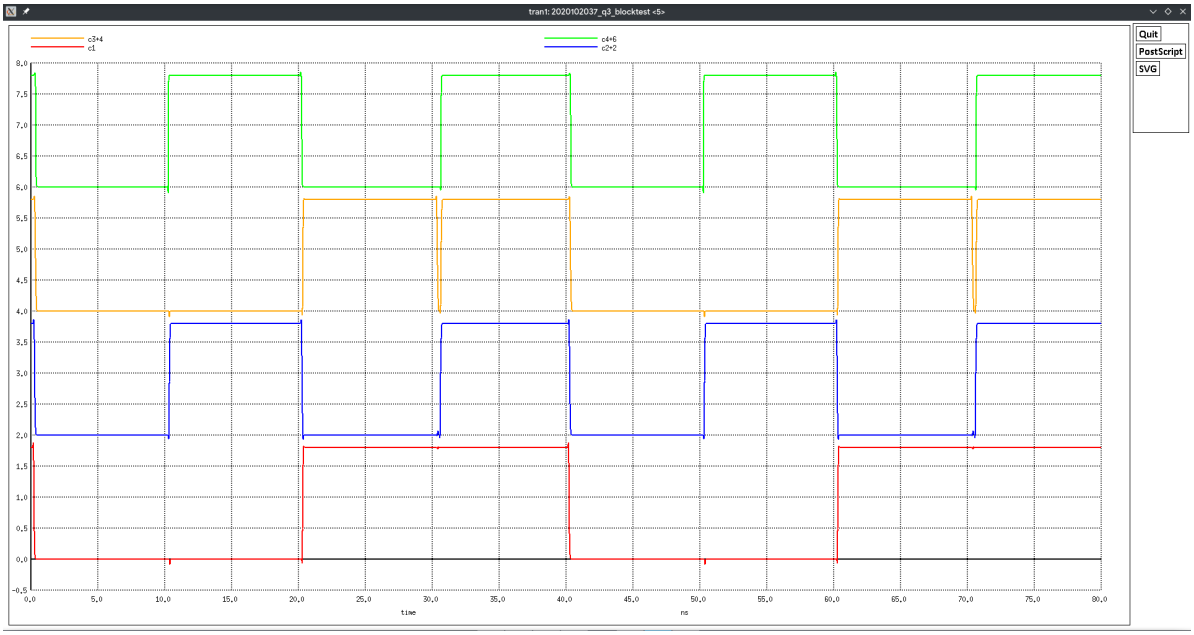
Input P



Input G



Output Carries



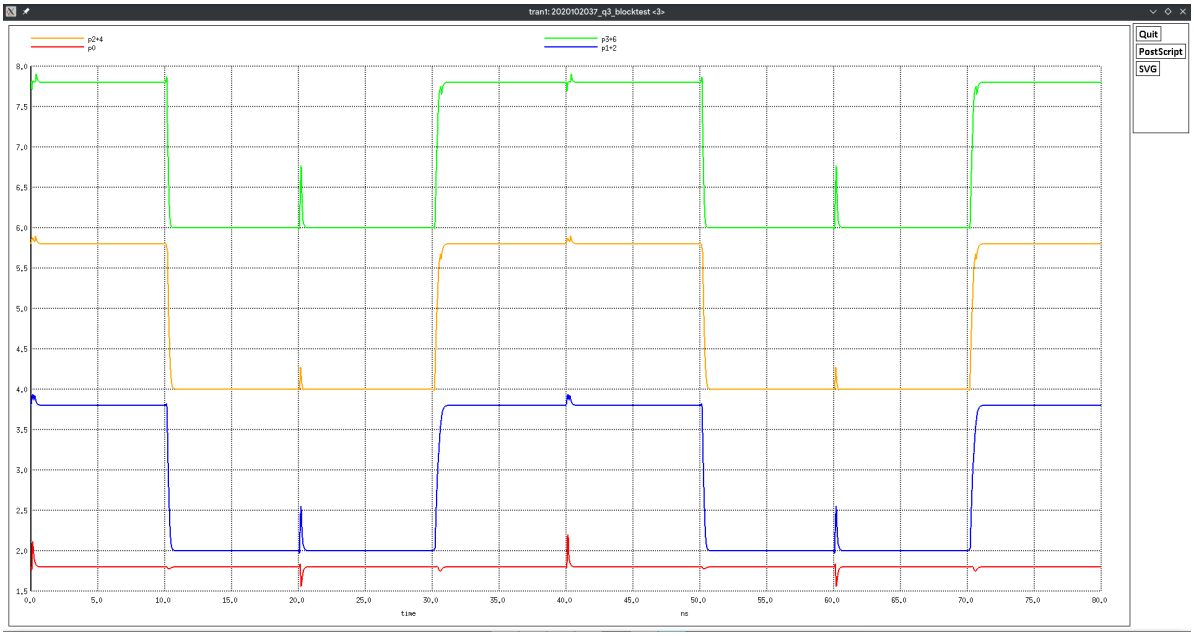
3.2.3 Sum Block

3.2.3.1 Netlist

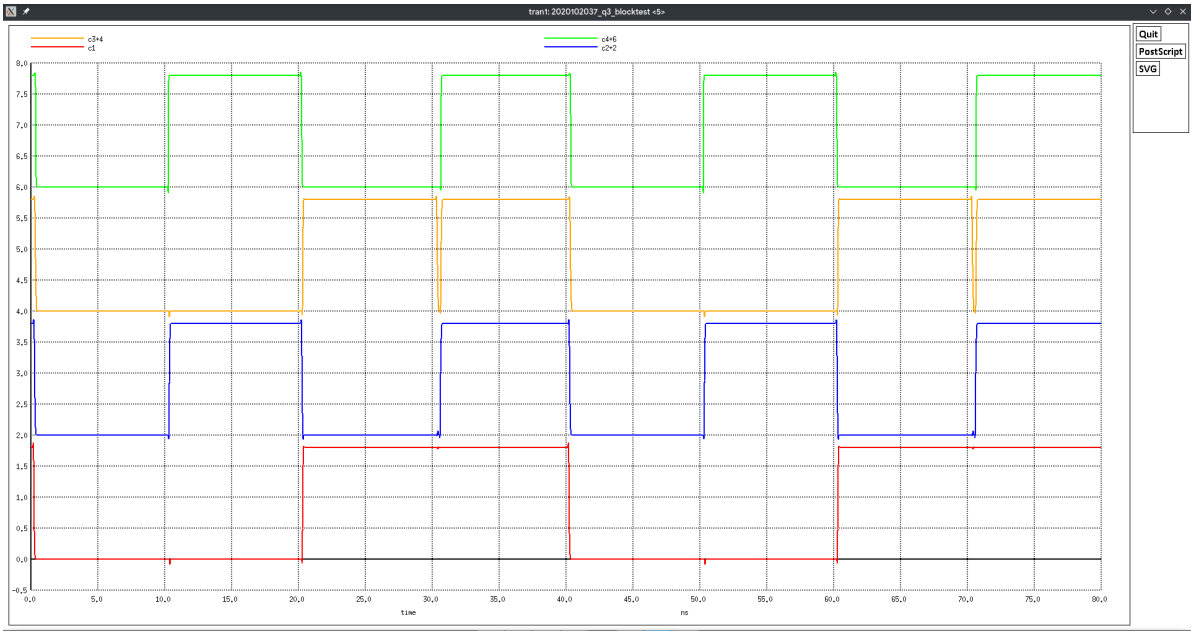
```
* Sum Block

.subckt sumblock s0 s1 s2 s3 p0 p1 p2 p3 c0 c1 c2 c3
xxor21 s0 p0 c0 xor2
xxor22 s1 p1 c1 xor2
xxor23 s2 p2 c2 xor2
xxor24 s3 p3 c3 xor2
.ends
```

3.2.3.2 Simulation Results

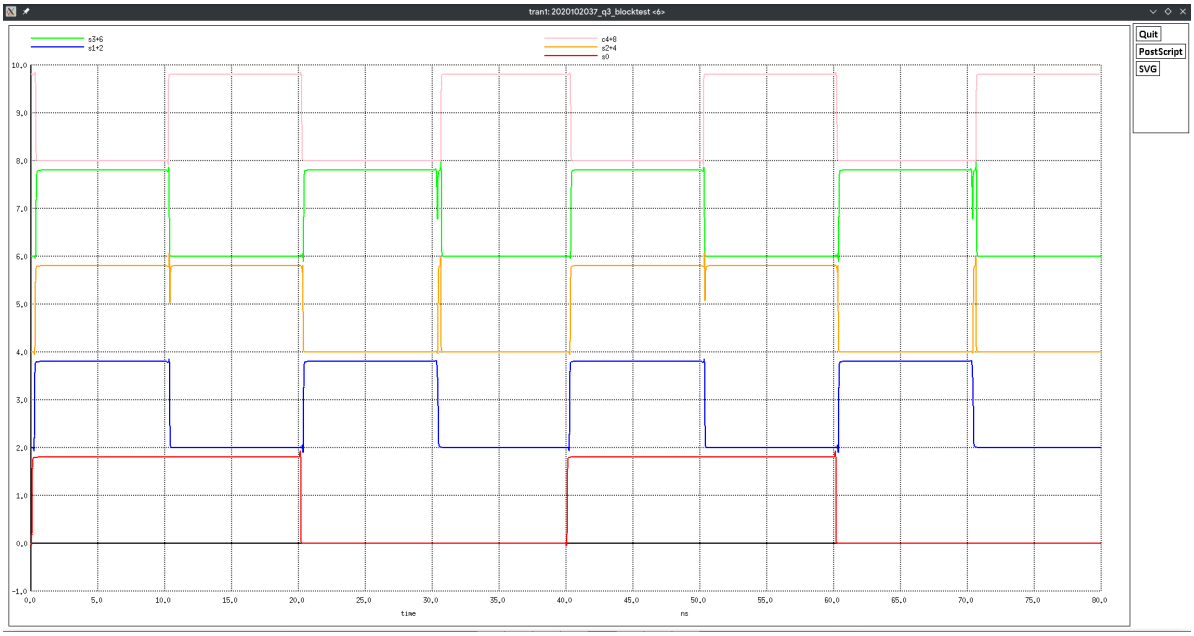
Input P



Input Carries



Output Sum



4. Stick Diagrams of Gates

5. Magic Layouts and Post-Layout Simulations

5.1 Gates

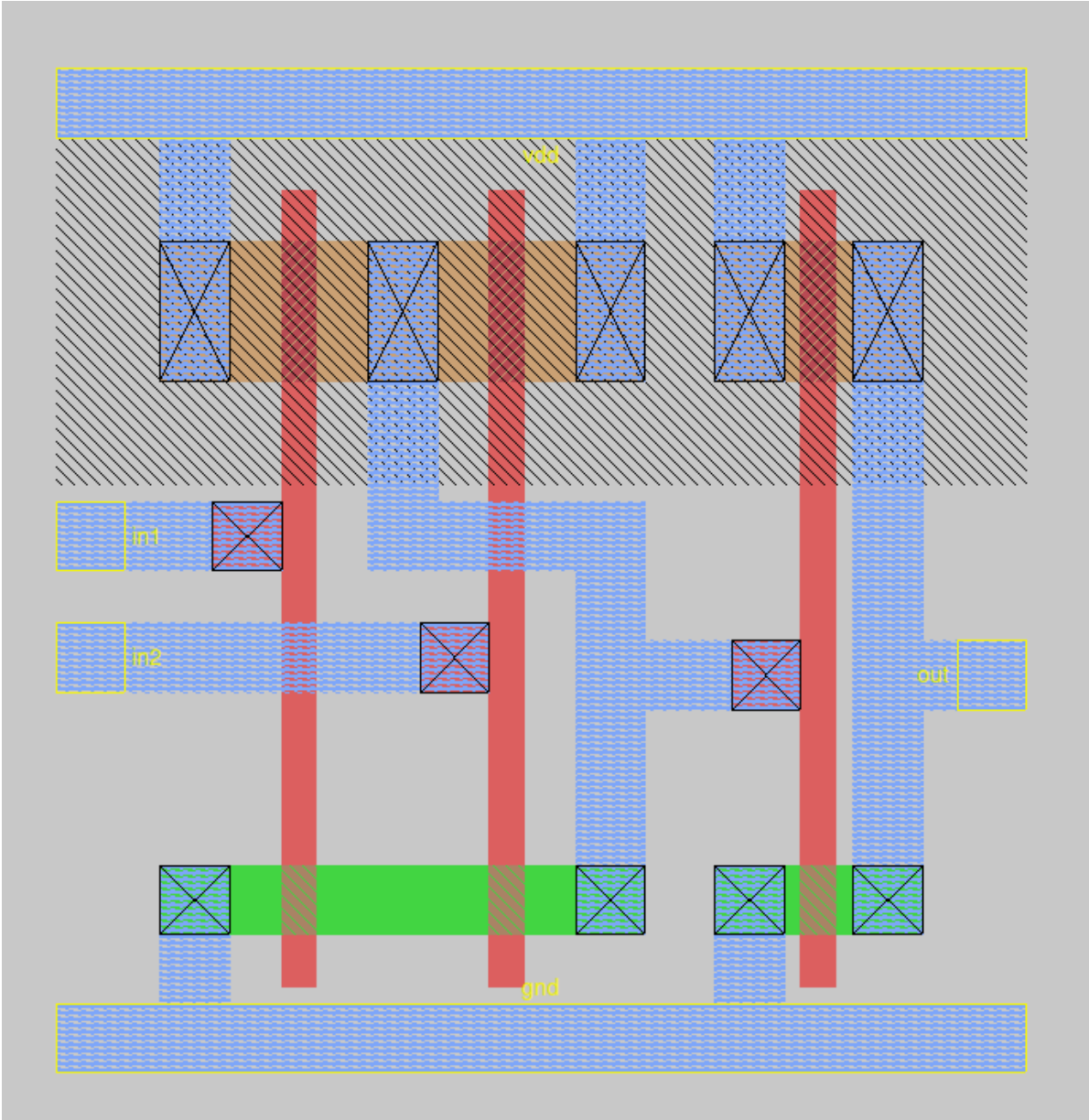
Gate Testing Code

```
.include ../../TSMC_180nm.txt

** Parameters **
.param VSupply=1.8
.global vdd gnd

** Input Voltages **
VS vdd gnd VSupply
```

```
* V1 in1 gnd pulse VSupply 0 0 100p 100p 10n 20n
* V2 in2 gnd pulse VSupply 0 0 100p 100p 20n 40n
* V3 in3 gnd pulse VSupply 0 0 100p 100p 40n 80n
* V4 in4 gnd pulse VSupply 0 0 100p 100p 80n 160n
* V5 in5 gnd pulse VSupply 0 0 100p 100p 160n 320n

** Circuit Description **
.option scale=0.09u
* Netlist

** Analysis **
* .tran 1p 40n
* .tran 1p 80n
* .tran 1p 160n
* .tran 1p 320n

** Plotting **
.control
set hcopypscolor=1
set color0=white
set color1=black
run
set curplottitle="2020102037_Q5_Test_Gate"
* plot out in1+2
* plot out in1+2 in2+4
* plot out in1+2 in2+4 in3+6
* plot out in1+2 in2+4 in3+6 in4+8
* plot out in1+2 in2+4 in3+6 in4+8 in5+10
.endc

.end
```

5.1.1 2-Input AND Gate

5.1.1.1 Layout

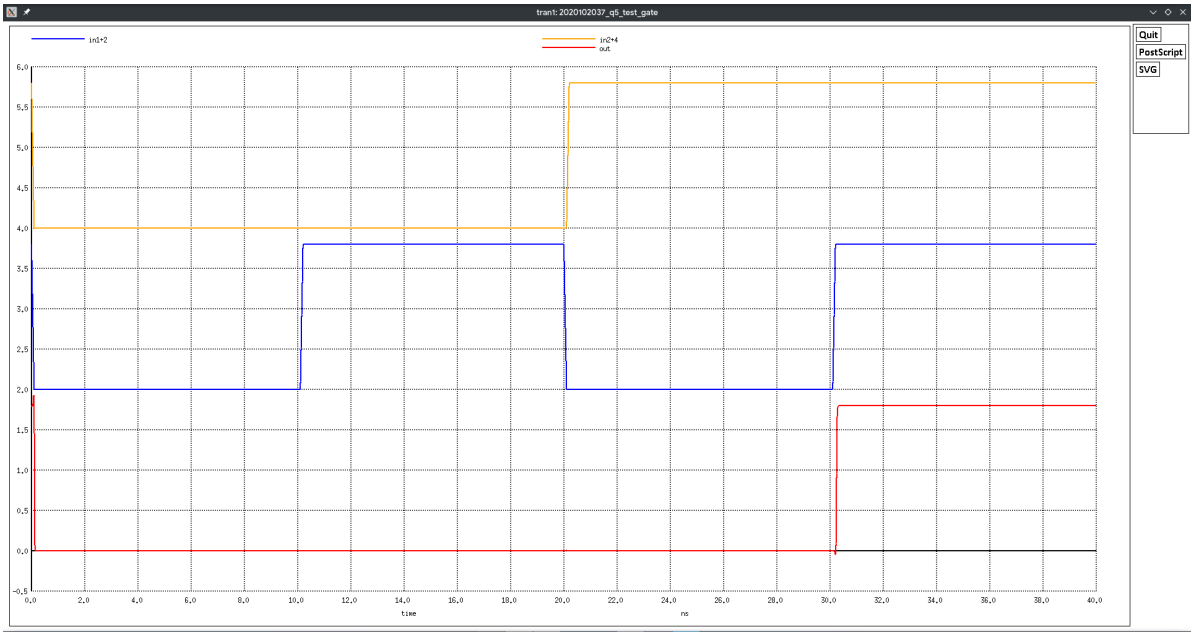


5.1.1.2 Netlist

```
* SPICE3 file created from and2.ext - technology: scmos

.option scale=0.09u

M1000 a_15_6# in1 vdd w_0_0# pfet w=8 l=2
+  ad=80 pd=36 as=152 ps=86
M1001 vdd in2 a_15_6# w_0_0# pfet w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1002 a_15_n26# in1 gnd Gnd nfet w=4 l=2
+  ad=40 pd=28 as=48 ps=40
M1003 out a_15_6# gnd Gnd nfet w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1004 out a_15_6# vdd w_0_0# pfet w=8 l=2
+  ad=40 pd=26 as=0 ps=0
M1005 a_15_6# in2 a_15_n26# Gnd nfet w=4 l=2
+  ad=28 pd=22 as=0 ps=0
C0 in1 vdd 0.02fF
C1 a_15_6# in1 0.03fF
C2 w_0_0# vdd 0.14fF
C3 w_0_0# a_15_6# 0.09fF
```

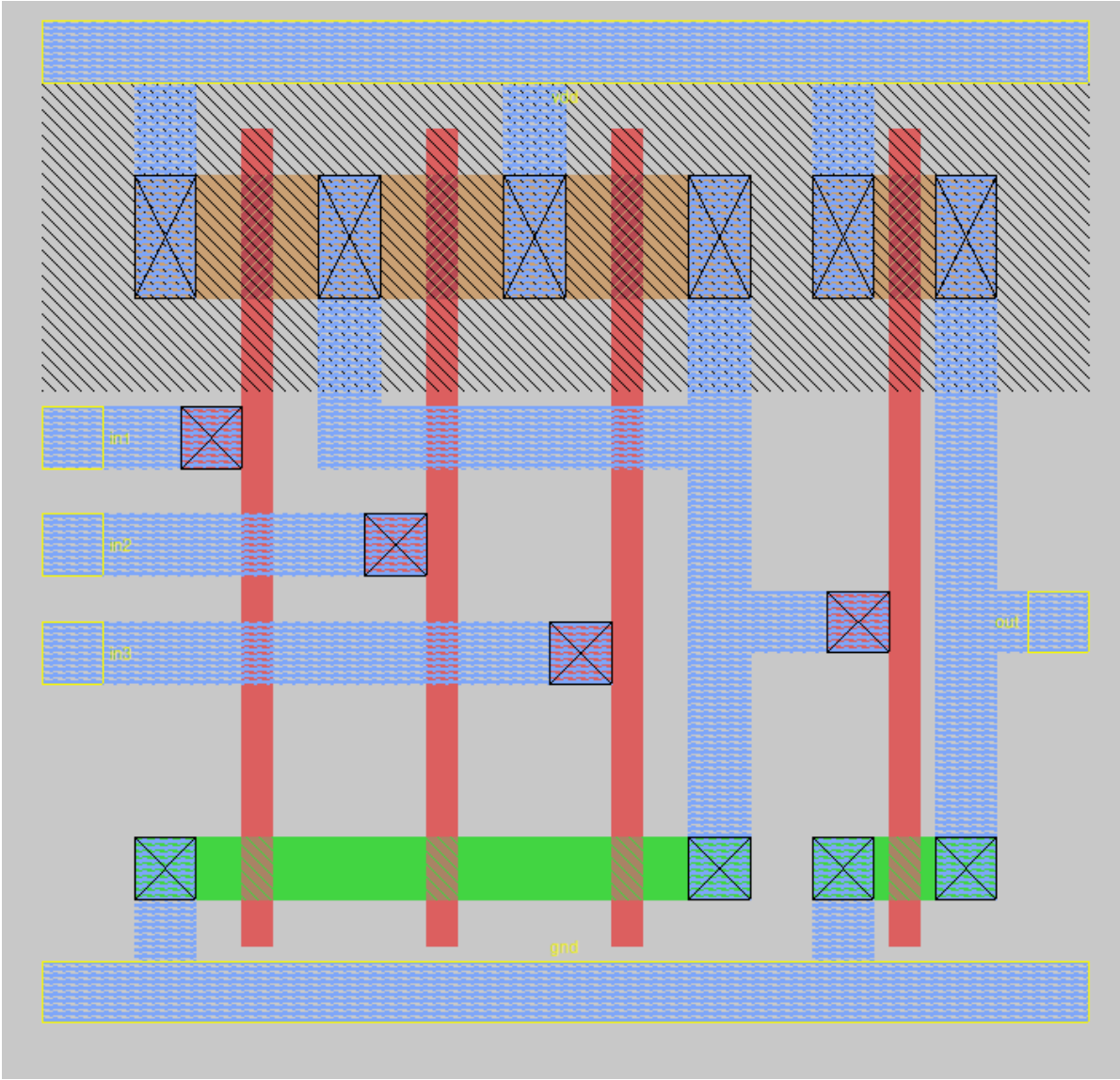
```
C4 w_0_0# out 0.03fF
C5 a_15_6# in2 0.21fF
C6 a_15_6# gnd 0.08fF
C7 gnd out 0.08fF
C8 w_0_0# in1 0.06fF
C9 a_15_6# vdd 0.05fF
C10 out vdd 0.11fF
C11 a_15_6# out 0.05fF
C12 in2 in1 0.27fF
C13 w_0_0# in2 0.06fF
C14 gnd Gnd 0.23fF
C15 out Gnd 0.10fF
C16 vdd Gnd 0.13fF
C17 a_15_6# Gnd 0.32fF
C18 in2 Gnd 0.26fF
C19 in1 Gnd 0.23fF
C20 w_0_0# Gnd 1.12fF
```

5.1.2.2 Simulations Results



5.1.2 3-Input AND Gate

5.1.2.1 Layout

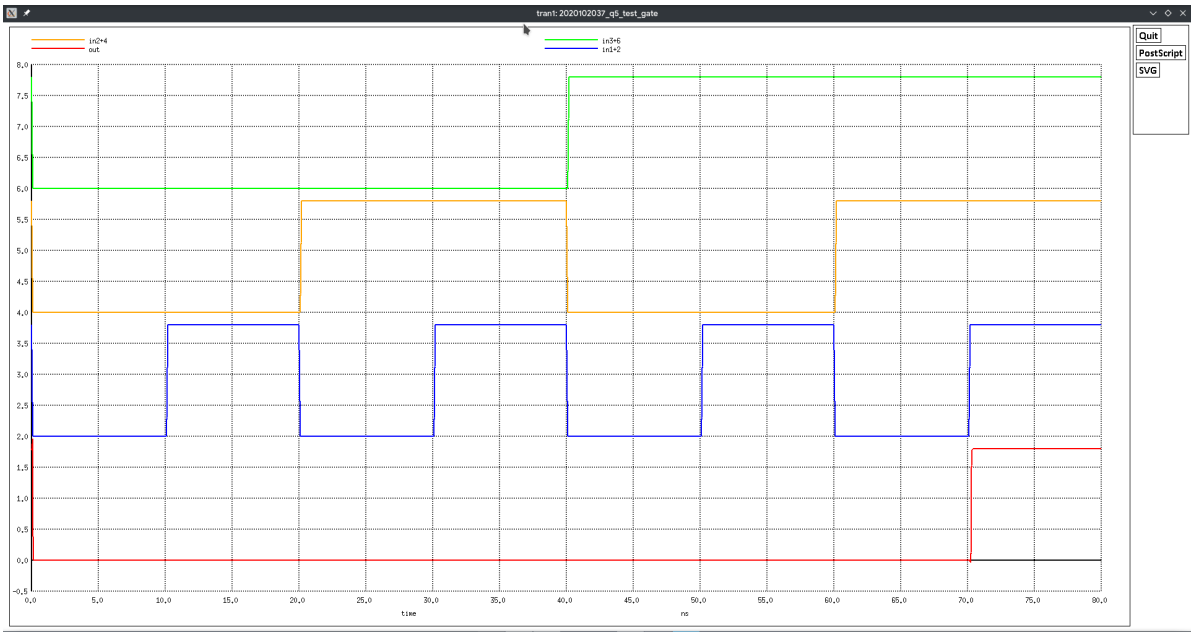


5.1.2.2 Netlist

```
* SPICE3 file created from and3.ext - technology: scmos

.option scale=0.09u

M1000 a_15_6# in1 vdd w_0_0# pfet w=8 l=2
+  ad=136 pd=66 as=176 ps=92
M1001 a_15_n33# in1 gnd Gnd nfet w=4 l=2
+  ad=40 pd=28 as=48 ps=40
M1002 vdd in2 a_15_6# w_0_0# pfet w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1003 a_15_6# in3 vdd w_0_0# pfet w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1004 a_27_n33# in2 a_15_n33# Gnd nfet w=4 l=2
+  ad=40 pd=28 as=0 ps=0
M1005 out a_15_6# gnd Gnd nfet w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1006 a_15_6# in3 a_27_n33# Gnd nfet w=4 l=2
+  ad=28 pd=22 as=0 ps=0
M1007 out a_15_6# vdd w_0_0# pfet w=8 l=2
+  ad=40 pd=26 as=0 ps=0
C0 in1 w_0_0# 0.06fF
C1 gnd out 0.08fF
C2 a_15_6# out 0.05fF
```

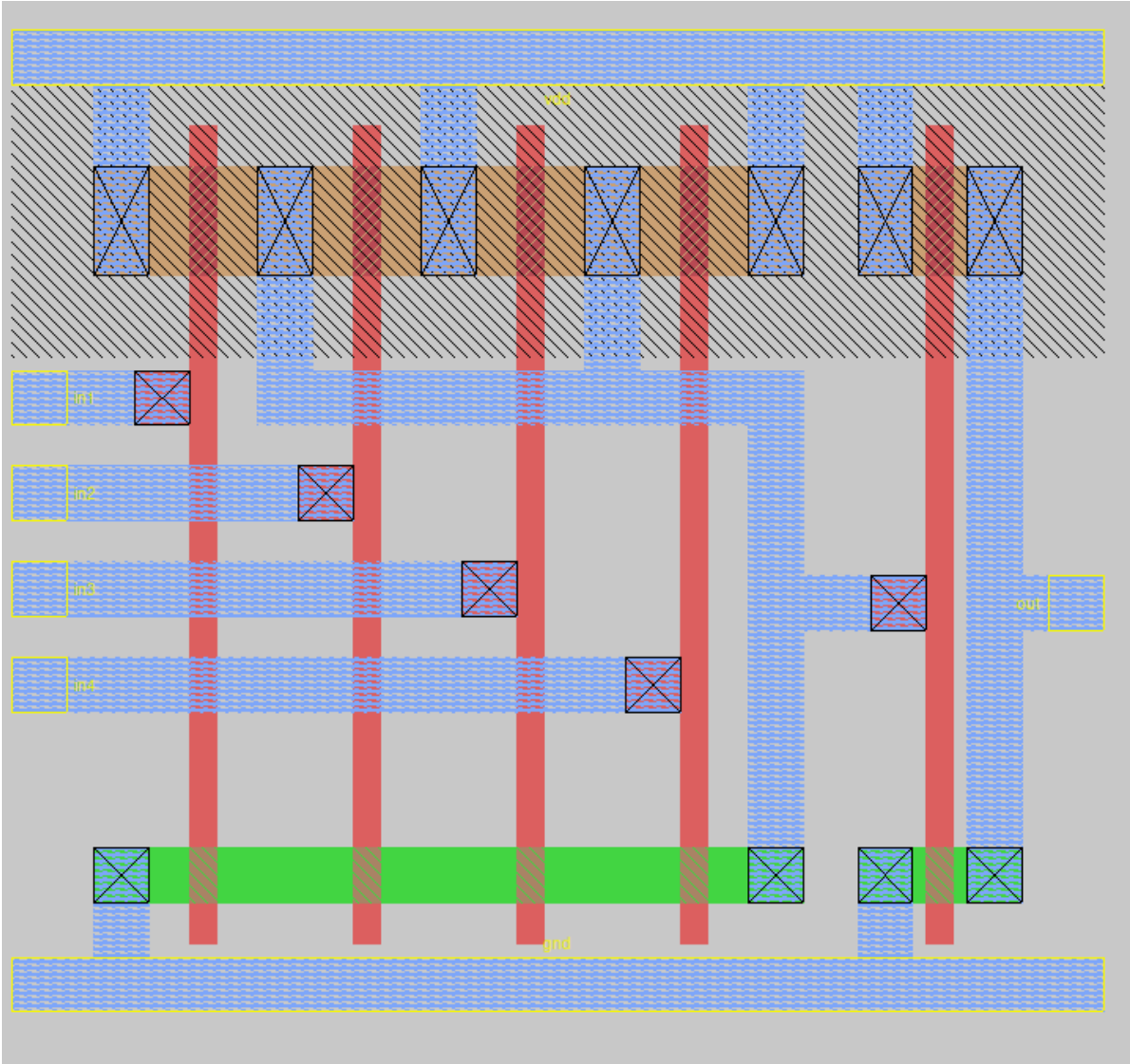
```
C3 vdd w_0_0# 0.14fF
C4 in1 vdd 0.02fF
C5 out w_0_0# 0.03fF
C6 a_15_6# in2 0.17fF
C7 vdd out 0.11fF
C8 in3 in2 0.44fF
C9 w_0_0# in2 0.06fF
C10 a_15_6# gnd 0.08fF
C11 in1 in2 0.27fF
C12 a_15_6# in3 0.11fF
C13 a_15_6# w_0_0# 0.12fF
C14 in1 a_15_6# 0.03fF
C15 in3 w_0_0# 0.06fF
C16 a_15_6# vdd 0.16fF
C17 in1 in3 0.08fF
C18 gnd Gnd 0.26fF
C19 out Gnd 0.12fF
C20 vdd Gnd 0.16fF
C21 a_15_6# Gnd 0.42fF
C22 in3 Gnd 0.34fF
C23 in2 Gnd 0.30fF
C24 in1 Gnd 0.27fF
C25 w_0_0# Gnd 1.37fF
```

5.1.2.2 Simulations Results



5.1.3 4-Input AND Gate

5.1.3.1 Layout

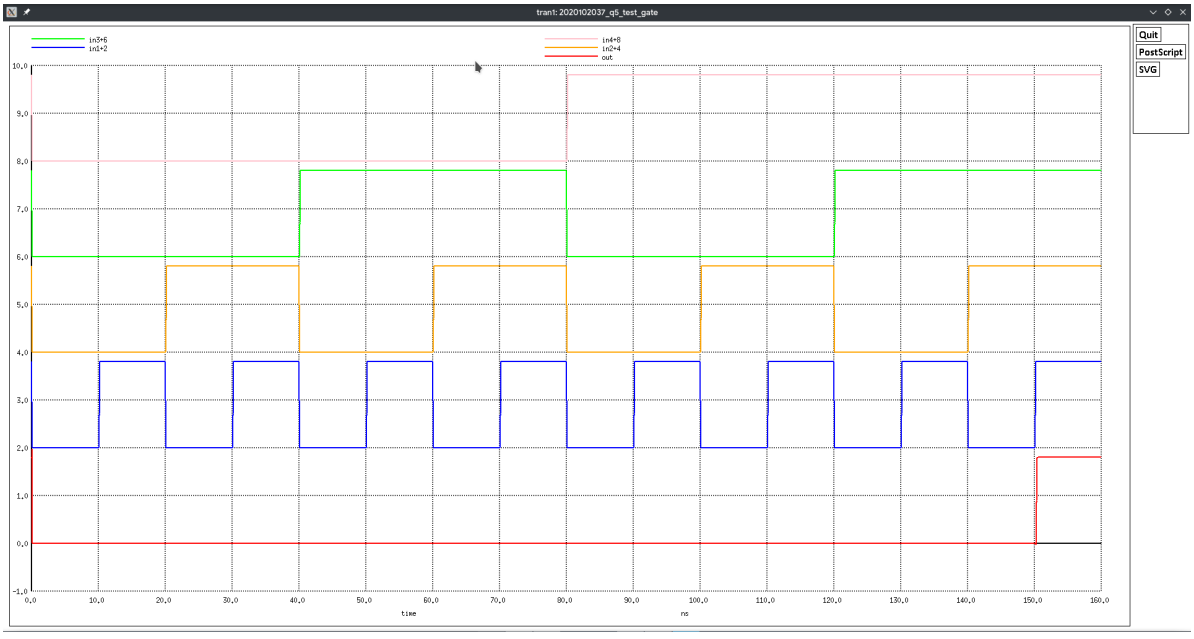


5.1.3.2 Netlist

```
* SPICE3 file created from and4.ext - technology: scmos

.option scale=0.09u

M1000 out a_15_6# vdd w_0_0# pfet w=8 l=2
+  ad=40 pd=26 as=232 ps=122
M1001 a_15_n40# in1 gnd Gnd nfet w=4 l=2
+  ad=40 pd=28 as=48 ps=40
M1002 a_15_6# in1 vdd w_0_0# pfet w=8 l=2
+  ad=160 pd=72 as=0 ps=0
M1003 a_27_n40# in2 a_15_n40# Gnd nfet w=4 l=2
+  ad=40 pd=28 as=0 ps=0
M1004 vdd in2 a_15_6# w_0_0# pfet w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1005 a_15_6# in3 vdd w_0_0# pfet w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1006 a_39_n40# in3 a_27_n40# Gnd nfet w=4 l=2
+  ad=40 pd=28 as=0 ps=0
M1007 vdd in4 a_15_6# w_0_0# pfet w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1008 out a_15_6# gnd Gnd nfet w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1009 a_15_6# in4 a_39_n40# Gnd nfet w=4 l=2
```

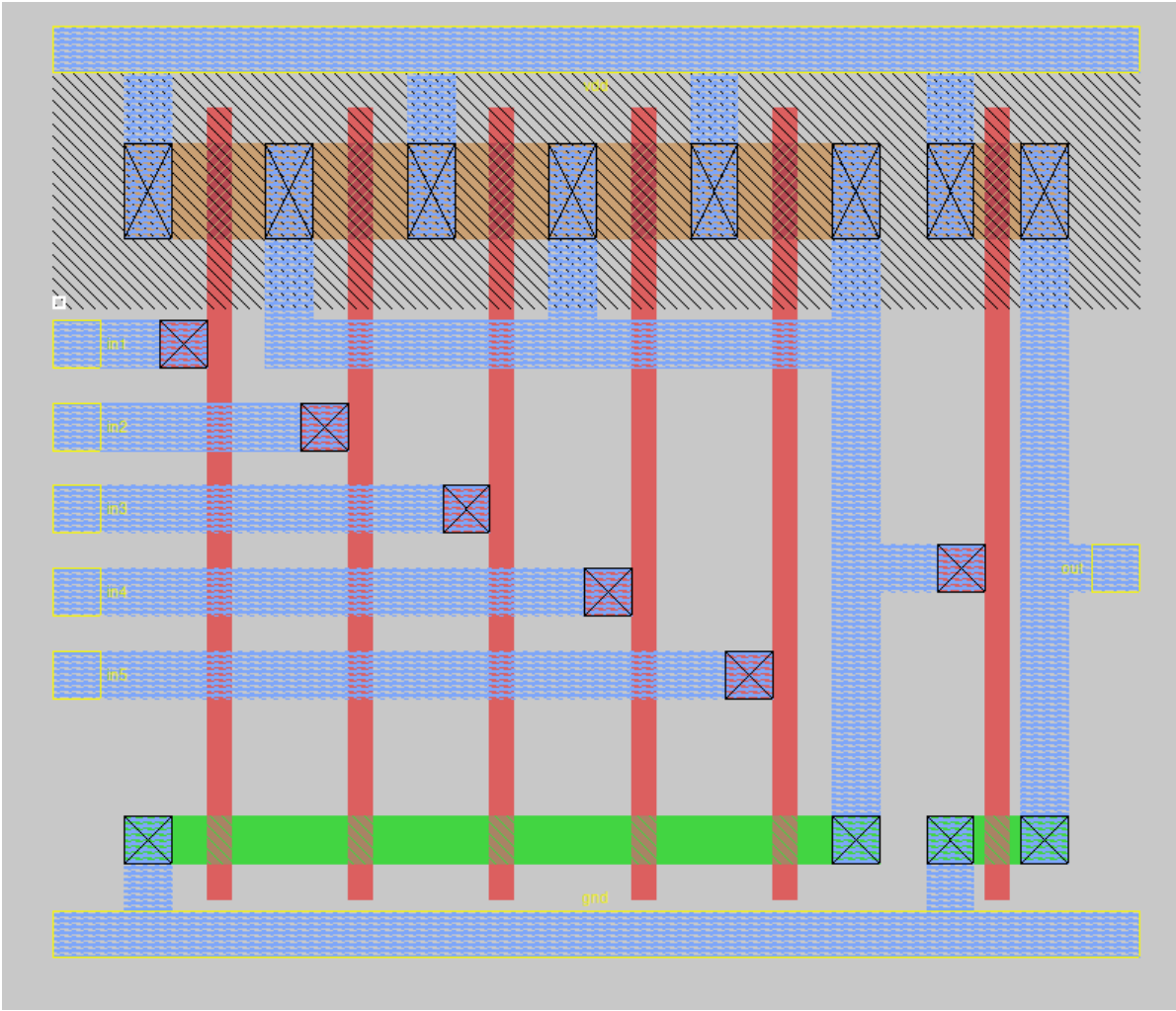
```
+  ad=28 pd=22 as=0 ps=0
C0 w_0_0# in3 0.06fF
C1 in2 in3 0.44fF
C2 a_15_6# in1 0.03fF
C3 in4 in3 0.60fF
C4 w_0_0# in2 0.06fF
C5 w_0_0# in4 0.06fF
C6 in2 in4 0.08fF
C7 vdd w_0_0# 0.18fF
C8 a_15_6# in3 0.08fF
C9 w_0_0# out 0.03fF
C10 in1 in3 0.08fF
C11 a_15_6# w_0_0# 0.11fF
C12 gnd out 0.08fF
C13 in1 w_0_0# 0.06fF
C14 vdd out 0.11fF
C15 a_15_6# in2 0.17fF
C16 a_15_6# in4 0.11fF
C17 in1 in2 0.27fF
C18 in1 in4 0.08fF
C19 a_15_6# gnd 0.08fF
C20 a_15_6# vdd 0.10fF
C21 in1 vdd 0.02fF
C22 a_15_6# out 0.05fF
C23 gnd Gnd 0.30fF
C24 out Gnd 0.15fF
C25 vdd Gnd 0.19fF
C26 a_15_6# Gnd 0.51fF
C27 in4 Gnd 0.41fF
C28 in3 Gnd 0.38fF
C29 in2 Gnd 0.34fF
C30 in1 Gnd 0.31fF
C31 w_0_0# Gnd 1.61fF
```

5.1.3.3 Simulation Results



5.1.4 5-Input AND Gate

5.1.4.1 Layout

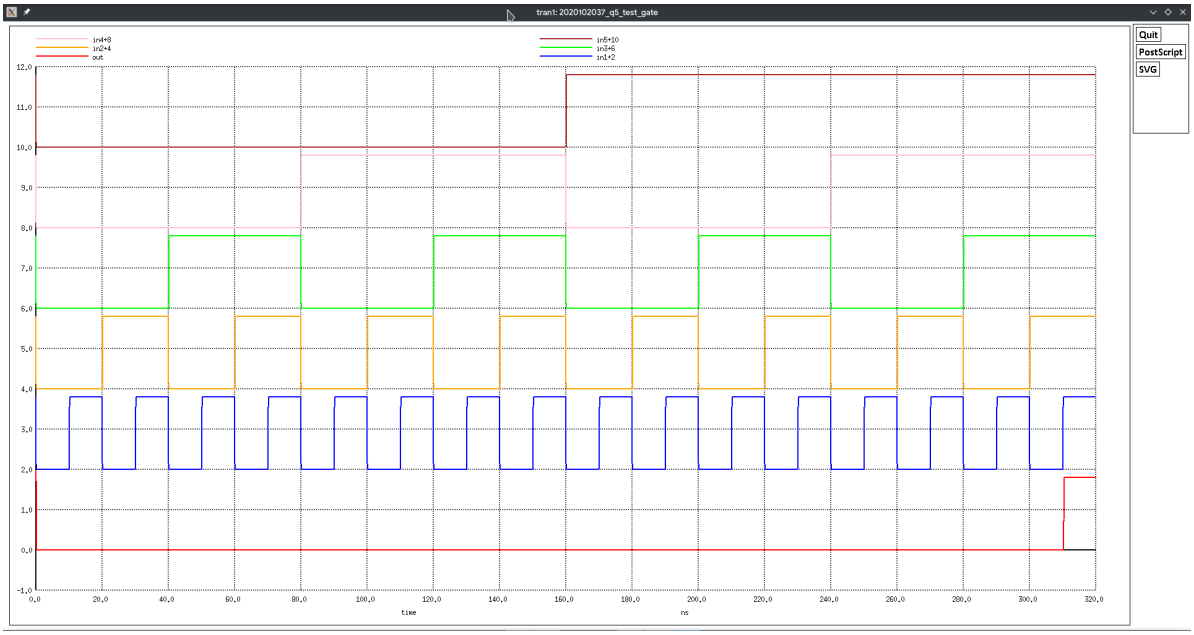


5.1.4.2 Netlist

```
* SPICE3 file created from and5.ext - technology: scmos

.option scale=0.09u

M1000 a_39_n47# in3 a_27_n47# Gnd nfet w=4 l=2
+  ad=40 pd=28 as=40 ps=28
M1001 out a_15_6# vdd w_0_0# pfet w=8 l=2
+  ad=40 pd=26 as=256 ps=128
M1002 a_15_6# in5 vdd w_0_0# pfet w=8 l=2
+  ad=216 pd=102 as=0 ps=0
M1003 a_15_6# in1 vdd w_0_0# pfet w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1004 a_51_n47# in4 a_39_n47# Gnd nfet w=4 l=2
+  ad=40 pd=28 as=0 ps=0
M1005 vdd in2 a_15_6# w_0_0# pfet w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1006 out a_15_6# gnd Gnd nfet w=4 l=2
+  ad=20 pd=18 as=48 ps=40
M1007 a_15_6# in3 vdd w_0_0# pfet w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1008 vdd in4 a_15_6# w_0_0# pfet w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1009 a_15_n47# in1 gnd Gnd nfet w=4 l=2
+  ad=40 pd=28 as=0 ps=0
```

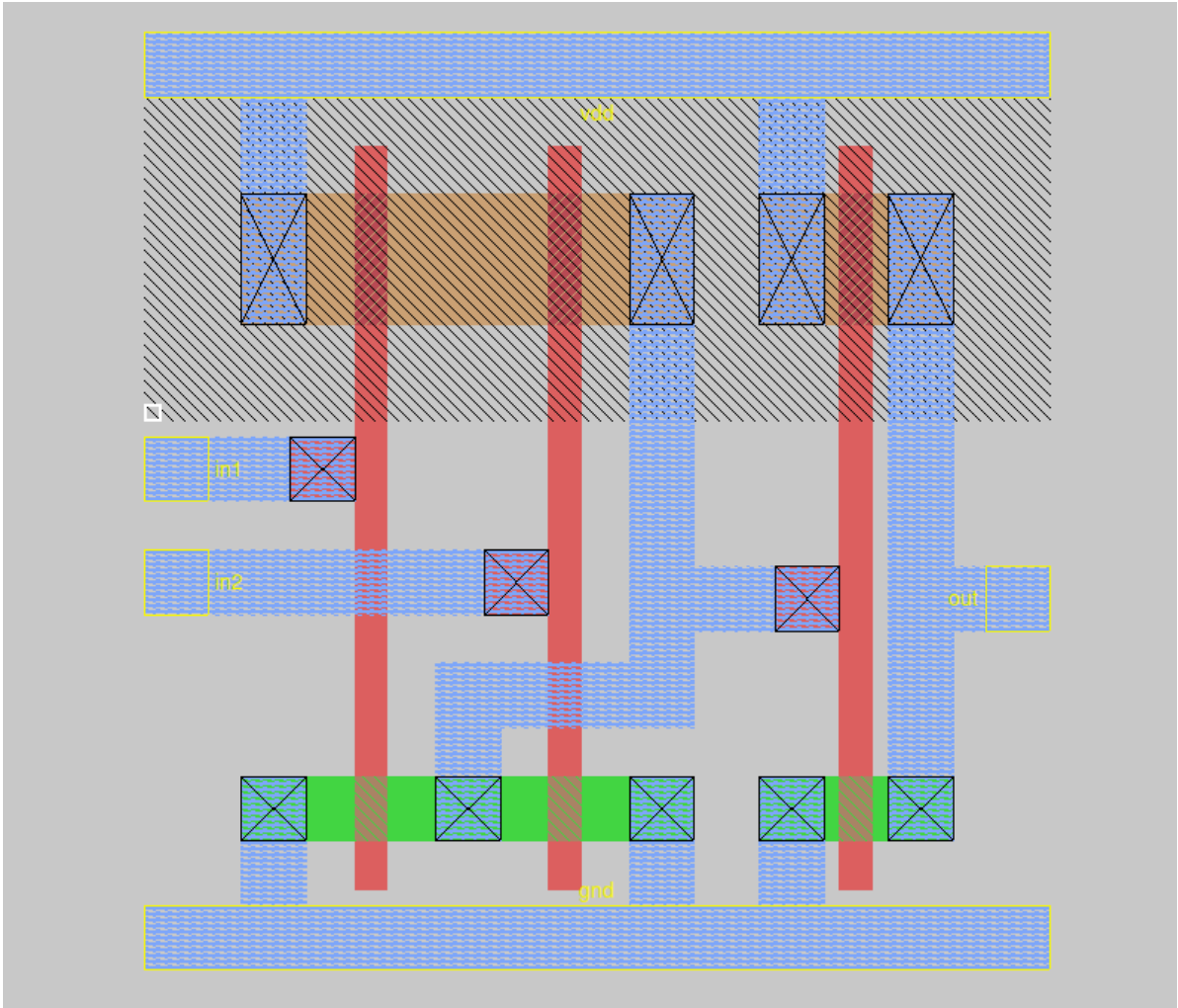
```
M1010 a_15_6# in5 a_51_n47# Gnd nfet w=4 l=2
+  ad=28 pd=22 as=0 ps=0
M1011 a_27_n47# in2 a_15_n47# Gnd nfet w=4 l=2
+  ad=0 pd=0 as=0 ps=0
C0 in3 in4 0.60fF
C1 a_15_6# in5 0.11fF
C2 in1 in5 0.08fF
C3 in2 in4 0.08fF
C4 vdd out 0.11fF
C5 w_0_0# in3 0.06fF
C6 in1 a_15_6# 0.03fF
C7 in2 w_0_0# 0.06fF
C8 vdd w_0_0# 0.19fF
C9 in4 in5 0.77fF
C10 in2 in3 0.44fF
C11 a_15_6# out 0.05fF
C12 a_15_6# in4 0.08fF
C13 w_0_0# in5 0.06fF
C14 in1 in4 0.08fF
C15 gnd a_15_6# 0.08fF
C16 a_15_6# w_0_0# 0.14fF
C17 in1 w_0_0# 0.06fF
C18 in3 in5 0.08fF
C19 in2 in5 0.08fF
C20 a_15_6# in3 0.08fF
C21 gnd out 0.08fF
C22 in1 in3 0.08fF
C23 a_15_6# in2 0.17fF
C24 in1 in2 0.27fF
C25 out w_0_0# 0.03fF
C26 a_15_6# vdd 0.21fF
C27 w_0_0# in4 0.06fF
C28 in1 vdd 0.02fF
C29 gnd Gnd 0.34fF
C30 out Gnd 0.17fF
C31 vdd Gnd 0.22fF
C32 a_15_6# Gnd 0.61fF
C33 in5 Gnd 0.48fF
C34 in4 Gnd 0.45fF
C35 in3 Gnd 0.42fF
C36 in2 Gnd 0.38fF
C37 in1 Gnd 0.35fF
C38 w_0_0# Gnd 1.85fF
```

5.1.4.3 Simulation Results



5.1.5 2-Input OR Gate

5.1.5.1 Layout

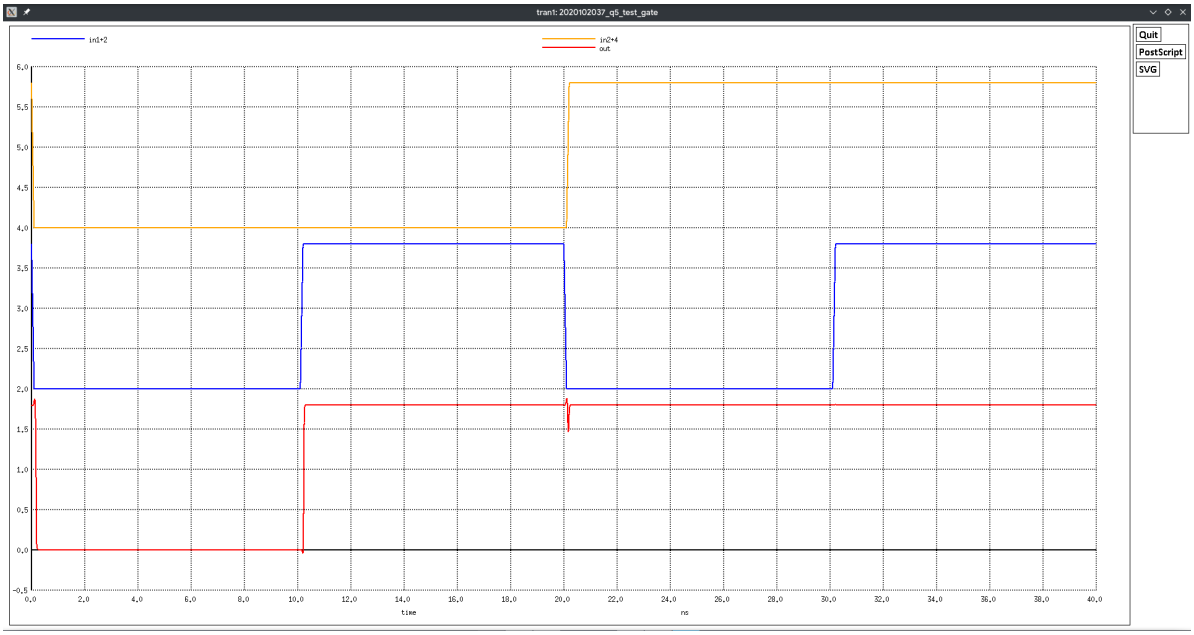


5.1.5.2 Netlist

```
* SPICE3 file created from or2.ext - technology: scmos

.option scale=0.09u
```

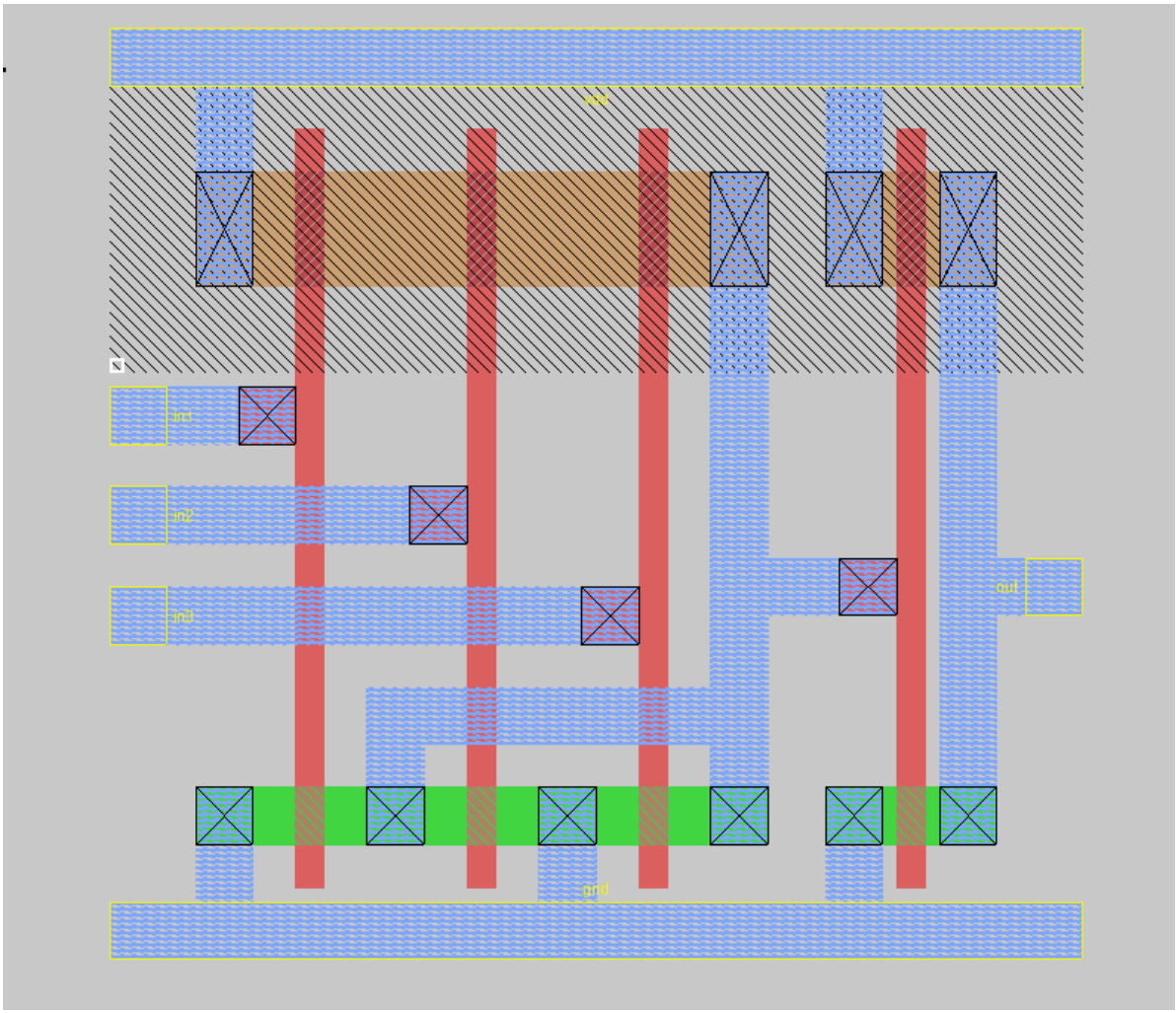
```
M1000 a_15_6# in1 vdd w_0_0# pfet w=8 l=2
+  ad=80 pd=36 as=96 ps=56
M1001 a_15_n26# in2 a_15_6# w_0_0# pfet w=8 l=2
+  ad=56 pd=30 as=0 ps=0
M1002 a_15_n26# in1 gnd Gnd nfet w=4 l=2
+  ad=40 pd=28 as=76 ps=62
M1003 out a_15_n26# gnd Gnd nfet w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1004 out a_15_n26# vdd w_0_0# pfet w=8 l=2
+  ad=40 pd=26 as=0 ps=0
M1005 gnd in2 a_15_n26# Gnd nfet w=4 l=2
+  ad=0 pd=0 as=0 ps=0
C0 out vdd 0.11fF
C1 a_15_n26# in2 0.21fF
C2 a_15_n26# vdd 0.11fF
C3 w_0_0# in2 0.06fF
C4 w_0_0# vdd 0.11fF
C5 w_0_0# in1 0.06fF
C6 in1 in2 0.27fF
C7 in1 vdd 0.02fF
C8 a_15_n26# out 0.05fF
C9 w_0_0# out 0.03fF
C10 out gnd 0.08fF
C11 w_0_0# a_15_n26# 0.10fF
C12 a_15_n26# gnd 0.10fF
C13 gnd Gnd 0.24fF
C14 out Gnd 0.10fF
C15 vdd Gnd 0.13fF
C16 a_15_n26# Gnd 0.32fF
C17 in2 Gnd 0.26fF
C18 in1 Gnd 0.23fF
C19 w_0_0# Gnd 1.12fF
```

5.1.5.2 Simulations Results



5.1.6 3-Input OR Gate

5.1.6.1 Layout

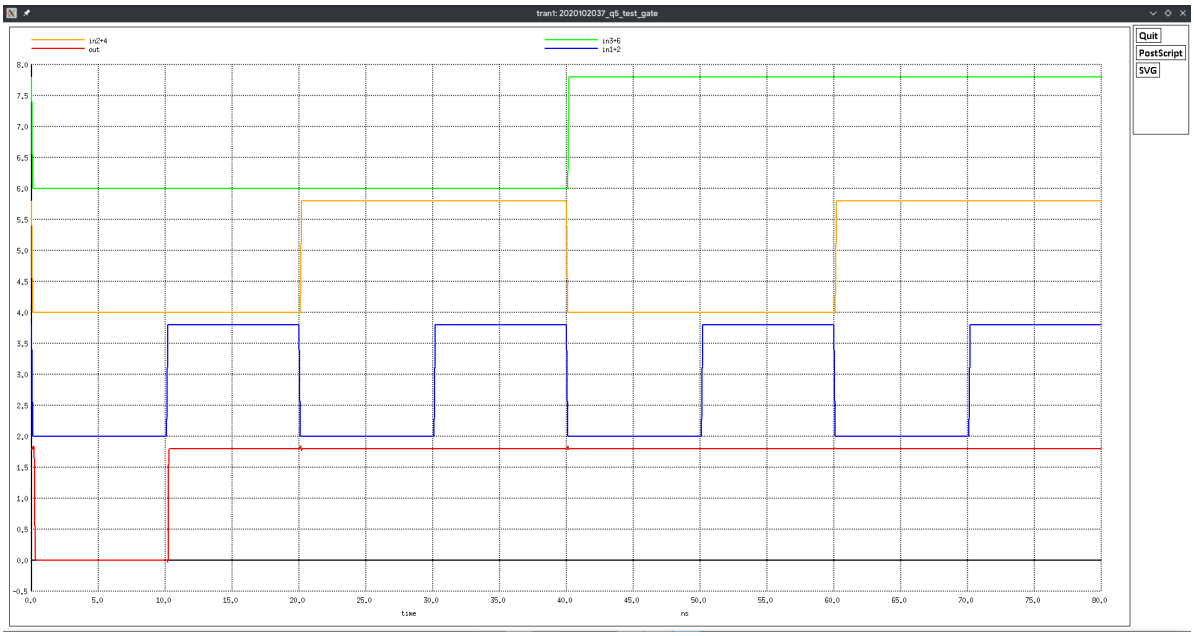


5.1.6.2 Netlist

```
* SPICE3 file created from or3.ext - technology: scmos

.option scale=0.09u

M1000 a_15_6# in1 vdd w_0_0# pfet w=8 l=2
+  ad=80 pd=36 as=96 ps=56
M1001 a_15_n33# in1 gnd Gnd nfet w=4 l=2
+  ad=68 pd=50 as=88 ps=68
M1002 a_27_6# in2 a_15_6# w_0_0# pfet w=8 l=2
+  ad=80 pd=36 as=0 ps=0
M1003 a_15_n33# in3 a_27_6# w_0_0# pfet w=8 l=2
+  ad=56 pd=30 as=0 ps=0
M1004 gnd in2 a_15_n33# Gnd nfet w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1005 out a_15_n33# gnd Gnd nfet w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1006 a_15_n33# in3 gnd Gnd nfet w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1007 out a_15_n33# vdd w_0_0# pfet w=8 l=2
+  ad=40 pd=26 as=0 ps=0
C0 out a_15_n33# 0.05fF
C1 a_15_n33# vdd 0.11fF
C2 w_0_0# out 0.03fF
C3 in1 in2 0.27fF
```

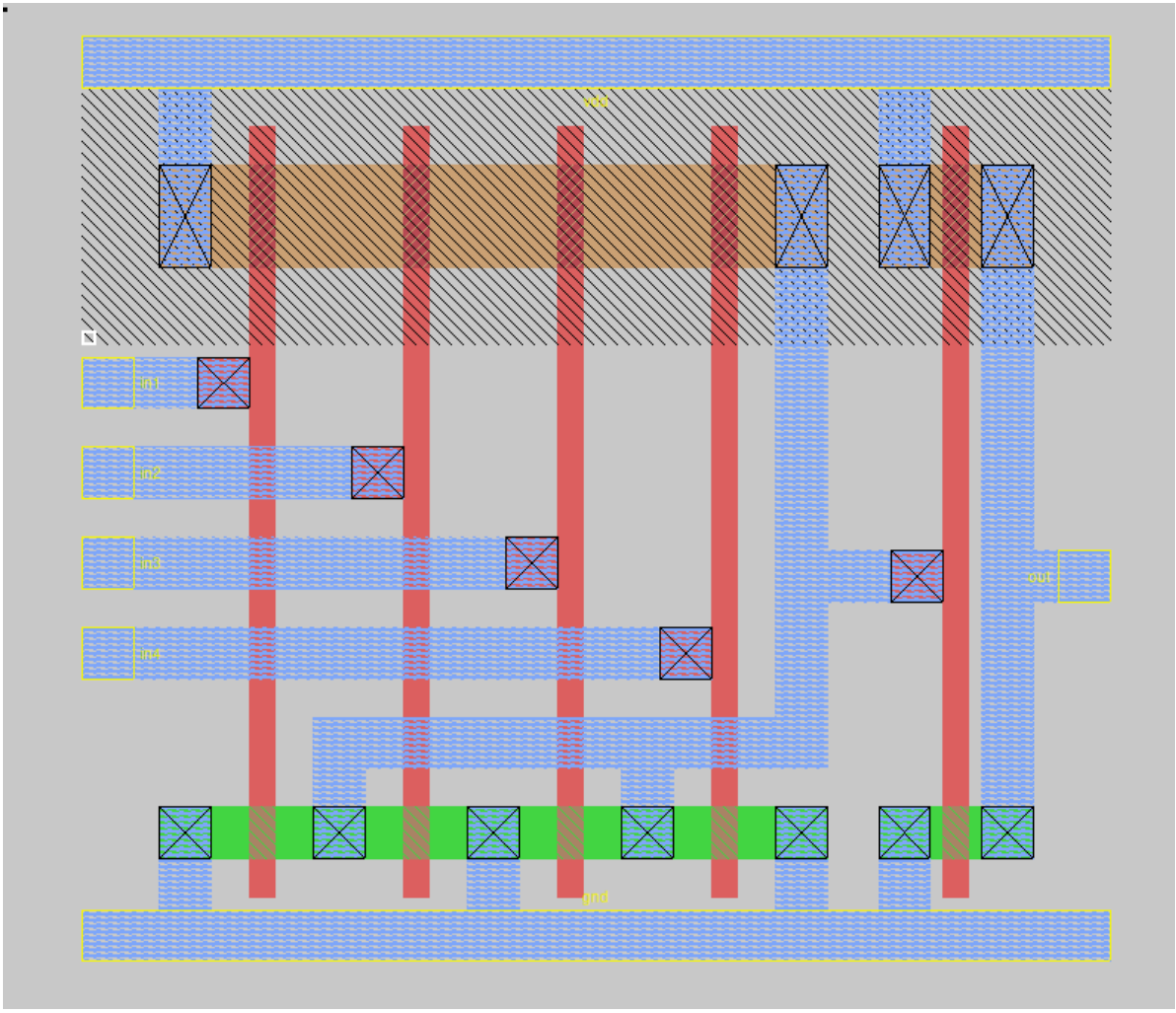
```
C4 w_0_0# vdd 0.12fF
C5 gnd out 0.08fF
C6 in1 vdd 0.02fF
C7 w_0_0# a_15_n33# 0.10fF
C8 in3 a_15_n33# 0.37fF
C9 gnd a_15_n33# 0.18fF
C10 in3 w_0_0# 0.06fF
C11 out vdd 0.11fF
C12 w_0_0# in1 0.06fF
C13 in3 in1 0.08fF
C14 a_15_n33# in2 0.08fF
C15 w_0_0# in2 0.06fF
C16 in3 in2 0.44fF
C17 gnd Gnd 0.28fF
C18 out Gnd 0.12fF
C19 vdd Gnd 0.16fF
C20 a_15_n33# Gnd 0.43fF
C21 in3 Gnd 0.34fF
C22 in2 Gnd 0.30fF
C23 in1 Gnd 0.27fF
C24 w_0_0# Gnd 1.37fF
```

5.1.6.2 Simulations Results



5.1.7 4-Input OR Gate

5.1.7.1 Layout

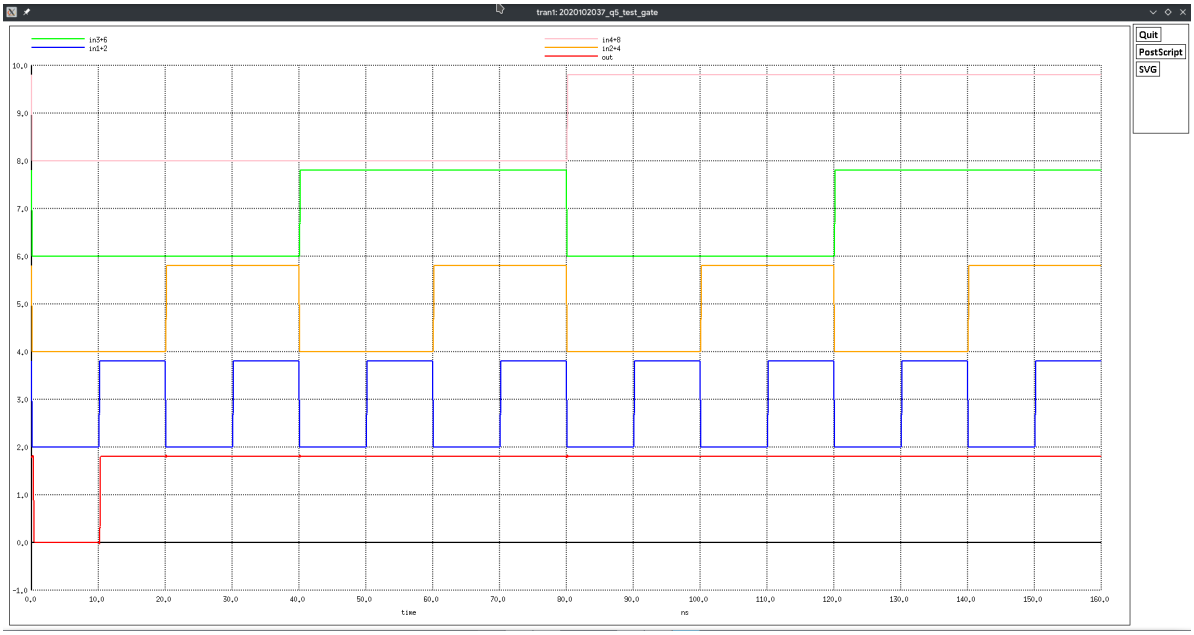


5.1.7.2 Netlist

```
* SPICE3 file created from or4.ext - technology: scmos

.option scale=0.09u

M1000 out a_15_n40# vdd w_0_0# pfet w=8 l=2
+  ad=40 pd=26 as=96 ps=56
M1001 a_15_n40# in1 gnd Gnd nfet w=4 l=2
+  ad=80 pd=56 as=116 ps=90
M1002 a_15_6# in1 vdd w_0_0# pfet w=8 l=2
+  ad=80 pd=36 as=0 ps=0
M1003 gnd in2 a_15_n40# Gnd nfet w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1004 a_27_6# in2 a_15_6# w_0_0# pfet w=8 l=2
+  ad=80 pd=36 as=0 ps=0
M1005 a_39_6# in3 a_27_6# w_0_0# pfet w=8 l=2
+  ad=80 pd=36 as=0 ps=0
M1006 a_15_n40# in3 gnd Gnd nfet w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1007 a_15_n40# in4 a_39_6# w_0_0# pfet w=8 l=2
+  ad=56 pd=30 as=0 ps=0
M1008 out a_15_n40# gnd Gnd nfet w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1009 gnd in4 a_15_n40# Gnd nfet w=4 l=2
+  ad=0 pd=0 as=0 ps=0
C0 in3 in1 0.08fF
C1 a_15_n40# in2 0.08fF
```

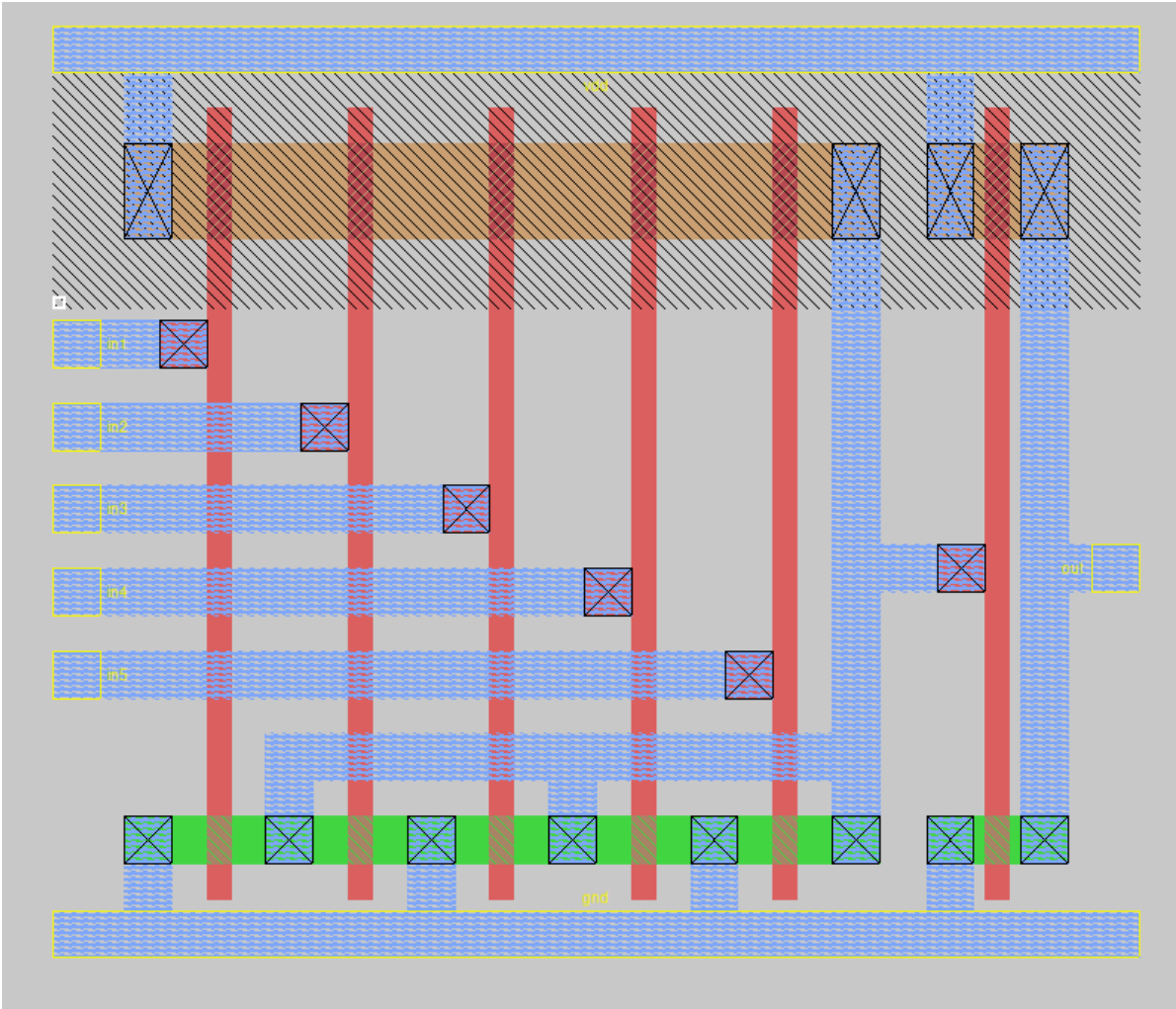
```
C2 a_15_n40# vdd 0.11fF
C3 in4 in1 0.08fF
C4 w_0_0# in1 0.06fF
C5 out vdd 0.11fF
C6 in1 in2 0.27fF
C7 out a_15_n40# 0.05fF
C8 in1 vdd 0.02fF
C9 in3 in4 0.60fF
C10 w_0_0# in3 0.06fF
C11 w_0_0# in4 0.06fF
C12 gnd a_15_n40# 0.19fF
C13 in3 in2 0.44fF
C14 out gnd 0.08fF
C15 in4 in2 0.08fF
C16 w_0_0# in2 0.06fF
C17 w_0_0# vdd 0.14fF
C18 in3 a_15_n40# 0.08fF
C19 in4 a_15_n40# 0.54fF
C20 w_0_0# a_15_n40# 0.10fF
C21 w_0_0# out 0.03fF
C22 gnd Gnd 0.33fF
C23 out Gnd 0.15fF
C24 vdd Gnd 0.19fF
C25 a_15_n40# Gnd 0.52fF
C26 in4 Gnd 0.41fF
C27 in3 Gnd 0.38fF
C28 in2 Gnd 0.34fF
C29 in1 Gnd 0.31fF
C30 w_0_0# Gnd 1.61fF
```

5.1.7.2 Simulations Results



5.1.8 5-Input OR Gate

5.1.8.1 Layout

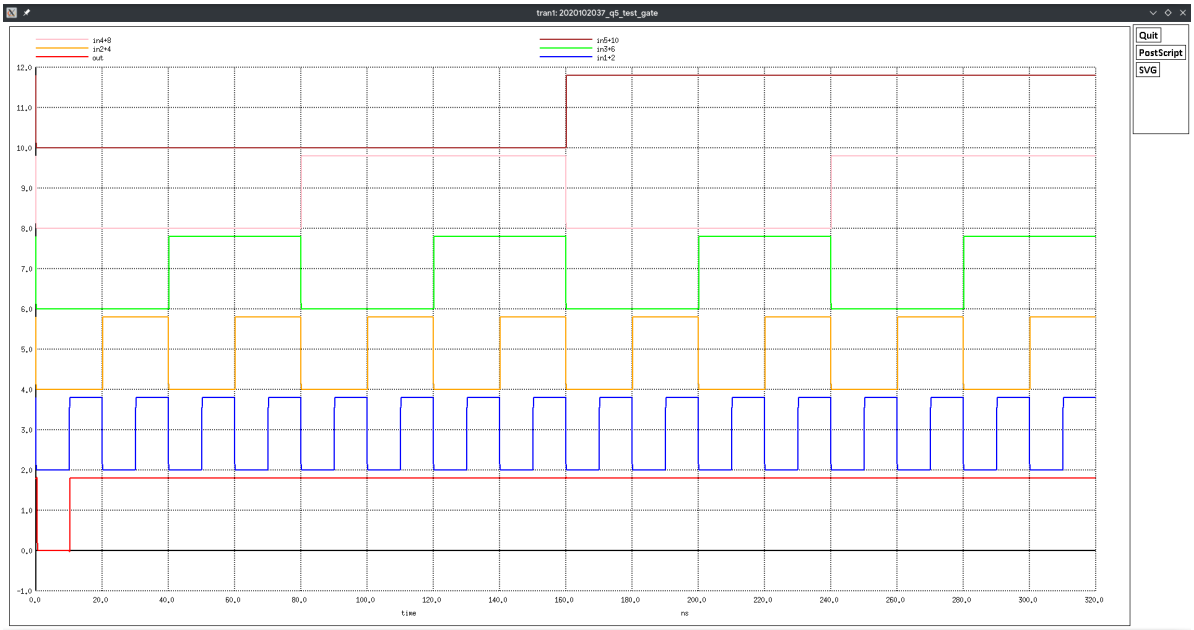


5.1.8.2 Netlist

```
* SPICE3 file created from or5.ext - technology: scmos

.option scale=0.09u

M1000 a_15_n47# in3 gnd Gnd nfet w=4 l=2
+  ad=108 pd=78 as=128 ps=96
M1001 out a_15_n47# vdd w_0_0# pfet w=8 l=2
+  ad=40 pd=26 as=96 ps=56
M1002 a_15_n47# in5 a_51_6# w_0_0# pfet w=8 l=2
+  ad=56 pd=30 as=80 ps=36
M1003 a_15_6# in1 vdd w_0_0# pfet w=8 l=2
+  ad=80 pd=36 as=0 ps=0
M1004 gnd in4 a_15_n47# Gnd nfet w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1005 a_27_6# in2 a_15_6# w_0_0# pfet w=8 l=2
+  ad=80 pd=36 as=0 ps=0
M1006 out a_15_n47# gnd Gnd nfet w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1007 a_39_6# in3 a_27_6# w_0_0# pfet w=8 l=2
+  ad=80 pd=36 as=0 ps=0
M1008 a_51_6# in4 a_39_6# w_0_0# pfet w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1009 a_15_n47# in1 gnd Gnd nfet w=4 l=2
+  ad=0 pd=0 as=0 ps=0
```

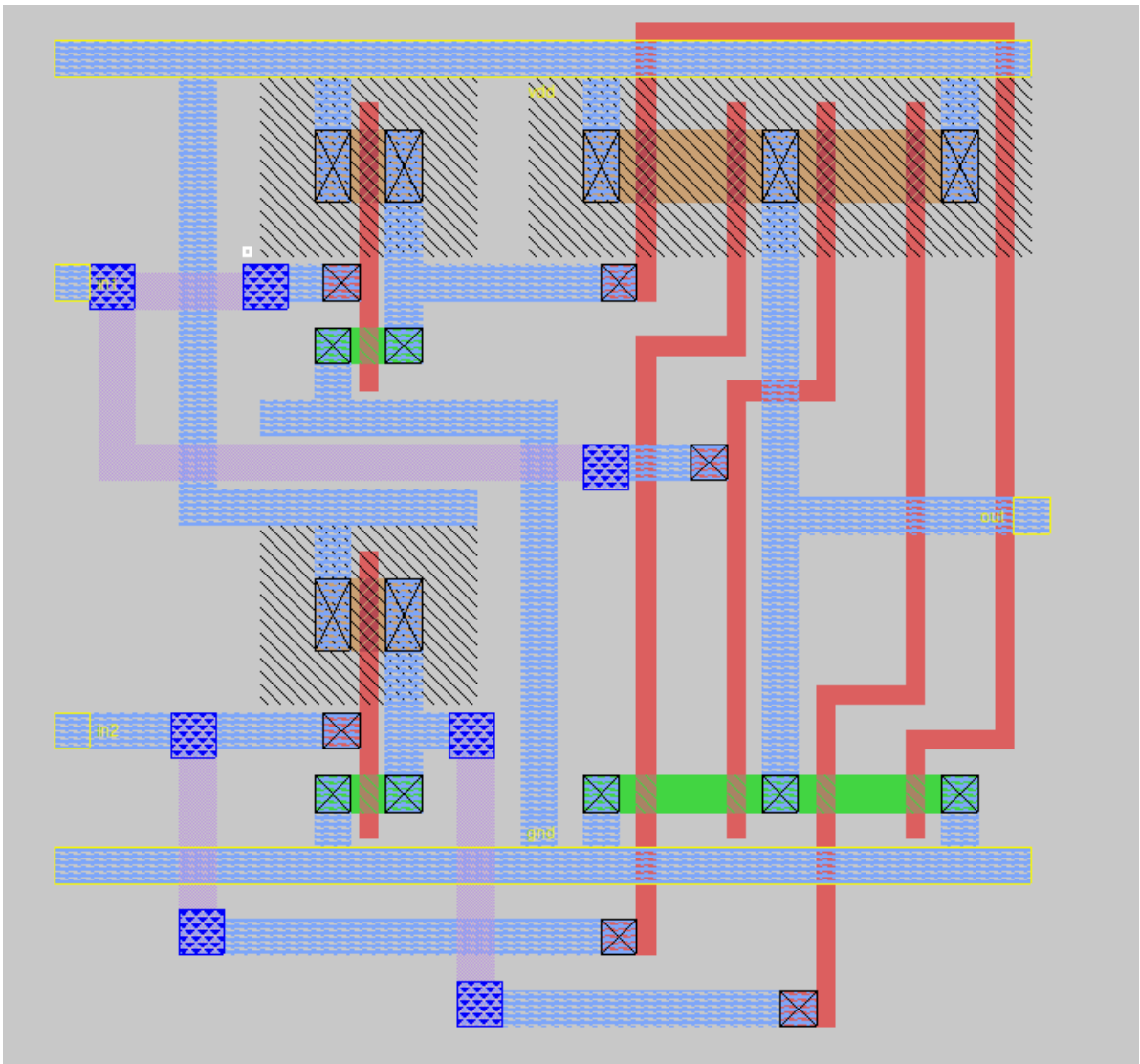
```
M1010 a_15_n47# in5 gnd Gnd nfet w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1011 gnd in2 a_15_n47# Gnd nfet w=4 l=2
+  ad=0 pd=0 as=0 ps=0
C0 a_15_n47# w_0_0# 0.10fF
C1 vdd w_0_0# 0.15fF
C2 a_15_n47# in5 0.70fF
C3 w_0_0# in3 0.06fF
C4 vdd a_15_n47# 0.11fF
C5 w_0_0# in4 0.06fF
C6 in5 in3 0.08fF
C7 in5 in4 0.77fF
C8 a_15_n47# in3 0.08fF
C9 a_15_n47# in4 0.08fF
C10 a_15_n47# gnd 0.27fF
C11 in3 in4 0.60fF
C12 in2 w_0_0# 0.06fF
C13 in2 in5 0.08fF
C14 a_15_n47# in2 0.08fF
C15 in2 in3 0.44fF
C16 in2 in4 0.08fF
C17 w_0_0# in1 0.06fF
C18 in5 in1 0.08fF
C19 vdd in1 0.02fF
C20 out w_0_0# 0.03fF
C21 in3 in1 0.08fF
C22 in4 in1 0.08fF
C23 a_15_n47# out 0.05fF
C24 vdd out 0.11fF
C25 w_0_0# in5 0.06fF
C26 out gnd 0.08fF
C27 in2 in1 0.27fF
C28 gnd Gnd 0.37fF
C29 out Gnd 0.17fF
C30 vdd Gnd 0.22fF
C31 a_15_n47# Gnd 0.63fF
C32 in5 Gnd 0.48fF
C33 in4 Gnd 0.45fF
C34 in3 Gnd 0.42fF
C35 in2 Gnd 0.38fF
C36 in1 Gnd 0.35fF
C37 w_0_0# Gnd 1.85fF
```

5.1.8.2 Simulations Results



5.1.9 2-Input XOR Gate

5.1.9.1 Layout

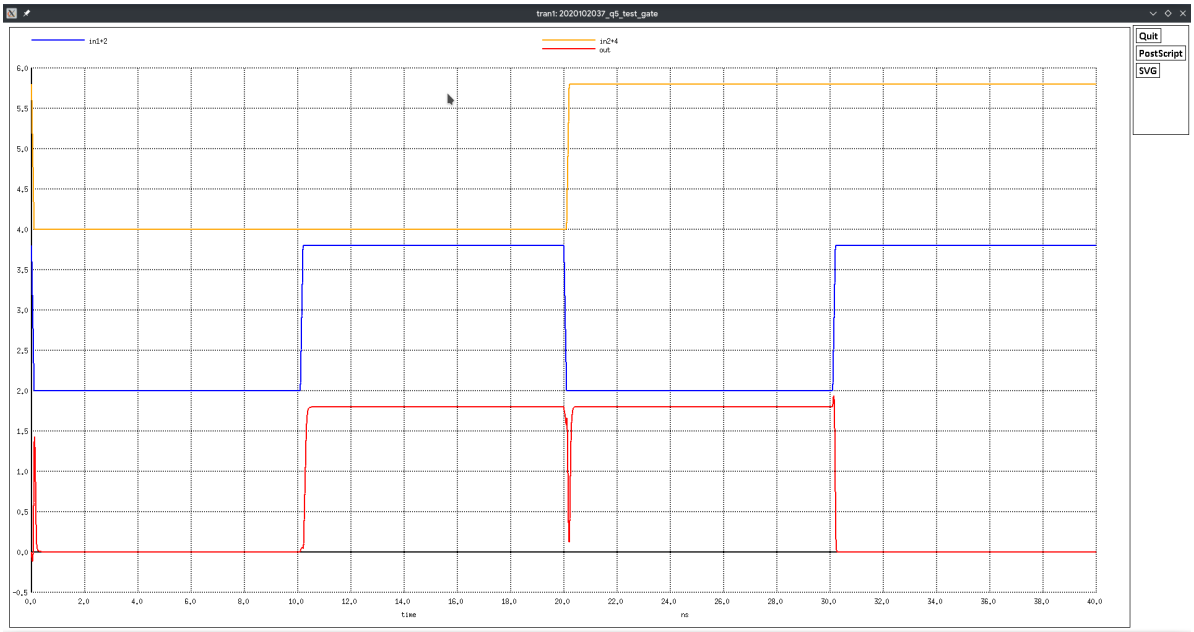


5.1.9.2 Netlist

```
* SPICE3 file created from xor2.ext - technology: scmos

.option scale=0.09u

M1000 a_66_6# in1 out w_32_0# pfet w=8 l=2
+  ad=64 pd=32 as=64 ps=32
M1001 a_15_n12# in1 gnd Gnd nfet w=4 l=2
+  ad=20 pd=18 as=88 ps=76
M1002 out in1 a_46_n62# Gnd nfet w=4 l=2
+  ad=32 pd=24 as=32 ps=24
M1003 a_15_n12# in1 vdd w_2_0# pfet w=8 l=2
+  ad=40 pd=26 as=176 ps=108
M1004 vdd a_15_n62# a_66_6# w_32_0# pfet w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1005 a_15_n62# in2 vdd w_2_n50# pfet w=8 l=2
+  ad=40 pd=26 as=0 ps=0
M1006 a_46_n62# in2 gnd Gnd nfet w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1007 gnd a_15_n12# a_66_n62# Gnd nfet w=4 l=2
+  ad=0 pd=0 as=32 ps=24
M1008 a_15_n62# in2 gnd Gnd nfet w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1009 a_46_6# a_15_n12# vdd w_32_0# pfet w=8 l=2
+  ad=64 pd=32 as=0 ps=0
M1010 a_66_n62# a_15_n62# out Gnd nfet w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1011 out in2 a_46_6# w_32_0# pfet w=8 l=2
+  ad=0 pd=0 as=0 ps=0
C0 a_15_n62# out 0.08fF
C1 a_15_n12# in2 0.02fF
C2 a_15_n12# a_15_n62# 0.02fF
C3 w_2_0# in1 0.06fF
C4 in2 vdd 0.02fF
C5 a_15_n62# vdd 0.11fF
C6 in2 a_15_n62# 0.36fF
C7 in1 w_32_0# 0.06fF
C8 w_2_0# a_15_n12# 0.03fF
C9 w_32_0# out 0.02fF
C10 in1 gnd 0.21fF
C11 w_2_0# vdd 0.05fF
C12 a_15_n12# w_32_0# 0.19fF
C13 in1 out 0.12fF
C14 gnd out 0.04fF
C15 in1 a_15_n12# 0.06fF
C16 w_2_n50# vdd 0.05fF
C17 vdd w_32_0# 0.11fF
C18 a_15_n12# gnd 0.08fF
C19 w_2_n50# in2 0.06fF
C20 in2 w_32_0# 0.06fF
C21 a_15_n12# out 0.08fF
C22 w_2_n50# a_15_n62# 0.03fF
C23 in1 vdd 0.30fF
C24 a_15_n62# w_32_0# 0.06fF
C25 gnd vdd 0.23fF
C26 in1 in2 0.11fF
```

```
C27 in2 gnd 0.76fF
C28 vdd out 0.03fF
C29 gnd a_15_n62# 0.31fF
C30 a_15_n12# vdd 0.74fF
C31 gnd Gnd 0.64fF
C32 out Gnd 0.23fF
C33 vdd Gnd 0.17fF
C34 a_15_n62# Gnd 0.26fF
C35 in2 Gnd 0.39fF
C36 in1 Gnd 1.62fF
C37 a_15_n12# Gnd 0.17fF
C38 w_2_n50# Gnd 0.48fF
C39 w_32_0# Gnd 1.12fF
C40 w_2_0# Gnd 0.48fF
```

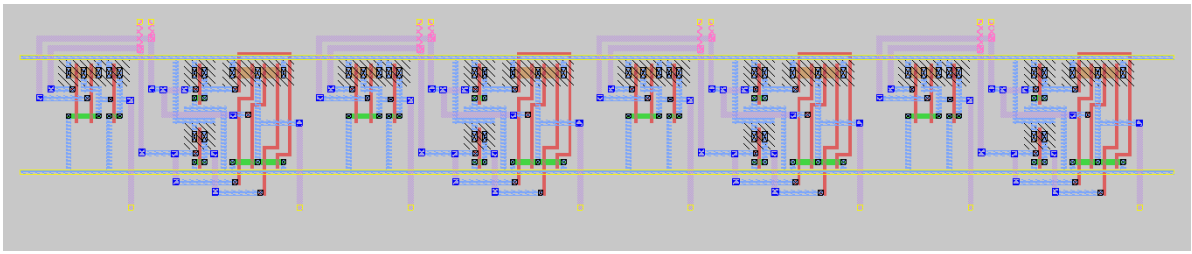
5.1.9.2 Simulations Results



5.2 Blocks

5.2.1 Carry Propogate and Carry Generate Block

5.2.1.1 Layout



5.2.1.2 Netlist

```
.include ../../../TSMC_180nm.txt

** Parameters **
.param VSupply=1.8
.global vdd gnd
```

```
** Input Voltages **
VS vdd gnd VSupply

.param HIGH=VSupply
.param LOW=0

* A = a3 a2 a1 a0
VA0 a0 gnd pulse LOW  HIGH 0 100p 100p 40n 80n
VA1 a1 gnd pulse HIGH LOW  0 100p 100p 10n 20n
VA2 a2 gnd pulse HIGH LOW  0 100p 100p 20n 40n
VA3 a3 gnd pulse LOW  HIGH 0 100p 100p 20n 40n

* B = b3 b2 b1 b0
VB0 b0 gnd pulse HIGH LOW  0 100p 100p 40n 80n
VB1 b1 gnd pulse LOW  HIGH 0 100p 100p 20n 40n
VB2 b2 gnd pulse LOW  HIGH 0 100p 100p 10n 20n
VB3 b3 gnd pulse HIGH LOW  0 100p 100p 10n 20n

* Carry-In = c0
VC0 c0 gnd pulse HIGH LOW  0 100p 100p 20n 40n

** Circuit Description **
.option scale=0.09u
M1000 a_829_92# a3 vdd w_814_86# CMOSP w=8 l=2
+  ad=80 pd=36 as=1312 ps=776
M1001 gnd a_266_74# a_317_24# Gnd CMOSN w=4 l=2
+  ad=544 pd=464 as=32 ps=24
M1002 a_169_92# b0 a_169_60# Gnd CMOSN w=4 l=2
+  ad=28 pd=22 as=40 ps=28
M1003 vdd a_486_24# a_537_92# w_503_86# CMOSP w=8 l=2
+  ad=0 pd=0 as=64 ps=32
M1004 a_757_24# a_706_24# p2 Gnd CMOSN w=4 l=2
+  ad=32 pd=24 as=32 ps=24
M1005 a_926_24# a3 gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1006 a_169_92# a0 vdd w_154_86# CMOSP w=8 l=2
+  ad=80 pd=36 as=0 ps=0
M1007 vdd b1 a_389_92# w_374_86# CMOSP w=8 l=2
+  ad=0 pd=0 as=80 ps=36
M1008 a_609_92# b2 a_609_60# Gnd CMOSN w=4 l=2
+  ad=28 pd=22 as=40 ps=28
M1009 a_977_92# b3 p3 w_943_86# CMOSP w=8 l=2
+  ad=64 pd=32 as=64 ps=32
M1010 a_609_92# a2 vdd w_594_86# CMOSP w=8 l=2
+  ad=80 pd=36 as=0 ps=0
M1011 vdd b3 a_829_92# w_814_86# CMOSP w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1012 g3 a_829_92# gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1013 a_266_24# a0 gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1014 vdd a_266_24# a_317_92# w_283_86# CMOSP w=8 l=2
+  ad=0 pd=0 as=64 ps=32
M1015 a_486_74# b1 vdd w_473_86# CMOSP w=8 l=2
+  ad=40 pd=26 as=0 ps=0
M1016 a_706_24# a2 gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1017 vdd b0 a_169_92# w_154_86# CMOSP w=8 l=2
```

```
+  ad=0 pd=0 as=0 ps=0
M1018 g0 a_169_92# gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1019 a_757_92# b2 p2 w_723_86# CMOSP w=8 l=2
+  ad=64 pd=32 as=64 ps=32
M1020 a_926_74# b3 vdd w_913_86# CMOSP w=8 l=2
+  ad=40 pd=26 as=0 ps=0
M1021 a_537_24# a_486_24# p1 Gnd CMOSN w=4 l=2
+  ad=32 pd=24 as=32 ps=24
M1022 vdd b2 a_609_92# w_594_86# CMOSP w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1023 g2 a_609_92# gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1024 p3 b3 a_957_24# Gnd CMOSN w=4 l=2
+  ad=32 pd=24 as=32 ps=24
M1025 a_266_74# b0 vdd w_253_86# CMOSP w=8 l=2
+  ad=40 pd=26 as=0 ps=0
M1026 g3 a_829_92# vdd w_814_86# CMOSP w=8 l=2
+  ad=40 pd=26 as=0 ps=0
M1027 a_706_74# b2 vdd w_693_86# CMOSP w=8 l=2
+  ad=40 pd=26 as=0 ps=0
M1028 a_317_24# a_266_24# p0 Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=32 ps=24
M1029 g0 a_169_92# vdd w_154_86# CMOSP w=8 l=2
+  ad=40 pd=26 as=0 ps=0
M1030 a_537_92# b1 p1 w_503_86# CMOSP w=8 l=2
+  ad=0 pd=0 as=64 ps=32
M1031 p2 b2 a_737_24# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=32 ps=24
M1032 g1 a_389_92# gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1033 p3 a3 a_957_92# w_943_86# CMOSP w=8 l=2
+  ad=0 pd=0 as=64 ps=32
M1034 g2 a_609_92# vdd w_594_86# CMOSP w=8 l=2
+  ad=40 pd=26 as=0 ps=0
M1035 a_317_92# b0 p0 w_283_86# CMOSP w=8 l=2
+  ad=0 pd=0 as=64 ps=32
M1036 p2 a2 a_737_92# w_723_86# CMOSP w=8 l=2
+  ad=0 pd=0 as=64 ps=32
M1037 p1 b1 a_517_24# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=32 ps=24
M1038 g1 a_389_92# vdd w_374_86# CMOSP w=8 l=2
+  ad=40 pd=26 as=0 ps=0
M1039 a_486_74# b1 gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1040 a_957_24# a3 gnd Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1041 a_926_74# b3 gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1042 a_297_24# a0 gnd Gnd CMOSN w=4 l=2
+  ad=32 pd=24 as=0 ps=0
M1043 p0 b0 a_297_24# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1044 p1 a1 a_517_92# w_503_86# CMOSP w=8 l=2
+  ad=0 pd=0 as=64 ps=32
M1045 a_737_24# a2 gnd Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1046 a_266_74# b0 gnd Gnd CMOSN w=4 l=2
```

```
+  ad=20 pd=18 as=0 ps=0
M1047 a_957_92# a_926_74# vdd w_943_86# CMOSP w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1048 a_706_74# b2 gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1049 a_297_92# a_266_74# vdd w_283_86# CMOSP w=8 l=2
+  ad=64 pd=32 as=0 ps=0
M1050 p0 a0 a_297_92# w_283_86# CMOSP w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1051 a_486_24# a1 vdd w_473_36# CMOSP w=8 l=2
+  ad=40 pd=26 as=0 ps=0
M1052 a_517_24# a1 gnd Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1053 gnd a_926_74# a_977_24# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=32 ps=24
M1054 a_737_92# a_706_74# vdd w_723_86# CMOSP w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1055 a_926_24# a3 vdd w_913_36# CMOSP w=8 l=2
+  ad=40 pd=26 as=0 ps=0
M1056 a_266_24# a0 vdd w_253_36# CMOSP w=8 l=2
+  ad=40 pd=26 as=0 ps=0
M1057 a_517_92# a_486_74# vdd w_503_86# CMOSP w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1058 gnd a_706_74# a_757_24# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1059 a_389_60# a1 gnd Gnd CMOSN w=4 l=2
+  ad=40 pd=28 as=0 ps=0
M1060 a_706_24# a2 vdd w_693_36# CMOSP w=8 l=2
+  ad=40 pd=26 as=0 ps=0
M1061 vdd a_926_24# a_977_92# w_943_86# CMOSP w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1062 a_829_60# a3 gnd Gnd CMOSN w=4 l=2
+  ad=40 pd=28 as=0 ps=0
M1063 gnd a_486_74# a_537_24# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1064 a_169_60# a0 gnd Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1065 a_389_92# b1 a_389_60# Gnd CMOSN w=4 l=2
+  ad=28 pd=22 as=0 ps=0
M1066 vdd a_706_24# a_757_92# w_723_86# CMOSP w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1067 a_977_24# a_926_24# p3 Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1068 a_389_92# a1 vdd w_374_86# CMOSP w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1069 a_829_92# b3 a_829_60# Gnd CMOSN w=4 l=2
+  ad=28 pd=22 as=0 ps=0
M1070 a_609_60# a2 gnd Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1071 a_486_24# a1 gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
C0 w_723_86# b2 0.06fF
C1 a_486_74# gnd 0.08fF
C2 p1 w_503_86# 0.02fF
C3 b0 p0 0.12fF
C4 a_609_92# b2 0.21fF
C5 vdd a_169_92# 0.05fF
C6 a1 w_503_86# 0.06fF
```

```
C7 gnd a_926_74# 0.08fF
C8 a_609_92# gnd 0.04fF
C9 vdd p2 0.03fF
C10 a3 gnd 0.76fF
C11 a0 b0 0.97fF
C12 w_283_86# a_266_74# 0.19fF
C13 a3 w_913_36# 0.06fF
C14 b3 gnd 0.21fF
C15 w_253_86# a_266_74# 0.03fF
C16 p3 gnd 0.13fF
C17 p0 gnd 0.13fF
C18 w_814_86# g3 0.03fF
C19 a_486_74# p1 0.08fF
C20 vdd w_503_86# 0.11fF
C21 b2 a_706_74# 0.06fF
C22 a_926_24# a_926_74# 0.02fF
C23 a3 a_926_24# 0.36fF
C24 a_706_24# gnd 0.31fF
C25 a_609_92# w_594_86# 0.09fF
C26 a0 gnd 0.76fF
C27 w_374_86# a1 0.06fF
C28 a_486_74# a1 0.02fF
C29 a_706_74# gnd 0.08fF
C30 w_913_86# a_926_74# 0.03fF
C31 a3 g3 0.12fF
C32 w_283_86# a_266_24# 0.06fF
C33 g1 a_389_92# 0.05fF
C34 a_926_24# p3 0.08fF
C35 g0 gnd 0.13fF
C36 w_283_86# vdd 0.11fF
C37 w_913_86# b3 0.06fF
C38 vdd w_253_86# 0.05fF
C39 w_693_86# a_706_74# 0.03fF
C40 a2 w_723_86# 0.06fF
C41 w_473_36# a1 0.06fF
C42 b1 a_389_92# 0.21fF
C43 vdd w_374_86# 0.14fF
C44 a_266_74# p0 0.08fF
C45 a_486_74# vdd 0.74fF
C46 w_693_36# a2 0.06fF
C47 vdd w_814_86# 0.14fF
C48 a2 a_609_92# 0.03fF
C49 vdd w_723_86# 0.11fF
C50 gnd a_389_92# 0.04fF
C51 a_486_24# gnd 0.31fF
C52 a0 a_266_74# 0.02fF
C53 w_473_86# b1 0.06fF
C54 a_829_92# gnd 0.04fF
C55 a_926_24# w_943_86# 0.06fF
C56 a0 w_154_86# 0.06fF
C57 g2 gnd 0.13fF
C58 w_693_36# vdd 0.05fF
C59 g1 gnd 0.13fF
C60 vdd a_926_74# 0.74fF
C61 vdd a_609_92# 0.05fF
C62 a3 vdd 0.22fF
C63 w_473_36# vdd 0.05fF
C64 b0 gnd 0.21fF
```

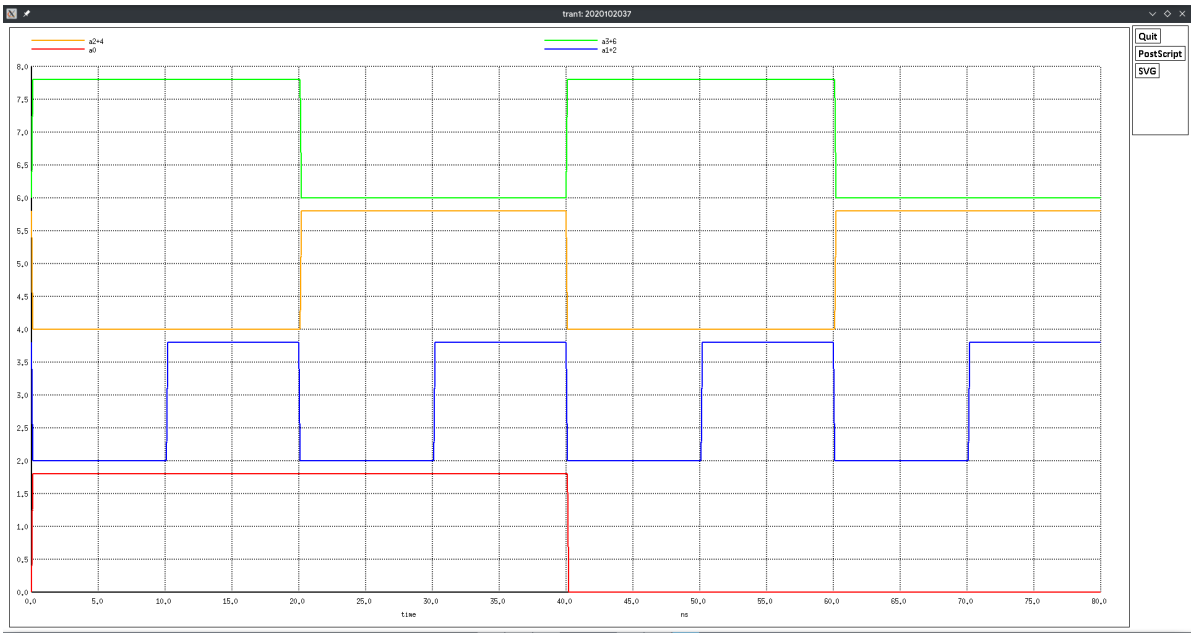
```
C65 vdd b3 0.48fF
C66 g0 w_154_86# 0.03fF
C67 p0 a_266_24# 0.08fF
C68 a2 a_706_24# 0.36fF
C69 p2 w_723_86# 0.02fF
C70 vdd p3 0.03fF
C71 vdd p0 0.03fF
C72 b1 gnd 0.21fF
C73 a2 a_706_74# 0.02fF
C74 b2 gnd 0.21fF
C75 a0 a_266_24# 0.36fF
C76 g2 w_594_86# 0.03fF
C77 vdd a_706_24# 0.11fF
C78 a0 vdd 0.22fF
C79 a_486_74# w_503_86# 0.19fF
C80 a_829_92# g3 0.05fF
C81 vdd a_706_74# 0.74fF
C82 a_486_24# p1 0.08fF
C83 w_693_86# b2 0.06fF
C84 a_266_24# w_253_36# 0.03fF
C85 vdd g0 0.11fF
C86 a1 a_389_92# 0.03fF
C87 b0 a_266_74# 0.06fF
C88 a_486_24# a1 0.36fF
C89 vdd w_253_36# 0.05fF
C90 b2 w_594_86# 0.06fF
C91 b0 w_154_86# 0.06fF
C92 vdd w_943_86# 0.11fF
C93 a0 a_169_92# 0.03fF
C94 g1 a1 0.12fF
C95 p2 a_706_24# 0.08fF
C96 a_926_24# gnd 0.31fF
C97 g2 a2 0.12fF
C98 w_913_36# a_926_24# 0.03fF
C99 p1 b1 0.12fF
C100 p2 a_706_74# 0.08fF
C101 g3 gnd 0.13fF
C102 g0 a_169_92# 0.05fF
C103 vdd a_389_92# 0.05fF
C104 a_486_24# vdd 0.11fF
C105 a1 b1 0.97fF
C106 a_266_74# gnd 0.08fF
C107 p1 gnd 0.13fF
C108 vdd a_829_92# 0.05fF
C109 vdd g2 0.11fF
C110 vdd g1 0.11fF
C111 vdd b0 0.48fF
C112 a2 b2 0.97fF
C113 a1 gnd 0.76fF
C114 vdd w_473_86# 0.05fF
C115 w_283_86# p0 0.02fF
C116 a3 w_814_86# 0.06fF
C117 a2 gnd 0.76fF
C118 vdd b1 0.48fF
C119 w_814_86# b3 0.06fF
C120 vdd b2 0.48fF
C121 a0 w_283_86# 0.06fF
C122 a_266_24# gnd 0.31fF
```

```
C123 b0 a_169_92# 0.21fF
C124 a3 a_926_74# 0.02fF
C125 vdd gnd 0.92fF
C126 b3 a_926_74# 0.06fF
C127 vdd w_913_36# 0.05fF
C128 a3 b3 0.97fF
C129 a2 w_594_86# 0.06fF
C130 w_723_86# a_706_24# 0.06fF
C131 p3 a_926_74# 0.08fF
C132 a_486_24# w_503_86# 0.06fF
C133 vdd w_693_86# 0.05fF
C134 p2 b2 0.12fF
C135 w_723_86# a_706_74# 0.19fF
C136 b3 p3 0.12fF
C137 w_693_36# a_706_24# 0.03fF
C138 a_169_92# gnd 0.04fF
C139 vdd a_926_24# 0.11fF
C140 vdd w_594_86# 0.14fF
C141 p2 gnd 0.13fF
C142 vdd g3 0.11fF
C143 w_913_86# vdd 0.05fF
C144 a_266_74# a_266_24# 0.02fF
C145 b1 w_503_86# 0.06fF
C146 vdd a_266_74# 0.74fF
C147 vdd p1 0.03fF
C148 w_283_86# b0 0.06fF
C149 vdd w_154_86# 0.14fF
C150 w_374_86# a_389_92# 0.09fF
C151 w_943_86# a_926_74# 0.19fF
C152 b0 w_253_86# 0.06fF
C153 a_486_74# a_486_24# 0.02fF
C154 a3 w_943_86# 0.06fF
C155 vdd a1 0.22fF
C156 a_829_92# w_814_86# 0.09fF
C157 w_374_86# g1 0.03fF
C158 b3 w_943_86# 0.06fF
C159 a_706_24# a_706_74# 0.02fF
C160 p3 w_943_86# 0.02fF
C161 vdd a2 0.22fF
C162 a_486_74# w_473_86# 0.03fF
C163 a_169_92# w_154_86# 0.09fF
C164 a0 g0 0.12fF
C165 w_473_36# a_486_24# 0.03fF
C166 w_374_86# b1 0.06fF
C167 vdd a_266_24# 0.11fF
C168 a3 a_829_92# 0.03fF
C169 a_486_74# b1 0.06fF
C170 a0 w_253_36# 0.06fF
C171 g2 a_609_92# 0.05fF
C172 a_829_92# b3 0.21fF
C173 p3 Gnd 1.05fF
C174 g3 Gnd 1.08fF
C175 a_926_24# Gnd 1.09fF
C176 a_829_92# Gnd 0.32fF
C177 b3 Gnd 3.91fF
C178 a3 Gnd 3.51fF
C179 a_926_74# Gnd 0.88fF
C180 p2 Gnd 1.05fF
```

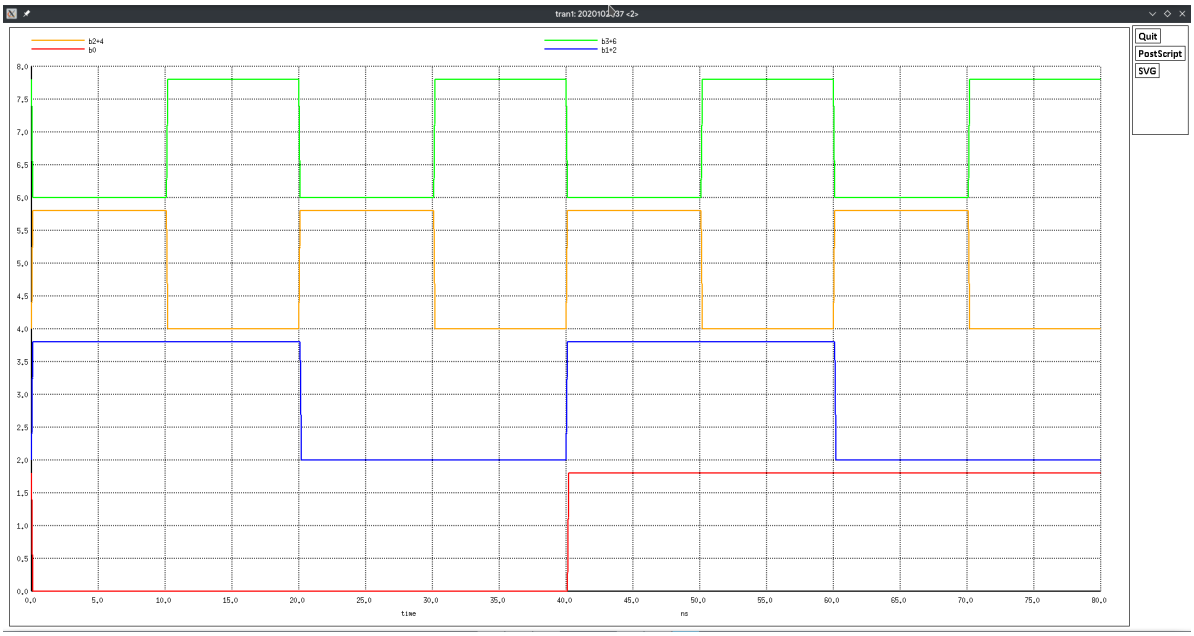
```
C181 g2 Gnd 1.08fF
C182 a_706_24# Gnd 1.09fF
C183 a_609_92# Gnd 0.32fF
C184 b2 Gnd 3.91fF
C185 a2 Gnd 3.51fF
C186 a_706_74# Gnd 0.88fF
C187 p1 Gnd 1.05fF
C188 g1 Gnd 1.08fF
C189 a_486_24# Gnd 1.09fF
C190 a_389_92# Gnd 0.32fF
C191 b1 Gnd 3.91fF
C192 a1 Gnd 3.51fF
C193 a_486_74# Gnd 0.88fF
C194 gnd Gnd 5.30fF
C195 p0 Gnd 1.05fF
C196 g0 Gnd 1.08fF
C197 vdd Gnd 3.17fF
C198 a_266_24# Gnd 1.09fF
C199 a_169_92# Gnd 0.32fF
C200 b0 Gnd 3.91fF
C201 a0 Gnd 3.51fF
C202 a_266_74# Gnd 0.88fF
C203 w_913_36# Gnd 0.48fF
C204 w_693_36# Gnd 0.48fF
C205 w_473_36# Gnd 0.48fF
C206 w_253_36# Gnd 0.48fF
C207 w_943_86# Gnd 1.12fF
C208 w_913_86# Gnd 0.48fF
C209 w_814_86# Gnd 1.12fF
C210 w_723_86# Gnd 1.12fF
C211 w_693_86# Gnd 0.48fF
C212 w_594_86# Gnd 1.12fF
C213 w_503_86# Gnd 1.12fF
C214 w_473_86# Gnd 0.48fF
C215 w_374_86# Gnd 1.12fF
C216 w_283_86# Gnd 1.12fF
C217 w_253_86# Gnd 0.48fF
C218 w_154_86# Gnd 1.12fF

** Analysis **
.tran 1p 80n

** Plotting **
.control
set hcopypscolor=1
set color0=white
set color1=black
run
set curplottitle="2020102037"
plot a0 a1+2 a2+4 a3+6
plot b0 b1+2 b2+4 b3+6
plot p0 p1+2 p2+4 p3+6
plot g0 g1+2 g2+4 g3+6
.endc

.end
```

5.2.1.3 Simulation Results

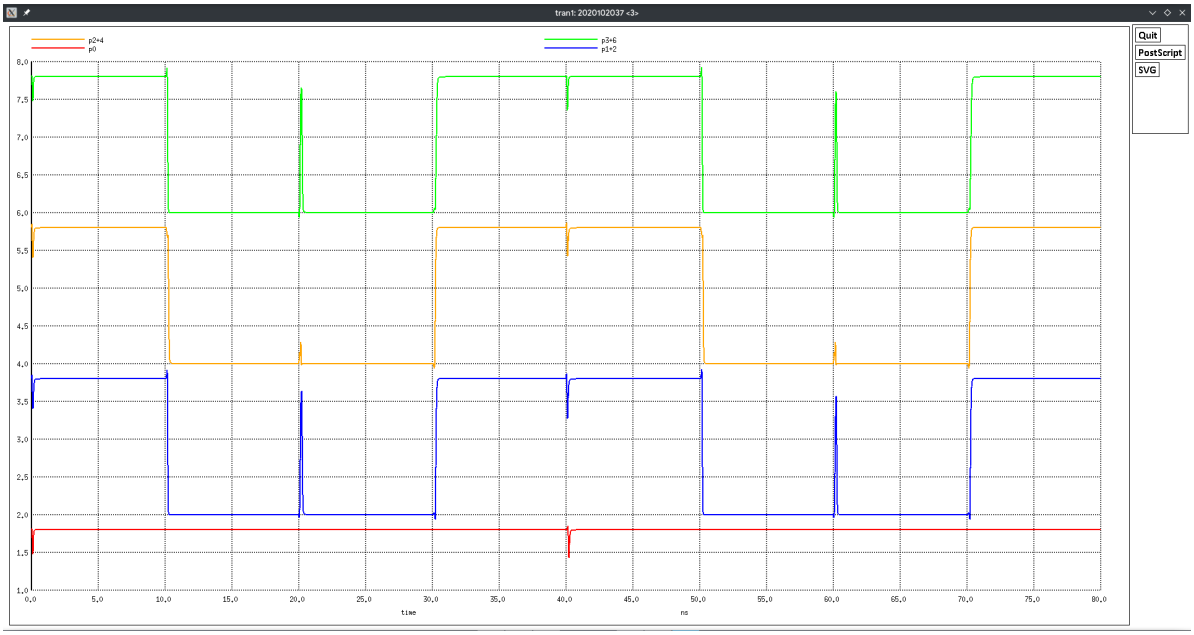
Input A



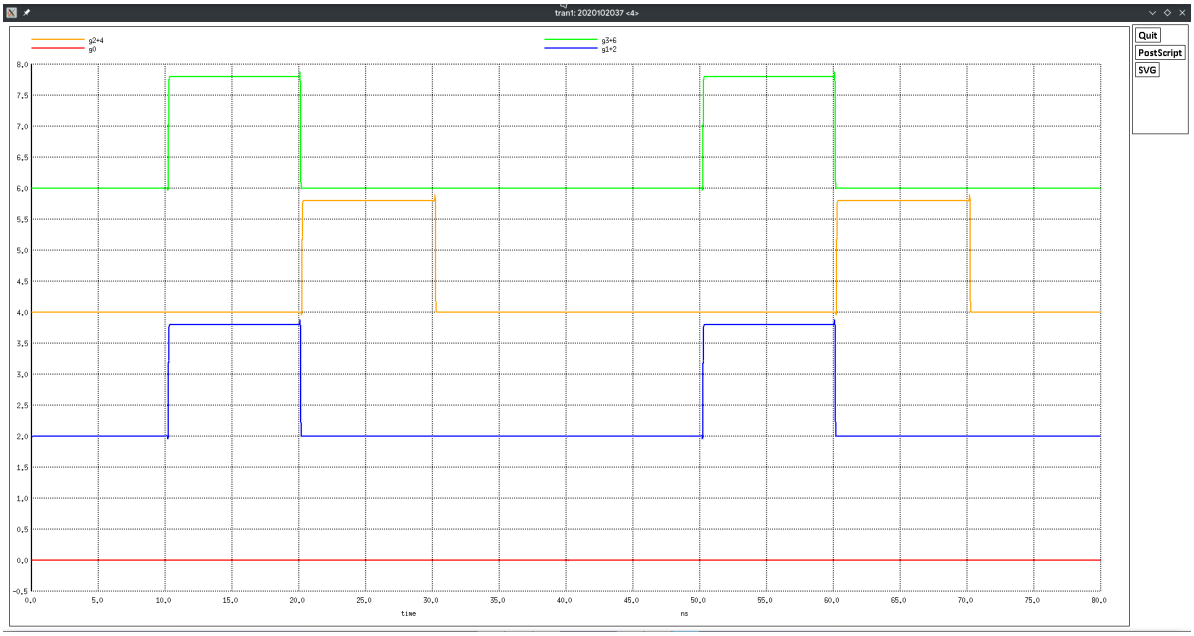
Input B



Output P

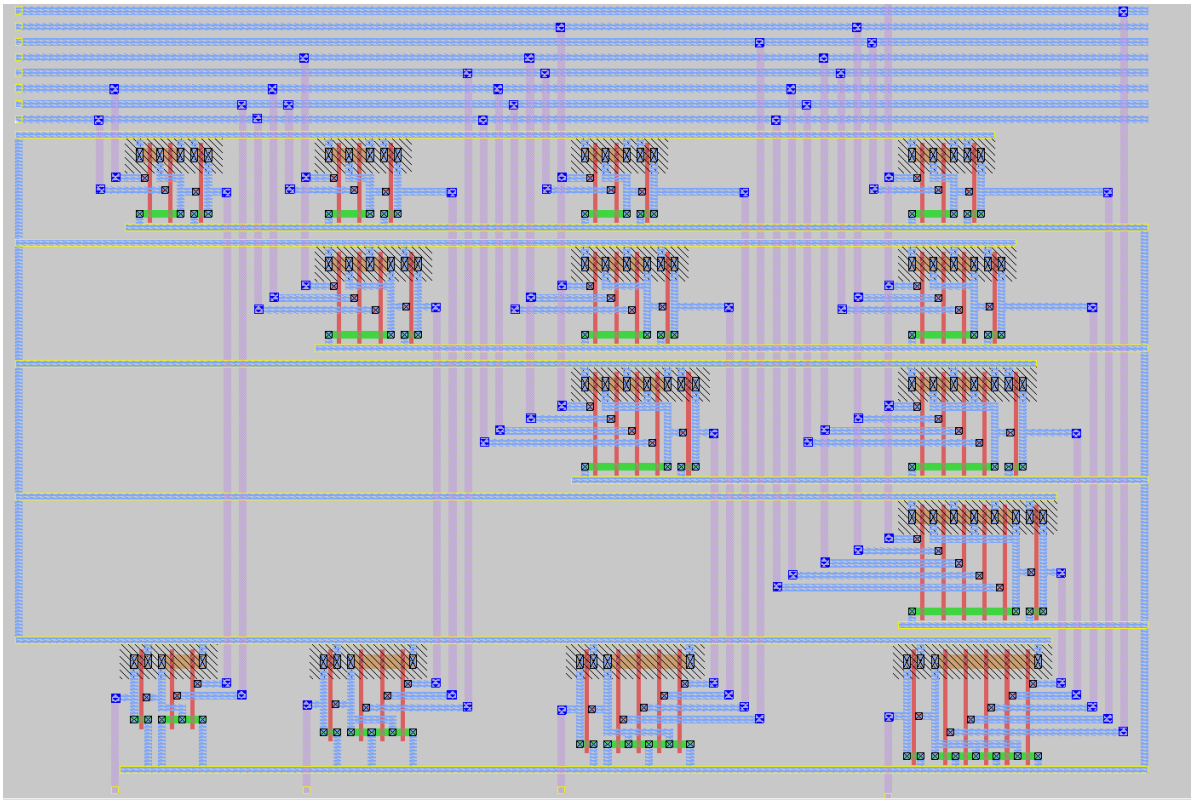


Output G



5.2.2 Carry Lookahead Block

5.2.2.1 Layout



5.2.2.2 Netlist

```
.include ../../../TSMC_180nm.txt


** Parameters **
.param VSupply=1.8
.global vdd gnd

** Input Voltages **
VS vdd gnd VSupply

.param HIGH=VSupply
.param LOW=0

VP0 p0 gnd pulse LOW  HIGH 0 100p 100p 40n 80n
VP1 p1 gnd pulse HIGH LOW  0 100p 100p 10n 20n
VP2 p2 gnd pulse HIGH LOW  0 100p 100p 20n 40n
VP3 p3 gnd pulse LOW  HIGH 0 100p 100p 20n 40n

VG0 g0 gnd pulse HIGH LOW  0 100p 100p 40n 80n
VG1 g1 gnd pulse LOW  HIGH 0 100p 100p 20n 40n
VG2 g2 gnd pulse LOW  HIGH 0 100p 100p 10n 20n
VG3 g3 gnd pulse HIGH LOW  0 100p 100p 10n 20n

VC0 c0 gnd pulse HIGH LOW  0 100p 100p 20n 40n

** Circuit Description **
.option scale=0.09u
M1000 vdd g0 a_528_n156# w_513_n162# CMOSP w=8 l=2
+  ad=2240 pd=1216 as=160 ps=72
M1001 a_189_n55# p1 gnd Gnd CMOSN w=4 l=2
+  ad=40 pd=28 as=888 ps=716
M1002 a_373_n366# a_338_n86# vdd w_323_n92# CMOSP w=8 l=2
```

```
+  ad=40 pd=26 as=0 ps=0
M1003 a_528_n156# g0 a_552_n202# Gnd CMOSN w=4 l=2
+  ad=28 pd=22 as=40 ps=28
M1004 a_385_n366# a_338_n156# vdd w_323_n162# CMOSP w=8 l=2
+  ad=40 pd=26 as=0 ps=0
M1005 gnd a_331_n366# c3 Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=20 ps=18
M1006 vdd a_331_n366# c3 w_320_n323# CMOSP w=8 l=2
+  ad=0 pd=0 as=40 ps=26
M1007 a_212_n359# a_189_n23# vdd w_174_n29# CMOSP w=8 l=2
+  ad=40 pd=26 as=0 ps=0
M1008 a_201_n125# p0 a_189_n125# Gnd CMOSN w=4 l=2
+  ad=40 pd=28 as=40 ps=28
M1009 a_528_n55# p3 gnd Gnd CMOSN w=4 l=2
+  ad=40 pd=28 as=0 ps=0
M1010 a_385_n366# a_338_n156# gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1011 a_575_n373# a_528_n156# vdd w_513_n162# CMOSP w=8 l=2
+  ad=40 pd=26 as=0 ps=0
M1012 gnd a_182_n359# c2 Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=20 ps=18
M1013 vdd a_521_n373# c4 w_510_n323# CMOSP w=8 l=2
+  ad=0 pd=0 as=40 ps=26
M1014 a_528_n286# p3 gnd Gnd CMOSN w=4 l=2
+  ad=40 pd=28 as=0 ps=0
M1015 a_575_n373# a_528_n156# gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1016 a_202_n317# g1 a_182_n359# w_171_n323# CMOSP w=8 l=2
+  ad=80 pd=36 as=56 ps=30
M1017 a_528_n86# g1 vdd w_513_n92# CMOSP w=8 l=2
+  ad=136 pd=66 as=0 ps=0
M1018 a_552_n286# p1 a_540_n286# Gnd CMOSN w=4 l=2
+  ad=40 pd=28 as=40 ps=28
M1019 a_551_n373# a_528_n23# gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1020 a_189_n23# g0 a_189_n55# Gnd CMOSN w=4 l=2
+  ad=28 pd=22 as=0 ps=0
M1021 gnd a_72_n352# c1 Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=20 ps=18
M1022 a_79_n55# p0 gnd Gnd CMOSN w=4 l=2
+  ad=40 pd=28 as=0 ps=0
M1023 a_189_n23# p1 vdd w_174_n29# CMOSP w=8 l=2
+  ad=80 pd=36 as=0 ps=0
M1024 a_521_n373# a_551_n373# gnd Gnd CMOSN w=4 l=2
+  ad=108 pd=78 as=0 ps=0
M1025 a_338_n125# p2 gnd Gnd CMOSN w=4 l=2
+  ad=40 pd=28 as=0 ps=0
M1026 a_528_n233# p3 vdd w_513_n239# CMOSP w=8 l=2
+  ad=216 pd=102 as=0 ps=0
M1027 a_338_n55# p2 gnd Gnd CMOSN w=4 l=2
+  ad=40 pd=28 as=0 ps=0
M1028 a_528_n23# g2 a_528_n55# Gnd CMOSN w=4 l=2
+  ad=28 pd=22 as=0 ps=0
M1029 a_540_n286# p2 a_528_n286# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1030 a_528_n23# p3 vdd w_513_n29# CMOSP w=8 l=2
+  ad=80 pd=36 as=0 ps=0
M1031 a_72_n352# g0 gnd Gnd CMOSN w=4 l=2
```

```
+  ad=40 pd=28 as=0 ps=0
M1032 a_528_n125# p3 gnd Gnd CMOSN w=4 l=2
+  ad=40 pd=28 as=0 ps=0
M1033 a_363_n317# a_361_n366# a_351_n317# w_320_n323# CMOSP w=8 l=2
+  ad=80 pd=36 as=80 ps=36
M1034 a_338_n86# g0 a_350_n125# Gnd CMOSN w=4 l=2
+  ad=28 pd=22 as=40 ps=28
M1035 gnd a_361_n366# a_331_n366# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=80 ps=56
M1036 a_214_n317# a_212_n359# a_202_n317# w_171_n323# CMOSP w=8 l=2
+  ad=80 pd=36 as=0 ps=0
M1037 a_528_n233# p1 vdd w_513_n239# CMOSP w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1038 a_189_n86# c0 a_201_n125# Gnd CMOSN w=4 l=2
+  ad=28 pd=22 as=0 ps=0
M1039 gnd g3 a_521_n373# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1040 a_564_n286# p0 a_552_n286# Gnd CMOSN w=4 l=2
+  ad=40 pd=28 as=0 ps=0
M1041 a_338_n86# g0 vdd w_323_n92# CMOSP w=8 l=2
+  ad=136 pd=66 as=0 ps=0
M1042 a_361_n366# a_338_n23# gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1043 a_553_n317# a_551_n373# a_541_n317# w_510_n323# CMOSP w=8 l=2
+  ad=80 pd=36 as=80 ps=36
M1044 a_528_n86# g1 a_540_n125# Gnd CMOSN w=4 l=2
+  ad=28 pd=22 as=40 ps=28
M1045 a_79_n23# c0 a_79_n55# Gnd CMOSN w=4 l=2
+  ad=28 pd=22 as=0 ps=0
M1046 a_102_n352# a_79_n23# gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1047 gnd a_563_n373# a_521_n373# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1048 a_551_n373# a_528_n23# vdd w_513_n29# CMOSP w=8 l=2
+  ad=40 pd=26 as=0 ps=0
M1049 vdd g0 a_189_n23# w_174_n29# CMOSP w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1050 a_351_n317# g2 a_331_n366# w_320_n323# CMOSP w=8 l=2
+  ad=0 pd=0 as=56 ps=30
M1051 a_350_n125# p1 a_338_n125# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1052 a_331_n366# g2 gnd Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1053 vdd a_72_n352# c1 w_61_n323# CMOSP w=8 l=2
+  ad=0 pd=0 as=40 ps=26
M1054 vdd p2 a_528_n233# w_513_n239# CMOSP w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1055 a_79_n23# p0 vdd w_64_n29# CMOSP w=8 l=2
+  ad=80 pd=36 as=0 ps=0
M1056 gnd a_102_n352# a_72_n352# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1057 a_189_n86# p1 vdd w_174_n92# CMOSP w=8 l=2
+  ad=136 pd=66 as=0 ps=0
M1058 a_338_n23# g1 a_338_n55# Gnd CMOSN w=4 l=2
+  ad=28 pd=22 as=0 ps=0
M1059 a_540_n125# p2 a_528_n125# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1060 a_541_n317# g3 a_521_n373# w_510_n323# CMOSP w=8 l=2
```

```
+  ad=0 pd=0 as=56 ps=30
M1061 a_331_n366# a_373_n366# gnd Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1062 a_375_n317# a_373_n366# a_363_n317# w_320_n323# CMOSP w=8 l=2
+  ad=80 pd=36 as=0 ps=0
M1063 vdd a_224_n359# a_214_n317# w_171_n323# CMOSP w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1064 vdd p0 a_528_n233# w_513_n239# CMOSP w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1065 a_338_n23# p2 vdd w_323_n29# CMOSP w=8 l=2
+  ad=80 pd=36 as=0 ps=0
M1066 vdd g2 a_528_n23# w_513_n29# CMOSP w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1067 a_224_n359# a_189_n86# vdd w_174_n92# CMOSP w=8 l=2
+  ad=40 pd=26 as=0 ps=0
M1068 a_528_n233# c0 a_564_n286# Gnd CMOSN w=4 l=2
+  ad=28 pd=22 as=0 ps=0
M1069 a_92_n317# g0 a_72_n352# w_61_n323# CMOSP w=8 l=2
+  ad=80 pd=36 as=56 ps=30
M1070 a_528_n86# p3 vdd w_513_n92# CMOSP w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1071 a_565_n317# a_563_n373# a_553_n317# w_510_n323# CMOSP w=8 l=2
+  ad=80 pd=36 as=0 ps=0
M1072 a_521_n373# a_575_n373# gnd Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1073 gnd g1 a_182_n359# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=68 ps=50
M1074 a_361_n366# a_338_n23# vdd w_323_n29# CMOSP w=8 l=2
+  ad=40 pd=26 as=0 ps=0
M1075 vdd c0 a_79_n23# w_64_n29# CMOSP w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1076 a_102_n352# a_79_n23# vdd w_64_n29# CMOSP w=8 l=2
+  ad=40 pd=26 as=0 ps=0
M1077 a_587_n373# a_528_n233# gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1078 vdd a_385_n366# a_375_n317# w_320_n323# CMOSP w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1079 vdd p0 a_189_n86# w_174_n92# CMOSP w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1080 gnd a_385_n366# a_331_n366# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1081 a_528_n233# c0 vdd w_513_n239# CMOSP w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1082 vdd a_102_n352# a_92_n317# w_61_n323# CMOSP w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1083 vdd g1 a_338_n23# w_323_n29# CMOSP w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1084 a_373_n366# a_338_n86# gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1085 a_224_n359# a_189_n86# gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1086 a_338_n156# p2 vdd w_323_n162# CMOSP w=8 l=2
+  ad=160 pd=72 as=0 ps=0
M1087 a_577_n317# a_575_n373# a_565_n317# w_510_n323# CMOSP w=8 l=2
+  ad=80 pd=36 as=0 ps=0
M1088 gnd a_587_n373# a_521_n373# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1089 a_182_n359# a_212_n359# gnd Gnd CMOSN w=4 l=2
```

```
+  ad=0 pd=0 as=0 ps=0
M1090 vdd a_182_n359# c2 w_171_n323# CMOSP w=8 l=2
+  ad=0 pd=0 as=40 ps=26
M1091 vdd p2 a_528_n86# w_513_n92# CMOSP w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1092 a_338_n86# p2 vdd w_323_n92# CMOSP w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1093 a_563_n373# a_528_n86# gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1094 a_587_n373# a_528_n233# vdd w_513_n239# CMOSP w=8 l=2
+  ad=40 pd=26 as=0 ps=0
M1095 a_338_n202# p2 gnd Gnd CMOSN w=4 l=2
+  ad=40 pd=28 as=0 ps=0
M1096 a_528_n156# p3 vdd w_513_n162# CMOSP w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1097 a_338_n156# p0 vdd w_323_n162# CMOSP w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1098 a_528_n202# p3 gnd Gnd CMOSN w=4 l=2
+  ad=40 pd=28 as=0 ps=0
M1099 a_362_n202# p0 a_350_n202# Gnd CMOSN w=4 l=2
+  ad=40 pd=28 as=40 ps=28
M1100 a_563_n373# a_528_n86# vdd w_513_n92# CMOSP w=8 l=2
+  ad=40 pd=26 as=0 ps=0
M1101 a_528_n156# p1 vdd w_513_n162# CMOSP w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1102 a_189_n86# c0 vdd w_174_n92# CMOSP w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1103 a_212_n359# a_189_n23# gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1104 vdd a_587_n373# a_577_n317# w_510_n323# CMOSP w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1105 vdd p1 a_338_n156# w_323_n162# CMOSP w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1106 gnd a_224_n359# a_182_n359# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1107 a_552_n202# p1 a_540_n202# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=40 ps=28
M1108 vdd p1 a_338_n86# w_323_n92# CMOSP w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1109 a_350_n202# p1 a_338_n202# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1110 vdd p2 a_528_n156# w_513_n162# CMOSP w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1111 vdd c0 a_338_n156# w_323_n162# CMOSP w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1112 a_189_n125# p1 gnd Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1113 gnd a_521_n373# c4 Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=20 ps=18
M1114 a_540_n202# p2 a_528_n202# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1115 a_338_n156# c0 a_362_n202# Gnd CMOSN w=4 l=2
+  ad=28 pd=22 as=0 ps=0
C0 gnd a_528_n23# 0.08fF
C1 p0 a_528_n233# 0.08fF
C2 g3 g1 0.09fF
C3 p2 a_528_n86# 0.17fF
C4 gnd a_189_n23# 0.08fF
```

```
C5 a_373_n366# w_320_n323# 0.06fF
C6 vdd a_331_n366# 0.11fF
C7 vdd a_189_n86# 0.16fF
C8 a_551_n373# g3 1.90fF
C9 gnd g1 0.26fF
C10 p1 w_323_n92# 0.06fF
C11 g3 c0 0.09fF
C12 vdd g2 0.51fF
C13 vdd w_513_n92# 0.14fF
C14 vdd a_338_n23# 0.05fF
C15 gnd a_551_n373# 0.42fF
C16 g1 a_182_n359# 0.37fF
C17 a_338_n156# p0 0.08fF
C18 gnd c0 0.51fF
C19 gnd c4 0.17fF
C20 a_102_n352# a_79_n23# 0.05fF
C21 vdd w_513_n162# 0.18fF
C22 p2 g2 5.81fF
C23 p2 w_513_n92# 0.06fF
C24 a_521_n373# w_510_n323# 0.10fF
C25 p2 a_338_n23# 0.03fF
C26 a_212_n359# a_189_n23# 0.05fF
C27 a_72_n352# vdd 0.11fF
C28 gnd a_528_n86# 0.08fF
C29 g1 w_171_n323# 0.06fF
C30 gnd a_79_n23# 0.08fF
C31 p0 g0 6.61fF
C32 w_323_n92# a_373_n366# 0.03fF
C33 vdd a_338_n86# 0.16fF
C34 g1 a_212_n359# 1.29fF
C35 p3 a_528_n233# 0.03fF
C36 a_563_n373# a_587_n373# 0.08fF
C37 w_510_n323# a_575_n373# 0.06fF
C38 p2 w_513_n162# 0.06fF
C39 p2 a_338_n86# 0.03fF
C40 a_521_n373# a_551_n373# 0.08fF
C41 g3 g2 0.09fF
C42 gnd a_331_n366# 0.11fF
C43 a_361_n366# a_385_n366# 0.08fF
C44 a_212_n359# w_174_n29# 0.03fF
C45 gnd a_189_n86# 0.08fF
C46 p1 w_323_n162# 0.06fF
C47 c4 a_521_n373# 0.05fF
C48 p0 w_513_n239# 0.06fF
C49 vdd w_174_n92# 0.14fF
C50 a_551_n373# a_575_n373# 0.08fF
C51 p1 vdd 0.82fF
C52 gnd g2 0.26fF
C53 gnd a_338_n23# 0.08fF
C54 w_64_n29# p0 0.06fF
C55 vdd a_528_n156# 0.10fF
C56 p2 p1 2.69fF
C57 p3 g0 0.25fF
C58 c0 a_528_n233# 0.11fF
C59 gnd a_72_n352# 0.05fF
C60 gnd a_338_n86# 0.08fF
C61 w_61_n323# g0 0.06fF
C62 vdd a_373_n366# 0.37fF
```

```
C63 a_224_n359# vdd 0.39fF
C64 p2 a_528_n156# 0.17fF
C65 vdd w_320_n323# 0.14fF
C66 a_563_n373# vdd 0.11fF
C67 p1 g3 0.09fF
C68 g0 a_189_n23# 0.21fF
C69 p3 w_513_n239# 0.06fF
C70 g1 g0 0.26fF
C71 c3 a_331_n366# 0.05fF
C72 gnd p1 0.51fF
C73 a_338_n156# c0 0.11fF
C74 vdd a_587_n373# 0.13fF
C75 p3 p0 0.16fF
C76 a_575_n373# w_513_n162# 0.03fF
C77 c0 g0 6.07fF
C78 g0 w_174_n29# 0.06fF
C79 a_361_n366# w_323_n29# 0.03fF
C80 gnd a_528_n156# 0.08fF
C81 w_323_n92# vdd 0.14fF
C82 gnd a_373_n366# 0.25fF
C83 gnd a_224_n359# 0.17fF
C84 a_563_n373# g3 0.08fF
C85 p2 w_323_n92# 0.06fF
C86 p0 g1 5.71fF
C87 c0 w_513_n239# 0.06fF
C88 gnd a_563_n373# 0.34fF
C89 w_61_n323# c1 0.03fF
C90 a_385_n366# g2 0.08fF
C91 w_64_n29# c0 0.06fF
C92 g3 a_587_n373# 0.08fF
C93 p0 c0 5.62fF
C94 g2 g0 0.17fF
C95 a_224_n359# w_171_n323# 0.06fF
C96 w_64_n29# a_79_n23# 0.09fF
C97 a_224_n359# a_212_n359# 0.85fF
C98 p1 a_528_n233# 0.08fF
C99 g1 w_323_n29# 0.06fF
C100 gnd a_587_n373# 0.17fF
C101 a_528_n156# a_575_n373# 0.05fF
C102 a_79_n23# p0 0.03fF
C103 p3 a_528_n23# 0.03fF
C104 vdd w_323_n162# 0.18fF
C105 g0 w_513_n162# 0.06fF
C106 a_72_n352# g0 0.21fF
C107 a_338_n86# g0 0.11fF
C108 a_521_n373# a_563_n373# 0.08fF
C109 p3 w_513_n29# 0.06fF
C110 p3 g1 0.25fF
C111 p2 w_323_n162# 0.06fF
C112 p0 a_189_n86# 0.17fF
C113 a_563_n373# a_575_n373# 1.00fF
C114 p2 vdd 0.67fF
C115 w_513_n29# a_528_n23# 0.09fF
C116 c3 w_320_n323# 0.03fF
C117 a_338_n156# p1 0.17fF
C118 p0 g2 0.17fF
C119 p3 c0 0.16fF
C120 a_551_n373# a_528_n23# 0.05fF
```

```
C121 a_587_n373# a_575_n373# 0.52fF
C122 p1 g0 3.63fF
C123 p3 a_528_n86# 0.03fF
C124 a_551_n373# w_510_n323# 0.06fF
C125 a_361_n366# a_331_n366# 0.08fF
C126 c4 w_510_n323# 0.03fF
C127 a_102_n352# vdd 0.48fF
C128 a_587_n373# a_528_n233# 0.05fF
C129 a_551_n373# w_513_n29# 0.03fF
C130 a_528_n156# g0 0.11fF
C131 w_323_n29# a_338_n23# 0.09fF
C132 a_385_n366# a_373_n366# 0.69fF
C133 a_361_n366# g2 1.59fF
C134 a_361_n366# a_338_n23# 0.05fF
C135 w_174_n29# a_189_n23# 0.09fF
C136 gnd vdd 10.78fF
C137 g1 c0 0.66fF
C138 p2 g3 5.52fF
C139 p1 w_513_n239# 0.06fF
C140 a_385_n366# w_320_n323# 0.06fF
C141 a_528_n86# g1 0.11fF
C142 vdd a_182_n359# 0.11fF
C143 p3 g2 0.74fF
C144 gnd p2 0.43fF
C145 p0 w_174_n92# 0.06fF
C146 a_72_n352# c1 0.05fF
C147 p3 w_513_n92# 0.06fF
C148 p1 p0 2.65fF
C149 g2 a_528_n23# 0.21fF
C150 vdd w_171_n323# 0.12fF
C151 vdd a_212_n359# 0.45fF
C152 a_79_n23# c0 0.21fF
C153 p3 w_513_n162# 0.06fF
C154 a_521_n373# vdd 0.11fF
C155 a_72_n352# w_61_n323# 0.10fF
C156 gnd g3 0.34fF
C157 w_513_n29# g2 0.06fF
C158 gnd a_102_n352# 0.17fF
C159 g1 g2 0.17fF
C160 vdd a_575_n373# 0.11fF
C161 g1 w_513_n92# 0.06fF
C162 g1 a_338_n23# 0.21fF
C163 w_323_n92# g0 0.06fF
C164 c0 a_189_n86# 0.11fF
C165 c3 vdd 0.11fF
C166 vdd a_528_n233# 0.21fF
C167 g2 c0 0.75fF
C168 gnd a_182_n359# 0.10fF
C169 w_513_n239# a_587_n373# 0.03fF
C170 p3 p1 0.32fF
C171 a_528_n86# w_513_n92# 0.12fF
C172 p2 a_528_n233# 0.17fF
C173 a_361_n366# a_373_n366# 1.15fF
C174 a_521_n373# g3 0.70fF
C175 p3 a_528_n156# 0.03fF
C176 gnd a_212_n359# 0.25fF
C177 g3 a_575_n373# 0.08fF
C178 a_361_n366# w_320_n323# 0.06fF
```

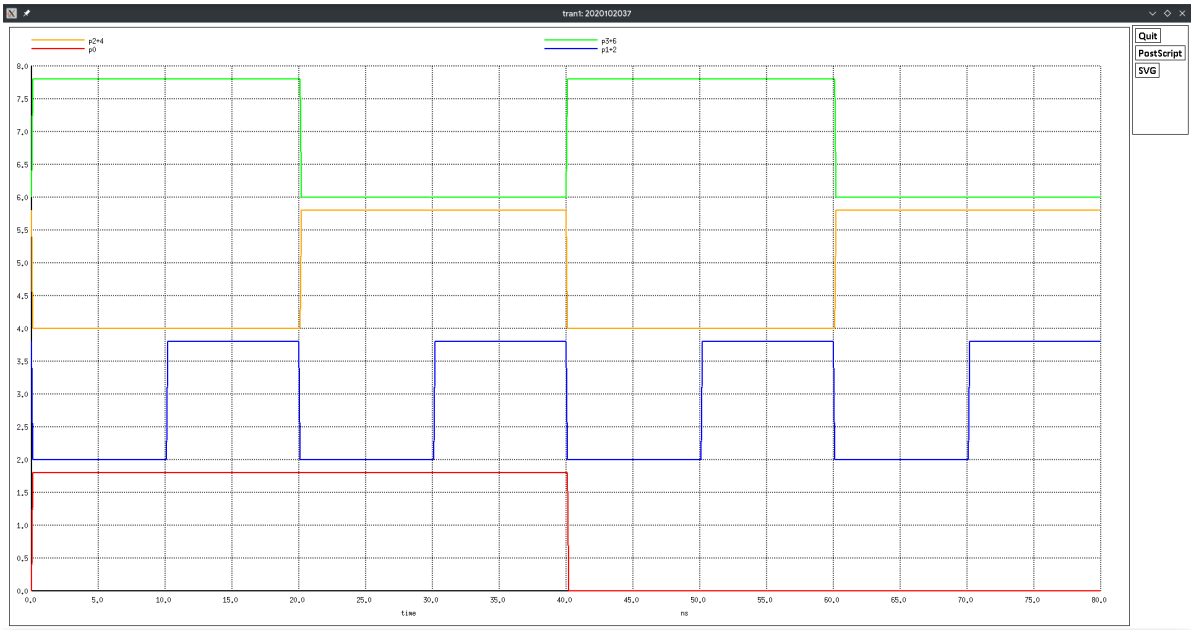
```
C179 gnd a_521_n373# 0.27fF
C180 a_338_n156# w_323_n162# 0.11fF
C181 p1 a_189_n23# 0.03fF
C182 a_385_n366# w_323_n162# 0.03fF
C183 a_182_n359# w_171_n323# 0.10fF
C184 a_338_n156# vdd 0.10fF
C185 p1 g1 6.12fF
C186 g2 a_331_n366# 0.54fF
C187 a_212_n359# a_182_n359# 0.08fF
C188 a_385_n366# vdd 0.30fF
C189 gnd a_575_n373# 0.25fF
C190 vdd g0 0.94fF
C191 gnd c3 0.13fF
C192 p2 a_338_n156# 0.03fF
C193 c0 w_174_n92# 0.06fF
C194 a_212_n359# w_171_n323# 0.06fF
C195 gnd a_528_n233# 0.08fF
C196 p1 c0 0.49fF
C197 p1 w_174_n29# 0.06fF
C198 p2 g0 0.49fF
C199 a_224_n359# g1 0.08fF
C200 a_563_n373# w_510_n323# 0.06fF
C201 vdd w_513_n239# 0.19fF
C202 a_521_n373# a_575_n373# 0.08fF
C203 w_64_n29# vdd 0.14fF
C204 p0 w_323_n162# 0.06fF
C205 w_510_n323# a_587_n373# 0.06fF
C206 w_174_n92# a_189_n86# 0.12fF
C207 p0 vdd 0.88fF
C208 g3 g0 0.09fF
C209 p1 a_189_n86# 0.03fF
C210 a_563_n373# a_551_n373# 1.45fF
C211 gnd a_338_n156# 0.08fF
C212 p2 w_513_n239# 0.06fF
C213 a_102_n352# g0 0.99fF
C214 a_385_n366# gnd 0.17fF
C215 p1 g2 5.62fF
C216 gnd g0 0.34fF
C217 p2 p0 0.32fF
C218 a_563_n373# a_528_n86# 0.05fF
C219 a_551_n373# a_587_n373# 0.08fF
C220 vdd c2 0.11fF
C221 vdd w_323_n29# 0.14fF
C222 p1 w_513_n162# 0.06fF
C223 a_331_n366# a_373_n366# 0.08fF
C224 a_224_n359# a_189_n86# 0.05fF
C225 a_361_n366# vdd 0.45fF
C226 vdd c1 0.11fF
C227 p1 a_338_n86# 0.17fF
C228 g2 a_373_n366# 0.08fF
C229 w_64_n29# a_102_n352# 0.03fF
C230 a_331_n366# w_320_n323# 0.10fF
C231 p0 g3 0.09fF
C232 a_528_n156# w_513_n162# 0.11fF
C233 p2 w_323_n29# 0.06fF
C234 p3 vdd 0.44fF
C235 g2 w_320_n323# 0.06fF
C236 a_563_n373# w_513_n92# 0.03fF
```

```
C237 gnd p0 0.51fF
C238 w_61_n323# vdd 0.11fF
C239 vdd a_528_n23# 0.05fF
C240 a_338_n86# a_373_n366# 0.05fF
C241 p1 w_174_n92# 0.06fF
C242 vdd w_510_n323# 0.15fF
C243 p3 p2 1.40fF
C244 vdd a_189_n23# 0.05fF
C245 w_513_n29# vdd 0.14fF
C246 gnd c2 0.13fF
C247 vdd g1 0.68fF
C248 p1 a_528_n156# 0.08fF
C249 a_361_n366# gnd 0.34fF
C250 gnd c1 0.04fF
C251 c2 a_182_n359# 0.05fF
C252 a_224_n359# w_174_n92# 0.03fF
C253 a_551_n373# vdd 0.11fF
C254 c0 w_323_n162# 0.06fF
C255 p3 g3 5.52fF
C256 p2 g1 1.97fF
C257 c4 vdd 0.11fF
C258 vdd c0 5.58fF
C259 vdd w_174_n29# 0.14fF
C260 a_102_n352# w_61_n323# 0.06fF
C261 a_385_n366# a_338_n156# 0.05fF
C262 w_513_n239# a_528_n233# 0.14fF
C263 p3 gnd 0.26fF
C264 w_323_n92# a_338_n86# 0.12fF
C265 a_528_n86# vdd 0.16fF
C266 c2 w_171_n323# 0.03fF
C267 a_79_n23# vdd 0.05fF
C268 g3 w_510_n323# 0.06fF
C269 p2 c0 0.32fF
C270 c4 Gnd 0.74fF
C271 c3 Gnd 0.71fF
C272 c2 Gnd 0.72fF
C273 c1 Gnd 0.79fF
C274 g3 Gnd 0.47fF
C275 a_521_n373# Gnd 0.63fF
C276 a_331_n366# Gnd 0.52fF
C277 a_182_n359# Gnd 0.36fF
C278 a_72_n352# Gnd 0.32fF
C279 a_587_n373# Gnd 0.30fF
C280 a_528_n233# Gnd 0.61fF
C281 a_575_n373# Gnd 0.37fF
C282 a_385_n366# Gnd 0.28fF
C283 a_528_n156# Gnd 0.51fF
C284 a_338_n156# Gnd 0.51fF
C285 a_563_n373# Gnd 0.41fF
C286 a_373_n366# Gnd 0.34fF
C287 a_224_n359# Gnd 0.60fF
C288 a_528_n86# Gnd 0.42fF
C289 a_338_n86# Gnd 0.42fF
C290 a_189_n86# Gnd 0.42fF
C291 gnd Gnd 0.13fF
C292 a_551_n373# Gnd 0.44fF
C293 a_361_n366# Gnd 0.37fF
C294 a_212_n359# Gnd 0.74fF
```

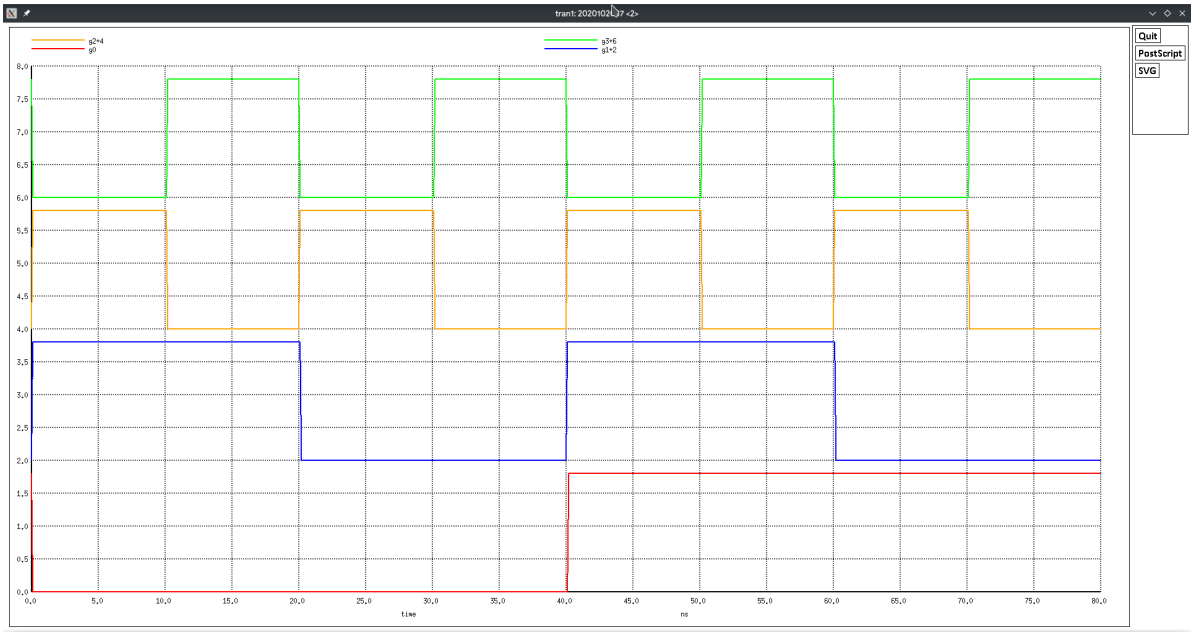
```
C295 vdd Gnd 0.80fF
C296 a_528_n23# Gnd 0.32fF
C297 g2 Gnd 0.40fF
C298 p3 Gnd 0.74fF
C299 a_338_n23# Gnd 0.32fF
C300 p2 Gnd 8.87fF
C301 g0 Gnd 0.21fF
C302 p1 Gnd 10.43fF
C303 c0 Gnd 1.10fF
C304 p0 Gnd 0.62fF
C305 w_510_n323# Gnd 1.81fF
C306 w_320_n323# Gnd 1.61fF
C307 w_171_n323# Gnd 0.58fF
C308 w_61_n323# Gnd 0.78fF
C309 w_513_n239# Gnd 1.75fF
C310 w_513_n162# Gnd 1.61fF
C311 w_323_n162# Gnd 1.61fF
C312 w_513_n92# Gnd 1.37fF
C313 w_323_n92# Gnd 1.37fF
C314 w_174_n92# Gnd 1.37fF
C315 w_513_n29# Gnd 1.12fF
C316 w_323_n29# Gnd 1.12fF
C317 w_174_n29# Gnd 0.52fF
C318 w_64_n29# Gnd 0.72fF

** Analysis **
.tran 1p 10n

** Plotting **
.control
set hcopypscolor=1
set color0=white
set color1=black
run
set curplottitle="2020102037"
plot p0 p1+2 p2+4 p3+6
plot g0 g1+2 g2+4 g3+6
plot c1 c2+2 c3+4 c4+6
.endc

.end
```

5.2.2.3 Simulation Results

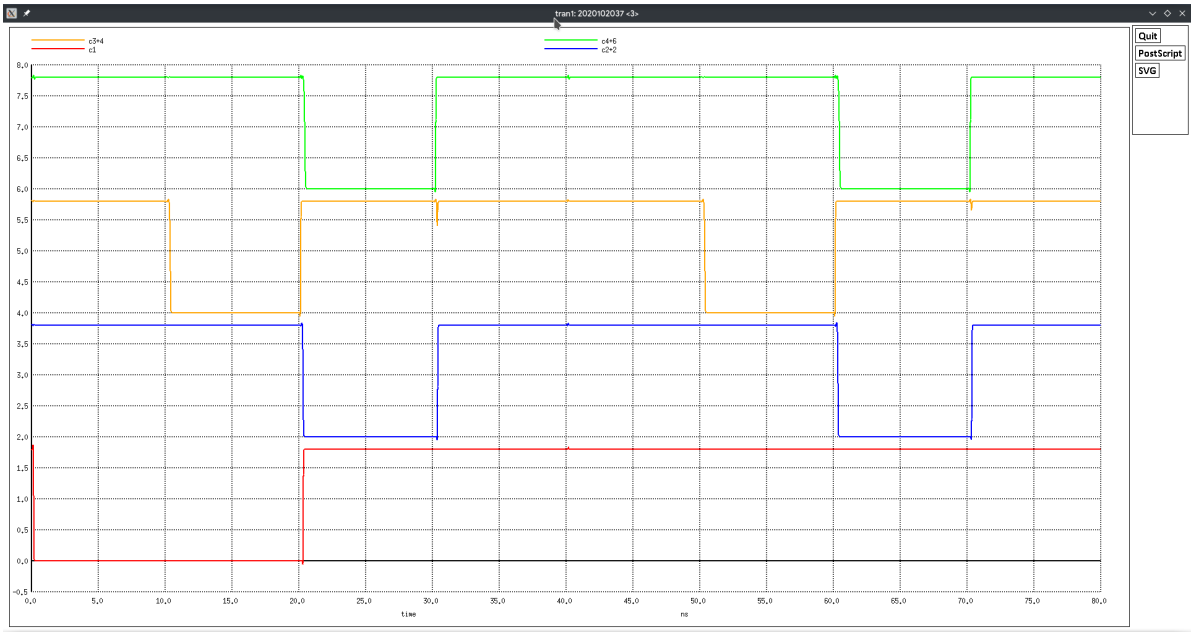
Input P



Input G

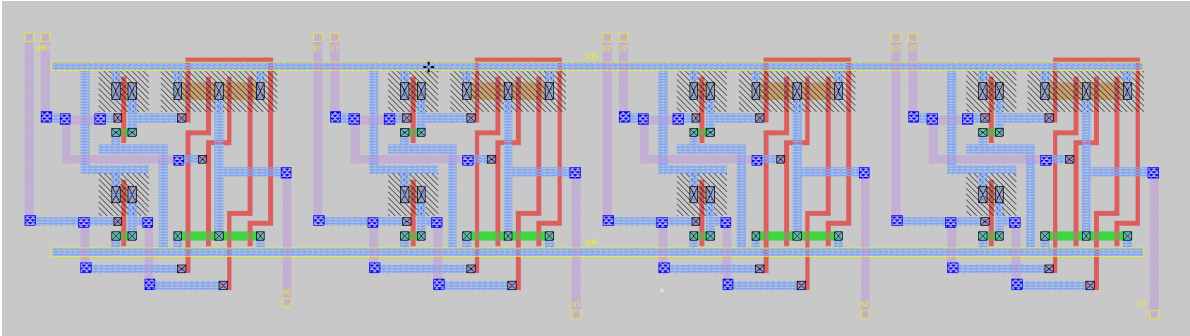


Ouput Carries



5.2.3 Sum Block

5.2.3.1 Layout



5.2.3.2 Netlist

```
.include ../../../TSMC_180nm.txt


** Parameters **
.param VSupply=1.8
.global vdd gnd

** Input Voltages **
VS vdd gnd VSupply

.param HIGH=VSupply
.param LOW=0

* Carry Propogates : p0 p1 p2 p3
VP0 p0 gnd HIGH
VP1 p1 gnd LOW
VP2 p2 gnd LOW
VP3 p3 gnd LOW

* Carries : c0 c1 c2 c3
VC0 c0 gnd HIGH
VC1 c1 gnd HIGH
VC2 c2 gnd HIGH
VC3 c3 gnd LOW

** Circuit Description **
.option scale=0.09u
M1000 a_432_74# c2 gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=352 ps=304
M1001 a_603_92# a_572_74# vdd w_589_86# CMOSP w=8 l=2
+  ad=64 pd=32 as=704 ps=432
M1002 s1 c1 a_323_24# Gnd CMOSN w=4 l=2
+  ad=32 pd=24 as=32 ps=24
M1003 a_152_74# c0 vdd w_139_86# CMOSP w=8 l=2
+  ad=40 pd=26 as=0 ps=0
M1004 a_292_74# c1 gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1005 a_463_92# a_432_74# vdd w_449_86# CMOSP w=8 l=2
+  ad=64 pd=32 as=0 ps=0
M1006 s0 c0 a_183_24# Gnd CMOSN w=4 l=2
+  ad=32 pd=24 as=32 ps=24
```

```
M1007 a_203_24# a_152_24# s0 Gnd CMOSN w=4 l=2
+  ad=32 pd=24 as=0 ps=0
M1008 gnd a_572_74# a_623_24# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=32 ps=24
M1009 s1 p1 a_323_92# w_309_86# CMOSP w=8 l=2
+  ad=64 pd=32 as=64 ps=32
M1010 gnd a_432_74# a_483_24# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=32 ps=24
M1011 s0 p0 a_183_92# w_169_86# CMOSP w=8 l=2
+  ad=64 pd=32 as=64 ps=32
M1012 a_203_92# c0 s0 w_169_86# CMOSP w=8 l=2
+  ad=64 pd=32 as=0 ps=0
M1013 a_432_24# p2 vdd w_419_36# CMOSP w=8 l=2
+  ad=40 pd=26 as=0 ps=0
M1014 a_572_24# p3 gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1015 vdd a_572_24# a_623_92# w_589_86# CMOSP w=8 l=2
+  ad=0 pd=0 as=64 ps=32
M1016 a_292_24# p1 vdd w_279_36# CMOSP w=8 l=2
+  ad=40 pd=26 as=0 ps=0
M1017 a_323_24# p1 gnd Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1018 vdd a_432_24# a_483_92# w_449_86# CMOSP w=8 l=2
+  ad=0 pd=0 as=64 ps=32
M1019 a_572_74# c3 vdd w_559_86# CMOSP w=8 l=2
+  ad=40 pd=26 as=0 ps=0
M1020 a_183_24# p0 gnd Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1021 a_623_24# a_572_24# s3 Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=32 ps=24
M1022 a_152_74# c0 gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1023 a_323_92# a_292_74# vdd w_309_86# CMOSP w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1024 a_483_24# a_432_24# s2 Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=32 ps=24
M1025 a_183_92# a_152_74# vdd w_169_86# CMOSP w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1026 gnd a_292_74# a_343_24# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=32 ps=24
M1027 a_623_92# c3 s3 w_589_86# CMOSP w=8 l=2
+  ad=0 pd=0 as=64 ps=32
M1028 a_432_24# p2 gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1029 a_483_92# c2 s2 w_449_86# CMOSP w=8 l=2
+  ad=0 pd=0 as=64 ps=32
M1030 a_152_24# p0 vdd w_139_36# CMOSP w=8 l=2
+  ad=40 pd=26 as=0 ps=0
M1031 a_292_24# p1 gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1032 s3 c3 a_603_24# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=32 ps=24
M1033 vdd a_292_24# a_343_92# w_309_86# CMOSP w=8 l=2
+  ad=0 pd=0 as=64 ps=32
M1034 a_432_74# c2 vdd w_419_86# CMOSP w=8 l=2
+  ad=40 pd=26 as=0 ps=0
M1035 a_572_74# c3 gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
```

```
M1036 s2 c2 a_463_24# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=32 ps=24
M1037 a_292_74# c1 vdd w_279_86# CMOSP w=8 l=2
+  ad=40 pd=26 as=0 ps=0
M1038 s3 p3 a_603_92# w_589_86# CMOSP w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1039 a_343_24# a_292_24# s1 Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1040 s2 p2 a_463_92# w_449_86# CMOSP w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1041 gnd a_152_74# a_203_24# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1042 a_343_92# c1 s1 w_309_86# CMOSP w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1043 a_572_24# p3 vdd w_559_36# CMOSP w=8 l=2
+  ad=40 pd=26 as=0 ps=0
M1044 a_603_24# p3 gnd Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1045 a_152_24# p0 gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1046 vdd a_152_24# a_203_92# w_169_86# CMOSP w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1047 a_463_24# p2 gnd Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
C0 gnd p2 0.76fF
C1 vdd s3 0.03fF
C2 a_292_24# gnd 0.31fF
C3 c1 gnd 0.21fF
C4 c3 w_589_86# 0.06fF
C5 vdd p1 0.11fF
C6 a_572_74# w_589_86# 0.19fF
C7 w_139_86# c0 0.06fF
C8 vdd c2 0.39fF
C9 vdd w_449_86# 0.11fF
C10 vdd p3 0.11fF
C11 a_432_74# vdd 0.74fF
C12 gnd c0 0.21fF
C13 gnd p0 0.76fF
C14 c3 gnd 0.21fF
C15 a_292_24# a_292_74# 0.02fF
C16 vdd a_572_24# 0.11fF
C17 c0 s0 0.12fF
C18 c1 a_292_74# 0.06fF
C19 a_572_74# gnd 0.08fF
C20 p0 w_139_36# 0.06fF
C21 w_309_86# a_292_74# 0.19fF
C22 a_152_74# c0 0.06fF
C23 p0 a_152_74# 0.02fF
C24 gnd s2 0.13fF
C25 vdd w_419_36# 0.05fF
C26 vdd p2 0.11fF
C27 vdd a_292_24# 0.11fF
C28 p1 w_279_36# 0.06fF
C29 c1 vdd 0.39fF
C30 a_432_24# w_449_86# 0.06fF
C31 w_169_86# c0 0.06fF
C32 p0 w_169_86# 0.06fF
C33 vdd w_309_86# 0.11fF
```

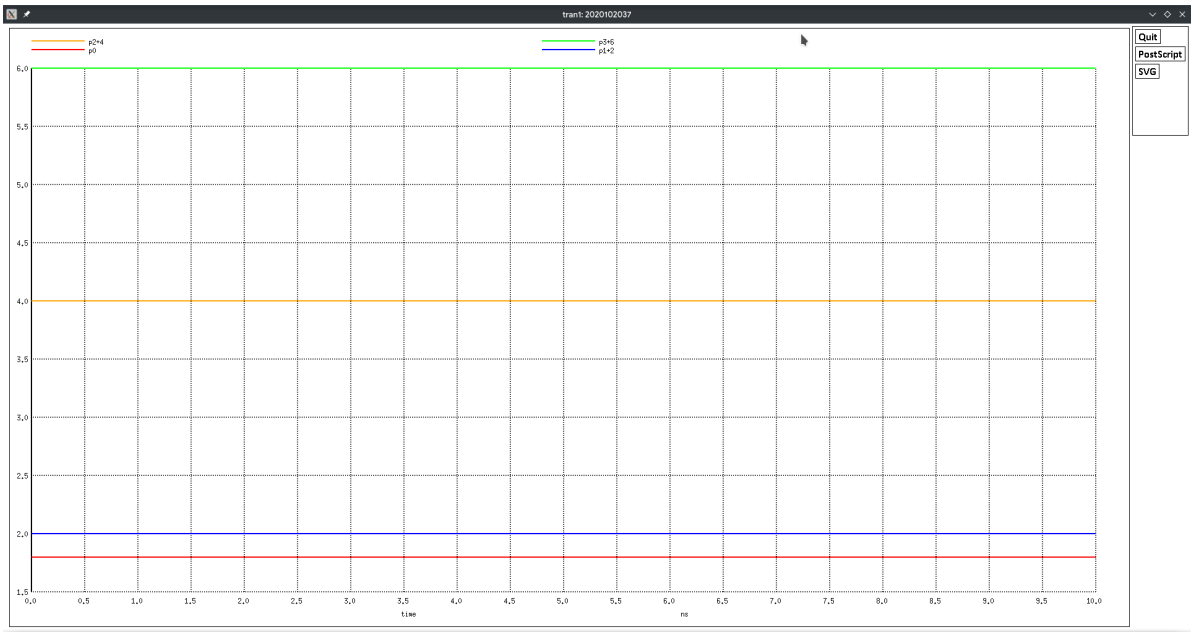
```
C34 a_432_74# a_432_24# 0.02fF
C35 gnd s0 0.13fF
C36 vdd c0 0.30fF
C37 vdd p0 0.02fF
C38 w_139_86# a_152_74# 0.03fF
C39 vdd c3 0.39fF
C40 vdd a_572_74# 0.74fF
C41 gnd a_152_74# 0.08fF
C42 gnd a_292_74# 0.08fF
C43 c1 w_279_86# 0.06fF
C44 a_292_24# s1 0.08fF
C45 vdd w_589_86# 0.11fF
C46 a_152_74# s0 0.08fF
C47 w_419_36# a_432_24# 0.03fF
C48 p2 a_432_24# 0.36fF
C49 a_572_24# s3 0.08fF
C50 c1 s1 0.12fF
C51 c2 w_449_86# 0.06fF
C52 c3 w_559_86# 0.06fF
C53 a_292_24# w_279_36# 0.03fF
C54 w_309_86# s1 0.02fF
C55 vdd s2 0.03fF
C56 a_432_74# c2 0.06fF
C57 a_432_74# w_449_86# 0.19fF
C58 w_139_86# vdd 0.05fF
C59 a_572_74# w_559_86# 0.03fF
C60 vdd w_419_86# 0.05fF
C61 w_169_86# s0 0.02fF
C62 vdd gnd 0.92fF
C63 p3 a_572_24# 0.36fF
C64 vdd s0 0.03fF
C65 vdd w_139_36# 0.05fF
C66 p0 a_152_24# 0.36fF
C67 w_169_86# a_152_74# 0.19fF
C68 a_292_24# p1 0.36fF
C69 p2 c2 0.23fF
C70 p2 w_449_86# 0.06fF
C71 vdd w_559_36# 0.05fF
C72 vdd a_152_74# 0.74fF
C73 vdd a_292_74# 0.74fF
C74 c1 p1 0.23fF
C75 a_432_74# p2 0.02fF
C76 w_309_86# p1 0.06fF
C77 c3 s3 0.12fF
C78 s2 a_432_24# 0.08fF
C79 vdd w_169_86# 0.11fF
C80 gnd s1 0.13fF
C81 a_572_74# s3 0.08fF
C82 gnd a_432_24# 0.31fF
C83 gnd a_152_24# 0.31fF
C84 s3 w_589_86# 0.02fF
C85 p3 c3 0.23fF
C86 w_279_86# a_292_74# 0.03fF
C87 a_152_24# s0 0.08fF
C88 w_419_36# p2 0.06fF
C89 w_139_36# a_152_24# 0.03fF
C90 p3 a_572_74# 0.02fF
C91 s1 a_292_74# 0.08fF
```

```
C92 a_572_74# a_572_24# 0.02fF
C93 gnd s3 0.04fF
C94 p3 w_589_86# 0.06fF
C95 w_309_86# a_292_24# 0.06fF
C96 a_152_24# a_152_74# 0.02fF
C97 s2 c2 0.12fF
C98 s2 w_449_86# 0.02fF
C99 vdd w_559_86# 0.05fF
C100 c1 w_309_86# 0.06fF
C101 a_572_24# w_589_86# 0.06fF
C102 c2 w_419_86# 0.06fF
C103 a_432_74# s2 0.08fF
C104 gnd p1 0.76fF
C105 gnd c2 0.21fF
C106 vdd w_279_86# 0.05fF
C107 a_432_74# w_419_86# 0.03fF
C108 w_169_86# a_152_24# 0.06fF
C109 p3 gnd 0.76fF
C110 a_432_74# gnd 0.08fF
C111 vdd s1 0.03fF
C112 gnd a_572_24# 0.31fF
C113 vdd a_432_24# 0.11fF
C114 vdd w_279_36# 0.05fF
C115 vdd a_152_24# 0.11fF
C116 p0 c0 0.23fF
C117 p1 a_292_74# 0.02fF
C118 p3 w_559_36# 0.06fF
C119 a_572_74# c3 0.06fF
C120 a_572_24# w_559_36# 0.03fF
C121 s3 Gnd 1.12fF
C122 a_572_24# Gnd 1.09fF
C123 p3 Gnd 2.23fF
C124 c3 Gnd 2.10fF
C125 a_572_74# Gnd 0.88fF
C126 s2 Gnd 1.08fF
C127 a_432_24# Gnd 1.09fF
C128 p2 Gnd 2.23fF
C129 c2 Gnd 2.10fF
C130 a_432_74# Gnd 0.88fF
C131 s1 Gnd 1.08fF
C132 a_292_24# Gnd 1.09fF
C133 p1 Gnd 2.23fF
C134 c1 Gnd 2.10fF
C135 a_292_74# Gnd 0.88fF
C136 gnd Gnd 2.99fF
C137 s0 Gnd 1.01fF
C138 vdd Gnd 2.16fF
C139 a_152_24# Gnd 1.09fF
C140 p0 Gnd 2.27fF
C141 c0 Gnd 2.15fF
C142 a_152_74# Gnd 0.88fF
C143 w_559_36# Gnd 0.48fF
C144 w_419_36# Gnd 0.48fF
C145 w_279_36# Gnd 0.48fF
C146 w_139_36# Gnd 0.48fF
C147 w_589_86# Gnd 1.12fF
C148 w_559_86# Gnd 0.48fF
C149 w_449_86# Gnd 1.12fF
```

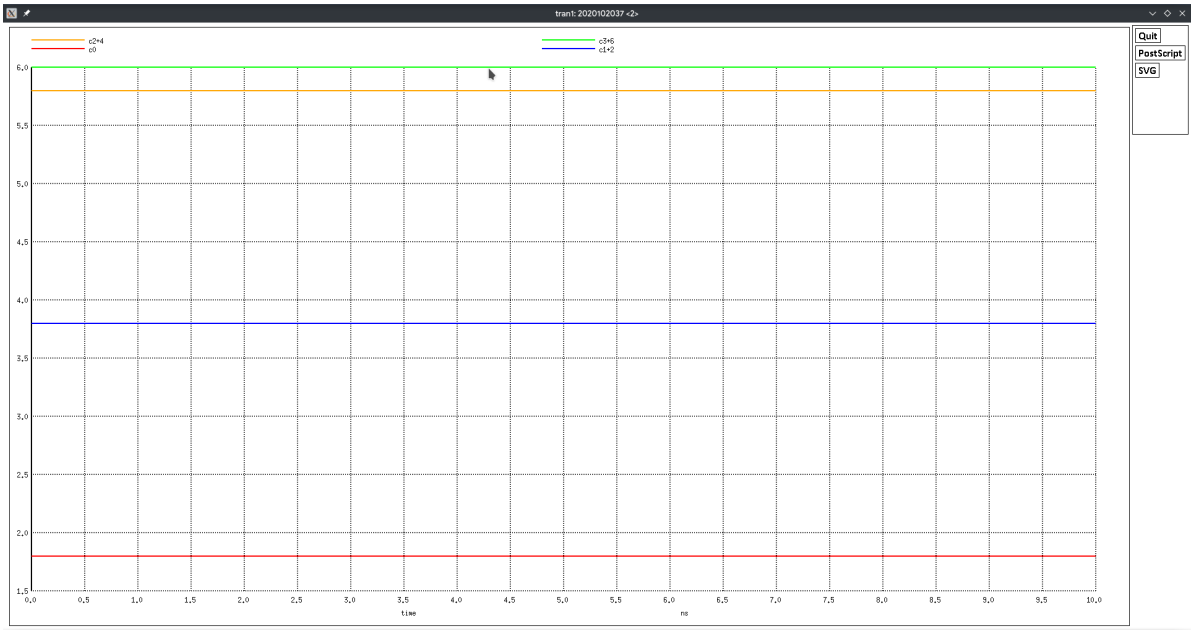
```
C150 w_419_86# Gnd 0.48fF
C151 w_309_86# Gnd 1.12fF
C152 w_279_86# Gnd 0.48fF
C153 w_169_86# Gnd 1.12fF
C154 w_139_86# Gnd 0.48fF

** Analysis **
.tran 1p 10n

** Plotting **
.control
set hcopypscolor=1
set color0=white
set color1=black
run
set curplottitle="2020102037"
plot p0 p1+2 p2+4 p3+6
plot c0 c1+2 c2+4 c3+6
plot s0 s1+2 s2+4 s3+6
.endc

.end
```

5.2.3.3 Simulation Results

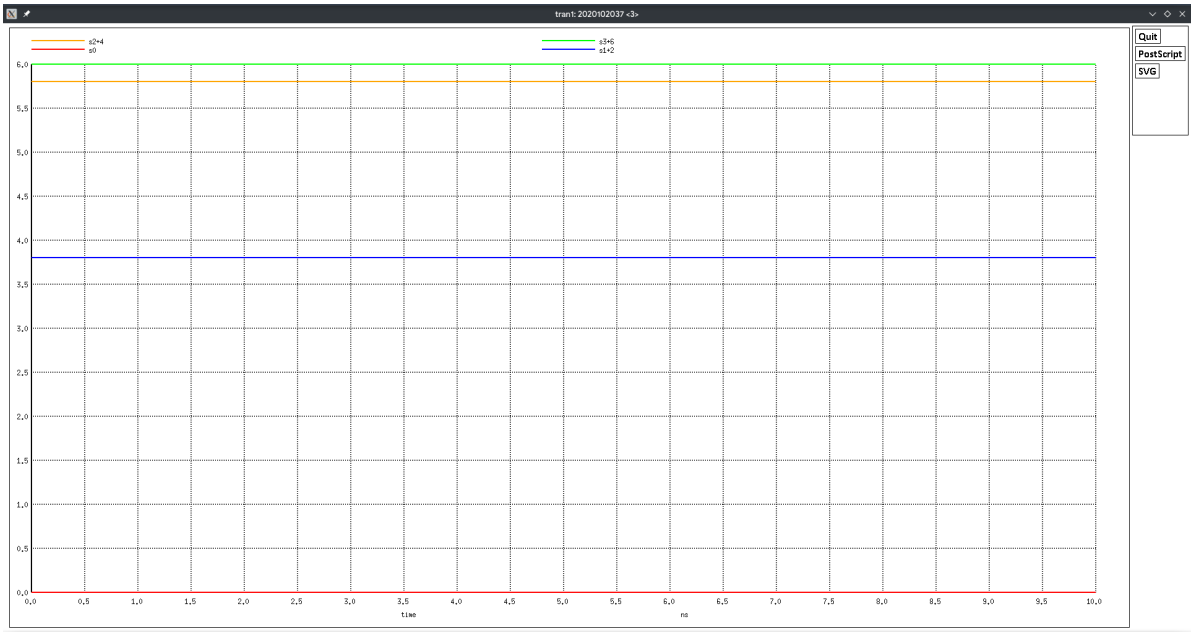
Input P



Input Carries



Output Sum



6. CLA (Pre-Layout)

6.1 Netlist

`carry-lookahead-adder.subs`

```
* Carry Lookahead Adder Subcircuit

.subckt cla s0 s1 s2 s3 c4 a0 a1 a2 a3 b0 b1 b2 b3 c0
xpgblock p0 p1 p2 p3 g0 g1 g2 g3 a0 a1 a2 a3 b0 b1 b2 b3 pgblock
xclblock c1 c2 c3 c4 p0 p1 p2 p3 g0 g1 g2 g3 c0 clblock
xsumblock s0 s1 s2 s3 p0 p1 p2 p3 c0 c1 c2 c3 sumblock
.ends
```

`test-cla.spice`

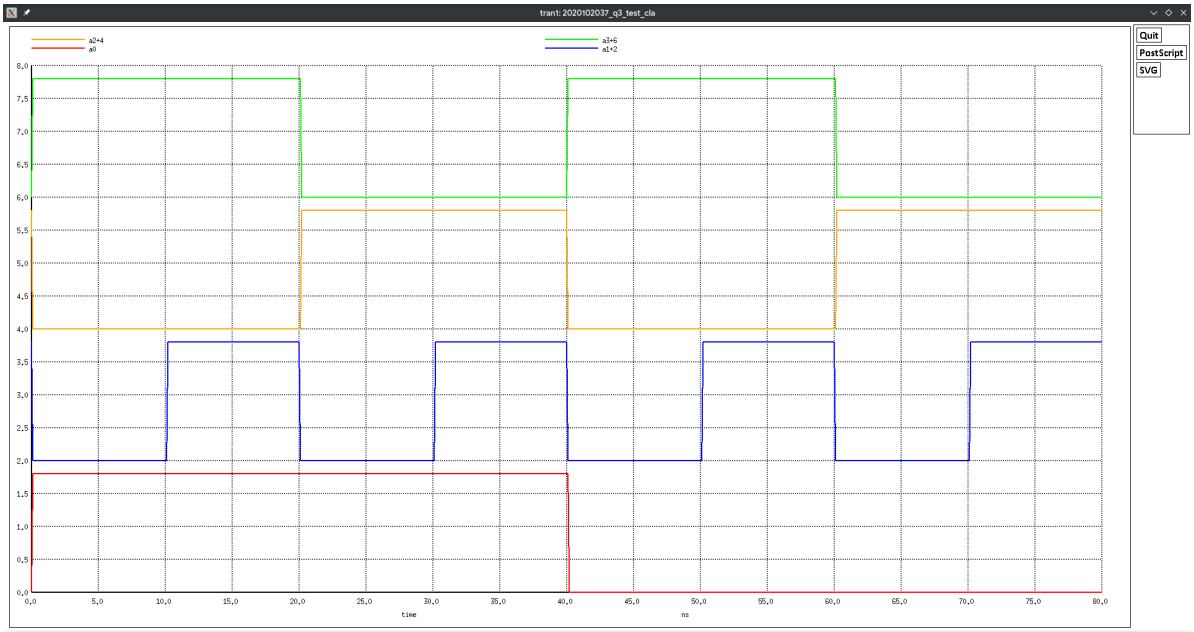
```
* Test CLA
```

```
.include ../../TSMC_180nm.txt
.include ../Gates/and2.subs
.include ../Gates/and3.subs
.include ../Gates/and4.subs
.include ../Gates/and5.subs
.include ../Gates/or2.subs
.include ../Gates/or3.subs
.include ../Gates/or4.subs
.include ../Gates/or5.subs
.include ../Gates/xor2.subs
.include ../Blocks/propogate-generate.subs
.include ../Blocks/carry-lookahead.subs
.include ../Blocks/sum.subs
.include carry-lookahead-adder.subs

** Parameters **
.param VSupply=1.8
.param LAMBDA=0.09u
.param width_N=10*LAMBDA
.param width_P=20*LAMBDA
.global vdd gnd

** Input Voltages **
VS vdd gnd VSupply

.param HIGH=VSupply
.param LOW=0

* A = a3 a2 a1 a0
VA0 a0 gnd pulse LOW  HIGH 0 100p 100p 40n 80n
VA1 a1 gnd pulse HIGH LOW  0 100p 100p 10n 20n
VA2 a2 gnd pulse HIGH LOW  0 100p 100p 20n 40n
VA3 a3 gnd pulse LOW  HIGH 0 100p 100p 20n 40n

* B = b3 b2 b1 b0
VB0 b0 gnd pulse HIGH LOW  0 100p 100p 40n 80n
VB1 b1 gnd pulse LOW  HIGH 0 100p 100p 20n 40n
VB2 b2 gnd pulse LOW  HIGH 0 100p 100p 10n 20n
VB3 b3 gnd pulse HIGH LOW  0 100p 100p 10n 20n

* Carry-In = c0
VC0 c0 gnd pulse HIGH LOW  0 100p 100p 20n 40n

** Circuit Description **
* SUM = c4 s3 s2 s1 s0
xcla1 s0 s1 s2 s3 c4 a0 a1 a2 a3 b0 b1 b2 b3 c0 cla

** Analysis **
.tran 1p 80n

** Plotting **
.control
set hcopypscolor=1
set color0=white
set color1=black
run
set curplottitle="2020102037_Q3_Test_CLA"
plot a0 a1+2 a2+4 a3+6
```

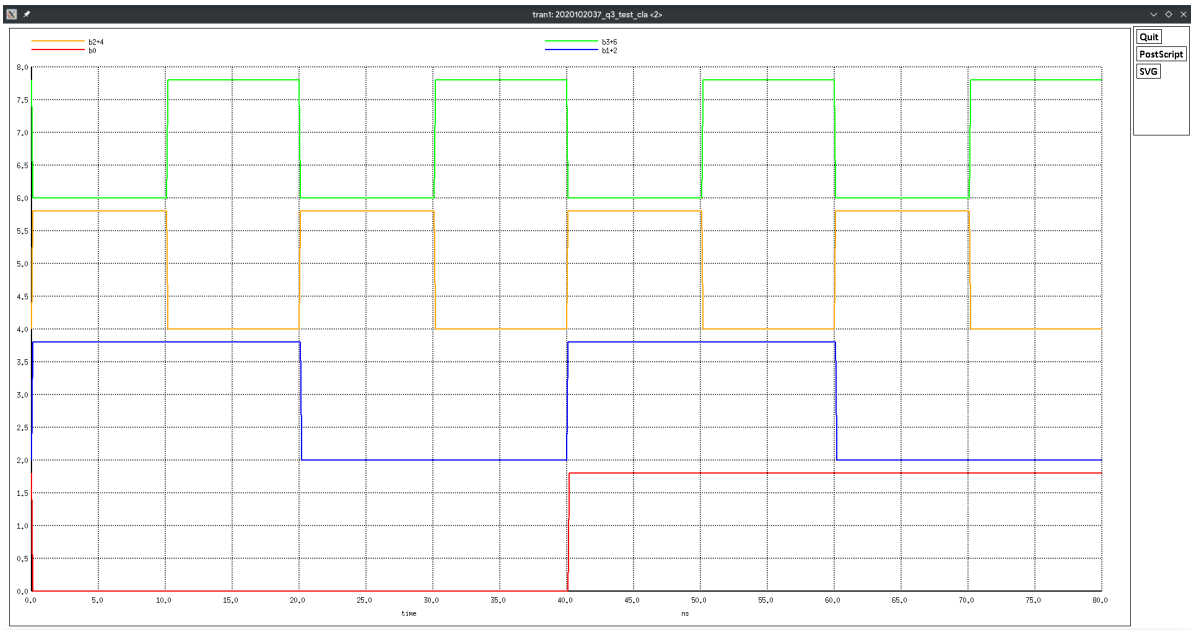
```
plot b0 b1+2 b2+4 b3+6
plot s0 s1+2 s2+4 s3+6 c4+8
.endc

.end
```

6.2 Simulation Results

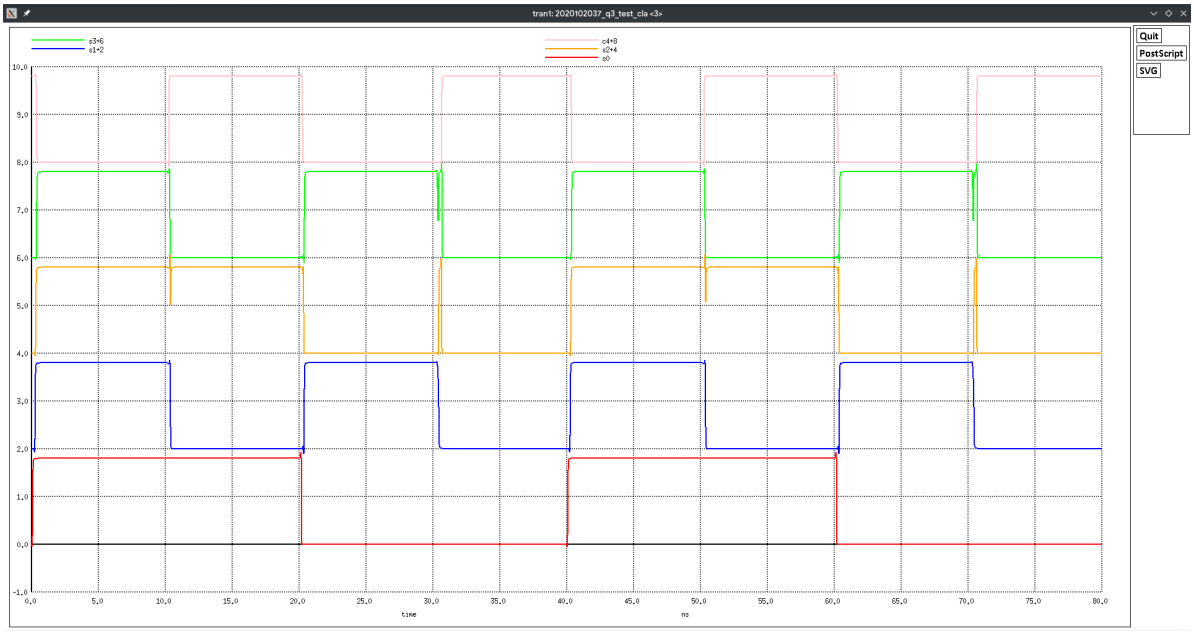
Input A



Input B



Output c4 and sum

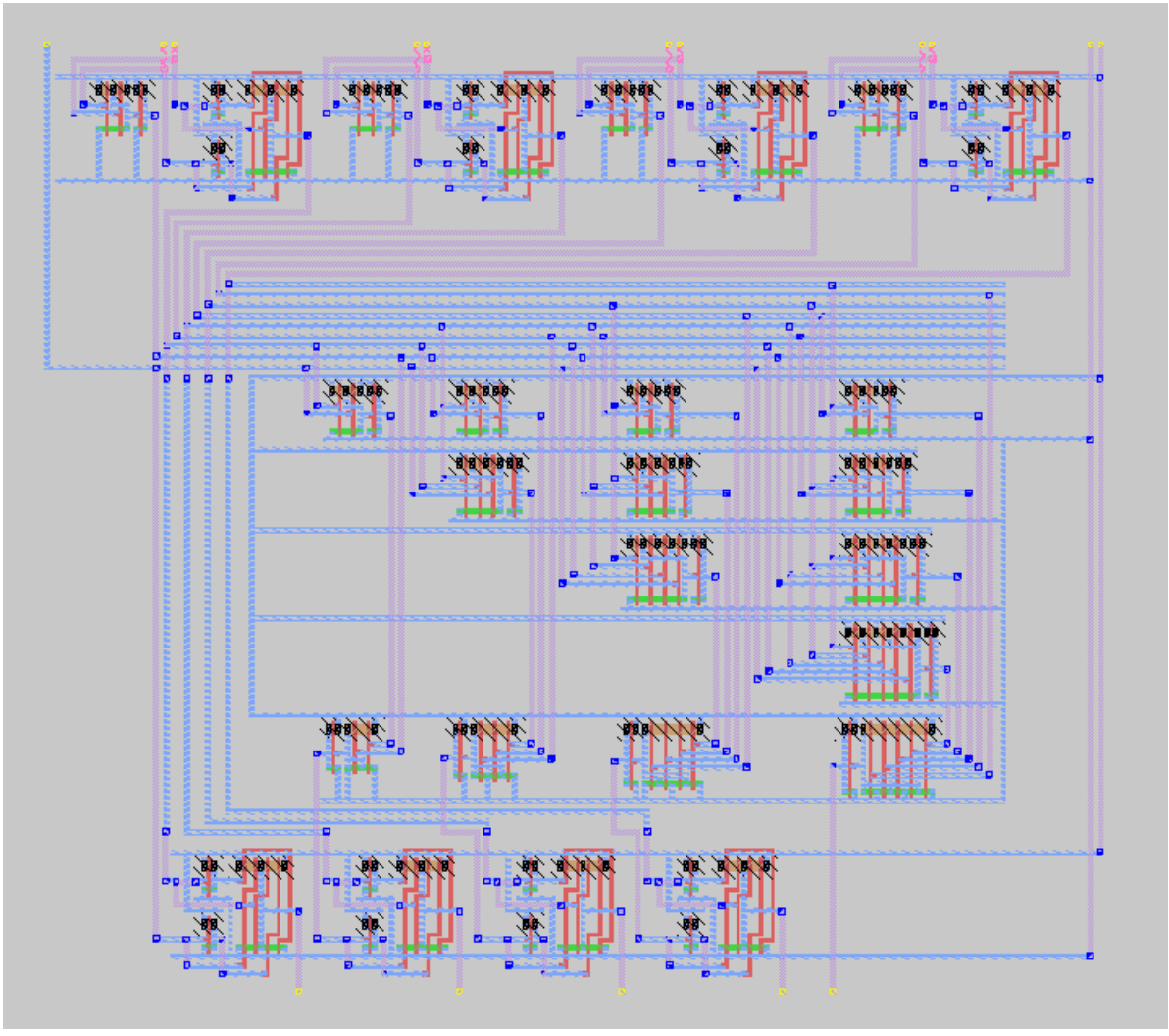


6.3 Delay

7. Floor Plan of CLA

8. CLA Complete Layout

8.1 Magic Layout



8.2 Post-Layout Netlist

```
.include ../../TSMC_180nm.txt

** Parameters **
.param VSupply=1.8
.global vdd gnd

** Input Voltages **
VS vdd gnd VSupply

.param HIGH=VSupply
.param LOW=0

* A = a3 a2 a1 a0
VA0 a0 gnd pulse LOW  HIGH 0 100p 100p 40n 80n
VA1 a1 gnd pulse HIGH LOW  0 100p 100p 10n 20n
VA2 a2 gnd pulse HIGH LOW  0 100p 100p 20n 40n
VA3 a3 gnd pulse LOW  HIGH 0 100p 100p 20n 40n

* B = b3 b2 b1 b0
VB0 b0 gnd pulse HIGH LOW  0 100p 100p 40n 80n
VB1 b1 gnd pulse LOW  HIGH 0 100p 100p 20n 40n
VB2 b2 gnd pulse LOW  HIGH 0 100p 100p 10n 20n
VB3 b3 gnd pulse HIGH LOW  0 100p 100p 10n 20n

* Carry-In = c0
VC0 c0 gnd pulse HIGH LOW  0 100p 100p 20n 40n

** Circuit Description **
.option scale=0.09u

M1000 a_685_911# c0 vdd w_670_905# CMOSP w=8 l=2
+  ad=216 pd=102 as=4256 ps=2424
M1001 a_253_1351# a1 gnd Gnd CMOSN w=4 l=2
+  ad=40 pd=28 as=1784 ps=1484
M1002 gnd a_339_785# a_334_788# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=20 ps=18
M1003 a_33_1351# a0 gnd Gnd CMOSN w=4 l=2
+  ad=40 pd=28 as=0 ps=0
M1004 a_381_1315# a1 gnd Gnd CMOSN w=4 l=2
+  ad=32 pd=24 as=0 ps=0
M1005 a_685_1089# a_536_696# gnd Gnd CMOSN w=4 l=2
+  ad=40 pd=28 as=0 ps=0
M1006 a_821_1315# a3 gnd Gnd CMOSN w=4 l=2
+  ad=32 pd=24 as=0 ps=0
M1007 a_593_639# a_542_639# s3 Gnd CMOSN w=4 l=2
+  ad=32 pd=24 as=32 ps=24
M1008 a_122_639# c0 vdd w_109_651# CMOSP w=8 l=2
+  ad=40 pd=26 as=0 ps=0
M1009 vdd a_116_696# a_346_1058# w_331_1052# CMOSP w=8 l=2
+  ad=0 pd=0 as=136 ps=66
M1010 vdd a_256_696# a_495_988# w_480_982# CMOSP w=8 l=2
+  ad=0 pd=0 as=160 ps=72
M1011 a_685_988# a_256_696# vdd w_670_982# CMOSP w=8 l=2
+  ad=160 pd=72 as=0 ps=0
M1012 a_698_827# a_696_771# a_678_771# w_667_821# CMOSP w=8 l=2
```

```
+  ad=80 pd=36 as=56 ps=30
M1013 a_350_1315# a1 gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1014 a_570_1315# a2 vdd w_557_1327# CMOSP w=8 l=2
+  ad=40 pd=26 as=0 ps=0
M1015 a_229_792# a_63_1351# gnd Gnd CMOSN w=4 l=2
+  ad=40 pd=28 as=0 ps=0
M1016 a_503_1351# a_473_1383# vdd w_458_1377# CMOSP w=8 l=2
+  ad=40 pd=26 as=0 ps=0
M1017 a_433_639# a_334_788# gnd Gnd CMOSN w=4 l=2
+  ad=32 pd=24 as=0 ps=0
M1018 vdd a_63_1351# a_346_1121# w_331_1115# CMOSP w=8 l=2
+  ad=0 pd=0 as=80 ps=36
M1019 s0 c0 a_153_707# w_139_701# CMOSP w=8 l=2
+  ad=64 pd=32 as=64 ps=32
M1020 vdd a_396_696# a_685_1058# w_670_1052# CMOSP w=8 l=2
+  ad=0 pd=0 as=136 ps=66
M1021 a_313_707# a_256_696# s1 w_279_701# CMOSP w=8 l=2
+  ad=64 pd=32 as=64 ps=32
M1022 a_262_689# a_256_696# vdd w_249_701# CMOSP w=8 l=2
+  ad=40 pd=26 as=0 ps=0
M1023 a_339_785# a_369_785# gnd Gnd CMOSN w=4 l=2
+  ad=68 pd=50 as=0 ps=0
M1024 vdd a_130_1315# a_181_1383# w_147_1377# CMOSP w=8 l=2
+  ad=0 pd=0 as=64 ps=32
M1025 vdd a_570_1315# a_621_1383# w_587_1377# CMOSP w=8 l=2
+  ad=0 pd=0 as=64 ps=32
M1026 a_495_988# a_396_696# vdd w_480_982# CMOSP w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1027 vdd a_396_696# a_685_988# w_670_982# CMOSP w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1028 a_495_1019# a_396_696# gnd Gnd CMOSN w=4 l=2
+  ad=40 pd=28 as=0 ps=0
M1029 vdd a_678_771# c4 w_667_821# CMOSP w=8 l=2
+  ad=0 pd=0 as=40 ps=26
M1030 a_253_1383# a1 vdd w_238_1377# CMOSP w=8 l=2
+  ad=80 pd=36 as=0 ps=0
M1031 vdd a_503_1351# a_685_1121# w_670_1115# CMOSP w=8 l=2
+  ad=0 pd=0 as=80 ps=36
M1032 a_346_1121# a_63_1351# a_346_1089# Gnd CMOSN w=4 l=2
+  ad=28 pd=22 as=40 ps=28
M1033 a_346_1019# a_256_696# gnd Gnd CMOSN w=4 l=2
+  ad=40 pd=28 as=0 ps=0
M1034 a_732_771# a_685_988# vdd w_670_982# CMOSP w=8 l=2
+  ad=40 pd=26 as=0 ps=0
M1035 a_253_1383# b1 a_253_1351# Gnd CMOSN w=4 l=2
+  ad=28 pd=22 as=0 ps=0
M1036 a_693_1383# b3 a_693_1351# Gnd CMOSN w=4 l=2
+  ad=28 pd=22 as=40 ps=28
M1037 gnd a_542_778# a_488_778# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=80 ps=56
M1038 gnd a_229_792# a_224_795# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=20 ps=18
M1039 a_381_1383# a_350_1365# vdd w_367_1377# CMOSP w=8 l=2
+  ad=64 pd=32 as=0 ps=0
M1040 a_33_1383# a0 vdd w_18_1377# CMOSP w=8 l=2
+  ad=80 pd=36 as=0 ps=0
M1041 a_821_1383# a_790_1365# vdd w_807_1377# CMOSP w=8 l=2
```

```
+  ad=64 pd=32 as=0 ps=0
M1042 gnd a_720_771# a_678_771# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=108 ps=78
M1043 a_520_827# a_518_778# a_508_827# w_477_821# CMOSP w=8 l=2
+  ad=80 pd=36 as=80 ps=36
M1044 gnd a_402_689# a_453_639# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=32 ps=24
M1045 a_130_1365# b0 gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1046 a_33_1383# b0 a_33_1351# Gnd CMOSN w=4 l=2
+  ad=28 pd=22 as=0 ps=0
M1047 a_790_1365# b3 gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1048 a_350_1365# b1 vdd w_337_1377# CMOSP w=8 l=2
+  ad=40 pd=26 as=0 ps=0
M1049 a_685_1121# a_503_1351# a_685_1089# Gnd CMOSN w=4 l=2
+  ad=28 pd=22 as=0 ps=0
M1050 a_685_1019# a_536_696# gnd Gnd CMOSN w=4 l=2
+  ad=40 pd=28 as=0 ps=0
M1051 a_369_785# a_346_1121# vdd w_331_1115# CMOSP w=8 l=2
+  ad=40 pd=26 as=0 ps=0
M1052 a_685_858# a_536_696# gnd Gnd CMOSN w=4 l=2
+  ad=40 pd=28 as=0 ps=0
M1053 a_346_1058# c0 vdd w_331_1052# CMOSP w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1054 a_153_639# c0 gnd Gnd CMOSN w=4 l=2
+  ad=32 pd=24 as=0 ps=0
M1055 a_181_1315# a_130_1315# a_116_696# Gnd CMOSN w=4 l=2
+  ad=32 pd=24 as=32 ps=24
M1056 a_621_1315# a_570_1315# a_396_696# Gnd CMOSN w=4 l=2
+  ad=32 pd=24 as=32 ps=24
M1057 s1 a_256_696# a_293_639# Gnd CMOSN w=4 l=2
+  ad=32 pd=24 as=32 ps=24
M1058 a_593_707# a_536_696# s3 w_559_701# CMOSP w=8 l=2
+  ad=64 pd=32 as=64 ps=32
M1059 a_685_911# a_536_696# vdd w_670_905# CMOSP w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1060 a_495_988# a_116_696# vdd w_480_982# CMOSP w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1061 vdd a_63_1351# a_685_988# w_670_982# CMOSP w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1062 a_402_639# a_334_788# gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1063 a_369_785# a_346_1121# gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1064 a_542_689# a_536_696# gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1065 a_433_707# a_402_689# vdd w_419_701# CMOSP w=8 l=2
+  ad=64 pd=32 as=0 ps=0
M1066 gnd a_259_792# a_229_792# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1067 a_249_827# a_63_1351# a_229_792# w_218_821# CMOSP w=8 l=2
+  ad=80 pd=36 as=56 ps=30
M1068 a_283_1351# a_253_1383# gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1069 a_236_1121# a_116_696# vdd w_221_1115# CMOSP w=8 l=2
+  ad=80 pd=36 as=0 ps=0
M1070 a_696_771# a_693_1383# gnd Gnd CMOSN w=4 l=2
```

```
+  ad=20 pd=18 as=0 ps=0
M1071 vdd b1 a_253_1383# w_238_1377# CMOSP w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1072 vdd b3 a_693_1383# w_678_1377# CMOSP w=8 l=2
+  ad=0 pd=0 as=80 ps=36
M1073 a_358_1019# a_116_696# a_346_1019# Gnd CMOSN w=4 l=2
+  ad=40 pd=28 as=0 ps=0
M1074 a_63_1351# a_33_1383# gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1075 gnd a_790_1365# a_841_1315# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=32 ps=24
M1076 a_236_1089# a_116_696# gnd Gnd CMOSN w=4 l=2
+  ad=40 pd=28 as=0 ps=0
M1077 gnd a_122_689# a_173_639# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=32 ps=24
M1078 a_381_785# a_346_1058# vdd w_331_1052# CMOSP w=8 l=2
+  ad=40 pd=26 as=0 ps=0
M1079 a_685_942# a_536_696# gnd Gnd CMOSN w=4 l=2
+  ad=40 pd=28 as=0 ps=0
M1080 vdd a_488_778# a_483_781# w_477_821# CMOSP w=8 l=2
+  ad=0 pd=0 as=40 ps=26
M1081 vdd b0 a_33_1383# w_18_1377# CMOSP w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1082 a_473_1351# a2 gnd Gnd CMOSN w=4 l=2
+  ad=40 pd=28 as=0 ps=0
M1083 a_488_778# a_503_1351# gnd Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1084 a_709_858# a_256_696# a_697_858# Gnd CMOSN w=4 l=2
+  ad=40 pd=28 as=40 ps=28
M1085 a_542_778# a_495_988# vdd w_480_982# CMOSP w=8 l=2
+  ad=40 pd=26 as=0 ps=0
M1086 s3 a_536_696# a_573_639# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=32 ps=24
M1087 vdd a_229_792# a_224_795# w_218_821# CMOSP w=8 l=2
+  ad=0 pd=0 as=40 ps=26
M1088 a_181_1383# b0 a_116_696# w_147_1377# CMOSP w=8 l=2
+  ad=0 pd=0 as=64 ps=32
M1089 a_621_1383# b2 a_396_696# w_587_1377# CMOSP w=8 l=2
+  ad=0 pd=0 as=64 ps=32
M1090 a_697_1019# a_396_696# a_685_1019# Gnd CMOSN w=4 l=2
+  ad=40 pd=28 as=0 ps=0
M1091 vdd a_381_785# a_371_827# w_328_821# CMOSP w=8 l=2
+  ad=0 pd=0 as=80 ps=36
M1092 a_122_639# c0 gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1093 a_678_771# a_732_771# gnd Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1094 a_685_911# a_256_696# vdd w_670_905# CMOSP w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1095 a_601_1315# a2 gnd Gnd CMOSN w=4 l=2
+  ad=32 pd=24 as=0 ps=0
M1096 vdd a_402_639# a_453_707# w_419_701# CMOSP w=8 l=2
+  ad=0 pd=0 as=64 ps=32
M1097 vdd a_256_696# a_495_1058# w_480_1052# CMOSP w=8 l=2
+  ad=0 pd=0 as=136 ps=66
M1098 a_262_689# a_256_696# gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1099 a_153_707# a_122_689# vdd w_139_701# CMOSP w=8 l=2
```

```
+  ad=0 pd=0 as=0 ps=0
M1100 a_697_858# a_396_696# a_685_858# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1101 a_570_1315# a2 gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1102 s1 a_224_795# a_293_707# w_279_701# CMOSP w=8 l=2
+  ad=0 pd=0 as=64 ps=32
M1103 a_130_1315# a0 vdd w_117_1327# CMOSP w=8 l=2
+  ad=40 pd=26 as=0 ps=0
M1104 a_283_1351# a_253_1383# vdd w_238_1377# CMOSP w=8 l=2
+  ad=40 pd=26 as=0 ps=0
M1105 a_790_1315# a3 vdd w_777_1327# CMOSP w=8 l=2
+  ad=40 pd=26 as=0 ps=0
M1106 a_696_771# a_693_1383# vdd w_678_1377# CMOSP w=8 l=2
+  ad=40 pd=26 as=0 ps=0
M1107 a_402_689# a_396_696# vdd w_389_701# CMOSP w=8 l=2
+  ad=40 pd=26 as=0 ps=0
M1108 vdd a_396_696# a_685_911# w_670_905# CMOSP w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1109 vdd c0 a_236_1121# w_221_1115# CMOSP w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1110 vdd a_283_1351# a_495_1121# w_480_1115# CMOSP w=8 l=2
+  ad=0 pd=0 as=80 ps=36
M1111 vdd c0 a_495_988# w_480_982# CMOSP w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1112 a_722_827# a_720_771# a_710_827# w_667_821# CMOSP w=8 l=2
+  ad=80 pd=36 as=80 ps=36
M1113 a_63_1351# a_33_1383# vdd w_18_1377# CMOSP w=8 l=2
+  ad=40 pd=26 as=0 ps=0
M1114 vdd a_790_1315# a_841_1383# w_807_1377# CMOSP w=8 l=2
+  ad=0 pd=0 as=64 ps=32
M1115 a_507_942# a_256_696# a_495_942# Gnd CMOSN w=4 l=2
+  ad=40 pd=28 as=40 ps=28
M1116 a_709_942# a_256_696# a_697_942# Gnd CMOSN w=4 l=2
+  ad=40 pd=28 as=40 ps=28
M1117 vdd a_259_792# a_249_827# w_218_821# CMOSP w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1118 a_346_1058# c0 a_358_1019# Gnd CMOSN w=4 l=2
+  ad=28 pd=22 as=0 ps=0
M1119 a_116_696# b0 a_161_1315# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=32 ps=24
M1120 a_396_696# b2 a_601_1315# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1121 a_473_1383# a2 vdd w_458_1377# CMOSP w=8 l=2
+  ad=80 pd=36 as=0 ps=0
M1122 a_236_1121# c0 a_236_1089# Gnd CMOSN w=4 l=2
+  ad=28 pd=22 as=0 ps=0
M1123 a_495_1121# a_283_1351# a_495_1089# Gnd CMOSN w=4 l=2
+  ad=28 pd=22 as=40 ps=28
M1124 a_542_639# a_483_781# vdd w_529_651# CMOSP w=8 l=2
+  ad=40 pd=26 as=0 ps=0
M1125 a_453_639# a_402_639# s2 Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=32 ps=24
M1126 a_473_1383# b2 a_473_1351# Gnd CMOSN w=4 l=2
+  ad=28 pd=22 as=0 ps=0
M1127 gnd a_542_689# a_593_639# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1128 vdd a_122_639# a_173_707# w_139_701# CMOSP w=8 l=2
```

```
+  ad=0 pd=0 as=64 ps=32
M1129 a_601_1383# a_570_1365# vdd w_587_1377# CMOSP w=8 l=2
+  ad=64 pd=32 as=0 ps=0
M1130 a_495_942# a_396_696# gnd Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1131 a_697_942# a_396_696# a_685_942# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1132 gnd a_518_778# a_488_778# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1133 a_721_858# a_116_696# a_709_858# Gnd CMOSN w=4 l=2
+  ad=40 pd=28 as=0 ps=0
M1134 a_350_1365# b1 gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1135 s3 a_483_781# a_573_707# w_559_701# CMOSP w=8 l=2
+  ad=0 pd=0 as=64 ps=32
M1136 a_570_1365# b2 vdd w_557_1377# CMOSP w=8 l=2
+  ad=40 pd=26 as=0 ps=0
M1137 a_259_792# a_236_1121# vdd w_221_1115# CMOSP w=8 l=2
+  ad=40 pd=26 as=0 ps=0
M1138 a_518_778# a_495_1121# vdd w_480_1115# CMOSP w=8 l=2
+  ad=40 pd=26 as=0 ps=0
M1139 a_495_1058# a_63_1351# vdd w_480_1052# CMOSP w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1140 a_401_1315# a_350_1315# a_256_696# Gnd CMOSN w=4 l=2
+  ad=32 pd=24 as=32 ps=24
M1141 a_732_771# a_685_988# gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1142 a_122_689# a_116_696# vdd w_109_701# CMOSP w=8 l=2
+  ad=40 pd=26 as=0 ps=0
M1143 gnd a_744_771# a_678_771# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1144 vdd a_116_696# a_685_911# w_670_905# CMOSP w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1145 a_841_1315# a_790_1315# a_536_696# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=32 ps=24
M1146 gnd a_381_785# a_339_785# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1147 a_381_785# a_346_1058# gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1148 a_259_792# a_236_1121# gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1149 a_518_778# a_495_1121# gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1150 a_116_696# a0 a_161_1383# w_147_1377# CMOSP w=8 l=2
+  ad=0 pd=0 as=64 ps=32
M1151 a_396_696# a2 a_601_1383# w_587_1377# CMOSP w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1152 a_708_771# a_685_1121# vdd w_670_1115# CMOSP w=8 l=2
+  ad=40 pd=26 as=0 ps=0
M1153 a_685_1058# a_283_1351# vdd w_670_1052# CMOSP w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1154 a_262_639# a_224_795# vdd w_249_651# CMOSP w=8 l=2
+  ad=40 pd=26 as=0 ps=0
M1155 a_173_639# a_122_639# s0 Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=32 ps=24
M1156 gnd a_262_689# a_313_639# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=32 ps=24
M1157 a_532_827# a_530_778# a_520_827# w_477_821# CMOSP w=8 l=2
```

```
+  ad=80 pd=36 as=0 ps=0
M1158 vdd b2 a_473_1383# w_458_1377# CMOSP w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1159 a_734_827# a_732_771# a_722_827# w_667_821# CMOSP w=8 l=2
+  ad=80 pd=36 as=0 ps=0
M1160 a_744_771# a_685_911# gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1161 a_507_1019# a_256_696# a_495_1019# Gnd CMOSN w=4 l=2
+  ad=40 pd=28 as=0 ps=0
M1162 a_519_942# a_116_696# a_507_942# Gnd CMOSN w=4 l=2
+  ad=40 pd=28 as=0 ps=0
M1163 a_685_988# a_63_1351# a_709_942# Gnd CMOSN w=4 l=2
+  ad=28 pd=22 as=0 ps=0
M1164 a_708_771# a_685_1121# gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1165 a_573_639# a_483_781# gnd Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1166 gnd a_350_1365# a_401_1315# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1167 a_744_771# a_685_911# vdd w_670_905# CMOSP w=8 l=2
+  ad=40 pd=26 as=0 ps=0
M1168 a_530_778# a_495_1058# vdd w_480_1052# CMOSP w=8 l=2
+  ad=40 pd=26 as=0 ps=0
M1169 a_693_1351# a3 gnd Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1170 a_453_707# a_396_696# s2 w_419_701# CMOSP w=8 l=2
+  ad=0 pd=0 as=64 ps=32
M1171 gnd a_488_778# a_483_781# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=20 ps=18
M1172 vdd a_542_639# a_593_707# w_559_701# CMOSP w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1173 a_401_1383# b1 a_256_696# w_367_1377# CMOSP w=8 l=2
+  ad=64 pd=32 as=64 ps=32
M1174 a_841_1383# b3 a_536_696# w_807_1377# CMOSP w=8 l=2
+  ad=0 pd=0 as=64 ps=32
M1175 a_402_689# a_396_696# gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1176 a_161_1315# a0 gnd Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1177 a_720_771# a_685_1058# vdd w_670_1052# CMOSP w=8 l=2
+  ad=40 pd=26 as=0 ps=0
M1178 a_678_771# a_708_771# gnd Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1179 a_359_827# a_283_1351# a_339_785# w_328_821# CMOSP w=8 l=2
+  ad=80 pd=36 as=56 ps=30
M1180 a_790_1315# a3 gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1181 a_130_1315# a0 gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1182 a_542_778# a_495_988# gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1183 a_350_1315# a1 vdd w_337_1327# CMOSP w=8 l=2
+  ad=40 pd=26 as=0 ps=0
M1184 a_293_639# a_224_795# gnd Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1185 vdd a_350_1315# a_401_1383# w_367_1377# CMOSP w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1186 s2 a_396_696# a_433_639# Gnd CMOSN w=4 l=2
```

```
+  ad=0 pd=0 as=0 ps=0
M1187 gnd a_696_771# a_678_771# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1188 a_256_696# b1 a_381_1315# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1189 a_495_1058# a_63_1351# a_507_1019# Gnd CMOSN w=4 l=2
+  ad=28 pd=22 as=0 ps=0
M1190 a_542_639# a_483_781# gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1191 a_536_696# b3 a_821_1315# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1192 a_173_707# a_116_696# s0 w_139_701# CMOSP w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1193 a_693_1383# a3 vdd w_678_1377# CMOSP w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1194 vdd a_262_639# a_313_707# w_279_701# CMOSP w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1195 vdd a_339_785# a_334_788# w_328_821# CMOSP w=8 l=2
+  ad=0 pd=0 as=40 ps=26
M1196 vdd a_744_771# a_734_827# w_667_821# CMOSP w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1197 vdd a_542_778# a_532_827# w_477_821# CMOSP w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1198 a_495_988# c0 a_519_942# Gnd CMOSN w=4 l=2
+  ad=28 pd=22 as=0 ps=0
M1199 a_573_707# a_542_689# vdd w_559_701# CMOSP w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1200 a_122_689# a_116_696# gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1201 a_161_1383# a_130_1365# vdd w_147_1377# CMOSP w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1202 a_570_1365# b2 gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1203 a_685_1058# a_283_1351# a_697_1019# Gnd CMOSN w=4 l=2
+  ad=28 pd=22 as=0 ps=0
M1204 a_790_1365# b3 vdd w_777_1377# CMOSP w=8 l=2
+  ad=40 pd=26 as=0 ps=0
M1205 a_130_1365# b0 vdd w_117_1377# CMOSP w=8 l=2
+  ad=40 pd=26 as=0 ps=0
M1206 gnd a_678_771# c4 Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=20 ps=18
M1207 a_495_1058# a_396_696# vdd w_480_1052# CMOSP w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1208 a_346_1058# a_256_696# vdd w_331_1052# CMOSP w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1209 a_530_778# a_495_1058# gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1210 s0 a_116_696# a_153_639# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1211 a_402_639# a_334_788# vdd w_389_651# CMOSP w=8 l=2
+  ad=40 pd=26 as=0 ps=0
M1212 a_371_827# a_369_785# a_359_827# w_328_821# CMOSP w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1213 gnd a_283_1351# a_339_785# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1214 a_256_696# a1 a_381_1383# w_367_1377# CMOSP w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1215 a_495_1121# a_396_696# vdd w_480_1115# CMOSP w=8 l=2
```

```
+  ad=0 pd=0 as=0 ps=0
M1216 a_685_988# a_536_696# vdd w_670_982# CMOSP w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1217 a_313_639# a_262_639# s1 Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1218 a_262_639# a_224_795# gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1219 a_536_696# a3 a_821_1383# w_807_1377# CMOSP w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1220 a_346_1121# a_256_696# vdd w_331_1115# CMOSP w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1221 a_503_1351# a_473_1383# gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1222 a_685_1058# a_536_696# vdd w_670_1052# CMOSP w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1223 a_293_707# a_262_689# vdd w_279_701# CMOSP w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1224 a_720_771# a_685_1058# gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1225 s2 a_334_788# a_433_707# w_419_701# CMOSP w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1226 a_495_1089# a_396_696# gnd Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1227 a_488_778# a_530_778# gnd Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1228 a_685_911# c0 a_721_858# Gnd CMOSN w=4 l=2
+  ad=28 pd=22 as=0 ps=0
M1229 gnd a_130_1365# a_181_1315# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1230 gnd a_570_1365# a_621_1315# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1231 a_346_1089# a_256_696# gnd Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1232 a_542_689# a_536_696# vdd w_529_701# CMOSP w=8 l=2
+  ad=40 pd=26 as=0 ps=0
M1233 a_685_1121# a_536_696# vdd w_670_1115# CMOSP w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1234 a_710_827# a_708_771# a_698_827# w_667_821# CMOSP w=8 l=2
+  ad=0 pd=0 as=0 ps=0
M1235 a_508_827# a_503_1351# a_488_778# w_477_821# CMOSP w=8 l=2
+  ad=0 pd=0 as=56 ps=30
C0 a_693_1383# w_678_1377# 0.09fF
C1 gnd a_402_689# 0.08fF
C2 a0 vdd 0.22fF
C3 a_283_1351# a_253_1383# 0.05fF
C4 a_283_1351# vdd 0.79fF
C5 a_495_1058# w_480_1052# 0.12fF
C6 a_536_696# a_685_988# 0.03fF
C7 a_262_639# vdd 0.11fF
C8 a_685_911# vdd 0.21fF
C9 gnd a_570_1315# 0.31fF
C10 a_536_696# c0 0.29fF
C11 gnd a_256_696# 0.85fF
C12 a_63_1351# w_670_982# 0.06fF
C13 a_536_696# a_396_696# 3.37fF
C14 a_503_1351# a_116_696# 0.17fF
C15 a_122_639# vdd 0.11fF
C16 a_530_778# a_503_1351# 0.08fF
```

```
C17 c0 w_109_651# 0.06fF
C18 a_122_639# a_122_689# 0.02fF
C19 a_542_689# vdd 0.74fF
C20 a_63_1351# vdd 1.05fF
C21 a_495_1121# w_480_1115# 0.09fF
C22 a_708_771# a_744_771# 0.08fF
C23 a_259_792# vdd 0.48fF
C24 gnd a0 0.76fF
C25 w_480_1052# a_256_696# 0.06fF
C26 a_283_1351# gnd 0.38fF
C27 w_670_982# a_732_771# 0.03fF
C28 a_503_1351# w_670_1115# 0.06fF
C29 w_117_1377# vdd 0.05fF
C30 a_346_1121# a_369_785# 0.05fF
C31 w_807_1377# a_790_1315# 0.06fF
C32 gnd a_262_639# 0.31fF
C33 vdd a_732_771# 0.11fF
C34 gnd a_685_911# 0.08fF
C35 a_283_1351# w_670_1052# 0.06fF
C36 b3 a_693_1383# 0.21fF
C37 b1 a_350_1365# 0.06fF
C38 a_495_1121# a_396_696# 0.03fF
C39 a_495_1058# a_396_696# 0.03fF
C40 a3 w_777_1327# 0.06fF
C41 s1 vdd 0.03fF
C42 w_419_701# a_396_696# 0.06fF
C43 a_224_795# a_256_696# 0.33fF
C44 a_116_696# w_139_701# 0.06fF
C45 a_693_1383# a3 0.03fF
C46 a_122_639# gnd 0.31fF
C47 a_346_1058# w_331_1052# 0.12fF
C48 a_570_1315# a2 0.36fF
C49 gnd a_542_689# 0.08fF
C50 a_63_1351# gnd 0.47fF
C51 a_402_689# a_396_696# 0.06fF
C52 gnd a_259_792# 0.17fF
C53 a_685_988# a_256_696# 0.08fF
C54 w_670_982# vdd 0.18fF
C55 w_328_821# a_283_1351# 0.06fF
C56 c0 a_256_696# 0.61fF
C57 a_518_778# vdd 0.45fF
C58 a_116_696# s0 0.12fF
C59 a_253_1383# vdd 0.05fF
C60 a_570_1315# a_396_696# 0.08fF
C61 a_495_988# vdd 0.10fF
C62 a_122_689# vdd 0.74fF
C63 w_587_1377# a_570_1315# 0.06fF
C64 a_63_1351# w_480_1052# 0.06fF
C65 gnd a_732_771# 0.25fF
C66 a_396_696# a_256_696# 3.67fF
C67 a_224_795# a_262_639# 0.36fF
C68 a_696_771# a_720_771# 0.08fF
C69 a_283_1351# w_480_1115# 0.06fF
C70 gnd s1 0.13fF
C71 b2 vdd 0.48fF
C72 a_685_1058# a_536_696# 0.03fF
C73 a_116_696# b0 0.12fF
C74 a_346_1121# w_331_1115# 0.09fF
```

```
C75 a_283_1351# c0 0.66fF
C76 a_283_1351# a_339_785# 0.37fF
C77 w_667_821# a_732_771# 0.06fF
C78 a_130_1365# a_130_1315# 0.02fF
C79 a_259_792# w_221_1115# 0.03fF
C80 c0 a_685_911# 0.11fF
C81 a_283_1351# a_396_696# 2.05fF
C82 gnd a_518_778# 0.34fF
C83 gnd a_253_1383# 0.04fF
C84 w_419_701# a_402_639# 0.06fF
C85 gnd vdd 14.37fF
C86 a_396_696# a_685_911# 0.17fF
C87 gnd a_495_988# 0.08fF
C88 a_63_1351# a_685_988# 0.11fF
C89 w_529_651# vdd 0.05fF
C90 a_122_639# c0 0.36fF
C91 a_122_689# gnd 0.08fF
C92 w_218_821# a_229_792# 0.10fF
C93 a_63_1351# c0 6.77fF
C94 a_536_696# a_503_1351# 0.83fF
C95 vdd w_670_1052# 0.14fF
C96 a_402_639# a_402_689# 0.02fF
C97 w_238_1377# a1 0.06fF
C98 b3 w_777_1377# 0.06fF
C99 b2 gnd 0.21fF
C100 w_667_821# vdd 0.15fF
C101 a_708_771# a_720_771# 1.45fF
C102 a_63_1351# a_396_696# 0.58fF
C103 w_480_1052# vdd 0.14fF
C104 w_117_1327# a0 0.06fF
C105 a_346_1058# a_116_696# 0.17fF
C106 a_685_988# a_732_771# 0.05fF
C107 a_542_778# w_477_821# 0.06fF
C108 w_279_701# a_256_696# 0.06fF
C109 a_488_778# w_477_821# 0.10fF
C110 a_116_696# a_130_1365# 0.08fF
C111 w_221_1115# vdd 0.14fF
C112 w_328_821# vdd 0.12fF
C113 a_708_771# a_685_1121# 0.05fF
C114 a_381_785# a_283_1351# 0.08fF
C115 a_224_795# vdd 0.22fF
C116 a_790_1315# vdd 0.11fF
C117 w_389_651# a_334_788# 0.06fF
C118 b3 a_790_1365# 0.06fF
C119 w_389_701# a_402_689# 0.03fF
C120 a_685_988# w_670_982# 0.11fF
C121 a_518_778# w_480_1115# 0.03fF
C122 w_480_1115# vdd 0.14fF
C123 a2 vdd 0.22fF
C124 a_685_988# vdd 0.10fF
C125 a_790_1365# a_536_696# 0.08fF
C126 s3 a_542_639# 0.08fF
C127 a_790_1365# a3 0.02fF
C128 a_339_785# vdd 0.11fF
C129 c0 vdd 6.36fF
C130 a_708_771# a_696_771# 1.90fF
C131 w_279_701# a_262_639# 0.06fF
C132 c0 a_495_988# 0.11fF
```

```
C133 a_396_696# w_670_982# 0.06fF
C134 a_122_689# c0 0.02fF
C135 a_283_1351# w_238_1377# 0.03fF
C136 a_685_1058# a_283_1351# 0.11fF
C137 b2 a2 0.97fF
C138 a_483_781# a_542_639# 0.36fF
C139 a_396_696# vdd 1.09fF
C140 a_396_696# a_495_988# 0.03fF
C141 a_503_1351# a_256_696# 6.82fF
C142 w_587_1377# vdd 0.11fF
C143 a_678_771# a_720_771# 0.08fF
C144 a_224_795# gnd 0.80fF
C145 gnd a_790_1315# 0.31fF
C146 a_542_778# w_480_982# 0.03fF
C147 w_249_701# a_262_689# 0.03fF
C148 b2 a_396_696# 0.12fF
C149 s3 w_559_701# 0.02fF
C150 b2 w_587_1377# 0.06fF
C151 a_530_778# w_477_821# 0.06fF
C152 a_685_1121# w_670_1115# 0.09fF
C153 a_116_696# w_670_905# 0.06fF
C154 a_116_696# w_331_1052# 0.06fF
C155 a_536_696# w_559_701# 0.06fF
C156 a_696_771# a_116_696# 0.09fF
C157 gnd a2 0.76fF
C158 gnd a_685_988# 0.08fF
C159 w_419_701# s2 0.02fF
C160 a_283_1351# a_503_1351# 0.17fF
C161 a_483_781# w_559_701# 0.06fF
C162 w_367_1377# a_350_1365# 0.19fF
C163 gnd a_339_785# 0.10fF
C164 gnd c0 1.30fF
C165 w_777_1327# vdd 0.05fF
C166 w_117_1327# vdd 0.05fF
C167 a_402_689# s2 0.08fF
C168 w_279_701# s1 0.02fF
C169 a_530_778# a_542_778# 0.69fF
C170 a_693_1383# vdd 0.05fF
C171 a_790_1365# w_807_1377# 0.19fF
C172 gnd a_396_696# 0.76fF
C173 a_350_1315# w_337_1327# 0.03fF
C174 a_236_1121# a_116_696# 0.03fF
C175 w_147_1377# b0 0.06fF
C176 b0 a_33_1383# 0.21fF
C177 a_530_778# a_488_778# 0.08fF
C178 vdd w_458_1377# 0.14fF
C179 a_116_696# a_130_1315# 0.08fF
C180 a_369_785# w_331_1115# 0.03fF
C181 a_396_696# w_670_1052# 0.06fF
C182 a_381_785# vdd 0.39fF
C183 a_350_1365# a1 0.02fF
C184 a_678_771# a_696_771# 0.70fF
C185 a_63_1351# a_503_1351# 0.17fF
C186 b2 w_458_1377# 0.06fF
C187 a_396_696# w_480_1052# 0.06fF
C188 w_279_701# vdd 0.11fF
C189 a_402_639# vdd 0.11fF
C190 w_678_1377# a_696_771# 0.03fF
```

```
C191 c0 w_221_1115# 0.06fF
C192 w_328_821# a_339_785# 0.10fF
C193 a_116_696# w_480_982# 0.06fF
C194 a_253_1383# w_238_1377# 0.09fF
C195 a_262_639# w_249_651# 0.03fF
C196 w_238_1377# vdd 0.14fF
C197 a_693_1383# gnd 0.04fF
C198 a_744_771# a_685_911# 0.05fF
C199 a_346_1121# a_256_696# 0.03fF
C200 a_685_1058# vdd 0.16fF
C201 w_337_1377# vdd 0.05fF
C202 a_224_795# a_396_696# 0.09fF
C203 a_256_696# a_350_1365# 0.08fF
C204 a_122_639# w_139_701# 0.06fF
C205 a_350_1315# w_367_1377# 0.06fF
C206 a_536_696# a_334_788# 0.09fF
C207 a_708_771# w_670_1115# 0.03fF
C208 a_381_785# gnd 0.17fF
C209 w_18_1377# b0 0.06fF
C210 a_396_696# w_480_1115# 0.06fF
C211 a_396_696# a_685_988# 0.17fF
C212 a_678_771# a_708_771# 0.08fF
C213 w_147_1377# a_130_1365# 0.19fF
C214 w_587_1377# a2 0.06fF
C215 b0 a0 0.97fF
C216 c0 a_396_696# 0.45fF
C217 w_389_701# vdd 0.05fF
C218 a_402_639# gnd 0.31fF
C219 a_518_778# a_503_1351# 1.59fF
C220 a_536_696# a_685_1121# 0.03fF
C221 a_122_639# s0 0.08fF
C222 a_350_1315# a1 0.36fF
C223 a_503_1351# vdd 0.62fF
C224 a_542_689# a_542_639# 0.02fF
C225 a_790_1315# w_777_1327# 0.03fF
C226 a_744_771# a_732_771# 0.52fF
C227 w_587_1377# a_396_696# 0.02fF
C228 a_685_1058# gnd 0.08fF
C229 w_419_701# a_334_788# 0.06fF
C230 w_777_1377# vdd 0.05fF
C231 a_346_1058# a_256_696# 0.03fF
C232 a_381_785# w_328_821# 0.06fF
C233 a_536_696# w_670_905# 0.06fF
C234 a_685_1058# w_670_1052# 0.12fF
C235 a_536_696# a_696_771# 7.08fF
C236 a_678_771# c4 0.05fF
C237 a_63_1351# a_346_1121# 0.21fF
C238 a3 a_696_771# 0.12fF
C239 a_483_781# w_477_821# 0.03fF
C240 a_402_689# a_334_788# 0.02fF
C241 a2 w_458_1377# 0.06fF
C242 a_542_689# w_559_701# 0.19fF
C243 a_350_1315# a_256_696# 0.08fF
C244 a_224_795# w_279_701# 0.06fF
C245 w_139_701# vdd 0.11fF
C246 gnd a_503_1351# 0.38fF
C247 w_249_651# vdd 0.05fF
C248 w_117_1377# b0 0.06fF
```

```
C249 a_262_689# a_256_696# 0.06fF
C250 a_122_689# w_139_701# 0.19fF
C251 a_744_771# vdd 0.13fF
C252 a_130_1365# a0 0.02fF
C253 a_488_778# a_483_781# 0.05fF
C254 a_790_1365# vdd 0.74fF
C255 vdd s2 0.03fF
C256 a_542_639# vdd 0.11fF
C257 b1 w_367_1377# 0.06fF
C258 s0 vdd 0.03fF
C259 a_122_689# s0 0.08fF
C260 a_262_689# a_262_639# 0.02fF
C261 a_346_1121# vdd 0.05fF
C262 w_147_1377# a_130_1315# 0.06fF
C263 b0 vdd 0.48fF
C264 b1 a1 0.97fF
C265 vdd a_350_1365# 0.74fF
C266 gnd a_744_771# 0.17fF
C267 a_685_1058# a_396_696# 0.17fF
C268 w_559_701# vdd 0.11fF
C269 w_670_905# a_256_696# 0.06fF
C270 w_331_1052# a_256_696# 0.06fF
C271 a_696_771# a_256_696# 0.09fF
C272 a_790_1365# gnd 0.08fF
C273 gnd s2 0.13fF
C274 w_117_1377# a_130_1365# 0.03fF
C275 a_503_1351# a2 0.12fF
C276 gnd a_542_639# 0.31fF
C277 a_744_771# w_667_821# 0.06fF
C278 gnd s0 0.13fF
C279 a_536_696# a_116_696# 0.25fF
C280 a_542_639# w_529_651# 0.03fF
C281 c0 a_503_1351# 0.75fF
C282 w_389_701# a_396_696# 0.06fF
C283 a_116_696# w_109_701# 0.06fF
C284 a_283_1351# a_696_771# 0.09fF
C285 a_503_1351# a_396_696# 7.17fF
C286 b1 a_256_696# 0.12fF
C287 a_720_771# a_732_771# 1.00fF
C288 a_63_1351# a_229_792# 0.21fF
C289 gnd a_346_1121# 0.08fF
C290 a_570_1365# w_557_1377# 0.03fF
C291 gnd b0 0.21fF
C292 a_536_696# w_670_1115# 0.06fF
C293 a_685_911# w_670_905# 0.14fF
C294 a_262_689# s1 0.08fF
C295 a_346_1058# vdd 0.16fF
C296 gnd a_350_1365# 0.08fF
C297 a_224_795# w_249_651# 0.06fF
C298 a_473_1383# vdd 0.05fF
C299 a_116_696# w_147_1377# 0.02fF
C300 a_790_1365# a_790_1315# 0.02fF
C301 a_530_778# a_495_1058# 0.05fF
C302 a_130_1365# vdd 0.74fF
C303 b3 w_678_1377# 0.06fF
C304 a0 a_130_1315# 0.36fF
C305 a_283_1351# a_369_785# 1.29fF
C306 a_350_1315# vdd 0.11fF
```

```
C307 a_63_1351# a_696_771# 0.09fF
C308 c0 w_139_701# 0.06fF
C309 b2 a_473_1383# 0.21fF
C310 a_256_696# w_480_982# 0.06fF
C311 a3 w_678_1377# 0.06fF
C312 a_720_771# vdd 0.11fF
C313 a_262_689# vdd 0.74fF
C314 vdd a_334_788# 0.22fF
C315 a_63_1351# w_218_821# 0.06fF
C316 a_503_1351# w_458_1377# 0.03fF
C317 a_696_771# a_732_771# 0.08fF
C318 a_346_1058# gnd 0.08fF
C319 w_218_821# a_259_792# 0.06fF
C320 a_259_792# a_236_1121# 0.05fF
C321 a_570_1315# w_557_1327# 0.03fF
C322 a_396_696# s2 0.12fF
C323 a_116_696# a_256_696# 2.73fF
C324 a_473_1383# gnd 0.04fF
C325 a_229_792# vdd 0.11fF
C326 w_331_1115# a_256_696# 0.06fF
C327 a_685_1121# vdd 0.05fF
C328 gnd a_130_1365# 0.08fF
C329 a_350_1315# gnd 0.31fF
C330 a_518_778# w_477_821# 0.06fF
C331 gnd a_262_689# 0.08fF
C332 gnd a_720_771# 0.34fF
C333 w_477_821# vdd 0.14fF
C334 a_283_1351# a_116_696# 6.72fF
C335 gnd a_334_788# 0.89fF
C336 w_670_905# vdd 0.19fF
C337 w_331_1052# vdd 0.14fF
C338 a_696_771# vdd 0.20fF
C339 a_720_771# w_670_1052# 0.03fF
C340 b3 a_536_696# 0.12fF
C341 b3 a3 0.97fF
C342 a_116_696# a_685_911# 0.08fF
C343 s3 a_536_696# 0.12fF
C344 a_720_771# w_667_821# 0.06fF
C345 w_249_701# a_256_696# 0.06fF
C346 a_570_1315# a_570_1365# 0.02fF
C347 a_518_778# a_542_778# 0.08fF
C348 a_708_771# a_732_771# 0.08fF
C349 gnd a_229_792# 0.05fF
C350 a_542_778# vdd 0.30fF
C351 w_337_1327# a1 0.06fF
C352 w_218_821# vdd 0.11fF
C353 a_542_778# a_495_988# 0.05fF
C354 a_488_778# a_518_778# 0.08fF
C355 gnd a_685_1121# 0.08fF
C356 a_488_778# vdd 0.11fF
C357 a_236_1121# vdd 0.05fF
C358 a_536_696# a_483_781# 0.32fF
C359 b1 a_253_1383# 0.21fF
C360 a_369_785# vdd 0.45fF
C361 a_63_1351# a_116_696# 7.59fF
C362 b1 vdd 0.48fF
C363 a_130_1315# vdd 0.11fF
C364 a_63_1351# w_331_1115# 0.06fF
```

```
C365 a_473_1383# a2 0.03fF
C366 a_346_1058# c0 0.11fF
C367 w_328_821# a_334_788# 0.03fF
C368 a_224_795# a_262_689# 0.02fF
C369 a_402_639# s2 0.08fF
C370 gnd a_696_771# 0.47fF
C371 a_708_771# vdd 0.11fF
C372 gnd a_542_778# 0.17fF
C373 vdd w_480_982# 0.18fF
C374 a_224_795# a_229_792# 0.05fF
C375 a_696_771# w_667_821# 0.06fF
C376 a_495_988# w_480_982# 0.11fF
C377 b3 w_807_1377# 0.06fF
C378 gnd a_488_778# 0.11fF
C379 a_339_785# a_334_788# 0.05fF
C380 w_367_1377# a1 0.06fF
C381 gnd a_236_1121# 0.08fF
C382 gnd a_369_785# 0.25fF
C383 gnd b1 0.21fF
C384 a_536_696# w_807_1377# 0.02fF
C385 gnd a_130_1315# 0.31fF
C386 a3 w_807_1377# 0.06fF
C387 a_396_696# a_334_788# 0.32fF
C388 w_389_651# vdd 0.05fF
C389 a_536_696# w_529_701# 0.06fF
C390 a_678_771# a_732_771# 0.08fF
C391 c4 vdd 0.20fF
C392 a_530_778# a_518_778# 1.15fF
C393 a_116_696# vdd 1.21fF
C394 a_530_778# vdd 0.37fF
C395 a_116_696# a_495_988# 0.08fF
C396 a_536_696# a_256_696# 0.41fF
C397 w_331_1115# vdd 0.14fF
C398 w_337_1377# a_350_1365# 0.03fF
C399 a_122_689# a_116_696# 0.06fF
C400 w_557_1327# vdd 0.05fF
C401 a_708_771# gnd 0.42fF
C402 a_473_1383# w_458_1377# 0.09fF
C403 a_790_1365# w_777_1377# 0.03fF
C404 a_381_785# a_346_1058# 0.05fF
C405 w_367_1377# a_256_696# 0.02fF
C406 w_419_701# a_402_689# 0.19fF
C407 a_236_1121# w_221_1115# 0.09fF
C408 a_224_795# w_218_821# 0.03fF
C409 w_670_1115# vdd 0.14fF
C410 w_328_821# a_369_785# 0.06fF
C411 c0 w_670_905# 0.06fF
C412 c0 w_331_1052# 0.06fF
C413 a_696_771# c0 0.09fF
C414 a_708_771# w_667_821# 0.06fF
C415 a_536_696# a_283_1351# 0.33fF
C416 a_678_771# vdd 0.11fF
C417 a_396_696# w_670_905# 0.06fF
C418 a_495_1058# a_256_696# 0.17fF
C419 a_696_771# a_396_696# 6.93fF
C420 a_536_696# a_685_911# 0.03fF
C421 w_249_701# vdd 0.05fF
C422 gnd c4 0.25fF
```

```
C423 gnd a_116_696# 0.85fF
C424 a_530_778# gnd 0.25fF
C425 w_678_1377# vdd 0.14fF
C426 c0 a_236_1121# 0.21fF
C427 a_570_1365# vdd 0.74fF
C428 w_139_701# s0 0.02fF
C429 w_18_1377# a_33_1383# 0.09fF
C430 a_339_785# a_369_785# 0.08fF
C431 s3 a_542_689# 0.08fF
C432 w_147_1377# a0 0.06fF
C433 w_279_701# a_262_689# 0.19fF
C434 a_33_1383# a0 0.03fF
C435 a_536_696# a_542_689# 0.06fF
C436 a_63_1351# a_536_696# 0.33fF
C437 a_283_1351# a_495_1121# 0.21fF
C438 c4 w_667_821# 0.03fF
C439 a_402_639# a_334_788# 0.36fF
C440 b2 a_570_1365# 0.06fF
C441 a_283_1351# a1 0.12fF
C442 a_483_781# a_542_689# 0.02fF
C443 a_530_778# w_480_1052# 0.03fF
C444 a_122_639# w_109_651# 0.03fF
C445 a_685_1058# a_720_771# 0.05fF
C446 a_678_771# gnd 0.27fF
C447 a_693_1383# a_696_771# 0.05fF
C448 w_337_1327# vdd 0.05fF
C449 a_473_1383# a_503_1351# 0.05fF
C450 a_116_696# w_221_1115# 0.06fF
C451 c0 w_480_982# 0.06fF
C452 vdd w_557_1377# 0.05fF
C453 a_381_785# w_331_1052# 0.03fF
C454 a_63_1351# a_33_1383# 0.05fF
C455 gnd a_570_1365# 0.08fF
C456 a_63_1351# a_495_1058# 0.11fF
C457 a_678_771# w_667_821# 0.10fF
C458 a_396_696# w_480_982# 0.06fF
C459 a_542_639# w_559_701# 0.06fF
C460 a_283_1351# a_256_696# 7.28fF
C461 w_117_1327# a_130_1315# 0.03fF
C462 b2 w_557_1377# 0.06fF
C463 b3 vdd 0.48fF
C464 a2 w_557_1327# 0.06fF
C465 w_18_1377# a0 0.06fF
C466 a_536_696# w_670_982# 0.06fF
C467 c0 a_116_696# 6.02fF
C468 s3 vdd 0.03fF
C469 a_685_911# a_256_696# 0.08fF
C470 a_536_696# vdd 0.85fF
C471 a_381_785# a_369_785# 0.85fF
C472 a3 vdd 0.22fF
C473 a_396_696# a_116_696# 0.41fF
C474 a_542_689# w_529_701# 0.03fF
C475 a_483_781# vdd 0.22fF
C476 w_109_701# vdd 0.05fF
C477 w_367_1377# vdd 0.11fF
C478 a_685_1121# a_503_1351# 0.21fF
C479 a_63_1351# a_256_696# 3.72fF
C480 w_109_651# vdd 0.05fF
```

```
C481 a_122_689# w_109_701# 0.03fF
C482 a_495_1121# a_518_778# 0.05fF
C483 a_63_1351# w_18_1377# 0.03fF
C484 b1 w_238_1377# 0.06fF
C485 a_495_1121# vdd 0.05fF
C486 w_147_1377# vdd 0.11fF
C487 a_744_771# a_720_771# 0.08fF
C488 a_503_1351# w_477_821# 0.06fF
C489 a_33_1383# vdd 0.05fF
C490 b3 gnd 0.21fF
C491 a_570_1365# a2 0.02fF
C492 a_495_1058# vdd 0.16fF
C493 b1 w_337_1377# 0.06fF
C494 a_253_1383# a1 0.03fF
C495 a_63_1351# a0 0.12fF
C496 vdd a1 0.22fF
C497 s3 gnd 0.13fF
C498 w_419_701# vdd 0.11fF
C499 a_696_771# a_503_1351# 0.09fF
C500 a_63_1351# a_283_1351# 0.26fF
C501 a_536_696# gnd 2.96fF
C502 s1 a_256_696# 0.12fF
C503 a3 gnd 0.76fF
C504 a_402_689# vdd 0.74fF
C505 gnd a_483_781# 0.89fF
C506 a_396_696# a_570_1365# 0.08fF
C507 a_536_696# w_670_1052# 0.06fF
C508 a_503_1351# a_542_778# 0.08fF
C509 a_483_781# w_529_651# 0.06fF
C510 b0 a_130_1365# 0.06fF
C511 w_587_1377# a_570_1365# 0.19fF
C512 w_807_1377# vdd 0.11fF
C513 a_488_778# a_503_1351# 0.54fF
C514 w_670_982# a_256_696# 0.06fF
C515 w_529_701# vdd 0.05fF
C516 a_402_639# w_389_651# 0.03fF
C517 a_570_1315# vdd 0.11fF
C518 a_350_1315# a_350_1365# 0.02fF
C519 vdd a_256_696# 1.23fF
C520 gnd a_495_1121# 0.08fF
C521 gnd a_33_1383# 0.04fF
C522 a_495_988# a_256_696# 0.17fF
C523 a_63_1351# a_259_792# 0.99fF
C524 a_495_1058# gnd 0.08fF
C525 a_262_639# s1 0.08fF
C526 gnd a1 0.76fF
C527 a_744_771# w_670_905# 0.03fF
C528 a_696_771# a_744_771# 0.08fF
C529 w_18_1377# vdd 0.14fF
C530 a_224_795# a_536_696# 0.09fF
C531 a_536_696# a_790_1315# 0.08fF
C532 a3 a_790_1315# 0.36fF
C533 s3 Gnd 1.08fF
C534 a_542_639# Gnd 1.09fF
C535 a_542_689# Gnd 0.88fF
C536 s2 Gnd 1.08fF
C537 a_402_639# Gnd 1.09fF
C538 a_402_689# Gnd 0.88fF
```

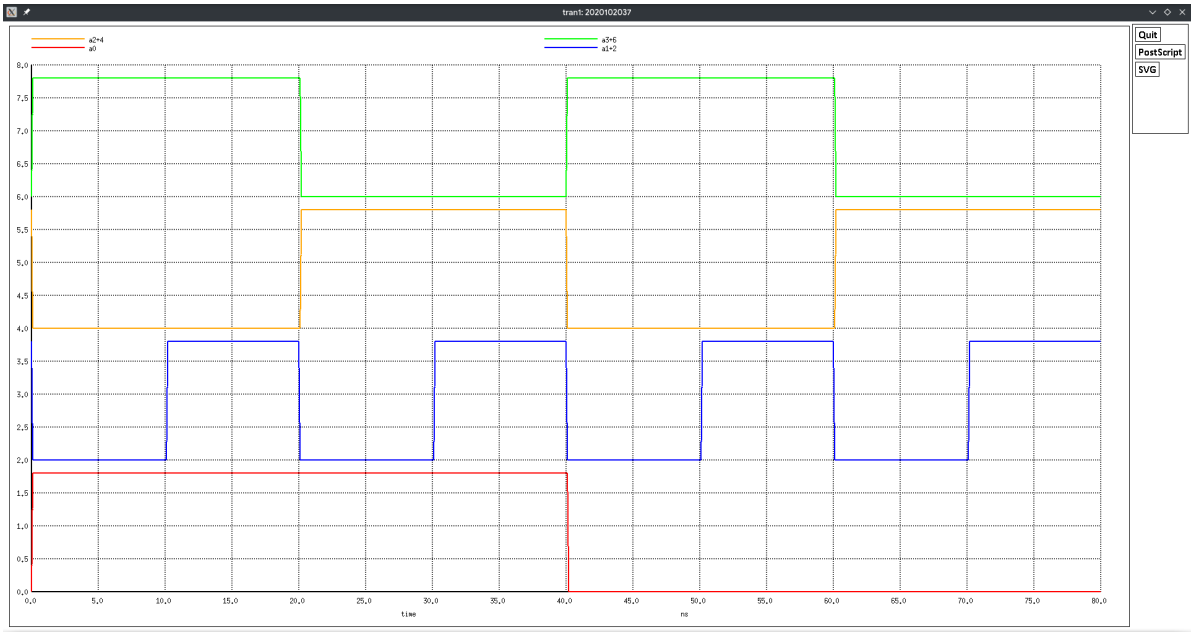
```
C539 s1 Gnd 1.08fF
C540 a_262_639# Gnd 1.09fF
C541 a_262_689# Gnd 0.88fF
C542 s0 Gnd 1.08fF
C543 a_122_639# Gnd 1.09fF
C544 a_122_689# Gnd 0.88fF
C545 c4 Gnd 2.29fF
C546 a_483_781# Gnd 3.25fF
C547 a_334_788# Gnd 3.30fF
C548 a_224_795# Gnd 3.01fF
C549 a_678_771# Gnd 0.63fF
C550 a_488_778# Gnd 0.52fF
C551 a_339_785# Gnd 0.43fF
C552 a_229_792# Gnd 0.32fF
C553 a_744_771# Gnd 1.30fF
C554 a_685_911# Gnd 0.61fF
C555 a_732_771# Gnd 2.34fF
C556 a_542_778# Gnd 2.05fF
C557 a_685_988# Gnd 0.51fF
C558 a_495_988# Gnd 0.51fF
C559 a_720_771# Gnd 3.29fF
C560 a_530_778# Gnd 2.95fF
C561 a_381_785# Gnd 2.74fF
C562 a_685_1058# Gnd 0.42fF
C563 a_495_1058# Gnd 0.42fF
C564 a_346_1058# Gnd 0.42fF
C565 a_708_771# Gnd 4.17fF
C566 a_518_778# Gnd 3.79fF
C567 a_369_785# Gnd 3.58fF
C568 a_259_792# Gnd 3.38fF
C569 a_685_1121# Gnd 0.32fF
C570 a_495_1121# Gnd 0.32fF
C571 a_346_1121# Gnd 0.32fF
C572 a_236_1121# Gnd 0.32fF
C573 c0 Gnd 18.74fF
C574 a_536_696# Gnd 21.08fF
C575 a_696_771# Gnd 15.60fF
C576 a_790_1315# Gnd 1.09fF
C577 a_693_1383# Gnd 0.32fF
C578 b3 Gnd 3.91fF
C579 a3 Gnd 3.51fF
C580 a_790_1365# Gnd 0.88fF
C581 a_396_696# Gnd 21.46fF
C582 a_503_1351# Gnd 14.24fF
C583 a_570_1315# Gnd 1.09fF
C584 a_473_1383# Gnd 0.32fF
C585 b2 Gnd 3.91fF
C586 a2 Gnd 3.51fF
C587 a_570_1365# Gnd 0.88fF
C588 a_256_696# Gnd 20.55fF
C589 a_283_1351# Gnd 13.67fF
C590 a_350_1315# Gnd 1.09fF
C591 a_253_1383# Gnd 0.32fF
C592 b1 Gnd 3.91fF
C593 a1 Gnd 3.51fF
C594 a_350_1365# Gnd 0.88fF
C595 gnd Gnd 27.15fF
C596 a_116_696# Gnd 18.02fF
```

```
C597 a_63_1351# Gnd 13.77fF
C598 vdd Gnd 24.27fF
C599 a_130_1315# Gnd 1.09fF
C600 a_33_1383# Gnd 0.32fF
C601 b0 Gnd 3.91fF
C602 a0 Gnd 3.51fF
C603 a_130_1365# Gnd 0.88fF
C604 w_529_651# Gnd 0.48fF
C605 w_389_651# Gnd 0.48fF
C606 w_249_651# Gnd 0.48fF
C607 w_109_651# Gnd 0.48fF
C608 w_559_701# Gnd 1.12fF
C609 w_529_701# Gnd 0.48fF
C610 w_419_701# Gnd 1.12fF
C611 w_389_701# Gnd 0.48fF
C612 w_279_701# Gnd 1.12fF
C613 w_249_701# Gnd 0.48fF
C614 w_139_701# Gnd 1.12fF
C615 w_109_701# Gnd 0.48fF
C616 w_667_821# Gnd 1.85fF
C617 w_477_821# Gnd 1.61fF
C618 w_328_821# Gnd 1.37fF
C619 w_218_821# Gnd 1.12fF
C620 w_670_905# Gnd 1.85fF
C621 w_670_982# Gnd 1.61fF
C622 w_480_982# Gnd 1.61fF
C623 w_670_1052# Gnd 1.37fF
C624 w_480_1052# Gnd 1.37fF
C625 w_331_1052# Gnd 1.37fF
C626 w_670_1115# Gnd 1.12fF
C627 w_480_1115# Gnd 1.12fF
C628 w_331_1115# Gnd 1.12fF
C629 w_221_1115# Gnd 1.12fF
C630 w_777_1327# Gnd 0.48fF
C631 w_557_1327# Gnd 0.48fF
C632 w_337_1327# Gnd 0.48fF
C633 w_117_1327# Gnd 0.48fF
C634 w_807_1377# Gnd 1.12fF
C635 w_777_1377# Gnd 0.48fF
C636 w_678_1377# Gnd 1.12fF
C637 w_587_1377# Gnd 1.12fF
C638 w_557_1377# Gnd 0.48fF
C639 w_458_1377# Gnd 1.12fF
C640 w_367_1377# Gnd 1.12fF
C641 w_337_1377# Gnd 0.48fF
C642 w_238_1377# Gnd 1.12fF
C643 w_147_1377# Gnd 1.12fF
C644 w_117_1377# Gnd 0.48fF
C645 w_18_1377# Gnd 1.12fF

** Analysis **
.tran 1p 80n

** Plotting **
.control
set hcopypscolor=1
set color0=white
set color1=black
```

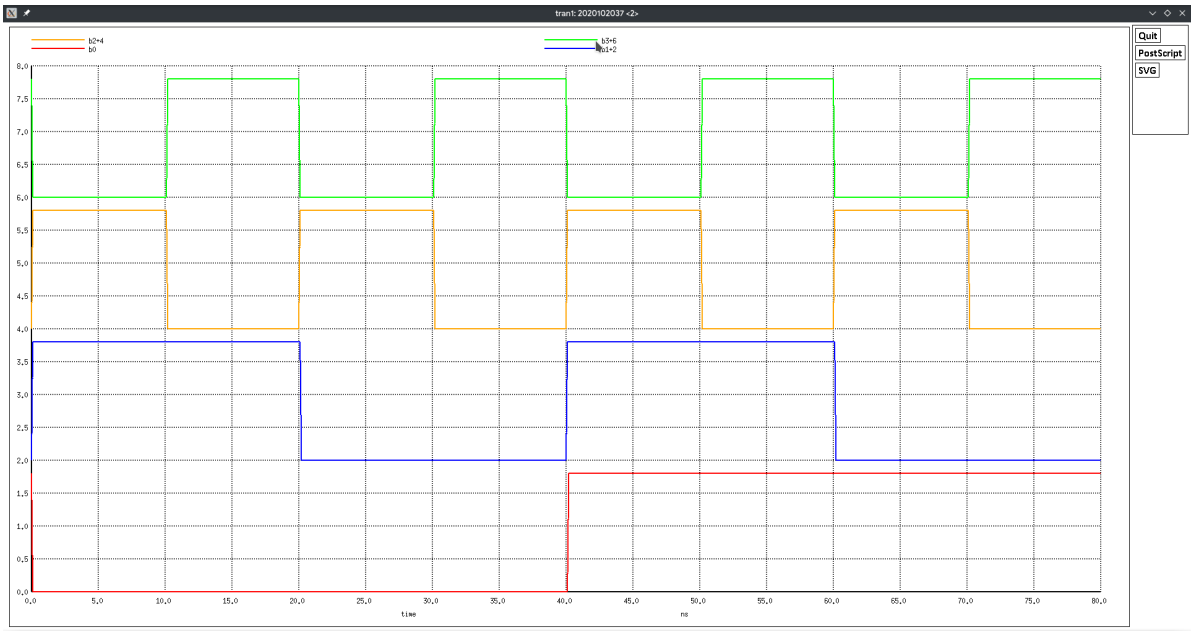
```
run
set curplottitle="2020102037"
plot a0 a1+2 a2+4 a3+6
plot b0 b1+2 b2+4 b3+6
plot s0 s1+2 s2+4 s3+6 c4+8
.endc

.end
```

8.3 Simulation Results

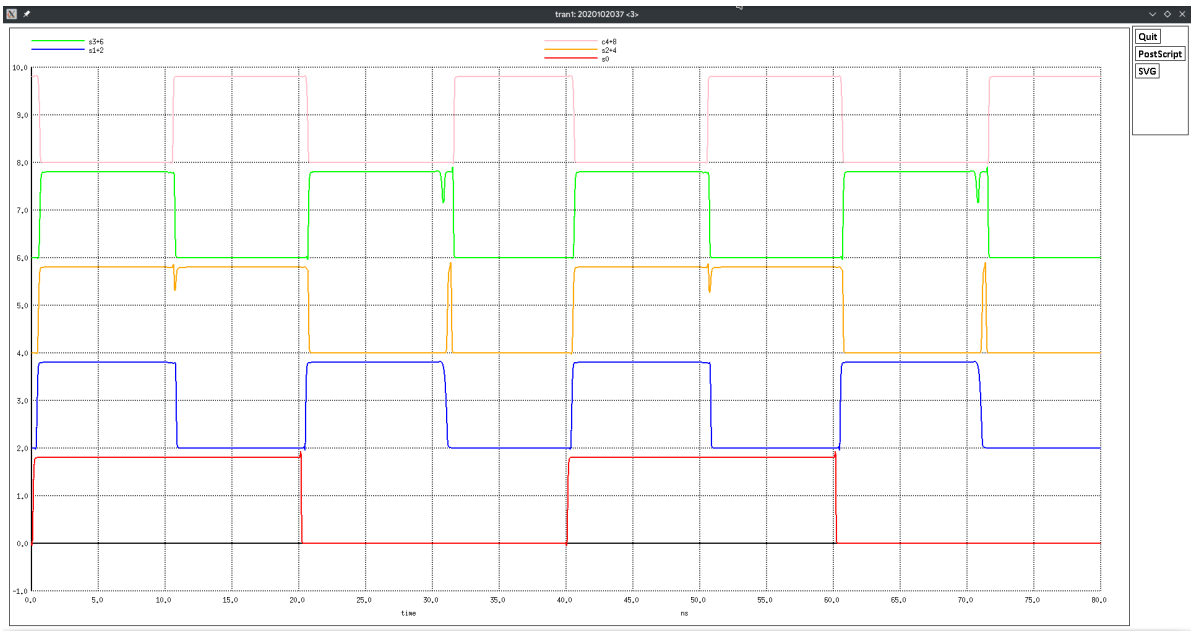
Input A



Input B



Output Sum



9. Delay and Maximum Clock Speed

10. Verilog

10.1 CLA Module

```
// 4-Bit Carry Lookahead Adder
module cla (a, b, cin, s, c);

    // Inputs
    input [3:0] a;
    input [3:0] b;
    input cin;

    //Outputs
    output [3:0] s;
    output [3:0] c;

    // Carry Propogate and Carry Generate Stage

    // Carry Propagates p_i = a_i XOR b_i
    wire [3:0] p;
    xor P0(p[0], a[0], b[0]);
    xor P1(p[1], a[1], b[1]);
    xor P2(p[2], a[2], b[2]);
    xor P3(p[3], a[3], b[3]);

    // Carry Generates g_i = a_i AND b_i
    wire [3:0] g;
    and G0(g[0], a[0], b[0]);
    and G1(g[1], a[1], b[1]);
    and G2(g[2], a[2], b[2]);
    and G3(g[3], a[3], b[3]);

    // Carry Lookahead Stage : c_{i+1} = g_i + p_i.c_i

    wire w0, w1, w2, w3, w4, w5, w6, w7, w8, w9;
```

```
    // c1 = g0 + p0.cin
    and AND20(w0, p[0], cin);
    or  OR20 (c[0], g[0], w0);

    // c2 = g1 + p1.g0 + p1.p0.cin
    and AND21(w1, p[1], g[0]);
    and AND30(w2, p[1], p[0], Cin);
    or  OR30 (c[1], g[1], w1, w2);

    // c3 = g2 + p2.g1 + p2.p1.g0 + p2.p1.p0.cin
    and AND22(w3, p[2], g[1]);
    and AND31(w4, p[2], p[1], g[0]);
    and AND40(w5, p[2], p[1], p[0], cin);
    or  OR40 (c[2], g[2], w3, w4, w5);

    // c4 = g3 + p3.g2 + p3.p2.g1 + p3.p2.p1.g0 + p3.p2.p1.p0.cin
    and AND23(w6, p[3], g[2]);
    and AND32(w7, p[3], p[2], g[1]);
    and AND41(w8, p[3], p[2], p[1], g[0]);
    and AND50(w9, p[3], p[2], p[1], p[0], cin);
    or  OR50 (c[3], g[3], w6, w7, w8, w9);

    // Sum Stage : s_i = p_i XOR c_i
    xor S0(s[0], p[0], cin);
    xor S1(s[1], p[1], c[0]);
    xor S2(s[2], p[2], c[1]);
    xor S3(s[3], p[3], c[2]);

endmodule
```

10.2 Testbench

```
`timescale 1ns/1ps
module testbench();
    reg [3:0] a;
    reg [3:0] b;
    reg cin;

    output [3:0] s;
    output [3:0] c;

    cla X(a, b, cin, s, c);

    initial begin
        $dumpfile("cla.vcd");
        $dumpvars(0,testbench);

        $monitor($time, " a = %d, b = %d, cin = %d, carry = %d, sum = %d", a, b, cin,
c[3], s);
        a = 4'd0; b = 4'd0; cin = 1'd0;

        #20 a = 4'd6; b = 4'd2; cin = 0;
        #20 a = 4'd3; b = 4'd10; cin = 0;
        #20 a = 4'd11; b = 4'd10; cin = 1;
        #20 a = 4'd0; b = 4'd0; cin = 0;
        #20 a = 4'd9; b = 4'd0; cin = 1;
```

```
        #20 a = 4'd15; b = 4'd15; cin = 1;
        #20 a = 4'd6; b = 4'd2; cin = 0;

        $finish;
    end
endmodule
```

10.3 Output

```
VCD info: dumpfile cla.vcd opened for output.
                   0 a =  0, b =  0, cin = 0, carry = 0, sum =  0
                  20 a =  6, b =  2, cin = 0, carry = 0, sum =  8
                  40 a =  3, b = 10, cin = 0, carry = 0, sum = 13
                  60 a = 11, b = 10, cin = 1, carry = 1, sum =  6
                  80 a =  0, b =  0, cin = 0, carry = 0, sum =  0
                 100 a =  9, b =  0, cin = 1, carry = 0, sum = 10
                 120 a = 15, b = 15, cin = 1, carry = 1, sum = 15
                 140 a =  6, b =  2, cin = 0, carry = 0, sum =  8
```

10.4 GTKWave Output