VLSI DESIGN: Course Project

Monsoon'21, IIIT Hyderabad

Due Date : 4th December, 2021

Instructions:

1. Submit your assignment as a single file in pdf format (*Name_RollNo.pdf*)
2. Use the given 180 nm technology file for the NGSPICE simulations and SCN6M_DEEP.09.tech27 for MAGIC layout
3. Consider lengths of NMOS and PMOS to be equal ($L_n = L_p$), and $V_{DD} = 1.8$V until stated otherwise
4. Use 'set curplottitle= Your-name-roll-question-number-part' for every plot in your report so that it is printed on the top of each plot
5. Answers should be complete and must be presented in a systematic way with explanation, plots, annotations net-lists and HDL description
6. Pre-layout simulations takes 25% weightage, verilog part takes 15%, 50% weightage is for the layout and post layout simulation results, 5% for report and bonus part gets 5% weightage.

Objective:

You are asked to design a 4-bit carry look ahead (CLA) adder as shown in Fig.1. Each output sum bit needs to drive an inverter of size $\frac{W_p}{W_n} = \frac{20\lambda}{10\lambda}$, where $\lambda = 0.09\mu m$. You can choose any logic style (static, dynamic, mix) to implement the circuit.

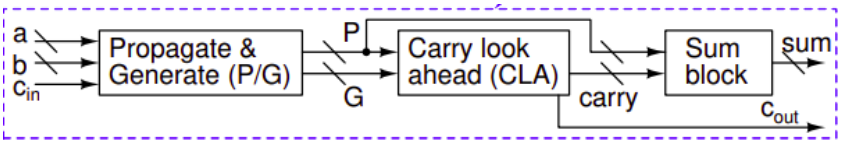

Figure 1: Different blocks in Adder

CLA Adder: If the numbers to be added are $a_4a_3a_2a_1$ and $b_4b_3b_2b_1$, then the propagate (p_i) and generate (g_i) signals for each bit position can be defined as (for i = 1,2,3,4)

$$p_i = a_i \oplus b_i$$
$$g_i = a_i.b_i$$

and the carry out (c_{i+1}) of the i_{th} bit position can be written as (assuming $c_0 = 0$) follows:

$$c_{i+1} = (p_i.c_i) + g_i, i = 1, 2, 3, 4$$

Thus, (c_{i+1}) can be expressed entirely in terms of p_i and g_i functions and the sum can be expressed as follows:

$$sum_i = p_i \oplus c_i$$

Deliverables:

1. Briefly discuss your proposed structure for the adder.
2. Give design details (topology and sizing) of each block (adder modules).
3. Simulate each block and verify its functionality using NGSPICE.
4. Give stick diagrams of all unique gates in your design.
5. Layout each block using MAGIC layout editor and previously given technology file. Perform post layout extraction and compare the results with schematic simulation.
6. Integrate different block designed in previous steps and write the netlist for the full circuit shown in figure 1. Use NGSPICE and verify the functionality of the circuit. Attach the properly annotated waveforms. Report the worst case delay of your adder and maximum clock speed for which your design operates correctly.
7. Give the floor plan of the layout for the complete circuit. Identify the horizontal and vertical pitches in the regular structures.
8. Make layout of the complete circuit and extract the spice netlist. Repeat the simulations discussed above on the extracted netlist. Give a table comparing the schematic and post-layout simulation results.
9. Report the delay of the CLA-adder and maximum clock frequency at which your circuit operates reliably.

10. Using Verilog HDL write the structural description of your circuit and show the correctness of the functionality using simulations. Attach the required wave forms.

Bonus part:

Instead of giving the inputs directly to the Adder, you need to give the input and pass the outputs through D-flip flops as shown in fig 2(a). As shown in Fig.2(b), consider that input bits are available before the rising edge of the clock and the output should be computed and present at the next rising edge of the clock

1. For D-flip-flop, find its setup time, hold time and clock to Q delay from NGSPICE simulations.
2. Show the functionality of the circuit using NGSPICE simulations.

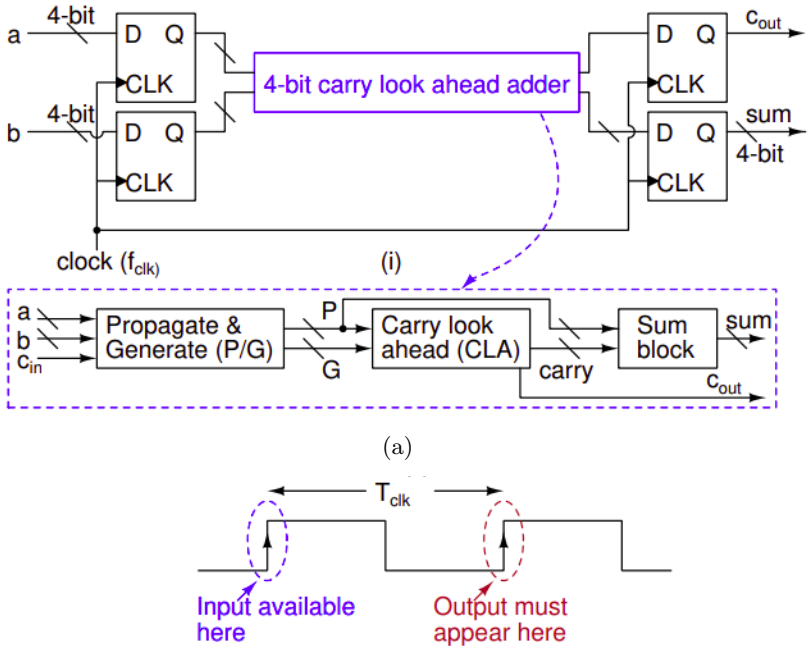

Figure 2: Sequencing inputs and outputs with D-flipflops
