(1) HW1_Report　王竑智　109062542

(2) core utilization=0.7

clock period=90

	(congestion-driven, timing-driven)			
	(off, off)	(on, off)	(off, on)	(on, on)
slack	54.41	51.67	56.45	55.19
total cell area	378622.047400	378930.974191	378099.248218	378732.378464
total wirelength	1184463	1184464	1191763	1097554

Coarse Placement	
Effort	medium
Congestion-driven(if on)	medium

Legalize placement	
Effort	medium

Core Placement and Optimization	
Effort	medium
Power optimization	disable
Clock compilation, optimization and routing	enable

(3) Congestion-driven 會拉大 cell 間的空間以避免繞線衝突發生，Timing-driven placement 則會減少間隙，並縮短繞線長度以減少延遲。

(4) Filler cells 用來填補 place and route 後，在 standard cells 間的空隙，用以連接 VDD、VSS，以確保每個 standard cells 都可以正確且穩固的連接到 VDD、VSS，以得到穩定的電路，或滿足工廠生產的條件。

(5) x=64 2x=128

core utilization=0.7

slack=0.7

core area=540789

total wirelength=1079769 micron