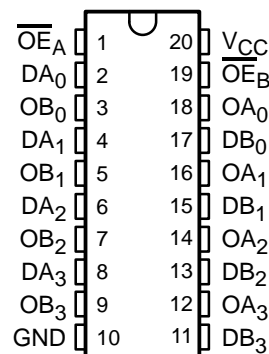


# CY54FCT244T, CY74FCT244T 8-BIT BUFFERS/LINE DRIVERS WITH 3-STATE OUTPUTS

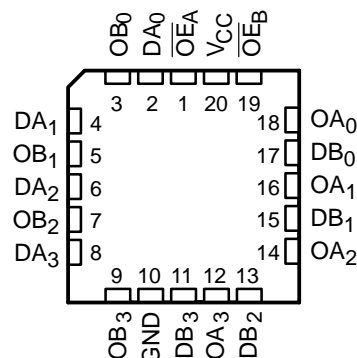
SCCS071 – OCTOBER 2001

- Function, Pinout, and Drive Compatible With FCT and F Logic
- Reduced  $V_{OH}$  (Typically = 3.3 V) Versions of Equivalent FCT Functions
- Edge-Rate Control Circuitry for Significantly Improved Noise Characteristics
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)
- Matched Rise and Fall Times
- Fully Compatible With TTL Input and Output Logic Levels
- CY54FCT244T
  - 48-mA Output Sink Current
  - 12-mA Output Source Current
- CY74FCT244T
  - 64-mA Output Sink Current
  - 32-mA Output Source Current
- 3-State Outputs

CY54FCT244T . . . D PACKAGE  
CY74FCT244T . . . P, Q, OR SO PACKAGE  
(TOP VIEW)



CY54FCT244T . . . L PACKAGE  
(TOP VIEW)



## description

The 'FCT244T devices are octal buffers and line drivers designed to be employed as memory address drivers, clock drivers, and bus-oriented transmitters/receivers. These devices provide speed and drive capabilities equivalent to their fastest bipolar logic counterparts, while reducing power consumption. The input and output voltage levels allow direct interface with TTL, NMOS, and CMOS devices without external components.

These devices are fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2001, Texas Instruments Incorporated  
On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

**CY54FCT244T, CY74FCT244T**  
**8-BIT BUFFERS/LINE DRIVERS**  
**WITH 3-STATE OUTPUTS**

SCCS071 – OCTOBER 2001

**ORDERING INFORMATION**

T <sub>A</sub>	PACKAGE†		SPEED (ns)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	QSOP – Q	Tape and reel	3.6	CY74FCT244DTQCT	FCT244D
	SOIC – SO	Tube	3.6	CY74FCT244DTSOC	FCT244D
		Tape and reel	3.6	CY74FCT244DTSOCT	
–40°C to 85°C	SOIC – SO	Tube	4.1	CY74FCT244CTSOC	FCT244C
		Tape and reel	4.1	CY74FCT244CTSOCT	
	QSOP – Q	Tape and reel	4.1	CY74FCT244CTQCT	FCT244C
	DIP – P	Tube	4.6	CY74FCT244ATPC	CY74FCT244ATPC
	SOIC – SO	Tube	4.6	CY74FCT244ATSOC	FCT244A
		Tape and reel	4.6	CY74FCT244ATSOCT	
	QSOP – Q	Tape and reel	4.6	CY74FCT244ATQCT	FCT244A
	SOIC – SO	Tube	6.5	CY74FCT244TSOC	FCT244
		Tape and reel	6.5	CY74FCT244TSOCT	
	QSOP – Q	Tape and reel	6.5	CY74FCT244TQCT	FCT244
–55°C to 125°C	CDIP – D	Tube	4.6	CY54FCT244CTDMB	
	LCC – L	Tube	4.6	CY54FCT244CTLMB	
	CDIP – D	Tube	5.1	CY54FCT244ATDMB	
	LCC – L	Tube	5.1	CY54FCT244ATLMB	
	CDIP – D	Tube	7	CY54FCT244TDMB	
	LCC – L	Tube	7	CY54FCT244TLMB	

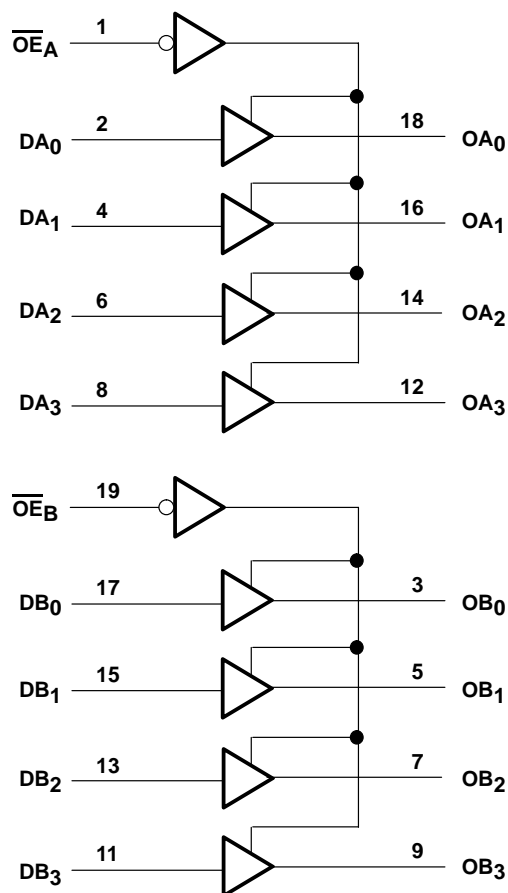
† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

**FUNCTION TABLE**

INPUTS			OUTPUT O
$\overline{OE}_A$	$\overline{OE}_B$	D	
L	L	L	L
L	L	H	H
H	H	X	Z

H = High logic level, L = Low logic level,  
X = Don't care, Z = High-impedance state

**logic diagram (positive logic)**



**absolute maximum rating over operating free-air temperature range (unless otherwise noted)<sup>†</sup>**

Supply voltage range to ground potential .....	–0.5 V to 7 V
DC input voltage range .....	–0.5 V to 7 V
DC output voltage range .....	–0.5 V to 7 V
DC output current (maximum sink current/pin) .....	120 mA
Package thermal impedance, $\theta_{JA}$ (see Note 1): P package .....	69°C/W
Q package .....	68°C/W
SO package .....	58°C/W
Ambient temperature range with power applied, $T_A$ .....	–65°C to 135°C
Storage temperature range, $T_{stg}$ .....	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied.

Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

# CY54FCT244T, CY74FCT244T

## 8-BIT BUFFERS/LINE DRIVERS

### WITH 3-STATE OUTPUTS

SCCS071 – OCTOBER 2001

#### recommended operating conditions (see Note 2)

	CY54FCT244T			CY74FCT244DT			CY74FCT244T			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub> Supply voltage	4.5	5	5.5	4.75	5	5.25	4.75	5	5.25	V
V <sub>IH</sub> High-level input voltage	2			2			2			V
V <sub>IL</sub> Low-level input voltage			0.8			0.8			0.8	V
I <sub>OH</sub> High-level output current			–12			–32			–32	mA
I <sub>OL</sub> Low-level output current			48			64			64	mA
T <sub>A</sub> Operating free-air temperature	–55		125	0		70	–40		85	°C

NOTE 2: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

**CY54FCT244T, CY74FCT244T**  
**8-BIT BUFFERS/LINE DRIVERS**  
**WITH 3-STATE OUTPUTS**

SCCS071 – OCTOBER 2001

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	CY54FCT244T			CY74FCT244T			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
$V_{IK}$	$V_{CC} = 4.5\text{ V}$ , $I_{IN} = -18\text{ mA}$		-0.7	-1.2				V
	$V_{CC} = 4.75\text{ V}$ , $I_{IN} = -18\text{ mA}$					-0.7	-1.2	
$V_{OH}$	$V_{CC} = 4.5\text{ V}$ , $I_{OH} = -12\text{ mA}$	2.4	3.3					V
	$V_{CC} = 4.75\text{ V}$ , $I_{OH} = -32\text{ mA}$				2			
	$V_{CC} = 4.75\text{ V}$ , $I_{OH} = -15\text{ mA}$				2.4	3.3		
$V_{OL}$	$V_{CC} = 4.5\text{ V}$ , $I_{OL} = 48\text{ mA}$	0.3	0.55					V
	$V_{CC} = 4.75\text{ V}$ , $I_{OL} = 64\text{ mA}$				0.3	0.55		
$V_{hys}$	All inputs	0.2			0.2			V
$I_I$	$V_{CC} = 5.5\text{ V}$ , $V_{IN} = V_{CC}$			5				$\mu\text{A}$
	$V_{CC} = 5.25\text{ V}$ , $V_{IN} = V_{CC}$						5	
$I_{IH}$	$V_{CC} = 5.5\text{ V}$ , $V_{IN} = 2.7\text{ V}$			$\pm 1$				$\mu\text{A}$
	$V_{CC} = 5.25\text{ V}$ , $V_{IN} = 2.7\text{ V}$						$\pm 1$	
$I_{IL}$	$V_{CC} = 5.5\text{ V}$ , $V_{IN} = 0.5\text{ V}$			$\pm 1$				$\mu\text{A}$
	$V_{CC} = 5.25\text{ V}$ , $V_{IN} = 0.5\text{ V}$						$\pm 1$	
$I_{OZH}$	$V_{CC} = 5.5\text{ V}$ , $V_{OUT} = 2.7\text{ V}$			10				$\mu\text{A}$
	$V_{CC} = 5.25\text{ V}$ , $V_{OUT} = 2.7\text{ V}$						10	
$I_{OZL}$	$V_{CC} = 5.5\text{ V}$ , $V_{OUT} = 0.5\text{ V}$			-10				$\mu\text{A}$
	$V_{CC} = 5.25\text{ V}$ , $V_{OUT} = 0.5\text{ V}$						-10	
$I_{OS}^\ddagger$	$V_{CC} = 5.5\text{ V}$ , $V_{OUT} = 0\text{ V}$	-60	-120	-225				mA
	$V_{CC} = 5.25\text{ V}$ , $V_{OUT} = 0\text{ V}$				-60	-120	-225	
$I_{off}$	$V_{CC} = 0\text{ V}$ , $V_{OUT} = 4.5\text{ V}$			$\pm 1$			$\pm 1$	$\mu\text{A}$
$I_{CC}$	$V_{CC} = 5.5\text{ V}$ , $V_{IN} \leq 0.2\text{ V}$ , $V_{IN} \geq V_{CC} - 0.2\text{ V}$	0.1	0.2					mA
	$V_{CC} = 5.25\text{ V}$ , $V_{IN} \leq 0.2\text{ V}$ , $V_{IN} \geq V_{CC} - 0.2\text{ V}$				0.1	0.2		
$\Delta I_{CC}$	$V_{CC} = 5.5\text{ V}$ , $V_{IN} = 3.4\text{ V}^\S$ , $f_1 = 0$ , Outputs open	0.5	2					mA
	$V_{CC} = 5.25\text{ V}$ , $V_{IN} = 3.4\text{ V}^\S$ , $f_1 = 0$ , Outputs open				0.5	2		
$I_{CCD}^\P$	$V_{CC} = 5.5\text{ V}$ , One input switching at 50% duty cycle, Outputs open, $\overline{OE}_A = \overline{OE}_B = \text{GND}$ , $V_{IN} \leq 0.2\text{ V}$ or $V_{IN} \geq V_{CC} - 0.2\text{ V}$	0.06	0.12					mA/ MHz
	$V_{CC} = 5.25\text{ V}$ , One input switching at 50% duty cycle, Outputs open, $\overline{OE}_A = \overline{OE}_B = \text{GND}$ , $V_{IN} \leq 0.2\text{ V}$ or $V_{IN} \geq V_{CC} - 0.2\text{ V}$				0.06	0.12		

† Typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample-and-hold techniques are preferable to minimize internal chip heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output can raise the chip temperature well above normal and cause invalid readings in other parametric tests. In any sequence of parameter tests,  $I_{OS}$  tests should be performed last.

§ Per TTL-driven input ( $V_{IN} = 3.4\text{ V}$ ); all other inputs at  $V_{CC}$  or GND

¶ This parameter is derived for use in total power-supply calculations.

**CY54FCT244T, CY74FCT244T**  
**8-BIT BUFFERS/LINE DRIVERS**  
**WITH 3-STATE OUTPUTS**

SCCS071 – OCTOBER 2001

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)**

PARAMETER	TEST CONDITIONS			CY54FCT244T			CY74FCT244T			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
I <sub>C</sub> <sup>#</sup>	V <sub>CC</sub> = 5.5 V, Outputs open, OE <sub>A</sub> = OE <sub>B</sub> = GND	One bit switching at f <sub>1</sub> = 10 MHz at 50% duty cycle	V <sub>IN</sub> ≤ 0.2 V or V <sub>IN</sub> ≥ V <sub>CC</sub> – 0.2 V	0.7	1.4				mA	
			V <sub>IN</sub> = 3.4 V or GND	1	2.4					
		Eight bits switching at f <sub>1</sub> = 2.5 MHz at 50% duty cycle	V <sub>IN</sub> = 0.2 V or V <sub>IN</sub> ≥ V <sub>CC</sub> – 0.2 V	1.3	2.6					
			V <sub>IN</sub> = 3.4 V or GND	3.3	10.6					
	V <sub>CC</sub> = 5.25 V, Outputs open, OE <sub>A</sub> = OE <sub>B</sub> = GND	One bit switching at f <sub>1</sub> = 10 MHz at 50% duty cycle	V <sub>IN</sub> ≤ 0.2 V or V <sub>IN</sub> ≥ V <sub>CC</sub> – 0.2 V				0.7	1.4		
			V <sub>IN</sub> = 3.4 V or GND				1	2.4		
		Eight bits switching at f <sub>1</sub> = 2.5 MHz at 50% duty cycle	V <sub>IN</sub> = 0.2 V or V <sub>IN</sub> ≥ V <sub>CC</sub> – 0.2 V				1.3	2.6		
			V <sub>IN</sub> = 3.4 V or GND				3.3	10.6		
C <sub>i</sub>				5	10		5	10	pF	
C <sub>O</sub>				9	12		9	12	pF	

† Typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

#  $I_C = I_{CC} + \Delta I_{CC} \times D_H \times N_T + I_{CCD} (f_0/2 + f_1 \times N_1)$

Where:

$I_C$  = Total supply current

$I_{CC}$  = Power-supply current with CMOS input levels

$\Delta I_{CC}$  = Power-supply current for a TTL high input ( $V_{IN} = 3.4 \text{ V}$ )

$D_H$  = Duty cycle for TTL inputs high

$N_T$  = Number of TTL inputs at  $D_H$

$I_{CCD}$  = Dynamic current caused by an input transition pair (HLH or LHL)

$f_0$  = Clock frequency for registered devices, otherwise zero

$f_1$  = Input signal frequency

$N_1$  = Number of inputs changing at  $f_1$

All currents are in milliamperes and all frequencies are in megahertz.

|| Values for these conditions are examples of the  $I_{CC}$  formula.

**switching characteristics over operating free-air temperature range (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CY54FCT244T		CY54FCT244AT		CY54FCT244CT		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	D	O	1.5	7	1.5	5.1	1.5	4.6	ns
t <sub>PHL</sub>			1.5	7	1.5	5.1	1.5	4.6	
t <sub>PZH</sub>	$\overline{OE}$	O	1.5	8.5	1.5	6.5	1.5	6.5	ns
t <sub>PZL</sub>			1.5	8.5	1.5	6.5	1.5	6.5	
t <sub>PHZ</sub>	$\overline{OE}$	O	1.5	7.5	1.5	5.9	1.5	5.7	ns
t <sub>PLZ</sub>			1.5	7.5	1.5	5.9	1.5	5.7	

**switching characteristics over operating free-air temperature range (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CY74FCT244T		CY74FCT244AT		CY74FCT244CT		CY74FCT244DT		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	D	O	1.5	6.5	1.5	4.6	1.5	4.1	1.5	3.6	ns
t <sub>PHL</sub>			1.5	6.5	1.5	4.6	1.5	4.1	1.5	3.6	
t <sub>PZH</sub>	$\overline{OE}$	O	1.5	8	1.5	6.2	1.5	5.8	1.5	4.8	ns
t <sub>PZL</sub>			1.5	8	1.5	6.2	1.5	5.8	1.5	4.8	
t <sub>PHZ</sub>	$\overline{OE}$	O	1.5	7	1.5	5.6	1.5	5.2	1.5	4	ns
t <sub>PLZ</sub>			1.5	7	1.5	5.6	1.5	5.2	1.5	4	

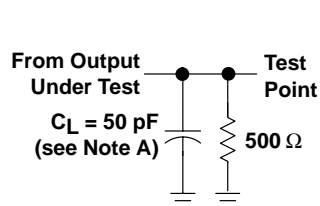
# CY54FCT244T, CY74FCT244T

## 8-BIT BUFFERS/LINE DRIVERS

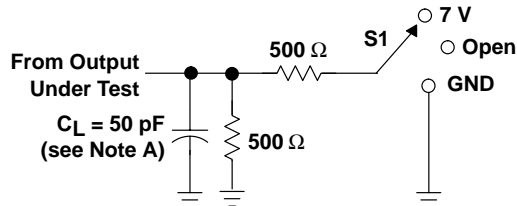
### WITH 3-STATE OUTPUTS

SCCS071 – OCTOBER 2001

#### PARAMETER MEASUREMENT INFORMATION

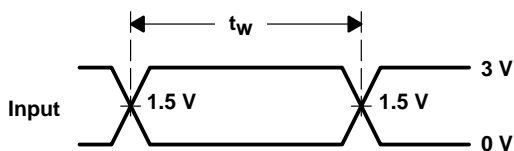


LOAD CIRCUIT FOR  
TOTEM-POLE OUTPUTS

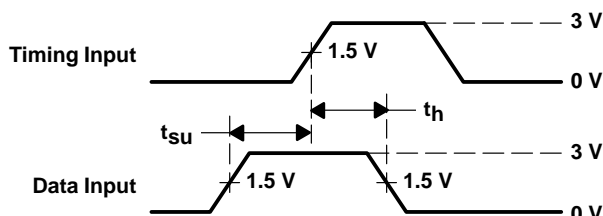


LOAD CIRCUIT FOR  
3-STATE OUTPUTS

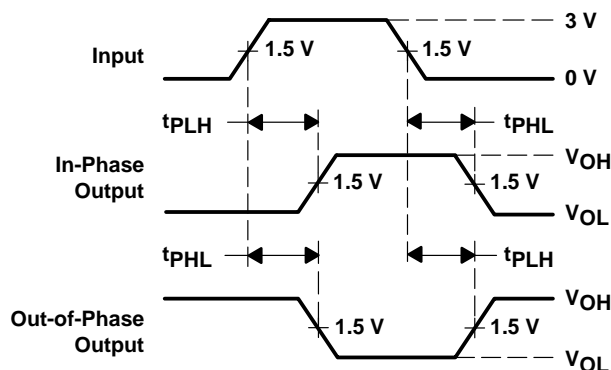
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	7 V
$t_{PHZ}/t_{PZH}$	Open



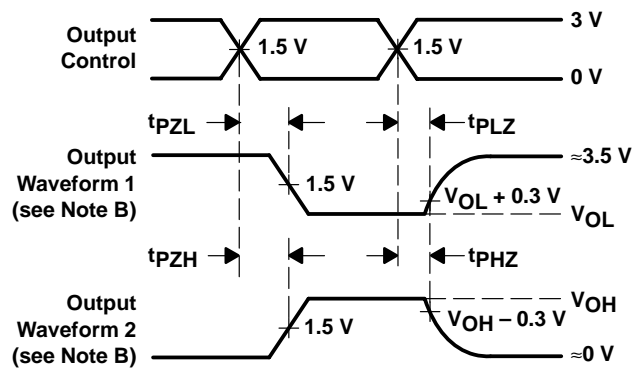
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9220301M2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9220301M2A CY54FCT 244TLMB	<a href="#">Samples</a>
5962-9220301MRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9220301MR A CY54FCT244TDMB	<a href="#">Samples</a>
5962-9220301MSA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9220301MS A CY54FCT244TW	<a href="#">Samples</a>
5962-9220302M2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9220302M2A CY54FCT 244ATLMB	<a href="#">Samples</a>
5962-9220302MRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9220302MR A CY54FCT244ATDM B	<a href="#">Samples</a>
5962-9220302MSA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9220302MS A CY54FCT244ATW	<a href="#">Samples</a>
5962-9220303M2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9220303M2A	<a href="#">Samples</a>
5962-9220303MRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9220303MR A CY54FCT244CTDM B	<a href="#">Samples</a>
5962-9220303MSA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9220303MS A CY54FCT244CTW	<a href="#">Samples</a>
CY54FCT244ATDMB	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9220302MR A CY54FCT244ATDM B	<a href="#">Samples</a>
CY54FCT244ATLMB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9220302M2A CY54FCT	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
										244ATLMB	
CY54FCT244ATW	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9220302MS A CY54FCT244ATW	<a href="#">Samples</a>
CY54FCT244CTDMB	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9220303MR A CY54FCT244CTDM B	<a href="#">Samples</a>
CY54FCT244CTW	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9220303MS A CY54FCT244CTW	<a href="#">Samples</a>
CY54FCT244TDMB	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9220301MR A CY54FCT244TDMB	<a href="#">Samples</a>
CY54FCT244TLMB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9220301M2A CY54FCT 244TLMB	<a href="#">Samples</a>
CY54FCT244TW	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9220301MS A CY54FCT244TW	<a href="#">Samples</a>
CY74FCT244ATPC	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	CY74FCT244ATPC	<a href="#">Samples</a>
CY74FCT244ATPCE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	CY74FCT244ATPC	<a href="#">Samples</a>
CY74FCT244ATQCT	ACTIVE	SSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT244A	<a href="#">Samples</a>
CY74FCT244ATQCTE4	ACTIVE	SSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT244A	<a href="#">Samples</a>
CY74FCT244ATQCTG4	ACTIVE	SSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT244A	<a href="#">Samples</a>
CY74FCT244ATSOC	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT244A	<a href="#">Samples</a>
CY74FCT244ATSOCG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT244A	<a href="#">Samples</a>
CY74FCT244ATSOCT	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT244A	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CY74FCT244ATSOCTE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT244A	<a href="#">Samples</a>
CY74FCT244CTQCT	ACTIVE	SSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT244C	<a href="#">Samples</a>
CY74FCT244CTSOC	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT244C	<a href="#">Samples</a>
CY74FCT244CTSOCT	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	-40 to 85		
CY74FCT244CTSOCTG4	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	-40 to 85		
CY74FCT244DTQCT	ACTIVE	SSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT244D	<a href="#">Samples</a>
CY74FCT244DTSOC	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT244D	<a href="#">Samples</a>
CY74FCT244DTSOCT	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT244D	<a href="#">Samples</a>
CY74FCT244DTSOCTE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT244D	<a href="#">Samples</a>
CY74FCT244TQCT	ACTIVE	SSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT244	<a href="#">Samples</a>
CY74FCT244TSOC	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT244	<a href="#">Samples</a>
CY74FCT244TSOCG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT244	<a href="#">Samples</a>
CY74FCT244TSOCT	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT244	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

---

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CY74FCT244ATQCT	SSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CY74FCT244ATSOCT	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
CY74FCT244CTQCT	SSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CY74FCT244DTQCT	SSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CY74FCT244DTSOCT	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
CY74FCT244TQCT	SSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CY74FCT244TSOCT	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1

## TAPE AND REEL BOX DIMENSIONS



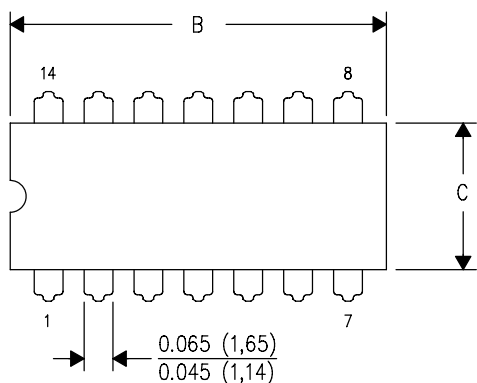
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CY74FCT244ATQCT	SSOP	DBQ	20	2500	367.0	367.0	38.0
CY74FCT244ATSOCT	SOIC	DW	20	2000	367.0	367.0	45.0
CY74FCT244CTQCT	SSOP	DBQ	20	2500	367.0	367.0	38.0
CY74FCT244DTQCT	SSOP	DBQ	20	2500	367.0	367.0	38.0
CY74FCT244DTSOCT	SOIC	DW	20	2000	367.0	367.0	45.0
CY74FCT244TQCT	SSOP	DBQ	20	2500	367.0	367.0	38.0
CY74FCT244TSOCT	SOIC	DW	20	2000	367.0	367.0	45.0

J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

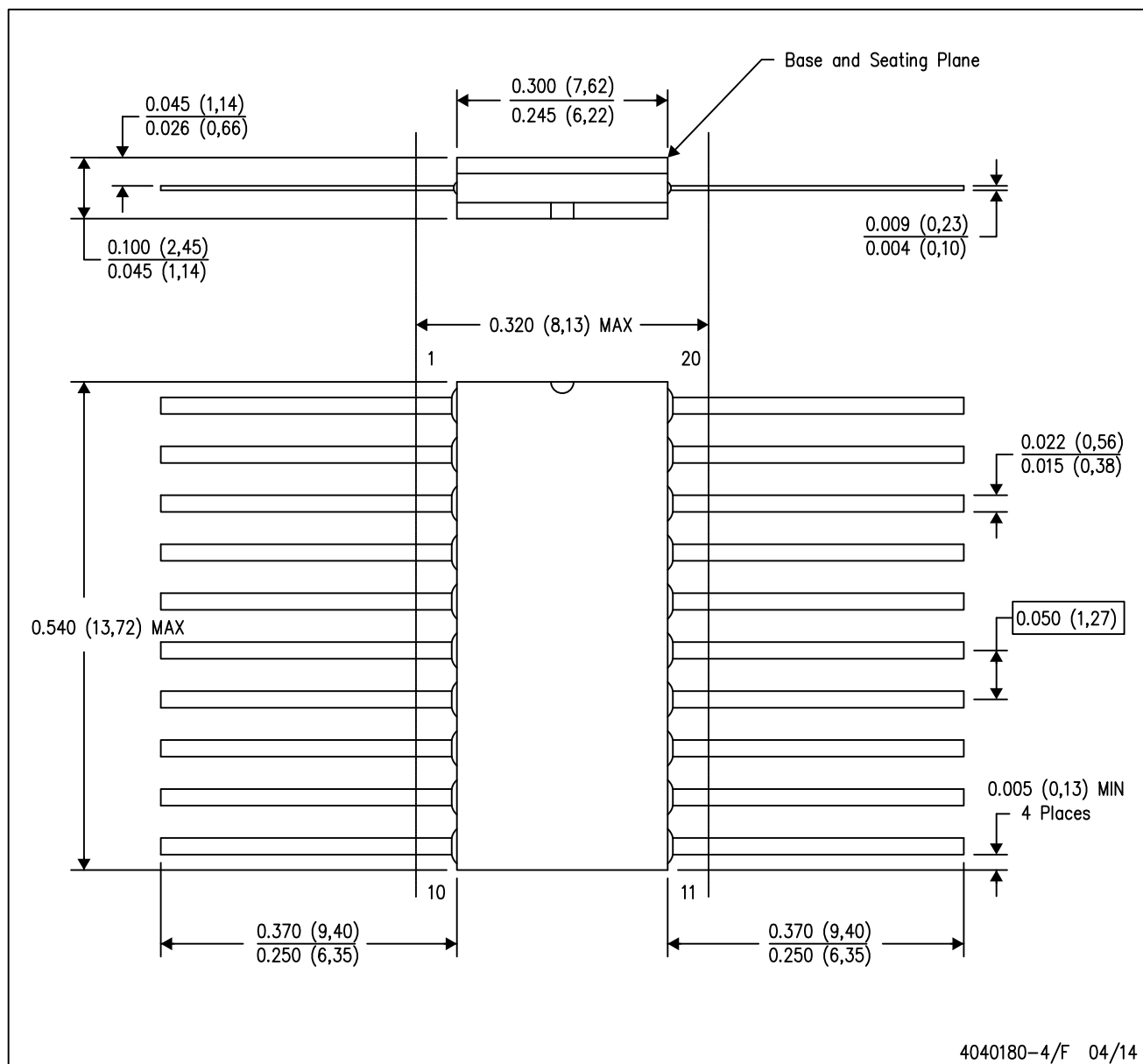


4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK

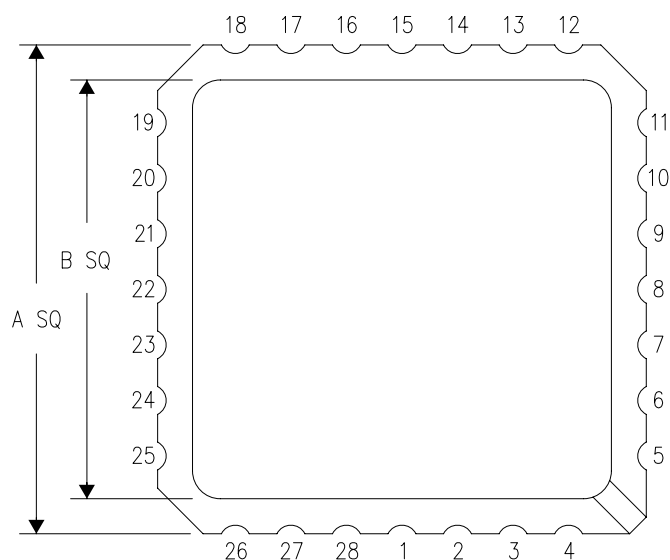




FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



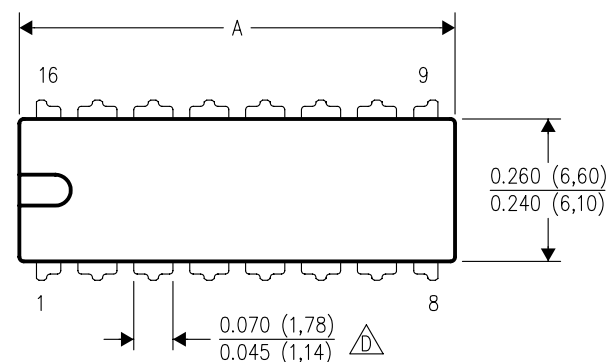
4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004

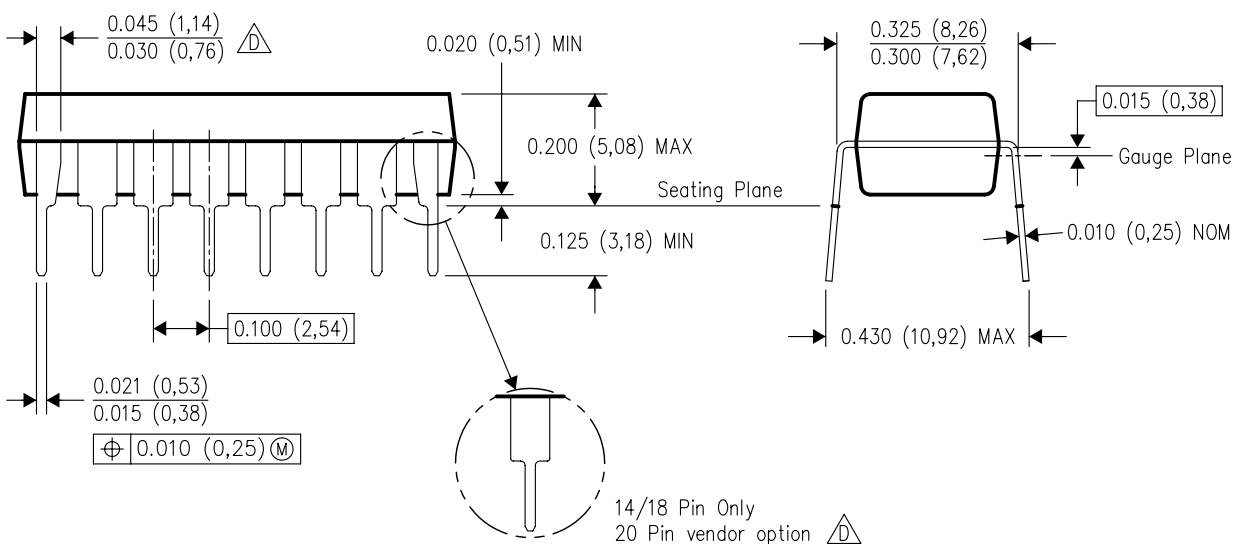
N (R-PDIP-T\*\*)

16 PINS SHOWN

# PLASTIC DUAL-IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



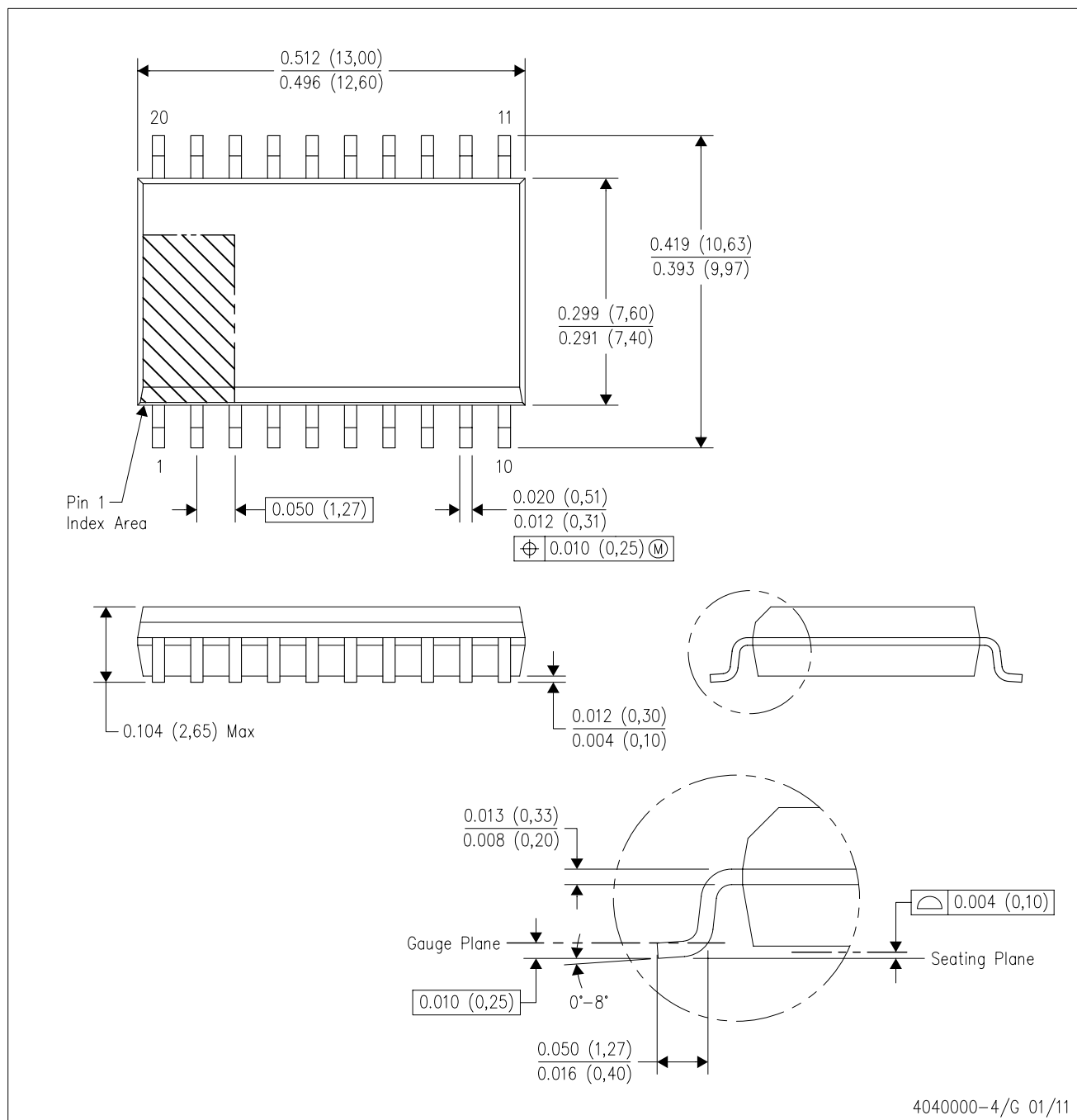
4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).  
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW (R-PDSO-G20)

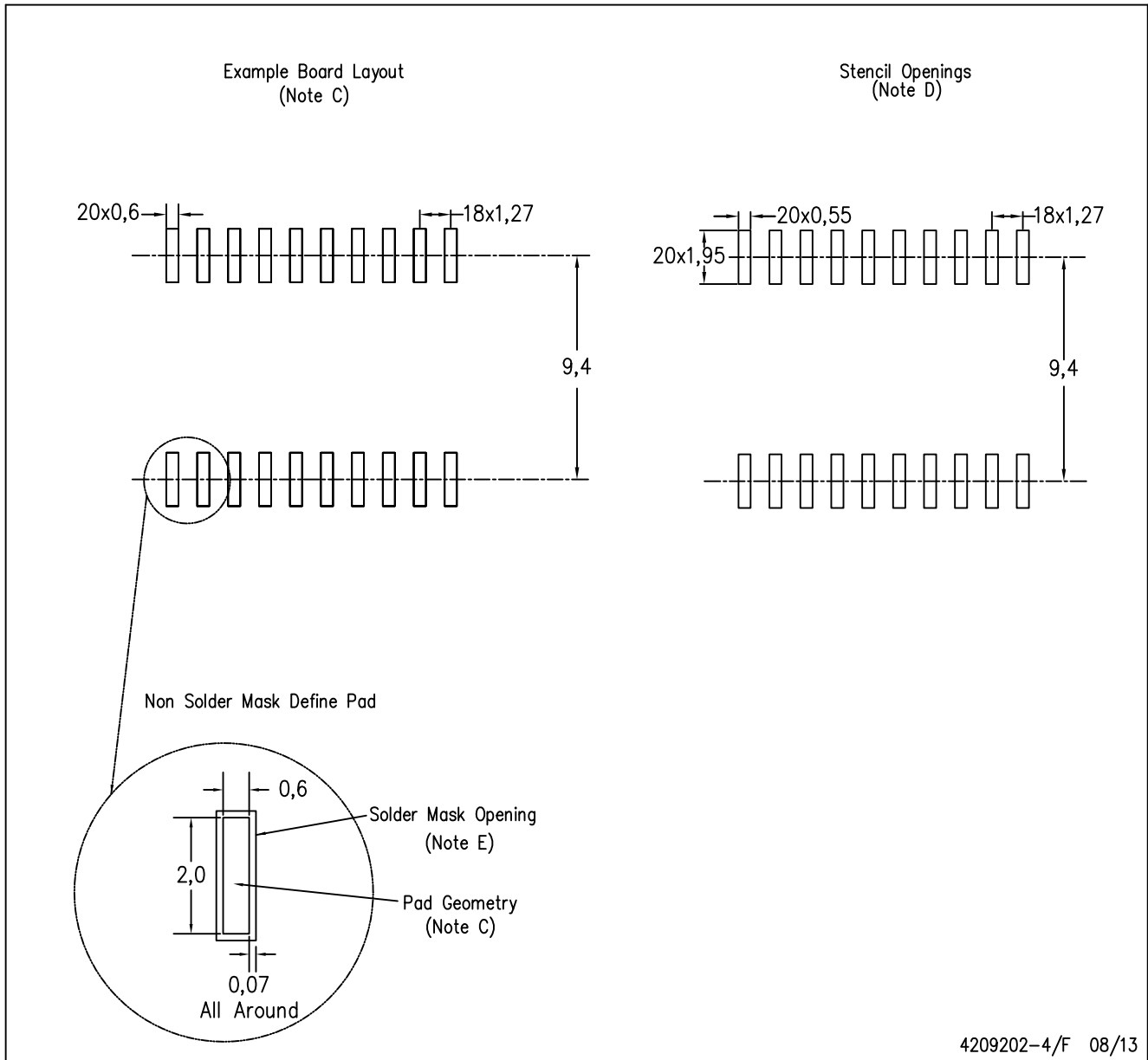
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AC.

DW (R-PDSO-G20)

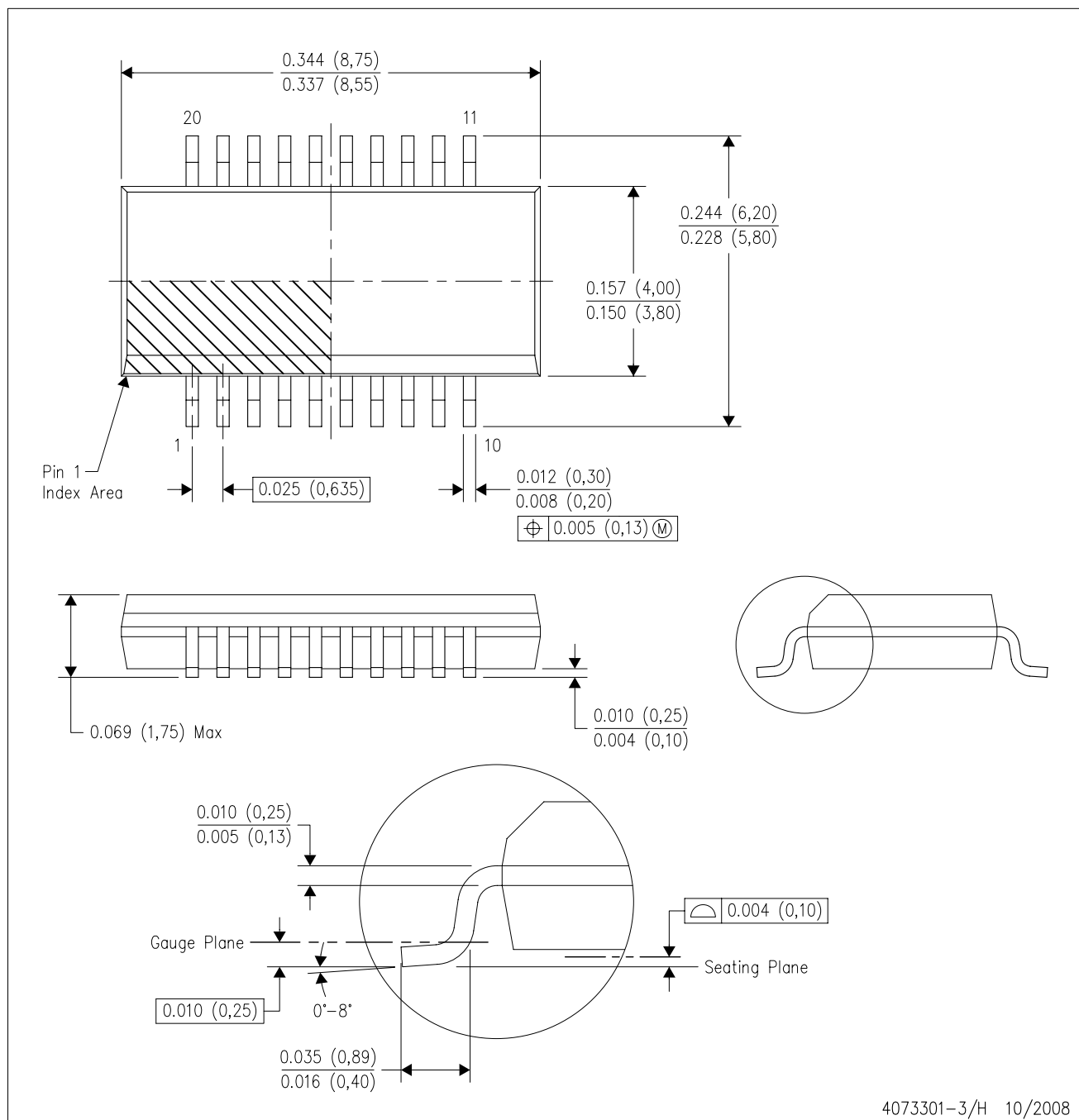
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Refer to IPC7351 for alternate board design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DBQ (R-PDSO-G20)

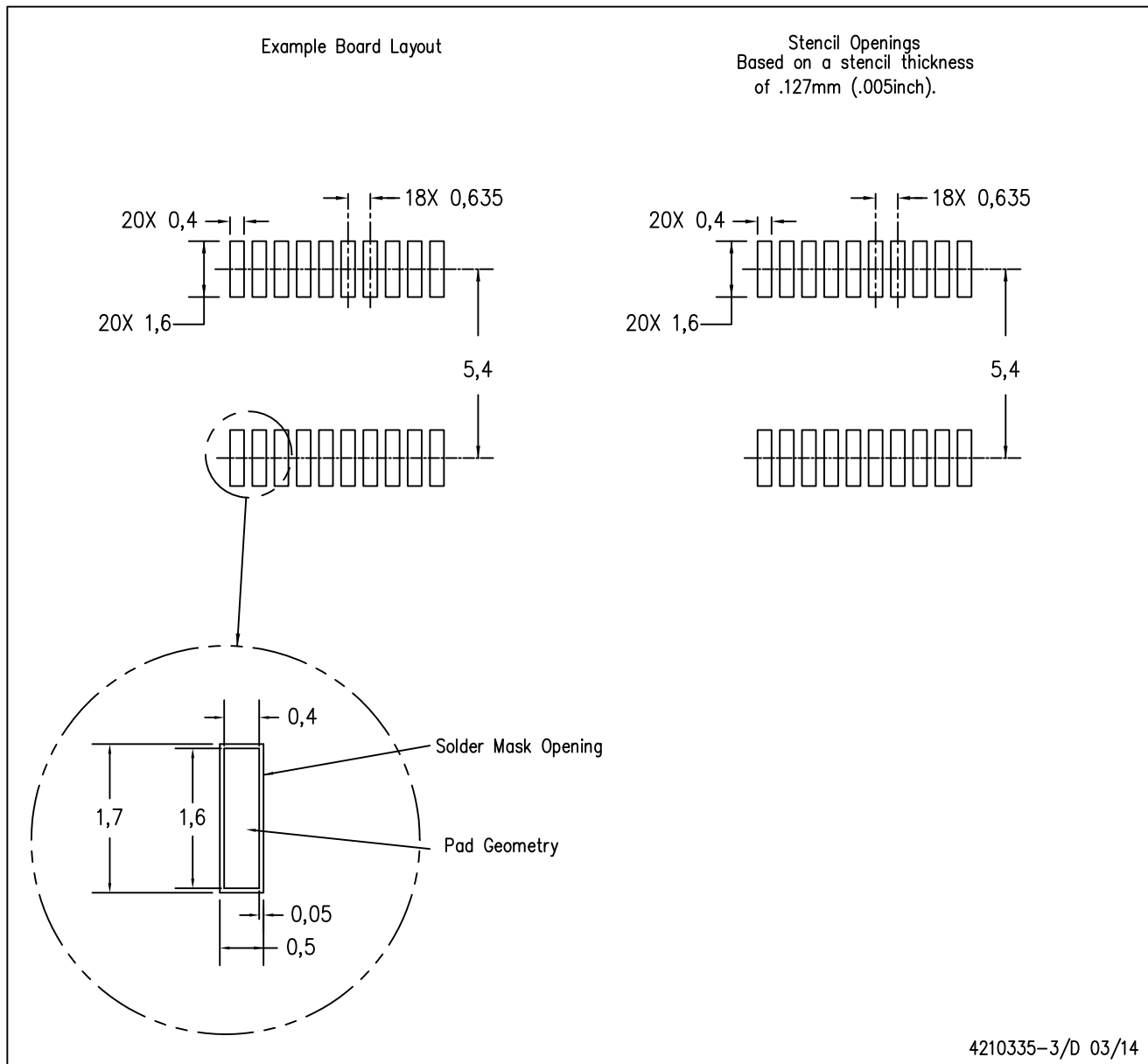
# PLASTIC SMALL-OUTLINE PACKAGE



- NOTES: A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.  
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.  
D. Falls within JEDEC MO-137 variation AD.

DBQ (R-PDSO-G20)

PLASTIC SMALL OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

### Products

Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>
DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>
RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>
OMAP Applications Processors	<a href="http://www.ti.com/omap">www.ti.com/omap</a>
Wireless Connectivity	<a href="http://www.ti.com/wirelessconnectivity">www.ti.com/wirelessconnectivity</a>

### Applications

Automotive and Transportation	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
Communications and Telecom	<a href="http://www.ti.com/communications">www.ti.com/communications</a>
Computers and Peripherals	<a href="http://www.ti.com/computers">www.ti.com/computers</a>
Consumer Electronics	<a href="http://www.ti.com/consumer-apps">www.ti.com/consumer-apps</a>
Energy and Lighting	<a href="http://www.ti.com/energy">www.ti.com/energy</a>
Industrial	<a href="http://www.ti.com/industrial">www.ti.com/industrial</a>
Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
Space, Avionics and Defense	<a href="http://www.ti.com/space-avionics-defense">www.ti.com/space-avionics-defense</a>
Video and Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>

### TI E2E Community

[e2e.ti.com](http://e2e.ti.com)