



Szu Chi Chung

POSTDOCTORAL RESEARCHER

Institute of Statistical Science, Academia Sinica.

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"If you can imagine it, you can achieve it. If you can dream it, you can become it."

Interests

I am currently working as a postdoctoral researcher at the Institute of Statistical Science, Academia Sinica. I have received Ph.D. degree from National Chiao Tung University in Sep. 2017. I am interested in the area of data analysis and data security, including but not limited to:

Field	Machine learning, Clustering analysis and dimensional reduction, Cryo-EM and medical image analysis, Side-channel analysis, Security system design
Skill	Software programming (Python, Java, C, C++, CUDA), Big data framework (Spark, Hadoop), FPGA prototyping and hardware design

Education

	PH.D. IN INSTITUTE OF ELECTRONICS <i>National Chiao Tung University, Hsinchu, Taiwan.</i> <ul style="list-style-type: none">• Research Group: Star group of Silicon implementation lab (SI2)• Advisor: Chen-Yi Lee• Thesis topic: Stream Cipher and ID-Based Crypto Systems for IoT Applications• GPA 4.3/4.3, 34 credits	Sep. 2011 - Sep. 2017
	BS IN EECS UNDERGRADUATE HONORS PROGRAM <i>National Chiao Tung University, Hsinchu, Taiwan.</i> <ul style="list-style-type: none">• GPA 4.3/4.3, 159 credits	Sep. 2007 - Jun. 2011
	EXCHANGE STUDENT IN EECS <i>University of Illinois Urbana-Champaign, USA</i> <ul style="list-style-type: none">• GPA 4.0/4.0, 13 credits	Aug. 2010 - DEC. 2010
	HIGH SCHOOL GRADUATION <i>National Hualien High School, Taiwan</i>	Sep. 2004 - Jun. 2007

Honors & Awards

2020	Best Paper Award , 2020 ICCM Best Paper Silver Award	<i>International Congress of Chinese Mathematicians</i>
2020	Participants , Global Young Scientists Summit	<i>National Research Foundation, Singapore</i>
2019	Third Place , Poster Competition of Institute of Statistical Science	<i>Academia Sinica</i>
2016	Dragon Gate Program Scholarship (科技部龍門計畫) , Visiting Student Researcher to Stanford University	<i>Ministry Of Science and Technology</i>
2013	Second Prize , IE Design Contest, Core Technology Category (教育部 IE 競賽)	<i>Ministry Of Education</i>
2012	Bronze Medal Award , 12th Macronix Golden Silicon Award	<i>Macronix Inc.</i>
2012	First Prize , IC Design Contest, Cell-Based IC Category (教育部 IC 競賽)	<i>Ministry Of Education</i>
2010	EECS Study Aboard Scholarship , Exchange student program to University of Illinois Urban-Champaign	<i>National Chiao Tung University</i>
2007	Second Prize , Programming Contest for Freshman	<i>National Chiao Tung University</i>

Academic and Working Experiences



POSTDOCTORAL RESEARCHER

Institute of Statistical Science, Academia Sinica, Taiwan.

- Laboratory Director: I-Ping Tu [↗](#)
- Research Group: Statistical Analysis for Biological Image Data [↗](#)

Dec. 2017 - PRESENT



POSTDOC SEMINARS HOST

Institute of Statistical Science, Academia Sinica, Taiwan.

- Website: Postdoc Seminars [↗](#)

Aug. 2018 - Jan. 2019



POSTDOCTORAL RESEARCHER

Institute of Electronics, National Chiao Tung University, Taiwan.

- Laboratory Director: Chen-Yi Lee [↗](#)
- Research Group: Security for Trust And Reliability Group [↗](#)

Oct. 2017 - Nov. 2017



VISITING STUDENT RESEARCHER

Department of Statistics, Stanford University, USA.

- Advisor: Wing-Hung Wong [↗](#)
- Collaborator: Tung-Yu Wu

Nov. 2016 - Aug. 2017



TEACHING ASSISTANT

National Chiao Tung University, Taiwan.

- Course: Introduction to VLSI Design [↗](#)
- Lecturer: Chen-Yi Lee [↗](#)

Fall 2015



TEACHING ASSISTANT

National Chiao Tung University, Taiwan.

- Course: Integrated Circuit Design Laboratory [↗](#)
- Lecturer: Chen-Yi Lee [↗](#) and Shyh-Jye Jou [↗](#)

Fall 2011, Fall 2013 and Fall 2014



TEACHING ASSISTANT

National Chiao Tung University, Taiwan.

- Course: Digital Circuit and System
- Lecturer: Chen-Yi Lee [↗](#)

Fall 2014



TEACHING ASSISTANT

National Chiao Tung University, Taiwan.

- Course: Electronics Laboratory (I) and (II)
- Lecturer: Meng-Wei Wang [↗](#)

2010-2014



TEACHING ASSISTANT

National Chiao Tung University, Taiwan.

- Course: Digital Circuit Laboratory
- Lecturer: Chien Chen [↗](#)

2012

Invited Talks

- 2020/12/14, "Dimension reduction and clustering method for noisy high-dimensional images and application to Cryogenic Electron Microscopy [↗](#)", *NCTS Optimization Day for Young Researchers* , (2020).
- 2020/12/12, "Two-stage dimension reduction method and application to Cryogenic Electron Microscopy [↗](#)", *Waseda University-Academia Sinica joint workshop* , (2020).
- 2020/10/08, "Accelerated Cryo-EM Workflow [↗](#)", *GPU Technology Conference 2020* , (2020).
- 2019/12/27, "ASCEP - A Speedy and robust Cryo-EM processing Platform [↗](#)", *2019 Symposium On Statistical Analysis For Molecular Imaging And Biorhythms* , (2019).
- 2018/12/11, "A Dimension Reduction Method For Cryo-EM Image Processing [↗](#)", *2018 Workshop On High Dimensional Statistical Analysis* , (2018).
- 2018/03/14, "Scalable Video Analysis Framework [↗](#)", *Postdoc Seminars* , (2018).

Dissertation

- Szu-Chi Chung, “Stream Cipher and ID-Based Crypto Systems for IoT Applications ”, *PhD dissertation*, (2017).


Research Projects

CRYO-EM AND MEDICAL IMAGE PROCESSING

Dec. 2017 - PRESENT

Academia Sinica, Taiwan



- Develop dimension reduction and clustering methods
- Accelerate clustering and alignment methods for cryo-EM
- Develop a unified platform for integrating different cryo-EM packages (Collaborating with Scipion team )

NOVATEK-NCTU SIDE-CHANNEL ANALYSIS PROJECT

Jan. 2019 - PRESENT

Novatek Microelectronics, Taiwan



- Developing side-channel countermeasure for SM2/SM4 circuits
- Examining side-channel leakage using hypothesis testing

SCALABLE VIDEO ANALYSIS FRAMEWORK

Nov. 2016 - Sep. 2017

Stanford, USA



- Bridging the gap between distributed computation framework and traditional computer vision modules
- Provides a solution to deal with distributed video/image analysis in big data framework

BIG DATA SECURITY PROJECT

Sep. 2014 - Sep. 2017

Ministry of Science and Technology, Taiwan



- Develop several high throughput Bilinear Pairing modules to support cloud security protocols
- Propose guidelines to design security modules for big data system

DELTA-NCTU IOT PROJECT

Mar. 2014 - Mar. 2016

Delta Inc., Taiwan



- Develop stream ciphers that are suited to IoT scenario
- Design several implementation attacks and countermeasures
- Conduct side-channel attacks on the embedded system

E-HOME PROJECT






Aug. 2011 - Jun. 2014

National Science Council, Taiwan



- Develop AES and ECC modules that are suited for IoT use
- Integrate with other submodules including computer vision, wireless and memory modules

Journal Paper

- Szu-Chi Chung, Hsin-Hung Lin, Tien-You Liu, Kuen-Phon Wu, Wei-Hau Chang, and I-Ping Tu, “Accelerating the stream of single particle cryo-EM analysis with DRMRA ”, *In preparation.*, (2020).
- Wei-Hau Chang, I-Kuen Tsai, Hsin-Hung Lin, Shih-Hsin Huang, Szu-Chi Chung, I-Ping Tu, Steve Yu, Sunney I. Chan, “Cryo-EM structure of particulate methane monooxygenase at 2.5 Å ”, *Submitted to Nature Communications.*, (2020).
- Tze Leung Lai, Shao-Hsuan Wang, Yi-Ching Yao, Szu-Chi Chung, Wei-Hau Chang, and I-Ping Tu, “Cryo-EM: Breakthroughs in Chemistry, Structural Biology, and Statistical Underpinnings ”, *Submitted to Statistical Science*, (2020).
- Szu-Chi Chung, Shao-Hsuan Wang, Po-Yao Niu, Su-Yun Huang, Wei-Hau Chang, I-Ping Tu, “Two-stage dimension reduction for noisy high-dimensional images and application to Cryogenic Electron Microscopy ”, *Annals of Mathematical Sciences and Applications* **5**, (2020). (Receive 2020 ICCM Best Paper Silver Award).
- Szu-Chi Chung, Hsin-Hung Lin, Po-Yao Niu, Shih-Hsin Huang, I-Ping Tu, Wei-Hau Chang, “Pre-Pro is a Fast Pre-Processor for Single-Particle Cryo-EM by Enhancing 2D Classification ”, *Nature Communications Biology* **3**, (2020).

- Szu-Chi Chung, Chun-Yuan Yu, Sung-Shine Lee, Hsie-Chia Chang, Chen-Yi Lee, “An Improved DPA Countermeasure Based on UDRPG for IoT Applications ”, *IEEE Transactions on Circuits and Systems I (TCAS-I)* **64**, 2522–2531 (2017).
- Szu-Chi Chung, Jing-Yu Wu, Hsing-Ping Fu, Jen-Wei Lee, Hsie-Chia Chang, Chen-Yi Lee, “Efficient Hardware Architecture of η_T Pairing Accelerator Over Characteristic Three ”, *IEEE Transactions on Very Large Scale Integration (VLSI) System* **23**, 88–97 (2015).
- Jen-Wei Lee, Szu-Chi Chung, Hsie-Chia Chang, Chen-Yi Lee, “Efficient Power-Analysis-Resistant Dual-Field Elliptic Curve Cryptographic Processor Using Heterogeneous Dual-Processing-Element Architecture ”, *IEEE Transactions on Very Large Scale Integration (VLSI) System* **22**, 49–61 (2014).

Conference Paper

- Szu-Chi Chung, Cheng-Yu Hung, Huei-Lun Siao, Hung-Yi Wu, Wei-Hau Chang, I-Ping Tu, “Cryo-RALib – a modular library for accelerating alignment in cryo-EM ”, *plan to submit to IEEE ICIP*, (2020).
- Szu-Chi Chung, Shao-Hsuan Wang, Po-Yao Niu, Su-Yun Huang, I-Ping Tu, Wei-Hau Chang, “Accelerated cryo-EM workflow ”, *The 29th South Taiwan Statistics Conference*, (2020).
- Szu-Chi Chung, Shih-Hao Huang, Po-Yao Niu, Su-Yun Huang, Wei-Hau Chang, I-Ping Tu, “A Two-Stage Dimension Reduction Method For Cryo-EM Image Processing ”, *Microscopy and Microanalysis 2019 Meeting*, (2019).
- Szu-Chi Chung, Po-Yao Niu, Su-Yun Huang, Wei-Hau Chang, I-Ping Tu, “A Dimension Reduction Method for cryo-EM Image Analysis ”, *The 27th South Taiwan Statistics Conference*, (2018).
- Sung-Shine Lee, Szu-Chi Chung, Chun-Yuan Yu, Hsie-Chia Chang, Chen-Yi Lee, “A New Power Analysis Attack on Stream cipher Trivium-64 ”, *VLSI Design/CAD Symposium (VLSI-CAD)*, (2015). Details. 
- Szu-Chi Chung, Sung-Shine Lee, Hsie-Chia Chang, Chen-Yi Lee, “Implementing Bilinear Pairing Accelerator Using Residue Number System ”, *VLSI Design/CAD Symposium (VLSI-CAD)*, (2014).
- Jen-Wei Lee, Szu-Chi Chung, Hsie-Chia Chang, Chen-Yi Lee, “A $3.40ms/GF(p_{521})$ and $2.77ms/GF(2^{521})$ DF-ECC Processor with Side-Channel Attack Resistance ”, *International Solid-State Circuits Conference (ISSCC)*, 50–51 (2013).
- Jen-Wei Lee, Szu-Chi Chung, Hsie-Chia Chang, Chen-Yi Lee, “An Efficient Countermeasure against Correlation Power-Analysis Attacks with Randomized Montgomery Operations for DF-ECC Processor ”, *Conference on Cryptographic Hardware and Embedded Systems (CHES)*, 548–564 (2012).
- Szu-Chi Chung, Jen-Wei Lee, Hsie-Chia Chang, Chen-Yi Lee, “High-performance elliptic curve cryptographic processor over $GF(p)$ with SPA resistance ”, *IEEE International Symposium on Circuits and Systems (ISCAS)*, 1456–1459 (2012).

Patents

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| 2019 | Cracking devices and methods thereof , 10277392 | US Patent |
| 2019 | Encryption/decryption apparatus and power analysis protecting method thereof , 10326586 | US Patent |


References

Dr. I-Ping Tu 

(Current Advisor)

Institute of Statistical Science

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Dr. Chen-Yi Lee 

(Ph.D. Advisor)

Department of Electronics Engineering

National Chiao Tung University


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Dr. Hsie-Chia Chang 

(Ph.D. Co-Advisor)

Department of Electronics Engineering

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Dr. Wing Hung Wong 

(Advisor at Stanford)

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