



Szu Chi Chung

POSTDOCTORAL RESEARCHER

✉ steve2003121@gmail.com | 🏠 [homepage](#) | 📱 [phonchi](#) | 📄 [steve](#)

"If you can imagine it, you can achieve it. If you can dream it, you can become it."

Interests

Currently working as a postdoctoral researcher in Institute of Statistical Science, Academia Sinica. Have received Ph.D degree from National Chiao Tung University in Sep. 2017. I am interested in the area of data analysis and data security, including but not limited to:

Field Machine learning, Clustering analysis and dimensional reduction, Cryo-EM and medical image analysis, Side-channel analysis, Security system design

Skill Software programming (Python, Java, C, C++), FPGA prototyping, ASIC chip design

Education

PHD. ELECTRICAL ENGINEERING

Sep. 2011 - Sep. 2017



National Chiao Tung University, Hsinchu, Taiwan.

- Research Group: Star group of Silicon implementation lab (SI2) [🔗](#)
- Advisor: Chen-Yi Lee
- Thesis topic: Stream Cipher and ID-Based Crypto Systems for IoT Applications
- GPA 4.0/4.0, 34 credits



BACHELOR OF EECS UNDERGRADUATE HONORS PROGRAM

Sep. 2007 - Jun. 2011

National Chiao Tung University, Hsinchu, Taiwan.

- GPA 4.0/4.0, 144 credits



EXCHANGE STUDENT IN EECS

Aug. 2010 - DEC. 2010

University of Illinois Urbana-Champaign, USA

- GPA 4.0/4.0, 13 credits



HIGH SCHOOL GRADUATION

Sep. 2004 - Jun. 2007

National Hualien High School, Taiwan

Honors & Awards

2020	Participants , Global Young Scientists Summit	<i>National Research Foundation, Singapore</i>
2019	Third Place , Poster Competition of Institute of Statistical Science	<i>Academia Sinica</i>
2016	Dragon Gate Program Scholarship (科技部龍門計畫) , Visiting Student Researcher to Stanford University	<i>Ministry Of Science and Technology</i>
2013	Second Prize , IE Design Contest, Core Technology Category (教育部 IE 競賽)	<i>Ministry Of Education</i>
2012	Bronze Medal Award , 12th Macronix Golden Silicon Award	<i>Macronix Inc.</i>
2012	First Prize , IC Design Contest, Cell-Based IC Category (教育部 IC 競賽)	<i>Ministry Of Education</i>
2010	EECS Study Aboard Scholarship , Exchange student program to University of Illinois Urban-Champaign	<i>National Chiao Tung University</i>
2007	Second Prize , Programming Contest for Freshman	<i>National Chiao Tung University</i>

Academic and Working Experiences



POSTDOCTORAL RESEARCHER

Dec. 2017 - PRESENT

Institute of Statistical Science, Academia Sinica, Taiwan.

- Laboratory Director: I-Ping Tu [↗](#)
- Research Group: Statistical Analysis for Biological Image Data [↗](#)



POSTDOC SEMINARS HOST

Aug. 2018 - Jan. 2019

Institute of Statistical Science, Academia Sinica, Taiwan.

- Website: Postdoc Seminars [↗](#)



POSTDOCTORAL RESEARCHER

Oct. 2017 - Nov. 2017

National Chiao Tung University, Taiwan.

- Laboratory Director: Chen-Yi Lee [↗](#)
- Research Group: Star group of Silicon implementation lab (SI2) [↗](#)



VISITING STUDENT RESEARCHER

Nov. 2016 - Aug. 2017

Stanford University, USA.

- Project: Scalable video analysis framework
- Advisor: Wing-Hung Wong [↗](#)
- Collaborator: Tung-Yu Wu



TEACHING ASSISTANT

Fall 2015

National Chiao Tung University, Taiwan.

- Course: Introduction to VLSI Design
- Lecturer: Chen-Yi Lee [↗](#)



TEACHING ASSISTANT

Fall 2011, Fall 2013 and Fall 2014

National Chiao Tung University, Taiwan.

- Course: Integrated Circuit Design Laboratory
- Lecturer: Chen-Yi Lee [↗](#) and Shyh-Jye Jou [↗](#)



TEACHING ASSISTANT

Fall 2014

National Chiao Tung University, Taiwan.

- Course: Digital Circuit and System
- Lecturer: Chen-Yi Lee [↗](#)



TEACHING ASSISTANT

2010-2014

National Chiao Tung University, Taiwan.

- Course: Electronics Laboratory (I) and (II)
- Lecturer: Meng-Wei Wang [↗](#)



TEACHING ASSISTANT

2012

National Chiao Tung University, Taiwan.

- Course: Digital Circuit Laboratory
- Lecturer: Chien Chen [↗](#)

Invited Talks

2. 2018/12/11, "A Dimension Reduction Method For Cryo-EM Image Processing [↗](#)", *2018 Workshop On High Dimensional Statistical Analysis*, (2018).
1. 2018/3/14, "Scalable Video Analysis Framework [↗](#)", *Institute of Statistical Science, Academia Sinica*, (2018).






Dessertation

1. Szu-Chi Chung, "Stream Cipher and ID-Based Crypto Systems for IoT Applications [↗](#)", *PHD Dessertation*, (2016).

Academic Services

2016-2017 **Reviewer**, IEEE Transactions on Circuits and Systems I (TCAS-I)
 2016-2017 **Reviewer**, IEEE Transactions on Very Large Scale Integration Systems (TVLSI)
 2016 **Reviewer**, IEEE Transactions on Computers

Research Projects

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|---|---|-----------------------|
|  | CRYO-EM IMAGE PROCESSING
<i>Academia Sinica, Taiwan</i> <ul style="list-style-type: none"> • Develop dimension reduction and clustering methods for cryo-EM • Develop platform for integrating cryo-EM packages | Dec. 2017 - PRESENT |
|  | SCALABLE VIDEO ANALYSIS FRAMEWORK
<i>Stanford, USA</i> <ul style="list-style-type: none"> • Bridging the gap between spark analytic framework and traditional computer vision modules • Provides a solution to deal with distributed video/image analysis in big data framework | Nov. 2016 - Sep. 2017 |
|  | BIG DATA SECURITY PROJECT
<i>Ministry of Science and Technology, Taiwan</i> <ul style="list-style-type: none"> • Develop several high throughput Bilinear Pairing modules to support cloud security protocols • Propose guidelines to design security modules for big data system | Sep. 2014 - Sep. 2017 |
|  | DELTA-NCTU IOT PROJECT
<i>Delta Inc., Taiwan</i> <ul style="list-style-type: none"> • Develop stream ciphers that is suited in IoT scenario • Propose and design several implementation attack countermeasures • Conduct side-channel attacks on the embedded system | Mar. 2014 - Mar. 2016 |
|  | E-HOME PROJECT
<i>National Science Council, Taiwan</i> <ul style="list-style-type: none"> • Develop AES and ECC modules that are suited for IoT use • Integrate with other submodules including computer vision, wireless, memory modules | Aug. 2011 - Jun. 2014 |

Full List of Publications

12. Tze Leung Lai, Shao-Hsuan Wang, Yi-Ching Yao, Szu-Chi Chung, Wei-Hau Chang, and I-Ping Tu, "Cryo-EM: Breakthroughs in Chemistry, Structural Biology, and Statistical Underpinnings", *Submitted*, (2020).
11. Szu-Chi Chung, Hsin-Hung Lin, Po-Yao Niu, Shih-Hsin Huang, I-Ping Tu, Wei-Hau Chang, "Pre-Pro is a Fast Pre-Processor for Single-Particle Cryo-EM by Enhancing 2D Classification", *Accepted by Nature Communications Biology*, (2020).
10. Szu-Chi Chung, Shao-Hsuan Wang, Po-Yao Niu, Su-Yun Huang, Wei-Hau Chang, I-Ping Tu, "Two-stage dimension reduction for noisy high-dimensional images and application to Cryogenic Electron Microscopy", *Accepted by Annals of Mathematical Sciences and Applications*, (2020).
9. Szu-Chi Chung, Shih-Hao Huang, Po-Yao Niu, Su-Yun Huang, Wei-Hau Chang, I-Ping Tu, "A Two-Stage Dimension Reduction Method For Cryo-EM Image Processing", *Microscopy and Microanalysis 2019 Meeting*, (2019).
8. Szu-Chi Chung, Chun-Yuan Yu, Sung-Shine Lee, Hsie-Chia Chang, Chen-Yi Lee, "An Improved DPA Countermeasure Based on UDRPG for IoT Applications", *IEEE Transactions on Circuits and Systems I (TCAS-I)*, (2017).
7. Sung-Shine Lee, Szu-Chi Chung, Chun-Yuan Yu, Hsie-Chia Chang, Chen-Yi Lee, "A New Power Analysis Attack on Stream cipher Trivium-64", *VLSI Design/CAD Symposium (VLSI-CAD)*, (2015).
6. Szu-Chi Chung, Jing-Yu Wu, Hsing-Ping Fu, Jen-Wei Lee, Hsie-Chia Chang, Chen-Yi Lee, "Efficient Hardware Architecture of η_T Pairing Accelerator Over Characteristic Three", *IEEE Transactions on Very Large Scale Integration (VLSI) System* **23**, 88–97 (2015).

5. Szu-Chi Chung, Sung-Shine Lee, Hsie-Chia Chang, Chen-Yi Lee, “Implementing Bilinear Pairing Accelerator Using Residue Number System”, *VLSI Design/CAD Symposium (VLSI-CAD)*, (2014).
4. Jen-Wei Lee, Szu-Chi Chung, Hsie-Chia Chang, Chen-Yi Lee, “Efficient Power-Analysis-Resistant Dual-Field Elliptic Curve Cryptographic Processor Using Heterogeneous Dual-Processing-Element Architecture”, *IEEE Transactions on Very Large Scale Integration (VLSI) System* **22**, 49–61 (2014).
3. Jen-Wei Lee, Szu-Chi Chung, Hsie-Chia Chang, Chen-Yi Lee, “A $3.40ms/GF(p_{521})$ and $2.77ms/GF(2^{521})$ DF-ECC Processor with Side-Channel Attack Resistance”, *International Solid-State Circuits Conference (ISSCC)*, 50–51 (2013).
2. Jen-Wei Lee, Szu-Chi Chung, Hsie-Chia Chang, Chen-Yi Lee, “An Efficient Countermeasure against Correlation Power-Analysis Attacks with Randomized Montgomery Operations for DF-ECC Processor”, *Conference on Cryptographic Hardware and Embedded Systems (CHES)*, 548–564 (2012).
1. Szu-Chi Chung, Jen-Wei Lee, Hsie-Chia Chang, Chen-Yi Lee, “High-performance elliptic curve cryptographic processor over $GF(p)$ with SPA resistance”, *IEEE International Symposium on Circuits and Systems (ISCAS)*, 1456–1459 (2012).

References

Dr. I-Ping Tu

(Current Advisor)

Institute of Statistical Science

Academia Sinica

✉ iping@stat.sinica.edu.tw

Dr. Chen-Yi Lee

(Ph.D. Advisor)

Department of Electronics Engineering

National Chiao Tung University

✉ cylee@si2lab.org

Dr. Hsie-Chia Chang

(Ph.D. Co-Advisor)

Department of Electronics Engineering

National Chiao Tung University

✉ hcchang@mail.nctu.edu.tw