

Szu Chi Chung

POSTDOCTORAL RESEARCHER

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"If you can imagine it, you can achieve it. If you can dream it, you can become it."

Interests

Currently working as a postdoctoral researcher in Institute of Statistical Science, Academia Sinica. Have received Ph.D degree from National Chiao Tung University in Sep. 2017. I am interested in the area of data analysis and data security, including but not limited to:

Field Skill Machine learning, Image and video data analysis, Side-channel analysis, Security system design, Big data infrastructure Software programming (Python, Java, C, C++), FPGA prototyping, ASIC chip design

Education _____

PHD. ELECTRICAL ENGINEERING

Sep. 2011 - Sep. 2017



National Chiao Tung University, Hsinchu, Taiwan.

- Research Group: Star group of Silicon implementation lab (SI2)
- · Advisor: Chen-Yi Lee
- Thesis topic: Stream Cipher and ID-Based Crypto Systems for IoT Applications
- GPA 4.0/4.0, 34 credits



BACHELOR OF EECS UNDERGRADUATE HONORS PROGRAM

Sep. 2007 - Jun. 2011

National Chiao Tung University, Hsinchu, Taiwan.

• GPA 4.0/4.0, 144 credits



EXCHANGE STUDENT IN EECS

Aug. 2010 - DEC. 2010

University of Illinois Urbana-Champaign, USA

• GPA 4.0/4.0, 13 credits



HIGH SCHOOL GRADUATION

Sep. 2004 - Jun. 2007

National Hualien High School, Taiwan

Honors & Awards

2019	Third Place, Poster Competition of Institute of Statistical Science	Academia Sinica
2016	Dragon Gate Program Scholarship (科技部龍門計畫), Visiting Student Researcher to Stanford	Ministry Of Science
	University	and Technology
2013	Second Prize, IE Design Contest, Core Technology Category (教育部 IE 競賽)	Ministry Of
		Education
2012	Bronze Medal Award, 12th Macronix Golden Silicon Award	Macronix Inc.
2012	First Prize, IC Design Contest, Cell-Based IC Category (教育部 IC 競賽)	Ministry Of
		Education
2010	EECS Study Aboard Scholarship , Exchange student program to University of Illinois	National Chiao
	Urban-Champaign	Tung University
2007	Second Prize, Programming Contest for Freshman	National Chiao
		Tung University

Academic and Working Experiences.



POSTDOCTORAL RESEARCHER

Dec. 2017 - PRESENT

Institute of Statistical Science, Academia Sinica, Taiwan.

• Laboratory Director: I-Ping Tu 🗹

• Research Group: Statistical Analysis for Biological Image Data 🗹



POSTDOCTORAL RESEARCHER

Oct. 2017 - Nov. 2017

National Chiao Tung University, Taiwan.

• Laboratory Director: Chen-Yi Lee

• Research Group: Star group of Silicon implementation lab (SI2)



VISITING STUDENT RESEARCHER

Nov. 2016 - Aug. 2017

Stanford University, USA.

• Project: Scalable video analysis framework

Advisor: Wing-Hung Wong Collaborator: Tung-Yu Wu



TEACHING ASSISTANT

Fall 2015

National Chiao Tung University, Taiwan.

• Course: Introduction to VLSI Design

• Lecturer: Chen-Yi Lee



TEACHING ASSISTANT

Fall 2011, Fall 2013 and Fall 2014

National Chiao Tung University, Taiwan.

Course: Integrated Circuit Design Laboratory

• Lecturer:Chen-Yi Lee ☑ and Shyh-Jye Jou ☑



TEACHING ASSISTANT

Fall 2014

National Chiao Tung University, Taiwan.

Course: Digital Circuit and System

• Lecturer: Chen-Yi Lee ☑



TEACHING ASSISTANT

2010-2014

National Chiao Tung University, Taiwan.

Course: Electronics Laboratory (I) and (II)

• Lecturer: Meng-Wei Wang ☑



TEACHING ASSISTANT

2012

National Chiao Tung University, Taiwan.

• Course: Digital Circuit Laboratory

Lecturer: Chien Chen ☑

Invited Talks

- 2. 2018/12/11, "A Dimension Reduction Method For Cryo-EM Image Processing ", 2018 Workshop On High Dimensional Statistical Analysis, (2018).
- 1. 2018/3/14, "Scalable Video Analysis Framework ", Institute of Statistical Science, Academia Sinica, (2018).

Dessertion

1. Szu-Chi Chung, "Stream Cipher and ID-Based Crypto Systems for IoT Applications ☑", PHD Dessertion , (2016).

Academic Services

2016-2017 **Reviewer**, IEEE Transactions on Circuits and Systems I (TCAS-I)

2016-2017 **Reviewer**, IEEE Transactions on Very Large Scale Integration Systems (TVLSI)

2016 **Reviewer**, IEEE Transactions on Computers

Research Projects



CRYO-EM IMAGE PROCESSING

Dec. 2017 - PRESENT

- Academia Sinica, Taiwan
- Develop dimension reduction and clustering methods for cryo-EM
- Develop platform for integrating cryo-EM packages



SCALABLE VIDEO ANALYSIS FRAMEWORK

Nov. 2016 - Sep. 2017

Stanford, USA

- Bridging the gap between spark analytic framework and traditional computer vision modules
- Provides a solution to deal with distributed video/image analysis in big data framework



BIG DATA SECURITY PROJECT

Sep. 2014 - Sep. 2017

Ministry of Science and Technology, Taiwan

- Develop several high throughput Bilinear Pairing modules to support cloud security protocols
- Propose guidelines to design security modules for big data system

DELTA-NCTU IOT PROJECT

Mar. 2014 - Mar. 2016



Delta Inc., Taiwan

- Develop stream ciphers that is suited in IoT scenario
- Propose and design several implementation attack countermeasures
- · Conduct side-channel attacks on the embedded system



E-HOME PROJECT

Aug. 2011 - Jun. 2014

National Science Council, Taiwan

- Develop AES and ECC modules that are suited for IoT use
- Integrate with other submodules including computer vision, wireless, memory modules

Full List of Publications

- 9. <u>Szu-Chi Chung</u>, Shih-Hao Huang, Po-Yao Niu, Su-Yun Huang, Wei-Hau Chang, I-Ping Tu, "A Two-Stage Dimension Reduction Method For Cryo-EM Image Processing ?", *In preparation*, (2019).
- 8. Szu-Chi Chung, Chun-Yuan Yu, Sung-Shine Lee, Hsie-Chia Chang, Chen-Yi Lee, "An Improved DPA Countermeasure Based on UDRPG for IoT Applications ", IEEE Transactions on Circuits and Systems I (TCAS-I), (2017).
- 7. Sung-Shine Lee, <u>Szu-Chi Chung</u>, Chun-Yuan Yu, Hsie-Chia Chang, Chen-Yi Lee, "A New Power Analysis Attack on Stream cipher Trivium-64 ", *VLSI Design/CAD Symposium (VLSI-CAD)*, (2015).
- 6. Szu-Chi Chung, Jing-Yu Wu, Hsing-Ping Fu, Jen-Wei Lee, Hsie-Chia Chang, Chen-Yi Lee, "Efficient Hardware Architecture of η_T Pairing Accelerator Over Characteristic Three $\overline{\mathcal{L}}$ ", IEEE Transactions on Very Large Scale Integration (VLSI) System 23, 88–97 (2015).
- 5. <u>Szu-Chi Chung</u>, Sung-Shine Lee, Hsie-Chia Chang, Chen-Yi Lee, "Implementing Bilinear Pairing Accelerator Using Residue Number System ", VLSI Design/CAD Symposium (VLSI-CAD), (2014).
- 4. Jen-Wei Lee, Szu-Chi Chung, Hsie-Chia Chang, Chen-Yi Lee, "Efficient Power-Analysis-Resistant Dual-Field Elliptic Curve Cryptographic Processor Using Heterogeneous Dual-Processing-Element Architecture 7", IEEE Transactions on Very Large Scale Integration (VLSI) System 22, 49–61 (2014).
- 3. Jen-Wei Lee, Szu-Chi Chung, Hsie-Chia Chang, Chen-Yi Lee, "A $3.40ms/GF(p_{521})$ and $2.77ms/GF(2^{521})$ DF-ECC Processor with Side-Channel Attack Resistance $\ref{2}$ ", International Solid-State Circuits Conference (ISSCC) , 50–51 (2013).
- 2. Jen-Wei Lee, Szu-Chi Chung, Hsie-Chia Chang, Chen-Yi Lee, "An Efficient Countermea- sure against Correlation Power-Analysis Attacks with Randomized Montgomery Operations for DF-ECC Processor ", Conference on Cryptographic Hardware and Embedded Systems (CHES), 548–564 (2012).
- 1. Szu-Chi Chung, Jen-Wei Lee, Hsie-Chia Chang, Chen-Yi Lee, "High-performance elliptic curve cryptographic processor over GF(p) with SPA resistance $\ref{eq:space}$ ", IEEE International Symposium on Circuits and Systems (ISCAS) , 1456–1459 (2012).

References

Dr. I-Ping Tu

(Current Advisor) Institute of Statistical Science Academia Sinica

iping@stat.sinica.edu.tw

Dr. Hsie-Chia Chang ☑

(Ph.D. Co-Advisor) Department of Electronics Engineering National Chiao Tung University

hcchang@mail.nctu.edu.tw

Dr. Chen-Yi Lee ☑

(Ph.D. Advisor)

Department of Electronics Engineering National Chiao Tung University