Programs After Market Services (PAMS)

Technical Documentation

SERVICE MANUAL

[NMP Part No.0275406]

RAE–2
CELLULAR PHONE/ PERSONAL DIGITAL ASSISTANT

NOKIA

RAE–2 ORIGINAL 02/99

AMENDMENT RECORD SHEET

Amendment Number	Date	Inserted By	Comments
	02/99		Original

RAE–2 SERVICE MANUAL
OVERALL CONTENTS

IMPORTANT

This document is intended for use by qualified service personnel only.

Company Policy

Our policy is of continuous development; details of all technical modifications will be included with service bulletins.

While every endeavour has been made to ensure the accuracy of this document, some errors may exist. If any errors are found by the reader, NOKIA MOBILE PHONES Ltd should be notified in writing.

Please state:

Title of the Document + Issue Number/Date of publication

Latest Amendment Number (if applicable)

Page(s) and/or Figure(s) in error

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PAMS Technical Documentation
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Finland

Warnings and Cautions

Please refer to the phone's user guide for instructions relating to operation, care and maintenance including important safety information. Note also the following:

Warnings:

CARE MUST BE TAKEN ON INSTALLATION IN VEHICLES FITTED WITH ELECTRONIC ENGINE MANAGEMENT SYSTEMS AND ANTI–SKID BRAKING SYSTEMS. UNDER CERTAIN FAULT CONDITIONS, EMITTED RF ENERGY CAN AFFECT THEIR OPERATION. IF NECESSARY, CONSULT THE VEHICLE DEALER/MANUFACTURER TO DETERMINE THE IMMUNITY OF VEHICLE ELECTRONIC SYSTEMS TO RF ENERGY

THE HANDPORTABLE TELEPHONE MUST NOT BE OPERATED IN AREAS LIKELY TO CONTAIN POTENTIALLY EXPLOSIVE ATMOSPHERES EG PETROL STATIONS (SERVICE STATIONS), BLASTING AREAS ETC.

OPERATION OF ANY RADIO TRANSMITTING EQUIPMENT, INCLUDING CELLULAR TELEPHONES, MAY INTERFERE WITH THE FUNCTIONALITY OF INADEQUATELY PROTECTED MEDICAL DEVICES. CONSULT A PHYSICIAN OR THE MANUFACTURER OF THE MEDICAL DEVICE IF YOU HAVE ANY QUESTIONS. OTHER ELECTRONIC EQUIPMENT MAY ALSO BE SUBJECT TO INTERFERENCE.

CLASS 1 LASER PRODUCT. See IEC60825–1 specification: 825–1;
5: Labelling, 5.1: General, 5.2: Class 1

Cautions:

1. Servicing and alignment must be undertaken by qualified personnel only.
2. Ensure all work is carried out at an anti–static workstation and that an anti–static wrist strap is worn.
3. Ensure solder, wire, or foreign matter does not enter the telephone as damage may result.
4. Use only approved components as specified in the parts list.
5 Ensure all components, modules screws and insulators are correctly re–fitted after servicing and alignment. Ensure all cables and wires are repositioned correctly.
6 All PC's used with NMP Service Software for this produce must be bios and operating system ”Year 2000 Compliant”

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Chapter 1

GENERAL INFORMATION

AMENDMENT RECORD SHEET

Amendment Number	Date	Inserted By	Comments
	01/99		Original

CHAPTER 1 – GENERAL INFORMATION

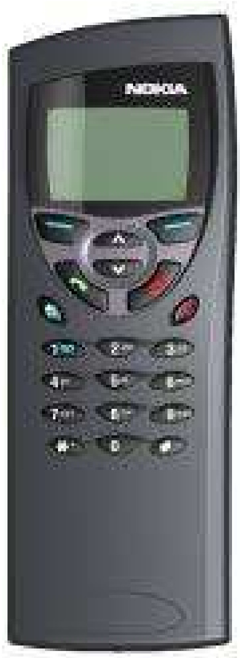
Contents

Introduction

RAE–2N is the 2nd generation communicator for GSM 900 network. Communicator extends the basic digital cellular phone with in–built data capabilities and applications.

RAE –2 is a phase 2, class4 transceiver with 2W peak TX power.

The device has two user interfaces. The conventional phone interface on the front cover. By opening the device the user can access the graphical user interface which can utilize the full communicator functionality.



Technical Summary

The Communicator is divided into two main domains: phone and personal digital assistant (PDA). Phone manages speech and data connections to GSM network. It also handles audio input and output. PDA runs all the applications (e.g. calendar, contact database etc...) and utilizes the data connections made by the phone.

The phone is based on DCT3 technology and CUI style user interface software. PDA uses AMD’s 486 CPU and GEOS operating system.

Battery technology is Li–ion.

The product has earpiece for conventional phone use but it also has an internal handsfree speaker.

Connection to the other devices can be handled with 115kbps serial cable or 115kbps IR. Product is IrDA compatible.

The phone display is graphical, transflective FSTN LCD display. Display resolution is 84x48 pixels. The PDA display is graphical, transflective FSTN LCD display. Display resolution is 640x200 pixels and dot pitch is 0.17mm. Contrast is good enough to show 16 gray scales.

Both LCD displays are backlit with EL–panel.

In addition to the fixed memory the product can use memory extension module, MMC, to expand the user file system area. The MMC supports hot insertion.

NOTE: Due to the infrared data link the RAE–2 is officially specificed as :

CLASS 1 LASER PRODUCT.
See IEC 60825–1 specification 825–1; Labelling, 5.1 General 5.2 Class 1.

Product Selection

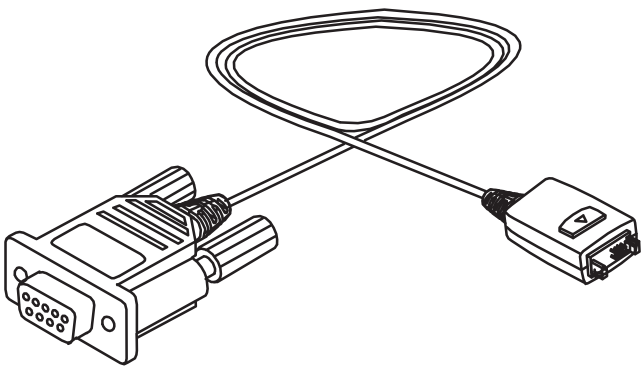
The product has only one design, however each user interface language version has its own product code. Some countries have e.g. English communicator but manuals in the local language.

Name of Sales Package	Sales Package Code	Notes
Nokia RAE–2NA	0069108	English
Nokia RAE–2NC	0069109	French
Nokia RAE–2NB	0069110	German
Nokia RAE–2NA Benelux	0069111	Benelux
Nokia RAE–2NS	0069112	Swedish
Nokia RAE–2NN	0069113	Norwegian
Nokia RAE–2NP	0069114	Danish
Nokia RAE–2NM	0069115	Finnish
Nokia RAE–2NR	0069116	Italian
Nokia RAE–2NA S/AFRICA	0069126	South Africa
Nokia RAE–2NA Poland	0069127	Polish
Nokia RAE–2NA Baltic	0069128	Estonian, Latvian, Lithuanian
Nokia RAE–2NF	0069129	Spanish
Nokia RAE–2NG	0069130	Portuguese
Nokia RAE–2NA EURO1	0069131	Hungarian, Turkish, Czech, Romanian
Nokia RAE–2NA EURO2	0069132	Greek, Romanian, Slovenian
Nokia RAE–2NA Russian	0069133	Russian

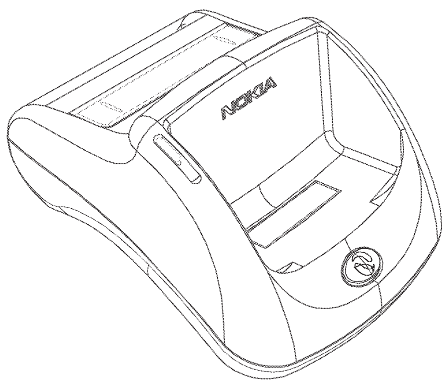
Units and Accessories

Name of unit or accessory	Type code	Material code	Notes
Battery	BLN–3	0670226	1140 mAh, Li–Ion
Performance Travel Charger	ACP–9E	0675149	Fore EURO version
Mobile Charger	LCH–9	0271056	
Advanced Desktop Stand	DCH–7	0271365	
RS–232 Adapter Cable	DLR–2	0730132	
Headset	HDC–8	0271368	
Advanced HF Car Kit	CARK–99	0085155	
Privacy Handset	HSU–1	0270830	
Upgrade HF Car Kit	CARK–102		
Memory Card	DTS–4	0271393	Removable memory card MMC
Carrying Case	CBR–4	0271410	

Accessories for PC connection



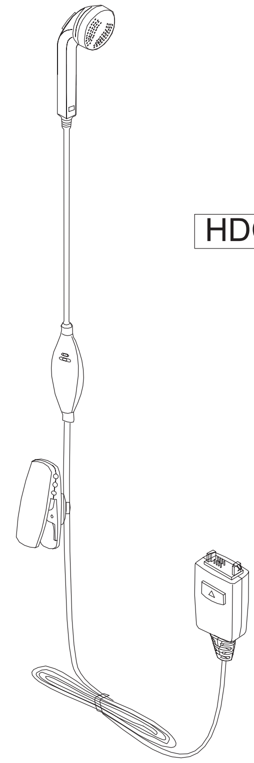
DLR–2



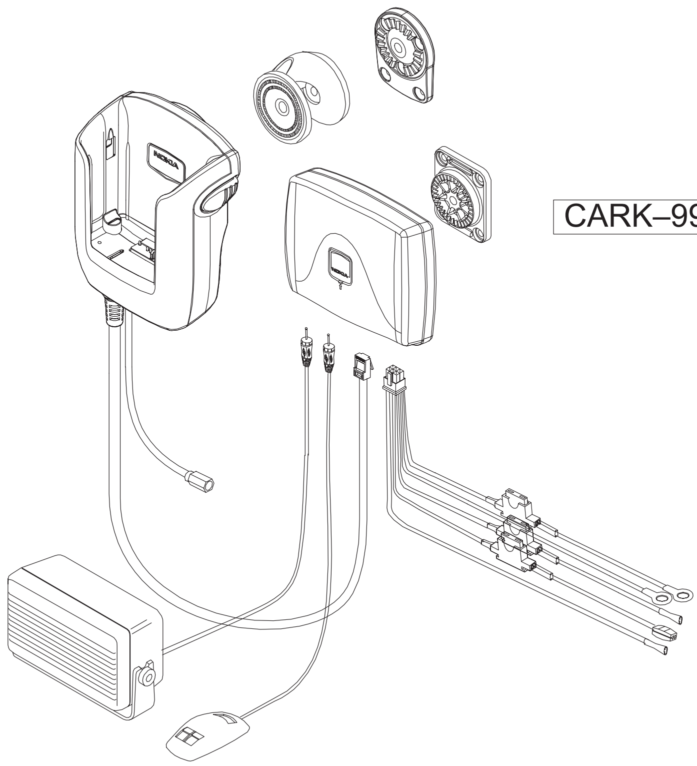
DCH–7

The desktop stand can charge the transceiver and one BLN–3 battery simultaneously. It also provides connectivity to personal computer. The button in the front of the deskstand starts synchronization operation if the deskstand is connected to PC with serial cable (DLR–2) and the connectivity software in PC is activated.

Audio Accessories



HDC–8



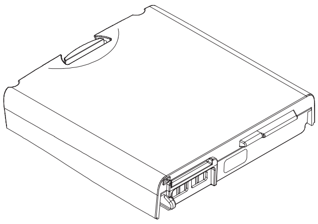
CARK–99

Headset differs from DCT3 headset, having a different connector.

The Car kit has a product specific cradle. It is possible to connect DLR–2 PC–connectivity cable to cradle. Privacy handset (HSU–1) is the same as used with DCT3 products .

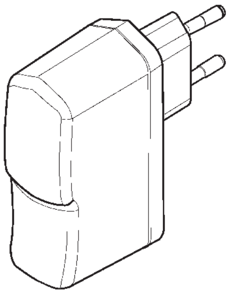
Battery and Chargers

Battery



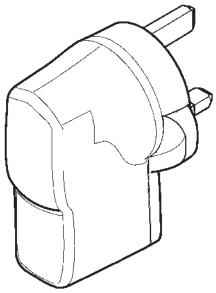
BLN–3

European charger



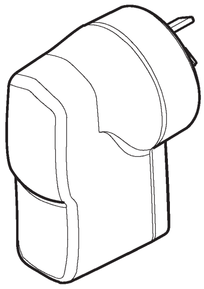
ACP–9E

UK charger



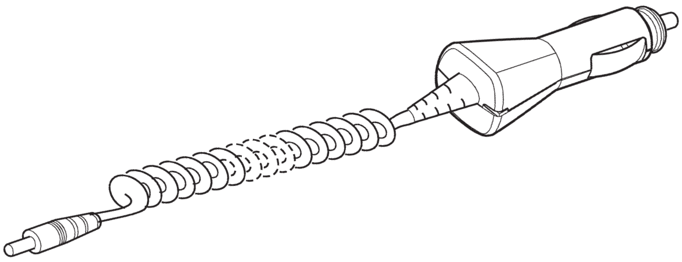
ACP–9X

Australian charger



ACP–9A

Travel charger



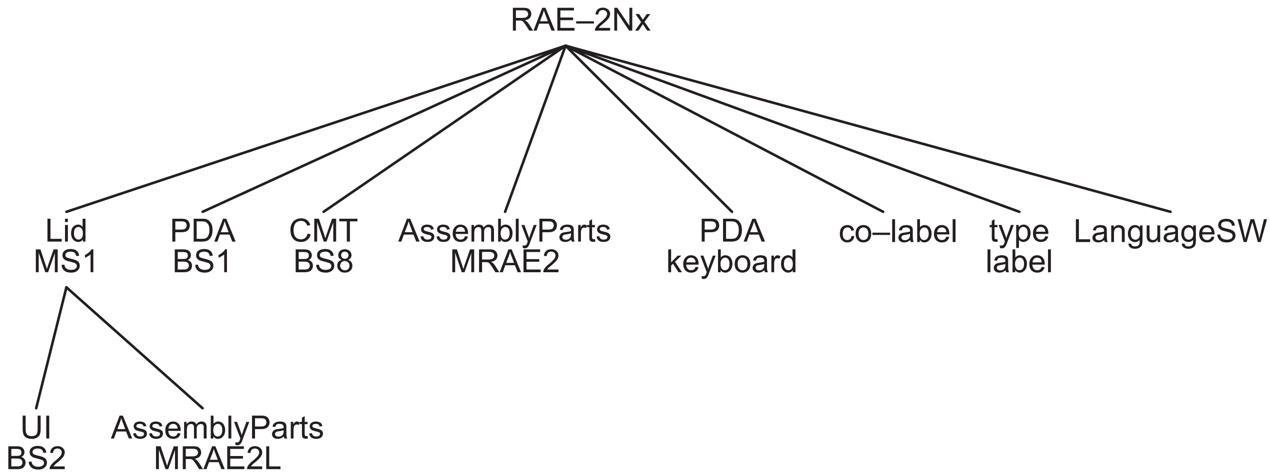
LCH–9

Other Accessories

The Memory card DTS–4 provides additional 4MB of user memory into the product. Memory cards complies to the open MMC specification. In the future there will be also larger memory capacities available.

Structure

RAE–2Nx consists of three electrical sub–modules and several mechanical parts. The structure is basically the same for all the language versions. The only parts that are unique to each language version are located on the first hierarchy level of the product structure; namely PDA keyboard, Language software and type label. All other parts and modules are language independent.



List of Modules

Name of module	Type code	Material code	Notes
MS1		0201224	Lid sub–assembly, contains UI
BS1	BS1	0201096	PDA module, includes CPU and memories
BS8	BS8	0201095	GSM phone module
MRAE2		0261780	Mechanical assembly parts , no language dependent parts
BS2	BS2	0201097	UI module, includes both LCD's
MRAE2L		0261786	Assembly parts for lid sub–assembly

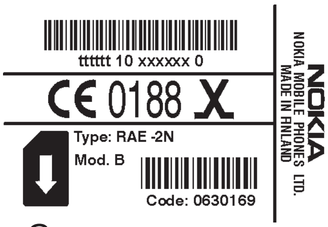
Basic Specifications

Dimensions	56x159x25 mm
Weight	200g (excluding battery)
Battery	BLN–3, Li–Ion, 1030mAh, 3.6V, 49,1g
Standby time	5–7 days
Talk time	3–7h
Transceiver	GSM, class 4
PDA cpu	AMD 486, 33MHz
Fixed user memory	2Mbytes
Fixed application memory	4Mbytes
RAM memory (PDA)	2Mbytes

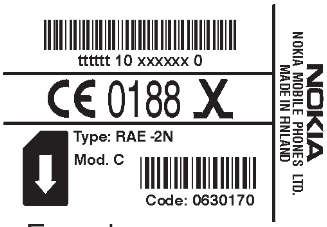
Type Labels

Each transceiver with unique mechanics or software has its own type label.

UK English

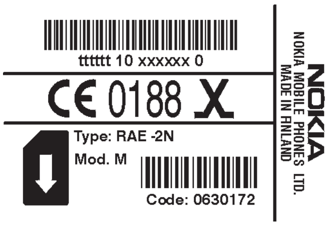


German

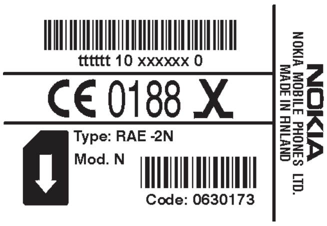


French

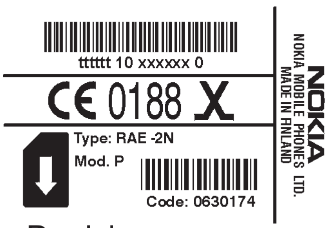
Scandinavian



Finnish

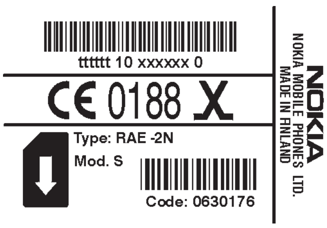


Norwegian



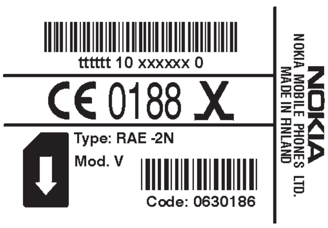
Danish

Italian

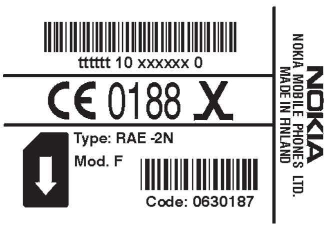


Swedish

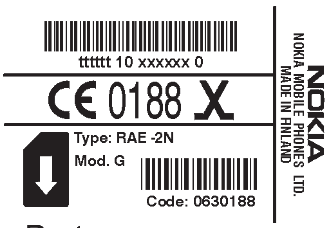
APAC1



APAC2



Spanish



Portuguese

APAC1 and APAC2 are products with UK English user interface with software settings meant for APAC. Scandinavian product has Scandinavian keyboard but UK English user interface.

Keymat Variants

The keymat used depends in the language environment.

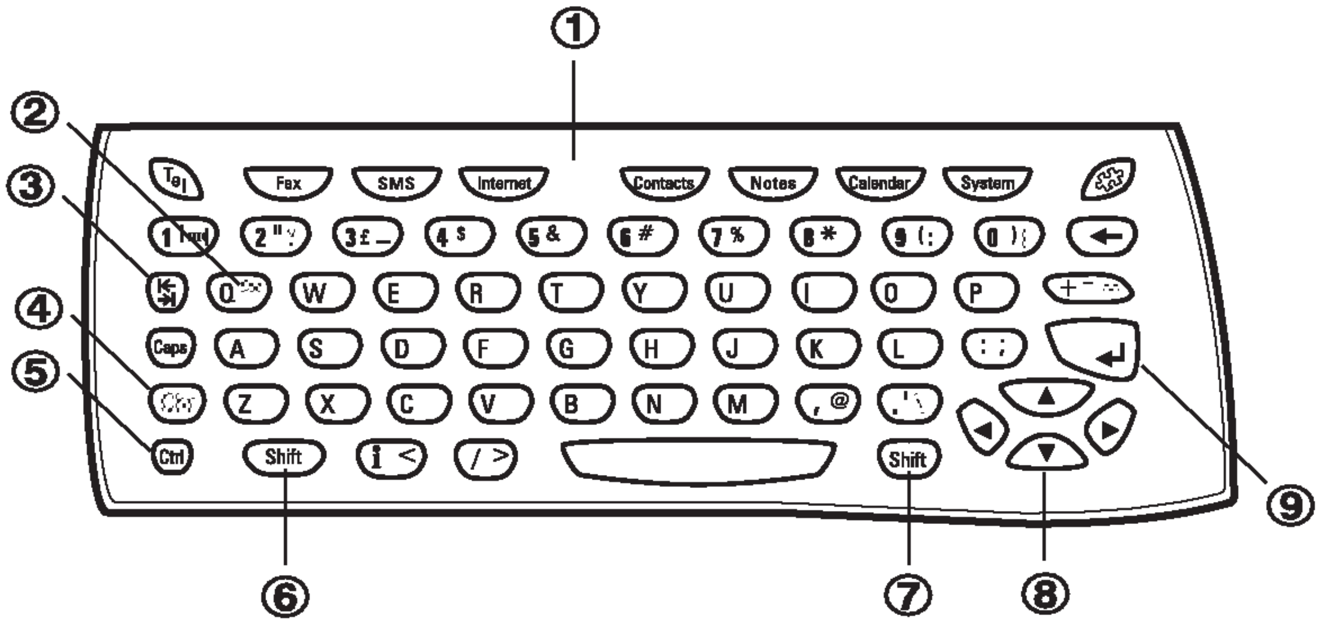


Figure 1. English keymat

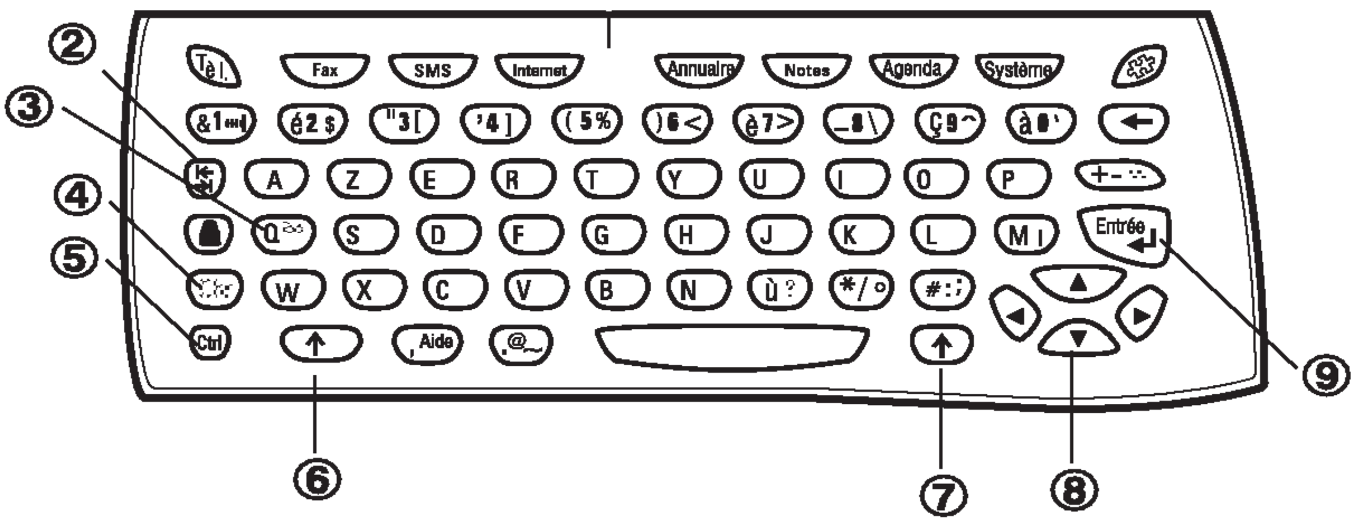


Figure 2. French keymat

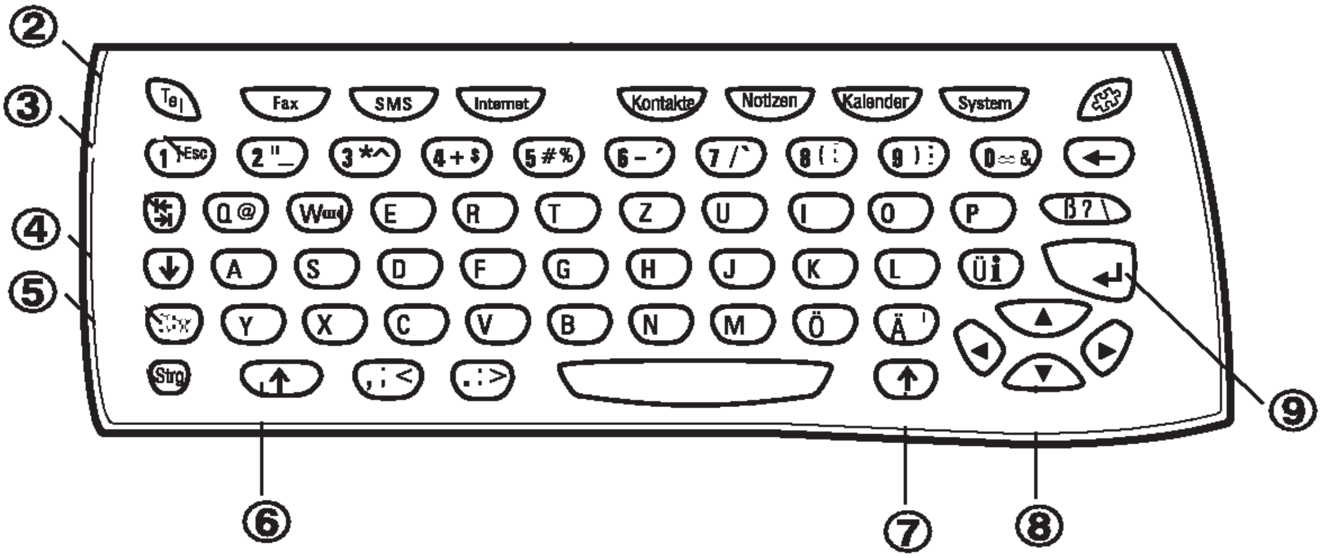


Figure 3. German keymat

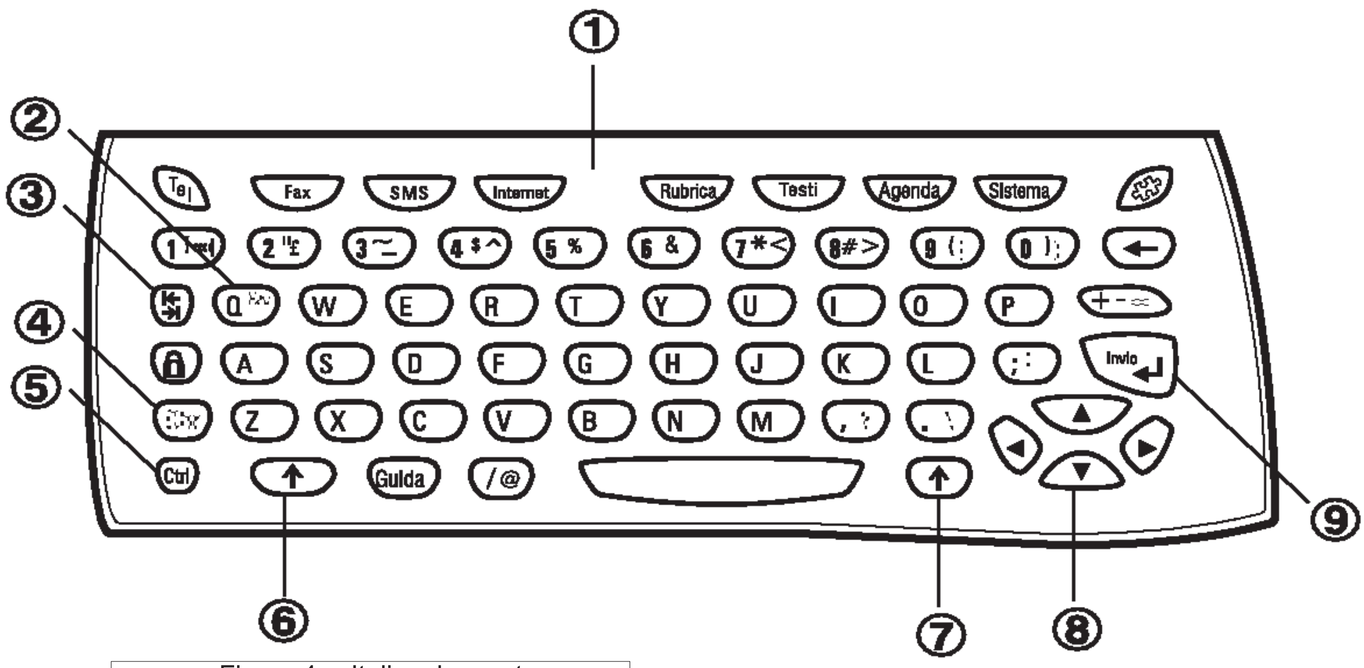


Figure 4. Italian keymat

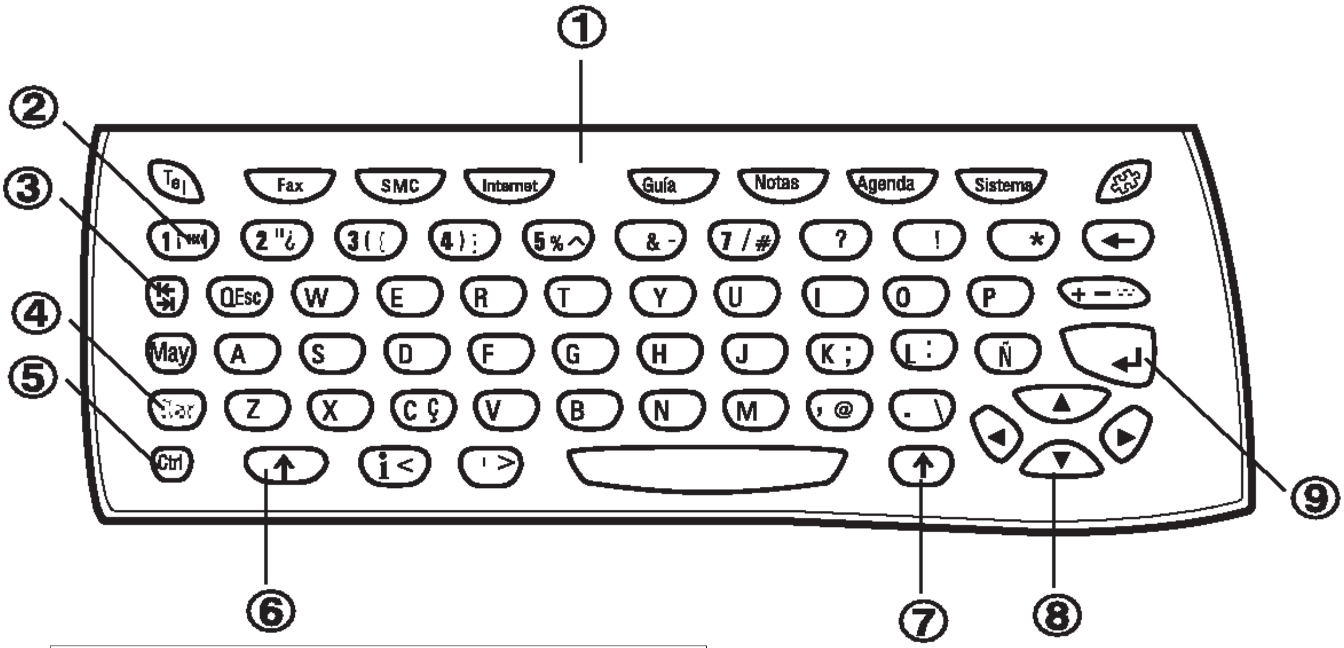


Figure 5. Spanish keymat

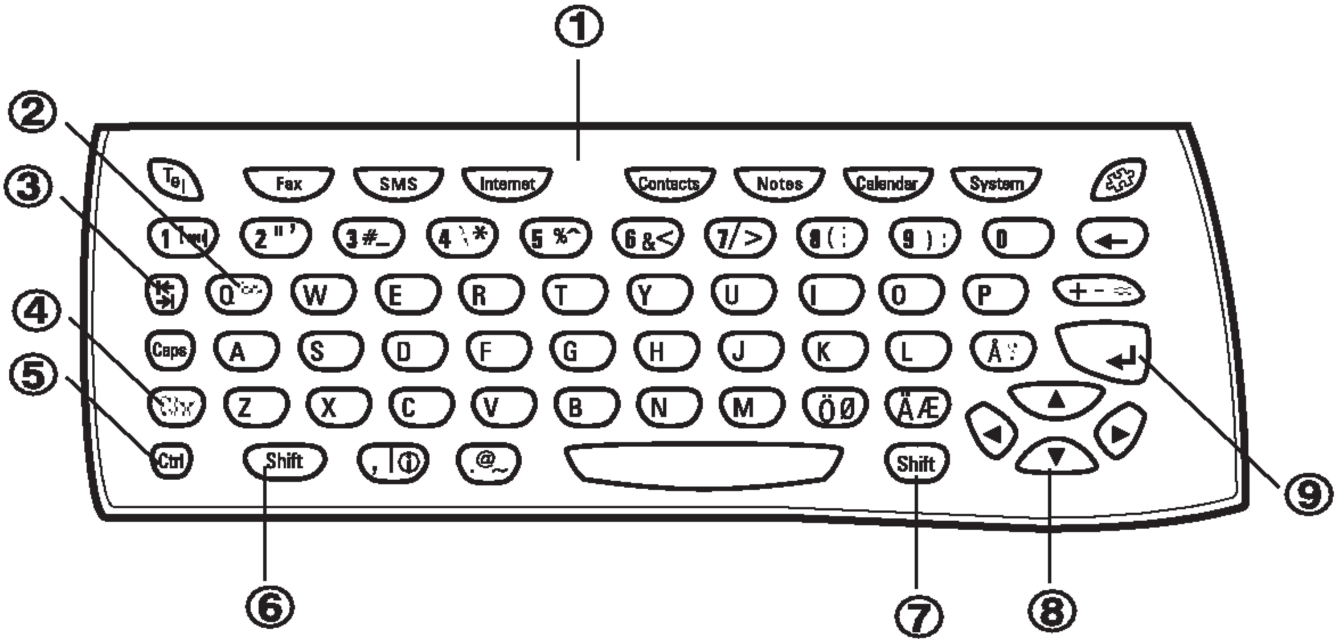


Figure 6. Scandinavian keymat

Technical Specifications

Modes of Operation

The Communicator has several different operating modes depending on the activity of CMT and PDA modules. CMT unit can be switched off, idle or call. PDA can be active, standby, suspended or reset. If the battery voltage is too low PDA is held in reset–mode.

Electrical Specifications

DC Characteristics

DC–supply for the product is BLN–3 Li–Ion battery. Nominal voltage is 3.6V, Capacity is 1030mAh i.e. 3708 mWh.

Nominal system voltage for both PDA and CMT is 2.8V.

Average Current Consumption

	CMT mode		
PDA mode	**Off**	**Idle**	**Call**
Active	90	100	240
Standby	60.5	63	185
Suspended	3.2	5.5	165

Backlight power consumption is 60mA. Handsfree consumes about 80mA.

AC Characteristics

Product contains two EL–panels for CMT and PDA display backlighting.

EL Characteristics, PDA and CMT

Parameter	Minimum	Typical / Nominal	Maximum	Unit
Frequency	60	70	180	Hz
Peak–to–peak voltage	170	175	180	V
RMS voltage	70	72	75	V

Main RF Characteristics

Item	Values
Receive frequency range	935 ... 960 MHz
Transmit frequency range	890 ... 915 MHz
Duplex spacing	45 MHz
Channel spacing	200 kHz
Number of RF channels	124
Power class	4
Number of power levels	15

Transmitter characteristics

Item	Values
Type	Upconversion, nonlinear, FDMA/TDMA
Intermediate frequency (phase modulated)	116 MHz
LO frequency range	1006 ... 1031 MHz
Output power	2 W peak (33 dBm)
Power control range	min. 5 ... 30 dBm
Maximum phase error (RMS/peak)	max 5 deg./20 deg. peak

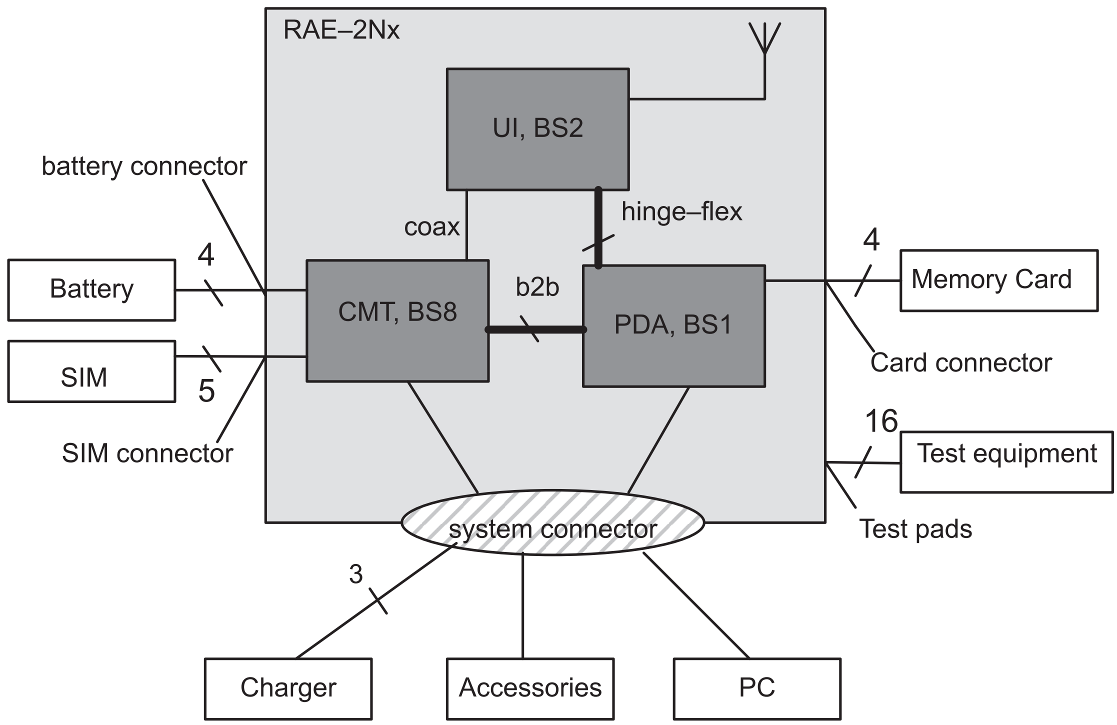
Receiver characteristics

Item	Values
Type	Linear, FDMA/TDMA
IF frequencies	1st 71 MHz, 2nd 13 MHz
LO frequencies	1st LO 1006 ... 1031 MHz, 2nd LO 58 MHz
Typical 1 dB bandwidth	+/– 90 kHz
Sensitivity	min. – 102 dBm , S/N >8 dB
Total typical receiver voltage gain (from antenna to RX ADC)	73 dB
Receiver output level (RF level –95 dBm)	50 mVpp (typical balanced signal level of 13 MHz IF in RF BB interface = input level to RX ADCs)
Typical AGC range	–17 ... +40 dB
Accurate AGC control range	57 dB
Typical AGC step in LNA	–15 dB
Usable input dynamic range	–102 ... –10 dBm
RSSI dynamic range	–110 ... –46 dBm
AGC relative accuracy on channel (accurate range)	+/– 0.8 dB
Compensated gain variation in receiving band	+/– 1.0 dB

Audio characteristics

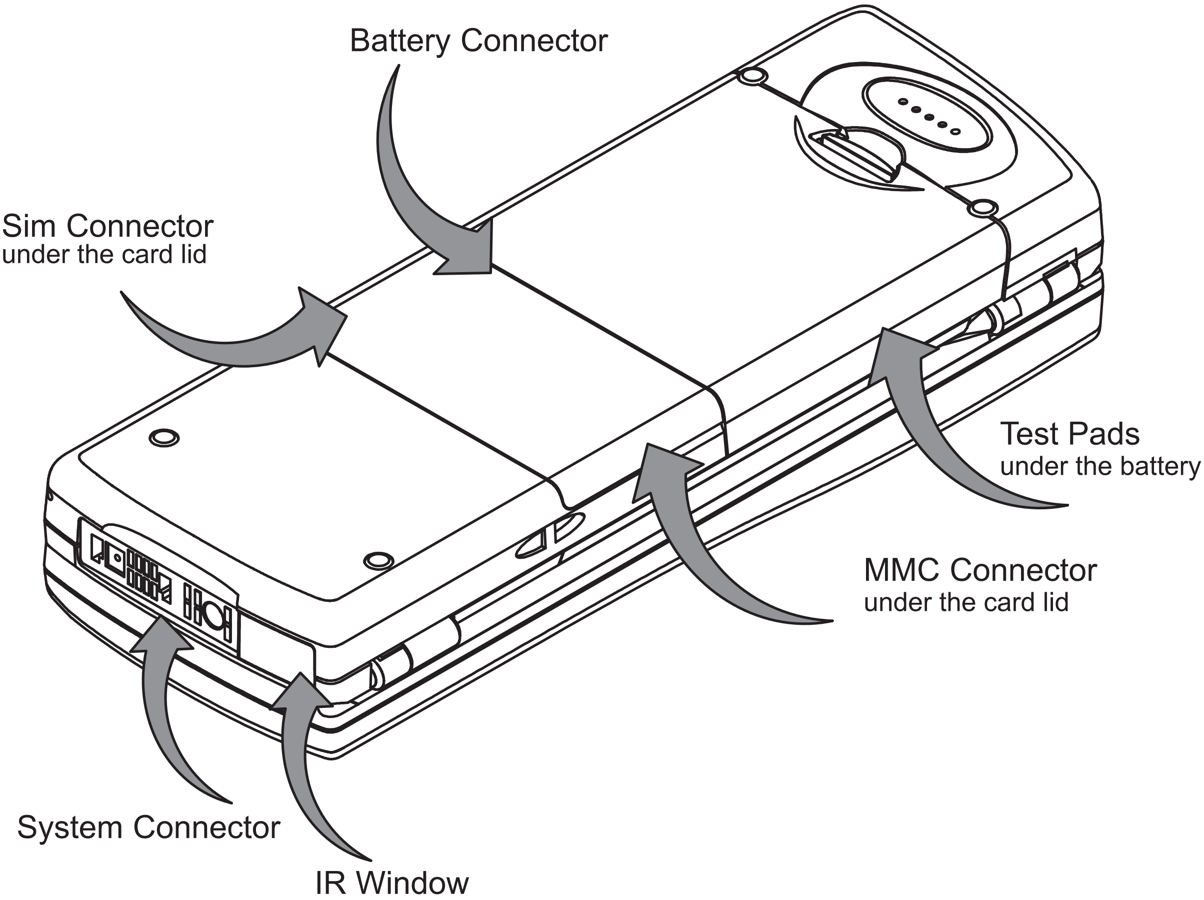
	Minimum	Typical / Nominal	Maximum	Unit / Notes
Output freq. range (earpiece)	300		3400	Hz
Output freq. range (HF speak-er)	300		3400	Hz
Mic. input range.	300		3400	Hz
ringing tone SPL			105	dB at 5 cm
HF speaker SPL		65		dB at 50 cm
Sampling rate		8		kHz
Dynamic range (input)		13		bits
Dynamic range (output)		13		bits

Interconnection Diagram



External connections and signals

External Connections:



List of external connectors

Connector Name	Code	Notes	Specifications / Ratings
Battery connector	5469087		
System connector	5469091	includes also DC and RF	
Memory card connector	5469085	removable memory card	
SIM connector	5409089		
Test pads		PCB test pads for production and after sales	

SIM and MMC cards cannot be removed until the BLN–3 battery has been removed.

Battery Connector

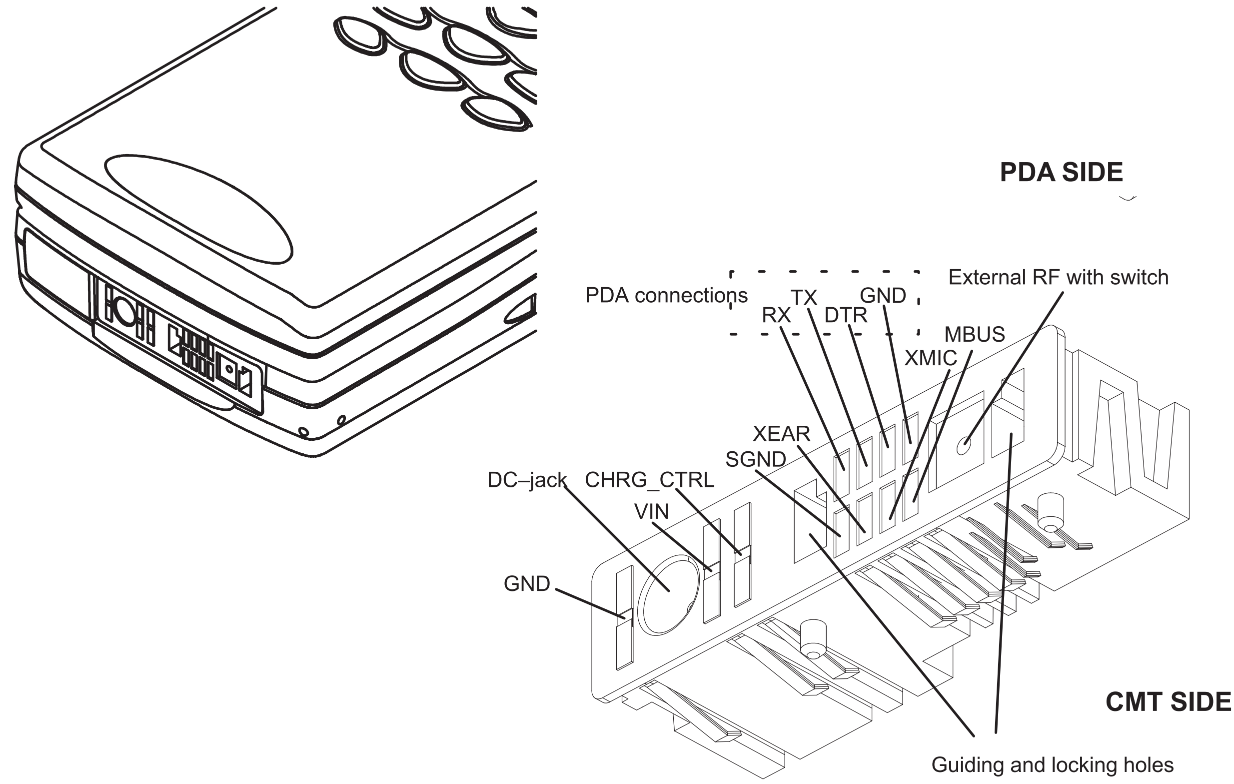
The Battery connector connects BLN–3 battery to the transceiver. The connector indicates the removal of battery about 5ms before the loss of power because pins BSI and BTEMP are shorter than BVOLT and BGND.

Pin	Name	Min	Typ	Max	Unit	Notes
1	VBATT	3.0	3.6	4.1	V	Battery voltage
2	BSI	0		2.85	V	Battery size indication Phone has 180kohm pull up resistor. SIM Card removal detection (Threshold is 2.4V@VBB=2.8V)
		21.8	22	22.2	kohm	BBS–5 Service battery (No cells)
		31.35	33	34.65	kohm	BLN–3 Li–Ion battery (4.1V)
		5			ms	The minimum time from BSI contact disengaged its battery contact to VBATT/GND disengaged its battery contacts when battery is removed.
3	BTEMP	0		1.4	V	Battery temperature indication Phone has a 100k (+–5%) pull–up resistor, Battery package has a NTC pull–down resistor: 47k+–5%@+25C , B=4050+–3%
4	GND	0		0	V	Battery ground

System Connector

The System connector combines the charger, external RF and system functions. External signals can connect to e.g. car kit, headset and PC.

The system connector is not physically compatible with DCT3 connectors except charger.

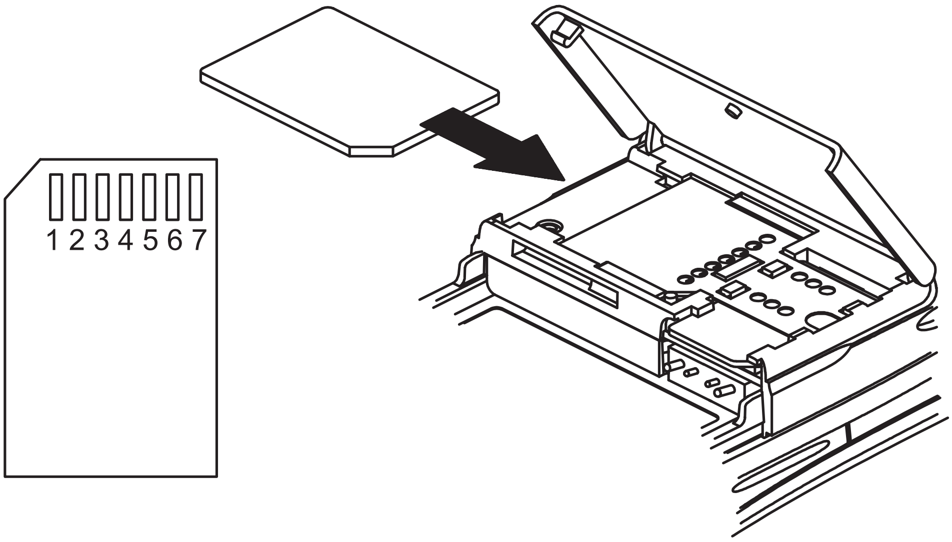


Contact	Line Symbol	CMT Function
1	L_GND	Charger ground
DC–jack side contact (DC–plug ring)	L_GND	Charger ground
DC–jack center pin	VIN	Charger input voltage
DC–jack side contact (DC–plug jacket)	CHRG_CTRL	Charger control output (from CMT)
2	VIN	Charger input voltage
3	CHRG_CTRL	Charger control output (from CMT)

Contact	Line Symbol	CMT Function
4	SGND	Accessory signal ground
5	XEAR	Accessory earphone signal output (from CMT)
6	XMIC	Accessory microphone signal input (to CMT)
7	MBUS	MBUS, bidirectional serial data I/O (DCD in PC use)
8	DCE_RX	serial_RX data. (input)
9	DCE_TX	serial_TX data. (output)
10	DTR	Data Terminal Ready (DTR). No CMT use
11	GND	Ground from BS1 module
12,15	GND	GND contacts for RF ground
13	RF_OUT	RF signal from RF switch to internal antenna
14	RF_IN	RF signal from Duplexer to RF switch

MMC Connector

The MMC connector connects a MMC card to the product. Connector has a small switch that can detect the opening of the card lid.



Pin	I/O	Name	Function	Min	Typ	Max	Unit	Description / Note
1		**RSV**	Reserved					Reserved for future use
2	I/O	**MMC_CMD**	MMC Command / Address / Response, Bidirectional	0	0	0.45	VDC	Low, Data to the card
				2.3	2.8	2.85	VDC	High, Data to the card, pulled up with 10kohm resistor to MMC_VSYS in CMT module
						0.34	VDC	Low, Data from the card
				2.1			VDC	High, Data from the card, pulled up with 10kohm resistor to MMC_VSYS in CMT module
					259.3		kHz	Frequency
3		**MMC_GND**	MMC ground				VDC	
4	I	**MMC_VSYS**	MMC Power Supply	2.75		2.85	VDC	
5	I	**MMC_CLK**	MMC Clock	0	0	0.45	VDC	Low
				2.3	2.8	2.85	VDC	High
				0.2592		8.294	MHz	Frequency
6		**MMC_GND**	MMC Ground					Ground line reserved for MMC use

Pin	I/O	Name	Function	Min	Typ	Max	Unit	Description / Note
7	**I/O**	**MMC_DATA**	MMC Bidirectional Data	0	0	0.45	VDC	Low, Data to the card
				2.3	2.8	2.85	VDC	High, Data to the card, pulled up with 10kohm resistor to MMC_VSYS in CMT module
				0	0	0.34	VDC	Low, Data from the card
				2.1			VDC	High, Data from the card, pulled up with 10kohm resistor to MMC_VSYS in CMT module
					8.294		MHz	Frequency

Mechanical Characteristics

Visible product material is ABS+PC except the lens which is clear PMMA. The bottom part of the device has a magnesium chassis.

Unit	Dimensions (mm) (W x H x D)	Weight (g)
Transceiver, RAE–2Nx	56x159x25	202.6
Battery, BLN–3	56x58x12	49.1

User Interface specifications

The product has tho separate user interfaces (UI): CMT UI on the front cover and PDA UI which can be accessed by opening the device.

CMT UI conforms to Jack–style defined by NMP. The detailed feature list and UI specifications can be found in PCMS.

User Interface Features

The RAE–2 has two separate user interfaces (UI): CMT UI on the front cover and PDA UI which can be accessed by opening the device.

Highlights of the CMT interface are:

PDA UI is based on the previous Nokia Communicator product, N9000. The main difference is that leftmost scroll buttons are replaced by Menu, Zoom and Backlight buttons.

Menu–button activates an additional pop–up menu window. The contents of the window depend on the current application. They can be e.g. settings for the telephone application.

Zoom–button toggles the font size of certain views. The zoomable view depends on the current application. The device has three different zoom levels.

Backlight–button activates the backlight for a pre–set period or until the button is pressed again. Backlight makes it possible to use the product in low light conditions.

Temperature and Environmental Conditions

Allowed ambient temperature ranges are listed below:

	Ambient temperature (degrees Celcius)	Notes
Operating range	–10 . . . +55	GSM phase2 requirements fulfilled.
Extended operating range	–20 . . . +70	Device works but not necessarily fullfill all GSM requirements.
Storage	–30 . . . +70	execept battery
Long time storage (sales package)	0 . . . +30	

Allowed ambient relative humidity :

	Ambient relative humidity	Notes
	5 . . . 95 %	except battery

The transceiver is not protected against ingress of water. The transceiver may be instantaneously subjected to dripped or condensed water. Longer term contact with water will cause permanent damage.

Warnings and Restrictions

See the User Manual.

Functional Description

The Communicator comprises two functionally independent units: PDA and CMT.

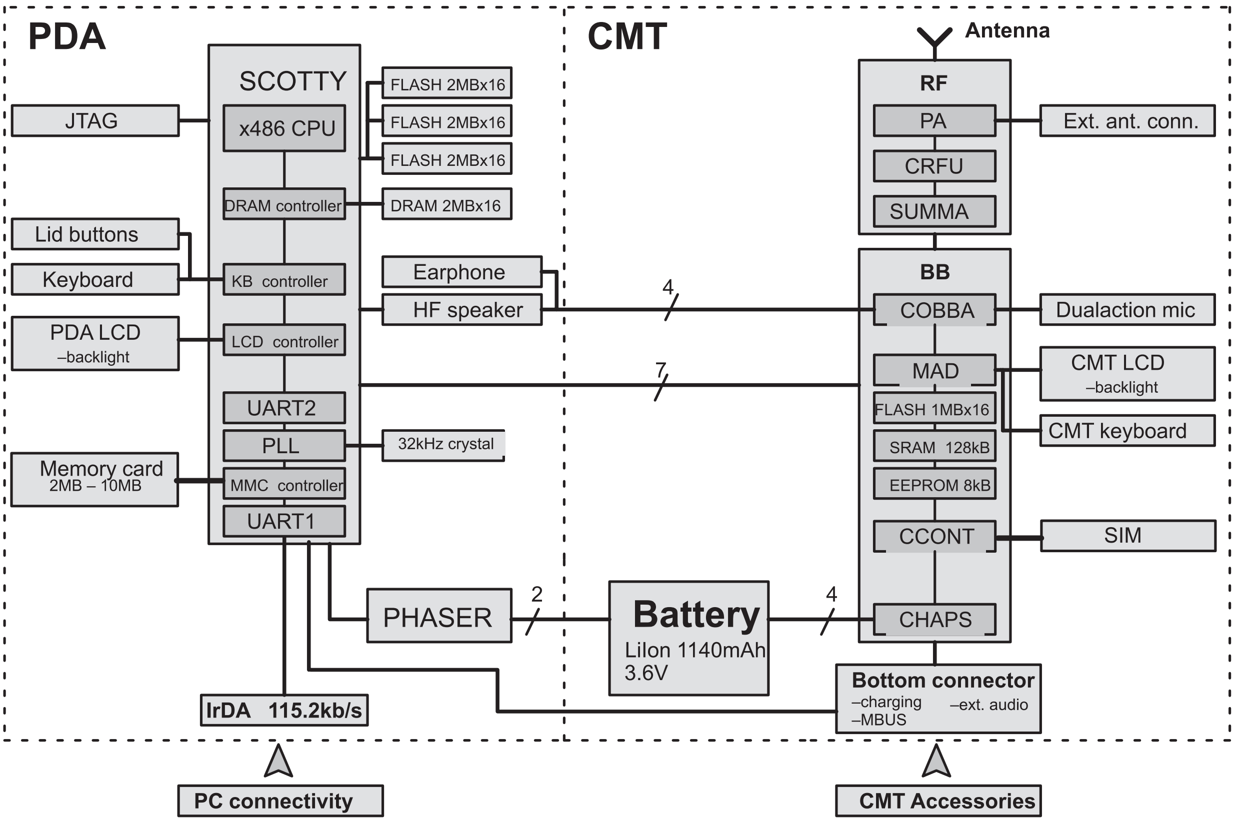
The PDA implements the communicator application platform.

The CMT implements the GSM transceiver and basic data functionality, both transparent and non–transparent data. All UI functionality is combined into one UI module (BS2) but both PDA and CMT control their respective UI independently.

The Functional units and the implementation differ slightly. Due to mechanical reasons some components are placed into a different module than they functionally belong. E.g. audio components are placed into BS1 (PDA) module even if they functionally belong to the CMT.

Block Diagram

The following diagram describes the functional RAE–2N block diagram.



PDA Module

The PDA modules has its own power management chip, the Phaser. The Phaser regulates the voltages for PDA components. It also controls PDA power–up/down procedure by providing POWERGOOD and RESET signals to Scotty.

The PDA processor Scotty is an embedded 486 processor manufactured by AMD. The Scotty contains a set of PC peripherals except a parallel port. It also has some additional peripherals like LCD controller and MMC host controller which are not standard to PCs. CPU has a 8k cache.

The PDA interfaces the CMT with 115kbps serial bus (FBUS). It also provides low frequency clock (32kHz) to CMT. PDA also can get information about CMT state (on/off) and wake up CMT.

CMT Module

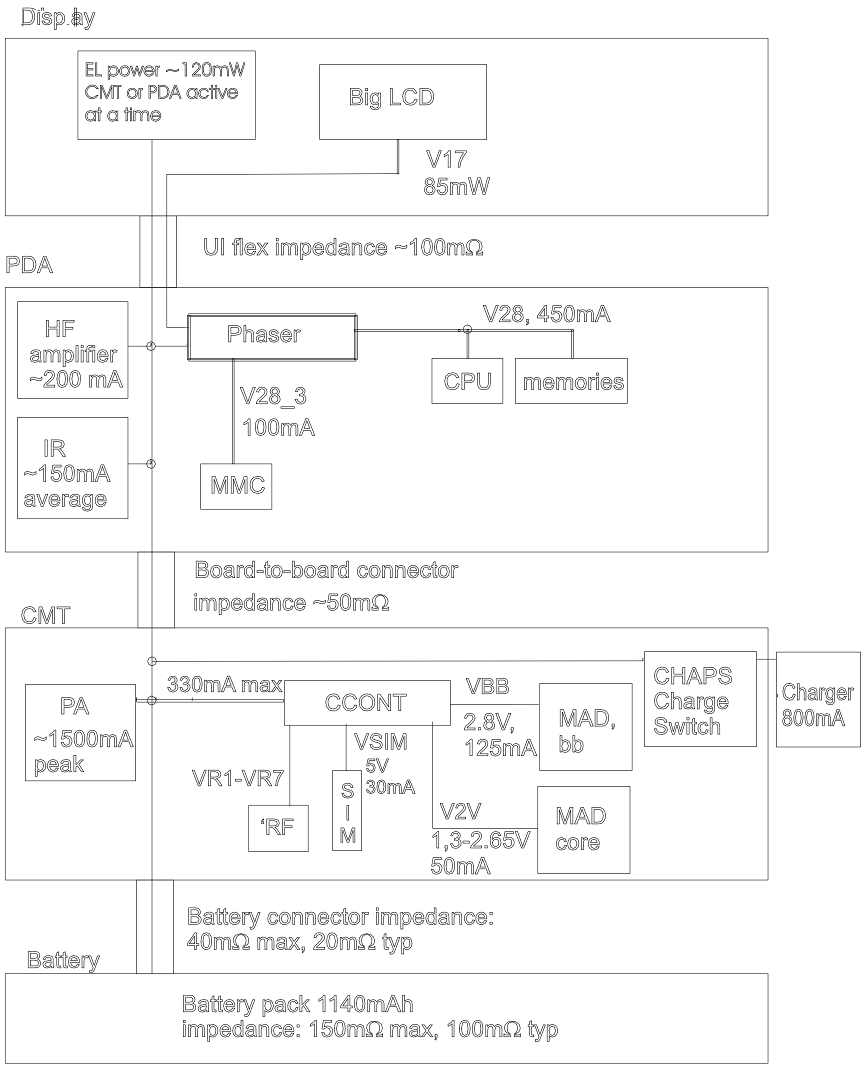
The CMT is based on DCT3 engine and it is functionally the same. Sleep clock (32kHz) is received from PDA side.

All the audio components are controlled by CMT (COBBA). It PDA wishes to play sounds those are first sent to CMT. Keyclicks and some system sounds are exceptions and are played directly by PDA.

Power Distribution

All the digital circuitry modules use 2.8V nominal operating voltage. Power is drawn from 1140mAh Li–Ion battery. Higher voltages are generated for LCD, SIM and backlighting.

The diagram below describes the power distribution of the product.



Audio

The transceiver has two speakers; earpiece for the telephone interface and handsfree (HF) speaker. Different kind of tones can be played through speakers. HF speaker is driven only by CMT module. The earpiece can be driven either by the PDA or the CMT. The transceiver has one microphone connected to the CMT module.

The speakers are used :

1 HF speaker:
Ringing tones
All PDA tones that can be WAV–type
Talk when HF speaker is enabled

2 Earpiece:
Talk and WAV–sounds when HF disabled
Keyclicks
Fixed PDA tones

Software Specifications of Interfaces

CMT SW is based on HD943. This product program has added internal data functionality and ECI message interface.

External Devices

External devices can be connected through serial cable (DLR–2) or IR. The protocols used are:

IrOBEX (ir–connectivity),

UltraIR (DCT3 connectivity),

IrDA (PC–connectivity)

IrTranP (camera connectivity).

The PC connectivity uses a specific PCCOM protocol on top of the IrDA or serial connection.

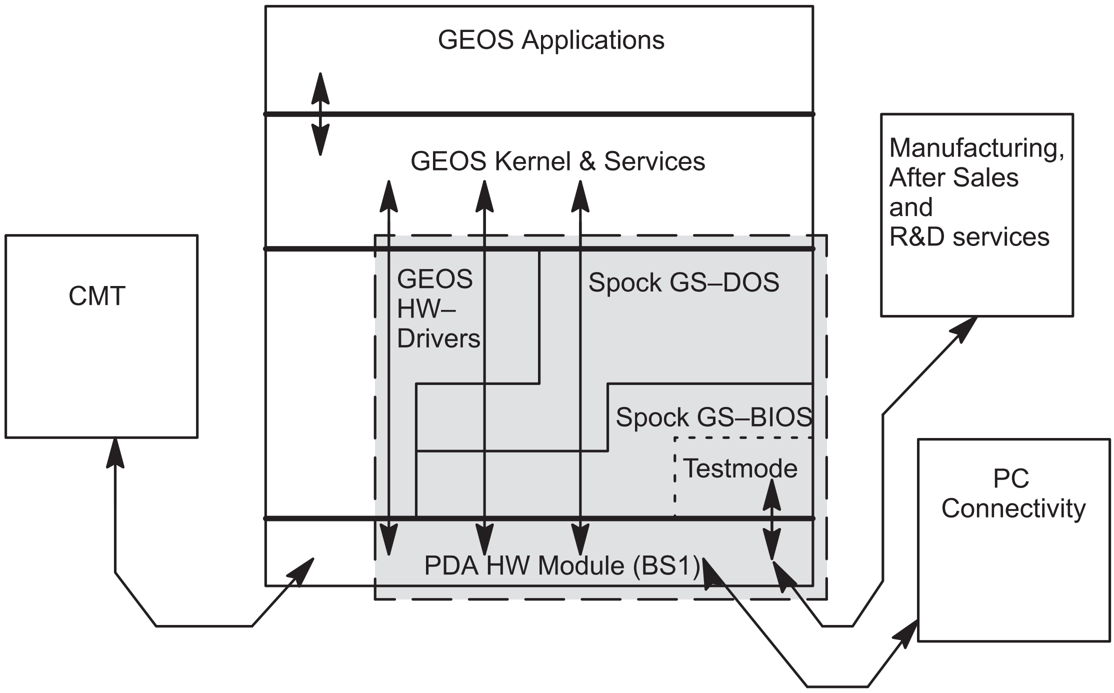
Interfaces Between Transceiver Processors

PDA and CMT processors interface through serial FBUS channel. On top of the physical FBUS link two separate protocols are used. The Phonet protocol is used to transport CMT related control information and data–frames. ”RBUS” is used to transport ECI (External Control Interface) messages between PDA UI and CMT.

Software–Hardware Interface

CMT sw/hw interface is the same as hd940 is using.

PDA software is running on AMD Elan SC450 processor. Operating frequency is 33MHz.



The lowest level of HW/SW interface is handled by the BIOS which provides some basic services for upper sw layers. E.g. read data from memory card.

Testmode is used by production and After Sales. It provides the interface to test and program PDA and CMT modules.

DOS layer implements only a subset of DOS functions known from conventional PC. DOS is used mainly in testmode and to launch GEOS.

GEOS is the basic SW platform to all applications that user sees. It however interfaces directly to some HW resources, like LCD display or serial ports, by its own HW drivers.

Alignment

Both PDA and CMT modules require alignment. Alignment is done at module level to modules BS8 and BS1. LCD temperature measurement can be done only after the assembly of the product.

The following parameters are adjusted in CMT module (BS8): TX power, RSSI, AFC ,TX I&Q, battery voltage and charging current.

PDA module (BS1) needs alignment of: battery voltage, LCD contrast voltage.

Alignment is software based. Predefined reference point measurements are stored into EEPROM (CMT) or flash (PDA).

Flashing

Product requires two separate flash images for executable code: one for the CMT and one for the PDA system. Language versions are held in separate files.

CMT flashing uses partly the same equipment as other DCT3 family products.

PDA flashing can be done with JTAG (low level flashing) or WinTesla. WinTesla flashing is recommended.

Vocabulary

AMD	Advanced MIcro Devices
BIOS	basic input/output system
CMT	cellular mobile telephone
FSTN	Film compensated Super Twisted Nematic
HF	Hands Free
IR	infra red
IrDA	IR data association
MMC	Multi Media Card
PDA	personal digital assistant
RX	receive
TX	transmit

Chapter 2

–Transceiver BS8–
Baseband Block

AMENDMENT RECORD SHEET

Amendment Number	Date	Inserted By	Comments
	11/98		Original

CONTENTS –Baseband

Page No

Introduction

This document contains the specification to the Baseband section of the BS8 module. The BS8 module carries out almost all CMT functions of RAE–2. BS8 can be divided into two functional sections; BaseBand (BB) and RF. Some of CMT baseband circuits are implemented to both BS1 and BS2 modules.

The Baseband module BS8 comprises four ASICs (CHAPS, CCONT, COBBA–GJ and MAD2) that perform the baseband functions of the module.

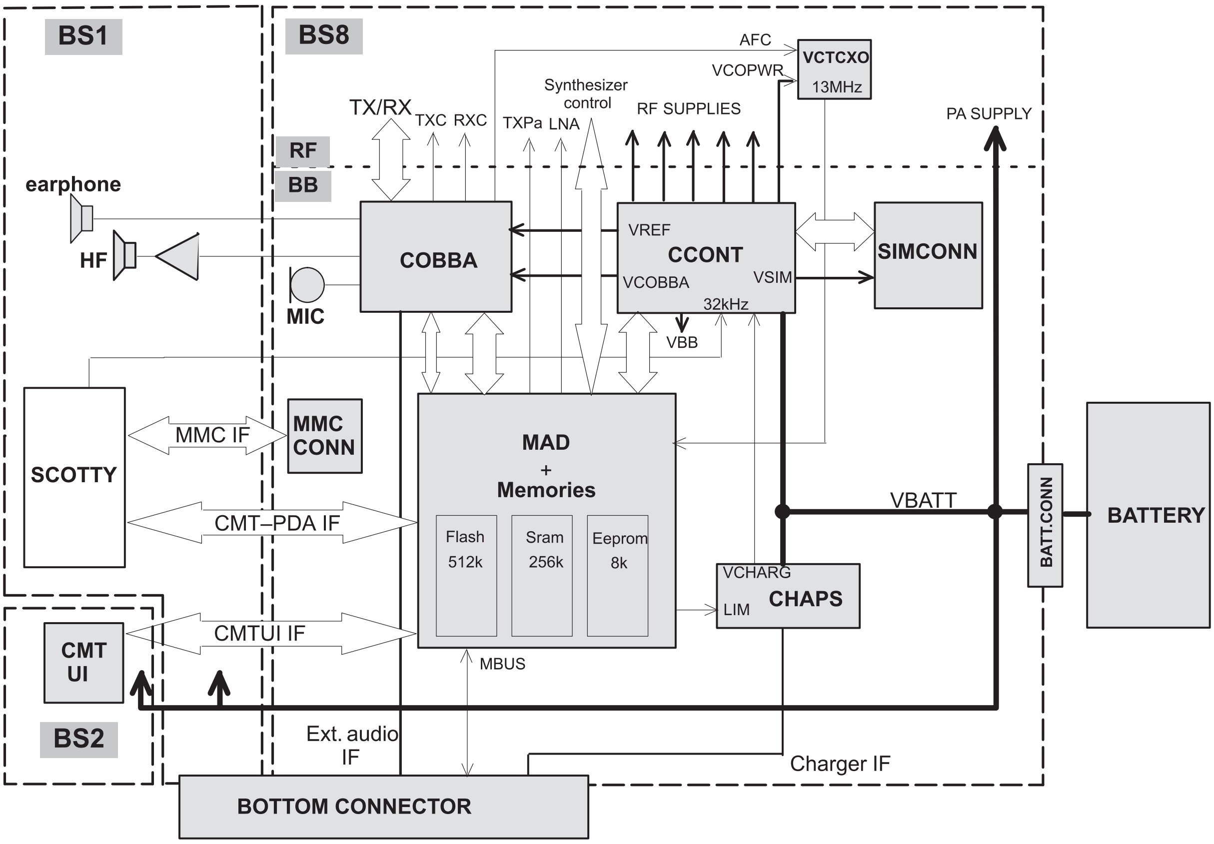


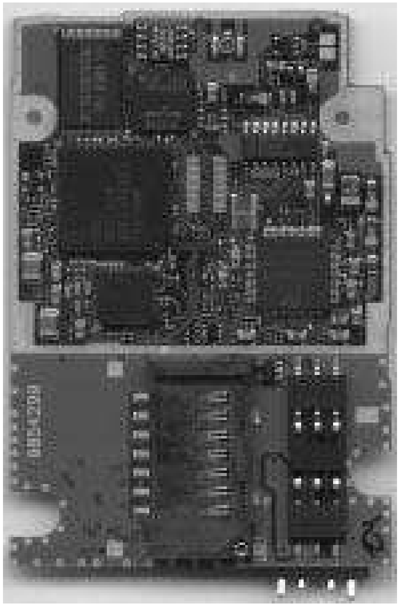
Figure 1. BS8 BaseBand block in RAE–2 product

Technical Summary

The BS8 module is implemented on a single double side 8–layer printed circuit board. The main part of the baseband area is located on the bottom side of the PCB and only some components (bottom connector, battery connector and some filter components) are placed on the upper side (RF side). Component height space on the baseband is 2.0mm.

The baseband is running from a 2.8V power rail, which is supplied by the power controlling ASIC. In the CCONT ASIC there are 6 individually controlled regulator outputs for RF–section and two outputs for the baseband. In addition there is one +5V power supply output (V5V) for flash programming voltage and for other purposes where a higher voltage is needed. The CCONT contains also a SIM interface, which supports both 3V and 5V SIM–cards.

BaseBand Side



RF Side

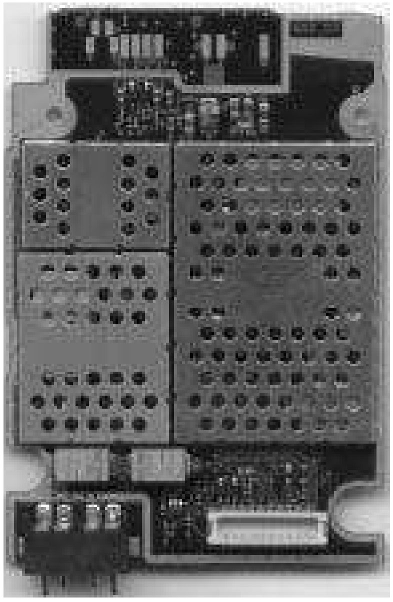


Figure 2. BS8 Module

The interface between the baseband and the RF section is handled by the specific ASIC COBBA. The COBBA provides:
– A/D and D/A conversion of the in–phase and quadrature receive and transmit signal paths
– A/D and D/A conversions of received and transmitted audio signals to and from the UI section.

The COBBA supplies the analog TXC and AFC signals to the RF section according to the MAD DSP digital control and converts the analog AGC into digital signal for the DSP. The data transmission between the COBBA and the MAD is implemented using a parallel connection for high speed signalling and a serial connection for PCM coded audio signals.

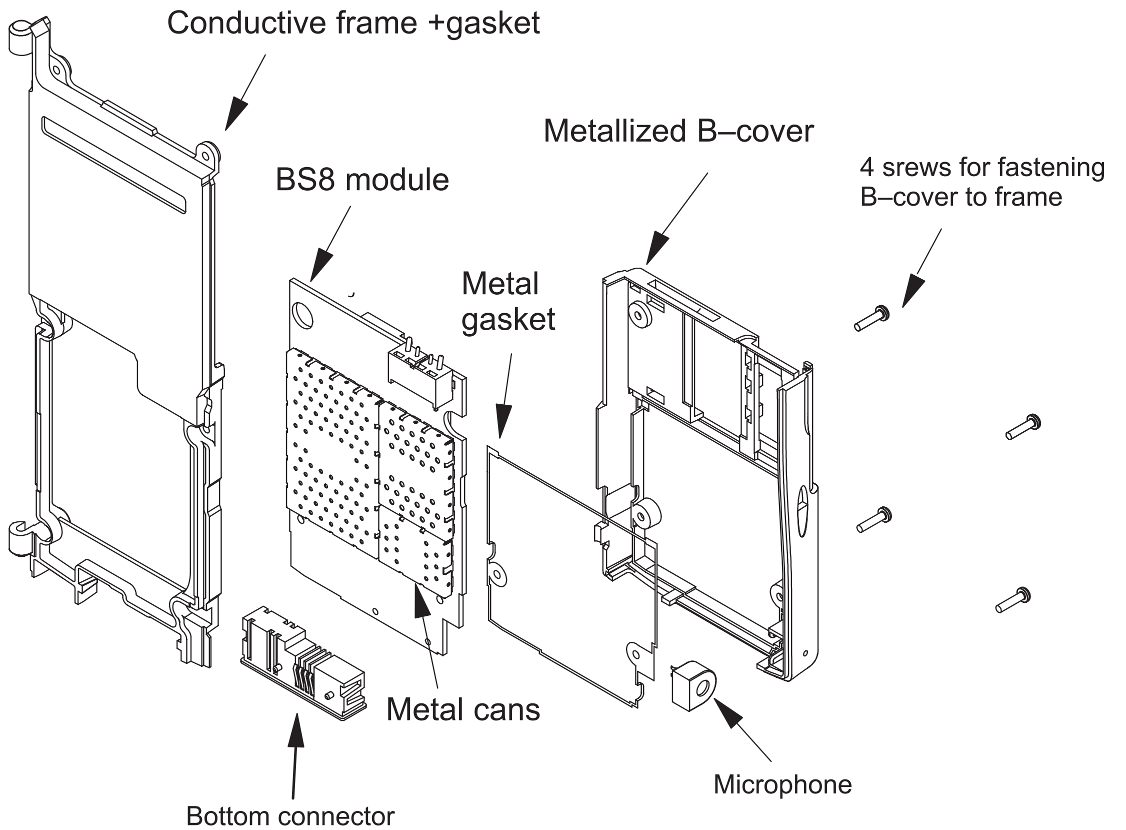
Digital speech processing is handled by the MAD asic.

The COBBA is a dual voltage circuit, the digital parts are running from the baseband supply VBB and the analog parts are running from the analog supply VCOBBA.

The COBBA supports three microphone inputs and two earphone outputs. The inputs can be taken from an internal microphone, a headset microphone or from an external microphone signal source.

The output for the internal earphone is a dual ended type output capable of driving a dynamic type speaker. Input and output signal source selection and gain control are performed inside the COBBA according to control messages from the MAD. Call alerts, keypad tones, DTMF, and other audio tones are generated and encoded by the MAD and transmitted to the COBBA for decoding.

EMC shielding (figure below) is implemented on the BB side using a metallized plastic B–cover and conductive gasket between the B–cover and the PCB. On the RF side the engine is shielded with a conductive frame which makes a contact to a ground ring of the CMT board and a ground plane of the PDA board. There is a conductive gasket between the frame and the PCB for ensuring proper shielding. In addition he RF area has three metal cans for RF shielding. Heat generated by the circuitry is conducted out mainly via the PCB ground planes.



Technical Specifications

Maximum Ratings

Parameter	Rating
Battery voltage, idle mode	–0.3 ... 4.1V without charger
Charger input voltage	–5.0 ... 16V
Operating temperature range	–25C to +70 C
Storage temperature range	–40C to +85 C

DC Characteristics

Supply voltages

Line Symbol	Minimum	Typical / Nominal	Maximum	Unit / Notes
Supply battery voltage	3.0	3.6	4.1	V
Battery powerup voltage (HW)	2.9	3.0	3.1	V
Battery cut off voltage (HW)	2.7	2.8	2.9	V
Regulated baseband supply voltage	2.7	2.8	2.85	V
Regulated baseband supply current	3	50	125	mA
Regulated VCORE supply voltage		1.3 – 2.65		V (changeable)
Regulated VCORE supply current			50	mA
COBBA analog supply voltage	2.7	2.8	2.85	V
COBBA analog supply current	5	20	100	mA
Regulated 5V supply voltage	4.8	5.0	5.2	V
Regulated 5V supply current	0	1	30	mA
Regulated 5V SIM supply voltage	4.8	5.0	5.2	V
Regulated 5V SIM supply current	3	10	30	mA
Regulated 3V SIM supply voltage	2.8	3.0	3.2	V
Regulated 3V SIM supply current	1	6	30	mA
Voltage reference	1.4775	1.5	1.5225	V

Note: The RF voltages are described later

AC Characteristics

Table 1. AC Specifications

Line symbol	Minimum	Typical / Nominal	Maximum	Unit / Notes
32kHz		32768		Hz, Sleep clock
RFIClk		13		MHz, System clock
PCMClk		8		kHz, PCM clock
SIMClk		3.25		MHz, SIM Clock

Connectors

External Connections from Baseband section of BS8 module

This section describes the external electrical connections and interface levels on the baseband section of the BS8 module. The electrical interface specifications are collected into tables that cover a connector or a defined interface each.

Connectors to other modules of the product

Bottom Connector

The bottom connector has spring type of connections. In BS8 module there are contact pads for the spring connections.

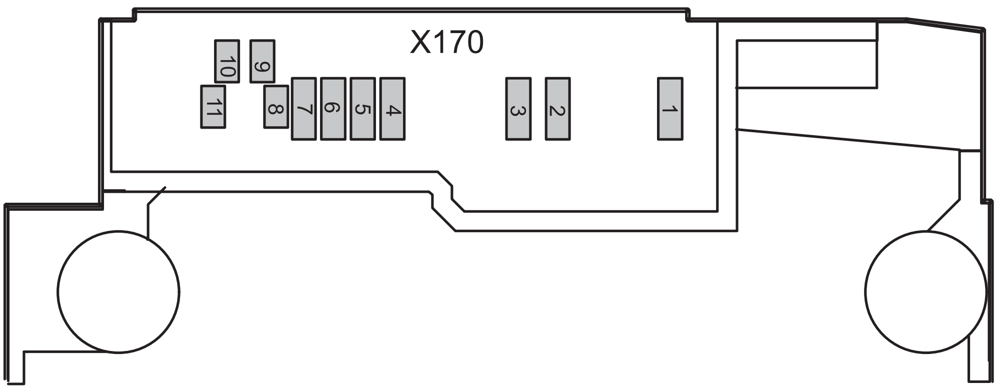


Figure 3. Bottom connector pads in BS8 module

The electrical specifications in the next table show the bottom connector signals and levels on the baseband. The system connector is used to connect the transceiver to accessories. The table gives the idle voltage produced by the acceptable chargers at the DC connector input. The absolute maximum input voltage is 30 V due to the transient suppressor that is protecting the charger input.

Table 2. Baseband signals of the bottom connector (X170)

Pin	Name	Min	Typ	Max	Unit	Notes
1	**L_GND**	0		0	V	Supply ground
2	**VIN**	7.25	7.6	7.95	V	Unloaded ACP–7 Charger (5kohms load)
				16.9	V	Peak charger output voltage (5kohms load)
		3.25	3.6	3.95	V	Loaded charger output voltage (10ohms load)
		320	370	420	mA	Supply current
		7.1	8.4	9.3	V	Unloaded ACP–9 Charger
		3.25	3.6	3.95	V	Loaded charger output voltage (10ohms load)
		720	800	850	mA	Supply current
3	**CHRG_ CTRL**	0		0.5	V	Charger control PWM low
		2.0		2.85	V	Charger control PWM high
			32		Hz	PWM frequency for a ACP–9
		1		99	%	PWM duty cycle
4	**SGND**		47		Ω	Output AC impedance (ref. GND)
			10		μF	Series output capacitance
			380		Ω	Resistance to phone ground
5	**XEAR**		47		Ω	Output AC impedance (ref. GND)
			10		μF	Series output capacitance
		16		300	Ω	Load AC impedance to SGND (Headset)
		4.7	10		kΩ	Load AC impedance to SGND (Accessory)
			1.0		Vpp	Maximum output level (no load)
			22	626	mV	Output signal level
			10		kΩ	Load DC resistance to SGND (Accessory)
		16		1500	Ω	Load DC resistance to SGND (Headset)
			2.8		V	DC voltage (47k pull–up to VBB)
	HEAR		28	626	mV	Earphone signal (HF– HFCM) Connected to COBBA HF output
6	**XMIC**	2.0		2.2	kΩ	Input AC impedance
				1	Vpp	Maximum signal level
		1.47		1.55	V	Mute (output DC level)
		2.5		2.85	V	Unmute (output DC level)
		100		600	μA	Bias current
			58	490	mV	Maximum signal level
	HMIC	0	3.2	29.3	mV	Microphone signal Connected to COBBA MIC3P input
7	**MBUS**	0 2.1	logic low logic high	0.5 2.85	V	Serial bidirectional control bus. Baud rate 9600 Bit/s Phone has a 4k7 pullup resistor
12,15	**GND**	0		0	V	RF ground
13	**RF_OUT**	5	(TX levels)	33	dBm	RF signal from RF switch to internal antenna
14	**RF_IN**	5	(TX levels)	33	dBm	RF signal from PA to RF switch.

The bottom connector has mounting holes for a fastening to a shielding frame located between the PDA and CMT modules. The bottom connector has spring type connections to the CMT and the PDA module.

The bottom connector includes the following parts:

– DC connector for external plug–in charger and a desktop charger
– System connector for accessories.
– Connector for external RF signal. This connector is equipped with throw–over–switch. This is needed to change the RF signal path between external and internal antenna depending whether the ext antenna cable is connected or not.

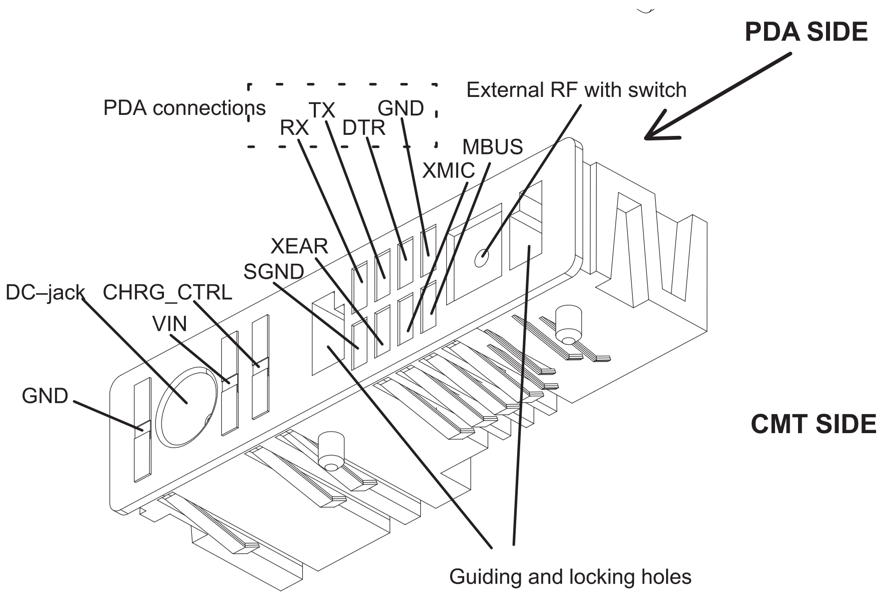


Figure 4. Bottom Connector

Battery Connector

The electrical specifications for the battery connector are listed in the next table. The BSI contact of the battery connector is also used to detect when the battery is removed suddenly.

This information is needed for driving the SIM card safely down before supply voltage is lost. The BSI contact in the battery connector has 0.5mm shorter working length than the supply power contacts to give enough time for the SIM shut down.

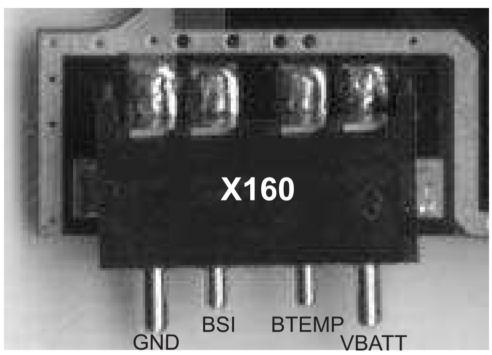


Figure 5. Battery Connector

Table 3. Battery Connector Electrical Specifications (X160)

Pin	Name	Min	Typ	Max	Unit	Notes
1	**VBATT**	3.0	3.6	4.1	V	Battery voltage
2	**BSI**	0		2.85	V	Battery size indication CMT has 180kohm pull up resistor. SIM Card removal detection (Threshold is 2.4V@VBB=2.8V)
		17.1	18	18.9	kohm	Field Test Battery (4.1V)
		21.8	22	22.2	kohm	BBS–5 Service battery (No cells)
		31.35	33	34.65	kohm	BLN–3 Li–ion battery (4.1V)
		5			ms	The minimum time from BSI contact disengaged its battery contact to VBATT/GND disengaged its battery contacts when battery is removed.
3	**BTEMP**	0		1.4	V	Battery temperature indication CMT has a 100k (+–5%) pullup resistor, Battery package has a NTC pulldown resistor: 47k+–5%@+25C , B=4050+–3%
		0		1	kohm	Local mode initialization (in production)
4	**GND**	0		0	V	Battery ground

SIM card Connector

The SIM card connector is located on the baseband side of the BS8 module. The contacts of the SIM card connector are protected against electric discharge with ESD protection components.

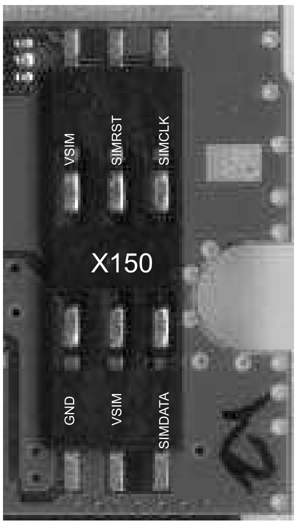


Figure 6. SIM Card Connector

Table 4. SIM Connector Electrical Specifications (X150)

Pin	Name	Parameter	Min	Typ	Max	Unit	Notes
4	**GND**	GND	0		0	V	Ground
3, 5	**VSIM**	5V SIM Card 3V SIM Card	4.8 2.8	5.0 3.0	5.2 3.2	V	Supply voltage
6	**DATA**	5V Vin/Vout 3V Vin/Vout	4.0 0 2.8 0	”1” ”0” ”1” ”0”	VSIM 0.5 VSIM 0.5	V	SIM data Trise/Tfall max 1us
2	**SIMRST**	5V SIM Card 3V SIM Card	4.0 2.8	”1” ”1”	VSIM VSIM	V	SIM reset
1	**SIMCLK**	Frequency Trise/Tfall		3.25	 25	MHz ns	SIM clock

VSIM supply voltages are specified to meet type approval requirements regardless the tolerances in components.

Memory Card Connector

The Memory card connector locates on BS8 module. Memory card is a changeable Flash or ROM memory with variable memory size. The PDA CPU can access with Memory card via synchronous serial interface. Memory card signals are routed from BS1 module to BS8 module through board to board connector.

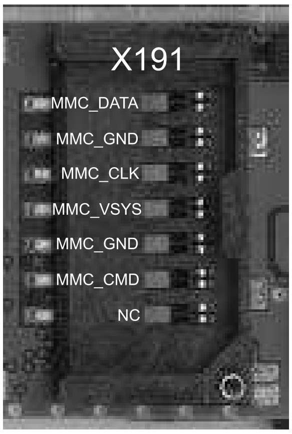


Figure 7. Memory Card Connector

The signals of the MMC connector are specified in the board to board connector table.

Board to Board Connector

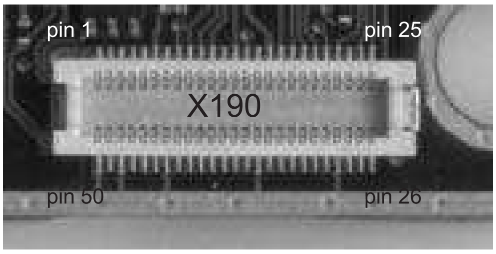


Figure 8. BoBo Connector

All interfaces (except RF antenna signal) from the BS8 module to the other RAE–2 modules are routed over a 50–pins board to board connector. The interfaces can be divided into several groups; CMT–UI, CMT–HF audio, CMT–PDA, MMC–PDA and supply lines for the BS1 and the BS2 modules.

The CMT keyboard with keyboard illumination parts and the CMT display module with display illumination parts are implemented on a separate UI module (BS2), which contains also the PDA user interface and an antenna matching circuit. The baseband signals to the UI are routed over an board to board connector to the BS1 module and from the BS1 module through the hinge flex to the BS2 module.

The Handsfree speaker and earpiece are included in the audio holder. Because the audio holder and the HF amplifier are located on the PDA module, several signals through the board to board connector are needed for carrying audios from the CMT to the PDA.

There are data signals for data transmission between the CMT and the PDA modules. Some I/O signals are needed for carrying logic state information between modules.

Signal definition and the most important specifications of signals are listed in the next table.

Table 5. Board to Board Connector (X190)

Pin	I/O	Name	Function	Min	Typ	Max	Unit	Description / Note
1,2, 3,4, 5		**VBATT**	Battery Positive	3.0	3.6	4.1	VDC	Unregulated Battery Voltage
				1.5		1000	mA	Current to BS1 and BS2 module (max=peak current)
6	O	**XEAR**	Audio Output for Handsfree			500	mVpp	
7		**GND**	Global Ground					Reference for other signals
8	O	**BATTDET**	Battery Position Information	0.23	0.26	0.28	VDC	Field Test battery (only R&D use)
				0.28	0.30	0.33	VDC	Service battery (BBS–5)
				0.39	0.43	0.48	VDC	BLN–3 battery
9	O	**HFENA**	Internal Handsfree Amplifier Control	0		0.5	VDC	Low, HF amplifier disabled
				2.1		2.85	VDC	High, HF amplifier enabled

Table 5. Board to Board Connector (X190) (continued)

Pin	I/O	Name	Function	Min	Typ	Max	Unit	Description / Note
10	O	**EARP**	Earpiece Positive	50		223	mVpp	Differential voltage between EARP and EARN nodes
11	O	**EARN**	Earpiece Negative					
12		**GND**	Global Ground					
13	I	**PWRONx**	PDA start CMT to Service Request State (SRS)	0		0.45	VDC	Active state, min. 64ms
				2.3	2.8	2.85	VDC	Inactive state
14	I	**32kHz**	Sleep clock to CMT	0		0.45	VDC	Pulse low level
				2.3	2.8	2.85	VDC	Pulse high level
						12	mA	Maximum current from PDA
					32768		Hz	Pulse frequency
				20	50	80	%	Duty cycle (CMT requirements)
						1	%	Jitter (CMT requirements)
15		**GND**	Global Ground					
16	O	**VBB**	CMT regulated system voltage	2.7	2.8	2.85	VDC	Regulated CMT baseband voltage
						1	mA	Maximum current
17	I	**PWRKEYx**	CMT Power On/Off Switch	0		0.5		Low, active state
				2.7		2.85	VDC	High, inactive state
18	O	**CMT_BL_ON**	CMT UI Backlight On	0		0.5	VDC	Low, backlight off
				2.1	2.8	2.85	VDC	High, backlight on
19	I	**ROW3**	CMT Keys Row 3	0		0.2	VDC	Low
				2.5	2.8	2.85	VDC	High
20	I	**ROW2**	CMT Keys Row 2	0		0.2	VDC	Low
				2.5	2.8	2.85	VDC	High
21	I	**ROW1**	CMT Keys Row 1	0		0.2	VDC	Low
				2.5	2.8	2.85	VDC	High
22	I	**ROW0**	CMT Keys Row 0	0		0.2	VDC	Low
				2.5	2.8	2.85	VDC	High
23		**GND**	Global Ground					
24	O	**COL4**	CMT Keys Column 4	0		0.5	VDC	Low
				2.1		2.85	VDC	High
25	O	**COL3**	CMT Keys Column 3	0		0.5	VDC	Low
				2.1		2.85	VDC	High
26	O	**COL2**	CMT Keys Column 2	0		0.5	VDC	Low
				2.1		2.85	VDC	High
27	O	**COL1**	CMT Keys Column 1	0		0.5	VDC	Low
				2.1		2.85	VDC	High
28	O	**COL0**	CMT Keys Column 0	0		0.5	VDC	Low
				2.1		2.85	VDC	High
29		**GND**	Global Ground					

Table 5. Board to Board Connector (X190) (continued)

Pin	I/O	Name	Function	Min	Typ	Max	Unit	Description / Note
30	O	**LCDCD**	CMT LCD Command / Data Select	0		0.5	VDC	Low, Command
				2.1		2.85	VDC	High, Data
31	O	**LCDRSTx**	CMT LCD Reset	0		0.5	VDC	Low, Reset active
				2.1		2.85	VDC	High, Reset inac-tive
32	O	**LCDCSx**	CMT LCD Chip Select	0		0.5	VDC	Low, active
				2.1		2.85	VDC	High, inactive
33		**GND**	Global Ground					
34	O	**GENSCLK**	CMT LCD and CCONT Serial Clock	0		0.5	VDC	Low
				2.1		2.85	VDC	HIgh
					3.250		MHz	Pulse frequency in active state (LCD communication)
35	O	**GENSDIO**	CMT LCD and CCONT Serial Data	0		0.5	VDC	Low
				2.1		2.85	VDC	High
					1.625		MHz	Maximum pulse frequency
36		**GND**	Global Ground					
37	I	**FBUS_RXD**	Fast Serial Data to CMT	0		0.45	VDC	Low
				2.3		2.85	VDC	High
					220		kΩ	Pulldown resistor in CMT
38	0	**FBUS_TXD**	Fast Serial Data to PDA	0		0.5	VDC	Low
				2.1		2.85	VDC	High
					47		kΩ	Pullup resistor in CMT
39		**GND**	Global Ground					
40	I/O	**MBUS**	Bidirectional Serial Bus	0		0.5	VDC	Low, to the PDA
				2.1		2.85	VDC	Low, to the PDA
				0		0.45	VDC	Low, from the PDA
				2.3	2.8	2.85	VDC	High, from the PDA
					47		kΩ	Pullup resistor in CMT
41	I	**VSYS**	PDA regulated system voltage	2.75	2.8	2.85	VDC	Max current 1mA
42	I	**LIDSWITCH**	Lid State Information		0		VDC	Low, Lid closed
				2.75	2.8	2.85	VDC	High, Lid open
					10		kohm	Pull–up resistor in PDA
43			THIS SIGNAL IS NOT IN USE!					
44		**GND**	Global Ground					

Table 5. Board to Board Connector (X190) (continued)

Pin	I/O	Name	Function	Min	Typ	Max	Unit	Description / Note
45	I/O	**MMC_CMD**	Memory Card Command / Address / Response, Bidirectional	0	0	0.45	VDC	Low, Data to the card
				2.3	2.8	2.85	VDC	High, Data to the card, pulled up with 10kohm resistor to MMC_VSYS in CMT module
						0.34	VDC	Low, Data from the card
				2.1			VDC	High, Data from the card, pulled up with 10kohm resistor to MMC_VSYS in CMT module
					259.3		kHz	Frequency
46	I	**MMC_VSYS**	Memory Card Power Supply	2.75		2.85	VDC	
47	I/O	**MMC_DATA**	Memory Card Bidirectional Data	0	0	0.45	VDC	Low, Data to the card
				2.3	2.8	2.85	VDC	High, Data to the card, pulled up with 10kohm resistor to MMC_VSYS in CMT module
				0	0	0.34	VDC	Low, Data from the card
				2.1			VDC	High, Data from the card, pulled up with 10kohm resistor to MMC_VSYS in CMT module
					8.294		MHz	Frequency
48		**GND**	Global Ground					
49	I	**MMC_CLK**	Memory Card Clock	0	0	0.45	VDC	Low
				2.3	2.8	2.85	VDC	High
				0.2592		8.294	MHz	Frequency
50		**GND**	Global Ground					

RF Coax cable connector

A small SMD coax cable connector is situated on the baseband side of the BS8 module. It comprises the RF output for the internal antenna.

Internal Signals and Connections

This section describes the internal electrical connections and interface levels on the baseband part of the BS8 module. The electrical interface specifications are collected into tables that cover a connector or a defined interface each.

Microphone

The internal microphone is connected to the PCB with spring contacts. The microphone input level is specified in the table below. The microphone requires a bias voltage to operate. The bias voltage is generated from the VCOBBA supply with a transistor which is driven by the MAD general I/O signal (MCUGenOut5).

Table 6. Microphone signals (B250)

Pin	Name	Min	Typ	Max	Unit	Notes
6	**MICP**		3.2	20	mVpp	Differential voltage between MICP and MICN

RF– Baseband interface

The interface signals between the BB and the RF section are shown in next the table as a logical interface. On PCB level the baseband supplies voltages from the CCONT to the separate rf–sub–blocks. The maximum values specified for the digital signals in the table are the absolute maximum values from the RF interface point of view.

Table 7. AC and DC Characteristics of RF/BB signals

Signal name	From To	Parameter	Minimum	Typical	Maximum	Unit	Function
VBATT	Battery RF	Voltage	3.0	3.6	5.0/6.0	V	Supply voltage for RF (PA on/PA off)
		Current			3500	mA	
VXOENA	MAD CCONT	Logic high ”1”	2.1		2.85	V	VR1, VR6 in CCONT ON
		Logic low ”0”	0		0.5	V	VR1, VR6 in CCONT OFF
SYNPWR	MAD CCONT	Logic high ”1”	2.1		2.85	V	VR3, VR4 in CCONT ON
		Logic low ”0”	0		0.5	V	VR3,VR4 in CCONT OFF
RXPWR	MAD CCONT	Logic high ”1”	2.1		2.85	V	VR2, VR5 in CCONT ON
		Logic low ”0”	0		0.5	V	VR2, VR5 in CCONT OFF
TXPWR	MAD CCONT	Logic high ”1”	2.1		2.85	V	VR7 in CCONT ON
		Logic low ”0”	0		0.5	V	VR7 in CCONT OFF
VREF	CCONT SUMMA	Voltage	1.478	1.5	1.523	V	Reference voltage for SUMMA and CRFU1a
		Current			100	uA	
		Source resistance		10		ohm	
PDATA0	MAD CRFU1A	Logic high ”1”	2.1		2.85	V	Nominal gain in LNA
		Logic low ”0”	0		0.5	V	Reduced gain in LNA
SENA	MAD SUMMA	Logic high ”1”	2.1		2.85	V	PLL enable
		Logic low ”0”	0		0.5	V	
SDATA	MAD SUMMA	Logic high ”1”	2.1		2.85	V	Synthesizer data
		Logic low ”0”	0		0.5	V	
		Data rate frequency		3.25		MHz	
SCLK	MAD SUMMA	Logic high ”1”	2.1		2.85	V	Synthesizer clock
		Logic low ”0”	0		0.8	V	
		Data rate frequency		3.25		MHz	

Table 7. AC and DC Characteristics of RF/BB signals (continued)

Signal name	From To	Parameter	Mini-mum	Typical	Maxi-mum	Unit	Function
AFC	COBBA VCTCXO	Voltage	0.046		2.254	V	Automatic frequency control signal for VC(TC)XO
		Resolution	11			bits	
		Load resistance (dynamic)	10			kohm	
		Load resistance (static)	1			Mohm	
		Noise voltage			500	uVrms	10...10000Hz
		Settling time			0.5	ms	
RFC	VCTCXO MAD	Frequency		13		MHz	High stability clock signal for the logic circuits
		Signal amplitude	0.5	1.0	2.0	Vpp	
		Load resistance	10			kohm	
		Load capacitance	5	7	10	pF	
RXIP/RXIN	SUMMA COBBA	Output level		50	1344	mVpp	Differential RX 13 MHz signal to baseband
		Source impedance			600	ohm	
		Load resistance		1		Mohm	
		Load capacitance			4	pF	
TXIP/TXIN	COBBA SUMMA	Differential voltage swing	0.75 x 1.022	0.75 x 1.1	0.75 x 1.18	Vpp	Differential in–phase TX baseband signal for the RF modulator
		DC level	0.784	0.8	0.816	V	
		Differential offset voltage (corrected)			+/– 2.0	mV	
		Diff. offset voltage temp. dependence			+/– 1.0	mV	
		Source impedance			200	ohm	
		Load resistance	40			kohm	
		Load capacitance			10	pF	
		DNL			+/– 0.9	LSB	
		INL			+/–1	LSB	
		Group delay missmatch			100	ns	
TXQP/TXQN	COBBA SUMMA	Differential voltage swing	0.75 x 1.022	0.75 x 1.1	0.75 x 1.18	Vpp	Differential quadrature phase TX baseband signal for the RF modulator
		DC level	0.784	0.8	0.816	V	
		Differential offset voltage (corrected)			+/– 2.0	mV	
		Diff. offset voltage temp. dependence			+/– 1.0	mV	
		Source impedance			200	ohm	
		Load resistance	40			kohm	
		Load capacitance			10	pF	
		Resolution	8			bits	
		DNL			+/– 0.9	LSB	
		INL			+/–1	LSB	
		Group delay mismatch			100	ns	

Table 7. AC and DC Characteristics of RF/BB signals (continued)

Signal name	From To	Parameter	Mini-mum	Typical	Maxi-mum	Unit	Function
TXP	MAD SUMMA	Logic high ”1”	2.1		2.85	V	Transmitter power control enable
		Logic low ”0”	0		0.5	V	
TXC	COBBA SUMMA	Voltage Min	0.12		0.18	V	Transmitter power control
		Voltage Max	2.27		2.33	V	
		Vout temperature dependence			10	LSB	
		Source impedance active state			200	ohm	
		Source impedance power down state		high Z			
		Input resistance	10			kohm	
		Input capacitance			10	pF	
		Settling time			10	us	
		Noise level			500	uVrms	0...200 kHz
		Resolution	10			bits	
		DNL			+/–0.9	LSB	
		INL			+/– 4	LSB	
		Timing inaccuracy			1	us	
RXC	COBBA SUMMA	Voltage Min	0.12		0.18	V	Receiver gain control
		Voltage Max	2.27		2.33	V	
		Vout temperature dependence			10	LSB	
		Source impedance active state			200	ohm	
		Source impedance power down state		grounded			
		Input resistance	1			Mohm	
		Input capacitance			10	pF	
		Settling time			10	us	
		Noise level			500	uVrms	0...200 kHz
		Resolution	10			bits	
		DNL			+/–0.9	LSB	
		INL			+/– 4	LSB	

NOTE: Logic controls in low state when RF in power off.

Functional Descriptions

Power Management

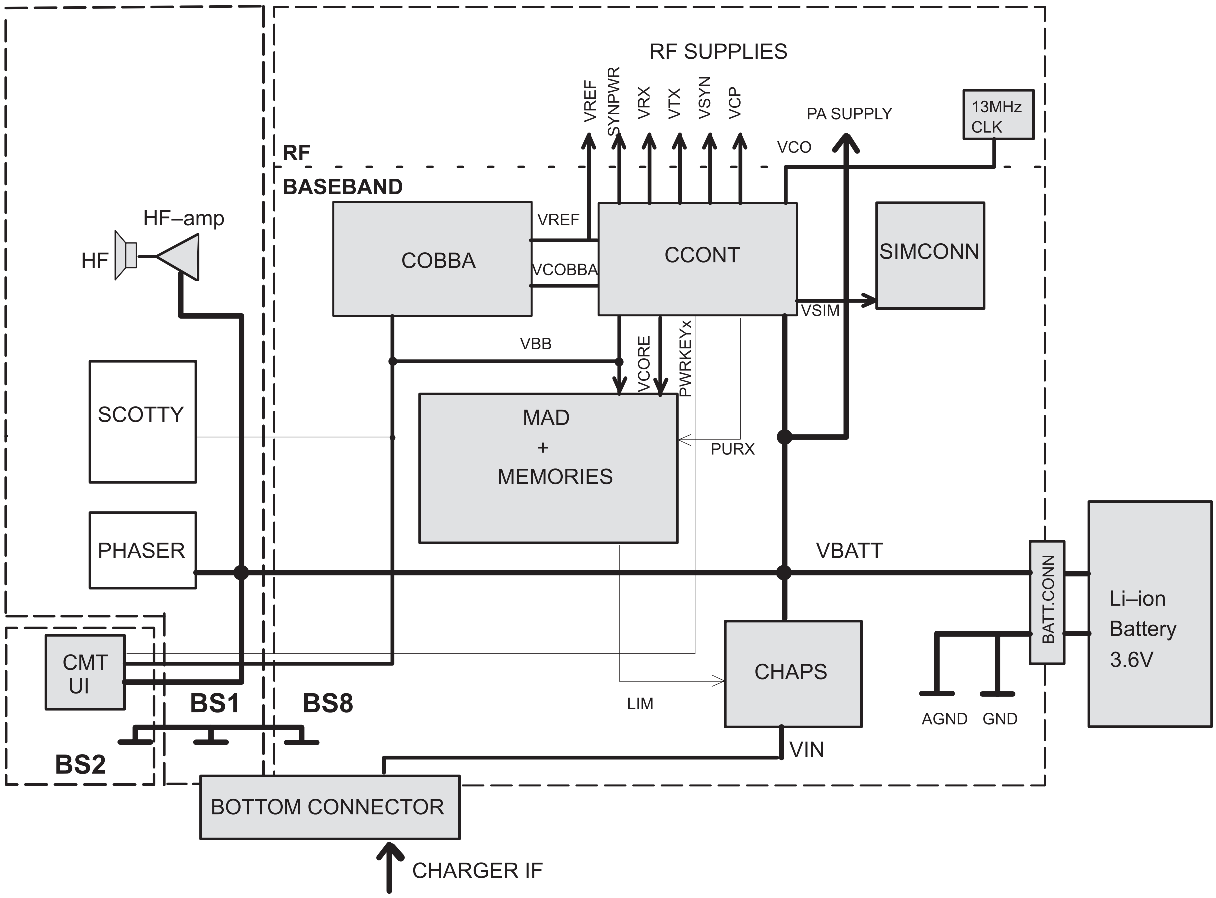


Figure 9. CMT power distribution

In normal operation the baseband is powered from the phone Li–ion battery. The battery consists of two Lithium–Ion cell connected in parallel. An external charger is used for recharging the battery and supplying power to the phone. The charger is a ”performance travel charger” (Nokia ACP–9) that can deliver supply current up to 850 mA . It is also possible to use a standard travel charger (Nokia ACP–7). The ACP–7 delivers only 400 mA which is too little for charging the battery during a call.

The baseband contains components that control power distribution to the CMT parts excluding those that use continuous battery supply. The battery feeds power directly to three CMT parts of the system: CCONT, power amplifier, and CMT UI. The figure above is the block diagram of the power distribution.

The charging control ASIC called CHAPS provides protection against overvoltages, charger failures and pirate chargers etc. that would otherwise cause damage to the phone.

Battery identification

Battery types are identified by a pulldown resistor inside the battery pack. The MCU can identify the battery by reading the BSI line DC–voltage level with a CCONT A/D converter.

Also the PDA needs to know whether the battery is connected or not. The BSI line inside transceiver has a 180k pullup to PDA system voltage, VSYS. CMOS switch (D100) is added between VSYS powered and VBB powered circuits for preventing leakage current.

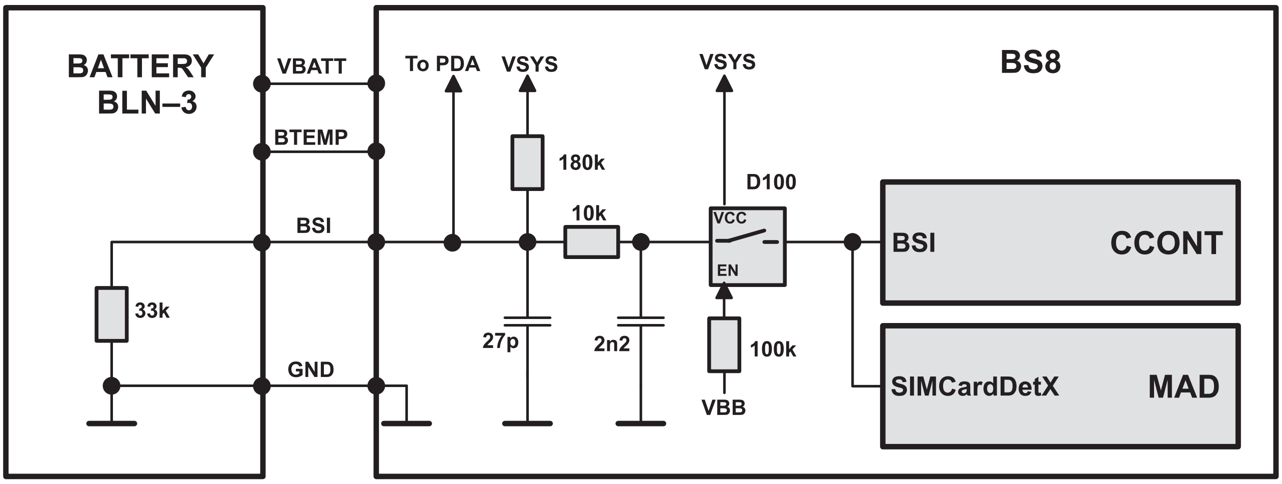


Figure 10. BSI connections

The battery identification line is used also for battery removal detection on the CMT side. The BSI line is connected to a SIMCardDetX line of MAD2 (D200). SIMCardDetX is a threshold detector with a nominal input switching level 0.85xVcc for a rising edge and 0.55xVcc for a falling edge. The battery removal detection is used as a trigger to power down the SIM card before the power is lost. The working length of the BSI contact in the battery connector is made 0.5 mm shorter than the supply voltage contacts so that there is a delay between battery removal detection and supply power off.

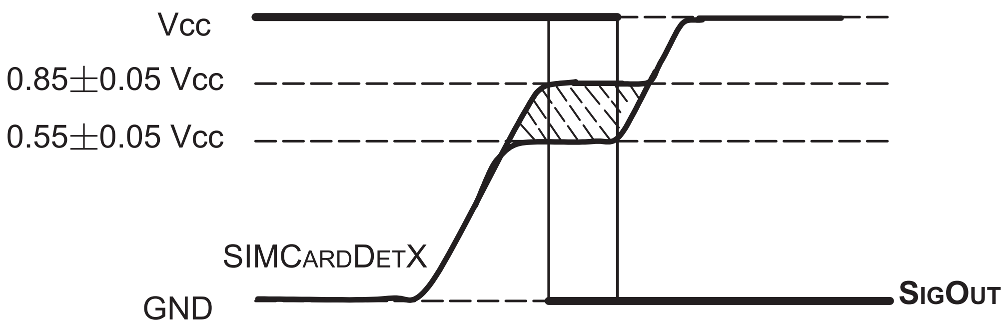


Figure 11. SIMCardDetX detection levels

Battery charging

The electrical specifications define the idle voltages generated by the acceptable chargers at the DC connector input. The absolute maximum input voltage is 30V due to the transient suppressor that is protecting the charger input. At the phone end there is no difference between a plug–in charger or a desktop charger. The DC–jack pins and bottom connector charging pads are connected together inside the phone. Charging block diagram is below.

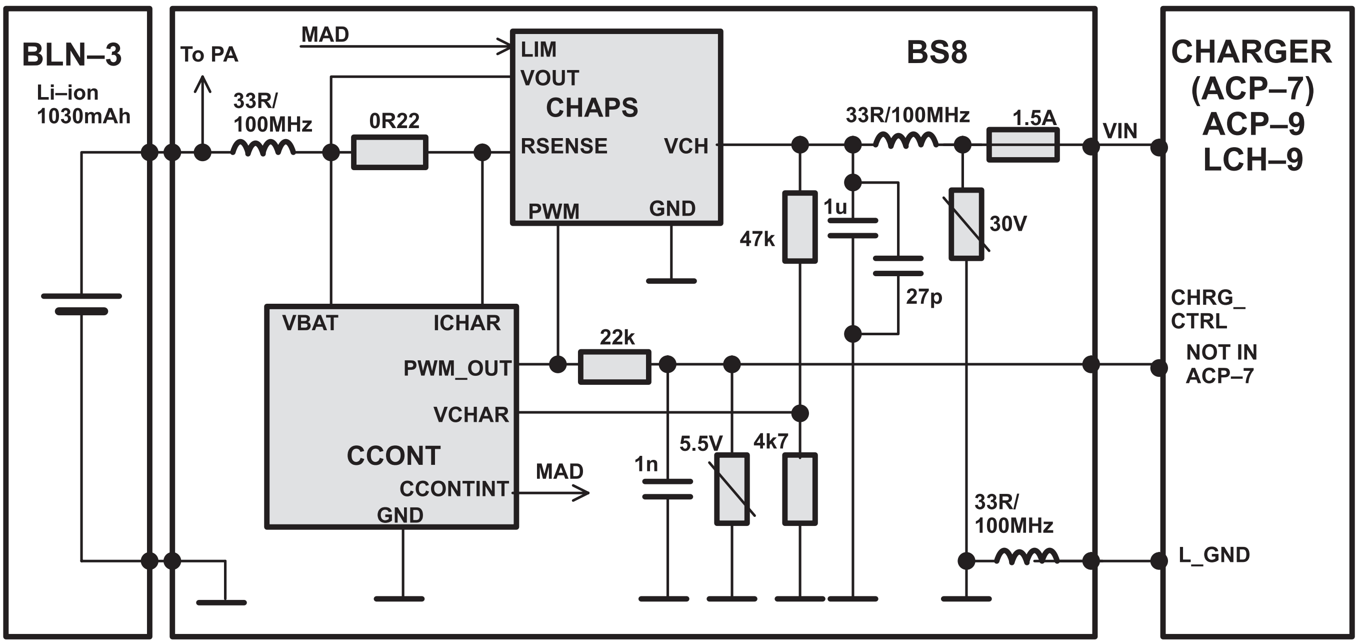


Figure 12. Charging block diagram

Startup charging

When a charger is connected, the CHAPS is supplying a startup current minimum of 130mA to the phone. The startup current provides initial charging to a phone with an empty battery. The startup circuit charges the battery until the battery voltage level 3.0V (+/– 0.1V) is reached. Then the CCONT releases the PURX reset signal and the program execution starts. The charging mode is changed from startup charging to PWM charging that is controlled by the MCU software. If the battery voltage reaches 3.55V (3.75V maximum) before the program has taken control over the charging, the startup current is switched off. The startup current is switched on again when the battery voltage has sunk to 100mV (nominal).

Table 8. Startup characteristics

Parameter	Symbol	Min	Typ	Max	Unit
VOUT Start– up mode cutoff limit	Vstart	3.45	3.55	3.75	V
VOUT Start– up mode hysteresis NOTE: Cout = 4.7 uF	Vstarthys	80	100	200	mV
Start–up regulator output current VOUT = 0V ... Vstart	Istart	130	165	200	mA

Battery overvoltage protection

Output overvoltage protection is used to protect the phone from damage. The power switch is immediately turned OFF if the voltage in VOUT rises above VLIM1.

Table 9. VLIM characteristics

Parameter	Symbol	LIM input	Min	Typ	Max	Unit
Output voltage cutoff limit	VLIM1	LOW	4.4	4.6	4.8	V

When the switch in output overvoltage situation has once turned OFF, it stays OFF until the the battery voltage falls below VLIM1 and PWM = LOW is detected. The switch can be turned on again by setting PWM = HIGH.

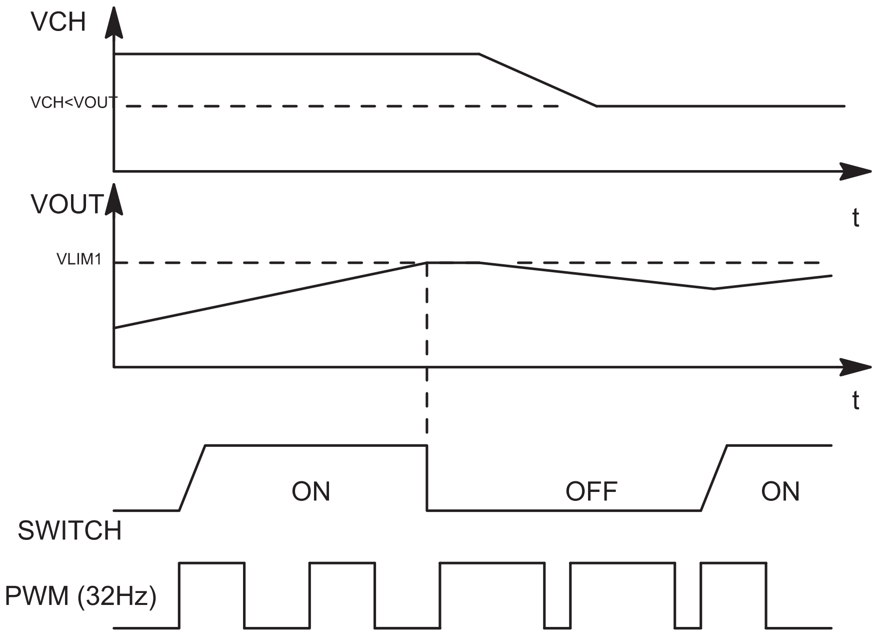


Figure 13. Output overvoltage protection(in principle; not in timescale)

Battery removal during charging

Output overvoltage protection is also needed in case the main battery is removed when charger connected or charger is connected before the battery is connected to the phone.

If the battery is removed during charging, the SIMCardDetX signal goes active and the SIMCard is driven down.

PWM control

The ACP–9 is controlled with PWM at a frequency of 32Hz. When the PWM rate is 32Hz CHAPS keeps the power switch continuously in the ON state.

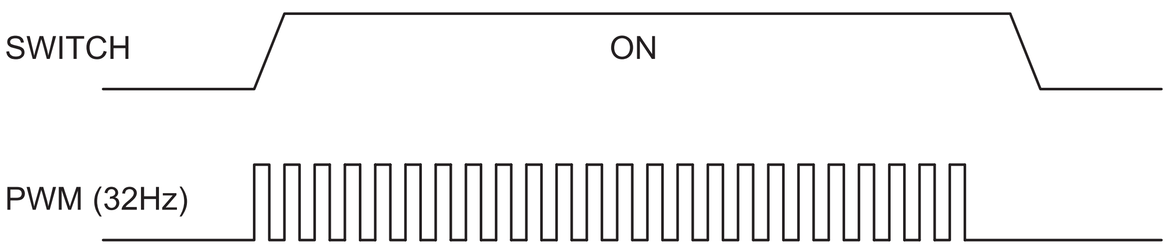


Figure 14. Switch control with 32 Hz frequency (in this case 50% duty cycle)

Battery temperature

The battery temperature is measured with a NTC inside the battery pack (see table 12). The BTEMP line in the transceiver has a 100k pull–up to the VREF. The MCU calculates the battery temperature by reading the BTEMP line DC–voltage level with a CCONT A/D–converter.

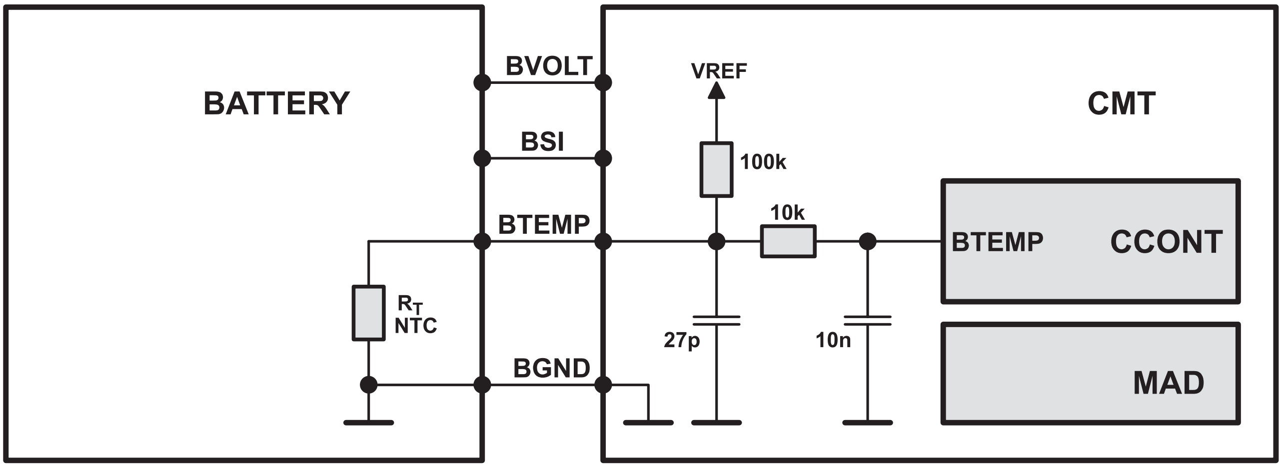


Figure 15. Standard battery BTEMP connection

Based on 47kΩ ± 5 % NTC with B = 4090 ±1.5 %. Without any alignment, with that and 1 % pull–up resistor, ± 2.5 °C accuracy is achieved between – 20 and +60 °C (± 3.5 °C @ –40 ... +85 °C).

Table 10. Battery temperature vs. AD readings and NTC resistance

T [°C]	AD	R [kΩ]	T [°C]	AD	R [kΩ]	T [°C]	AD	R [kΩ]
–40	963	1589	5	560	120.9	50	145	16.53
–35	942	1151	10	497	94.53	55	122	13.63
–30	915	842.8	15	436	74.40	60	103	11.30
–25	882	622.6	20	379	58.95	65	88	9.404
–20	842	464.1	25	327	47.00	70	74	7.865
–15	795	349.0	30	280	37.71	75	63	6.607
–10	743	264.6	35	238	30.43	80	54	5.573
–5	685	202.3	40	202	24.70	85	46	4.721
0	623	155.8	45	171	20.15	90	39	4.015

NOTE: NTC R values and corresponding AD values are calculated values. Because of tolerances real values may differ from the calculated values.

Supply voltage regulators

The heart of the CMT power distribution is the CCONT. It includes all the voltage regulators and feeds power to the whole system. The baseband digital parts are powered from the VBB regulator which provides 2.8V baseband supply. The baseband regulator is active always when the phone is powered on. The VBB baseband regulator feeds the MAD and memories, the COBBA digital parts and the LCD driver in the UI section. There is a separate regulator for the SIM card. The regulator is selectable between 3V and 5V and controlled by the SIMPwr line from MAD to CCONT. The COBBA analog parts are powered from a dedicated 2.8V supply VCOBBA. The CCONT supplies also 5V for RF and for flash VPP.

Table 11. Regulator activity in different operating modes

Operating mode	Vref	RF REG	VCOBBA	VBB	VSIM	SIMIF
Power off	Off	Off	Off	Off	Off	Pull down
Power on	On	On/Off	On	On	On	On/Off
Reset	On	Off VR1 On	On	On	Off	Pull down
Sleep	On	Off	Off	On	On	On/Off

NOTE: The COBBA regulator is off in SLEEP mode. Its output pin may be fed from V_{BB} in SLEEP mode by setting bit RFReg(5) to ’1’ (default).

CCONT includes also five additional 2.8V regulators providing power to the RF section. These regulators are controlled either by the direct control signals from the MAD or by the RF regulator control register in the CCONT which the MAD updates. Below are the listed the MAD control lines and the regulators they are controlling.

– TxPwr controls VTX regulator (VR5)

– RxPwr controls VRX regulator (VR2)

– SynthPwr controls VSYN_1 and VSYN_2 regulators (VR4 and VR3)

– VCXOPwr controls VXO regulator (VR1)

The CCONT generates also a 1.5 V reference voltage VREF to the COBBA, SUMMA and CRFU. The VREF voltage is also used as a reference to some of the CCONT A/D converters.

In addition to the above mentioned signals, the MAD includes also a TXP control signal to the SUMMA power control block and to the power amplifier. The transmitter power control TXC is led from the COBBA to the SUMMA.

NOTE 1:   Characteristics above are NOT valid if Vbat < 3.0V.
NOTE 2:   Line regulation is 20dB for f<100kHz when battery voltage is lower than 3.1V.

MAD core regulator

This block includes a linear voltage regulator with programmable output voltage, which supplies the MAD core. The output voltage can be changed from typical 1.30 V to 2.65 V in 225mV steps. The default output voltage is 1.975V. Control is possible via control register CVReg; the details are available in the digital specification of CCONT ASIC. If the regulator is not used, the control must be set to ’0’, and the output left floating.

The lower core voltage is used only with MAD c07 technology in near future. There are two jumper resistors (R151 and R152, see the BS8 schematics) in baseband for selecting between normal or lower MAD core voltage.

Switched mode supply VSIM

There is a switched mode supply for SIM–interface. SIM voltage is selected via serial IO. The 5V SMR can be switched on independently of the SIM voltage selection, but can't be switched off when the VSIM voltage value is set to 5V.

In the next figure the principle of the SMR / VSIM–functions is shown.

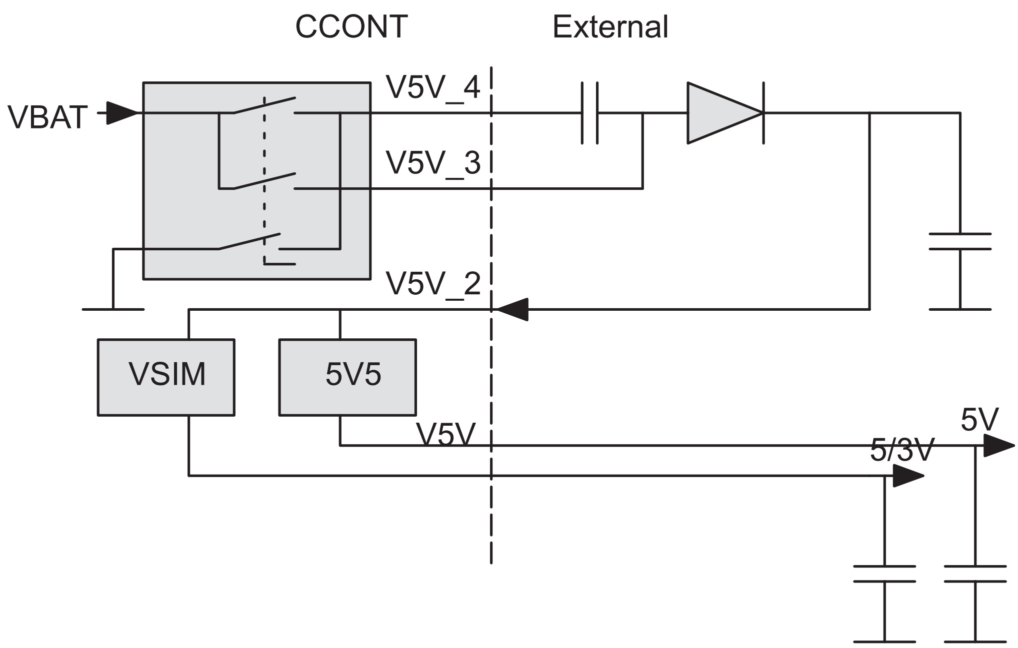


Figure 16. Principle of the SMR power functions

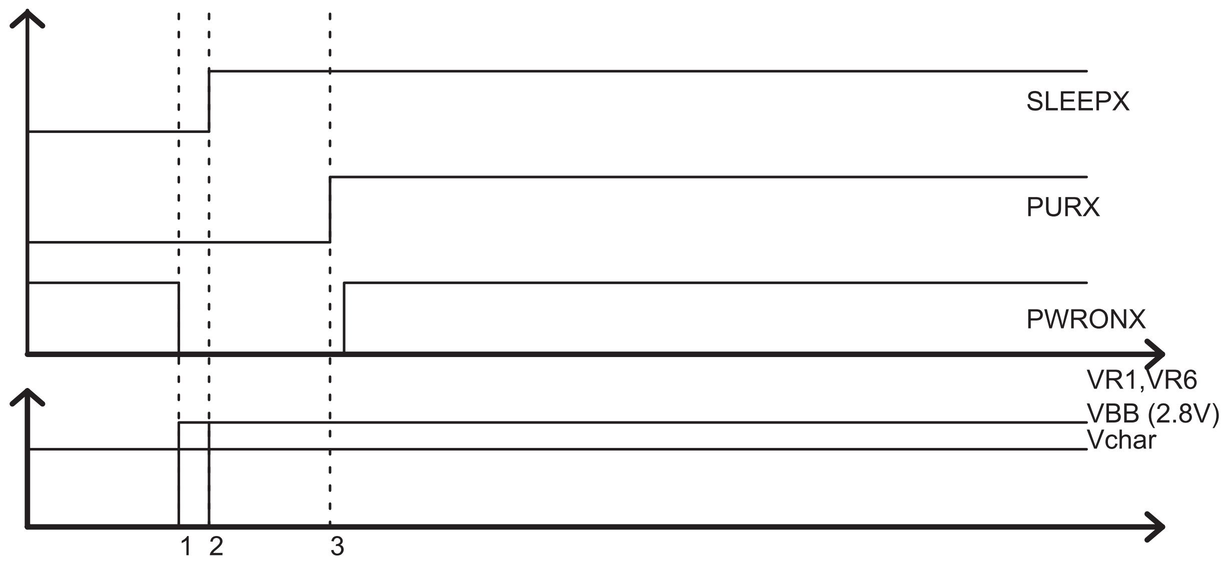
Power up

The baseband is powered up by:

1. Pressing the power key
2. Connecting a charger to the phone.
3. PDA can power BB to SRS by pulling PWRONx line to low state.

Power up with power switch (PWRKEYx)

When the power on switch is pressed, the PWRKEYx signal goes low and pulls the CCONT PWRONx pin to low. The CCONT then switches on the CCONT digital section and the VCXO as was the case with the charger driven power up. If the PWRONX is low when the 62 ms delay expires, the PURX is released and the SLEEPX control goes to MAD. If the PWRONX is not low when 62 ms expires, the PURX will not be released, and CCONT will go to power off (digital section will send power off signal to analog parts).



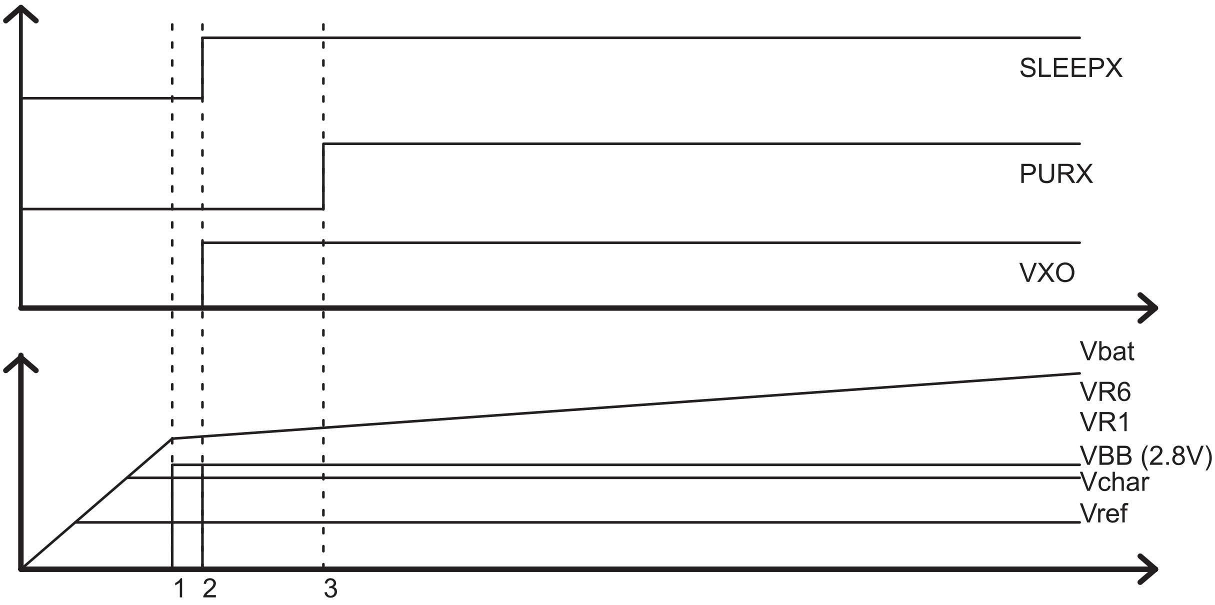
1:Power switch pressed ==> Digital voltages on in CCONT (VBB)
2: CCONT digital reset released. VCXO turned on
3: 62 ms delay to see if power switch is still pressed.

Figure 17. Power up with switch

Power up with a charger

When the charger is connected, the CCONT switches on the CCONT digital voltage as soon as the battery voltage exceeds 3.0V. The reset for the CCONT's digital parts is released when the operating voltage is stabilized (50 us from switching on the voltages). The operating voltage for the VCXO is also switched on. The counter in the CCONT digital section keeps the MAD in reset for 62 ms (PURX) to make sure that the clock provided by VCXO is stable. After this delay the MAD reset is released, and the VCXO –control (SLEEPX) is given to the MAD. The CMT start to so called acting dead–state which means that only the charging software is running and e.g. the RF is powered off.

The next diagram describes the power on procedure with charger (the picture assumes empty battery, but the situation would be the same with full battery):



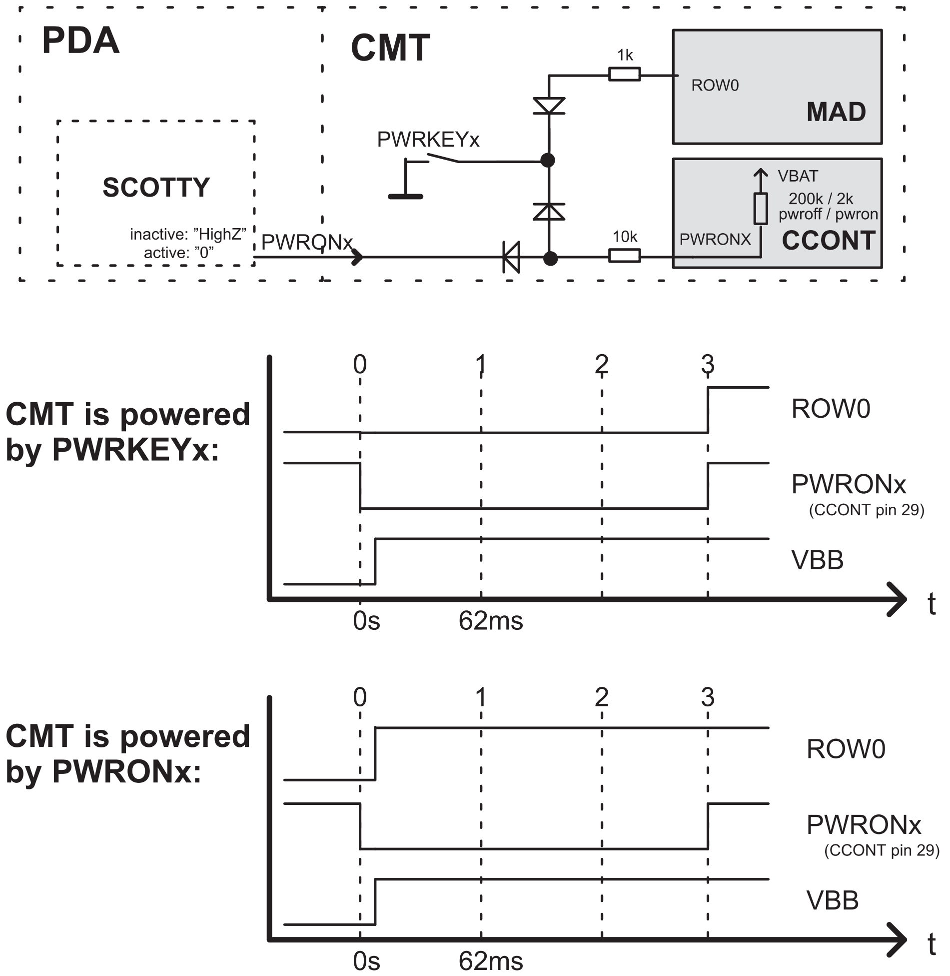
1: Battery voltage over 3.0==>Digital voltages to CCONT (VBB)
2: CCONT digital reset released. VCXO turned on
3: 62ms delay before PURX released

Figure 18. Power up with charger

Service Request State (SRS)

If CMT is powered off, the PDA has a possibility to startup the CMT to SERVICE REQUEST (SRS) state by using PWRONx line. The PDA can do it by pulling the PWRONx line to the low (”0”) state. The difference between the SRS and acting dead is that the SRS is invisible to the user. Also during the SRS the RF parts are always powered off.

The SRS is needed when the PDA is going to communicate with the CMT (e.g. asking some SIM information or battery voltage information) when the CMT is powered off.



0: –CCONT PWRONx input goes to ”0”. CCONT start power on sequency and releases BB regulator (VBB → 2.8V).

1: –When PWRONx has been ”0” at least 62ms, CCONT gives system control to MAD. MAD start execute MCU SW.

2: –MCU SW read the state of the ROW0 signal.
– If it is ”1” MCU SW go to SRS
– If it is ”0” MCU SW continues to active state.

3: –Power on/off key or PWRONx are released.

Figure 19. SRS versus normal powerup.

Active Mode

In the active mode the phone is in normal operation, scanning for channels, listening to a base station, transmitting and processing information. All the CCONT regulators are operating. There are several sub–states in the active mode depending on if the phone is in burst reception, burst transmission, if DSP is working etc..

Sleep Mode

In the sleep mode all the regulators except the baseband VBB and the SIM card VSIM regulators are off. Sleep mode is activated by the MAD after MCU and DSP clocks have been switched off. The voltage regulators for the RF section are switched off and the VCXO power control, VCXOPwr is set low. In this state only the 32 kHz sleep clock oscillator in CCONT is running. The flash memory power down input is connected to the ExtSysResetX signal, and the flash is deep powered down during the sleep mode.

The sleep mode is exited either by the expiration of a sleep clock counter in the MAD or by some external interrupt, generated by a charger connection, key press, headset connection etc. The MAD starts the wake up sequence and sets the VCXOPwr and ExtSysResetX control high. After VCXO settling time other regulators and clocks are enabled for active mode.

If the battery pack is disconnected during the sleep mode, the CCONT pulls the SIM interface lines low as there is no time to wake up the MCU.

Charging

Charging can be performed in any operating mode. The battery type is indicated by a resistor inside the battery pack. The resistor value corresponds to a specific battery capacity which is defined in the RAE–2 to 1030mAh.

The battery voltage, temperature, size and current are measured by the CCONT controlled by the charging software running in the MAD.

The power management circuitry controls the charging current delivered from the charger to the battery. Charging is controlled with a PWM input signal, generated by the CCONT. The PWM pulse width is controlled by the MAD and sent to the CCONT through a serial data bus. The battery voltage rise is limited by turning the CHAPS switch off when the battery voltage has reached 4.1V (Li–Ion). Charging current is monitored by measuring the voltage drop across a 220mohm resistor.

Power Off

The baseband is powered down by:

1. Pressing the power key, that is monitored by the MAD, which starts the power down procedure.
2. If the battery voltage is dropped below the operation limit, either by not charging it or by removing the battery.
3. Letting the CCONT watchdog expire, which switches off all CCONT regulators and the phone is powered down.

The power down is controlled by the MAD. When the power key has been pressed long enough or the battery voltage is dropped below the limit, the MCU initiates a power down procedure and disconnects the SIM power. Then the MCU outputs a system reset signal and resets the DSP. If there is no charger connected, the MCU writes a short delay to CCONT watchdog and resets itself. After the set delay the CCONT watchdog expires, which activates the PURX and all regulators are switched off and the phone is powered down by the CCONT.

If a charger is connected when the power key is pressed the phone enters into the acting dead mode.

Watchdog

The Watchdog block inside the CCONT contains a watchdog counter and some additional logic which are used for controlling the power on and power off procedures of CCONT. Watchdog output is disabled when WDDisX pin is tied low. The WD-counter runs during that time, though. Watchdog counter is reset internally to 32s at power up. Normally it is reset by the MAD writing a control word to the WDReg.

Audio control

The audio control and processing is controlled by the COBBA–GJ ASIC, which contains the audio and rf codecs, and the MAD2, which contains the MCU, ASIC and DSP blocks handling and processing the audio signals. The RAE–2 audio block diagram is presented in the figure next page.

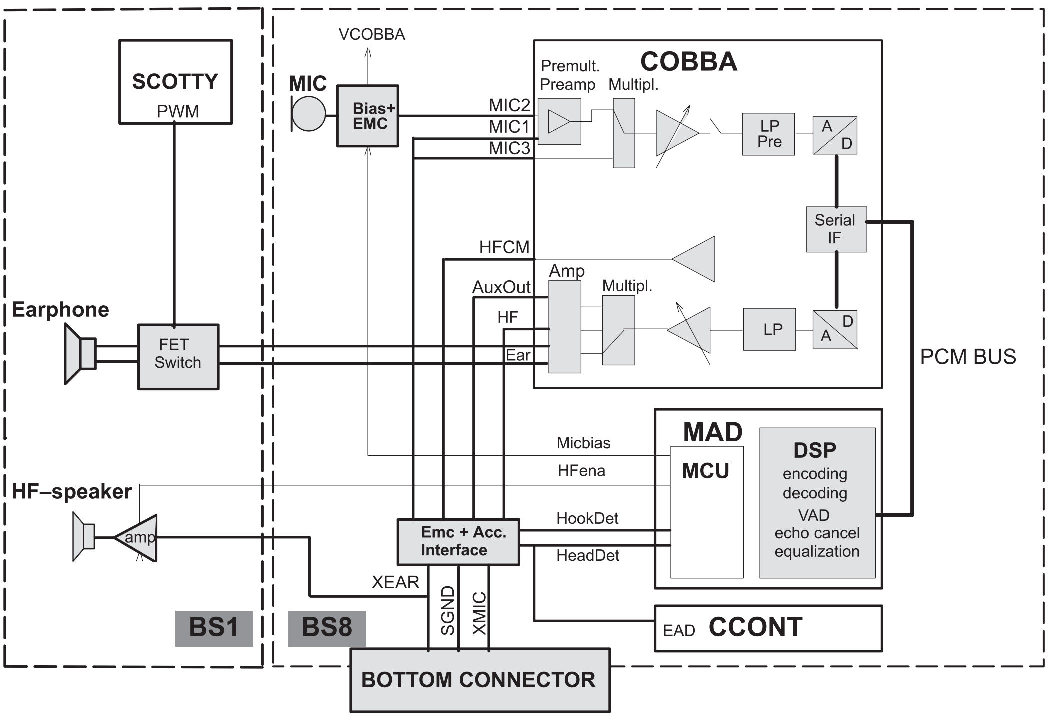


Figure 20. RAE–2 audio block diagram

The baseband supports three microphone inputs and two earphone outputs. The inputs can be taken from an internal microphone, a headset microphone or from an external microphone signal source. The microphone signals from different sources are connected to separate inputs at the COBBA–GJ. Inputs for the microphone signals are differential type.

The MIC3 input is used for a headset microphone that can be connected directly to the system connector. The internal microphone is connected to the MIC2 input and an external pre–amplified microphone (handset/ handsfree) signal is connected to the MIC1 input. In the COBBA there are also three audio signal outputs of which dual ended EAR lines are used for internal earpiece and HF line for accessory audio output. The third audio output AUXOUT is used only for bias supply to the headset microphone.

When the lid is open the downlink audios can be routed to the internal HF amplifier. This amplifier and the HF speaker are located on the PDA module. The MAD is able to enable the HF amplifier with an HFena–signal. The internal microphone acts as a handsfree microphone during a HF call. The microphone signal level is amplified more during an HF call than a normal call.

PDA Tones

The PDA keyclicks and warning tones are played via the earphone. There is an external paraller FET switch circuit with earphone located on the PDA module. The PWM output of the PDA processor is connected to this circuit and thus the PDA is able to play tones via the earphone.

CMT Alert Signal Generation

A HF speaker is used for giving alert tones and/or melodies as a signal of an incoming call. The alert signals are routed to the XEAR line by the DSP. Keypress and user function response beeps are generated with the earphone.

External audio connections

The external audio connections are presented in the next figure. A headset can be connected directly to the system connector. The headset microphone bias is supplied from the COBBA AUXOUT output and fed to the microphone through the XMIC line. The 330ohm resistor from the SGND line to the AGND provides a return path for the bias current.

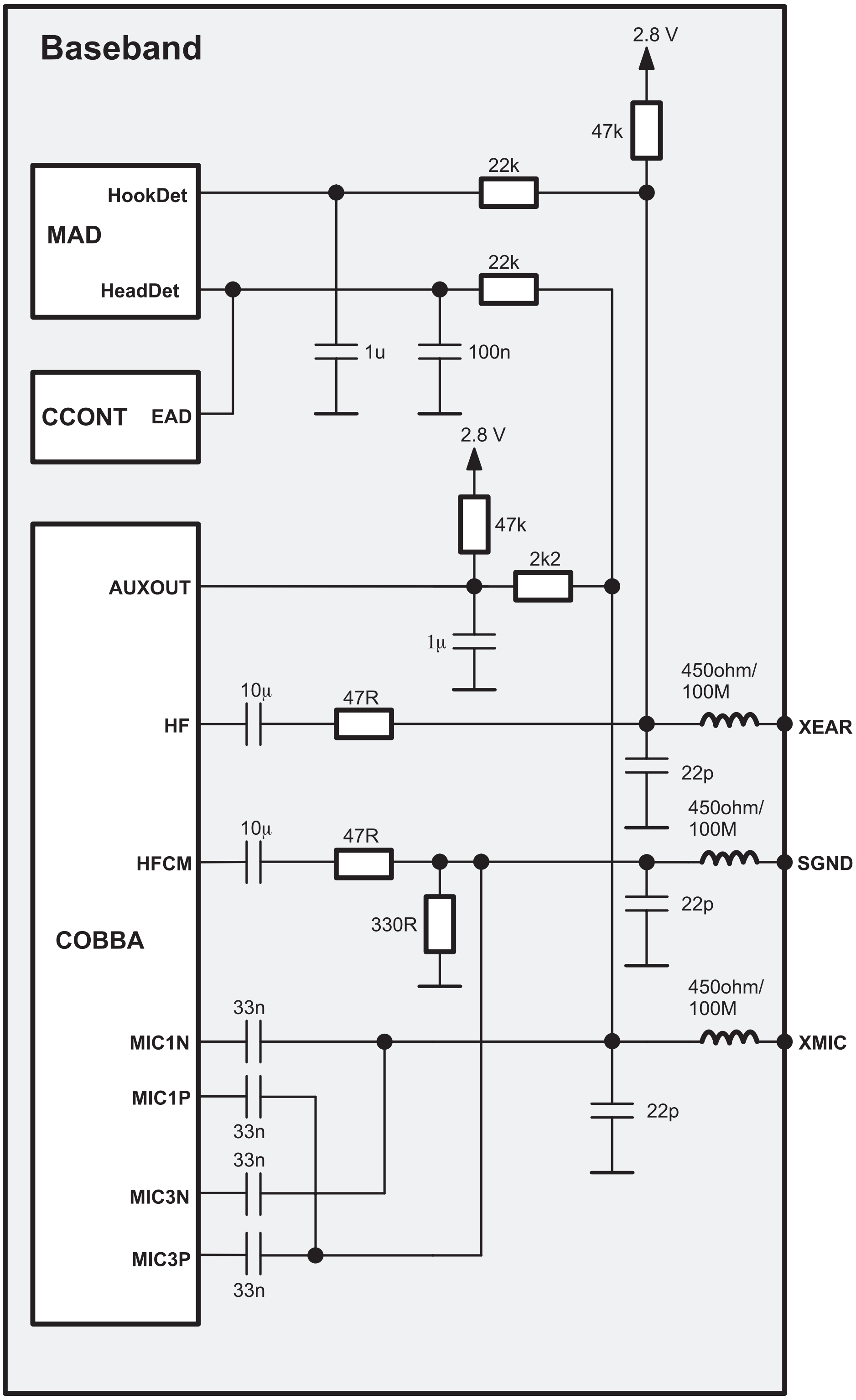


Figure 21. Combined headset and system connector audio signals (Headset can be connected to system connector)

Analog audio accessory detection

The XEAR signal line comprises a 47 kΩ pullup in the transceiver and 10 kΩ pulldown to SGND in the accessory. The XEAR is pulled down when an accessory is connected, and pulled up when disconnected. The XEAR is connected to the HookDet line (in MAD), an interrupt is given due to both connection and disconnection. There is filtering between XEAR and HookDet to prevent audio signal giving unwanted interrupts.

External accessory notices tha powered–up phone by detecting voltage in XMIC line. The table below is a truth table for detection signals.

Table 12. Truth table for HookDet and HeadDet

Accessory connected	HookDet	HeadDet	Notes
No accessory connected	High	High	Pullups in the transceiver
Headset HDC–8 with a button switch pressed	Low	Low	XEAR and XMIC loaded (dc)
Headset HDC–8 with a button switch released	High	Low *)	XEAR unloaded (dc)
Handsfree (HFU–2)	High	High	Detected via MBUS

*) HeadDet (MAD) cannot be used during a call, because of the 1.5V bias from AUX OUT (COBBA)

Headset detection

The external headset device is connected to the system connector, from which the signals are routed to the COBBA headset microphone inputs and earphone outputs. In the XMIC line there is a (47 + 2.2) kΩ pull–up in the transceiver. The microphone is a low resistance pull–down compared to the transceiver pull–up.

When there is no call going, the AUXOUT is in high impedance state and the XMIC is pulled up. When the headset is connected, the XMIC is pulled down. The XMIC is connected to the HeadDet line (in MAD), an interrupt is given due to both connection and disconnection. There is filtering between the XMIC and the HeadDet to prevent audio signal giving unwanted interrupts (when an accessory is connected).

Headset switch detection

The XEAR line comprises a 47 kΩ pull–up in the transceiver. The earphone is a low resistance pull–down compared with the transceiver pull–up. When a remote control switch is open, there is a capacitor in series with the earphone, so the XEAR (and HookDet) is pulled up by the phone. When the switch is closed, the XEAR (and HookDet) is pulled down via the earphone. So both press and release of the button gives an interrupt.

During a call there is a bias voltage (1.5 V) in the AUXOUT, and the HeadDet cannot be used. The headset interrupts should to be disabled during a call and the EAD line (AD converter in CCONT) should be polled to see if the headset is disconnected.

Internal audio connections

The speech coding functions are performed by the DSP in the MAD2 and the coded speech blocks are transferred to the COBBA–GJ for digital to analog conversion, down link direction. In the up link direction the PCM coded speech blocks are read from the COBBA–GJ by the DSP.

There are two separate interfaces between the MAD2 and COBBA–GJ: a parallel bus and a serial bus.

The parallel bus features 12 data bits, 4 address bits, read and write strobes and a data available strobe. The parallel interface is used to transfer all the COBBA–GJ control information (both the RFI part and the audio part) and the transmit and receive samples.

The serial interface between MAD2 and COBBA–GJ includes transmit and receive data, clock and frame synchronization signals. It is used to transfer the PCM samples. The frame synchronization frequency is 8 kHz which indicates the rate of the PCM samples and the clock frequency is 1 MHz. The COBBA generates both clocks.

4–wire PCM serial interface

The interface consists of the following signals:

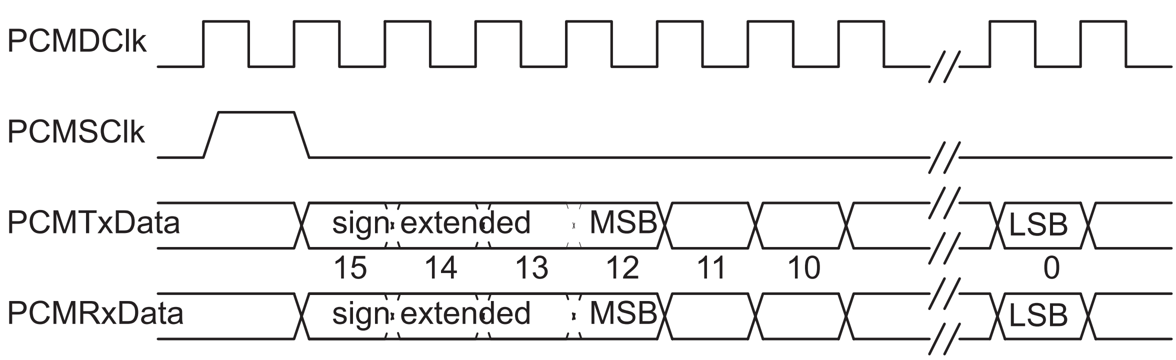
a PCM codec master clock (PCMDClk),

a frame synchronization signal to DSP (PCMSClk),

a codec transmit data line (PCMTX) and

a codec receive data line (PCMRX).

The COBBA–GJ generates the PCMDClk clock, which is supplied to DSP SIO. The COBBA–GJ also generates the PCMSClk signal to DSP by dividing the PCMDClk. The PCMDClk frequency is 1.000 MHz and is generated by dividing the RFIClk 13 MHz by 13. The COBBA–GJ further divides the PCMDClk by 125 to get a PCMSClk signal, 8.0 kHz.



Digital control

All the baseband functions are controlled by the MAD2 ASIC, which consists of a MCU, a system ASIC and a DSP. In addition to the internal RAM/ROM memory, the MAD2 has an external RAM memory and external FLASH and EEPROM type of memories.

MAD2

MAD2 comprises the following building blocks:

- ARM RISC processor with both 16–bit instruction set (THUMB mode) and 32–bit instruction set (ARM mode)
- TI Lead DSP core with peripherals:
  - API (Arm Port Interface memory) for MCU–DSP communication, DSP code download, MCU interrupt handling vectors (in DSP RAM) and DSP booting
  - Serial port (connection to PCM)
  - Timer
  - DSP memory (80 kW RAM in PD version of MAD2)
- BUSC (BusController for controlling accesses from ARM to API, System Logic and MCU external memories, both 8– and 16–bit memories)
- System Logic
  - CTSI (Clock, Timing, Sleep and Interrupt control)
  - MCUIF (Interface to ARM via BUSC). Contains MCU BootROM
  - DSPIF (Interface to DSP)
  - MFI (Interface to COBBA AD/DA Converters)
  - CODER (Block encoding/decoding and A51&A52 ciphering)
  - AccIF(Accessory Interface)
  - SCU (Synthesizer Control Unit for controlling 2 separate synthesizer)
  - UIF (Keyboard interface, serial control interface for COBBA PCM Codec, LCD Driver and CCONT)
  - SIMI (SimCard interface with enhanced features)
  - PUP (Parallel IO, USART and PWM control unit for vibra and buzzer)

The MAD2 operates from a 13 MHz system clock, which is generated from the 13MHz VCXO frequency. The MAD2 supplies a 6,5MHz or a

13MHz internal clock for the MCU and system logic blocks and a 13MHz clock for the DSP, where it is multiplied to 45.5MHz DSP clock. The system clock can be stopped for a system sleep mode by disabling the VCXO supply power from the CCONT regulator output. The CCONT provides a 32kHz sleep clock for internal use and to the MAD2, which is used for the sleep mode timing. The sleep clock is active when there is a battery voltage available i.e. always when the battery is connected.

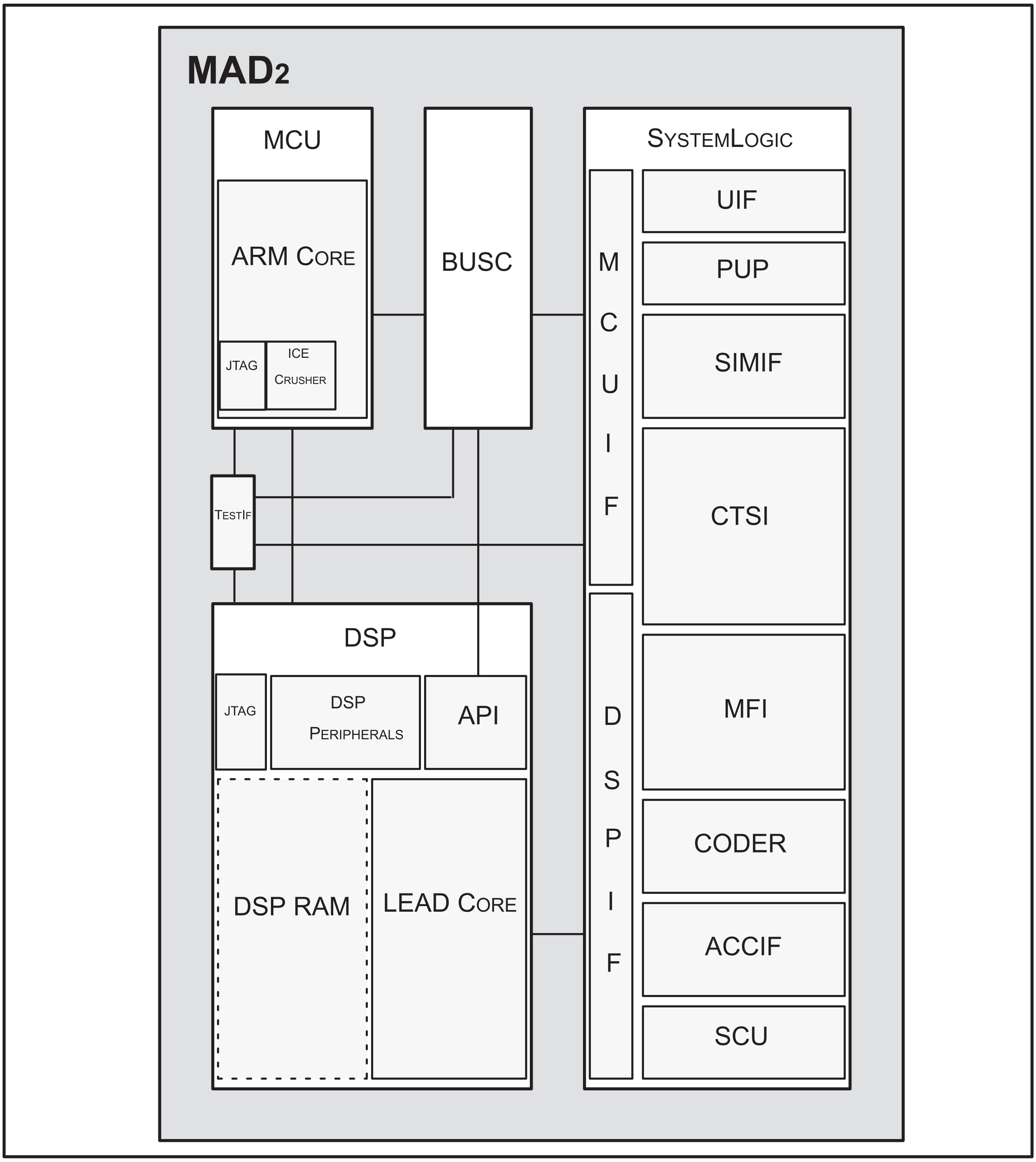


Figure 22. MAD2 ARCHITECTURE

MAD2 memory configuration

MAD2 contains 12 kb RAM memory, 68 kb ROM memory. Memory is divided as follows

– Data:	10 kb DARAM 16 kb DROM	2 kb API RAM
– Program:	48 kb PROM	
– Program/Data:	4 kb PDROM	

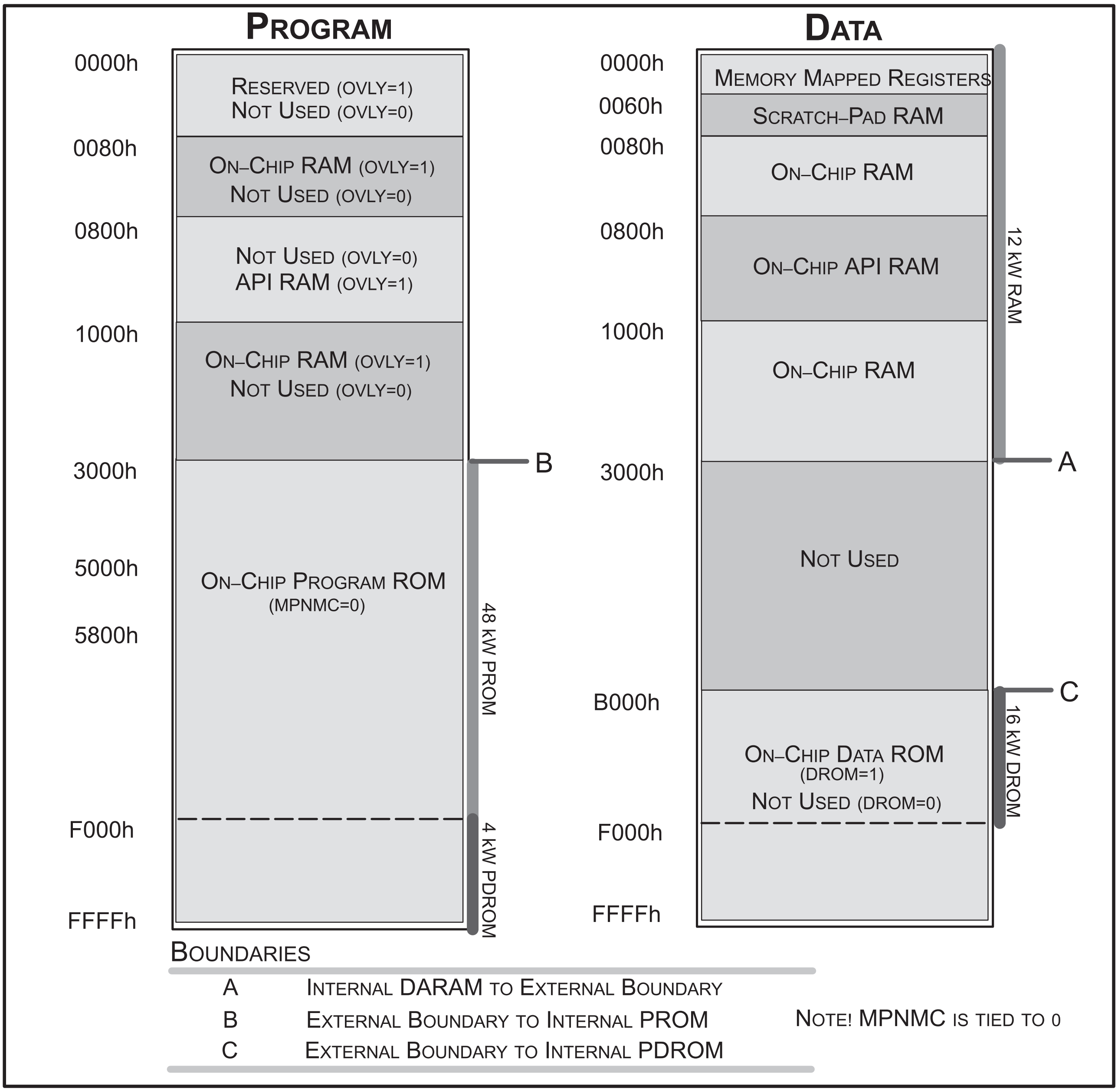


Figure 23. MAD2 12/68 DSP MEMORY MAP

MCU Memory Map

The MAD2 supports a maximum of 4GB internal and 4MB external address space. The external memories use address lines MCUAd0 to MCUAd21 and 8–bit/16–bit databus. The BUSC bus controller supports 8– and 16–bit access for byte, double byte, word and double word data. Access wait states (0, 1 or 2) and used databus width can be selected separately for each memory block.

Table 13. MCU Memory map

Memory block	Chip select	Start address	Stop address	Size	Size
boot ROM (*)	internal	0000 0000	0000 FFFF	64k	64k
API RAM	internal	0001 0000	0001 FFFF	64k	64k
System logic	internal	0002 0000	0002 FFFF	64k	64k
API ctl reg.	internal	0003 0000	0003 FFFF	64k	64k
Bus Controller	Internal	0004 0000	0007 FFFF	256k	256k
The same as 0–7FFFF		0008 0000	000F FFFF	512 k	512 k
ext. RAM (*)	RAMSelX	0010 0000	001F FFFF	1M	1M
ext. ROM1	ROM1SelX	0020 0000	005F FFFF	4M	4M
ext. ROM2 (*)	ROM2SelX	0060 0000	009F FFFF	4M	4M
ext. EEPROM	EEPROMSelX	00A0 0000	00DF FFFF	4M	4M
reserved		00E0 0000	00FF FFFF	4M	4M
The same as 0–FF FFFF		0100 0000	FFFF FFFF	4G – 16 M	4G – 16 M

(*) After reset and when BootROMDis and ROM2Boot are low.

MCU can boot from different memory locations, depending on hardware (GenSDIO0) and software settings.

Table 14. MCU boot memory selection

Start address	Stop address	BootROMDis=0 ROM2Boot=0	BootROMDis=1 ROM2Boot=0	BootROMDis=0 ROM2Boot=1	BootROMDis=1 ROM2Boot=1
0000 0000	0000 FFFF	boot ROM	External RAM	ext. ROM2	External RAM

Memories

The BusController (BUSC) section in the MAD decodes the chip select signals for the external memory devices and the system logic. The BUSC controls the internal and external bus drivers and multiplexers connected to the MCU data bus. The MCU address space is divided into access areas with separate chip select signals. The BUSC supports a programmable number of wait states for each memory range.

The minimum access time for all external memories is specified to 120ns.

Program Memory

The MCU program code resides in the program memory. The program memory size is 8Mbits (512kx16bit) and package is uBGA48.

The flash memory has a power down pin that is kept low during the power up phase of the flash to ensure that the device is powered up in the correct state, read only. The power down pin is utilized in the system sleep mode by connecting the ExtSysResetX to the flash power down pin to minimize the flash power consumption during the sleep.

SRAM Memory

The work memory is a static ram of size 2Mbits (256kx8bit) in a shrink TSOP32 package. The work memory is supplied from the common baseband VBB voltage and the memory contents are lost when the baseband voltage is switched off. All retainable data is stored into the EEPROM (or flash) when the phone is powered down.

EEPROM Memory

An EEPROM is used for a nonvolatile data memory to store the tuning parameters and phone setup information. The short code memory for storing user defined information is also implemented in the EEPROM. The EEPROM size is 8kbytes and the default package is SO8. The memory is accessed through a serial bus including also write protection signal for protecting EEPROM content against any malfunctions.

Flash Programming

RAE–2 Flashing connections

the RAE–2 has two entities which can be programmed: PDA and CMT. There are four different interfaces from outside to the RAE–2 which can be used to transmit software code to the RAE–2. These interfaces are the following:

– JTAG	(PDA flashing only)
– MMC	(PDA flashing only)
– FBUS/MBUS	(PDA and/or CMT flashing)

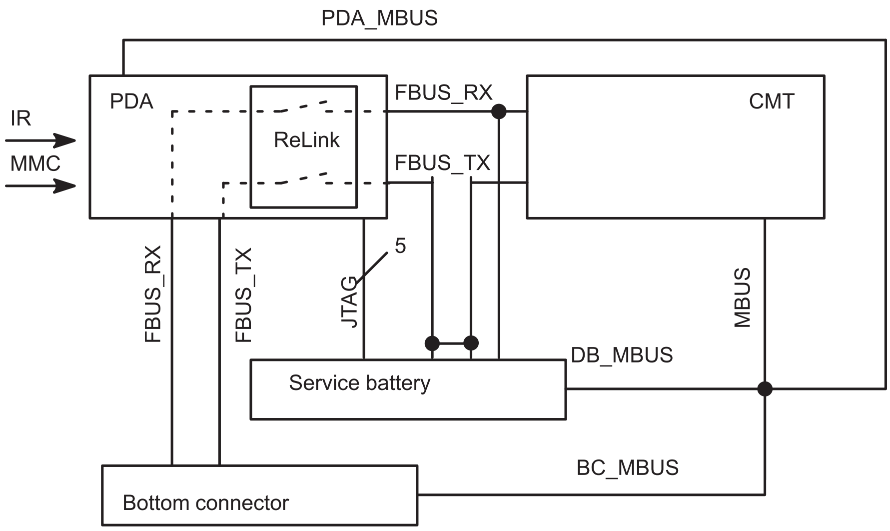


Figure 24. SPOCK's flashing connections

Flashing methods

During external CMT programming only the FBUS and MBUS is used for transmitting software data. The data transmission is done in DCT3 way. This means that the data is transmitted through the FBUS synchronously. The clock signal is transmitted on the MBUS line. Since the FBUS does not go directly to the CMT (as in DCT3 phone) the PDA has to be driven to ReLink mode before the external CMT programming. In order to boot the PDA to Relink mode Testmode connection has to established. This is done inside the Service battery.

The relink causes changes to the DCT3 type power–up procedure during programming. This is because if the RAE–2's VBAT is turned off and on, the PDA will lose the Relink mode. In order to prevent this the CMT is started by using IBI pulse.

In the DCT3 type the CMT programming bootstrap code is used for starting SW downloading. The bootstrap code resides in the small internal ROM of the MAD. The bootstrap code is a small part of the download code and is used only for downloading more code into the RAM.

Data on CMT Flash is divided on two parts:

– CMT SW code
– PPM

The idea is that first the CMT SW code is programmed and after that the PPM is programmed in same method. This allows the change of language without changing the software code.

Flashing procedure

The phone is connected to the flash loading adapter FLA–7 so that supply voltage for the phone and data transmission lines can be supplied from/to the FLA–7. When the FLA–7 triggers an IBI pulse to the phone, the program execution starts from the BOOT ROM and the MCU investigates in the early start–up sequence if the flash prommer is connected. This is done by checking the status of the MBUS–line. Normally this line is high but when the flash prommer is connected the line is forced low by the prommer.

The flash prommer serial data receive line is in receive mode waiting for an acknowledgement from the phone. The data transmit line from the baseband to the prommer is initially high. When the baseband has recognized the flash prommer, the TX–line is pulled low. This acknowledgement is used to start to toggle MBUS (FCLK) line three times in order that MAD2 gets initialized. This must be happened within 15 ms after TX line is pulled low. After that the data transfer of the first two bytes from the flash prommer to the baseband on the RX–line must be done within 1 ms.

When the MAD2 has received the secondary boot byte count information, it forces TX line high. Now, the secondary boot code must be sent to the phone within 10 ms per 16 bit word (If these timeout values are exceeded, the MCU (MAD2) starts normal code execution from flash). After this, the timing between the phone and the flash prommer is handled with dummy bytes.

A 5V programming voltage is supplied inside the transceiver from the battery voltage with a switch mode regulator (5V/30mA) of the CCONT.

Table 15. Flash programming timing characteristic

Characteristics	Min	Typ	Max	Unit
Time from boot indication to MAD2 initialization sequence			15	ms
Time from MAD2 initialization sequence to byte lenght information			1	ms
Time from byte length information to end of secondary boot code loading.			10 per16 bit word	ms

Security

The phone flash program and IMEI code are software protected using an external security device that is connected between the phone and a PC. The security device uses the phone given IMEI number, the software version number and a 24bit hardware random serial number that is read from the COBBA and calculates a flash authority identification number that is stored into the phone EEPROM.

COBBA–GJ ASIC

The COBBA–GJ ASIC provides an interface between the baseband and the RF–circuitry. The COBBA–GJ performs analogue to digital conversion of the received signal. For transmit path the COBBA_GJ performs digital to analogue conversion of the transmit amplifier power control ramp and the in–phase and quadrature signals. A slow speed digital to analogue converter will provide automatic frequency control (AFC).

The COBBA ASIC is at any time connected to the MAD ASIC with two interfaces, one for transferring tx and rx data between the MAD and COBBA and one for transferring codec rx/tx samples.

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Chapter 3
–Transceiver BS8 –
BS8_RF Block

AMENDMENT RECORD SHEET

Amendment Number	Date	Inserted By	Comments
	02/99		Original

CONTENTS – RF

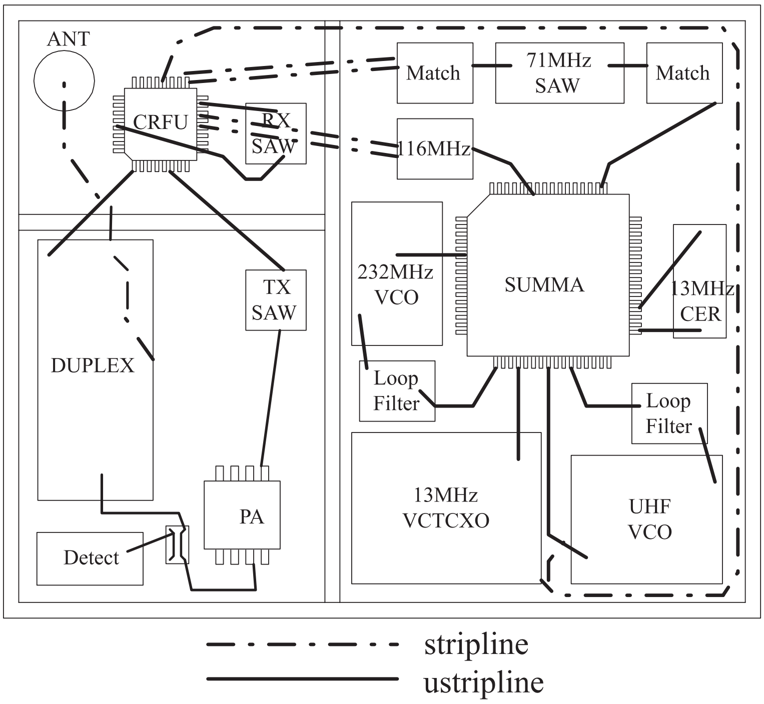
Introduction

This document defines the RF–module of the RAE–2 GSM–”engine”. This section contains electrical specifications, functional descriptions, block diagrams etc.

Technical summary

The RF in the RAE–2 GSM is based on the architecture used in DCT 3.

The RAE–2 RF Engine (figure below) is a single side design, on the A–side, with all components located under the PDA unit. Shielding comprises three shielding cans with removable lids. The maximum building height for the RF Engine is 2 mm.



RF Characteristics

Table 1. Main RF characteristics

Item	Values
Receive frequency range	935 ... 960 MHz
Transmit frequency range	890 ... 915 MHz
Duplex spacing	45 MHz
Channel spacing	200 kHz

Table 1. Main RF characteristics (continued)

Item	Values
Number of RF channels	124
Power class	4
Number of power levels	15

Note 1 : Standard of primary GSM 900 Band, **P – GSM**

890 – 915 MHz : Mobile transmit, Downlink
935 – 960 MHz : Mobile receive, Uplink

Transmitter Characteristics

Item	Values
Type	Upconversion, nonlinear, FDMA/TDMA
Intermediate frequency (phase modulated)	116 MHz
LO frequency range	1006 ... 1031 MHz
Output power	2 W peak (33 dBm)
Power control range	min. 5 ... 33 dBm
Maximum phase error (RMS/peak)	max 5 deg./20 deg. peak

Output power

Parameter	Min.	Typ.	Max.	Unit / Notes
Max. output power		33.0		dBm
Max. output power tolerance (power level 5)			+/– 2.0 +/– 2.5	dB, normal cond. dB, extreme cond.
Output power tolerance / power levels 6...15			+/– 3.0 +/– 4.0	dB, normal cond. dB, extreme cond.
Output power tolerance / power levels 16...19			+/– 5.0 +/– 6.0	dB, normal cond. dB, extreme cond.
Output power control step size	0.5	2.0	3.5	dB

Note 1 : Output power refers to the measure of power when averaged over the useful part of the burst. Power levels are measured at the antenna connector.

Note 2 : Interval between power steps shall be 2 +/–1.5 dB

Receiver characteristics

Item	Values
Type	Linear, FDMA/TDMA
IF frequencies	1st 71 MHz, 2nd 13 MHz
LO frequencies	1st LO 1006 ... 1031 MHz, 2nd LO 58 MHz
Typical 1 dB bandwidth	+/– 90 kHz
Sensitivity	min. – 102 dBm , S/N >8 dB
Total typical receiver voltage gain (from antenna to RX ADC)	73 dB
Receiver output level (RF level –95 dBm)	50 mVpp (typical balanced signal level of 13 MHz IF in RF BB interface = input level to RX ADCs)
Typical AGC range (dynamic range –93dB)	–17 ... +40 dB
Accurate AGC control range	57 dB
Typical AGC step in LNA	–15 dB
Usable input dynamic range	–102 ... –10 dBm
RSSI dynamic range	–110 ... –48 dBm
AGC relative accuracy on channel (accurate range)	+/– 0.8 dB
Compensated gain variation in receiving band	+/– 1.0 dB

DC characteristics

Regulators

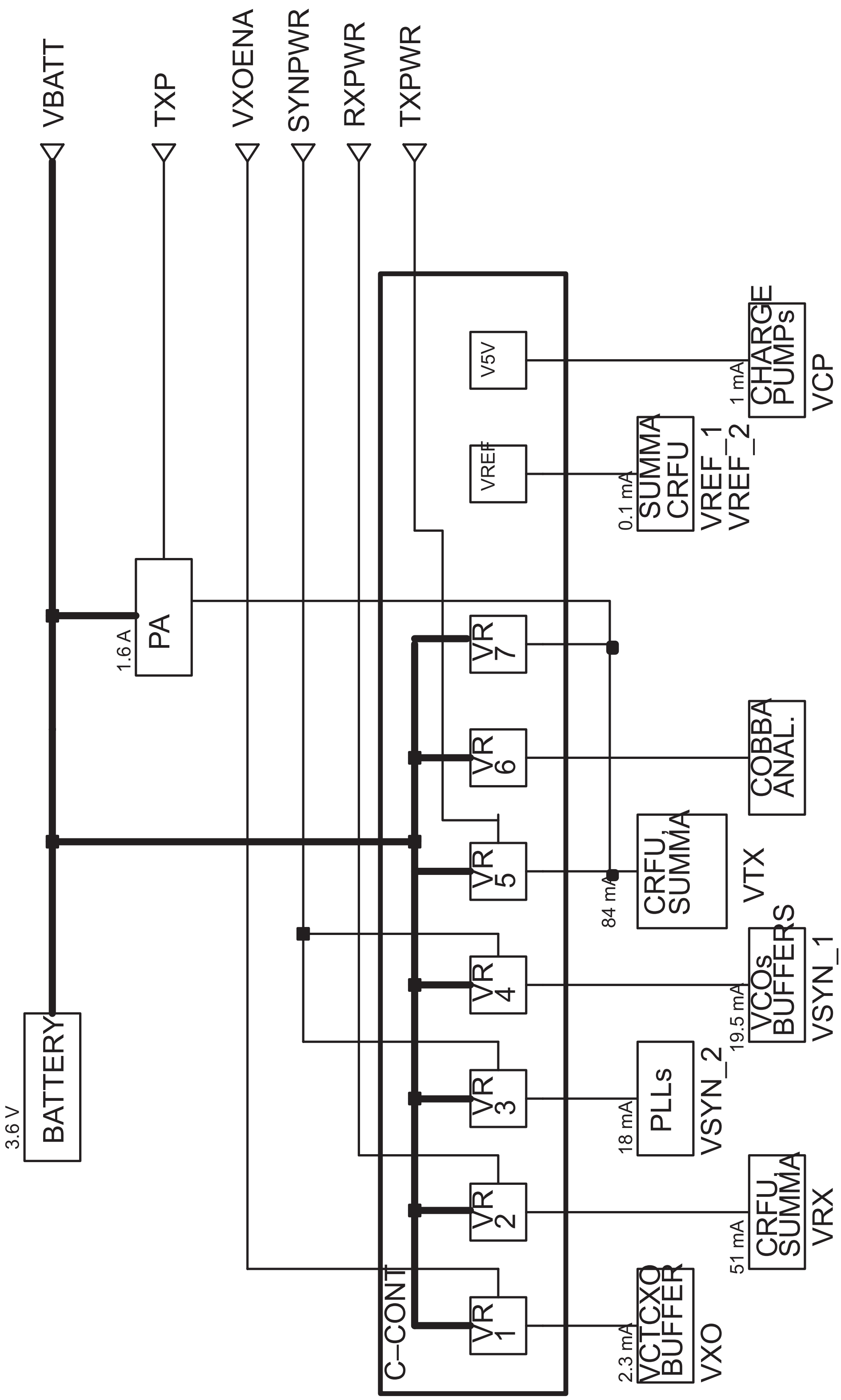
Transceiver has got a multi function power management IC, which contains among other functions, also 7 pcs of 2.8 V regulators. All regulators can be controlled individually with 2.8 V logic directly or through control register. In GSM direct controls are used to get fast switching, because regulators are used to enable RF–functions.

Use of the regulators can be seen in the power distribution diagram.

CCONT also provides 1.5 V reference voltage for SUMMA and CRFU1a (and for DACs and ADCs in COBBA too).

All control signals are coming from MAD and they are 2.8 V logic signals..

Power distribution diagram



Functional descriptions

RF block diagram

The RF block comprises a conventional dual conversion receiver and the transmitter features an up–conversion mixer for the final TX–frequency.

The architecture contains three ICs. Most of the functions are horizontally and vertically integrated. UHF functions except power amplifier and VCO are integrated into CRFU_1a, which is a BiCMOS–circuit suitable for LNA– and mixer–function. Most of the functions are in SUMMA, which also is a BiCMOS–circuit. SUMMA is a IF–circuit including IQ–modulator and PLLs for VHF– and UHF–synthesizers.

Power amplifier is also an ASIC, it is a so called MMIC (monolithic microwave integrated circuit). It has got three amplifier stages including input and interstage matchings. Output matching network is external. Also TX gain control is integrated into this chip.

See block diagram next page

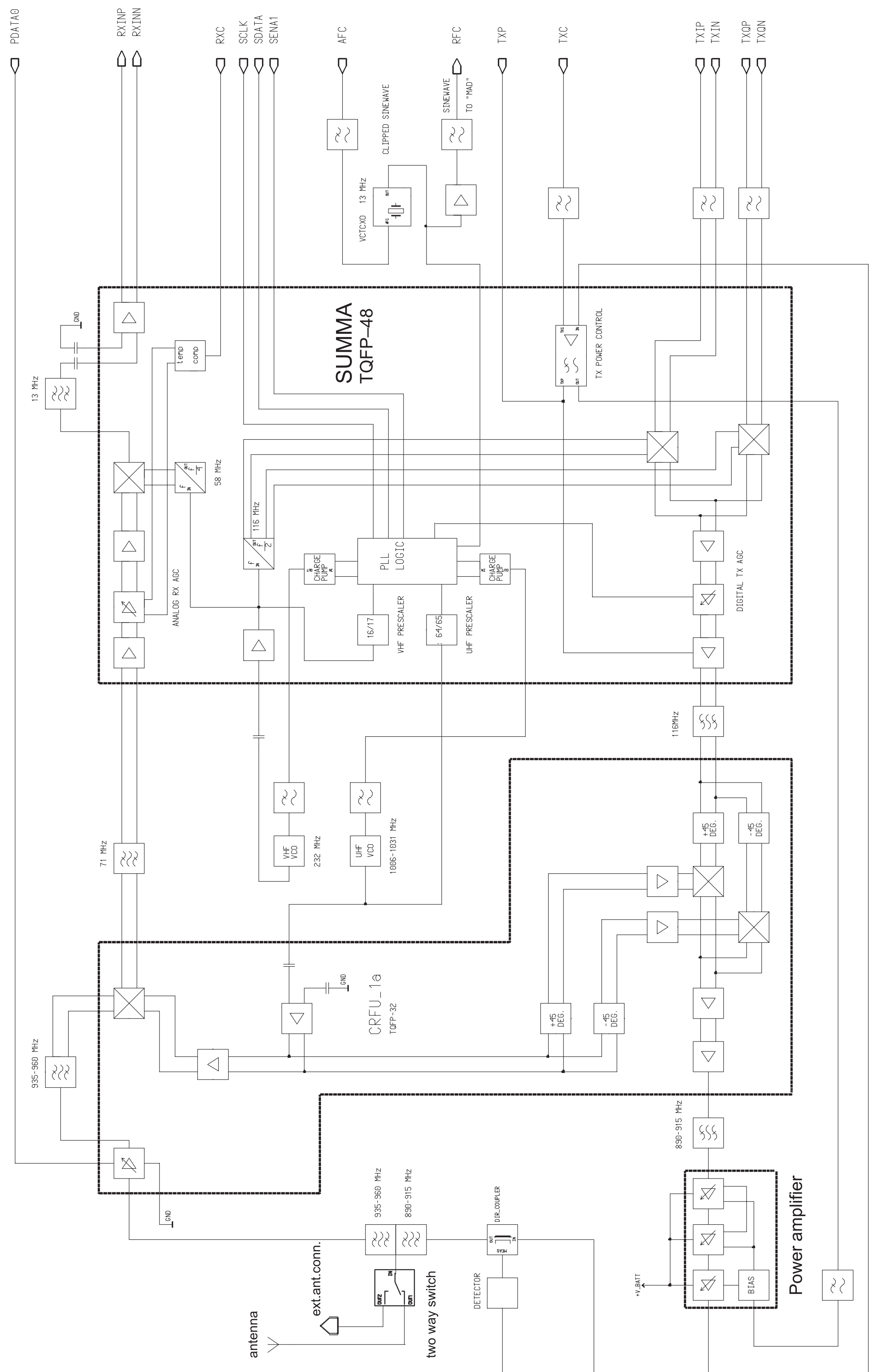


Figure 1.

Frequency synthesizers

Both VCOs are locked with PLLs into stable frequency source, which is a VCTCXO–module (voltage controlled temperature compensated crystal oscillator). The VCTCXO is running at 13 MHz. Temperature effect is controlled with AFC (automatic frequency control) voltage, the VCTCXO is locked into the frequency of the base station. AFC is generated by baseband with a 11 bit conventional DAC in COBBA.

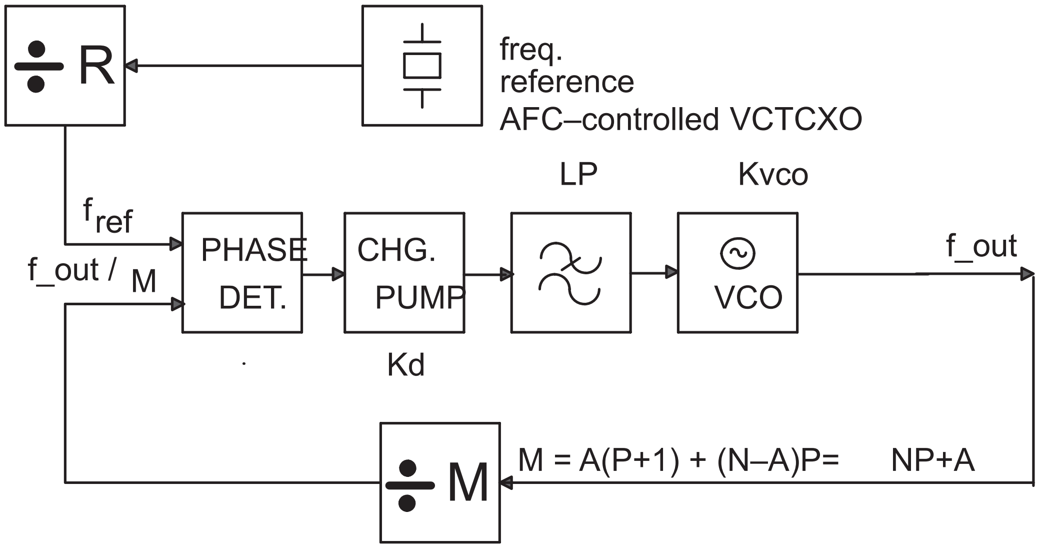
The UHF PLL is located in the SUMMA. There is 64/65 (P/P+1) prescaler, N– and A–divider, reference divider, phase detector and charge pump for the external loop filter.

The UHF local signal is generated by a VCO–module (VCO = voltage controlled oscillator) and sample of frequency of VCO is fed to prescaler. The prescaler is a dual modulus divider. The output of the prescaler is fed to the N– and A–dividers, which produce the input to phase detector.

The phase detector compares this signal to reference signal, which is divided with reference divider from VCTCXO output. Output of the phase detector is connected into charge pump, which charges or discharges integrator capacitor in the loop filter depending on the phase of the measured frequency compared to reference frequency.

The loop filter filters out the pulses and generates the DC to control the frequency of UHF–VCO. The loop filter defines step response of the PLL (settling time) and effects to stability of the loop, that's why integrator capacitor has got a resistor for phase compensation.

The other filter components are for sideband rejection. Dividers are controlled via serial bus. SDATA is for data, SCLK is serial clock for the bus and SENA1 is a latch enable, which stores new data into dividers. The UHF–synthesizer is the channel synthesizer, so the channel spacing is 200 kHz. 200 kHz is the reference frequency for the phase detector.



VHF PLL is also located into SUMMA. It comprises a 16/17 (P/P+1) dual modulus prescaler, N– and A–dividers, reference divider, phase detector and charge pump for the loop filter. The VHF local signal is generated with a discrete VCO–circuit. The VHF PLL works in the same way as UHF–PLL. The VHF–PLL is locked on fixed frequency, so higher reference frequency is used to decrease phase noise.

Receiver

Receiver is a dual conversion linear receiver.

The received RF–signal from the antenna is fed via the duplex filter to LNA (low noise amplifier) in CRFU_1a. Active parts (RF–transistor and biasing and AGC–step circuitry) are integrated into this chip. Input and output matching networks are external.

Gain selection is carried out with PDATA0 control. Gain step in LNA is activated when the RF–level in the antenna is about –45 dBm.

After the LNA amplified signal (with low noise level) is fed to bandpass filter, which is a SAW–filter (SAW, surface acoustic wave).

This bandpass filtered signal is then mixed down to 71 MHz, which is the first intermediate frequency. The 1st mixer is located into CRFU_1a ASIC. This integrated mixer is a double balanced Gilbert cell. All active parts and biasing are integrated and matching components are external. Because this is an axtive mixer it also amplifies IF–frequency. Also local signal buffering is integrated and upper side injection is used. First local signal is generated by the UHF–synthesizer.

The first IF–signal is then bandpass filtered with a selective SAW–filter. From the mixer output to the IF–circuit input the signal path is balanced. The IF–filter provides selectivity for channels greater than +/–200 kHz. Also it attenuates image frequency of the second mixer and intermodulating signals. Selectivity is required in this place, because of needed linearity and adjacent channel interferers will be on too high signal level for the stages following.

The next stage in the receiver chain is AGC–amplifier. It is integrated into SUMMA–ASIC. The AGC has got analog gain control. The control voltage for the AGC is generated with DA–converter in COBBA in baseband. AGC–stage provides accurate gain control range (min. 57 dB) for the receiver.

After the AGC there is the second mixer, which generates the second intermediate frequency, 13 MHz. The local signal is generated in SUMMA by dividing VHF–synthesizer output (232 MHz) by four, so the 2nd LO–frequency is 58 MHz.

The 2nd IF–filter is a ceramic bandpass filter at 13 MHz. It attenuates adjacent channels, except for +/– 200 kHz there is not much attenuation. Those +/– 200 kHz interferers are filtered digitally by the baseband. So the RX DACs are so good, that there is enough dynamic range for the faded 200 kHz interferer. Also the whole RX has to be able to handle signal levels in a linear way

After the 13 MHz filter there is a buffer for the IF–signal, which also converts and amplifies single ended signal from filter to balanced signal for the buffer and AD–converters in COBBA. Buffer in SUMMA has got voltage gain of 36dB and buffer gain setting in COBBA is 0 dB. It is possible to set gainstep (9.5 dB) into COBBA via control bus, if needed..

Transmitter

The transmitter chain consists of IQ–modulator, upconversion mixer, power amplifier and there is a power control loop.

I– and Q–signals are generated by baseband in COBBA–ASIC. After post filtering (RC–network) they are fed into IQ–modulator in SUMMA. It generates modulated TX IF–frequency, which is VHF–synthesizer output divided by two, that is 116 MHz. The TX–amplifier in SUMMA has two selectable gain levels. Output is set to maximum via control register of SUMMA. After SUMMA there is a bandpass LC–filter for noise and harmonic filtering before the signal is fed for upconversion into final TX–frequency in CRFU_1a.

Upconversion mixer in CRFU_1a is a so called image reject mixer. It attenuates the unwanted sideband in the upconverter output. The mixer itself is a double balanced Gilbert cell. The phase shifters required for image rejection are also integrated. The local signal needed in upconversion is generated by the UHF–synthesizer, but buffers for the mixer are integrated into CRFU_1a.

The output of the upconverter is buffered and matching network makes a single ended 50 ohm impedance.

The next stage is a TX interstage filter, which attenuates the unwanted signals from the upconverter, mainly LO–leakage and image frequency from the upconverter. Also it attenuates the wideband noise. This bandpass filter is a SAW–filter.

The final amplification is carried out by the third IC, the power amplifier which is a MMIC. It features a 50 ohm input, output requires an external matching network. The MMIC comprises three amplifier stages and interstage matchings. Also included is a gain control, which is controlled with a power control loop. The PA features over 35 dB power gain and it is able to produce 2.5 W into output with 0 dBm input level. The gain control range is over 35 dB to get desired power levels and power ramping up and down.

The harmonics generated by the nonlinear PA (class AB) are filtered out with the matching network and lowpass/bandstop filtering in the duplexer. Bandstop is required because of wideband noise located on RX–band.

Power control circuitry consists of a power detector in the PA output and an error amplifier in SUMMA. There is a directional coupler connected between the PA–output and the duplex filter. It takes a sample from the forward going power with certain ratio. This signal is rectified in a schottky–diode and it produces a DC–signal signal after filtering. This peak–detector is linear on absolute scale, except it saturates on very low and high power levels – it produces a S–shape curve.

This detected voltage is compared in the error–amplifier in SUMMA to TXC–voltage, which is generated by DA–converter in COBBA. Because also gain control characteristics in PA are linear in absolute scale, control loop defines a voltage loop, when closed. The closed loop tracks the TXC–voltage quite linearly.

The TXC has got a raised cosine form ($\cos^4$ – function), which reduces switching transients, when pulsing power up and down. Because dynamic range of the detector is not wide enough to control the power (actually RF output voltage) over the whole range, there is a control named TXP to work under detected levels. Burst is enabled and set to rise with the TXP until the output level is high enough, that feedback loop works. The loop controls the output via the control pin in the PA MMIC to the desired output level and burst has got the waveform of TXC–ramps. Because feedback loops could be unstable, this loop is compensated with a dominating pole. This pole decreases gain on higher frequencies to get phase margins high enough.

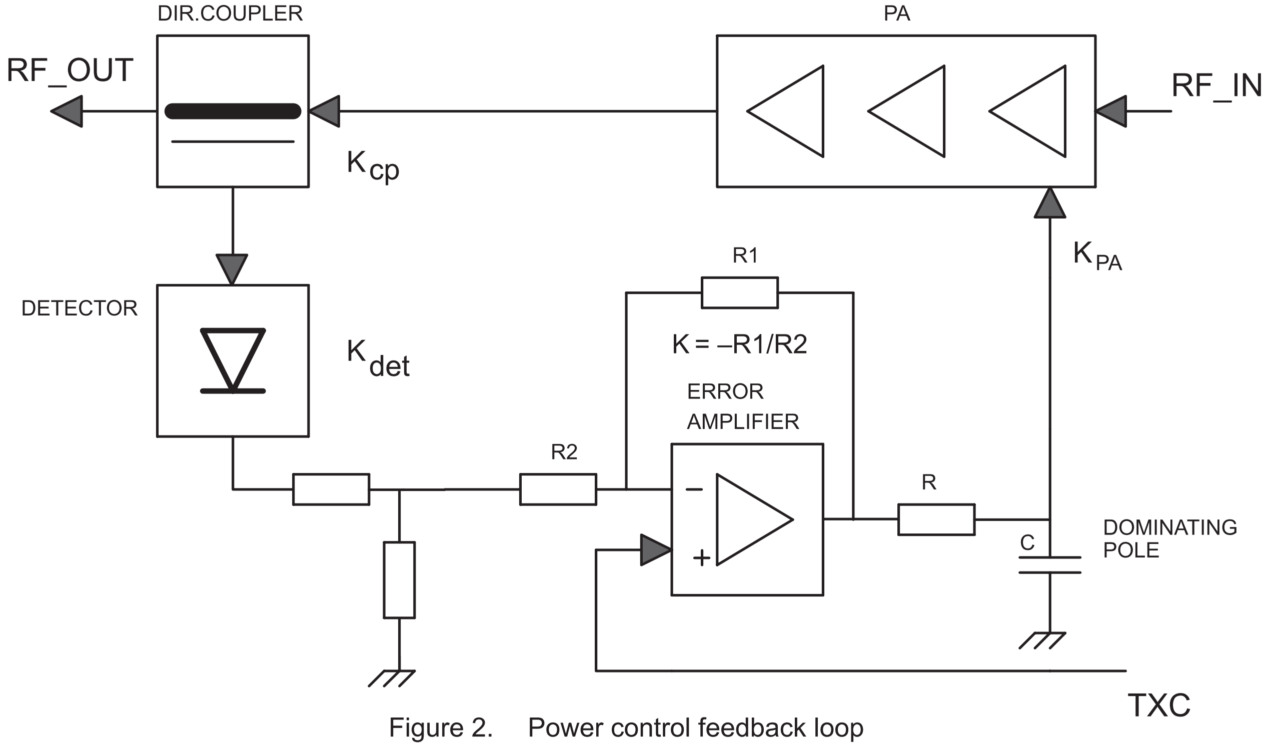


Figure 2. Power control feedback loop

AGC strategy

The AGC–amplifier is used to maintain output level of the receiver almost constant.

AGC has to be set before each received burst, this is called pre–monitoring. The receiver is switched on before the burst begins, the DSP measures received signal level and adjusts RXC, which controls RX AGC–amplifier or it switches off the LNA with PDATA0 control line. This pre–monitoring is done in three phases and this sets the settling times for RX AGC. Pre–monitoring is required because of linear receiver, received signal must be in full swing, no clipping is allowed and because DSP doesn't know, what is the level going to be in next burst.

There is at least 60 dB accurate gain control (continuous, analog) and one digital step in LNA. It is typically about 30...35 dB.

RSSI must be measured on range –48...–110 dBm. After –48 dBm level MS reports to base station the same reading.

Because of RSSI–requirements, gain step in LNA is used roughly on –45 dBm RF–level and up to –10 dBm input RF–level accurate AGC is used to set RX output level. LNA is ON (PDATA0 = "0") below –47 dBm. from –47 dBm down to –95 dBm

This accurate AGC in SUMMA is used to adjust the gain to desired value. RSSI–function is in DSP, but it works out received signal level by measuring RX IQ–level after all selectivity filtering (meaning IF–filters, ΣΔ±converter and FIR–filter in DSP). So 50 dB accurate AGC dynamic range is required. Remaining 10 dB is for gain variations in RX–chain (for calibration)

Below –95 dBm RF–levels, output level of the receiver drops dB by dB. At –95 dBm level output of the receiver gives 50 mVpp. This is the target value for DSP. Below this it drops down to ca. 9 mVpp @ –110 dBm RF–level.

This strategy is chosen because we have to roll off the AGC in PLUSSA early enough, that it won't saturate in selectivity tests. Also we can't start too early, then we will sacrifice the signal to noise ratio and it would require more accurate AGC dynamic range. 50 mVpp target level is set, because RX–DAC will saturate at 1.4 Vpp. This over 28 dB headroom is required to have margin for +/– 200 kHz faded adjacent channel (ca. 19 dB) and extra 9 dB for pre–monitoring.

Production calibration is done with two RF–levels, LNA gain step is not calibrated. The gain changes in the receiver are taken off from the dynamic range of accurate AGC. Variable gain stage in SUMMA is designed in a way, that it is capable of compensating itself, there is good enough margin in AGC.

AFC function

AFC is used to lock the transceivers clock to the frequency of the base station.

AFC–voltage is generated in the COBBA with a 11 bit AD–converter. There is a RC–filter in AFC control line to reduce the noise from the converter. Settling time requirement for the RC–network comes from signalling, how often PSW (pure sine wave) slots occur. They are repeated after 10 frames , meaning that there is PSW in every 46 ms.

AFC tracks the base station frequency continuously, so the transceiver has got a stable frequency, because changes in the VCTCXO–output don't occur so fast (temperature).

Settling time requirement comes also from the start up–time allowed. When transceiver is in sleep mode and "wakes" up to receive mode , there is only about 5 ms for the AFC–voltage to settle. When the first burst comes in system clock has to be settled into +/– 0.1 ppm frequency accuracy. Settling time requirement comes also from the start up–time allowed. When transceiver is in sleep mode and "wakes" up to receive mode , there is only about 5 ms for the AFC–voltage to settle. When the first burst comes in system clock has to be settled into +/– 0.1 ppm frequency accuracy.

The VCTCXO–module requires also 5 ms to settle into final frequency. Amplitude rises into full swing in 1 ... 3 ms, but frequency settling time is longer so this oscillator must be powered up early enough.

RF block requirements

Duplex filter

Parameter	Transmit section		Receive section		unit
Center frequency, ftx,frx	ftx : 902.5		frx : 947.5		MHz
BW (bandwidth) at passband	+/– 12.5		+/– 12.5		MHz
Maximum insertion loss at BW	1.6 (at +25 deg. C) 1.9 (at –20...+85 deg. C)		3.2 (at +25 deg. C) 3.7 (at –20...+85deg. C)		dB
Ripple at BW, peak to peak	1.1		1.5		dB
Terminating imped-ance	50		50		ohms
Maximum VSWR	2.2		1.8		
Minimum attenuations	Freq.range	Att.	Freq.range	Att.	
	925...935	3	3...200	30	MHz/dB
	935...960	15	200...500	16	MHz/dB
	1780...1830	28	500...890	25	MHz/dB
	2670...2745	35	890...915	26	MHz/dB
			980...1000	21	MHz/dB
			1000...1050	23	MHz/dB
			1400...1500	35	MHz/dB
Permissible input pow-er	4.0 AVG (12.5% duty cyclr)				W

Part no: NMP code 4512075

Receiver blocks

LNA in CRFU_1a

Parameter	Min.	Typ.	Max.	Unit/Notes
Frequency band	935 – 960			MHz
Supply voltage	2.7	2.8	2.855	V
Current consumption			8	mA
Insertion gain	17.5	18.5	19.5	dB
Noise figure		1.7	2.2	dB,PDATA0=H
Input 1 dB compression point	–19			dBm, PDATA0=H
Reverse isolation	15			dB
Input VSWR			2	

Parameter	Min.	Typ.	Max.	Unit/Notes
Output VSWR			2	
Gain reduction	30		35	dB,room temp.
Step accuracy	–2		+2	dB,over temp.range
Noise figure, when PDATA=0		20		dB

RX interstage filter

Parameter	Min.	Typ.	Max.	Unit
Passband	935 – 960			MHz
Insertion loss			3.3	dB
Ripple in passband			1.3	dB
Attenuation DC...890 MHz	45			dB
Attenuation 890...915 MHz	25			dB
Attenuation 980...1030 MHz	25			dB
Attenuation 1025...3000 MHz	35			dB
Terminating impedance	UNBALANCED–BALANCED 50/50			ohm
VSWR			2.0	
Maximum drive level			+15	dBm

Part no: NMP code 4511049

1st mixer in CRFU_1a

Parameter	Min.	Typ./ Nom.	Max.	Unit/Notes
Supply voltage	2.7	2.8	2.85	V
Current consumption		9		mA
RX frequency range	935		960	MHz
LO frequency range	1006		1031	MHz
IF frequency		71		MHz
Insertion gain	9		12	dB
NF, SSB			11.5	dB
IIP3	0			dBm
1 dB input compression point	–10			dBm
IF/2 spurious level	–30			dBm, *
LO power level in RF–port			–25	dBm
Input VSWR			2	
Output resistance (balanced)	10 k			ohm
Output capacitance (balanced)		1.2		pF

1st IF–filter

Parameter	min.	typ.	max.	unit
Operating temperature range	–20		+75	deg.C
Center frequency , fo		71		MHz
Maximum ins. loss at 1dBBW			11	dB
Group delay ripple at +/–90 kHz BW			1.3	us pp
Bandwidths relative to 71 MHz 1 dB bandwidth 3 dB bandwidth 5 dB bandwidth 22 dB bandwidth 30 dB bandwidth 40 dB bandwidth	 +/– 70 +/–120		 +/– 230 +/– 350 +/– 550 +/– 700	kHz
Spurious rejection, fo +/– 26 MHz	65			dB, *
Terminating impedance (balanced) resistance input resistance output capacitance (parallel) input capacitance (parallel) output		 1.1 1.2 15.6 10.6		 kohm kohm pF pF

* Matching network included. NMP part no. 4510137

AGC–stage and 2nd mixer in SUMMA

Parameter	Min.	Typ.	Max.	Unit/Notes
Supply voltage	2.7	2.8	2.85	V
Current consumption		27	32	mA
Input frequency range	45		120	MHz
2nd IF frequency range	0.4		17	MHz
Total noise figure, SSB, max. gain			15	dB,
Total noise figure, SSB, min. gain			65	dB,
Max. voltage gain	40			dB
Min. voltage gain			–20	dB
Control voltage for min. gain		0.5		V
Control voltage for max. gain		1.4		V
Output 1 dB compression point @ max. gain	800			mVpp
Input 1 dB compresion point @ min. gain	80			mVpp
IF input impedance (balanced)	2.4/tbd	3.8/2	5.6/tbd	kohm/pF
2nd mixer output impedance (single output)			100	ohm

2nd IF Filter

Parameter	min.	typ.	max.	unit
Center frequency, fo		13		MHz
1 dB bandwidth, 1dBBW (relative to 13 MHz)	+/– 90			kHz
Insertion loss			6.0	dB
Amplitude ripple at 1dBBW			1.0	dB
Group delay ripple at 1 dB BW, peak to peak			1.5	us
Attenuations, relative to 13 MHz fo +/– 400 kHz fo +/– 600 kHz fo +/– 800 kHz	 25 35 45			dB
Terminating impedance	313	330	347	ohm

NMP part no. 4510009

Buffer in SUMMA for 2nd IF

Parameter	Min.	Typ.	Max.	Unit
Input frequency range	0.4		17	MHz
Voltage gain (single ended input and balanced output)	34	36	38	dB
1 dB output compression point (Rload=10 kohm balanced)		1.4		Vpp
Input impedance		3.3/4		kohm/pF
Output impedance, balanced			600	ohm

Transmitter blocks

IQ–modulator and TX–AGC in SUMMA

Parameter	Min.	Typ.	Max.	Unit
Supply voltage	2.7	2.8	2.85	V
Current consumption		28	tbd.	mA
Modulator Inputs (I/Q)	**Minimum**	**Typical / Nominal**	**Maximum**	**Unit / Notes**
Input bias current (balanced)			100	nA
Input common mode voltage		0.8		V
Input level (balanced)			1.2	Vpp
Input frequency range	0		300	kHz
Input resistance (balanced)	tbd			kohms
Input capacitance (balanced)			2	pF
IQ–input phase balance total, temperature included	–4		4	deg.
IQ–input phase balance temperature effect	–2		2	deg.
IQ–input amplitude balance total, temperature included	–0.5		0.5	dB
IQ–input amplitude balance temperature effect	–0.2		0.2	dB
Modulator Output	**Minimum**	**Typical / Nominal**	**Maximum**	**Unit / Notes**
Output frequency	85		400	MHz
Output power, high (balanced, into 100 ohm) NOTE: Requires input level of 1.1 Vpp (difrential)	–5	–3		dBm
Output power, low (balanced, into 100 ohm) NOTE: Requires input level of 1.1 Vpp (diff.)	–10	–8		dBm
Noise level in output			–145	dBm/Hz avg.
Total gain control range	35			dB
Gain step		5		dB

Modulator Output	Minimum	Typical / Nominal	Maximum	Unit / Notes
Absolute gain accuracy	–2		+2	dB
Any gain step up/down settling time			10	usec
Output 3rd Order Intermodulation products, when both wanted signals are at the level of –12 dBm at the output			–35	dB

116 MHz LC TX IF–filter

Parameter	Min.	Typ.	Max.	Unit
Center frequency		116		MHz
Insertion loss @ 116 MHz			3.7	dB
Relative attenuation @ +/– 10 MHz offset	5			dB
Relative attenuation @ +/– 20 MHz offset	8			dB
Relative attenuation @ 232 MHz	15			dB
Relative attenuation @ 348 MHz	20			dB
Relative attenuation @ 464–1000 MHz	25			dB
Input impedance, balanced		100		ohm
Output impedance, balanced		200		ohm

Upconversion mixer and in CRFU_1a

Parameter	Min.	Typ.	Max.	Unit
Supply voltage	2.7	2.8	2.85	V
Supply current			50	mA
Input frequency		116		MHz
Input level		–5	–8	dBm
Output frequency range	890		915	MHz
Output level	+3	+5		dBm
NF,SSB			20	dB
LO–signal level in output			–29	dBc
Unwanted sideband level			–15	dBc
fLO+/–2xIF spurious level			–40	dBc
7x116 MHz spurious level			–40	dBc

Parameter	Min.	Typ.	Max.	Unit
8x116 MHz spurious level			–55	dBc
Input impedance (balanced)		600//2		ohm//pF
Output VSWR, (with matching network and output balun)			2	

TX interstage filter

Parameter	Min.	Typ.	Max.	Unit
Passband	890 – 915			MHz
Insertion loss			3.8	dB
Ripple in passband			1.5	dB
Attenuation DC...813 MHz	35			dB
Attenuation 925...935 MHz	7			dB
Attenuation 935...960 MHz	15			dB
Attenuation 1006...1031 MHz	40			dB
Attenuation 1122...1147 MHz	45			dB
Attenuation 1780...1830 MHz	10			dB
Attenuation 2670...2745 MHz	10			dB
Terminating impedance	50			ohm
VSWR			2.5	
Maximum drive level			+15	dBm

NMP part no. 4511015

Power amplifier MMIC

Parameter	Symbol	Test condition	Min	Typ	Max	Unit
Operating freq. range			880		915	MHz
Supply voltage	Vcc		3.0	3.5	5.0	V
Auxiliary supply voltage	Vreg		2.7	2.8	2.9	V
Auxiliary supply current	Ireg				tdb.	mA
Input power	Pin	Pout=35.0 dBm, Vcc=3.5 V, Vpc=2.2 V,	0	2	5	dBm
Output power	Pout	Pin= 0 dBm, Vcc=3.0 V, Vpc=2.2 V, Tamb=+85 deg.C	34.2			dBm
Gain control range (overall dynamic range)		Vpc= 0.5 ... 2.2 V	45			dB
Gain control slope (sensitivity at the linear range)	S	Vpc1 @10 Vpeak output volt. Vpc2 @0.5 Vpeak output volt. S=((10–0.5)/(Vpc1–Vpc2)) V/V, Pin = 0...+5dBm	20	tbd.	40	V/V

Parameter	Symbol	Test condition	Min	Typ	Max	Unit
Isolation		Vcc=3.5 V, Vpc=0.2 V, Pin=0 dBm			–40	dB
Carrier switching time	tr, tf	Vcc=3.5 V, Pin=0 dBm Vpc is a pulse from 0.2 to 2.2 V. Rise time up to –0.5 dB from the final power. Fall time vice versa.			1	us
Total efficiency	η	Pin= 0 dBm , Pout= +34.3 dBm, Vcc=3.5 V, Tamb = + 25 deg. C	50			%
Control current	Ipc	Pin= 0...+5 dBm , Pout= +34.8 dBm, Vcc=3.5 V			+/– 3	mA peak
Harmonics					–35	dBc
Input VSWR	VSWRi1	Pin= 0...+5 dBm , Pout= +34.0 dBm, Vcc=3.5 V			2:1	
	VSWRi2	Pin= 0...+5 dBm , Pout= +6.0 ... +32.0 dBm, Vcc=3.5 V Vpc adjusted for desired power levels			4:1	
Leakage current	Ileak	Vcc=3.5 V, Vpc=0 V, Vreg=0 V, no RF–drive			10	uA
Intermodulation distortion	IMD	Pinwant= 0 dBm @ 915 MHz Pinint = –50 dBm @ 905 MHz Poutwant= +34.8 dBm Vcc=3.5 V, Poutint @905 MHz Poutimd @925 MHz IMD=Poutint – Poutimd, Tamb = + 25 deg. C	5			dB
AM–PM conversion	Kp	Pin= –2.0 ... +5.0 dBm, Pout= +6.0 ... +34.0 dBm Vpc adjusted for desired output power levels Vcc=3.0 V			3	deg/dB
Receive band noise power	Pn	Vcc=3.5 V , RBW=30kHz Pout = +34.8 dBm, Freq. band: 925...960 MHz			–80	dBm
Stability		Pin= 0 dBm+/–3dBm, Vcc=3.0...5.0 V, Vpc=0 ... 2.2 V Load VSWR 12:1, all phases	All spurious outputs more than 65 dB below desired signal			
Load mismatch stress		Pin= 0 dBm, Vcc=5.0 V, Pout=Pmax Load VSWR 20:1, all phases	No module damage			

Directional coupler

Parameter	Min.	Typ.	Max.	Unit/Notes
Frequency range	890		915	MHz
Insertion loss			0.5	dB
Coupling factor		15		dB
Directivity	13		14	dB
Impedance level of the main line		50		ohm
VSWR on main line			1.6	
Impedance level of the coupled line		50		ohm

NMP part no. 4551001

Power detector

Parameter	Min.	Typ.	Max.	Unit/Notes
Supply voltage	2.7	2.8	2.85	V
Supply current			2.0	mA
Frequency range	890		915	MHz
Dynamic range	45			dB
Linear range, *	35			dB
Bias current for detector diode		40		uA
Input power range, **	–8		20	dBm
Output voltage	0.1		2.2	V
Variation of the detected voltage over temperature range			0.7	mV/°C
Load resistance	10			kohm

* RF input voltage versus detected output voltage
* * Directional coupler coupling factor 14 dB

Power control section in SUMMA, closed loop characteristics

Parameter	Min.	Typ.	Max.	Unit/Notes
Supply voltage	2.7	2.8	2.85	V
Supply current		tbd.		mA
TXP input voltage, LOW			0.5	V
TXP input voltage, HIGH	2.4			V
Detector input voltage	0.1		2.2	V
TXC input voltage	0.1		2.2	V

Parameter	Min.	Typ.	Max.	Unit/Notes
TXC and TXP input resis- tance	50			kohm
TXC and TXP input capaci- tance		4		pF
Output voltage (POP & POG)	0.5		2.2	V
POP– and POG–output im- pedance		50		ohm
POP and POG –output cur- rent driving capability	+/– 4			mA
Switch on resistance (bet– ween INL& POP or POG)		tbd.		ohm
Voltage of POP/POG when inactive (max. 3.5mA sink)		0.1		V
Offset of OP1 and OP2 op.amp.	–40		40	mV
Temperature coefficient of the offset voltage		30		uV/deg.C
Bandwidth (OP1 & OP2), unity gain	6			MHz
Open loop gain		20		dB
Closed loop gain		15		dB
Closed loop –3 dB bandwidth		70		kHz
Phase margin	45	60		degrees
Gain margin		30		dB

Synthesizers blocks

VCTCXO, reference oscillator

Parameter	Min.	Typ.	Max	Unit/.Notes
Supply voltage, Vcc	2.70	2.80	2.85	V
Current consumption, Icc			1.5	mA
Operating temperature range	–20		+75	deg. C
Nominal frequency		13		MHz
Output voltage swing (swing of 13 MHz component, se- lective measurement from the spec- trum)	800			mVpp
Load, resistance capacitance		2 10		kohm pF
Frequency tolerance @+25 deg. C	– 1.0		+ 1.0	ppm
Frequency tolerance after reflow (@ +25 deg. C)	– 2.0		+ 2.0	ppm

Parameter	Min.	Typ.	Max	Unit/.Notes
Frequency stability vs. temperature (ref. @+25 , –20....+75 deg. C)	– 5.0		+ 5.0	ppm
Frequency stablity vs. supply voltage (2.8 V +/– 100 mV)	– 0.1		+ 0.1	ppm
Frequency stability vs. load change (2 kohm//10 pF +/– 10 %)	– 0.3		+ 0.3	ppm
Aging	– 1.0		+ 1.0	ppm/year
Nominal control voltage, Vc		1.15		V
Voltage control range	0.0		2.3	V
Voltage control characteristics (see note 1.)	+/– 12		+/– 24	ppm/V when 0.3 V<Vc<2.3 V
Vc input resistance	1			Mohm
Frequency adjustment	+/– 3.0			ppm with inter– nal trimmer
Harmonics (with 2 kohm//10 pF)			– 5	dBc
Start up time output level within 90% output frequency limits +/–0.05ppm from the final value			 5 5	ms
Phase noise @ 1 kHz offset			–130	dBc/Hz

VHF PLL in SUMMA

The same VHF VCO and also the same frequency is used so the VHF PLL is common.

Table 2. VHF–synthesizer, specification

Parameter	Min.	Typ.	Max.	Unit/Notes
Start up settling time			3.0	ms
Phase error			1	deg./rms
Sidebands +/– 1 MHz +/– 2 MHz +/– 3 MHz > +/– 3.0 MHz			 –70 –80 –80 –90	 dBc

Table 3. VHF PLL block in SUMMA, specification

Parameter	Min.	Typ.	Max.	Unit/notes
Input frequency range	150		500	MHz
Input signal level	80		800	mVpp
Input resistance	tbd.			kohm
Input capacitance			tbd.	pF
Supply current		3.5		mA
Reference input frequency			30	MHz

Table 3. VHF PLL block in SUMMA, specification (continued)

Parameter	Min.	Typ.	Max.	Unit/notes
Phase comparison frequency			1	MHz
Charge pump output current 1 current 2		 0.5 2.0		mA
Sink to source current matching error of the charge pump			+/– 5	%
Charge pump current error			+/– 10	%
Charge pump min. output voltage		0.5		V
Charge pump max. output voltage		* Vcp–0.5		V
Charge pump leakage current			5	nA
Phase detector phase noise level			–163	dBc/Hz

*Vcp = 5V

VHF VCO and low pass filter

Parameter	Min.	Typ.	Max.	Unit/Notes
Supply voltage range	2.7	2.8	2.85	V
Current consumption		4	7	mA
Control voltage	0.5		4.0	V
Operation frequency		232		MHz
Output level	–13	–10		dBm (output after the lowpass filter)
Harmonics			–30	dBc, (filtered)
Phase noise, fo +/– 600 kHz fo +/– 1600 kHz fo +/– 3000 kHz			 –120 –130 –140	dBc
Control voltage sensitivity	8.0		14.0	MHz/V
Pushing figure			+/– 2	MHz/V
Frequency stability			+/– 3	MHz (over temperature range –10...+75 C deg.)
Spurious content			–70	dBc

UHF PLL

Table 4. UHF–synthesizer,

Parameter	Min.	Typ.	Max.	Unit/Notes
Start up settling time			3.0	ms
Settling time +/– 25 MHz		500	800	us, (into +/– 20 Hz from final frequency)
Phase error			3.7	deg./rms
Sidebands +/– 200 kHz +/– 400 kHz +/– 600...+/–1400 kHz +/–1.4... +/– 3.0 MHz > +/– 3.0 MHz			 –40 –60 –66 –76 –86	 dBc

Table 5. UHF PLL block in SUMMA

Parameter	Min.	Typ.	Max.	Unit/notes
Input frequency range	650		1700	MHz
Input signal level (f<1.5 GHz)	200			mVpp
Input resistance	tbd.			kohm
Input capacitance			tbd.	pF
Supply current		8		mA
Reference input frequency			30	MHz
Reference input level	100			mVpp
Reference input impedance		tbd.		
Phase comparison frequency			1	MHz
Charge pump output current 1 current 2		 0.5 2.0		 mA
Sink to source current matching error of the charge pump			+/– 5	%
Charge pump current error			+/– 10	%
Charge pump current temperature variation			tbd.	%
Charge pump leakage current			5	nA
Phase detector phase noise level			–163	dBc/Hz

UHF VCO module

Parameter	Conditions	Rating	Unit/ Notes
Supply voltage, Vcc		2.8 +/– 0.1	V
Supply current, Icc	Vcc = 2.8 V, Vc= 2.25 V	< 10	mA
Control voltage, Vc	Vcc = 2.8 V	0.8... 3.7	V

Parameter	Conditions	Rating	Unit/ Notes
Oscillation frequency	Vcc = 2.8 V Vc = 0.8 V Vc = 3.7 V	 < 1006 > 1031	 MHz MHz
Tuning voltage in center frequency	f = 1018.5 MHz	2.25 +/– 0.25	V
Tuning voltage sensitivity in operating frequency range on each spot freq.	Vcc = 2.8 V f=1006...1031 MHz	14 +/– 2	MHz/V
Output power level	Vcc=2.7 V f=1006...1031 MHz	–6.0 min.	dBm
Output impedance and VSWR	f=1006...1031 MHz	50 ohms,VSWR <2	
Phase noise, fo +/– 25 kHz fo +/– 600 kHz fo +/– 1600 kHz fo +/– 3000 kHz	Vcc=2.8 V f=1006...1031 MHz	–100 –120 –130 –140	dBc/Hz max.
Pulling figure	VSWR=2, any phase	+/– 1.0	MHz max.
Pushing figure	Vcc=2.8 +/– 0.1 V	+/– 2.0	MHz/V max.
Frequency stability over temperature range	Ta=–20 ... +75 deg. C	+/– 3.0	MHz max.
Harmonics		–10 max.	dBc
Spurious	Vcc=2.8 V, Vc=0...6 V	–70 max.	dBc
Input capacitance in Vc–pin	Vc= 0 V	100 max.	pF

UHF local signal input in CRFU_1a

Parameter	Min.	Typ.	Max.	Unit/Notes
Input frequency range	990		1040	MHz
Input level	200		700	mVpp
Input resistance		100		ohm
Input capacitance			1.5	pF

RF/BB/DSP Interface

The following three sections describe the hardware and timing interface between RF and the BB/DSP section of the RAE–2.

Interface Signal Characteristics

The interface signals between the BB and the RF section are shown in the next table as a logical interface. On physical board level baseband supplies voltages from CCONT to separate RF sub–blocks. The maximum values specified for the digital signals in the table are the absolute maximum values from the RF interface point of view.

Table 6. AC and DC Characteristics of RF/BB signals

Signal name	From - To	Function
VBATT	Battery RF	Supply voltage for RF (PA on/PA off)
VXOENA	MAD CCONT	VR1, VR6 in CCONT ON
		VR1, VR6 in CCONT OFF
SYNPWR	MAD CCONT	VR3, VR4 in CCONT ON
		VR3,VR4 in CCONT OFF
RXPWR	MAD CCONT	VR2, VR5 in CCONT ON
		VR2, VR5 in CCONT OFF
TXPWR	MAD CCONT	VR7 in CCONT ON
		VR7 in CCONT OFF
VREF	CCONT SUMMA	Reference voltage for SUMMA and CRFU1a
PDATA0	MAD CRFU1A	Nominal gain in LNA
		Reduced gain in LNA
SENA	MAD SUMMA	PLL enable
SDATA	MAD SUMMA	Synthesizer data
SCLK	MAD SUMMA	Synthesizer clock
AFC	COBBA VCTCXO	Automatic frequency control signal for VC(TC)XO
		10...10000Hz
RFC	VCTCXO MAD	High stability clock signal for the logic circuits
RXIP/RXIN	SUMMA COBBA	Differential RX 13 MHz signal to baseband
TXIP/TXIN	COBBA SUMMA	Differential in–phase TX baseband signal for the RF modulator
TXQP/TXQN	COBBA SUMMA	Differential quadrature phase TX baseband signal for the RF modulator
TXP	MAD SUMMA	Transmitter power control enable

Table 6. AC and DC Characteristics of RF/BB signals (continued)

Signal name	From - To	Function
TXC	COBBA SUMMA	Transmitter power control
		0...200 kHz
RXC	COBBA SUMMA	Receiver gain control
		0...200 kHz

TXC and AGC signals originate from the same DAC, controlled in COBBA

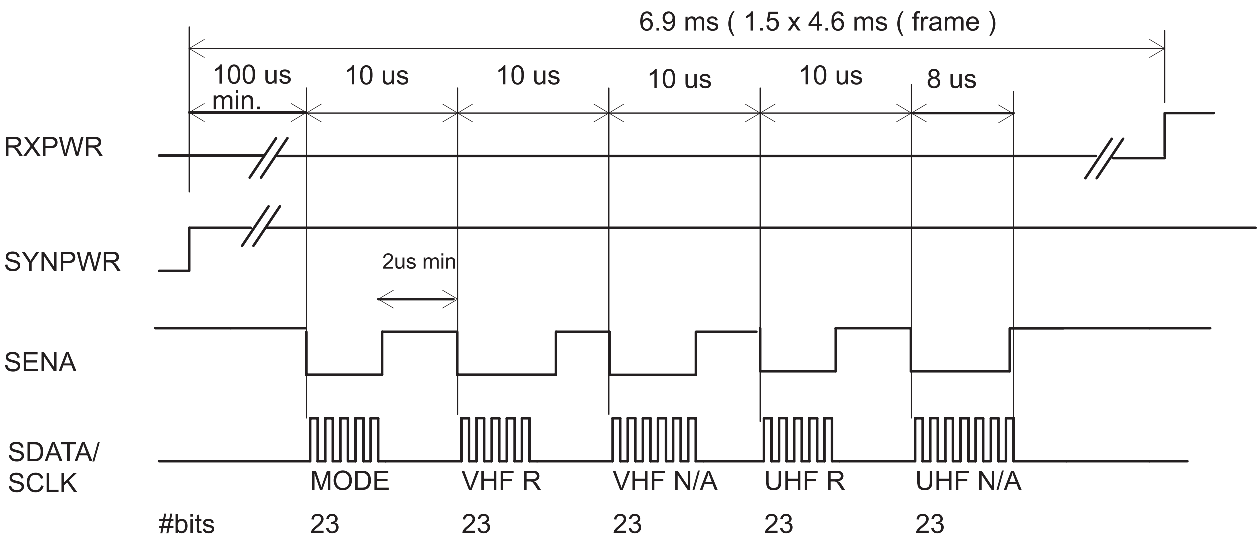
Data Interface and Timing

The SUMMA is programmed via the serial bus SENA, SDATA and SCLK. The data of the SDATA is clocked by rising edge of SCLK. The data is fed MSB first and address bits before data bits. The data for the Programmable dual modulus counter is fed first and the Swallow counter last. SENA is kept low while clocking the data. (Figure below)

During programming, the charge pump attached to programmed divider is switched to high impedance state. Also all counters connected to the PLL that is programmed, are kept on reset while the SENA is low.

Table 7. Logic levels

Parameters	Min	Typ	Max	Units
High	2			Volt
Low			0.8	Volt



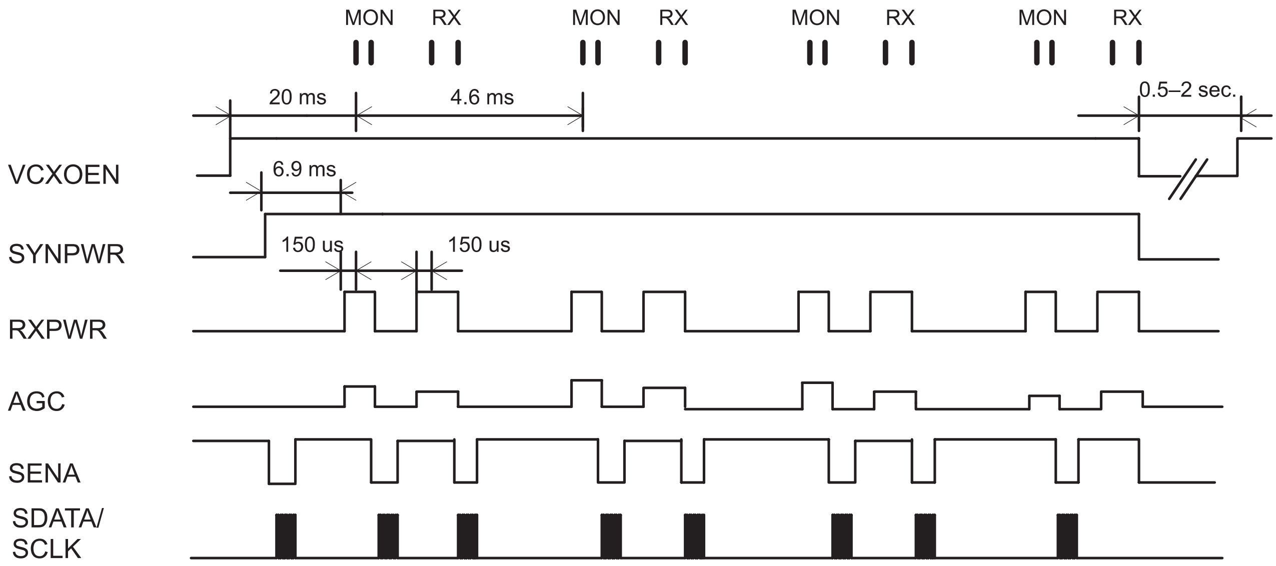


Figure 3. Synthesizer timing / IDLE, one monitoring/frame, frame can start also from RX–burst

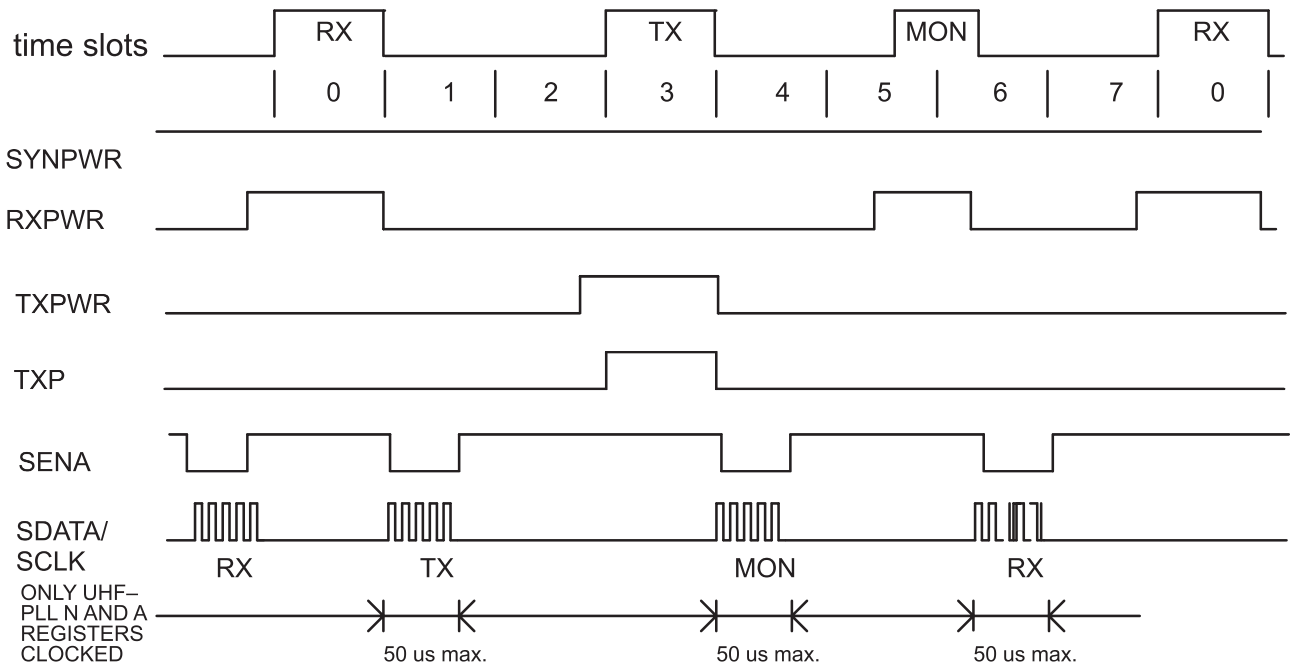


Figure 4. UHF–synthesizer timing/clocking on traffic channel

Transmit Power Timing

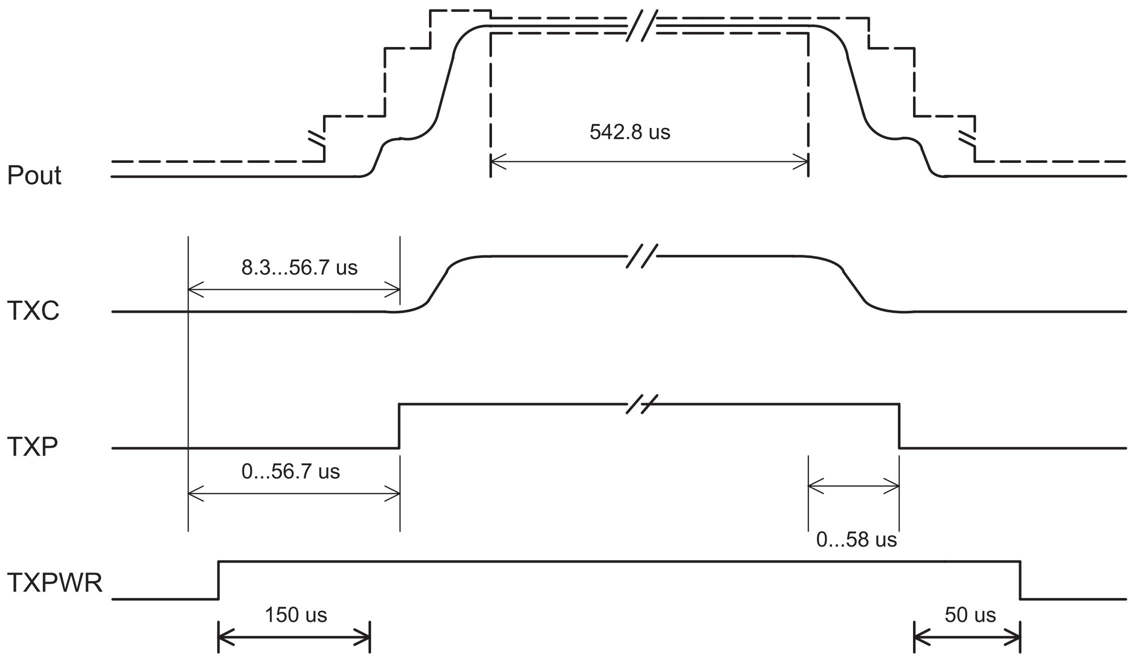


Figure 5. Transmitter timing diagram for normal bursts

SUMMA and Synthesizer Control

Registers

The following table shows the programmable registers in SUMMA which are used for programmable counters and mode selection.

Table 8. Registers addressing

A2	A1	A0	HEX addr.	Bits	Register
0	0	0	0	18	Control register
0	0	1	1	15	VHF VDIV (VDIV2)
0	1	0	2	12	VHF RDIV (RDIV2)
0	1	1	3	18	UHF VDIV
1	0	0	4	12	UHF RDIV

PLL Control Word Format

Serial data format is shown below. Amount of bits needed for each address can be seen from Table 2. **When less bits are sent, dummy bits must be inserted between the address and the real data**.

MSB													LSB
A2	A1	A0	...	...	S9	S8	S7	S6	S5	S4	S3	S2	S1

Control Register

Bit no	Sign.	BS8 Def.	Name	Purpose
S1	LSB	0	VHFOFF	1=VHF synth power down
S2		0	NF	No Function
S3		1	MODE1	Mode selection LSB
S4		0	MODE2	Mode selection MSB
S5		0	TEST	Test Mode selection
S6		0	VHFCPCS	VHF charge pump current Set = 0 (0.5 mA) 1(2.0 mA)
S7		0	UHFCPCS	UHF charge pump current Set 0 (0.5 mA) 1(2.0mA)
S8		0	VPDMOD	Logic high keeps counters reset
S9		0	ADDBIAS	Extra bias for UHF prescaler
S10		1	G1	TX AGC step
S11		0	NF	No Function

Bit no	Sign.	BS8 Def.	Name	Purpose
S12		0	NF	No Function
S13		0	NF	No Function
S14		1	fast	Add current to chargepump
S15		0	PD_lin	UHF Phase detector mode
S16		0	UHFOFF	1=UHF synthesizer power down
S17		0	RX_SEL	digital RX on
S18		1	OA_sel	Selects pwrctrl opamp
S19	MSB	1	TX_AGC_LATCH	TXP driven agc gain latching

NOTE: NDIV2 divides reference frequency by programmable figure of 2–2047. Divide ratio less than 2 is prohibited.

Synthesizer clocking

GSM Division ratios

The values of ch range from 1 to 124

UHF synthesizer

reference divider ratio	R=65
N counter division ratio	N=INT((ch + 5030)/64)
A counter division ratio	A=MOD((ch + 5030)/64)

VHF synthesizer

reference divider ratio	R=13
N counter division ratio	N=14
A counter division ratio	A=8

Clocking scheme

During power up (first clocking) SUMMA synthesizers should be enabled in the following order :

1. Mode setting (GSM)
2. reference divider for VHF PLL
3. N and A dividers for VHF PLL
4. reference divider for UHF PLL
5. N and A dividers for UHF PLL

When transceiver is on allocated channel, then only (N and A dividers) UHF PLL is controlled, because it is the channel synthesizer. Mode settings and VHF PLL division ratios are fixed.

List of abbreviations

ADC	Analog to Digital Converter
AFC	Automatic Frequency Control
AGC	Automatic Gain Control
AM	Amplitude Modulation
ASIC	Application Specific Integrated Circuit
AVG	Average
BB	Baseband
BiCMOS	Bipolar and Complementary Metal Oxide Semiconductor process
BT	Bandwidth x symbol time (GMSK filter parameter)
BW	Bandwidth
CCONT	DCT3 power management ASIC
CLK	Clock
COBBA	DCT3 RF/BB and audio interface ASIC
CRFU1A	DCT3 dualband RF ASIC
CW	Continuous Wave
DAC	Digital to Analog Converter
DC	Direct Current
DCS	Digital Cellular System
DCT	Digital Core Technology
DSP	Digital Signal Processing or Digital Signal Processor
E–GSM	Extended GSM (wider TX/RX bands)
ESD	Electrostatic Discharge
ESR	Effective Series Resistance
ETSI	European Telecommunications Standard Institute
FDMA	Frequency Division Multiple Access
FIR	Finite Impulse Response
GMSK	Gaussian Minimum Shift Keying
GND	Ground
GSM	Global System for Mobile communications
HT	Hilly Terrain (GSM standard fading profile)
IC	Integrated Circuit
IF	Intermediate Frequency
IIP3	3rd order intermodulation Input Intercept Point

IMD	Intermodulation Distortion
LNA	Low Noise Amplifier
LO	Local Oscillator
MAD	DCT3 DSP/MCU/system logic ASIC (**M**CU–**A**SIC–**D**SP)
MMIC	Monolithic Microwave Integrated Circuit
MON	Monitoring slot
MS	Mobile Station
NF	Noise Figure
OIP3	3rd order Output Intercept Point
PA	Power Amplifier
PCB	Printed Circuit Board
PLL	Phase Locked Loop
PM	Phase Modulation
RA	Rural Area (GSM standard fading profile)
RBW	Resolution Bandwidth
RF	Radio Frequency
RMS	Root Mean Square
RSSI	Received Signal Strength Indicator
RX	Receiver
RXLEV	RX Level
SAW	Surface Acoustic Wave
SACCH	Slow Associated Control Channel
SPR	Standard Product Requirements (NMP's internal standard)
SSB	Single Sideband
SUMMA	DCT3 dualband IF ASIC
TCH	Traffic Channel
TDMA	Time Division Multiple Access
TU	Typical Urban (GSM standard fading profile)
TX	Transmitter
UHF	Ultra High Frequency (300 MHz ... 3 GHz)
VCO	Voltage Controlled Oscillator
VCTCXO	Voltage Controlled Temperature Compensated Crystal Oscillator
VHF	Very High Frequency (30 MHz ... 300 MHz)
VSWR	Voltage Standing Wave Ratio

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Chapter 4

UIF Module BS2

AMENDMENT RECORD SHEET

Amendment Number	Date	Inserted By	Comments
	02/99		Original

CONTENTS – User Interface

Introduction

This document describes the RAE–2 UI module BS2. The module comprises PDA LCD display and function keys and all CMT UI electronics except the audio components.

Technical Summary

The following sections of circuitry are included in the BS2 UI module:

– External components of BC2 CMT LCD module
– External components of PDA LCD display
– Backlighting circuit of CMT LCD display and keyboard
– PDA display backlighting circuit
– PDA function keyboard and CMT keyboard switch matrices including key dome sheets (3 pcs)
– RF coaxial cable connector and antenna clip

Other parts covered in this document:

– BC2 CMT LCD module
– PDA LCD display
– PDA LCD display EL backlighting panel
– CMT LCD display and keyboard EL backlighting panel

Technical Specifications

DC Characteristics

Pin / Conn.	Line Symbol	Parameter	Minimum	Typical / Nominal	Maximum	Unit	Notes
1/X700	VPDA	Filtered battery voltage from PDA	3.0	3.6	4.1	V	
				0		mA	PDA and CMT LCD backlights OFF
			13		30	mA	PDA LCD backlight ON
			7		15	mA	CMT LCD backlight ON
3/X700	VBB	Regulated baseband voltage	2.7	2.8	2.85	V	
					300	µA	
42/X700	V17_i4	PDA LCD intermediate bias voltage	1.3	1.5	1.7	V	1/13xV17_OUT Throughout the whole temperature range
			1.4	1.5	1.6	V	At +20°C
43/X700	V17_i3	PDA LCD intermediate bias voltage	2.6	3.0	3.3	V	2/13xV17_OUT Throughout the whole temperature range
			2.9	3.0	3.2	V	At +20°C
44/X700	V17_i2	PDA LCD intermediate bias voltage	13.5	16.4	18.6	V	11/13xV17_OUT Throughout the whole temperature range
			15.4	16.4	17.4	V	At +20°C
45/X700	V17_i1	PDA LCD intermediate bias voltage	14.7	17.9	20.3	V	12/13xV17_OUT Throughout the whole temperature range
			16.8	17.9	19.0	V	At +20°C
47/X700	V17_OUT	PDA LCD bias voltage	16.0	19.4	22.0	V	Throughout the whole temperature range
			18.2	19.4	20.6	V	At +20°C

Pin / Conn.	Line Symbol	Parameter	Minimum	Typical / Nominal	Maximum	Unit	Notes
49/X700	V28_1	PDA LCD logic supply voltage	2.7	2.8	2.85	V	
				0.3	2.0	mA	
5,7,9,31, 34,36,38, 41,46,51/ X700	GND			0		V	

AC Characteristics

Pin / Conn.	Parameter	Minimum	Typical / Nominal	Maximum	Unit	Notes
6,7/ N700	Frequency	152	158	165	Hz	Differential measurement between the pins, NOT between pin and ground
	Peak–to–peak voltage	155	164	175	V	
	RMS voltage	58	63	70	V	
6,7/ N730	Frequency	148	156	168	Hz	Differential measurement between the pins, NOT between pin and ground
	Peak–to–peak voltage	160	164	170	V	
	RMS voltage	61	65	70	V	
X790, X791	Transmitter frequency	890		915	MHz	
	Receiver frequency	935		960	MHz	

Interface to BS1 PDA Module

Pin	I/O	Line Symbol	Parameter	Minimum	Typical / Nominal	Maximum	Unit	Notes
1		VPDA	Filtered battery voltage from PDA	3.0	3.6	4.1	V	
					0		mA	PDA and CMT backlights OFF
				13		30	mA	PDA LCD backlight ON
				7		15	mA	CMT LCD backlight ON
2	O	PWRKEYx	Power on key	0 0.7xVBB		0.3xVBB VBB	V	Low, Power key pressed High
3		VBB	Regulated baseband voltage	2.7	2.8	2.85	V	
						300	µA	

Pin	I/O	Line Symbol	Parameter	Mini-mum	Typical / Nominal	Maxi-mum	Unit	Notes
4	I	LCDRSTx	CMT LCD driver reset	0 0.7xVBB		0.3xVBB VBB	V	Low, Reset active High, Reset in-active
5		GND			0		V	
6	I	GENSDIO	CMT LCD driver serial data	0 0.7xVBB		0.3xVBB VBB	V	Low High
				0		4.0	MHz	
7		GND			0		V	
8	I	GENSCLK	CMT LCD driver bus clock	0 0.7xVBB		0.3xVBB VBB	V	Low High
				0	3.2	4.0	MHz	
9		GND			0		V	
10	I	LCDSCx	CMT LCD driver chip se-lect	0 0.7xVBB		0.3xVBB VBB	V	Low, Chip se-lected High, Chip un-selected
11	I	LCDCD	CMT LCD driver com-mand/data selection	0 0.7xVBB		0.3xVBB VBB	V	Low, Com-mand High, Data
12	I	APP_COL0	PDA function keyboard col-umn 0	0 0.7xVSY S		0.3xVSY S VSYS	V	Low High
13	I	APP_COL1	PDA function keyboard col-umn 1	0 0.7xVSY S		0.3xVSY S VSYS	V	Low High
14	I	APP_COL2	PDA function keyboard col-umn 2	0 0.7xVSY S		0.3xVSY S VSYS	V	Low High
15	I	APP_COL3	PDA function keyboard col-umn 3	0 0.7xVSY S		0.3xVSY S VSYS	V	Low High
16	O	APP_ROW0	PDA function keyboard row 0	0 0.7xVSY S		0.3xVSY S VSYS	V	Low High
17	O	APP_ROW1	PDA function keyboard row 1	0 0.7xVSY S		0.3xVSY S VSYS	V	Low High
18	I	COL0	CMT Key-board column 0	0 0.7xVBB		0.3xVBB VBB	V	Low High
19	I	COL1	CMT Key-board column 1	0 0.7xVBB		0.3xVBB VBB	V	Low High

Pin	I/O	Line Symbol	Parameter	Mini-mum	Typical / Nominal	Maxi-mum	Unit	Notes
20	I	COL2	CMT Key-board column 2	0 0.7xVBB		0.3xVBB VBB	V	Low High
21	I	COL3	CMT Key-board column 3	0 0.7xVBB		0.3xVBB VBB	V	Low High
22	I	COL4	CMT keyboard column 4	0 0.7xVBB		0.3xVBB VBB	V	Low High
23	O	ROW0	CMT keyboard row 0	0 0.7xVBB		0.3xVBB VBB	V	Low High
24	O	ROW1	CMT keyboard row 1	0 0.7xVBB		0.3xVBB VBB	V	Low High
25	O	ROW2	CMT keyboard row 2	0 0.7xVBB		0.3xVBB VBB	V	Low High
26	O	ROW3	CMT keyboard row 3	0 0.7xVBB		0.3xVBB VBB	V	Low High
27	I	CMT_BL_ON	CMT LCD and keyboard backlight en-able	0 0.7xVBB		0.3xVBb VBB	V	Low, backlight OFF High, backlight ON
28	I	PDA_BL_ON	PDA LCD backlight en-able	0 0.7xVSYS		0.3xVSYS VSYS	V	Low, backlight OFF High, backlight ON
29	I	LCDD3	PDA LCD data, leftmost pixel	0 0.8xVSYS		0.2xVSYS VSYS	V	Low High
30	I	LCDD2	PDA LCD data	0 0.8xVSYS		0.2xVSYS VSYS	V	Low High
31		GND			0		V	
32	I	LCDD1	PDA LCD data	0 0.8xVSYS		0.2xVSYS VSYS	V	Low High
33	I	LCDD0	PDA LCD data, right-most pixel	0 0.8xVSYS		0.2xVSYS VSYS	V	Low High
34		GND			0		V	
35	I	SCK	PDA LCD bus clock	0 0.8xVSYS		0.2xVSYS VSYS	V	Low High
				0	2.3	3.2	MHz	
36		GND	GND		0		V	

Pin	I/O	Line Symbol	Parameter	Mini-mum	Typical / Nominal	Maxi-mum	Unit	Notes
37	I	LC	PDA LCD line pulse	0 0.8xVSYS		0.2xVSYS VSYS	V	Low High
				0	13.6	20	kHz	
					870		ns	Pulse 'high' time
38		GND			0		V	
39	I	M	PDA LCD AC modulation	0 0.8xVSYS		0.2xVSYS VSYS	V	Low High
				0	1		kHz	
40	I	FRM	PDA LCD frame pulse	0 0.8xVSYS		0.2xVSYS VSYS	V	Low High
				0	67	100	Hz	
					75		μs	Pulse 'high' time
41		GND			0		V	
42		V17_i4	PDA LCD intermediate bias voltage	1.3	1.5	1.7	V	1/13xV17_OUT Throughout the whole temperature range
				1.4	1.5	1.6	V	At +20°C
43		V17_i3	PDA LCD intermediate bias voltage	2.6	3.0	3.3	V	2/13xV17_OUT Throughout the whole temperature range
				2.9	3.0	3.2	V	At +20°C
44		V17_i2	PDA LCD intermediate bias voltage	14.4	16.4	18.3	V	11/13xV17_OUT Throughout the whole temperature range
				16.1	16.8	17.4	V	At +20°C
45		V17_i1	PDA LCD intermediate bias voltage	15.8	17.9	19.9	V	12/13xV17_OUT Throughout the whole temperature range
				17.5	18.3	19.0	V	At +20°C
46		GND			0		V	
47		V17_OUT	PDA LCD bias voltage	17.1	19.8	21.6	V	Throughout the whole temperature range
				19.0	19.8	20.6	V	At +20°C

Pin	I/O	Line Symbol	Parameter	Mini-mum	Typical / Nominal	Maxi-mum	Unit	Notes
48	I	LCD_ON	PDA LCD enable	0 0.8xVSYS		0.2xVSYS VSYS	V	Low High
49		V28_1	PDA LCD logic supply voltage	2.7	2.8	2.85	V	
					0.3	2.0	mA	
50	O	LCD_TEMP	PDA LCD temperature	0.2	0.9	2.5	V	Voltage range throughout the whole temperature range
				0.88	0.90	0.91	V	At +25°C
51		GND			0		V	

Note: VSYS is PDA system voltage used in BS1 module, min. 2.75 V, typ. 2.80 V, max. 2.85 V.

Interface to BS8 CMT Module

Conn.	Parameter	Mini-mum	Typical / Nominal	Maxi-mum	Unit / Notes	Notes
X790, X791	Impedance		50		Ω	
	Transmitter frequency	890		915	MHz	
	Receiver frequency	935		960	MHz	
	Max. output power		2W (33 dBm)			

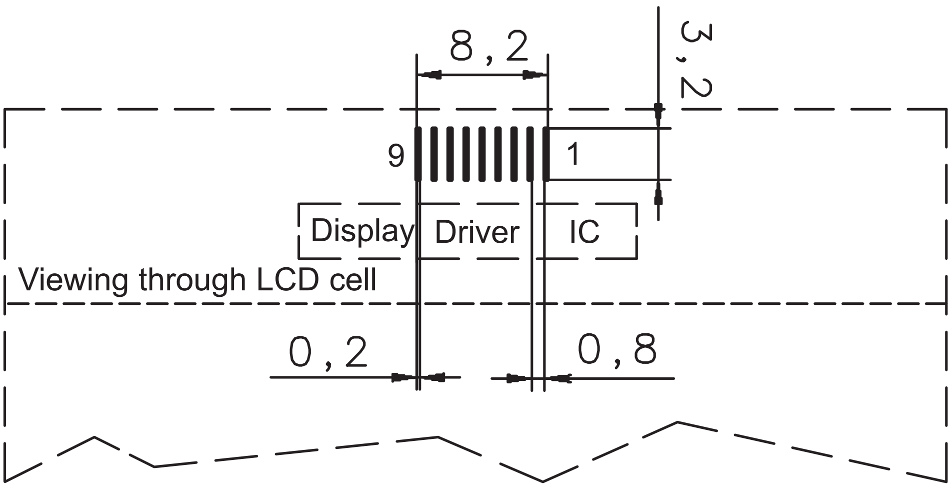
Interface to BC2 LCD Module

Pin	Line Symbol	Parameter	Mini-mum	Typical	Maxi-mum	Unit	Notes
1	VBB	Supply voltage	2.7	2.8	2.85	V	
					300	μA	
2	GENSCLK	Serial clock input	0	3.2	4.0	MHz	
			0		0.3xVBB	V	Low
			0.7xVBB		VBB	V	High
3	GENSDIO	Serial data input	0		0.3xVBB		Low
			0.7xVBB		VBB		High
4	LCDCD	Control/display data flag input	0		0.3xVBB		Low, Control
			0.7xVBB		VBB		High, Data
5	LCDCSx	Chip select input	0		0.3xVBB		Low, Chip selected
			0.7xVBB		VBB		High, Chip unselected

Pin	Line Symbol	Parameter	Mini-mum	Typical	Maxi-mum	Unit	Notes
6	OSC*	External clock for LCD	30.4	32.0	33.6	kHz	Connected to VBB on UI
7	GND	Ground		0		V	
8	VOUT	DC/DC voltage converter output		6.8	9		
9	LCDRSTx	Reset	0		0.3xVBB		Low, Reset Active
			0.7xVBB		VBB		High,Reset Inactive

* External oscillator is not used in BS2.

Connection layout diagram of interface to BC2 module



Interface to PDA LCD Display

Table 1. Interface to PDA LCD display, connector X730.

Pin	Line Symbol	Parameter	Minimum	Typical / Nominal	Maxi-mum	Unit	Notes
1 2	V17_OUT	PDA LCD bias voltage	16.0	19.4	22.0	V	Throughout the whole temperature range
			18.2	19.4	20.6	V	At +20°C
3	V17_i1	PDA LCD intermediate bias voltage	14.7	17.9	20.3	V	12/13xV17_OUT Throughout the whole temperature range
			16.8	17.9	19.0	V	At +20°C

Table 1. Interface to PDA LCD display, connector X730. (continued)

<table>
<tr><th>Pin</th><th>Line Symbol</th><th>Parameter</th><th>Minimum</th><th>Typical / Nominal</th><th>Maxi-mum</th><th>Unit</th><th>Notes</th></tr>
<tr><td rowspan="2">4</td><td rowspan="2">V17_i2</td><td rowspan="2">PDA LCD inter-mediate bias voltage</td><td>13.5</td><td>16.4</td><td>18.6</td><td>V</td><td>11/13xV17_OUT Throughout the whole tem-perature range</td></tr>
<tr><td>15.4</td><td>16.4</td><td>17.4</td><td>V</td><td>At +20°C</td></tr>
<tr><td rowspan="2">5</td><td rowspan="2">V17_i3</td><td rowspan="2">PDA LCD inter-mediate bias voltage</td><td>2.6</td><td>3.0</td><td>3.3</td><td>V</td><td>2/13xV17_OUT Throughout the whole tempera-ture range</td></tr>
<tr><td>2.9</td><td>3.0</td><td>3.2</td><td>V</td><td>At +20°C</td></tr>
<tr><td rowspan="2">6</td><td rowspan="2">V17_i4</td><td rowspan="2">PDA LCD inter-mediate bias voltage</td><td>1.3</td><td>1.5</td><td>1.7</td><td>V</td><td>1/13xV17_OUT Throughout the whole tempera-ture range</td></tr>
<tr><td>1.4</td><td>1.5</td><td>1.6</td><td>V</td><td>At +20°C</td></tr>
<tr><td>7</td><td>GND</td><td></td><td></td><td>0</td><td></td><td>V</td><td></td></tr>
<tr><td>8</td><td>GND</td><td></td><td></td><td>0</td><td></td><td>V</td><td></td></tr>
<tr><td>9</td><td>V28_1</td><td></td><td>2.7</td><td>2.8</td><td>2.85</td><td>V</td><td>PDA LCD logic supply voltage</td></tr>
<tr><td rowspan="3">10</td><td rowspan="3">FRM</td><td rowspan="3">PDA LCD frame pulse</td><td>0
0.8xVSYS</td><td></td><td>0.2xVSYS
VSYS</td><td>V</td><td>Low
High</td></tr>
<tr><td></td><td>70</td><td>100</td><td>Hz</td><td></td></tr>
<tr><td></td><td>75</td><td></td><td>μs</td><td>Pulse ’high’ time</td></tr>
<tr><td rowspan="3">11</td><td rowspan="3">SCK</td><td rowspan="3">PDA LCD bus clock</td><td>0
0.8xVSYS</td><td></td><td>0.2xVSYS
VSYS</td><td>V</td><td>Low
High</td></tr>
<tr><td>0</td><td>2.3</td><td>3.2</td><td>MHz</td><td></td></tr>
<tr><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td rowspan="2">12</td><td rowspan="2">M</td><td rowspan="2">PDA LCD AC modulation</td><td>0
0.8xVSYS</td><td></td><td>0.2xVSYS
VSYS</td><td>V</td><td>Low
High</td></tr>
<tr><td>0</td><td>2.5</td><td>3.4</td><td>kHz</td><td></td></tr>
<tr><td rowspan="3">13</td><td rowspan="3">LC</td><td rowspan="3">PDA LCD line pulse</td><td>0
0.8xVSYS</td><td></td><td>0.2xVSYS
VSYS</td><td>V</td><td>Low
High</td></tr>
<tr><td>0</td><td>32</td><td>44.5</td><td>kHz</td><td></td></tr>
<tr><td></td><td>870</td><td></td><td>ns</td><td>Pulse ’high’ time</td></tr>
</table>

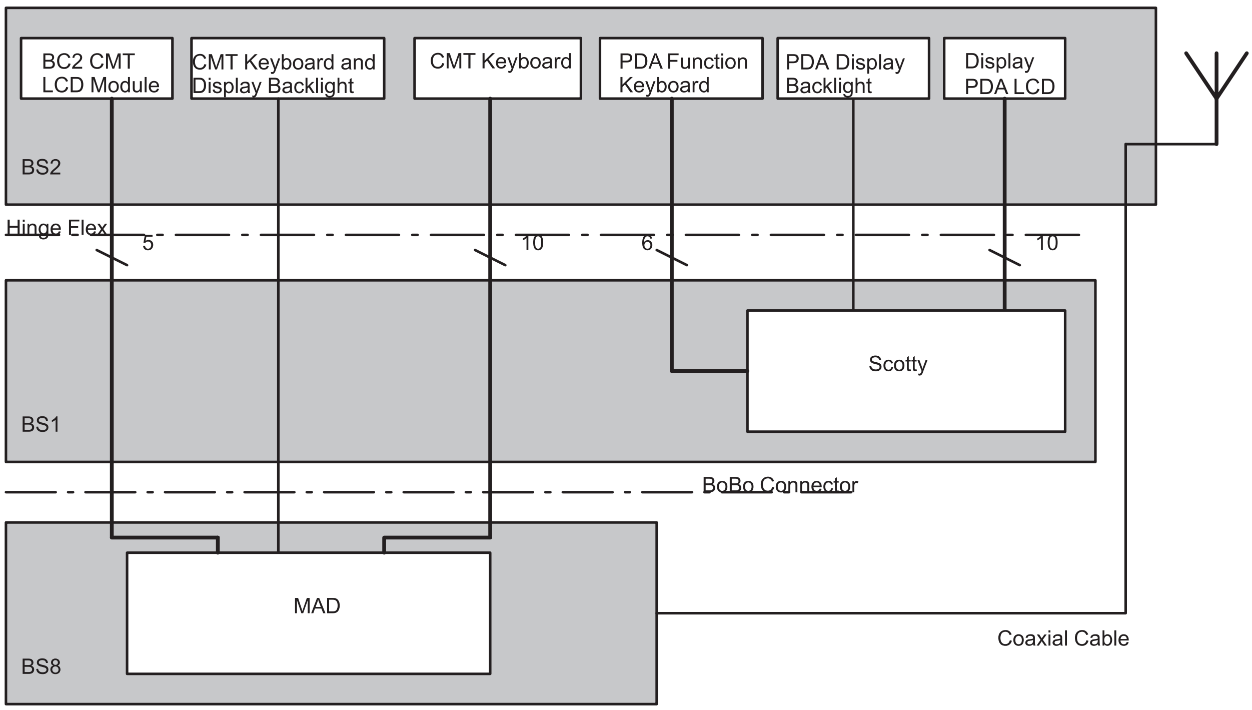
Table 1. Interface to PDA LCD display, connector X730. (continued)

Pin	Line Symbol	Parameter	Minimum	Typical / Nominal	Maxi-mum	Unit	Notes
14	LCD_ON	PDA LCD en-able	0 0.8xVSYS		0.2xVSYS VSYS	V	Low, Display OFF High, Display ON
15	LCDD3	PDA LCD data, leftmost pixel	0 0.8xVSYS		0.2xVSYS VSYS	V	Low High
16	LCDD2	PDA LCD data	0 0.8xVSYS		0.2xVSYS VSYS	V	Low High
17	LCDD1	PDA LCD data	0 0.8xVSYS		0.2xVSYS VSYS	V	Low High
18	LCDD0	PDA LCD data, rightmost pixel	0 0.8xVSYS		0.2xVSYS VSYS	V	Low High

Note: VSYS is PDA system voltage used in BS1 module, min. 2.75 V, typ. 2.80 V, max. 2.85 V.

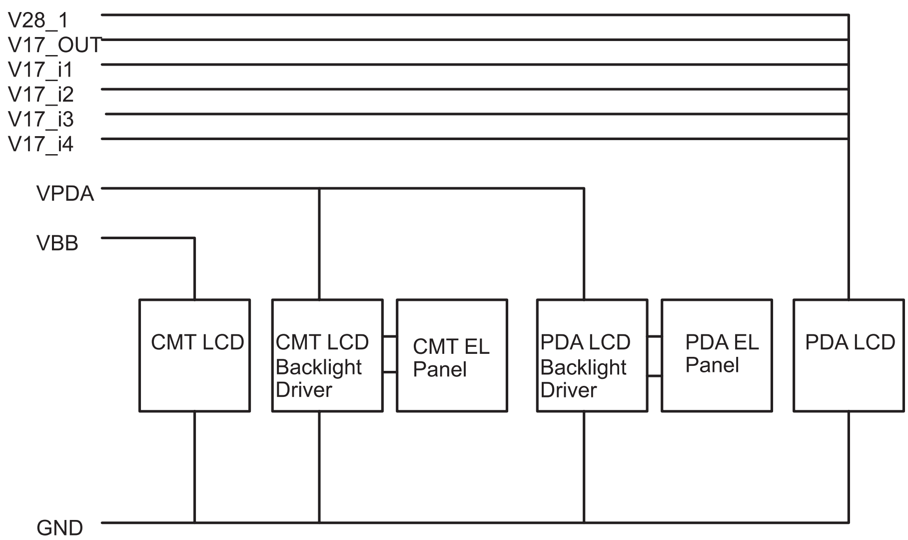
Signal number 1 is marked with a triangle in the connector X730.

Interconnection Diagram



Functional Description

Power Distribution Diagram



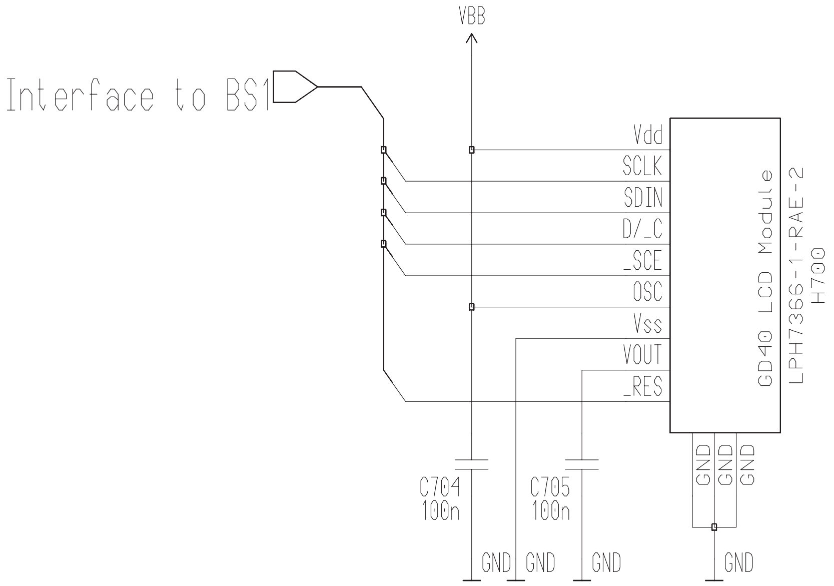
CMT LCD Display Circuit

The display circuit includes the LCD module BC2 and two capacitors. The LCD module uses COG (Chip On Glass) technology. The connection method for chip on the glass is ACF, Adhesive Conductive Film. The LCD module is electrically connected to UI board with gold wired elastomer. Two external capacitors are placed on UI PCB.

The display driver includes hw–reset, voltage tripler or quadrupler which depends on temperature, temperature compensating circuit and low power control. The driver includes a 84x48 RAM memory which is used for storing display data. The driver does not include character generator ROM. One bit in RAM is mapped directly to one pixel on display.

Main characteristics of the CMT LCD display:

– Display resolution:	84 x 48
– Viewing area:	34.96 x 23.50 mm
– Dot size:	0.31 x 0.37 mm
– Dot pitch:	0.345 x 0.405 mm
– Display type:	Transflective black and white FSTN



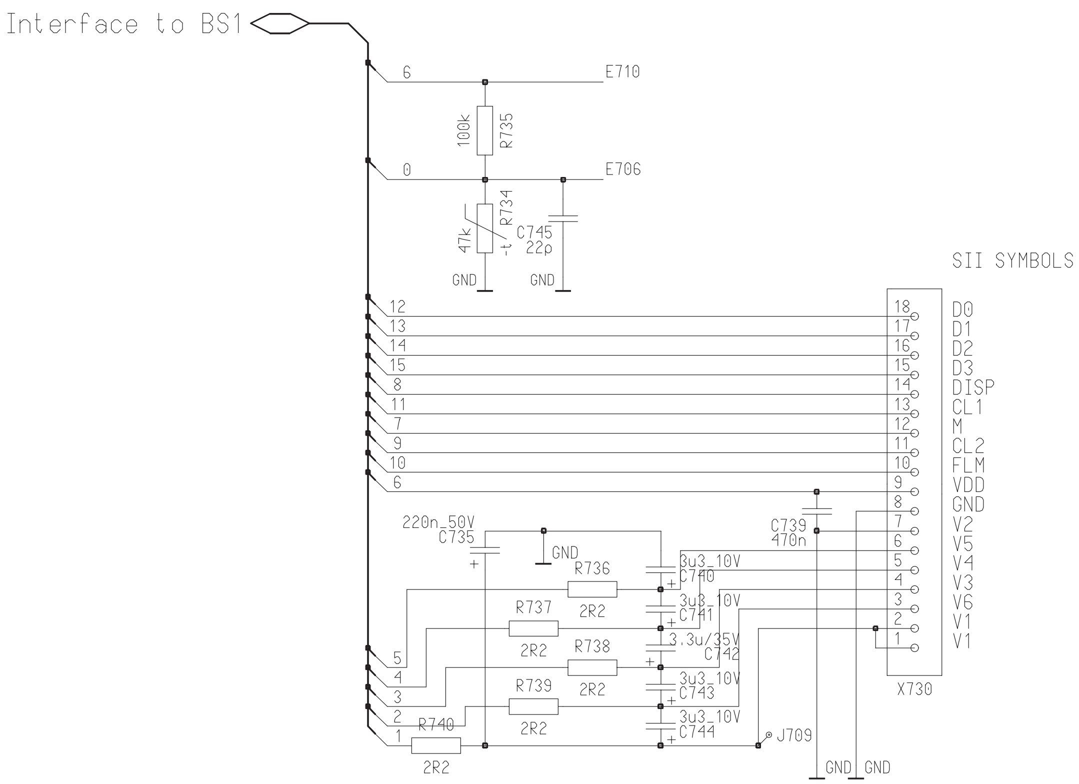
PDA LCD Display Circuit

The PDA LCD display circuit consists of the LCD display 4850049, logic and bias voltage filtering capacitors and an NTC resistor that is used to measure the temperature of the display. The voltage over the NTC is read by PDA SW via Phaser power supply ASIC and the information is used for contrast control of the display.

Main characteristics of the PDA LCD display:

– Display resolution:	640 x 200
– Viewing area:	111.8 x 37.0 mm
– Dot size:	0.16 x 0.16 mm
– Dot pitch:	0.17 x 0.17 mm
– Display type:	Transflective black and white FSTN

The PDA LCD interface is a typical black–and–white LCD interface with four data bits, pixel clock, line and frame pulse signals, AC modulation signal and enable signal. Logic and bias voltages are supplied by the Phaser power supply ASIC located in the PDA module.



Backlighting Circuit of CMT LCD And Keyboard

An electroluminescent (EL) panel is used for CMT LCD and keyboard backlighting. Electrically it can be considered as a capacitor. An inverter circuit is used to generate the high voltage AC to drive the EL panel. The inverter can be divided into two sections: power converter section and lamp driver section.

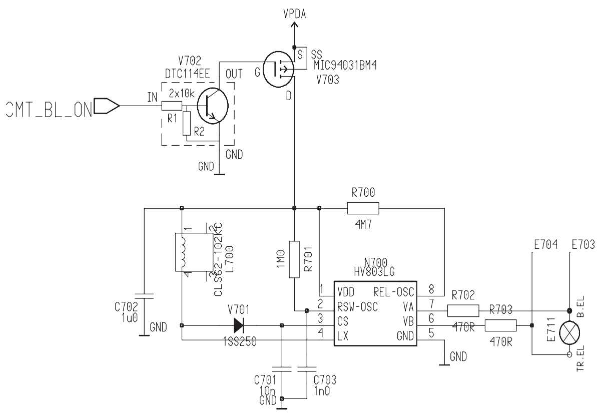
The power converter section employs a switch–mode converter to generate a voltage of maximum 90V. This voltage is connected to the EL panel through the lamp driver section, which changes the polarity of the output pins at a frequency that is set by one external resistor. Since the switch–mode converter's output is regulated to 90 volts at maximum, it is possible to achieve almost constant illuminance from the EL panel throughout the battery voltage range.

Connection between the EL panel and the PCB is a simple pressure contact. The frame of the CMT display module has two springs that press the EL panel against the pads on the PCB.

NOTE: The EL driver output voltage between pins 6 and 7 is over 150 V peak–to–peak. When making measurements, be sure that measuring equipment like oscilloscope, probe etc. have high enough voltage rating. There is no risk of getting a harmful or fatal electric shock due to low current driving capability of the inverter.

Table 2. CMT display illuminance measured with Tektronics J17 on the surface of the display lense.

Parameter	Minimum	Typical / Nominal	Maximum	Unit	Notes
Display illuminance	1.5		2.1	cd/m^2	Throughout the VPDA voltage range
	1.6	1.8	2.0	cd/m^2	VPDA = 3.5 V



PDA LCD Backlighting Circuit

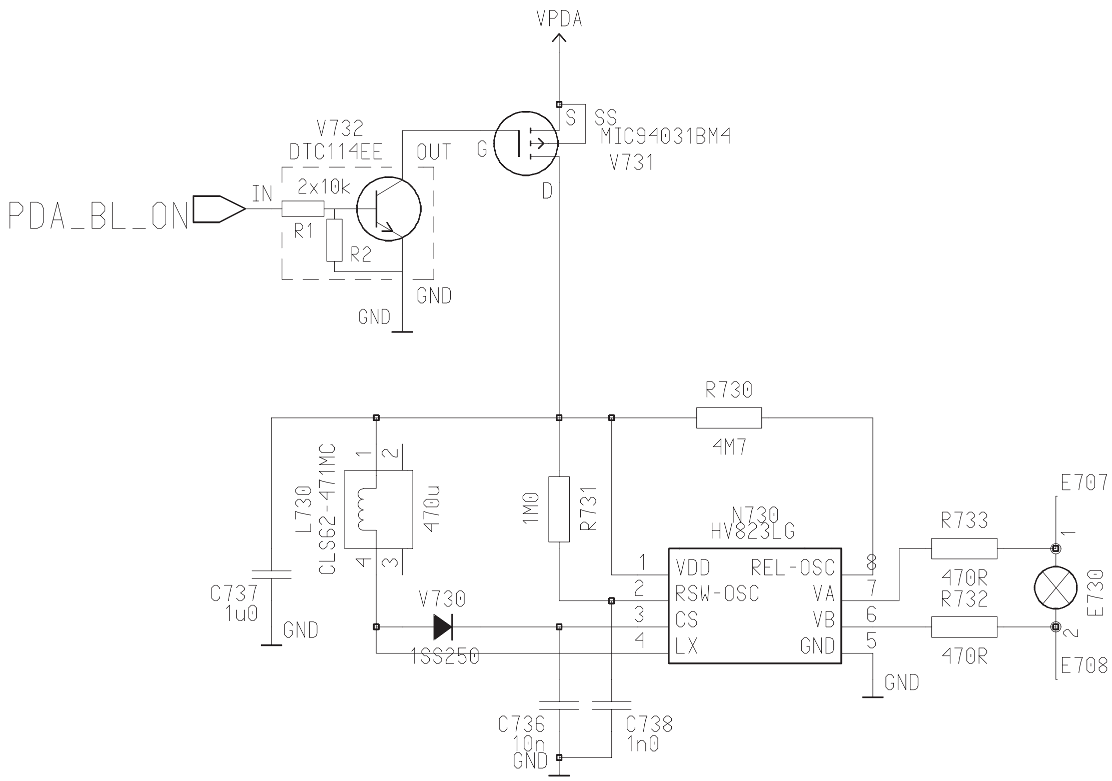
Electroluminescent (EL) panel is used for PDA LCD backlighting. The circuit is similar to the CMT keyboard and the display backlighting circuit, only some component values are different.

PDA display frame presses the EL panel contacts against the pads on PCB.

NOTE: The EL driver output voltage between pins 6 and 7 is over 150 V peak–to–peak. When making measurements, be sure that measuring equipment like oscilloscope, probe etc. have high enough voltage rating. There is no risk of getting a harmful or fatal electric shock due to low current driving capability of the inverter.

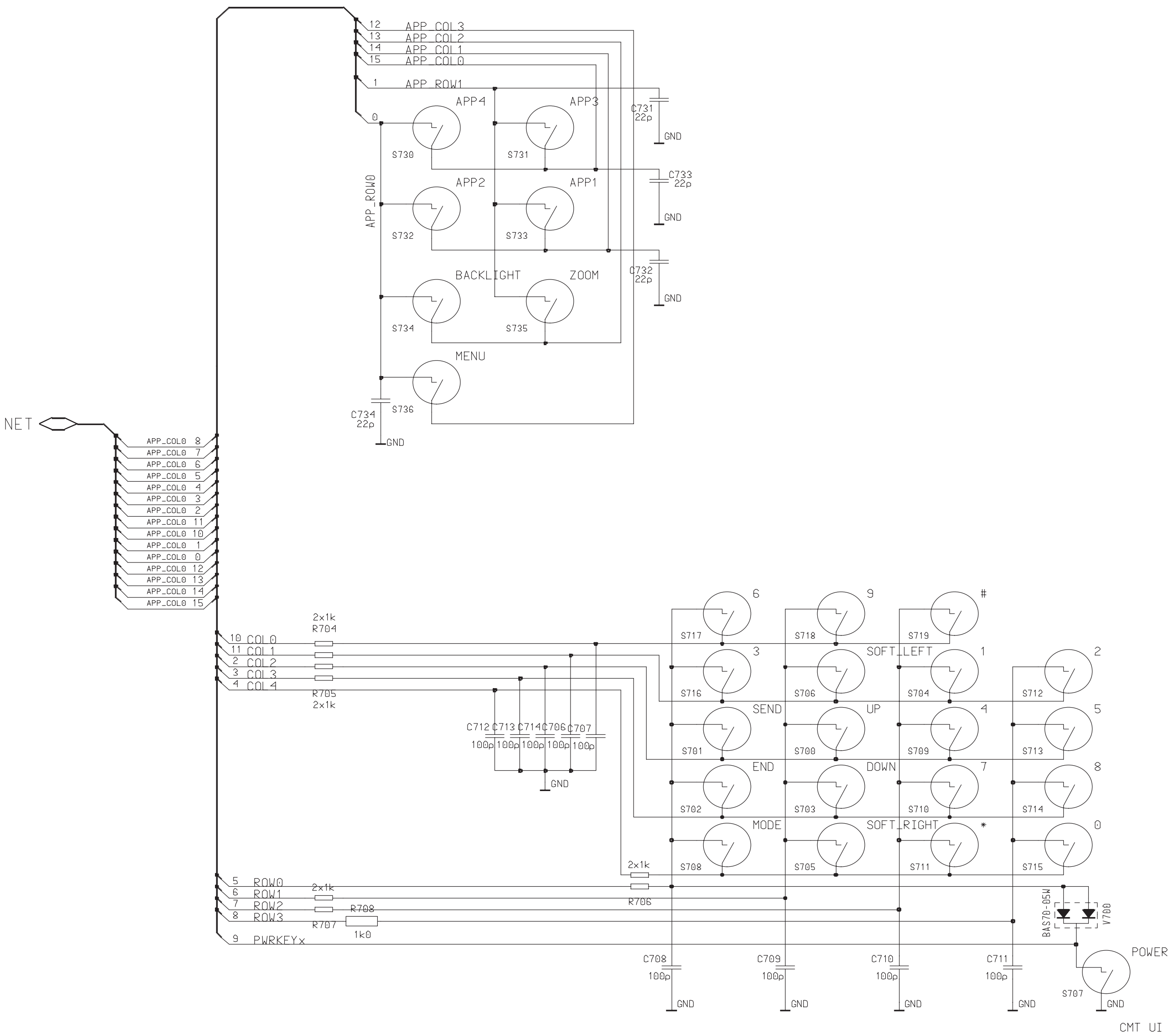
Table 3. PDA display illuminance measured with Tektronics J17 on the surface of the display.

Parameter	Minimum	Typical / Nominal	Maximum	Unit	Notes
Display illuminance	1.0		2.0	cd/m^2	Throughout the VPDA voltage range
	1.2	1.5	1.8	cd/m^2	VPDA = 3.5 V



PDA Function Keyboard And CMT Keyboard Circuit

There are 5 columns and 4 rows in the CMT keyboard matrix and 2 rows and 4 columns in the PDA function keyboard matrix. The power key is connected to the CMT row 0 through a diode, that prevents the POWER-KEYx line from being pulled down when the other keys are scanned. A normal keyboard scanning is used to read both matrices.



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Chapter 5

BS1 PDA Module

AMENDMENT RECORD SHEET

Amendment Number	Date	Inserted By	Comments
	02/99	OJuntune	Original

CONTENTS – PDA module BS1

Page No

Introduction

The function of the BS1 PDA module in RAE–2 Communicator device is to run all applications that utilize the PDA LCD display of the device. The GEOS operating system is applied on a 486 based PDA module platform. This processing platform utilizes the communicator–type user interface which is accessible when the RAE–2 is opened.

Technical Summary

The BS1 PDA module consists of a printed circuit board with a CPU, two kinds of memories, a Power unit, HF amplifier circuitry, and an IR–transceiver.

The PDA module is assembled on a single 8–layer printed circuit board. All components are assembled on one single side. The other side is reserved for keyboard keypads.

Serial ports, DMA– and LCD controller for timers are integrated in the CPU. The operating system is GEOS supplied by Geoworks.

The BS1 module includes three non–volatile Flash memories which are used for two kind of purposes. XIP (executed in place) memory is used for program file storage and RFD (resident flash disk) memory is writeable for user data.

One DRAM Memory is used for the code execution and for the volatile storage of the internal run–time system data.

Both memory types (DRAM and Flash) have their own address– and data bus, routed directly from the CPU.

Table 1. Used memory blocks

Memory type	Amount (Bytes)
Flash (XIP)	4M
Flash (RFD)	2M
DRAM	2M

The BS1 PWRU block regulates the PDA module power and controls the power-up and -down. After a battery has been connected, the PWRU gives the CPU system voltage and releases the reset as fast as possible after which the CPU SW has full power management control. The PWRU also generates and controls the voltages that the PDA LCD uses. The PDA has a rechargeable back–up battery which the PWRU block charges when the main battery is connected. The VBACK voltage is normally always available for real time clock. Power is fed from the battery through the CMT module to the PDA PWRU. The PWRU has a filter in battery line to reduce interference from the CMT module. The PWRU provides

A/D converter readings of the battery voltage and temperature via a parallel interface to the CPU. Many PWRU items can be controlled by register writing or directly via pin. The system voltage is always present until battery voltage drops below 3.0V.

Electronics

The following sections of circuitry are included on the BS1:

Function
PWRU Power supply unit
PDA CPU
IR transceiver
DRAM memory
Flash memory
HF Amplifier
QWERTY Keyboard pads

Interconnection Diagram

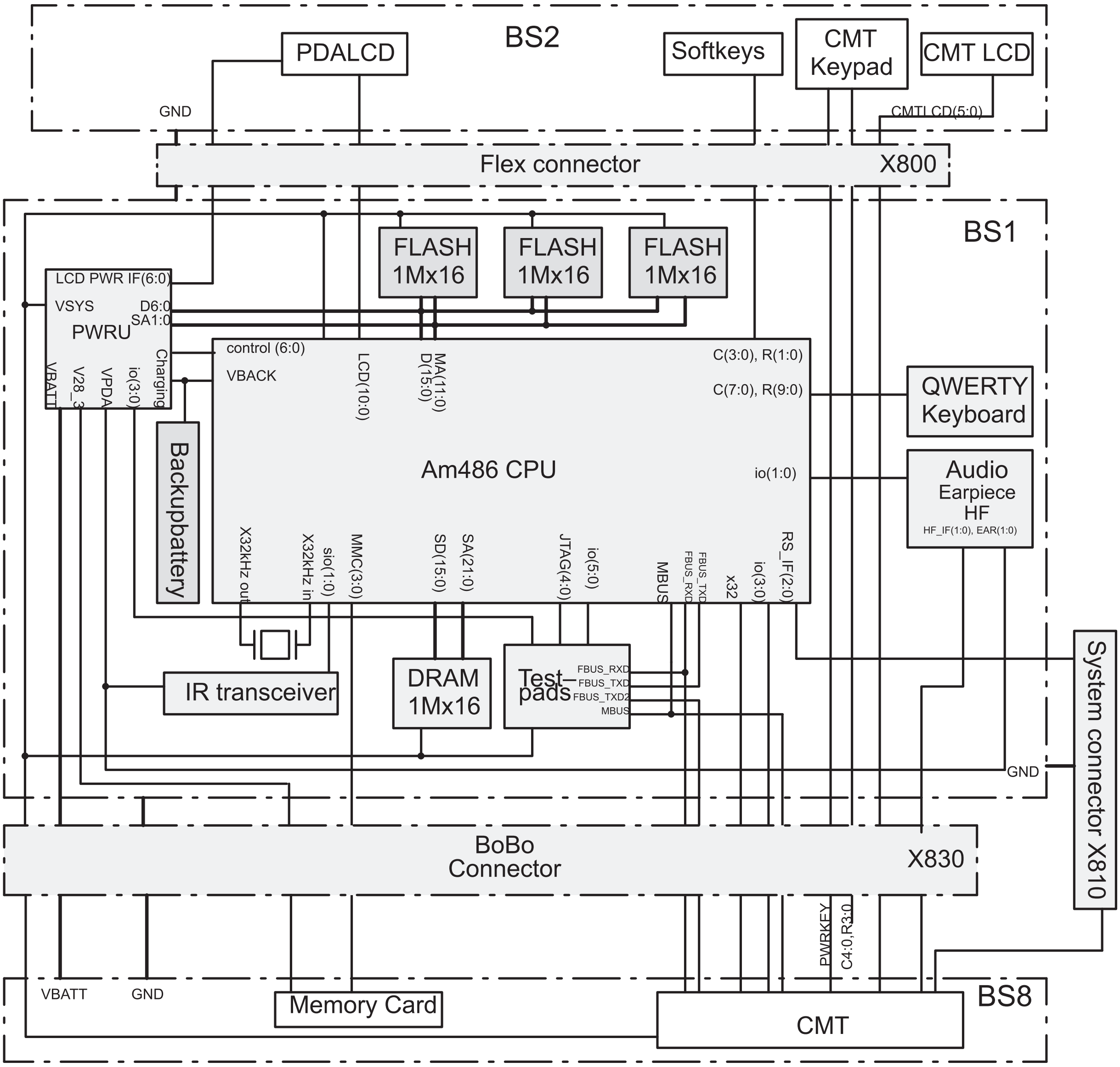


Figure 1. BS 1 PDA block in RAE–2 product

NOTE: All modules have same ground.

DC Characteristics

Table 2. **Supply Voltages and Power Consumption**

Pin / Conn.	Line Symbol	Minimum	Nominal	Maximum	Unit	Notes
1,2,3,4,5/ X830	VBATT	3.0	3.6	4.1	VDC	Battery voltage, SW limit
1,2,3,4,5/ X830				900	mA	Current
E307	VBACK	2.4	3.0	3.15	VDC	Backup battery voltage
		0.4	0.5	0.7	mA	Charge current
			0.25	0.4	mA	Quiescent current in suspend mode
E312	VSYS	2.75	2.8	2.85	VDC	System voltage
		0.050	300	450	mA	Current
E300	V17_OUT	17.1	19.4	21.6	VDC	LCD Biasing voltage, NOTE1
		19.0	19.8	20.6	VDC	LCD Biasing voltage, at +20C
			2	5	mA	Current
7/X800	V17_i1	15.8	17.9	19.9	VDC	LCD intermediate voltage1 (12/13xV17_OUT). NOTE1
		17.5	18.3	19.0	VDC	at +20C
				4	mA	Current
8/X800	V17_i2	14.4	16.4	18.3	VDC	LCD intermediate voltage2 (11/13xV17_OUT). NOTE1
		16.1	16.8	17.4	VDC	at +20C
				4	mA	Current
9/X800	V17_i3	2.6	3.0	3.3	VDC	LCD intermediate voltage3 (2/13xV17_OUT). Max range
		2.9	3.0	3.2	VDC	at +20C
				4	mA	Current
10/X800	V17_i4	1.3	1.5	1.7	VDC	LCD intermediate voltage4 (1/13xV17_OUT). NOTE1
		1.4	1.5	1.6	VDC	at +20C
				4	mA	Current

Table 2. **Supply Voltages and Power Consumption** (continued)

Pin / Conn.	Line Symbol	Minimum	Nominal	Maximum	Unit	Notes
3/X800	V28_1	2.70	2.80	2.85	VDC	LCD Logic voltage
			1	4	mA	Current
21/N450	V28_2	2.70	2.8	2.85	VDC	IrDA Logic voltage
			2	4	mA	Current
46/X830	V28_3	2.75	2.8	2.85	VDC	MMC supply voltage
		0.01	50	100	mA	Current
16/X830	VBB	2.75	2.8	2.85	VDC	Base Band operating voltage
					mA	Current

NOTE : Complete temperature range

AC Characteristics

	Minimum	Nominal	Maximum	Unit / Notes
External XTAL		32.768		kHz
			20	ppm, accuracy
CPU clock		33.18		MHz, Rise time 1–2ns
Memory bus clock		33.18		MHz, Rise time 2–3ns
Memory Controller clock		66.3552		MHz, Rise time 1–2ns
MMC clock during data	0.2592		8.294	Mhz, Rise time 2–3ns, NOTE1
MMC clock during identification		259.2		kHz, Rise time 2–3ns

NOTE: Frequency is a multiple of 259.2kHz

External Signals and Connections

This section describes the external electrical connection and interface levels on BS1 module. The electrical interface specifications are collected into tables that cover each connector and defined interface.

Table 3. List of Connectors and testpoints

Connector Name	Code	Notes
UI flex connector	X800	CMT/PDA LCD– and Keyboard signals
Board to Board connector	X830	CMT PDA interface
System connector pads	X810	

Table 3. List of Connectors and testpoints (continued)

Connector Name	Code	Notes
Audio connector pads	E880, E881, E850, E851	HF–speaker connection and earpiece connection
Backup battery holder	X451	
Testpads	E300–E315	Testpads ”under” battery pack
Frame connector pads	X840	Include manufacturing testpads. Is removed before assembly
Testpoints	J310, J400–J404, J430, J434, J435, J440 – J456, J497 – J499, J801, J803, J804, J808, J854, J880, J881	Testpoints around the BS1 PCB.

UI flex connector

The Interface between the BS2 and BS1 modules comprises a 51–pin flex connector. The connector includes supply voltage for the BS2 module, and required information signals. Signals from the BS8 module are also carried via the flex connector.

Table 4. UI flex Connector X800

Pin	I/O	Name	Function	Min	Nom	Max	Unit	Description / Note
1		GND	Global Ground					
2	I	LCD_TEMP	PDA LCD Temperature	0.2	0.9	2.5	VDC	Voltage range throught the whole temperature range.
				0.2	0.9	0.91	VDC	At +25°C
3	O	V28_1	PDA LCD Logic voltage	2.70	2.80	2.85	VDC	
4	O	LCD_ON	PDA LCD enable	2.30	2.8	2.85	VDC	High
					0	0.4	VDC	Low
5	O	V17_OUT	PDA LCD Biasing voltage	19.0	19.8	20.6	VDC	Range at +20C. Whole range can be seen from table2
6		GND	Global Ground					
7	O	V17_i1	PDA LCD Intermediate bias voltage	17.5	18.3	19.0	VDC	Range at +20C. Whole range can be seen from table2
8	O	V17_i2		16.1	16.8	17.4	VDC	
9	O	V17_i3		2.9	3.0	3.2	VDC	
10	O	V17_i4		1.4	1.5	1.6	VDC	
11		GND	Global Ground					

Table 4. UI flex Connector X800 (continued)

Pin	I/O	Name	Function	Min	Nom	Max	Unit	Description / Note
12	**O**	**FRM**	PDA LCD Frame pulse	2.30	2.80	2.85	VDC	High
					0	0.45	VDC	Low
					72	100	Hz	
							%	Duty cycle
13	**O**	**M**	PDA LCD AC Modulation	2.30	2.80	2.85	VDC	High
					0	0.45	VDC	Low
					2.5	3.4	kHz	
14		**GND**	Global Ground					
15	**O**	**LC**	PDA LCD Line pulse	2.30	2.80	2.85	VDC	High
					0	0.45	VDC	Low
					32	44.5	kHz	
16		**GND**	Global Ground					
17	**O**	**SCK**	PDA LCD bus clock	2.30	2.80	2.85	VDC	High
					0	0.45	VDC	Low
					2.3	3.2	MHz	
18		**GND**	Global Ground					
19	**O**	**LCDD0**	PDA LCD Data signal	2.30	2.80	2.85	VDC	High
					0	0.45	VDC	Low
20	**O**	**LCDD1**	PDA LCD Data signal	2.30	2.80	2.85	VDC	High
					0	0.45	VDC	Low
21		**GND**	Global Ground					
22	**O**	**LCDD2**	PDA LCD Data signal	2.30	2.80	2.85	VDC	High
					0	0.45	VDC	Low
23	**O**	**LCDD3**	PDA LCD Data signal	2.30	2.80	2.85	VDC	High
					0	0.45	VDC	Low
24	**O**	**PDA_BL_ON**	PDA LCD Backlight enabled	2.30	2.80	2.85	VDC	High, backlight enabled
					0	0.45	VDC	Low
25	**O**	**CMT_BL_ON**	CMT Backlight enabled	2.1	2.80	2.85	VDC	High, backlight enabled
					0	0.5	VDC	Low
26	**I**	**ROW3**	CMT Keys Row3, Lid closed, Base band powered	2.1	2.80	2.85	VDC	High
					0	0.5	VDC	Low
27	**I**	**ROW2**	CMT Keys Row2, Lid closed, Base band powered	2.1	2.80	2.85	VDC	High
					0	0.5	VDC	Low
28	**I**	**ROW1**	CMT Keys Row1, Lid closed, Base band powered	2.1	2.80	2.85	VDC	High
					0	0.5	VDC	Low
29	**I**	**ROW0**	CMT Keys Row0, Lid closed, Base band powered	2.1	2.80	2.85	VDC	High
					0	0.5	VDC	Low
30	**O**	**COL4**	CMT Keys Col4	2.1	2.80	2.85	VDC	High
					0	0.5	VDC	Low
31	**O**	**COL3**	CMT Keys Col3	2.1	2.80	2.85	VDC	High
					0	0.5	VDC	Low

Table 4. UI flex Connector X800 (continued)

Pin	I/O	Name	Function	Min	Nom	Max	Unit	Description / Note
32	**O**	**COL2**	CMT Keys Col2	2.1	2.80	2.85	VDC	High
					0	0.5	VDC	Low
33	**O**	**COL1**	CMT Keys Col1	2.1	2.80	2.85	VDC	High
					0	0.5	VDC	Low
34	**O**	**COL0**	CMT Keys Col0	2.1	2.80	2.8	VDC	High
					0	0.5	VDC	Low
35	**I**	**APP_ROW1**	PDA Application row1	2.0	2.80	2.85	VDC	High
					0	0.8	VDC	Low
36	**I**	**APP_ROW0**	PDA Application row0	2.0	2.80	2.85	VDC	High
					0	0.8	VDC	Low
37	**O**	**APP_COL3**	PDA Application col3	2.3	2.80	2.85	VDC	High
					0	0.45	VDC	Low
38	**O**	**APP_COL2**	PDA Application col2	2.3	2.80	2.85	VDC	High
					0	0.45	VDC	Low
39	**O**	**APP_COL1**	PDA Application col1	2.3	2.80	2.85	VDC	High
					0	0.45	VDC	Low
40	**O**	**APP_COL0**	PDA Application col0	2.3	2.80	2.85	VDC	High
					0	0.45	VDC	Low
41	**O**	**LCDCD**	CMT LCD driver command/ data selection	2.1	2.80	2.85	VDC	High, data
					0	0.5	VDC	Low, command
42	**O**	**LCDSCx**	CMT LCD driver chip select	2.1	2.80	2.85	VDC	High
					0	0.5	VDC	Low, chip selected
43		**GND**	Global Ground					
44	**O**	**GENSCLK**	CMT LCD driver bus clock	2.1	2.80	2.85	VDC	High
					0	0.5	VDC	Low
						4.0	MHz	
45		**GND**	Global Ground					
46	**O**	**GENSDIO**	CMT LCD driver serial data	2.1	2.80	2.85	VDC	High
					0	0.5	VDC	Low
						4.0	MHz	
47		**GND**	Global Ground					
48	**O**	**LCDRST**	CMT LCD Reset	2.1	2.80	2.85	VDC	High
					0	0.5	VDC	Low
49		**VBB**		2.7	2.8	2.85	VDC	
50	**I**	**PWRKEY**	CMT Power switch	2.1	2.80	2.85	VDC	Inactive state
					0	0.45	VDC	L(Pulse)=Power on/off, min 64ms
51		**VPDA**	Filtered battery voltage from PDA	3.0	3.6	4.1	V	
					0		mA	PDA and CMT backlights off
				40		65	mA	PDA LCD back-light ON
				10		20	mA	PDA LCD back-light OFF

Board to board connector signals

All interfaces from the BS8 module to the BS1 module are fed over a 50–pin board-to-board connector.

The function of the Interface is to transfer the battery voltage from the BS8 module, and transfer data between the BS8, BS2, and BS1 modules.

The signal definition and the most significant specifications of signals are collected in the next table.

Table 5. Board to board connector X830

Pin	I/O	Name	Function	Min	Nom	Max	Unit	Description / Note
1		**VBATT**	Battery Positive	3.0	3.6	4.1	V	Unregulated Battery Voltage
2				0.3		1000	mA	Current from BS8 module
3								
4								
5								
6	I	**XEAR**	Audio Output for Handsfree and Car Kit Use			500	mVpp	
7		**GND**	Global Ground					Reference for other signals
8	I	**BATTDET**	Battery Position Information	2.0	2.80	2.85	VDC	
				0	0	0.8	VDC	
9	I	**HFENA**	Internal Handsfree Amplifier Control	2.1	2.80	2.85	VDC	High, HF amplifier enabled
					0	0.5	VDC	Low, HF amplifier disabled
10		**EARP**	Earpiece Positive	50		223	mVpp	Differential signal
11		**EARN**	Earpiece Negative					
12		**GND**	Global Ground					
13	O	**PWRONx**	PDA start baseband to service Request State (SRS)	2.30	2.8	2.85	VDC	High
					0	0.45	VDC	Low, powering up the CMT
14	O	**32kHz**	Sleep clock for the CMT	2.30	2.8	2.85	VDC	high
					0	0.45	VDC	low
						12	mA	Maximum current for PDA
					32768		Hz	Pulse frequency
				20	50	80	%	Duty cycle
						1	%	Jitter
15		**GND**	Global Ground					
16		**VBB**	CMT System Power	2.7	2.8	2.85	VDC	Regulated CMT baseband voltage
						1	mA	Maximum current
17	O	**PWRKEYx**	CMT Power Switch	2.0	2.80	2.85	VDC	Inactive state
					0	0.45	VDC	L(Pulse)=Power on/off, min. 64ms

Table 5. Board to board connector X830 (continued)

Pin	I/O	Name	Function	Min	Nom	Max	Unit	Description / Note
18	I	CMT_BL_ON	CMT UI Light On	2.1	2.8	2.85	VDC	High, backlight enabled
					0	0.5	VDC	Low
19	O	ROW3	CMT Keys Row 3	2.5	2.8	2.85	VDC	High
					0	0.2	VDC	Low
20	O	ROW2	CMT Keys Row 2	2.5	2.8	2.85	VDC	High
					0	0.2	VDC	Low
21	O	ROW1	CMT Keys Row 1	2.5	2.8	2.85	VDC	High
					0	0.2	VDC	Low
22	O	ROW0	CMT Keys Row 0	2.5	2.8	2.85	VDC	High
					0	0.2	VDC	Low
23		GND	Global Ground					
24	I	COL4	CMT Keys Column 4	2.1	2.80	2.85	VDC	High
					0	0.5	VDC	Low
25	I	COL3	CMT Keys Column 3	2.1	2.80	2.85	VDC	High
					0	0.5	VDC	Low
26	I	COL2	CMT Keys Column 2	2.1	2.80	2.85	VDC	High
					0	0.5	VDC	Low
27	I	COL1	CMT Keys Column 1	2.1	2.80	2.85	VDC	High
					0	0.5	VDC	Low
28	I	COL0	CMT Keys Column 0	2.1	2.80	2.85	VDC	High
					0	0.5	VDC	Low
29		GND	Global Ground					
30	I	LCDCD	CMT LCD Command / Data Select	2.1	2.80	2.85	VDC	High, data
					0	0.5	VDC	Low, command
31	I	LCDRSTx	CMT LCD Reset	2.1	2.80	2.85	VDC	High
					0	0.5	VDC	Low, LCD reset
32	I	LCDCSx	CMT LCD Chip Select	2.1	2.80	2.85	VDC	High
					0	0.5	VDC	Low, chip selected
33		GND	Global Ground					
34	I	GENSCLK	CMT LCD and CCONT Serial Clock	2.1	2.80	2.85	VDC	High
					0	0.5	VDC	Low
					3.250		MHz	Pulse frequency in active state
35	I	GENSDIO	CMT LCD and CCONT Serial Data	2.1	2.80	2.85	VDC	High
					0	0.5	VDC	Low
					1.625		MHz	Maximum pulse frequency
36		GND	Global Ground					
37	O	FBUS_RXD	Fast Serial Data to CMT	2.30	2.80	2.85	VDC	High
					0	0.45	VDC	Low
38	I	FBUS_TXD	Fast Serial Data to PDA	2.1	2.80	2.85	VDC	High
					0	0.5	VDC	Low

Table 5. Board to board connector X830 (continued)

Pin	I/O	Name	Function	Min	Nom	Max	Unit	Description / Note
39		**GND**	Global Ground					
40	**I/O**	**MBUS**	Bidirectional Serial Bus	2.30	2.80	2.85	VDC	High, to the CMT
					0	0.45	VDC	Low, to the CMT
				2.1	2.80	2.85	VDC	High, from the CMT
					0	0.5	VDC	Low, from the CMT
41		**VSYS**	PDA System voltage	2.75	2.80	2.85	VDC	
						2	mA	
42	**O**	**LIDSWITCH**	Lid State Information	2.75	2.80	2.85	VDC	High, Cover open
					0		VDC	Low, Cover closed
					10		kohm.	Pull–up resistor
43	**I**	**MMC_SWITCH**	MMC Cover State Information	2.75	2.80	2.85	VDC	High, Cover open
					0		VDC	Low, Cover closed
44		**GND**	Global ground					
45	**I/O**	**MMC_CMD**	MMC Command / Address / Response, Bidirectional	2.30	2.80	2.85	VDC	Data to the card High, Pulled up with 10kohm resistor to MMC_VSYS in CMT Module
					0	0.45	VDC	Data to the Card Low
				2.1	2.80	2.85	VDC	data from the card High, Pulled up with 10kohm resistor to MMC_VSYS in CMT Module
						0.34	VDC	Data from the card Low
					259.3		kHz	frequency
46		**MMC_VSYS**	MMC Power Supply	2.75		2.85	VDC	
				0.01		100	mA	Current
47	**I/O**	**MMC_DATA**	MMC Bidirectional Data	2.30	2.80	2.85	VDC	Data to the Card High, Pulled up with 10kohm resistor to MMC_VSYS in CMT Module
					0	0.45	VDC	Data to the card Low
				2.1	2.80	2.85	VDC	Data from the Card High, Pulled up with 10kohm resistor to MMC_VSYS in CMT Module
					0	0.34	VDC	Data from the card Low
					8.294		MHz	frequency
48		**GND**	Global ground					

Table 5. Board to board connector X830 (continued)

Pin	I/O	Name	Function	Min	Nom	Max	Unit	Description / Note
49	**O**	**MMC_CLK**	MMC Clock	2.30	2.80	2.85	VDC	High
					0	0.45	VDC	Low
				0.2592		8.294	MHz	Frequency
50		**GND**	Global Ground					

System connector pads

The RAE–2 System connector is a multipurpose connector, which is shared with the BS8 module. In this section are described only the signals that are connected to the BS1 module. These signals are needed for PC–connectivity. The connector comprises spring type contacts to the BS1 and BS8 module. The PCB comprises pads on which the springs are pressed.

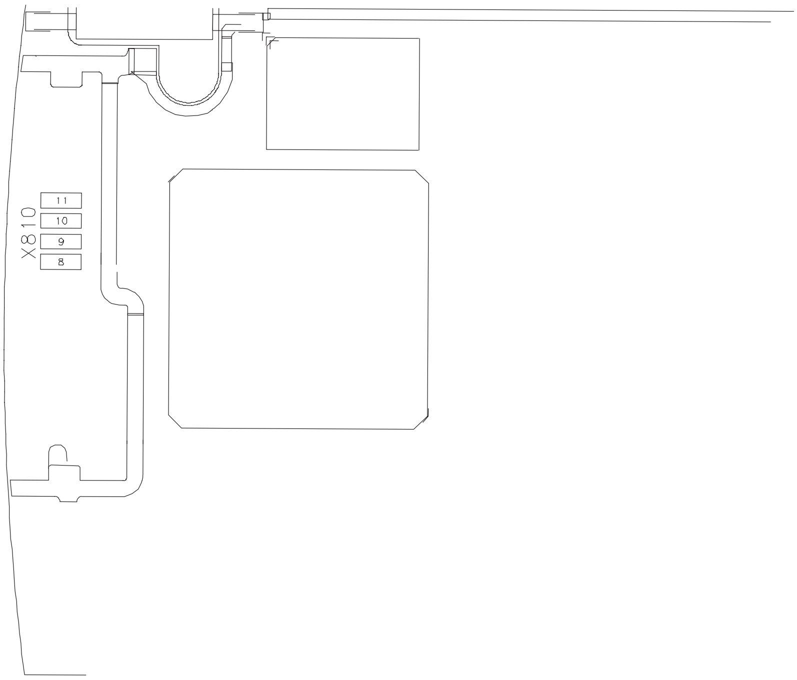


Table 6. System Connector pads X810

Pin	Line Symbol	Parameter	Minimum	Nominal	Maximum	Unit	Unit / Notes
8	**DCT_TX**	PDA CPU Receive data	2.0	2.80	2.85	VDC	
			0		0.8	VDC	
9	**DCE_RX**	PDA CPU Transmit data	2.30	2.80	2.85	VDC	
			0		0.45	VDC	
10	**DCE_DTR**	PDA CPU Data set ready	2.0	2.80	2.85	VDC	
			0		0.8	VDC	
11	**GND**	Global ground					

Audio connector pads

The audio connector has two contact types. The earpiece contacts are of spring type, and the contacts for the handsfree speaker are elastomeric contacts.

Table 7. Audio connector pads

Pin	Line Symbol	Parameter	Minimum	Nominal	Maximum	Unit	Unit / Notes
E850	**EARP**	Earpiece positive node	50		223	mVpp	Differential voltage between EARP and EARN nodes
E851	**EARN**	Earpiece negative node					
E880	**PHFEARN**	Handsfree speaker negative node			6.0	Vpp	VBATT=4.4V. Differential voltage between PHFEARN and PHFEARP nodes
					4.4	Vpp	VBATT=3.6V. Differential voltage between PHFEARN and PHFEARP nodes
E881	**PHFEARP**	Handsfree speaker positive node			6.0	Vpp	VBATT=4.4V. Differential voltage between PHFEARN and PHFEARP nodes
					4.4	Vpp	VBATT=3.6VBATT=4.4V. Differential voltage between PHFEARN and PHFEARP nodes.

Backup battery

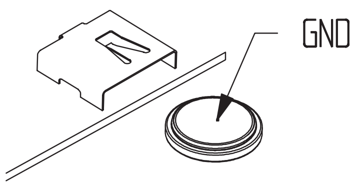


Figure 2. Backup battery insertion direction

NOTE: Positive node is against PCB, it can be identified by 2mm diameter contact plate

Table 8. Backup battery holder X450

Pin	Name	Function	Min	Nom	Max	Unit	Description / Note
	VBACK	Backup battery voltage	2.4	3.0	3.1	VDC	
	GND	Global ground					

Internal Signals and Connections

Table 9. IR–transceiver (N300) signals

Pin	Line Symbol	Parameter	Minimum	Nominal	Maximum	Unit / Notes
3	**TXD**	Transmit data from CPU	2.30V	2.80V	2.85V	
				0V	0.45V	
4	**RXD**	Receive data to CPU	2.0V	2.8V	2.85V	
				0	0.8V	

Table 10. Signals between PDA CPU and Flash memories

Name	Function	Min	Nom	Max	Unit	Description / Note
SA(21:1)	System address	2.30	2.80	2.85	VDC	High
			0	0.4	VDC	Low
SD(15:0)	System data from CPU	2.30	2.8	2.85	VDC	High
			0	0.4	VDC	Low
	System data from memory	2.40	2.8	2.85	VDC	High
			0	0.4	VDC	Low
ROMCS(2:0)	Chip selects for Flash memories	2.30	2.80	2.85	VDC	High
			0	0.4	VDC	Low
FLSHWRx	Flash write signal	2.30	2.80	2.85	VDC	High
			0	0.4	VDC	Low, write enabled
ROMRDx	Flash read signal	2.30	2.80	2.85	VDC	High
			0	0.4	VDC	Low, read enabled
GPIO_CS1	Write protect for RFD memory	2.30	2.80	2.85	VDC	High
			0	0.4	VDC	Low, powered down
GPIO_CS7	RFD Flash ready	2.0	2.80	2.85	VDC	High, ready
			0	0.8	VDC	Low, busy

Table 11. Signals between PDA CPU and DRAM Memory

Name	Function	Min	Nom	Max	Unit	Description / Note
MA(11:0)	Memory address	2.30	2.80	2.85	VDC	High
			0	0.4	VDC	Low
SD(15:0)	Memory data from CPU	2.30	2.8	2.85	VDC	High
		0	0	0.4	VDC	Low
	Memory data from memory	2.0	2.8	2.85	VDC	High
		0	0	0.6	VDC	Low
RAS0	Row access strobe	2.30	2.80	2.85	VDC	High
			0	0.4	VDC	Low
CAS(1:0)	Column access strobe	2.30	2.80	2.85	VDC	High
			0	0.4	VDC	Low
MWEx	Memory write enable	2.30	2.80	2.85	VDC	High
			0	0.4	VDC	Low, write enabled

Table 12. Signals between PDA CPU and PWRU

Name	Function	Min	Nom	Max	Unit	Description / Note
SA(2:0)	System address	2.30	2.80	2.85	VDC	High
			0	0.4	VDC	Low
SD(6:0)	System data	2.40	2.8	2.85	VDC	High
			0	0.4	VDC	Low
CS3x	Chip select for Phaser	2.30	2.80	2.85	VDC	High
			0	0.4	VDC	Low
IOWx	Phaser write signal	2.30	2.80	2.85	VDC	High
			0	0.4	VDC	Low, write enabled
IORx	Phaser read signal	2.30	2.80	2.85	VDC	High
			0	0.4	VDC	Low, read enabled
RESETx	Reset for CPU, and for Flash memories.	2.30	2.80	2.85	VDC	High
			0	0.4	VDC	Low
VBACK	Back–up battery voltage	2.40	3.0	3.1	VDC	High
V17_EN	LCD bias voltage enable	2.30	2.80	2.85	VDC	High
			0	0.4	VDC	Low
V28_1EN	LCD logic voltage enable	2.30	2.80	2.85	VDC	High
			0	0.4	VDC	Low

Functional Description

Power Unit

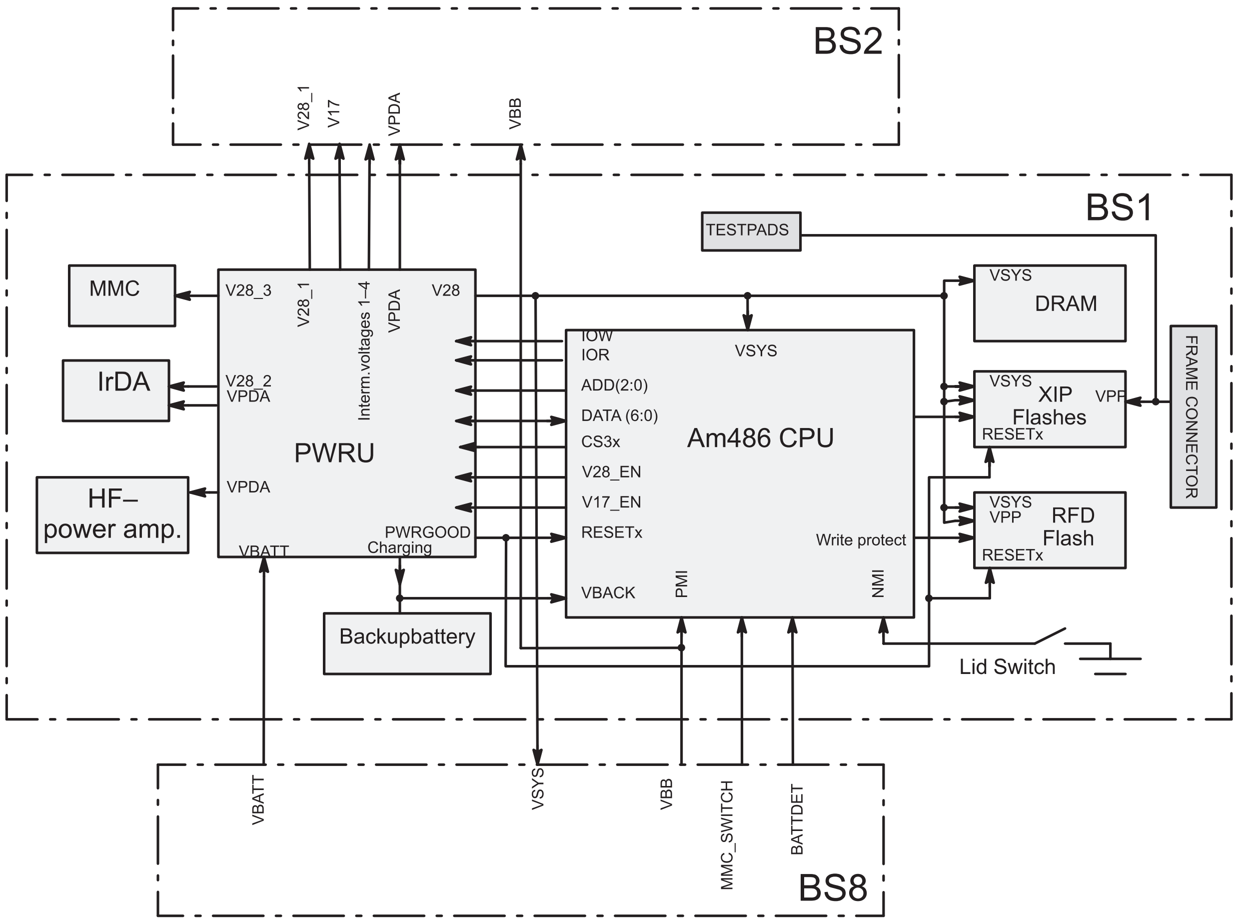


Figure 3. PDA Power distribution diagram

Battery voltage is supplied from the BS8 module through a board to board connector. In the BS1 module the battery voltage is filtered and then supplied to the Phaser, IR–transceiver circuit, BS2 module, and PHF–speaker circuitry.

The phaser generates internally the system voltage V28, switched voltages V28_1 ,V28_2, V28_3, the LCD bias voltage V17, the LCD intermediate voltages V17_ix, x=1–4 and the backup battery charging voltage VBACK.

When the battery voltage level is adequate, the PWRU switches V28 on and after a certain time releases the reset–signal for the CPU. The CPU controls the LCD, MMC, and IR–transceiver logic voltages by writing command to the PWRU register. Optionally the CPU can control the LCD logic- and biasing voltage directly by means of I/O signals.

The backup battery supplies power to the CPU's real time clock. The PWRU charges the backup battery when the main battery is connected. The CPU puts the Flash memories to power down mode when they are not used.

The BS8 signal BATTDET is a warning signal that the battery will be removed soon, when power down procedure is started. VBB is the supply voltage for the CMT display, located in the BS2 module, and the VBB provides information for the BS1 CPU whether the CMT powered or not and it enables the keyboard buffer. The MMC_SWITCH indicates that the MMC card will be removed, when the CPU controls the Phaser to turn the V28_3 off.

Input filter

The Battery voltage is fed from the BS8 module and then filtered by using a LC–lowpass filter, after filtering the voltage is named VPDA. The VPDA is then fed to the PWRU, the IR–transceiver, the PHF–speaker circuitry, and to the BS2 module.

Linear regulator V28

System voltage V28 is generated by a linear regulator. V28 stays on all the time when the battery voltage is higher than cutoff limit.

Linear regulator V28_1,_2,_3

These regulators are controlled by the CPU. The CPU can enable these regulators by writing a command to the PWRU's register. V28_1 is the switched V28 and is used for the LCD logic. V28_2 is the switched V28 and is used for the IRDA logic. V28_3 is the MMC voltage.

Switchmode regulator V17

The LCD bias voltage V17 is generated by a step–up DC–DC converter. The control scheme is the current limited pulse width modulation (PWM). The switching transistor is internal. The regulator output, too, is separated from the battery line by an integrated switch transistor between the regulator output and load.

Backup battery

The Real time clock is kept running by a backup battery only when the main battery is not connected. At the nominal RTC load used , the 12mAh capacity of the backup battery provides about 40 days of RTC operation when the main battery is not connected. The backup battery is rechargeable. It is charged by the Phaser VBACK regulator using 0.5mA current when the main battery is connected.

Reset and power management

The Phaser is connected to the I/O space of the H3 by using a 7 bit wide data bus and a 3 bit wide address bus. The BS2 PDAPWRU on the PDA board supplies two different voltage levels to the system;
2.85V is used as the main operating voltage for all circuits and
about 19V that is needed for the LCD bias (V17). The LCD bias voltage is used to adjust the contrast ratio of the LCD screen. The LCD bias voltage is controlled by the Phaser ASIC.

The V17 and V28_1 ON/OFF are switched by the Phaser, but optionally also the CPU can control these signals directly with HW means, independently of the SW controlled register settings. The phaser provides also the POWERGOOD signal for the CPU. The system reset circuit is part of the power supply. When the battery voltage is higher than 3.4V a PWRGOOD is generated for the CPU. The reset circuit also asserts the reset signal whenever the Vcc supply voltage declines below the threshold, keeping it asserted for at least 50ms after Vcc has risen above the reset threshold. The reset circuit is designed to ignore fast transients ($t < 64\mu s$) in Vcc.

There is an undervoltage lockout (UVLO) block inside the Phaser. Below the threshold limit the comparator shuts down all Phaser functionality to prevent the battery from overdischarge. Otherwise the VSYS regulator current drains the battery when left unused for long period. After the UVLO there is only reference block in the Phaser drawing current from the battery. The UVLO has a little hysteresis and is cancelled when the battery voltage has risen to 2.7V. However, reset to the CPU is given only when battery voltage rises to 3.45V. This in order to avoid unsuccessful power–ups. When the lockout voltage level is reached, the battery voltage rises because the load is removed.

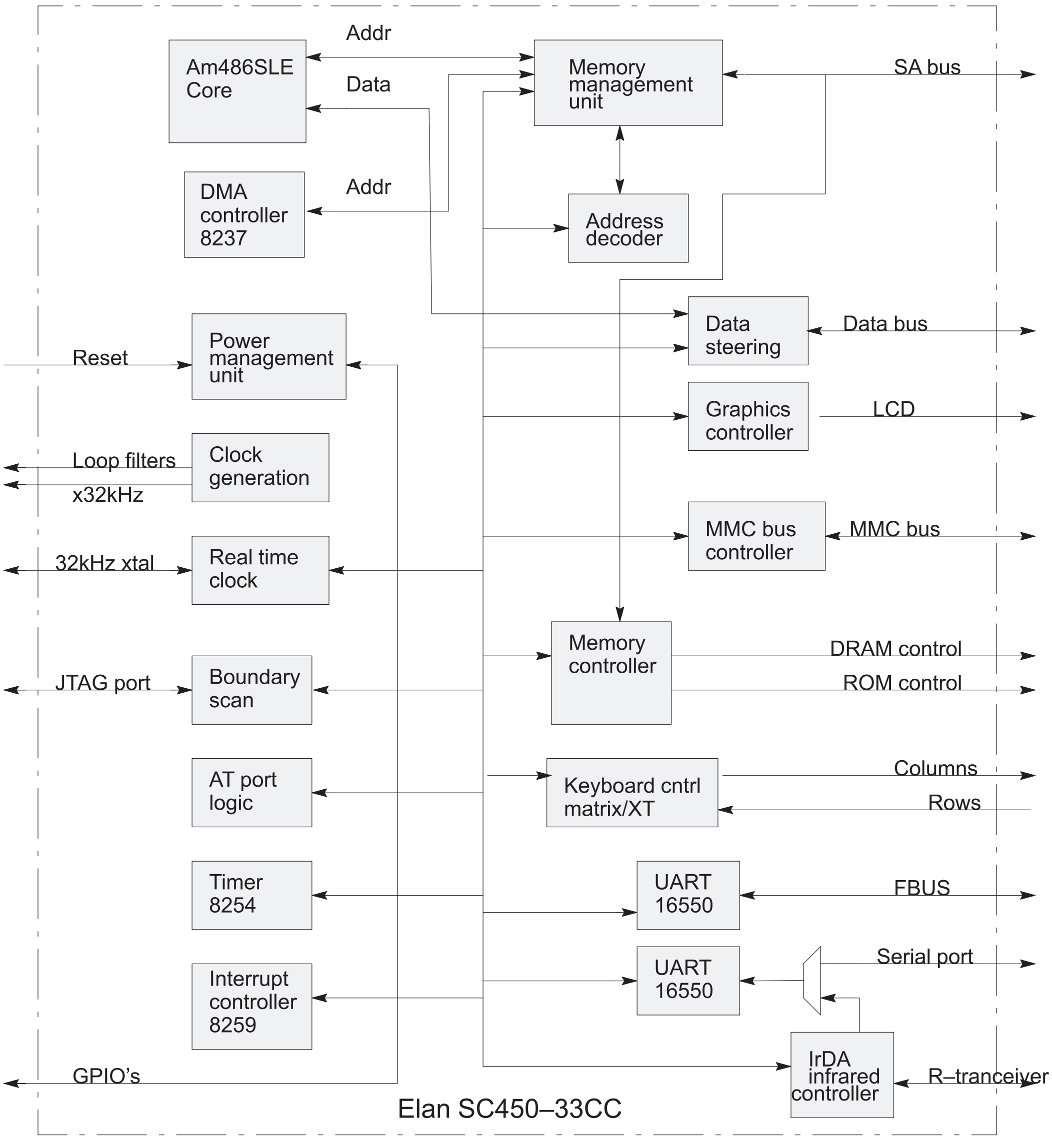
PDA CPU

The PDA CPU is a SC450–33CC in a 256 pin plastic ball grid array package.

The core features a 32–bit architecture with internal 8k write–back cache. The clock rate is 33MHz, which can be slowed down to1MHz. The default clock rate on reset is 8.29MHz. The bus clock rate is 33MHz. A 32kHz clock signal for the BS8 module is provided by the CPU PLL circuit. The clock signal is started when ever the system voltage is applied to the CPU.

The CORE starts when the reset signal is provided and then it begins to execute the program code from the Flash memory. The external pull–up resistor controls the start–up procedure (Boot code Chip select, and data bus width).

The memory controllers are integrated to the chip. A ROM controller is used for Flash interface and a DRAM controller supports extended data out (EDO) page mode DRAMs. Both memory types (DRAM and Flash) have their own address and data bus routed directly to the CPU. The power unit is controlled via an I/O-mapped 7-bit wide data- and 3-bit wide address bus, which is shared with Flash data- and address bus. The CPU block diagram is the figure below.



For serial interface two UART circuits are used. UART2 is a serial interface reserved for data transfer between the BS1 and BS8 modules. UART2 is disabled or enabled according to the CMT voltage. UART1 is used for RS–232 interface with external level changer. The UARTs can be connected together to establish Re–Link connection, where received data is directly linked to the UART's transmit data pin. That way the BS8 module can be programmed by using an external RS-interface. Autobauding detection circuitry is included in the UART1 block.

The LCD–controller supports a 4-bit data and 16-grey shades. The display control signals are routed from the CPU. The bigger (640x200) LCD is located in the lid. The interconnection between the CPU and the LCD comprises a flex through the hinge. Data and control signals are provided by the CPU. The required voltages are supplied by the PWRU.

The PDA CPU supports a synchronous serial interface that is compatible with the Multimedia Card Bus (MMC) Protocol. The MMC is changeable Flash or ROM memory card with variable memory size. The MMC connector is located on the BS8 Module. MMC signals are routed to the BS8 module through a Board to board connector. The interface consists of three pins: one clock(output), one command/response (bidirectional), and one data pin (bidirectional). The controller is capable up to 8Mbits/second transfer rate.

The keyboard controller includes a matrix keyboard which is used for PDA keyboard and for PDA lid keys.   The PC/AT standard core includes a 8254 programmable interval timer, two 8259 programmable interrupt controllers, and a real time clock. The CPU's general purpose input/outputs (GPIO) are controlled by the CPU's registers.

I/O Signals

In the Table 13 below are listed BS1 module I/O signals which are mapped to general purpose pins of the CPU.

Table 13. Spock CPU Controllable I/O Signals

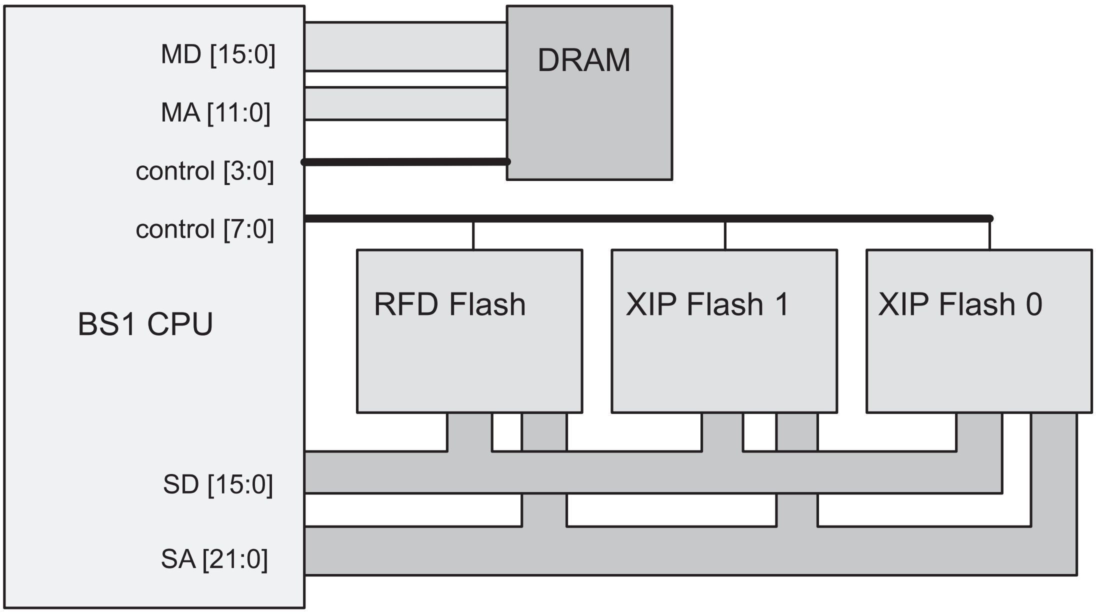
Scotty Pin	Signal Name	Low	High	Note
GPIO_CS1	RFD_WPx	Write operation	Write not possible	
GPIO_CS2	XIP_STS	Memory busy	Memory ready	Input, CS(1:0) Flash memory status
GPIO_CS5	TESTMODEx	Testmode activated	Reset, Suspend, Operation	Input.
GPIO_CS6	PWRONx	Powering the CMT up	Reset, Suspend	Activate the power on procedure for the CMT
GPIO_CS7	Flash_RDY	Flash performing an internal operation	Flash ready for new command	Input. Open drain output, processor's internal pull–up is used. (Only for the RFD)
GPIO_CS8	MMC_Switch	MMC cover closed	Reset, MMC cover open	Input. MMC cover status indication
GPIO_CS9	MBUS			Output during BS8 Flashing from BS1 module, Input otherwise.
GPIO_CS11	Phaser_CSx	Chip Selected	Chip not selected	Output.
GPIO_CS12	VBB	CMT off	Reset, CMT on	Input.
GPIO_CS13				
GPIO16	LCDBL_EN	Reset, Suspend, BL disabled	Backlight activated	Backlight EL driver controller.
GPIO18	BZR_EN	Reset, Suspend	Operation	Enables the PA.
BL1	BATTDET	Battery connected	Battery removed	Indicates when the battery is going to be removed. Pin has build in 15ms debounce
SUS/RES	LIDSWITCH	Cover closed	Cover open	STI. Indicates when the coved is open or closed

Table 13. Spock CPU Controllable I/O Signals (continued)

LVDD	LVDD	Reset, Suspend	PDA LCD Logic voltage activated	Routed to the Phaser
LVEE	LVEE	Reset, Suspend	PDA LCD bias voltage activated	Routed to the Phaser

Memories

The memory units of the module are connected to the CPU via a 16–bit wide data bus. Both memory types (DRAM and Flash) have an own data– and address bus.



DRAM memory

The 1Mx16bit DRAM is connected to the CPU with a dedicated 16–bit wide data- and 12-bit wide address bus. The DRAM type used is the extended data out (EDO) DRAM with 60ns access time, and self–refresh capability. DRAM is packaged in a 5.55mmX9.10mm, 40–ball uBGA package.

When the DRAM is driven by the CPU, no wait states is needed.

Flash memory

Three 1Mx16bit Flash memory devices are used for non–volatile memory. The Flash type features a 120ns access time. The Flash is packaged in 8mmX11mm 64–ball CSP package. When the Flash is read by the CPU, 4 wait states are needed to ensure proper timing.

External Serial Interface

The UART1 External serial interface is used for PC–connectivity. The RS–connection is provided by a 3–signal interface (RXD,TXD, and DTR) which is routed to the system connector. Maximum data rate is 230.4kbps.

The re–link feature connects the UART1 and the UART2 (FBUS) internally together. This provides the signal routing from the system connector to the CMT.

The Autobaud detection circuitry can detect bit rates from 300 bps tp 115.2kbps. The autobaud state machine starts when enabled by the CPU. The bit rate measurement begins on the first negative edge of the CPU_RXD line. After detecting the start bit width, and therefore the bit rate, the remainder of the incoming data stream is sampled at this rate.

This UART is shared with the IrDA circuitry and thus only one of them can be used at a time.

IR–Transceiver

The IR–transceiver controller is shared with the UART1. Infrared data transfer is started with 9600bps and then the data rate is increased to 115.2kbps if the connected device supports higher speed. The protocol is the standard one of the Infrared Data Association. The CPU hardware implementation includes bit stuffing (when transmitting), CRC calculation, removing bit stuffing, and removing beginning of frame (when receiving) .

Handsfree loudspeaker

The Handsfree speaker power amplifier circuitry is located on the BS1 module. The HF–speaker is used to produce the PDA key–click sounds, error beeps, and tunes. When the lid is opened, the loudspeaker is used as an handsfree speaker, producing key–click sound when a PDA QWERTY key is pressed, and producing tunes. The HF–speaker power amplifier can be controlled by the PDA CPU, or CMT.

Keyboard

The keyboard interface comprises 10x8 matrix lines. The QWERTY keyboard pads are located on the other side of the BS1 module board. 4x2 (2Row/4Column) matrix is routed to the lid. Four columns are multiplexed with CMT keyboard columns. Multiplexing is done by using buffer located on the BS1 module. This buffer is controlled by Baseband voltage (VBB). When the lid is closed these four columns are switched to inputs and they are not read by the CPU.

Table 14. Key Reference Numbers vs. Senses and Drives.

	Column							
	Col0	**Col1**	**Col2**	**Col3**	**Col4**	**Col5**	**Col6**	**Col7**
Row0	S730	S732	S734	S736	S331	S337		S343
Row1	S731	S733	S735	S325	S330	S336	S341	S342
Row2	S300	S318	S347	S324	S335	S311	S303	S305
Row3	S306	S307	S308	S327	S328	S310	S309	S323, S329, S334
Row4	S312	S313	S314	S332	S333	S316	S315	S317
Row5	S301	S319	S320	S321	S322	S348	S349	S302
Row6	S352	S353	S354	S338	S339	S356	S355	
Row7	S357	S358	S359	S344	S345	S361	S360	S346
Row8	S362	S363	S364	S326	S351	S365	S350	
Row9							S304, S340	

NOTE1: Shift pads has dedicated Sense line (ROW9), These shift pads are connected parallel

NOTE2: Grey shaded switches are located in BS2 module.

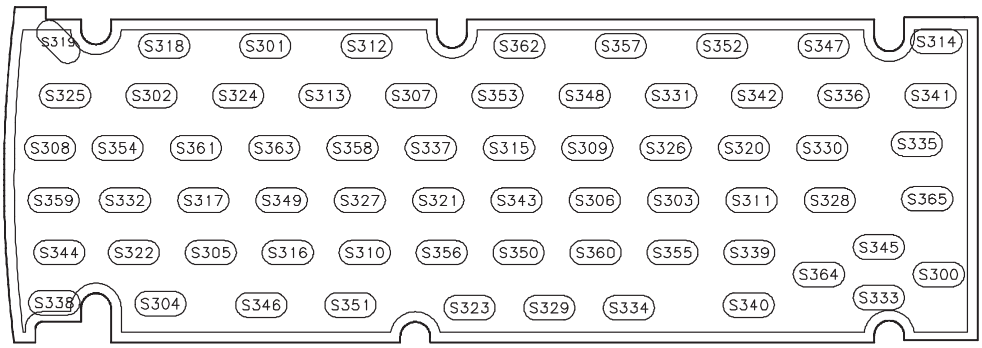


Figure 4. BS1 PDA keyboard

Test pads

Test pads are located under the battery pack. They include JTAG port which is used for After Sales Flashing purposes. The different voltages can be measured from these testpads. Serial data transfer test pads are used for data transfer between the BS1 and BS8 modules.

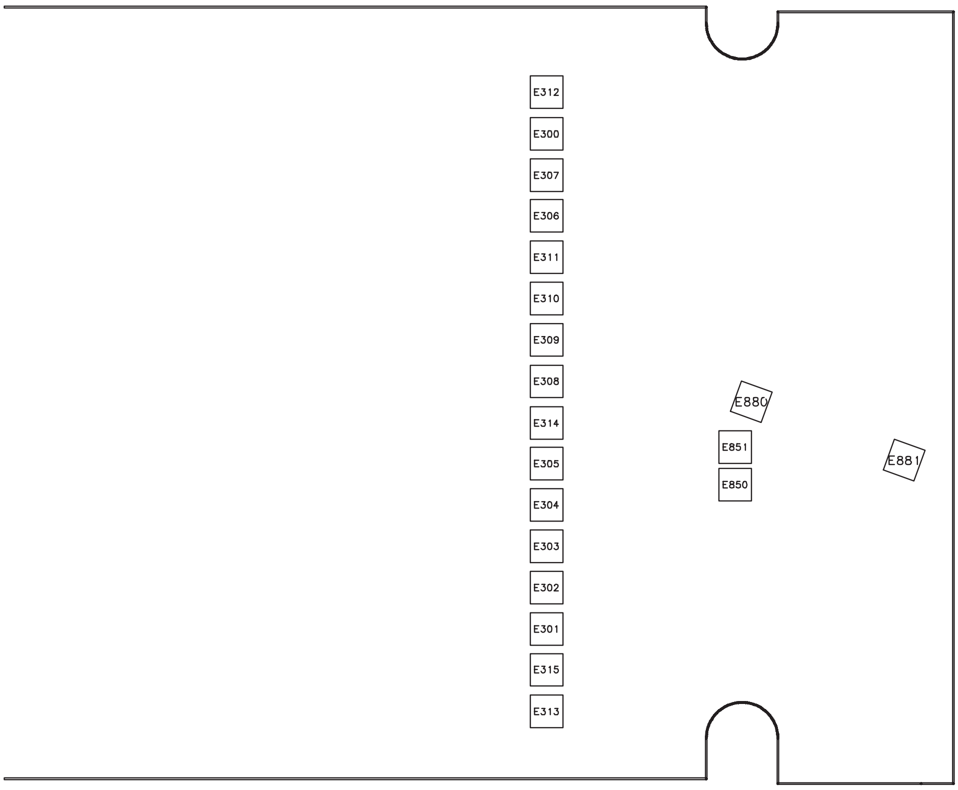


Figure 5. Test pad layout

Table 15. Test pads

Pin	I/O	Name	Function	Min	Nom	Max	Unit	Description / Note
E300		**V17_OUT**	PDA LCD Biasing voltage	13.8	19.4	22.2	VDC	High
					0		VDC	Low
E301	**I**	**BNDSCN_TMS**	Boundary scan Test mode select	2.0	2.80	2.85	VDC	High, test mode selected
					0	0.8	VDC	Low
E302	**I**	**BNDSCN_TCK**	Boundary scan test clock	2.0	2.80	2.85	VDC	High
					0	0.8	VDC	Low
E303	**I**	**BNDSCN_TDI**	Boundary scan data in	2.0	2.80	2.85	VDC	High
					0	0.8	VDC	Low
E304	**O**	**BNDSCN_TDO**	Boundary scan data out	2.30	2.80	2.85	VDC	High
					0	0.45	VDC	Low
E305	**I**	**BNDSCN_EN**	Boundary scan enabled	2.0	2.80	2.85	VDC	High, boundary scan enabled
					0	0.8	VDC	Low
E306	**I**	**Flash VPP**	Flashing voltage for XIP Flashes.	2.75	2.80	2.85	VDC	Connected to VBATT inside the Service battery.
E307		**VBACK**	Backup battery voltage	2.40	3.0	3.10	VDC	High
E308	**O**	**FBUS_RXD**	PDA CPU Tx–pin	2.30	2.80	2.85	VDC	High
					0	0.45	VDC	Low
E309/ E310	**I**	**FBUS_TXD1,2**	PDA CPU Rx–pin	2.0	2.80	2.85	VDC	High
					0	0.8	VDC	Low
E311	**I/O**	**MBUS**	Bidirectional Serial Bus	2.30	2.80	2.85	VDC	High, to the CMT
					0	0.45	VDC	Low, to the CMT
				2.1	2.80	2.85	VDC	High, from the CMT
					0	0.5	VDC	Low, from the CMT
E312		**VSYS**	System voltage	2.75	2.80	2.85	VDC	
E313		**GND**	Global Ground					
E314	**I**	**FLSHWRx**	Write signal for Flash memories	2.30	2.80	2.85	VDC	High
					0	0.45	VDC	Low, write enabled
E315	**I**	**TESTMODEx**	testmode activation	2.0	2.80	2.85	VDC	High
					0	0.8	VDC	Low, testmode enabled

NOTE : Testpad E308 ... E310 is reserved for R&D use.

Testpoints

Testpoints are located around the PDA PCB. They include clock, control, data signals and voltages which is used for R&D, fault finding and testing purposes.

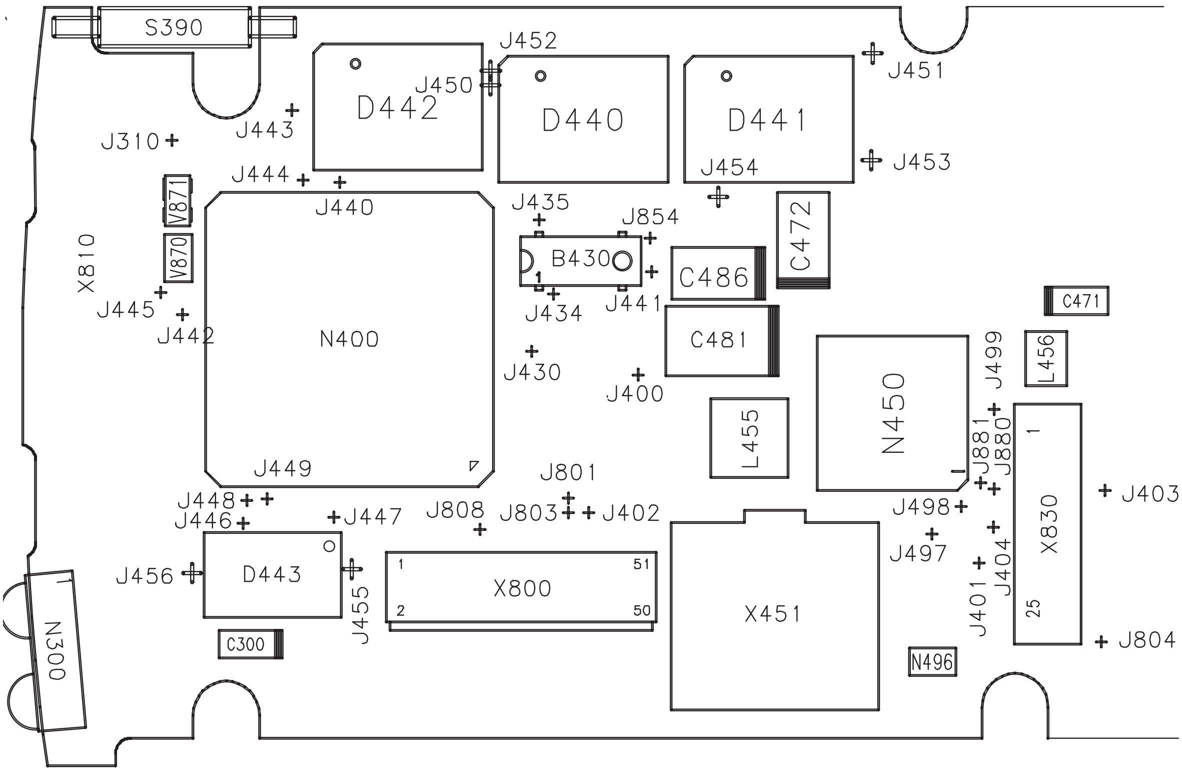


Figure 6.   Testpoints layout

Table 16. Testpoints

Point	I/O	Name	Function	Min	Nom	Max	Unit	Description / Note
J310		**LID_SWITCH_IF**	Lid switch state	2.75	2.8	2.85	VDC	High, lid open
					0		VDC	Low, lid closed
J400		**33MHz**	CPU core clock	2.3	2.80	2.85	VDC	High
					0	0.45	VDC	Low
J401	**O**	**X32_CLK**	CMT sleep clock	2.3	2.80	2.85	VDC	High
					0	0.45	VDC	Low
J402	**I**	**VBB**	CMT baseband voltage	2.7	2.80	2.85	VDC	High
						1.0	mA	Maximum current

Table 16. Testpoints (continued)

Point	I/O	Name	Function	Min	Nom	Max	Unit	Description / Note
J403	I/O	MBUS	Bidirectional Serial Bus	2.30	2.80	2.85	VDC	High, to the CMT
					0	0.45	VDC	Low, to the CMT
				2.1	2.80	2.85	VDC	High, from the CMT
					0	0.5	VDC	Low, from the CMT
J404	O	PWR_ONx		2.0	2.80	2.85	VDC	High
					0	0.45	VDC	Low
J430		LF_INT	Intermidiate PLL loop filter		1.2		VDC	When PLLs are locked
J434	I	X32IN			1.35		VDC	High, Sini vawe
					0		VDC	Low
J435	O	X32OUT			1.0		VDC	High
					–0.3		VDC	Low
J440		ROMCS2	RFD flash chip select	2.3	2.80	2.85	VDC	High
					0	0.45	VDC	Low, chip selected
J441		ROMCS0	XIP1 flash chip select	2.3	2.80	2.85	VDC	High
					0	0.45	VDC	Low, chip selected
J442		FLASHWRx	XIP and RFD flashes write enable from CPU	2.3	2.80	2.85	VDC	High
					0	0.45	VDC	Low, write enabled
	I		XIP and RFD flashes write enable from frame connector or testpads	2.0	2.80	2.85	VDC	High
					0	0.8	VDC	Low, write enabled
J443		ROMRDx	RFD flash read enable	2.3	2.80	2.85	VDC	High
					0	0.45	VDC	Low, read enabled
J444		WP	RFD flash write protect	2.3	2.80	2.85	VDC	High
					0	0.45	VDC	Low, write protected
J445		ROMCS1	XIP2 flash chip select	2.3	2.80	2.85	VDC	High
					0	0.45	VDC	Low
J446		RASx	DRAM row address strobe	2.3	2.80	2.85	VDC	High
					0	0.45	VDC	Low
J447		MWEx	DRAM write enable	2.3	2.80	2.85	VDC	High
					0	0.45	VDC	Low
J448		CASL1x	DRAM upper column address select	2.3	2.80	2.85	VDC	High
					0	0.45	VDC	Low
J449		CASL0x	DRAM lower column address select	2.3	2.80	2.85	VDC	High
					0	0.45	VDC	Low
J450		FLASH_CTRL2	RFD flash status	2.4	2.80	2.85	VDC	High
					0	0.4	VDC	Low

Table 16. Testpoints (continued)

Point	I/O	Name	Function	Min	Nom	Max	Unit	Description / Note
J451		**STS1**	XIP1 flash status	2.4	2.80	2.85	VDC	High
					0	0.4	VDC	Low
J452		**STS2**	XIP2 flash status	2.4	2.80	2.85	VDC	High
					0	0.4	VDC	Low
J453		**SD1**	System data bus line 1	2.3	2.80	2.85	VDC	High, data to memory
					0	0.45	VDC	Low, data to memory
				2.4	2.8	2.85	VDC	High, data to CPU
					0	0.4	VDC	Low, data to CPU
J454		**SA4**	System address bus line 4	2.3	2.80	2.85	VDC	High
					0	0.45	VDC	Low
J455		**D0**	Memory data bus line 0	2.3	2.80	2.85	VDC	High
					0	0.45	VDC	Low
J456		**MA3**	Memory address bus line 3	2.3	2.80	2.85	VDC	High
					0	0.45	VDC	Low
J497		**VCOMP1**		1.24		1.285	VDC	
J498		**CS3x**	Phaser chip select	2.3	2.80	2.85	VDC	High
					0	0.4	VDC	Low, chip selected
J499		**RESETx**	Reset from Phaser to CPU and flash memories	2.5	2.80	2.85	VDC	High
					0	0.5	VDC	Low
J801	**O**	**GENSDIO**	CMT LCD and CCONT serial data	2.0	2.80	2.85	VDC	High
					0	0.5	VDC	Low
J803	**I/O**	**LCDCD**	CMT LCD command / data select	2.0	2.80	2.85	VDC	High, data
					0	0.6	VDC	Low, command
J804	**I/O**	**LCDCSx**	CMT LCD chip select	2.1	2.80	2.85	VDC	High
					0	0.5	VDC	Low, chip selected
J808	**O**	**SCK**	PDA LCD data clock	2.3	2.80	2.85	VDC	High
J854		**BZR_IF**	Buzzer signal	2.0	2.80	2.85	VDC	High
					0	0.6	VDC	Low
J880		**HFENA**	Handsfree earpiece enable	2.3	2.80	2.85	VDC	High, HF amplified enabled
					0	0.45	VDC	Low, HF amplified disabled
J881	**O**	**XEAR**	Audio output for handsfree use			2.0	Vpp	

Chapter 7

Troubleshooting

AMENDMENT RECORD SHEET

Amendment Number	Date	Inserted By	Comments
	02/99		Original

CONTENTS –Troubleshooting

Page No

Introduction

This document is intend to be a guide for localizing and repairing electrical faults in RAE–2 device. First there is short guide for fault localizing. Then fault repairing is divided into three troubleshooting paths, each per any module. Needed equipments are present before any actions.

Before any service operation you must be familiar with RAE–2 product and module level architecture. You must also be familiar with RAE–2 specified service tools like the WinTesla service software, Flashing tools and softwares. Basic skills of using RF measurement devices are required when you are starting to follow RF troubleshooting paths.

General

When you have a faulty RAE–2 device and you are starting troubleshooting it, check first the following basics.

– Device hasn't any mechanical damage.
– Device, especially connectors, are not dirty or moist.
– Screws are tightened as specificed.
– Battery voltage is high enough (nominal battery voltage is 3.6V).
– Current consumption is in normal area (this can be checked with Service Battery BBS–5, if ReLink mode is disabled).

Current consumption

	CMT mode (CMT current)		
PDA mode (PDA current)	**Off (< 1.0mA)**	**Idle (3–40mA)**	**Call (140–320mA)**
Active (200–380mA)	200–380mA	203–420mA	340mA–700mA
Standby (35–65mA)	35–45mA	38–85mA	175–365mA
Suspended (2–4mA)	2–3mA	5–43mA	142–323mA
Reset	<1.0mA	3–40mA	140–320mA

Note1: CMT peak current consumption might be 5x more than is specified above.

Finding faulty module

Then you define the faulty module. Normally this isn't difficult because the RAE–2 device has three quite independent modules; CMT, PDA and UI.

If you can't conclude which is the faulty module, try to program new software to the RAE–2. Usually when a module has a real fault also its programming fails. If programming succeeds, it means that the CMT and

PDA modules basically work and the fault might be in UI module or flex connectors between PDA and UI module. Before CMT programming check that PDA goes to the ReLink mode (use BBS–5 service battery).

After that you can replace the faulty module with the reference (Golden Sample) module and be sure that module is really faulty. Alternatively you can change the suspected faulty module to the reference RAE–2 device. After this cross–checking you should have found certainty about the faulty module(s) and you can start to study module level problems.

CMT Troubleshooting

The following hints should facility finding the cause of the problem when the CMT circuitry seems to be faulty. This troubleshooting instruction is divided in main level to BaseBand and RF faults.

The first thing to do is carry out a through visual check of the module. Ensure in particular that there are not any mechanical damages and soldered joints are OK. If the CMT module is able to communicate with WinTesla software, you can use it to find out faulty circuits from CMT module. Selftest checks all CMT baseband Asics and memory components and reports the result as passed or failed. If every test is passed, you can perform different kind of calibration and tuning operations and deduce which is the faulty circuit.

Baseband faults

At least the following measurement devices are needed for fault debugging in BaseBand section:

– PC for the Wintesla with software protection key (dongle)
– RS–232 cable (DAU –9C)
– Repairing jig MJS–4
– Flashing Tools FLA–7, FPS–4 and TDF–4
– Service Battery BBS–5
– Calibration Unit JBE–1
– power supply, digital multimeter and oscilloscope

CMT is totally dead

This means that CMT doesn't take current at all when the power switch is pressed or when the Watchdog Disable signal (J113) is rounded. Used battery voltage must be at least the nominal, 3.6 V.

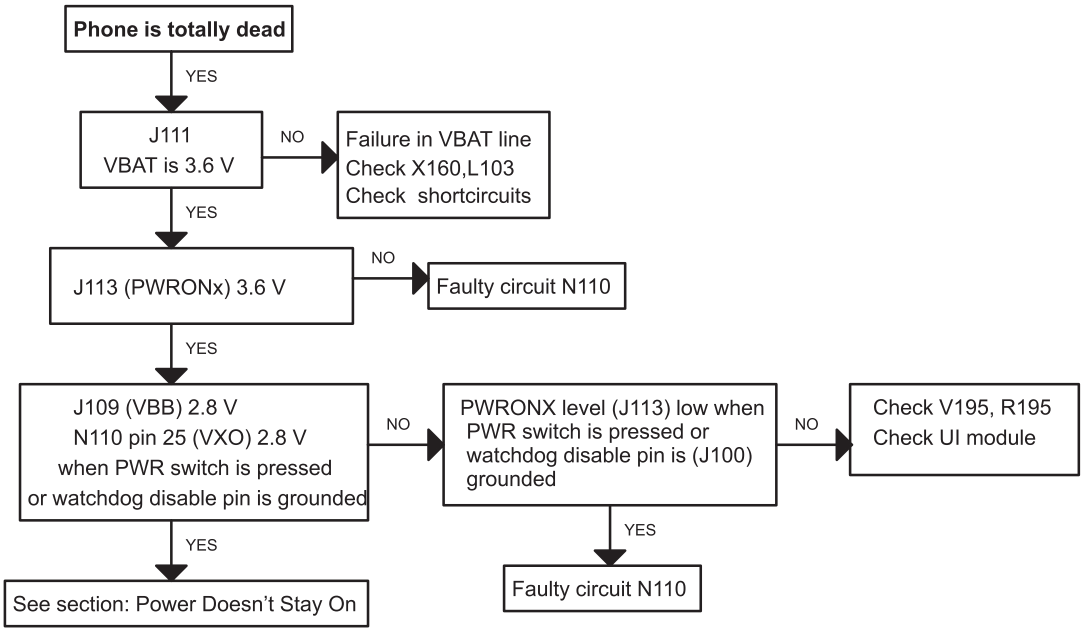


Figure 1. Trouble Shooting Diagram for Phone is totally dead failure

Power doesn’t stay on or phone is jammed

Normally the power will be switched off by CCONT (N110) after 30 seconds, if the watchdog of the CCONT can not be served by software. The watchdog updating can be seen by oscilloscope at pin 50 (DataselX) of CCONT. In normal case there is a short pulse from ”1” –> 0 every 8 seconds.

The power off function of CCONT can be prevented by connecting a short circuit wire from CCONT pin 29 (or J113) to ground.

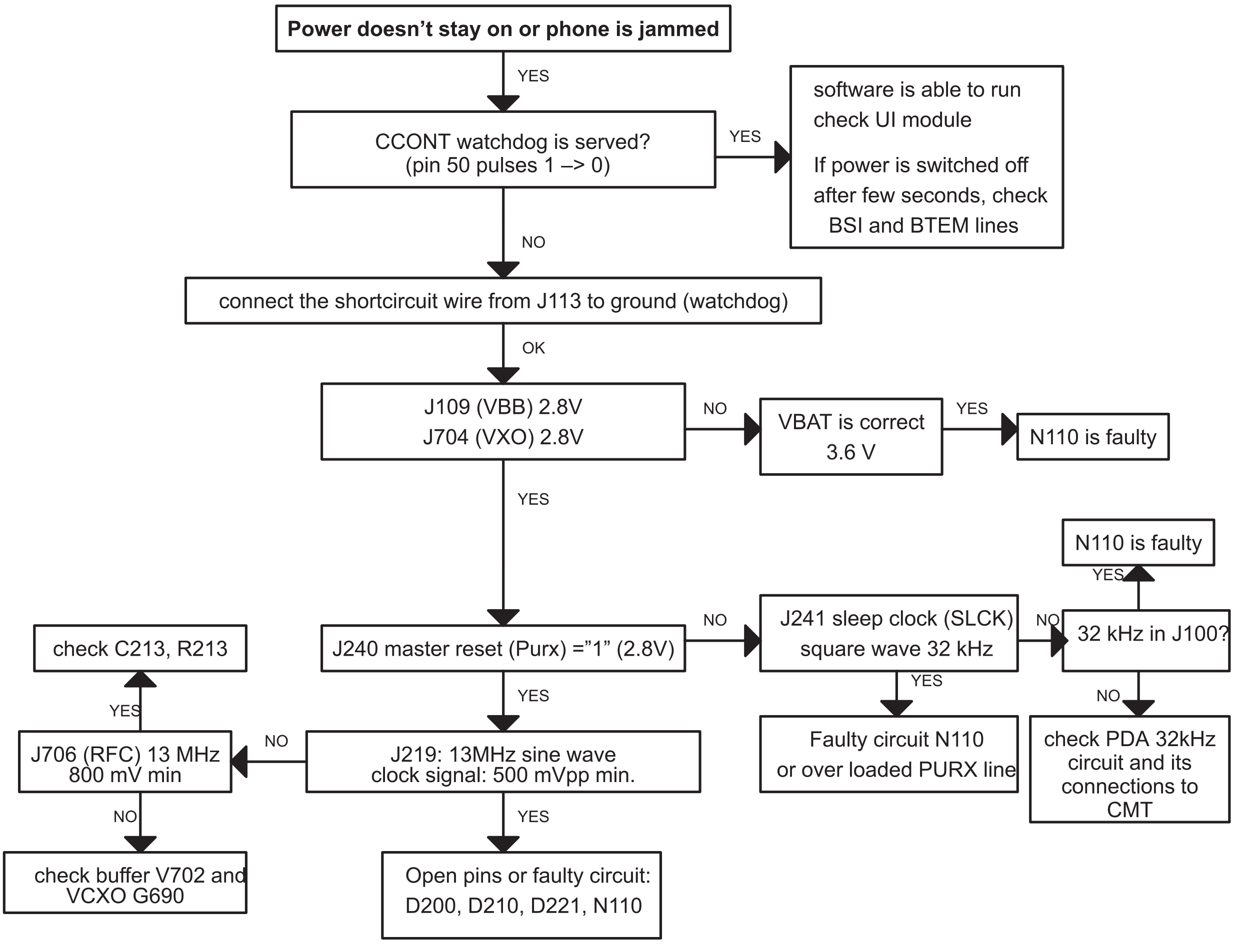


Figure 2. Trouble Shooting Diagram for Power Doesn’t Stay On or phone is jammed failures

Display Information: Contact Service

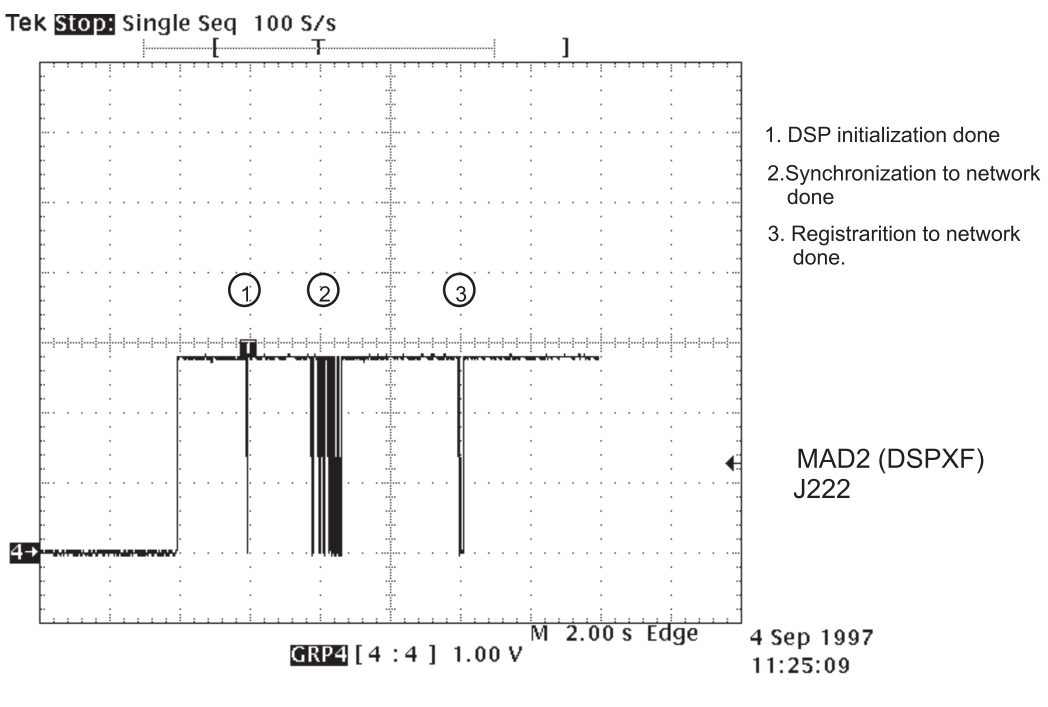
This fault means that software is able to run and thus the watchdog of CCONT (N110) can be served. Selftest functions are run when power is switched on and the software is started to execute from flash. If any of the self–tests fails, **Contact Service** text will be shown on the display. Find out which circuit is faulty using the WinTesla software (select from Testing menu item Self Tests... and WinTesla shows which circuit are not passed selftests).

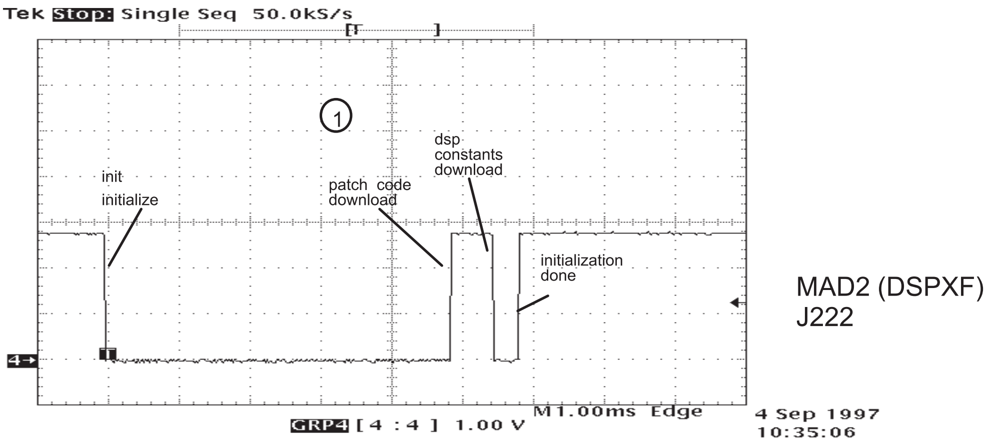
The phone doesn't register to the network or phone doesn't make a call

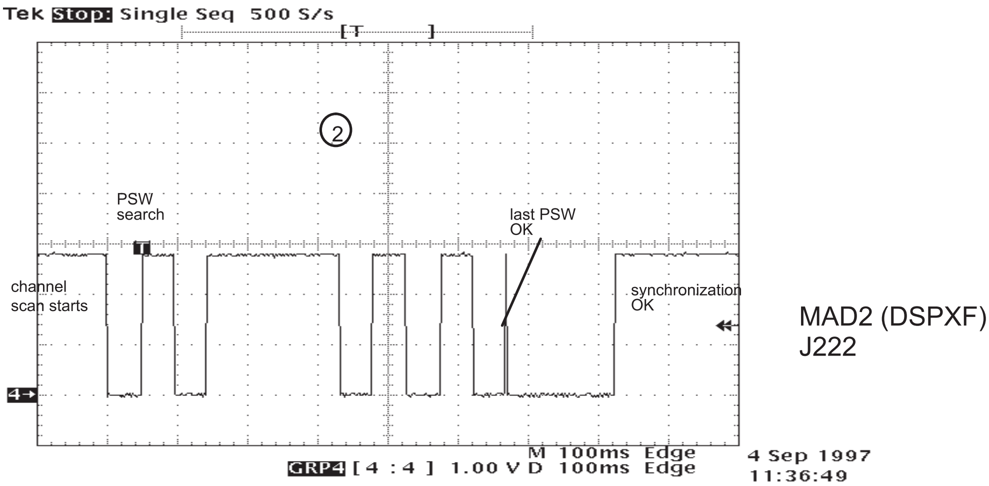
If the phone does not register to the network or the phone does not make a call, the reason could be either the baseband or the RF part. The phone can be set to wanted mode by WinTesla service software and determinate if the fault is in RF or in baseband part (RF interface measurements).

The control lines for RF part are supplied both the System Asic (MAD2; D200) and the RFI (Cobba; N250). MAD2 handles the digital control lines (like synthe, TxP etc.) and Cobba handles the analog control lines (like AFC, TxC etc.).

The DSP software is constructed so that the operation states of DSP (MAD2) can be seen in external flag (DSPXF) output pin (J222). After power up, the DSP signals all completed functions by changing the state of the XF pin.







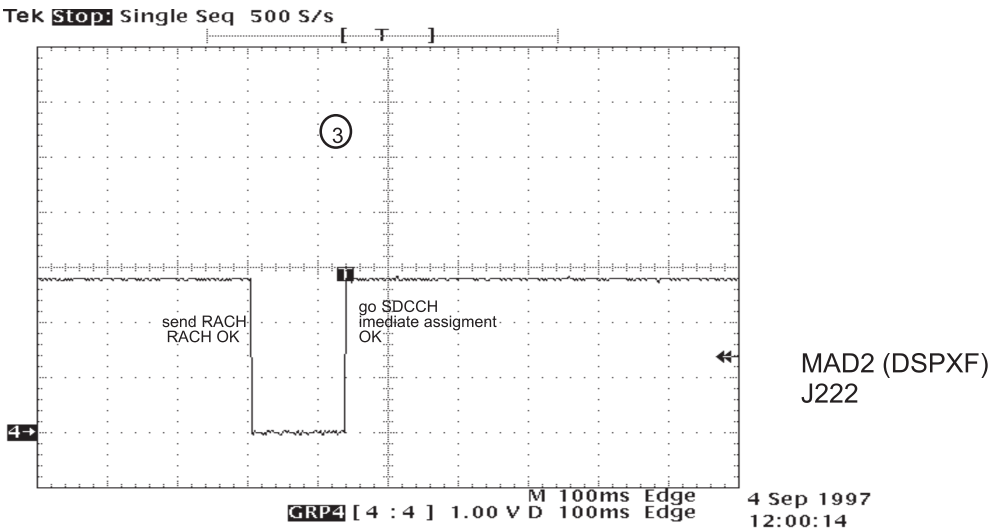


Figure 3.   The states of DSP after power on

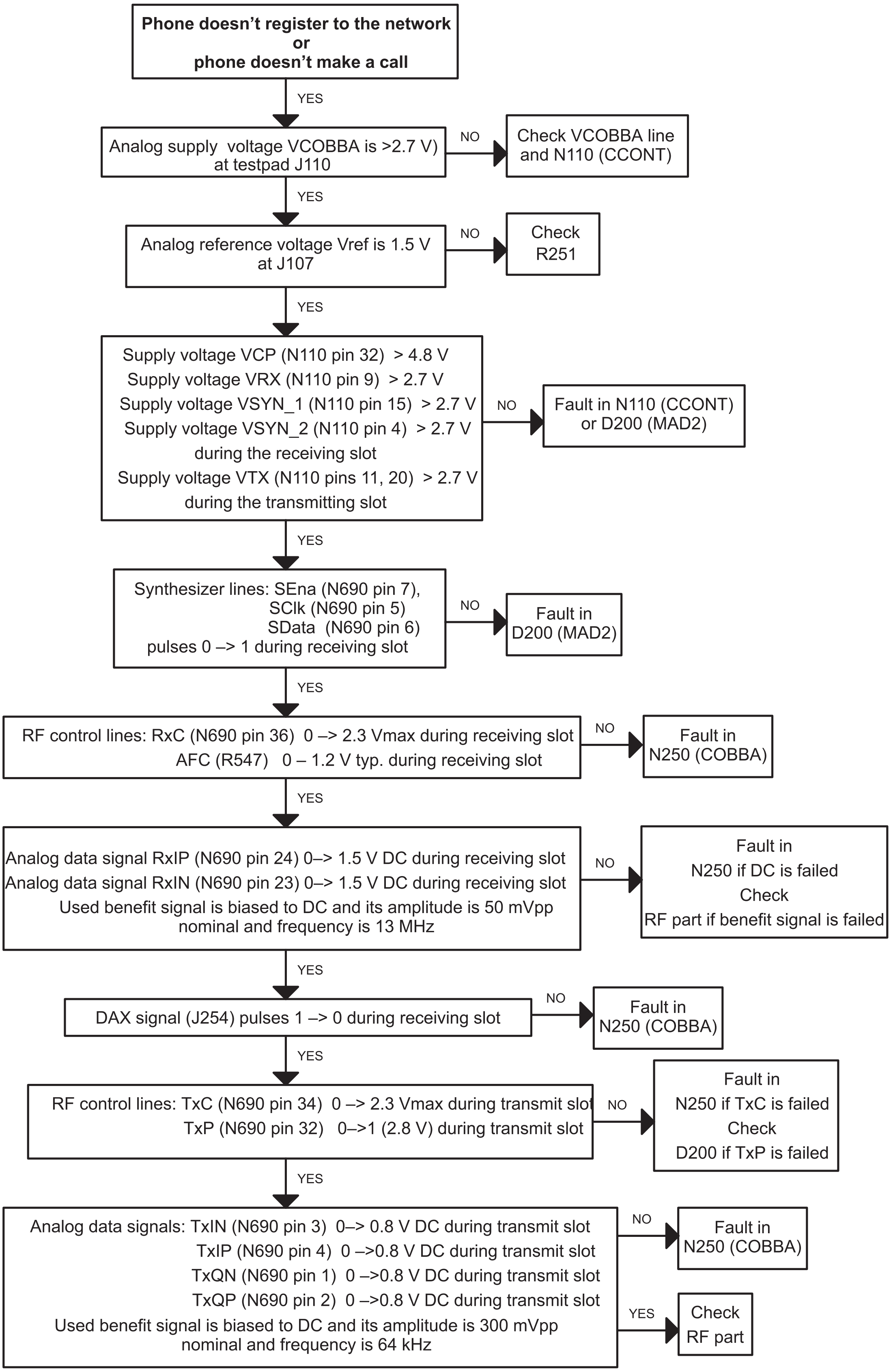


Figure 4. The phone doesn’t register or doesn’t make a call

SIM card is out of order

The hardware of the SIM interface from the MAD2 (D200) to the SIM connector (X150) can be tested without SIM card. When the power is switched on and if the BSI line (X160;2) is grounded by resistor, all the used lines (VSIM, RST, CLK, DATA) rise up to 5 V four times. Thus ”**Insert SIM card**” faults can be found without SIM card. The fault information ”**Card rejected**” means that the ATR message (the first message is always sent from card to phone) is sent from card to phone but the message is somehow corrupted, data signal levels are wrong etc. or factory set values (stored to the EEPROM) are not correct.

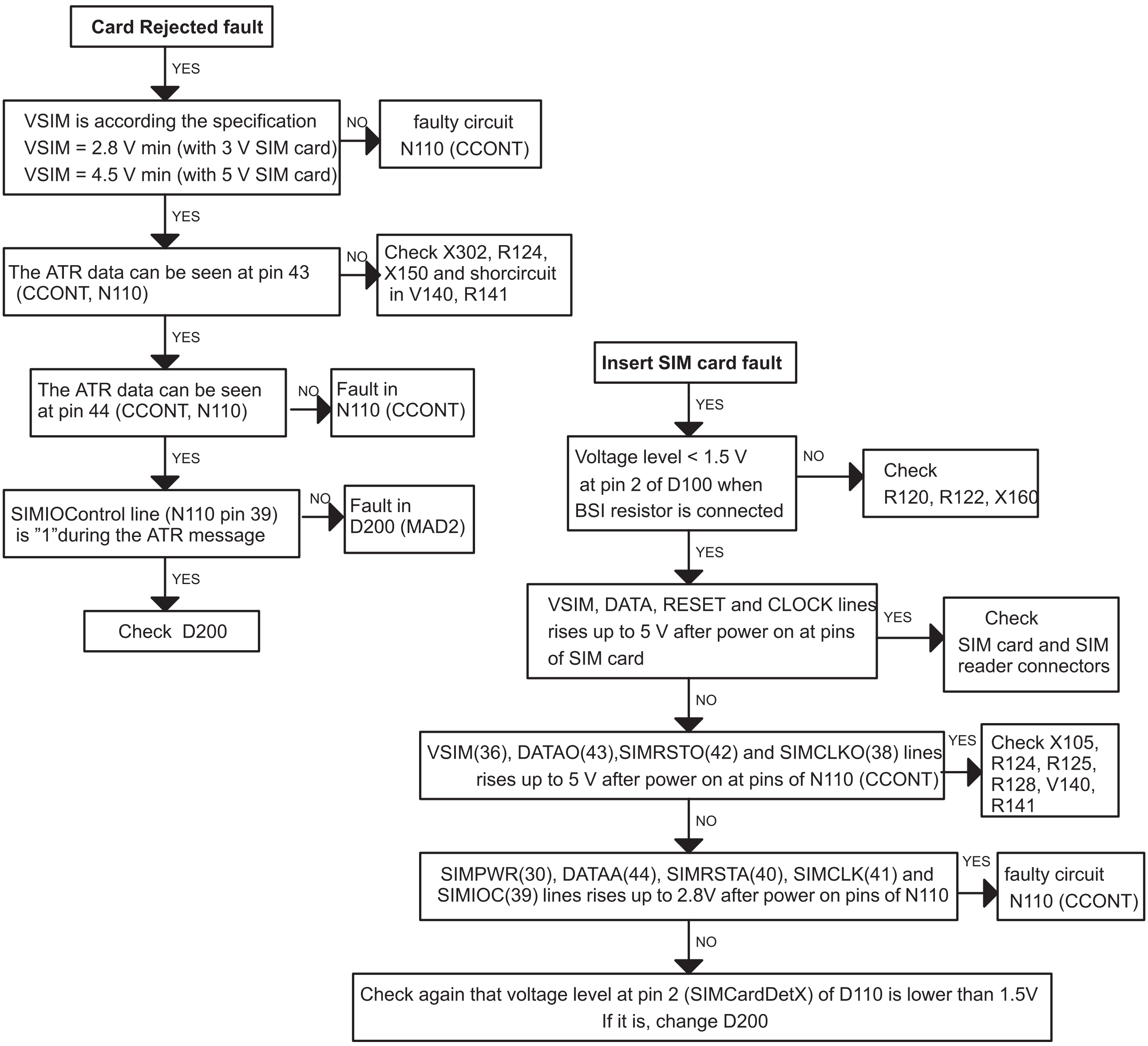


Figure 5. Troubleshooting for SIM card faults

Audio fault

Troubleshooting tree for Audio fault:

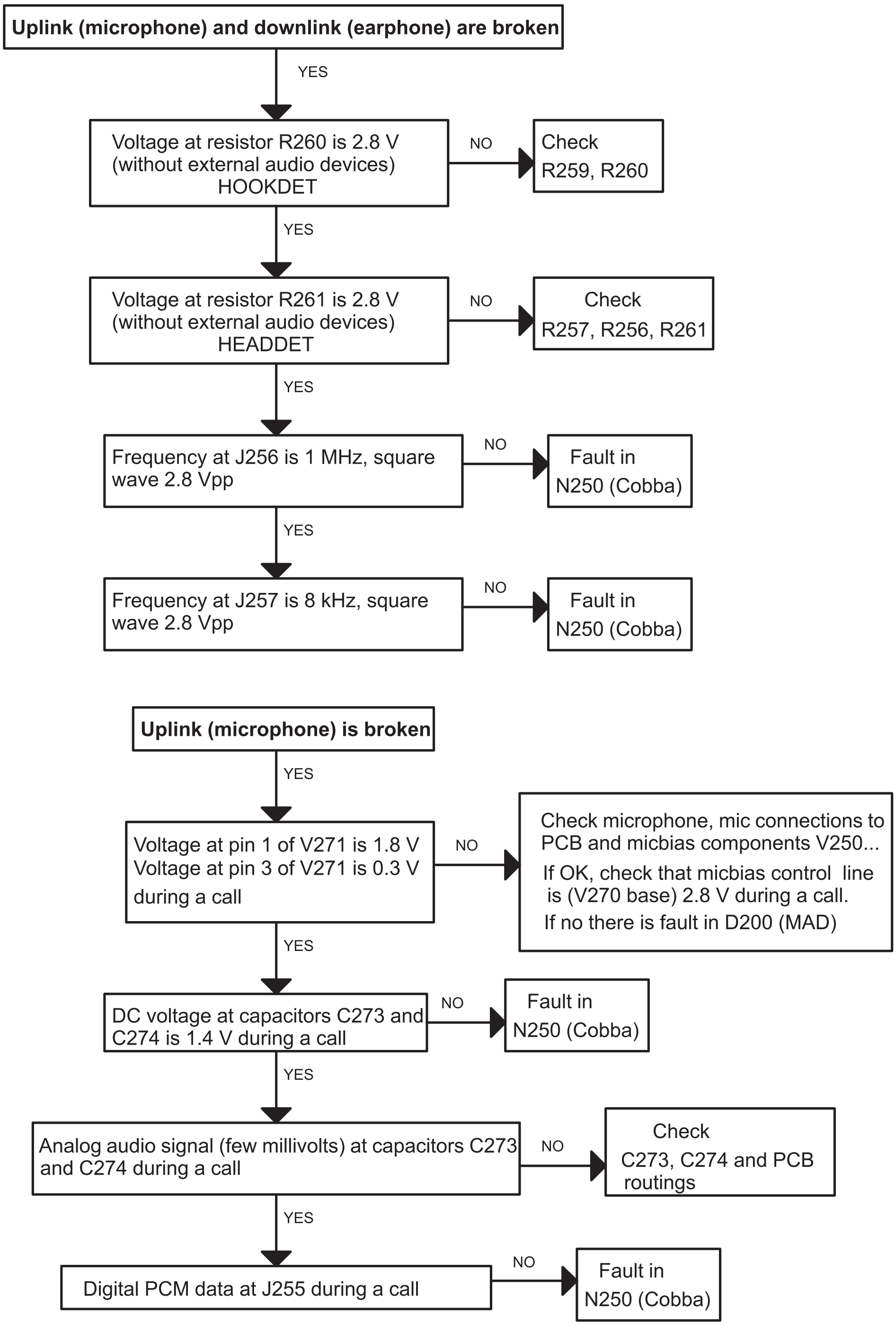


Figure 6. Trouble Shooting Diagram for Audio Failure

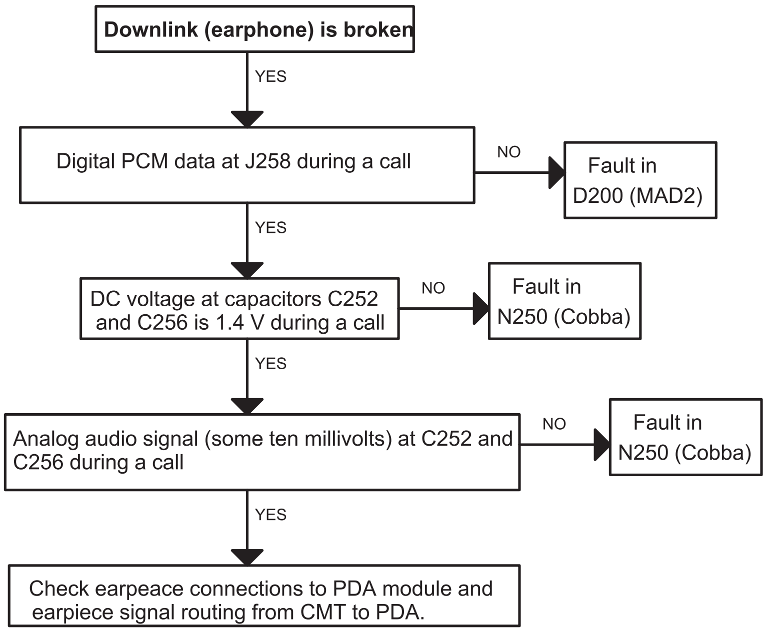


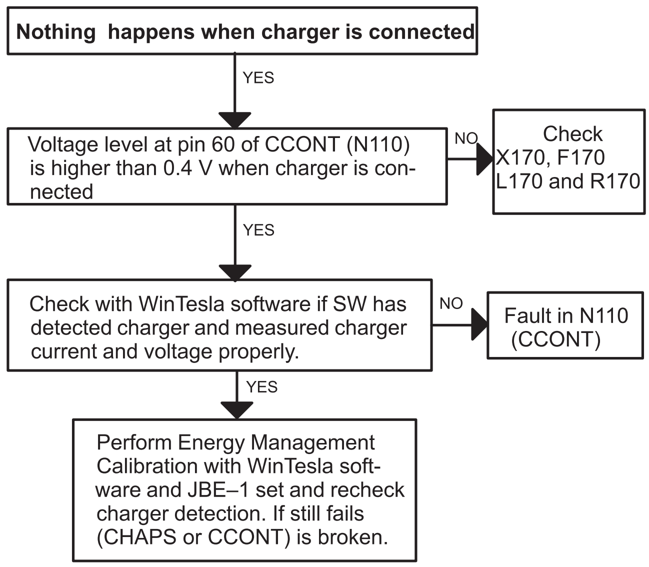
Figure 7. Trouble Shooting Diagram for Audio Failure

Charging fault

When you are charging totally empty battery, remember that start–up charging might take 2 minutes with ACP–9 charger and several minutes with ACP–7 charger. During this time display is blank.

If charger is not NMP approved type then the software doesn't start charging.

Remove and reconnect battery and charger few times before you start to measure module. This check ensure if module fault really exist.



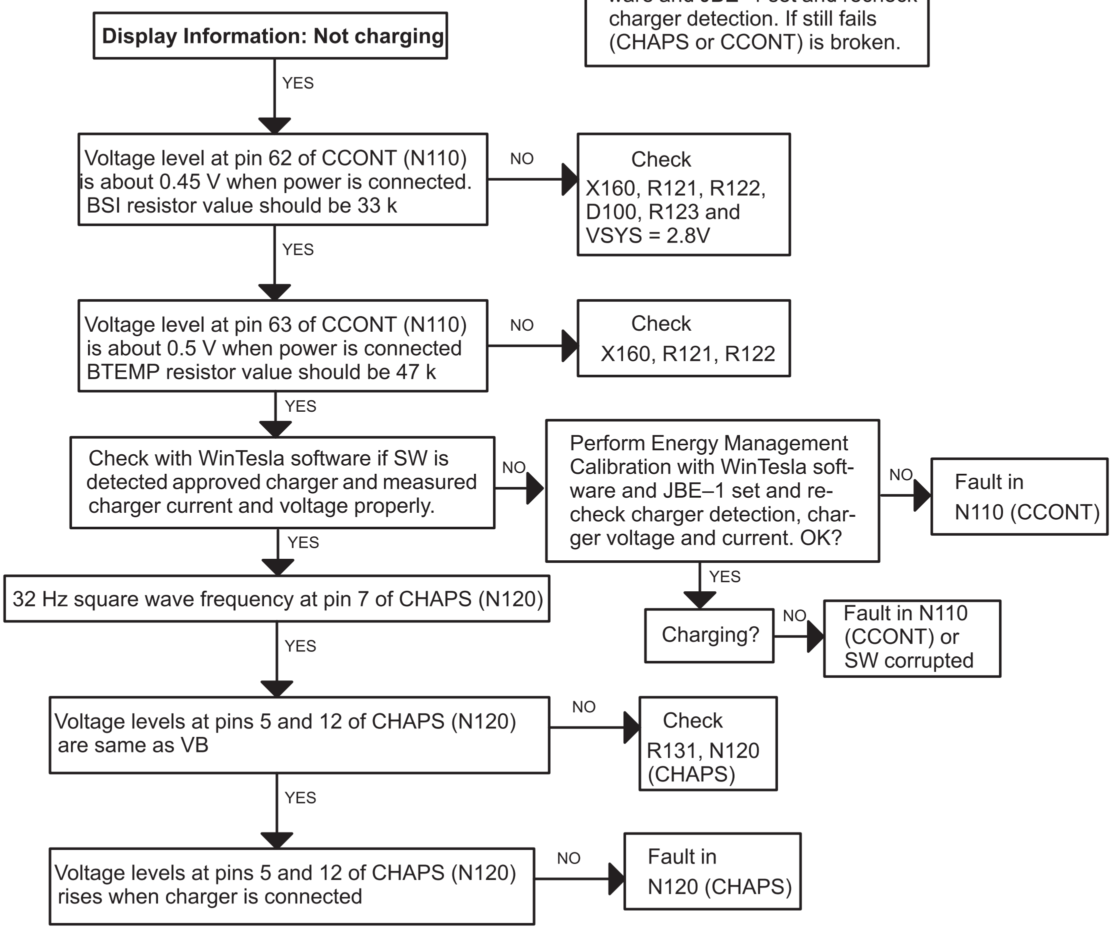


Figure 8. Trouble Shooting Diagram for Charging Failure

Flash programming doesn't work

The flash programming is done over the system connector X170.

In flash programming error cases the flash prommer can give some information about a fault. The fault information messages could be:

– MCU doesn't boot
– Serial clock line failure
– Serial data line failure
– External RAM fault
– Algorithm file or alias ID don't find
– MCU flash Vpp error

In cases that the flash programming doesn't succeed there is a possibility to check short circuits between the memories and the MCU (MAD2).This test is useful to do, when the fault information is:
MCU doesn't boot,
Serial clock line failure or
Serial data line failure.

The test procedure is following:

1. Connect the short circuit wire between the test points J229 and ground.
2. Switch power on
3. If the voltage level in testpoint J203 is 2.8 V ("1"), the interface is OK. If there is a short circuit, the voltage level in testpoint J203 stays low and 32kHz square wave signal can be seen in the lines which are already tested.

One must be noticed that this test can be found only short circuits, not open pins. Also upper data lines (15:8) of flash circuit D210 are not included to this test.

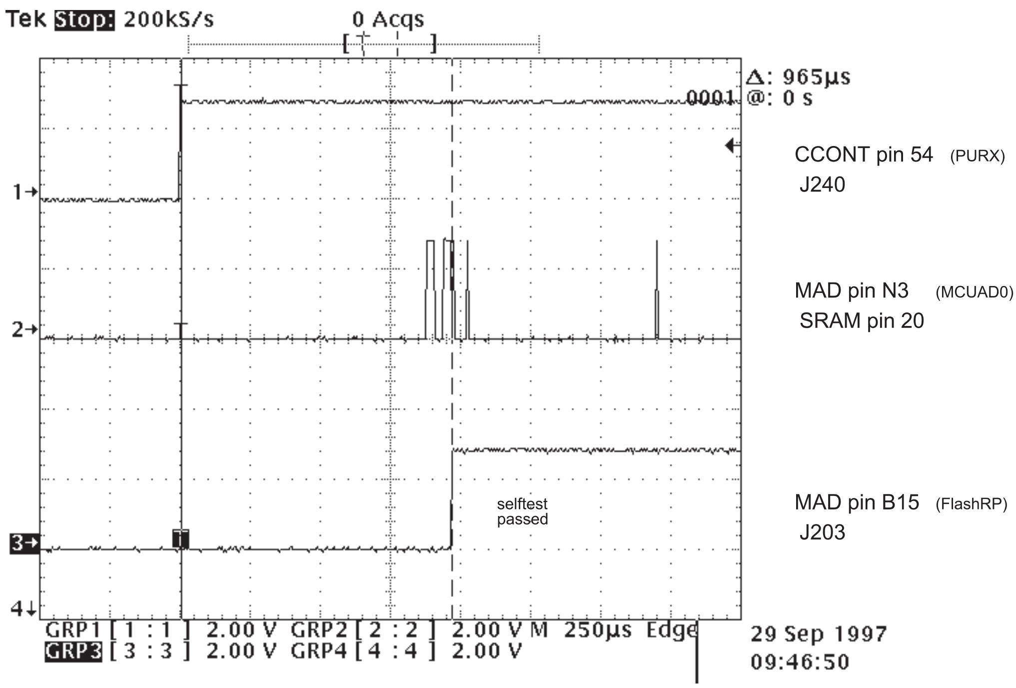


Figure 9. MAD selftest indication after power on (passed)

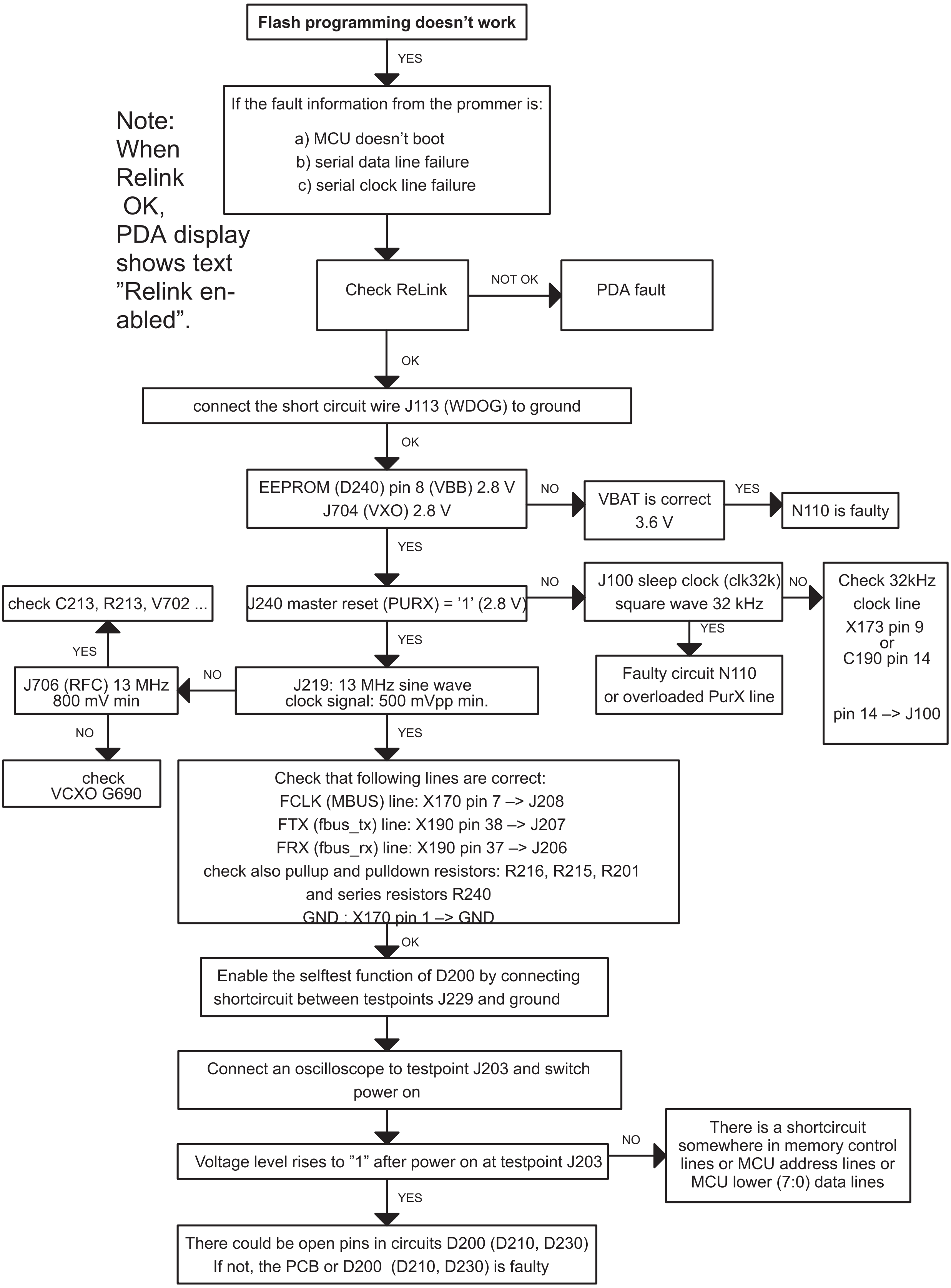


Figure 10. Trouble Shooting Diagram for flash programming doesn't work (via system connector X170)

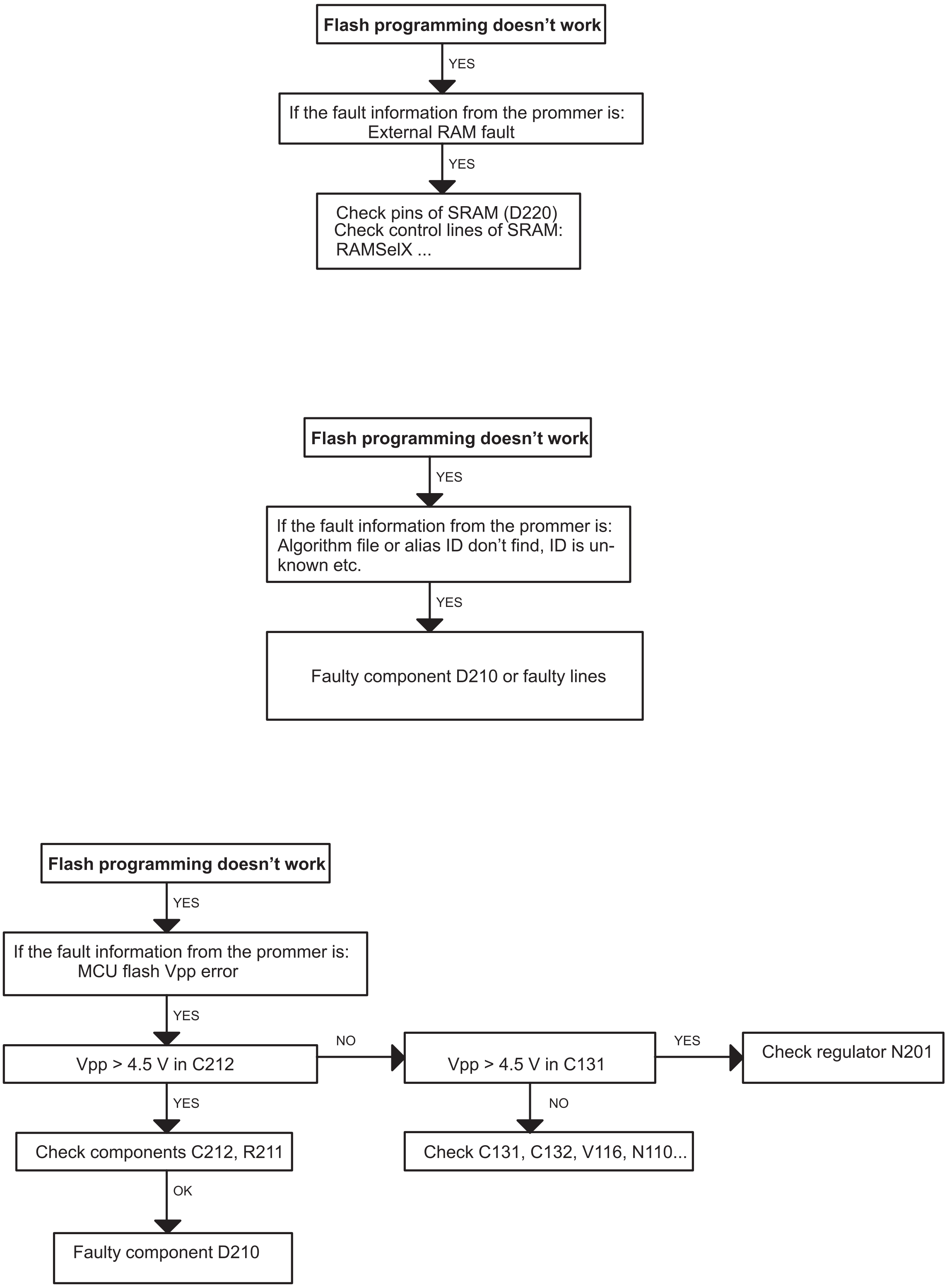


Figure 11. Trouble shooting Diagram for Flash programming doesn't work (via system connector X170)

RF Fault

Here is a block diagram for repairing the RF section. First select the fault and follow the diagram.

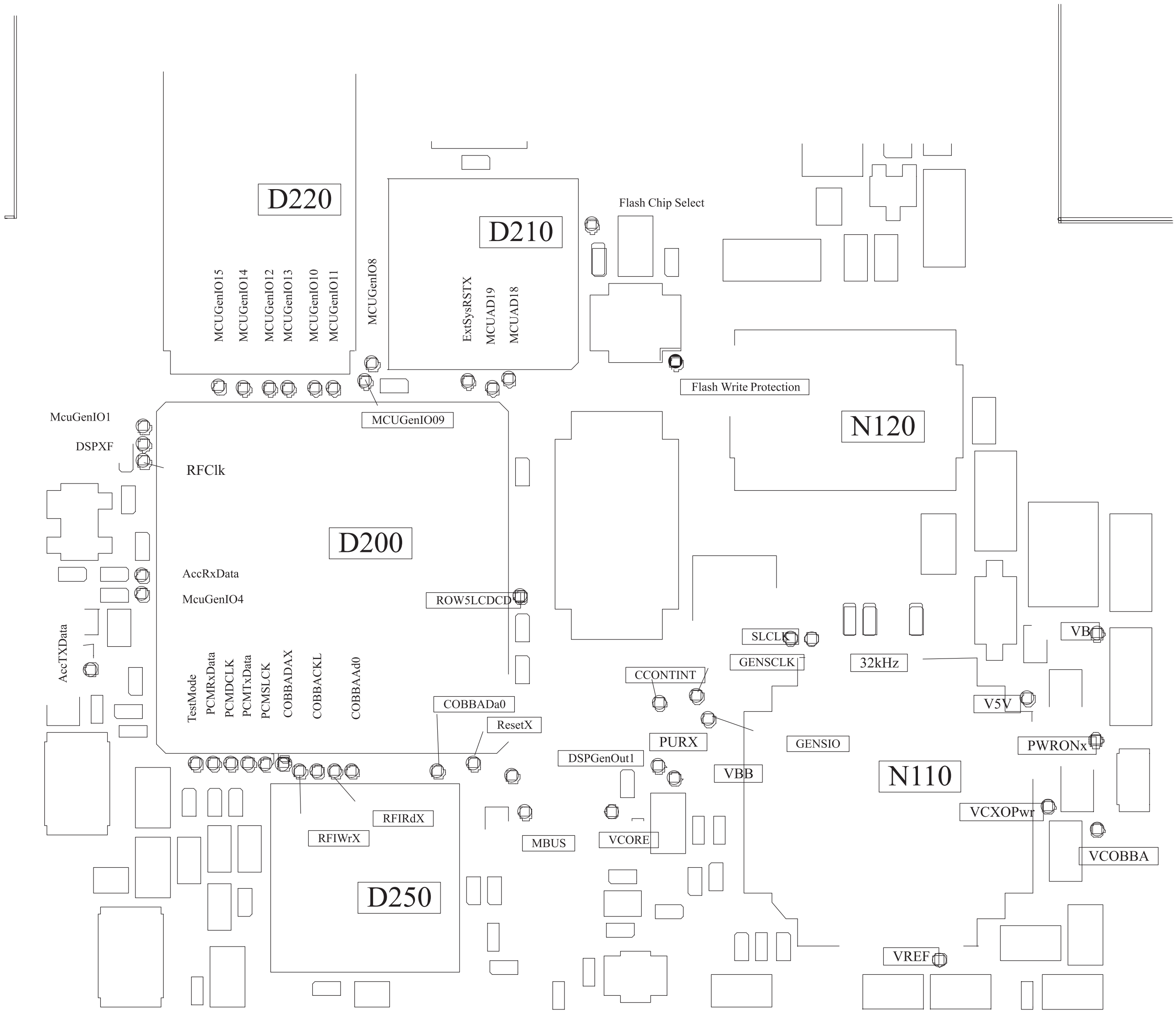
Required Servicing Equipment:

– PC for the Wintesla
– Power supply
– Digital multimeter
– Oscilloscope
– Spectrum analyzer
– GSM MS test set
– Signal generator
– RF probe
– Phone test jig

Test Points on BS8 Module

Test points are placed on baseband for service and production trouble shooting purposes in some supply voltage and signal lines.

Because some of baseband signal are routed totally inner layers (due to uBGA packages) some testpoints are added for these signals.



The figure above describes and the next table lists the test points.

Test Point	Name	Description
J100	32kHz	32kHz clock from BS1 module
J103	CCONTINT	CCONT interrupt output
J105	GENSCLK	Serial data clock
J106	GENSIO	Serial data
J107	VREF	Reference voltage
J108	V5V	Supply voltage for flash programming (Vpp) and RF circuits.
J109	VBB	Supply voltage for digital circuits
J110	VCOBBA	Supply voltage for analog circuits
J111	VB	Battery voltage
J112	VCORE	Supply voltage for MAD c07 core
J113	PWRONx	CCONT's PWRONx / Watchdog disable signal
J203	ExtSysRSTX	Testpoint for fault diagnostic. If missing, check power supply, PurX line and 13 MHz clock signal.
J204	VCXOPwr	Control line for VCXO module. If low, 13 MHz clock signal for baseband is disable.
J206	AccRxData	FBUS RX
J207	AccTxData	FBUS TX
J208	MBUS	Serial data bus max 9600b/s. Flash programming clock
J209	McuGenio4	General purpose out in MAD
J211–J218	MCUGenIO(8:15)	Test point for fault diagnostic. MCUDA(15:8)
J219	RFClk	13 Mhz System clock
J220	TestMode	MAD test mode select input
J221	DSPGenOut1	General purpose DSP out
J222	DSPXF	Test point for fault diagnostic.
J223–J224	MCUAD(18:19)	Memory address signals
J225	Flash Chip Sel	Flash chip select pin
J226	Flash Write Prot	Flash write protection pin
J229	ROW5LCDCD	Selftest pin. If shortcircuit is made between testpoint J229 and J230, the selftest will be executed.
J232	COBBAAd0	
J233	COBBADa0	
J240	PurX	Reset line from CCONT to MAD. If low, the BB circuits are in reset state.
J241	SLCLK	32 kHz clock from CCONT to MAD
J243	McuGenio1	General purpose input in MAD
J250	RFIRdX	COBBA paraller interface read strobe
J251	RFIWrX	COBBA paraller interface write strobe
J252	ResetX	COBBA master reset
J253	COBBACLK	COBBA 13Mhz clock
J254	COBBADAX	COBBA paraller interface data available strobe
J255	PCMTxData	COBBA PCM bus transmit data
J256	PCMDCLK	COBBA bus data transfer clock
J257	PCMSCLK	COBBA bus 8kHz frame sync
J258	PCMRxData	COBBA PCM bus receive data

Transmitter fault

Troubleshooting tree for Transmitter fault:

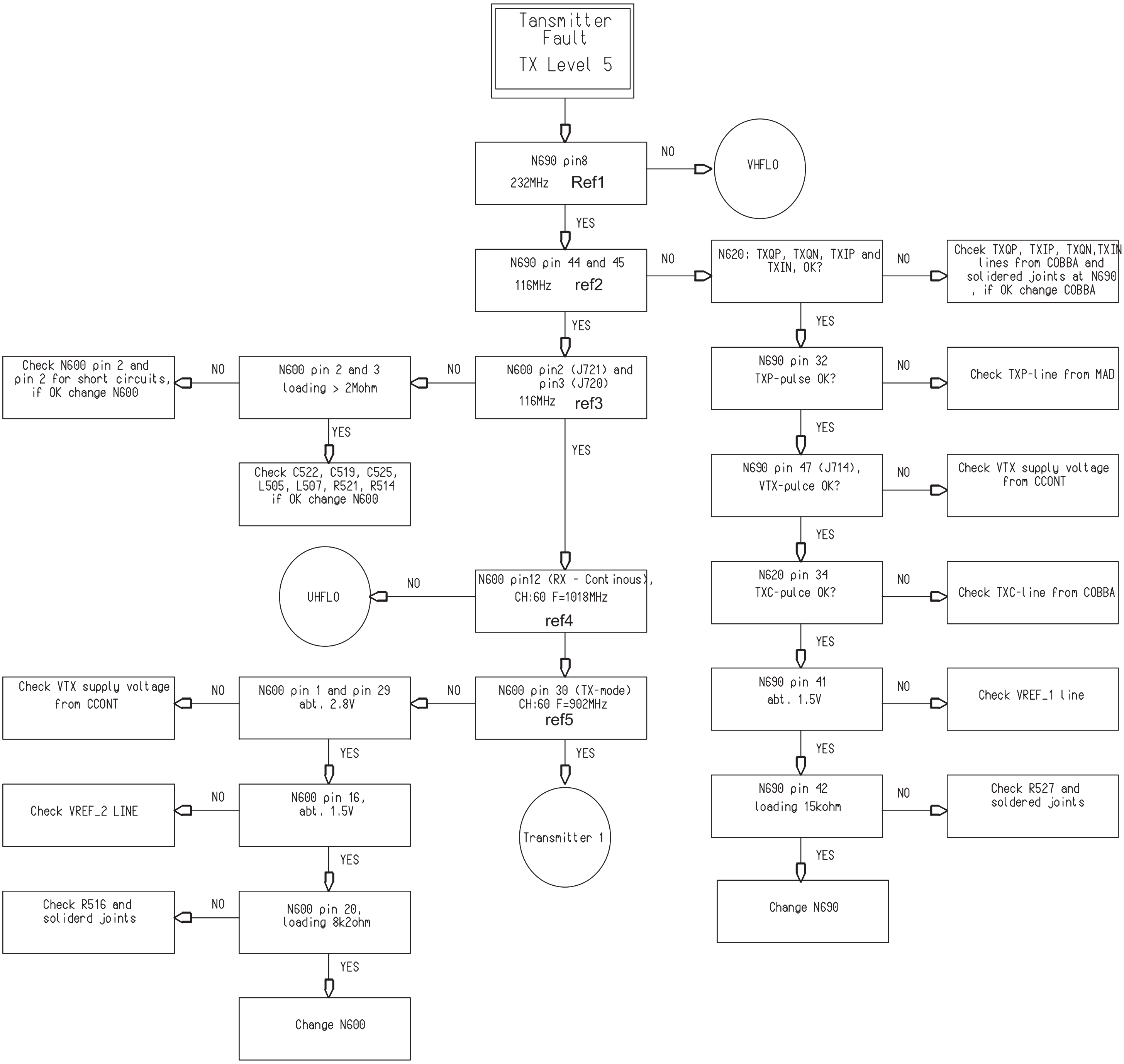


Figure 12. Transmitter fault TX level 5

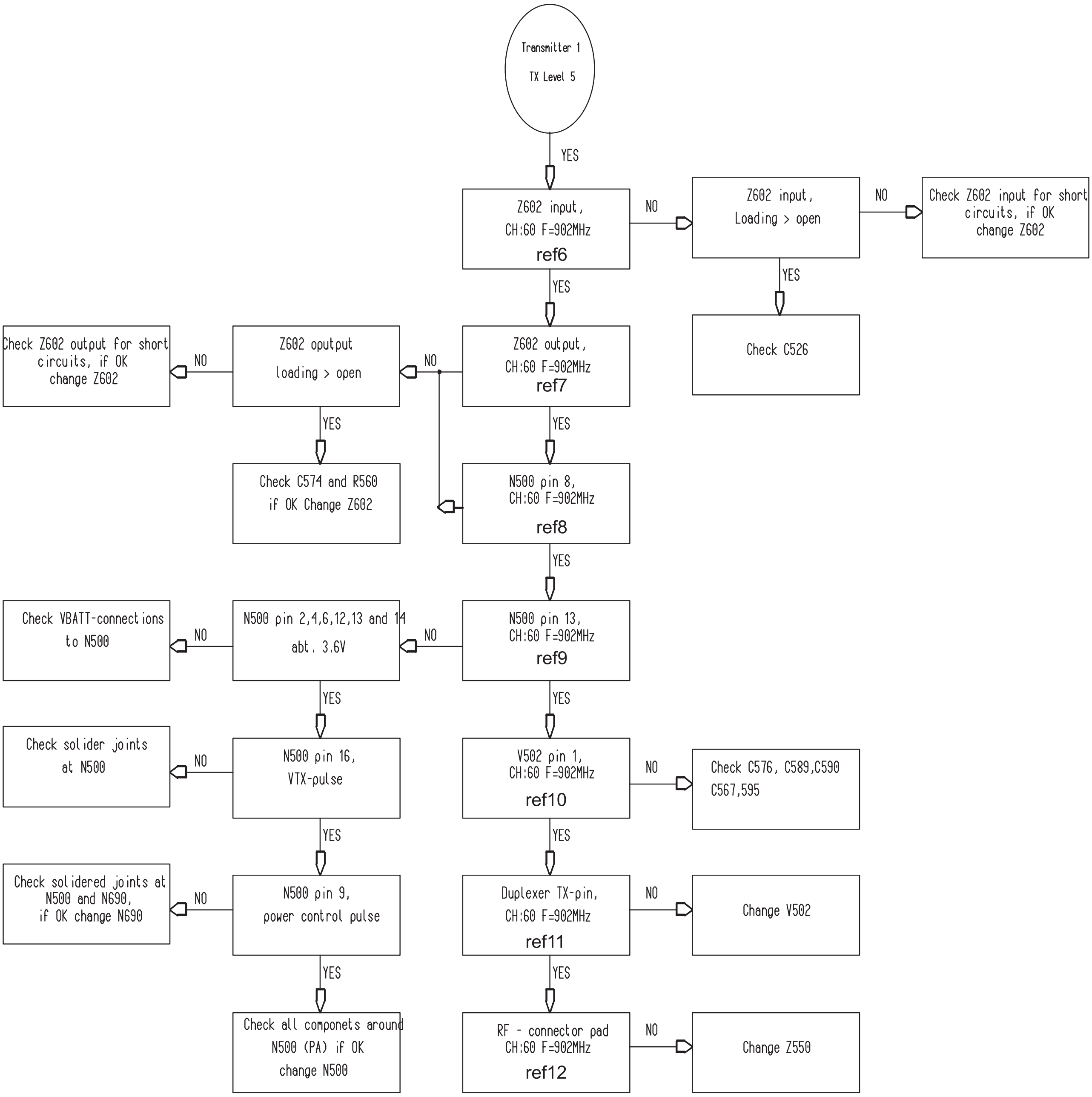
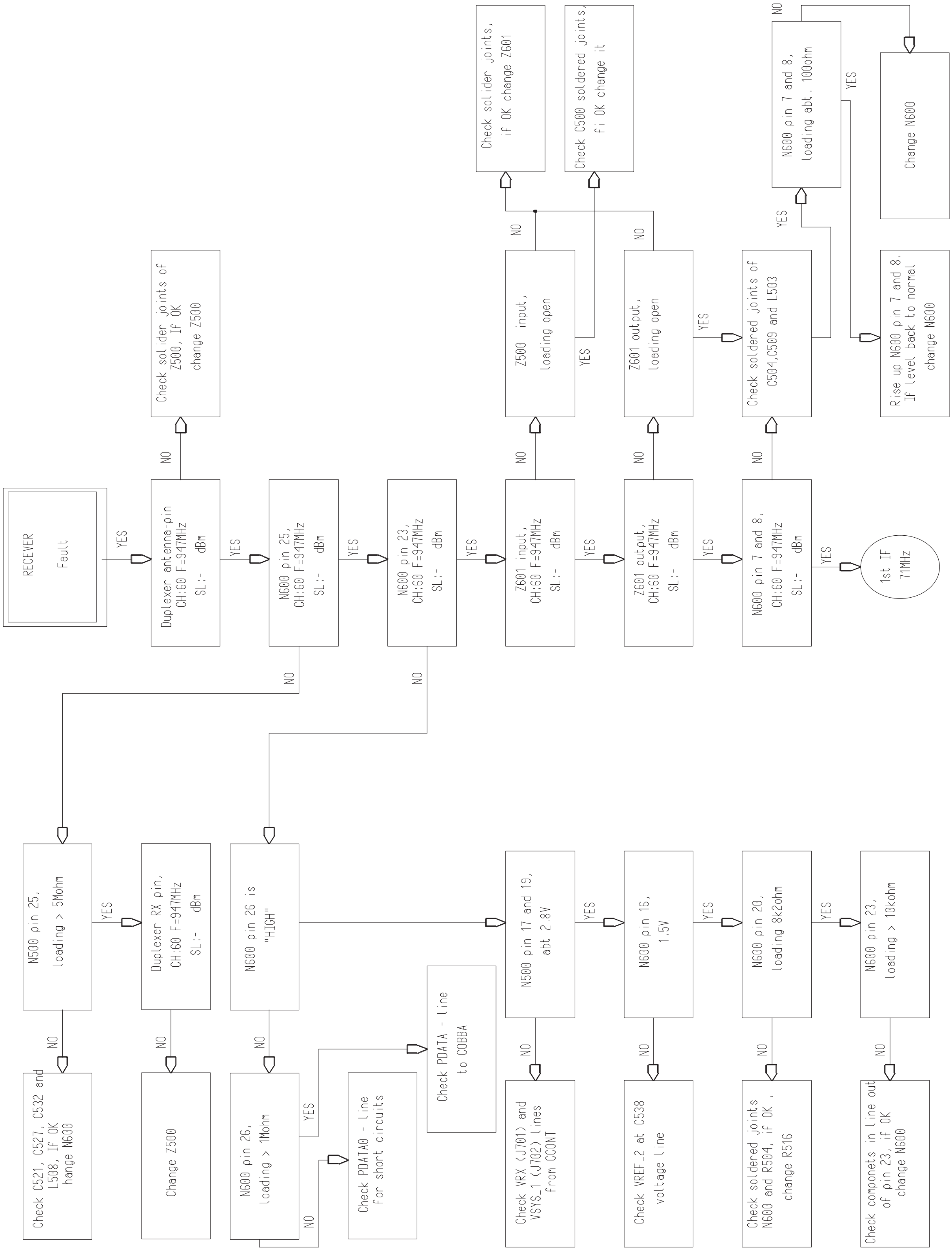


Figure 13. Transmitter 1 TX level 5

Receiver fault

Troubleshooting tree for Receiver fault:



AFC Fault

Troubleshooting tree for AFC fault:

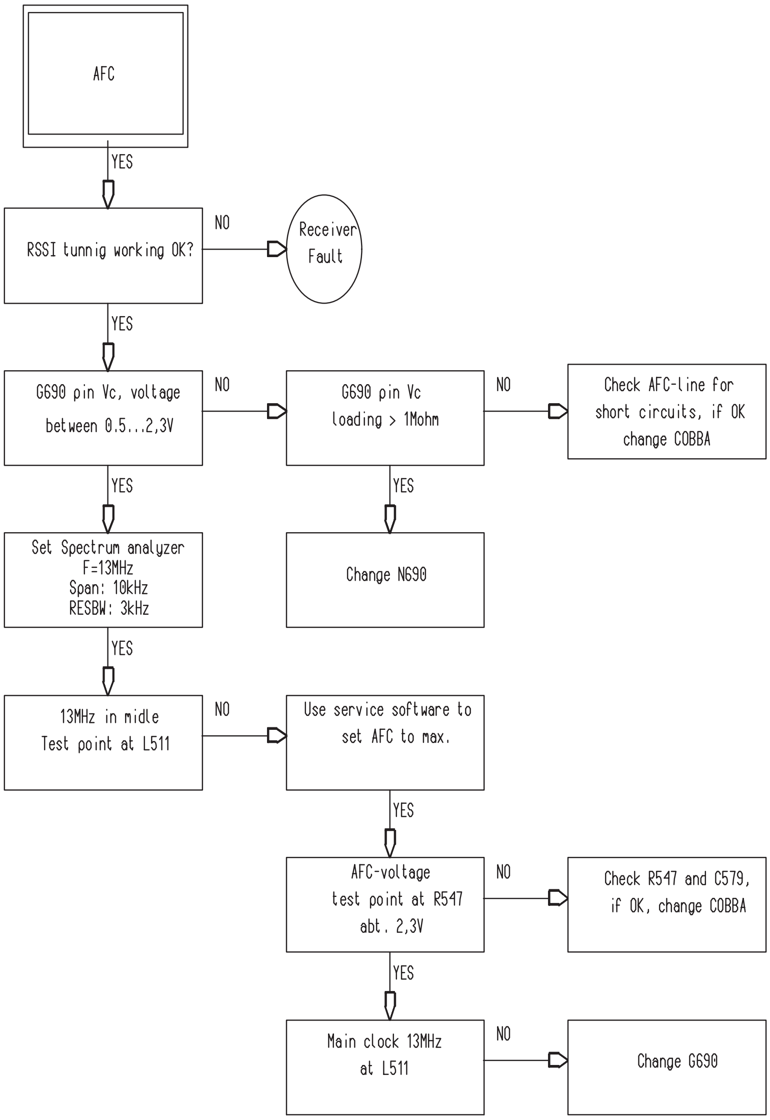


Figure 14. AFC

1st IF

Troubleshooting tree for First IF fault:

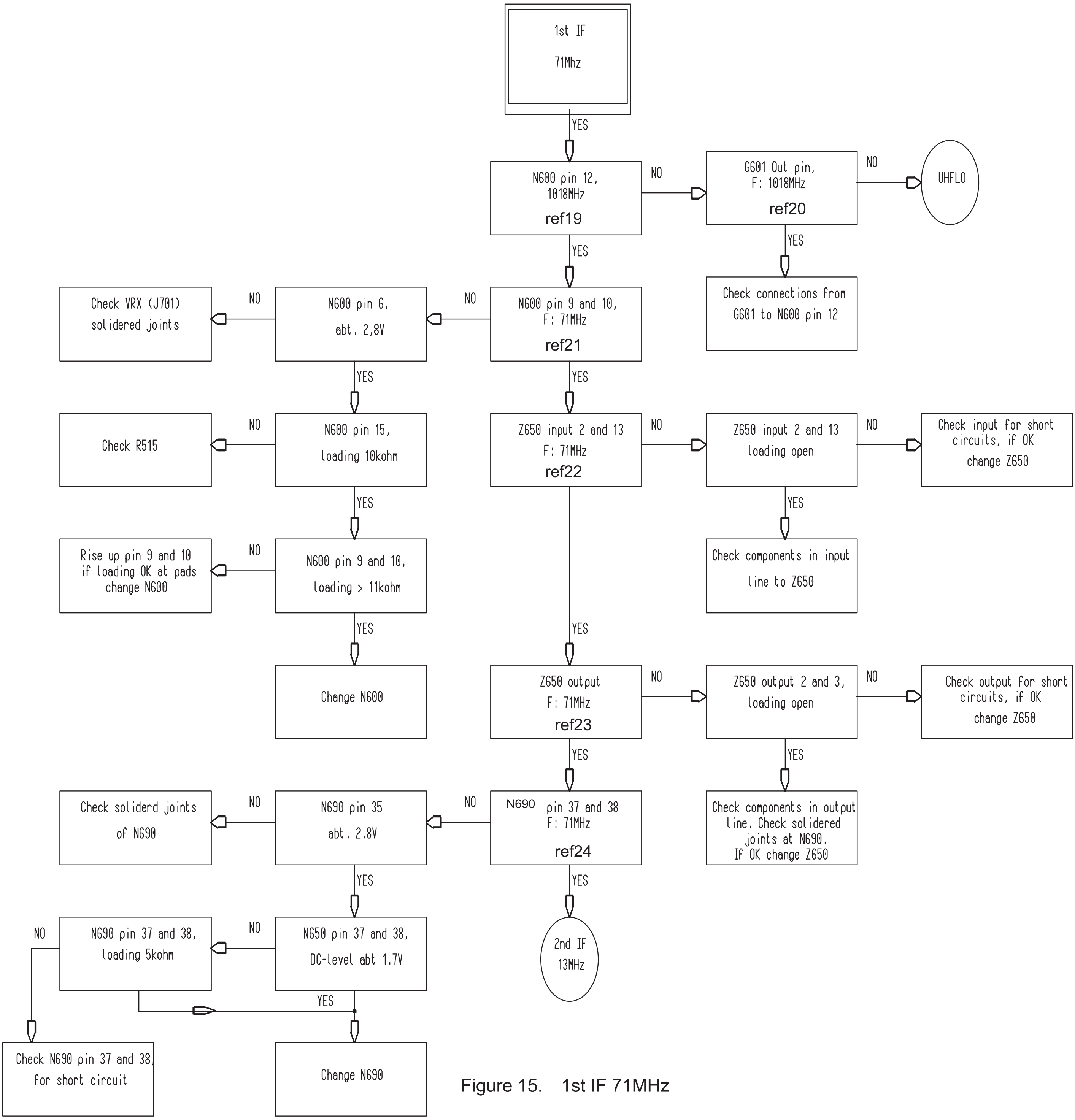


Figure 15. 1st IF 71MHz

2nd IF

Troubleshooting tree for Second IF fault:

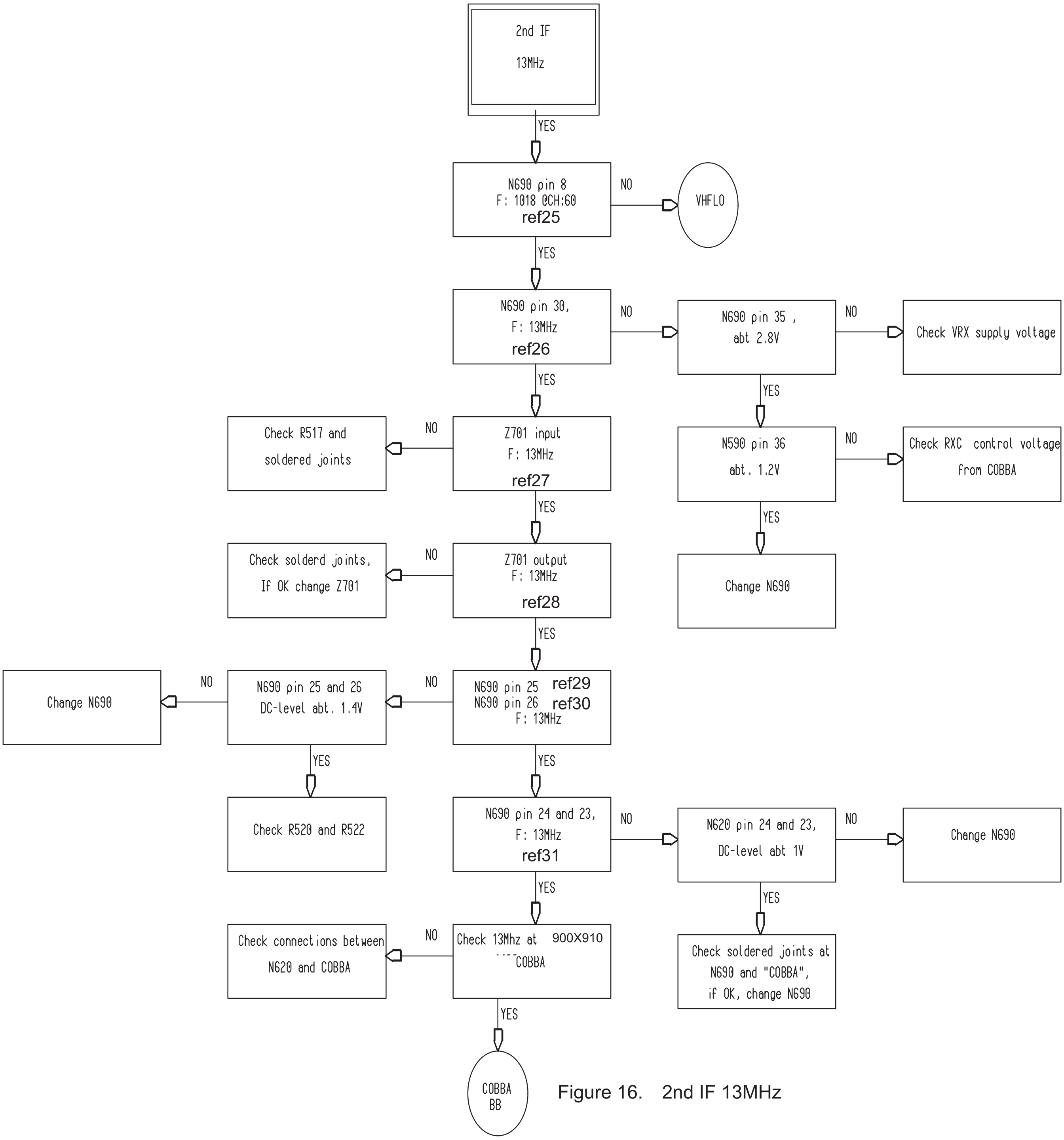


Figure 16. 2nd IF 13MHz

UHF LO

Troubleshooting tree for UHF LO fault:

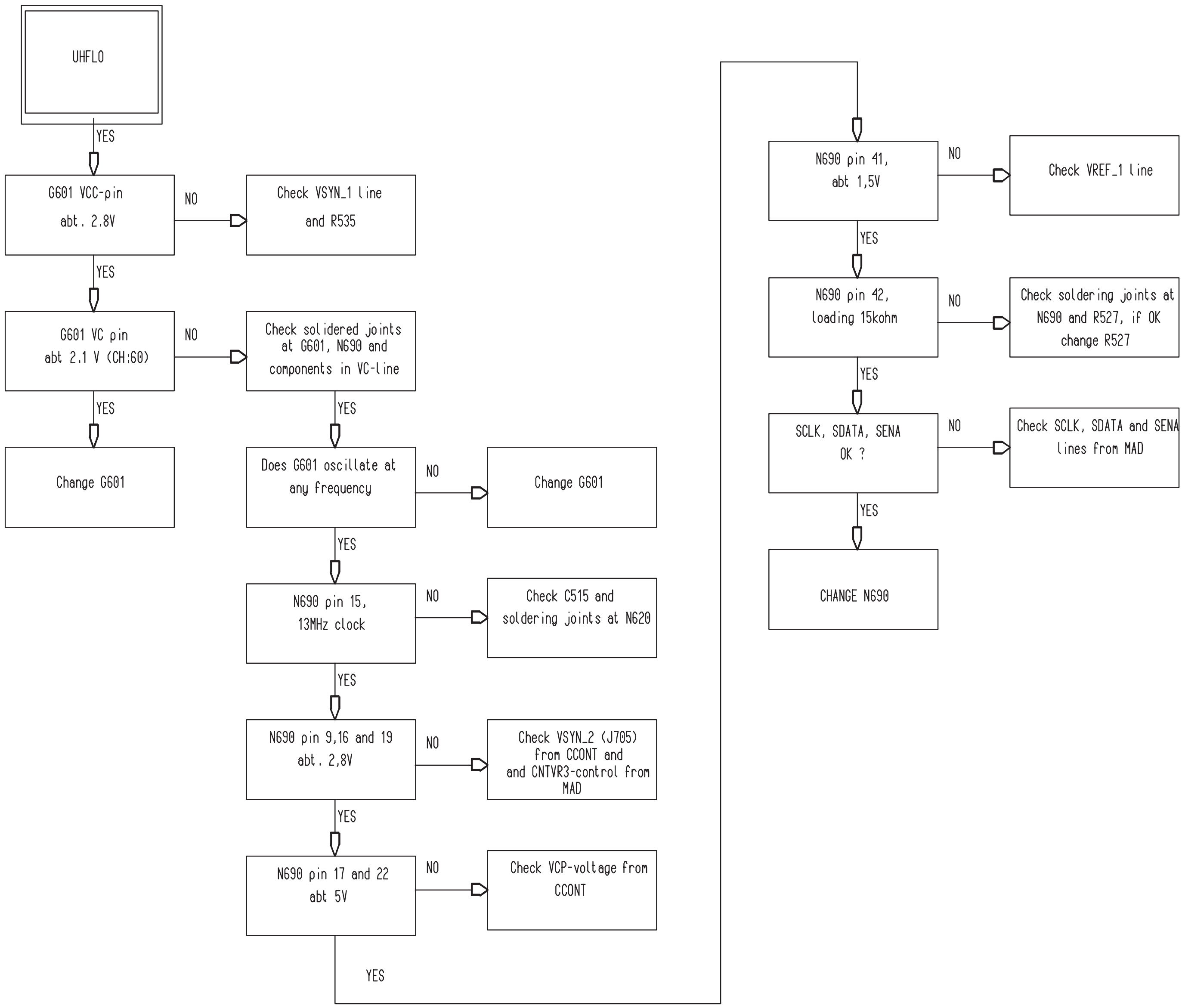


Figure 17. UHF LO

VHF LO

Troubleshooting tree for VHF LO fault:

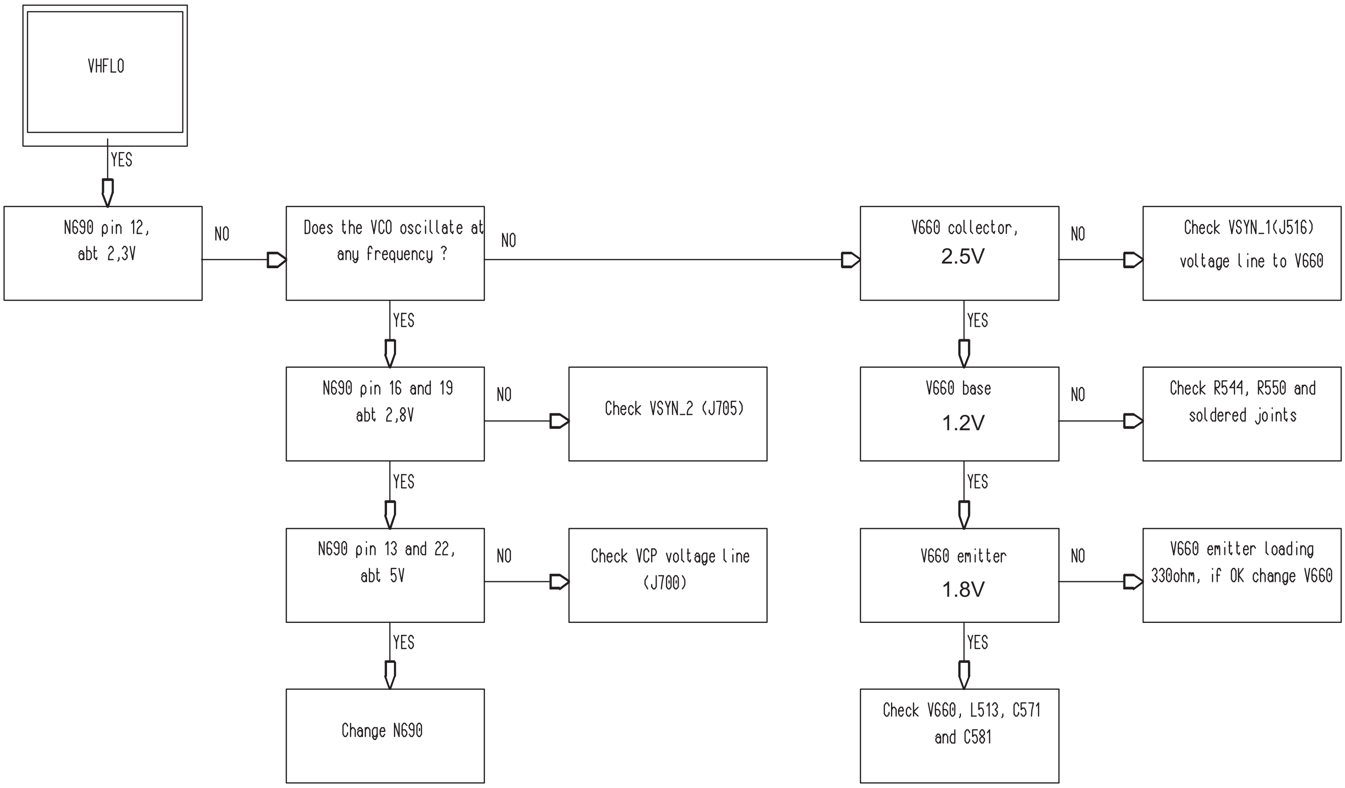


Figure 18. VHF LO

PDA Troubleshooting and Service

The purpose of this sectionis to provide methods to find the component that is malfunctioning in the PDA module of the RAE–2. Due to the large integration scale of used components, it is always not possible to point the faulty component for sure. However the flow diagram introduced here is made to fulfill the aim as well as it is possible.

Required Servicing Equipment:

– PC for the Wintesla
– Service battery BBS–5
– Service cable DAU–9C
– Combox TDC–4
– IR transceiver module JLP–1
– digital multimeter
– oscilloscope
– frequency counter (optional)

Block Diagram

The block diagram of the BS1 PDA is described in the next figure:

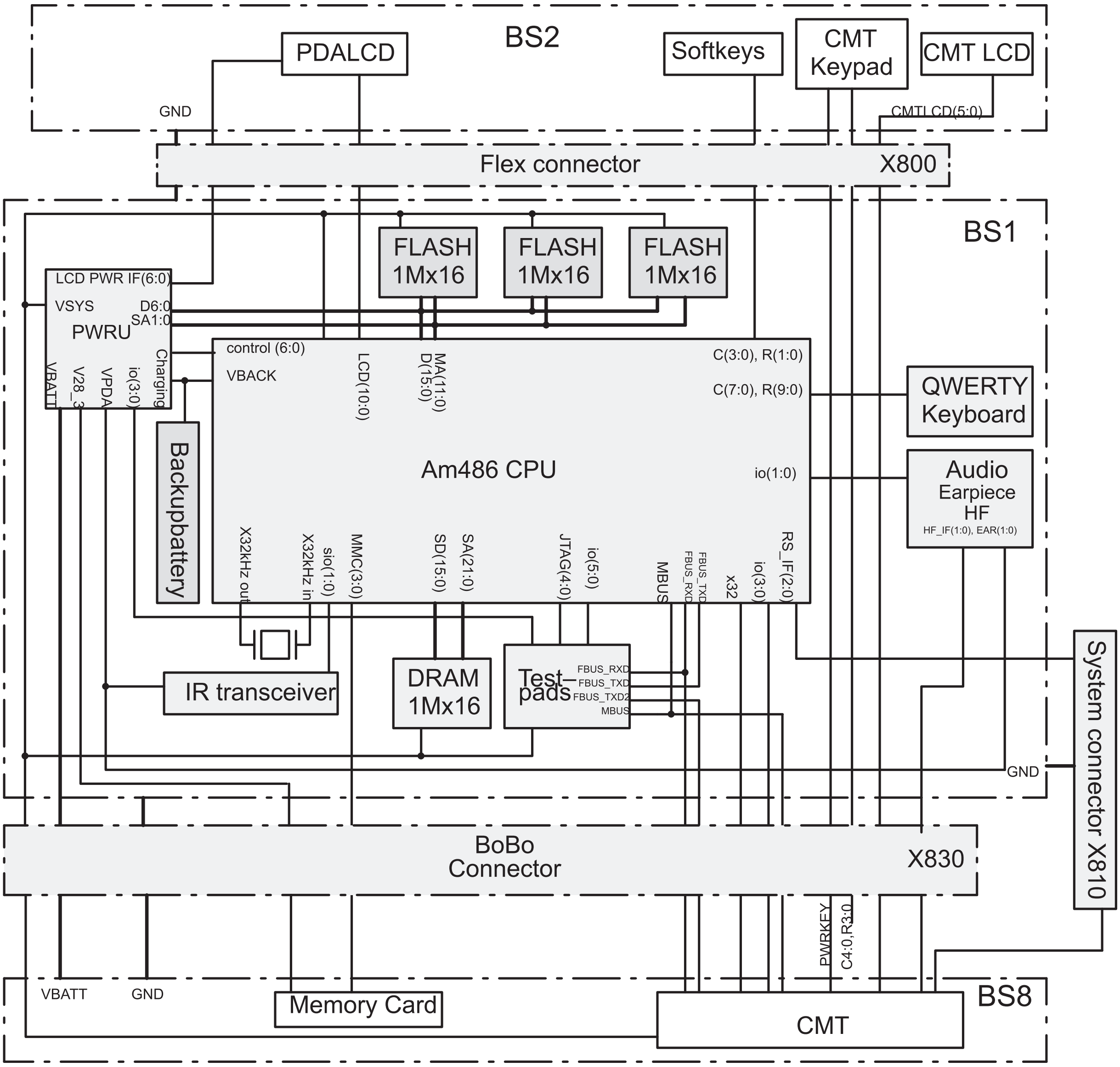


Figure 19. BS 1 PDA block in RAE–2 product

BS1 PDA Components

The following components of the BS1 have an dramatic effect to the functionality of the module, a fault in any of these may cause the module to appear totally 'dead':

– PDA power unit
– CPU
– PLL clock generation circuit
– UCS Flash chip

If the device has some functionality, then the following components, along with the ones above, can be tested:

– DRAM chip

– CS1 and CS0 Flash chips

– Handsfree speaker circuitry

– Earpice circuitry

– IR transceiver

– keyboard

– LCD module

– Memory Card interface

– Serial connections (FBUS and system bus)

BS1 Troubleshooting

The highest level of the RAE–2 PDA troubleshooting diagram is shown in the following figure. All the diagrams are made assuming that there is no visible faults, such as short–circuits or loose pins, on the PDA.

The module check begins with connecting the supply voltage to the PDA. If the current consumption differs a great deal from the normal limits, it is good to proceed to the Power–On check.

During BIOS detects some error during POST it tries to beep the buzzer for further fault analysis for the user. The POST beep codes, number of beeps are in the Appendix A on p.54.

If the current consumption is OK, it can be tried if the wintesla service software is able to get connection to the PDA. If the target PDA does not respond to the pings from the host, it is good to check the Power–On procedure.

When the PDA responds to the wintesla, further peripheral tests may be carried out. The execution order is not significant and it may be freely changed. Along with the actual tests, wintesla offers advanced methods for isolating the possible cause of the fault.

After all the functional tests are working, the device under test should be re–booted, and the normal usability of the GEOS, along with the CMT module should be checked before the PDA can be considered to be fully functional.

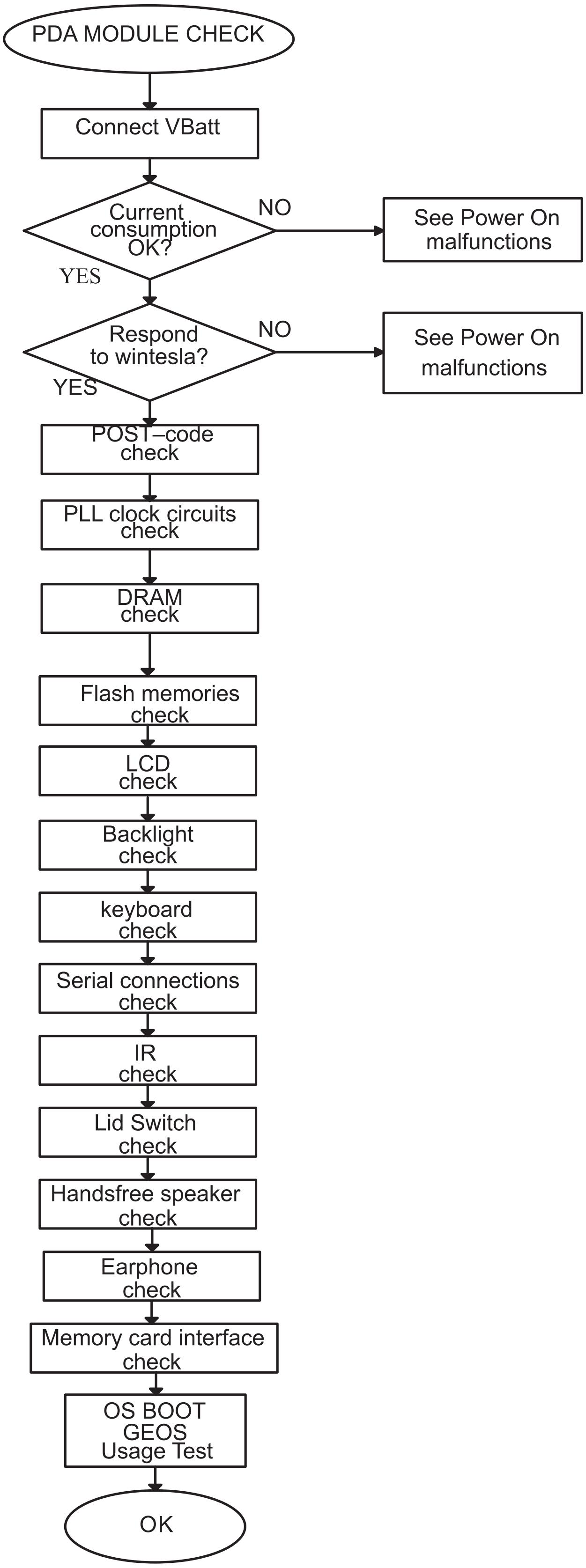


Figure 20. The highest level of the PDA troubleshooting diagrams

Power–on malfunction

The following picture illustrates the troubleshooting diagram for Power–On malfunctions.

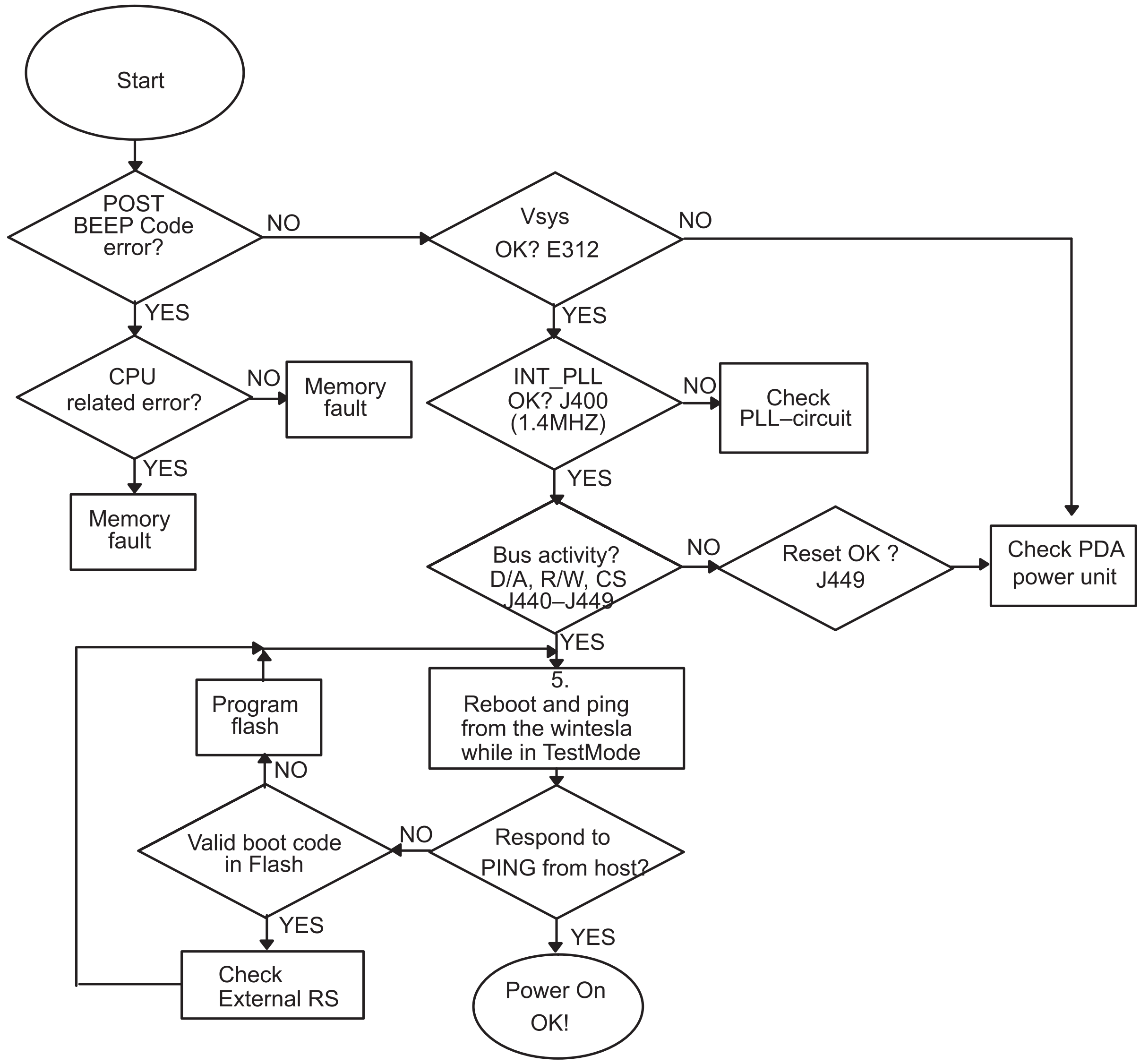


Figure 21. Troubleshooting of the power–on malfunction

Power Circuitry Check

The following figure illustrates how to check power circuits. The upper part of the flowchart must be passed before the swicthable voltages (lower part of the flowchart) can be considered to be alright.

The LCD temperature compensation affects the LCD bias voltage values. Because of this temperature compensation, the LCD bias voltages are different in different temperatures, but anyway bias voltage maximum and minimum values should differ 4 Volts from the typical value (DAC 63) in every temperature.

Figure on the next page.

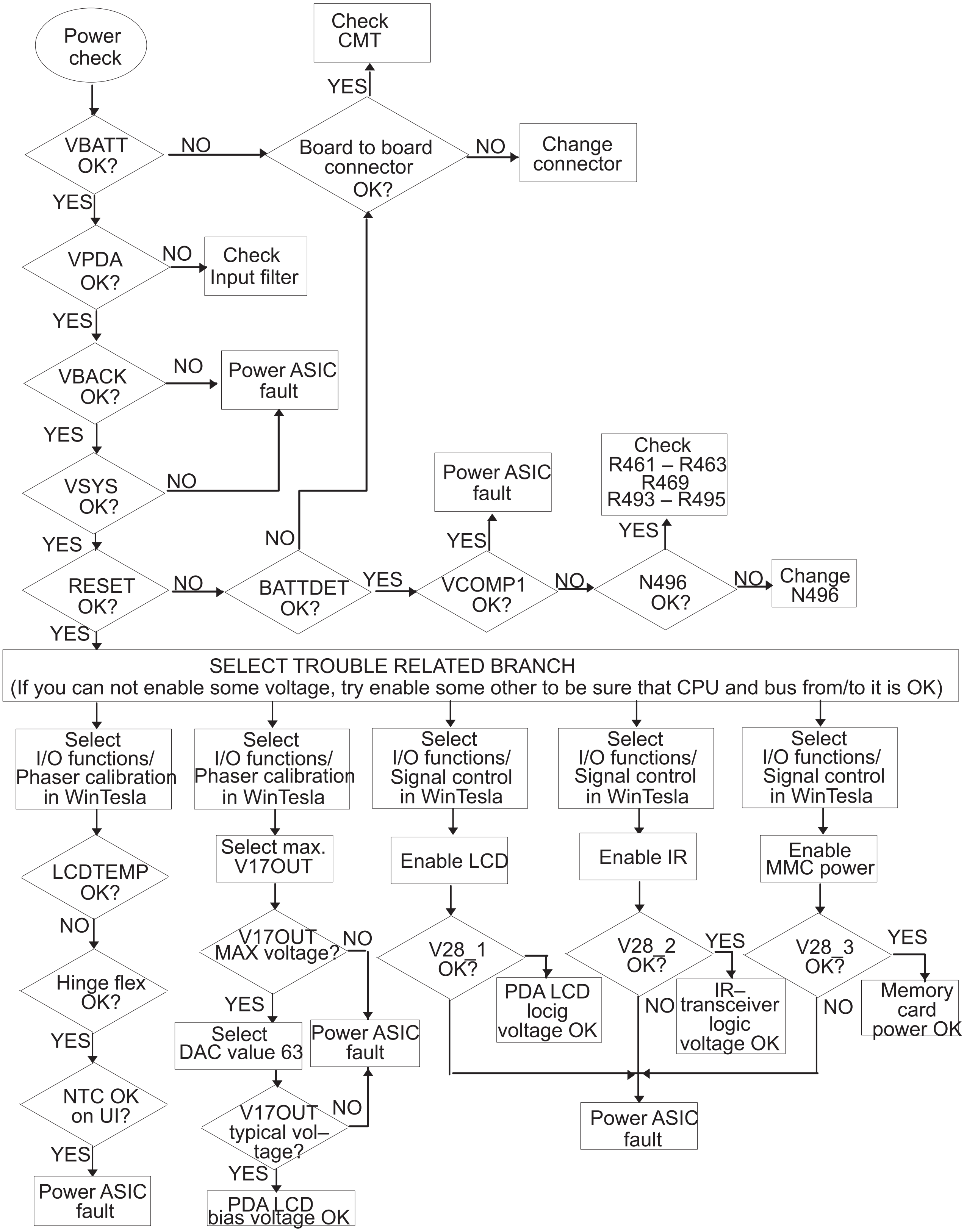


Figure 22. Power unit troubleshooting diagram

Troubleshooting Diagram of the PLL clock generation circuit

The following diagram illustrates how to check PLL clock generation circuits.

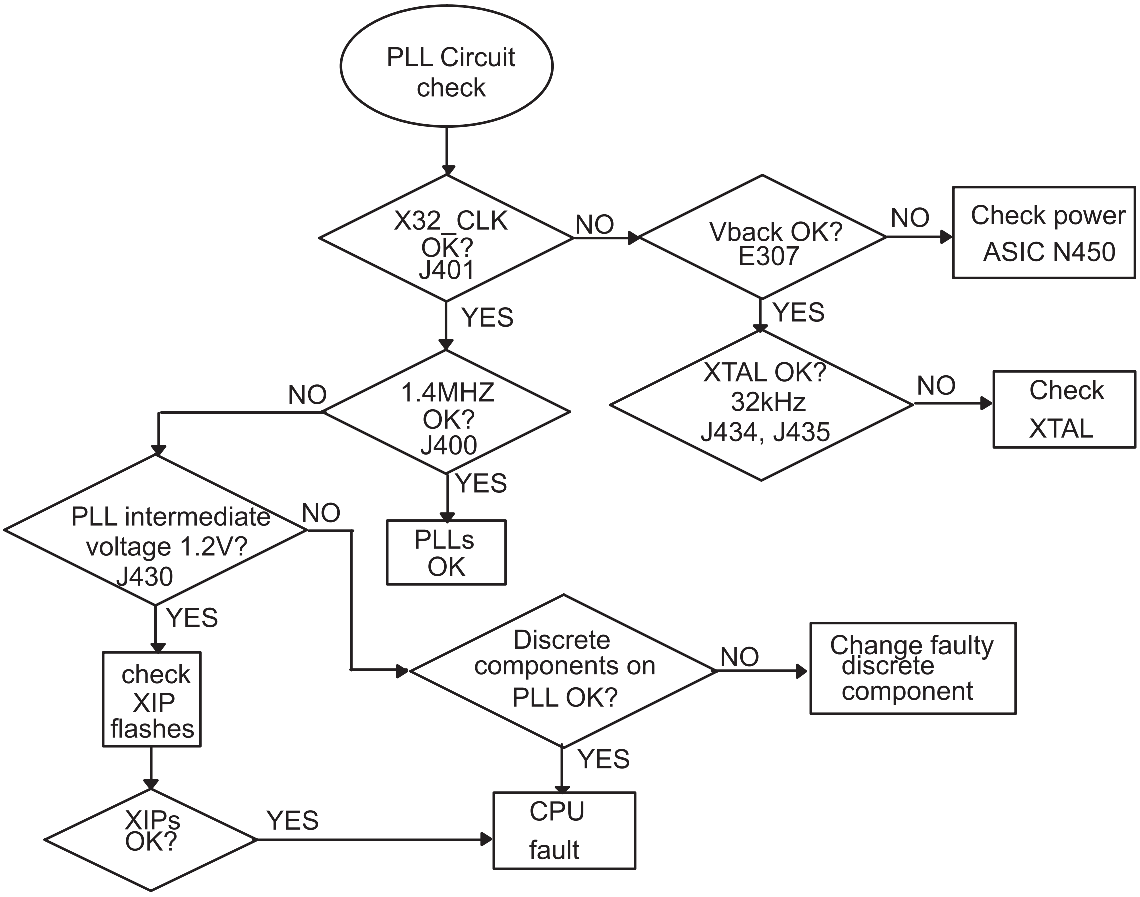


Figure 23. PLL clock generation circuit check

Troubleshooting Diagram of the DRAM

The following figure illustrates how to check DRAM. Open DRAM test in WInTesla and select RandomTest. If test passed DRAM should be alright.

If the test is not passed, run test again and measure the data and control lines activity.

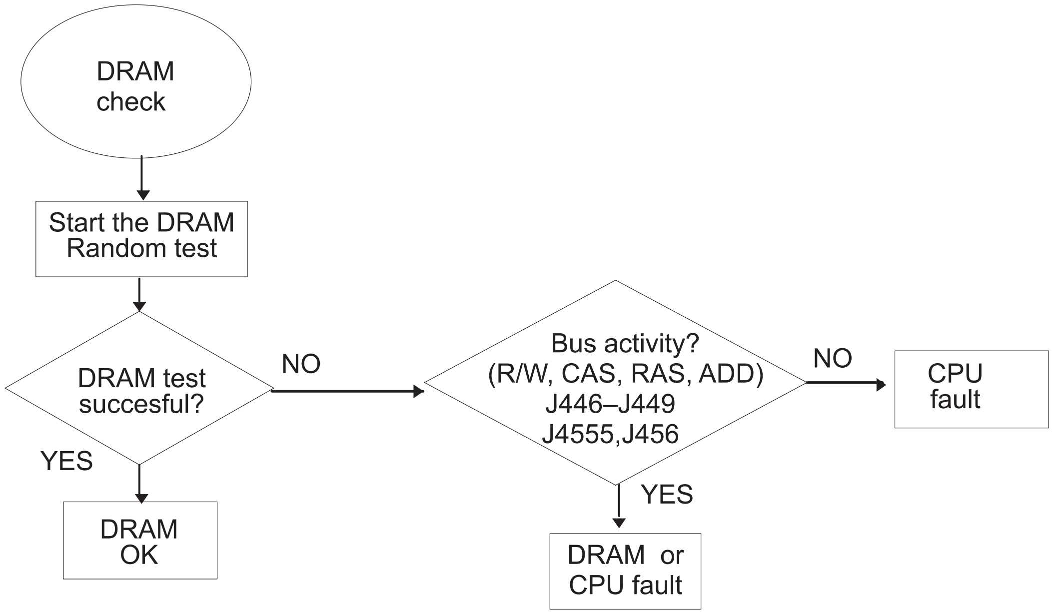


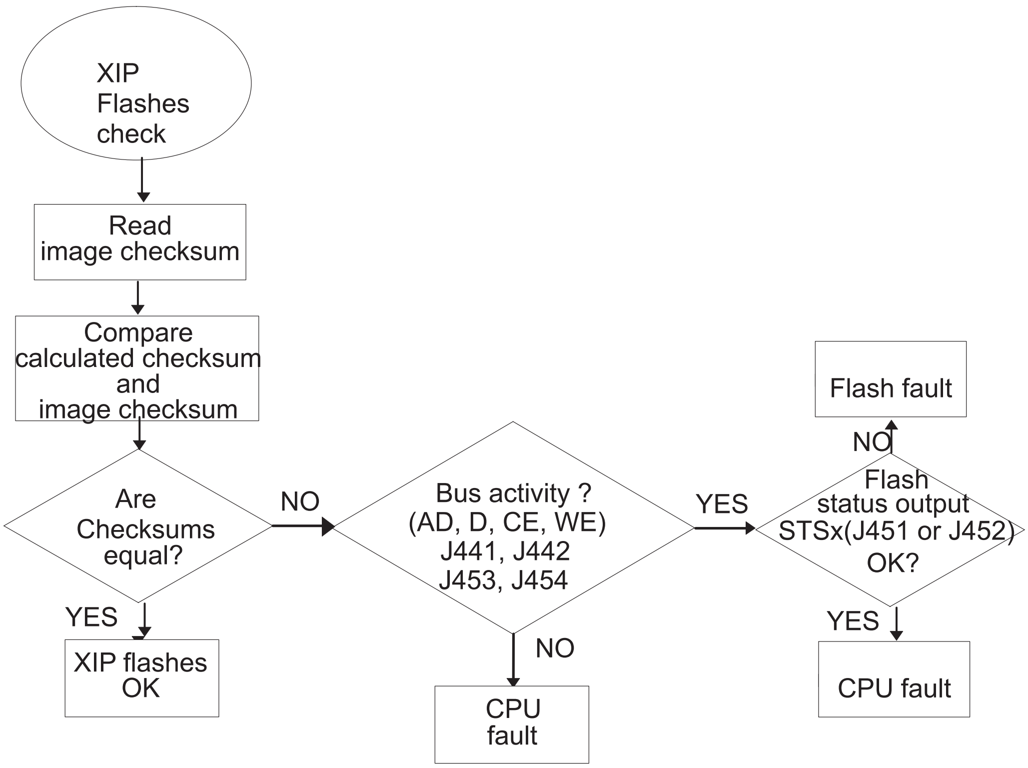
Figure 24. DRAM troubleshooting diagram

Troubleshooting Diagram of the Flash memories

The PDA comprises two kind of flash memories, two XIP (eXecute In Place) flashes and one RFD flash.

The XIP flash can be checked by comparing image checksum and calculated checksum.

If you can read and write from/to RFD flash, it is likely to be OK.



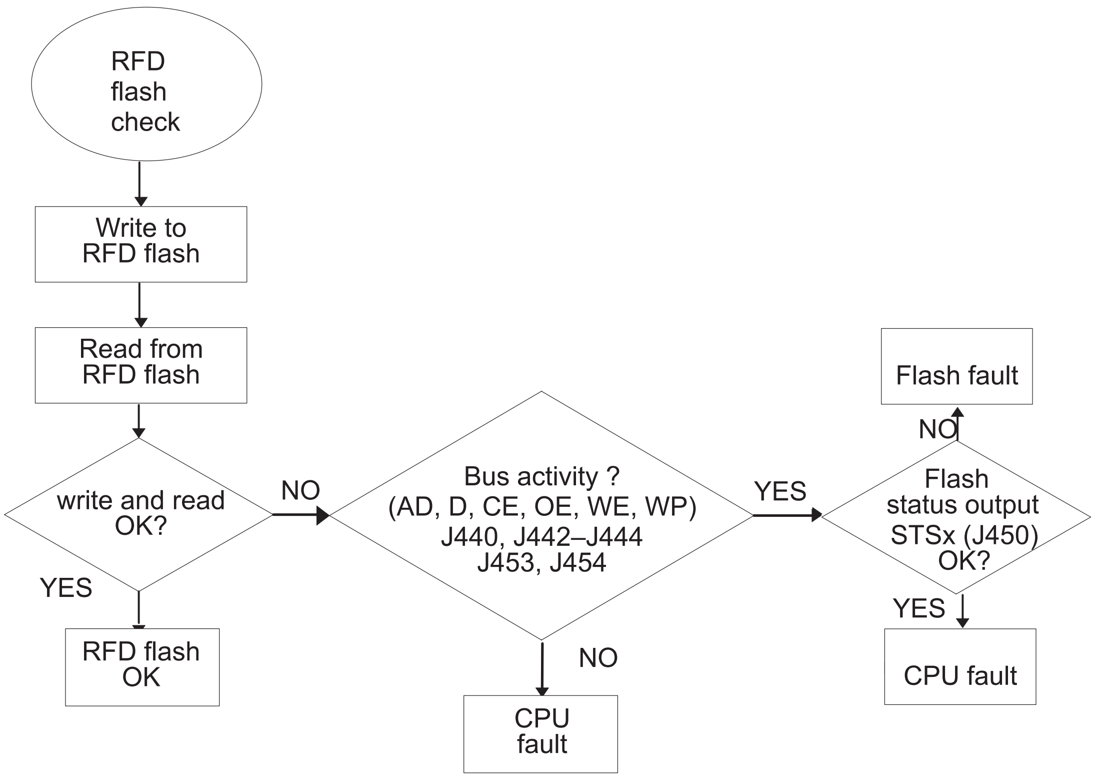


Figure 25. Flash memories troubleshooting diagrams

Troubleshooting Diagram of the LCD

The idea of the following diagram of the LCD Check is to make the difference whether the LCD BS2 module or the PDA BS1 is broken. The case where the fault is in the BS2 module is beyond the scope of this document. The fix in that case is likely the change of the whole module.

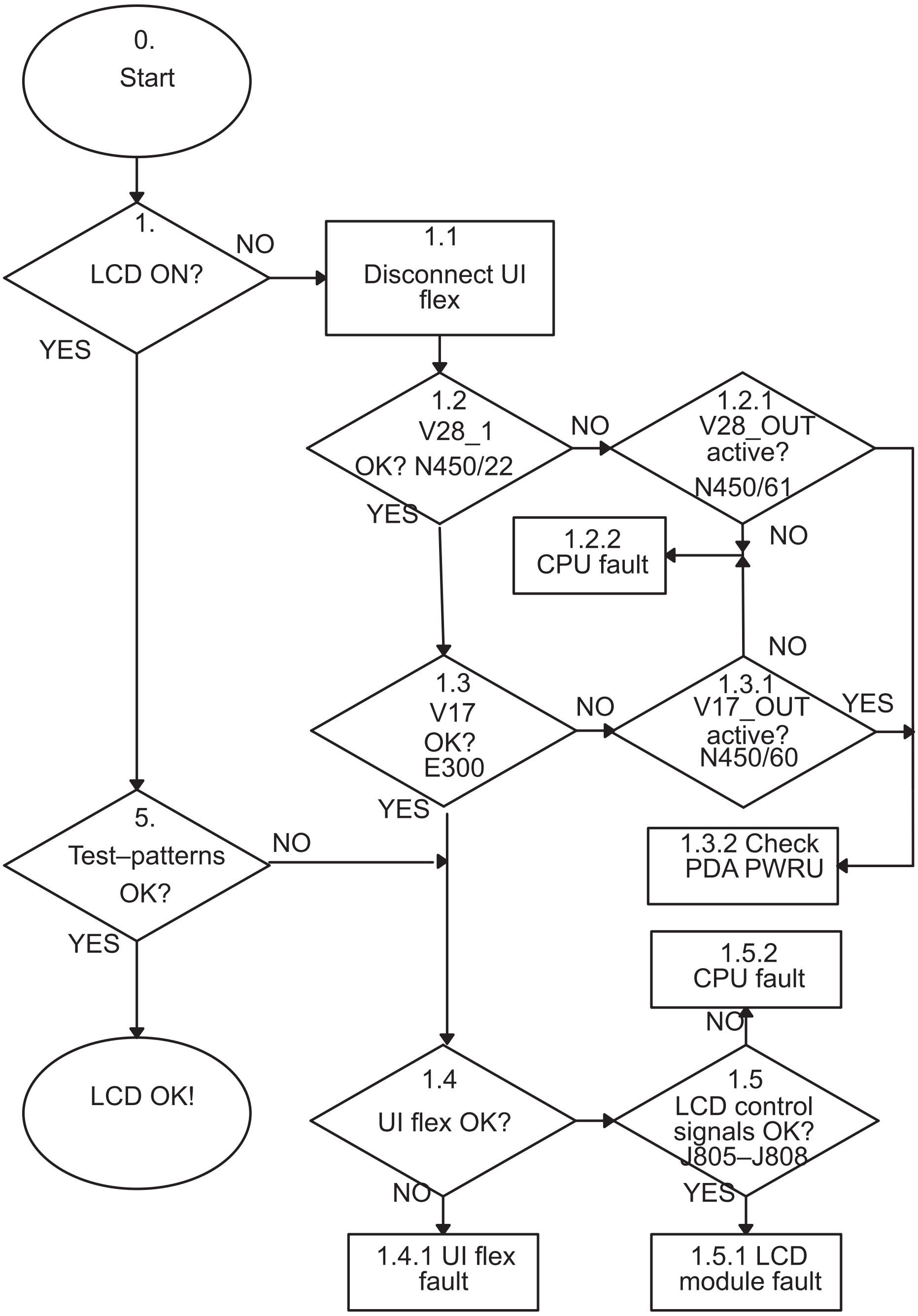


Figure 26. Troubleshooting of LCD signals

Troubleshooting Diagram of the PDA LCD Backlight

This troubleshooting diagram describe troubleshooting procedure on the PDA LCD backlight. If PDA is OK, look then backlight troubleshooting procedure from next chapter UI TROUBLESHOOTING.

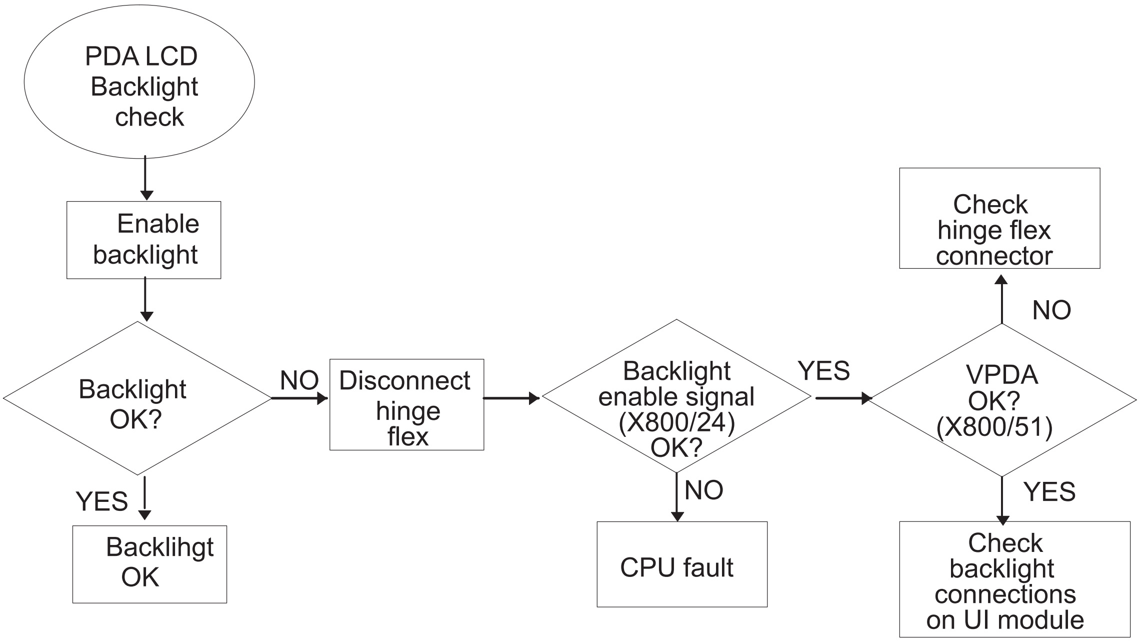


Figure 27. PDA LCD backlight troubleshooting

Troubleshooting Diagram of the PDA Keyboard

This section describe PDA keyboard troubleshooting procedure. Possible cause to keyboard faults are keyboard interface in CPU, broken keymat or keydomes (UI) . Also, dirty keymat or keypad area can cause the fault.

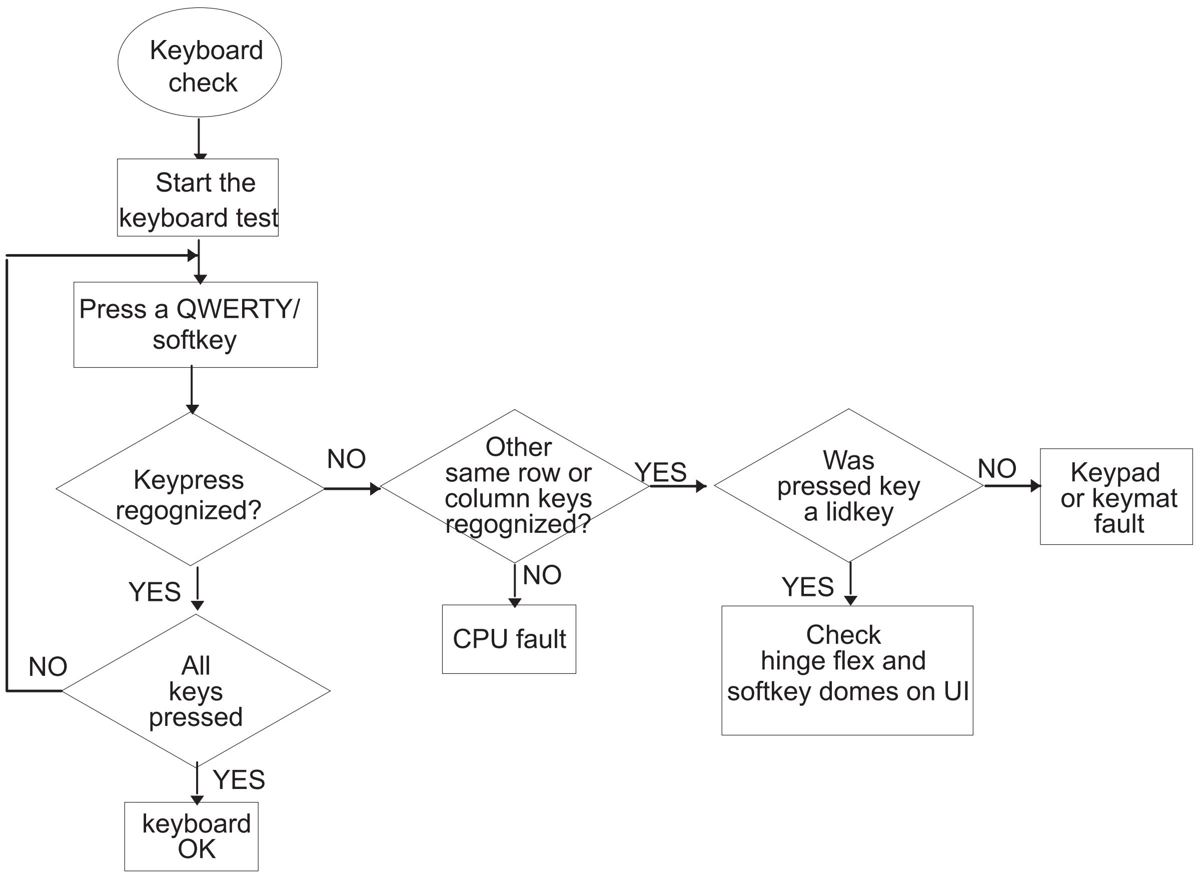


Figure 28. Keypad troubleshooting diagram

Troubleshooting Diagram of the serial connections

External bus connection is alright if the device is PINGing, if not is good to check system connector and discrete components on RX and TX lines. External bus use RS232 data protocol, but signal voltage levels on PDA and system connector are only 2.8V digital voltage levels. External buffer cable needed (DLR–2) for connecting to PC.

Serial connection between CMT and PDA (FBUS) can be checked as following flow chart described.

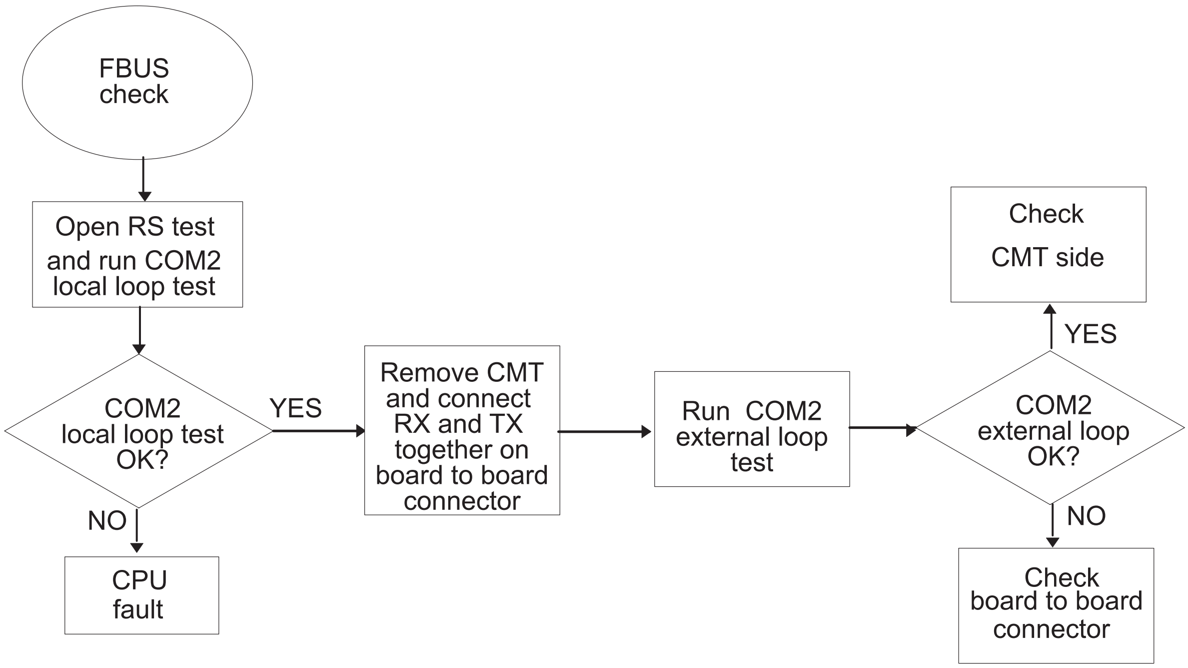


Figure 29. FBUS troubleshooting diagram

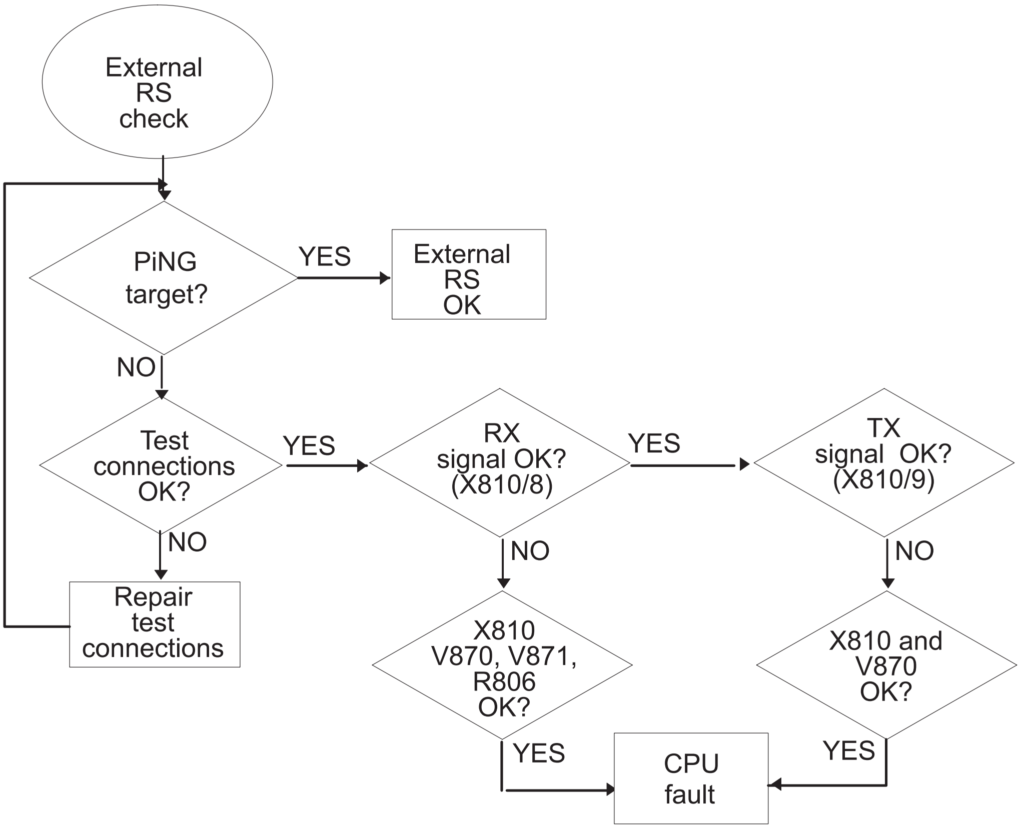


Figure 30. External serial connection troubleshooting diagram

Troubleshooting Diagram of the IR connection

This section describe infrared connection troubleshooting procedure.
IR test need Combox TDC–4 with IR transceiver JLP–1.
Place PDA so that IR transceiver have clear light route to JLP–1 and run the IR test. If test not passed follow flowchart to find out the fault.
IR shutdown is not in use.

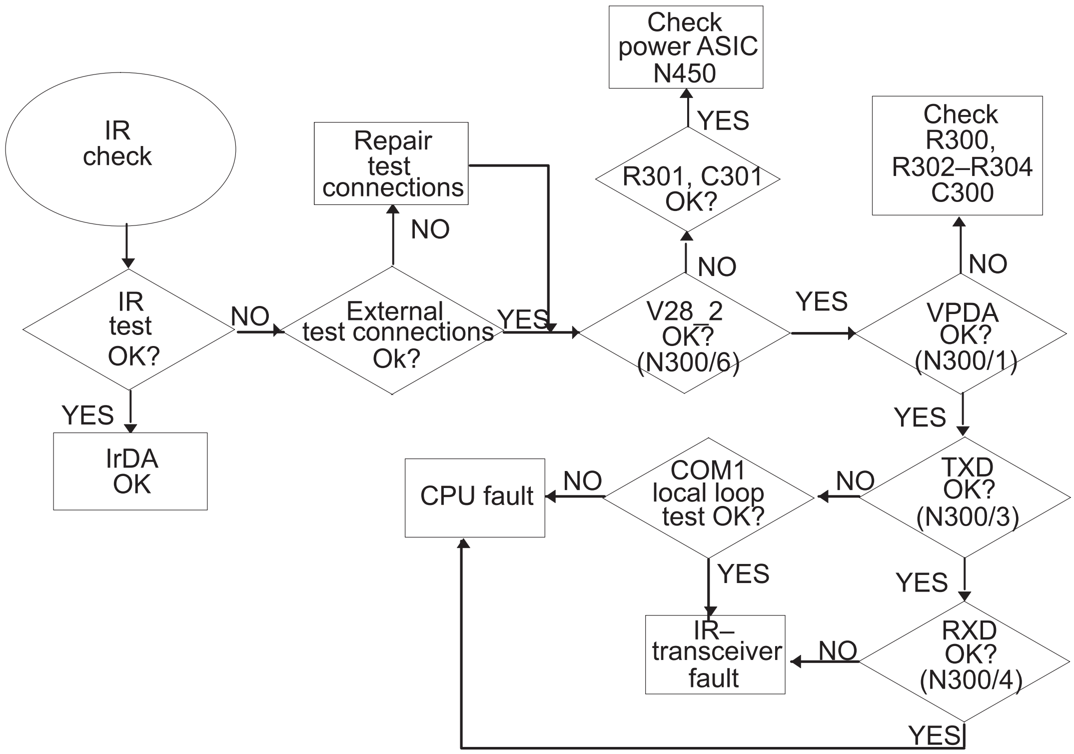


Figure 31. IR connections troubleshooting diagram

Troubleshooting Diagram of the lid switch

The idea of this diagram is to find out whether the CPU or the reed relay circuit is not working.

If CPU and reed relay circuit on PDA is alright, then possible cause of fault is magnet in lid.

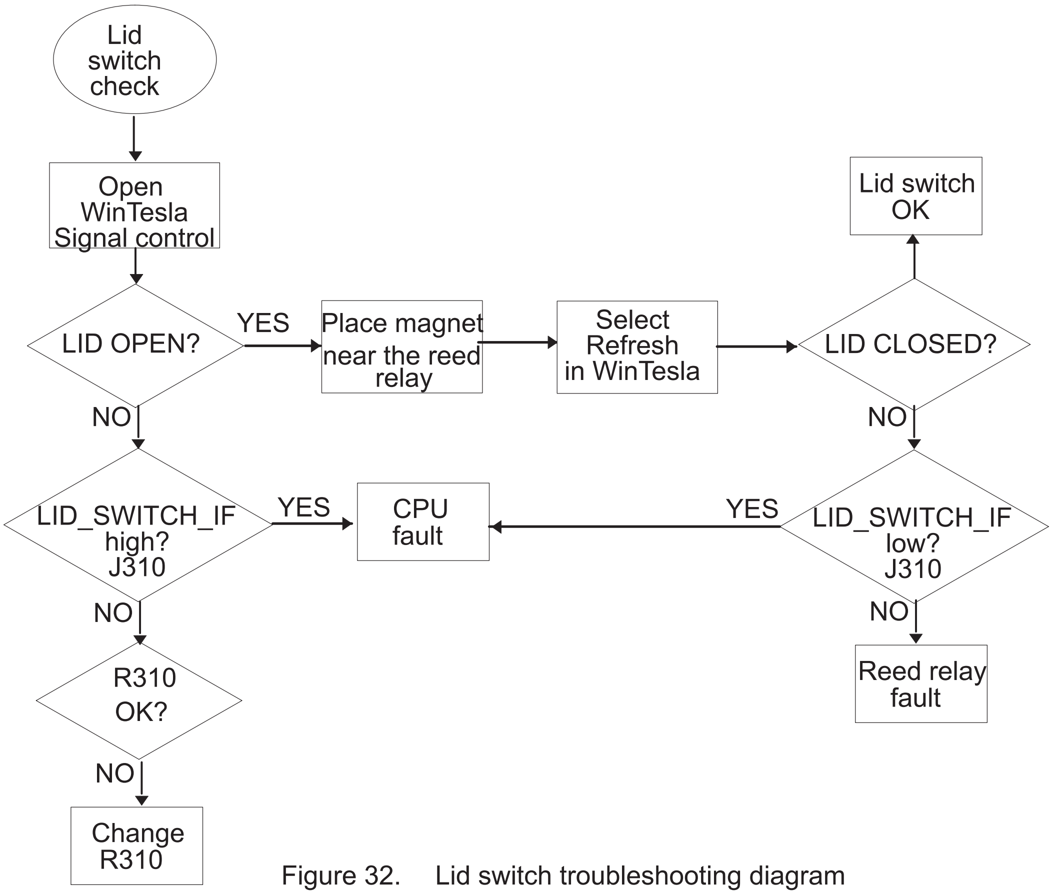


Figure 32. Lid switch troubleshooting diagram

Troubleshooting Diagram of the HF Speaker

The idea of this diagram is to find out whether the CPU, loudspeaker, or power amplifier or it circuitry is not working.

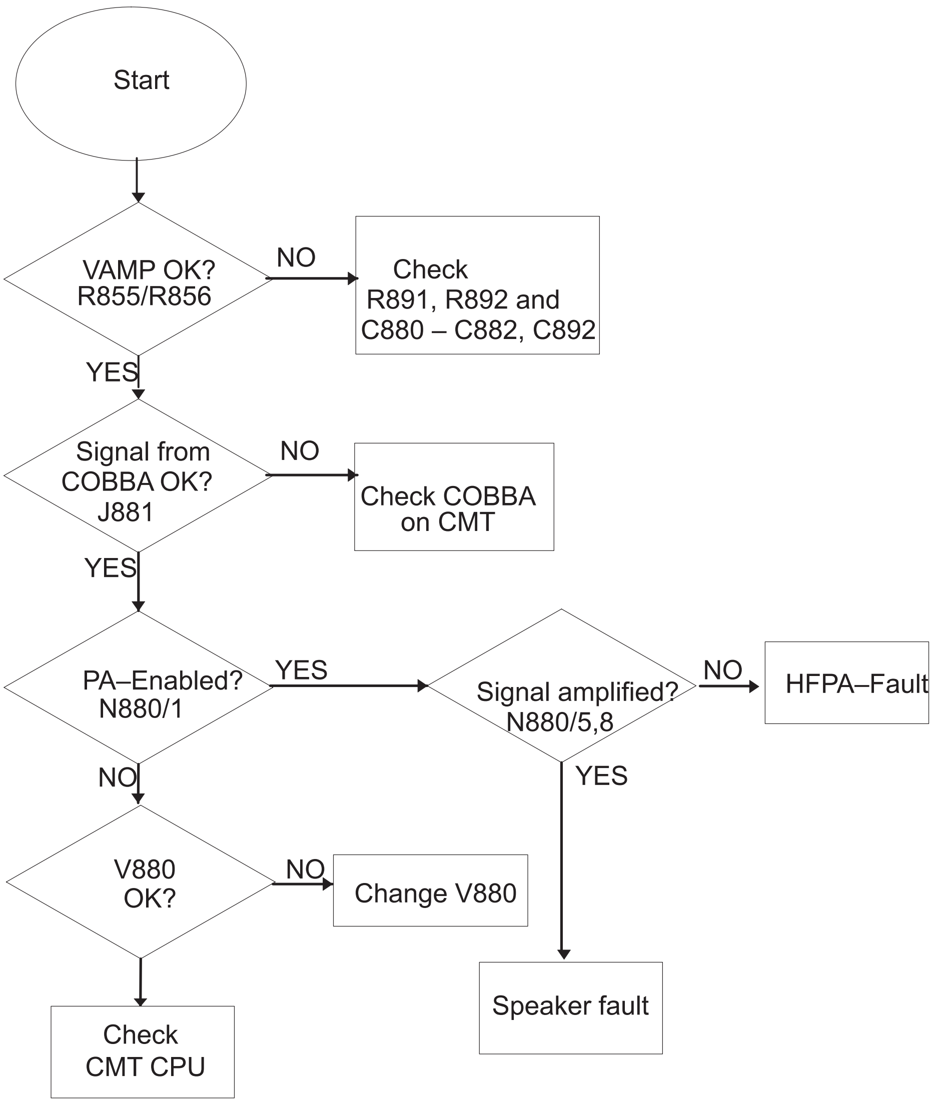


Figure 33.   HF–Speaker troubleshooting diagram

Troubleshooting Diagram of the Earpiece

The following diagram illustrates how to check earpiece connections on the PDA side.

Run the wintesla buzzer test. If the sound is not good then check earpiece connections as following flowchart illustrates.

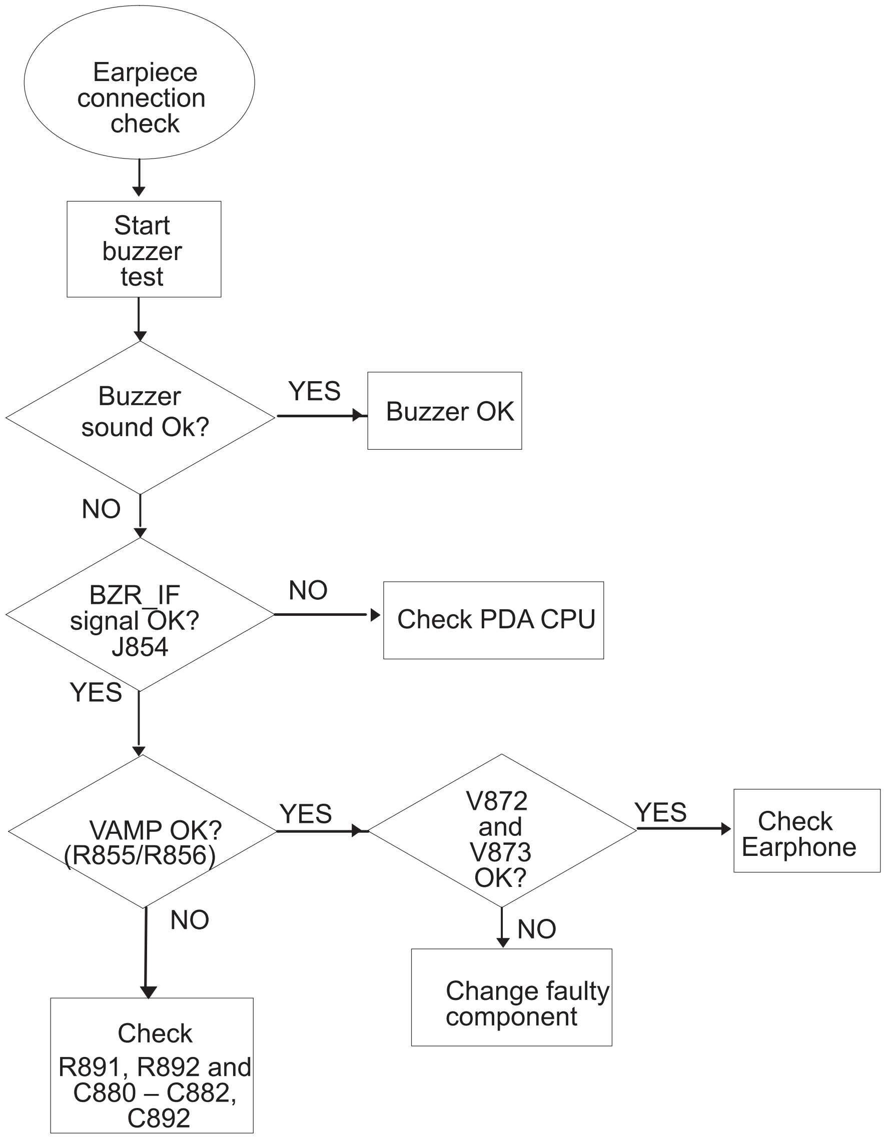


Figure 34. Earphone troubleshooting diagram

Troubleshooting Diagram of the Memory Card interface

To check the memory card interface:

- Take a good memory card and place it in the memory card connector.
- Run Wintesla MMC test. If test failed then take memory card out and run test again.
- Measure memory card system voltage and bus signals when test running.

If the signal and the card voltage are OK, then the interface is likely to be OK. If everything is not alright check interface connections as the flowchart illustrate.

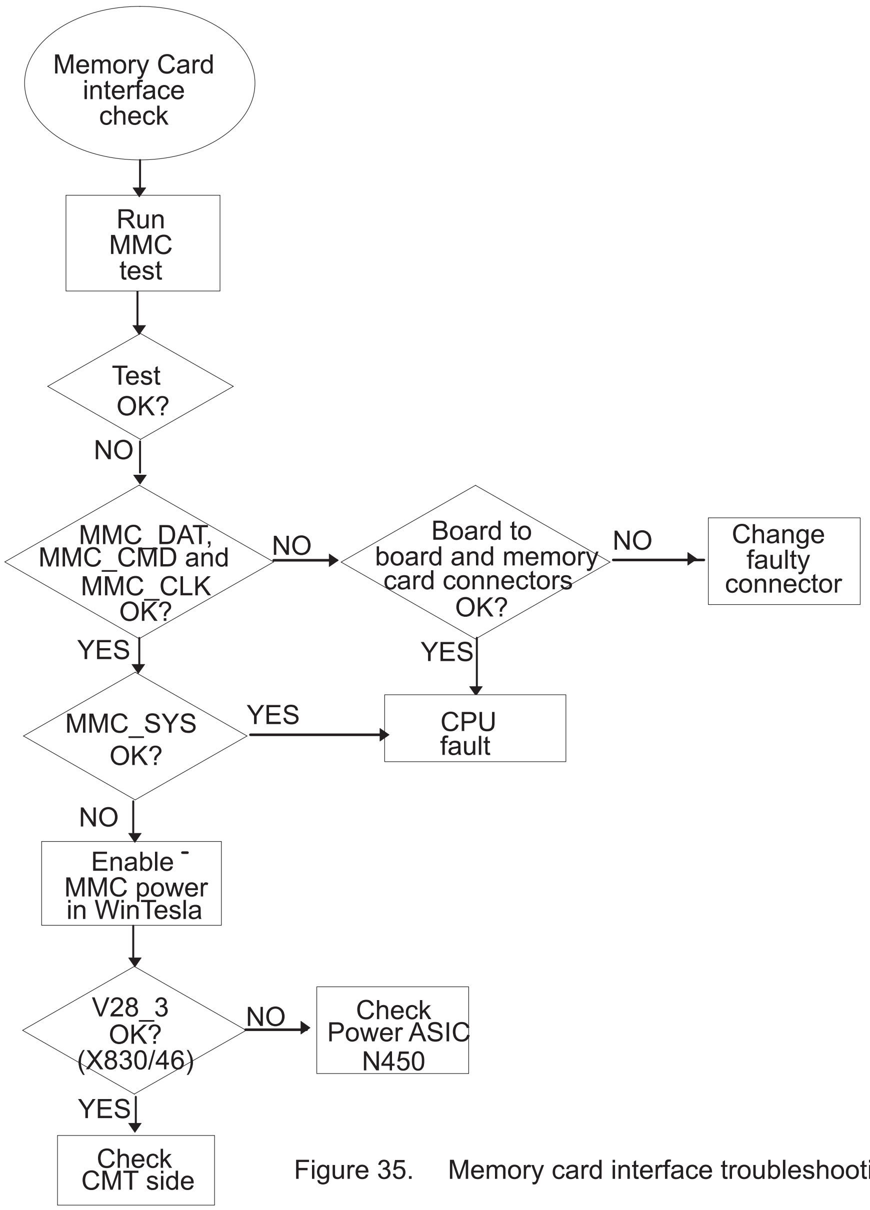


Figure 35. Memory card interface troubleshooting diagram

POST BEEP Codes

1	Memory refresh is not working.
3	Memory failure in 1st 64kB of memory.
4	Timer T1 not operational.
5	CPU test failed.
6	Gate A20 failure.
10	CMOS shutdown register failed.
13	Exhaustive low memory test failed.
14	Exhaustive extended memory test failed.
15	CMOS restart byte can’t hold data.
16	Address line test failed.
18	Interrupt controller failure.

UI Troubleshooting

Mechanical Troubleshooting

In mechanical failures it is better to replace a whole unit or module than try to fix it in service. The replaceable units or modules on BS2 UI module are:

– BC2 CMT LCD module
– PDA LCD display
– UI PCB
– EL backlight panels
– Keydome sheets

Keyboard Troubleshooting

– Equipment: Resistance meter (multimeter)

– If CMT keyboard does not function when the lid is closed, it is possible that reed relay (in the BS1 module) is damaged. If text ”Please close cover” comes to CMT LCD when a CMT key is pressed when lid is closed, the reed relay is probably damaged.

– Check that the dome sheets are properly placed. Improperly placed dome sheet may cause malfunction of some key(s) or power down of the CMT when a key is pressed.

Table 1. CMT keyboard checklist.

Non–functioning CMT keys	Check components
6, 9, #	R704, C707
1, 2, 3, Soft_left	R705, C706
4, 5, Send, Up	R705, C714
7, 8, End, Down	R705, C713
0, *, Mode, Soft_right	R706, C712
3, 6, Send, End, Mode	R706, C708
9, Soft_left, Soft_right, Up, Down	R707, C709
1, 4, 7, #, *	R707, C710
2, 5, 8, 0	R708, C711

CMT LCD Module Troubleshooting

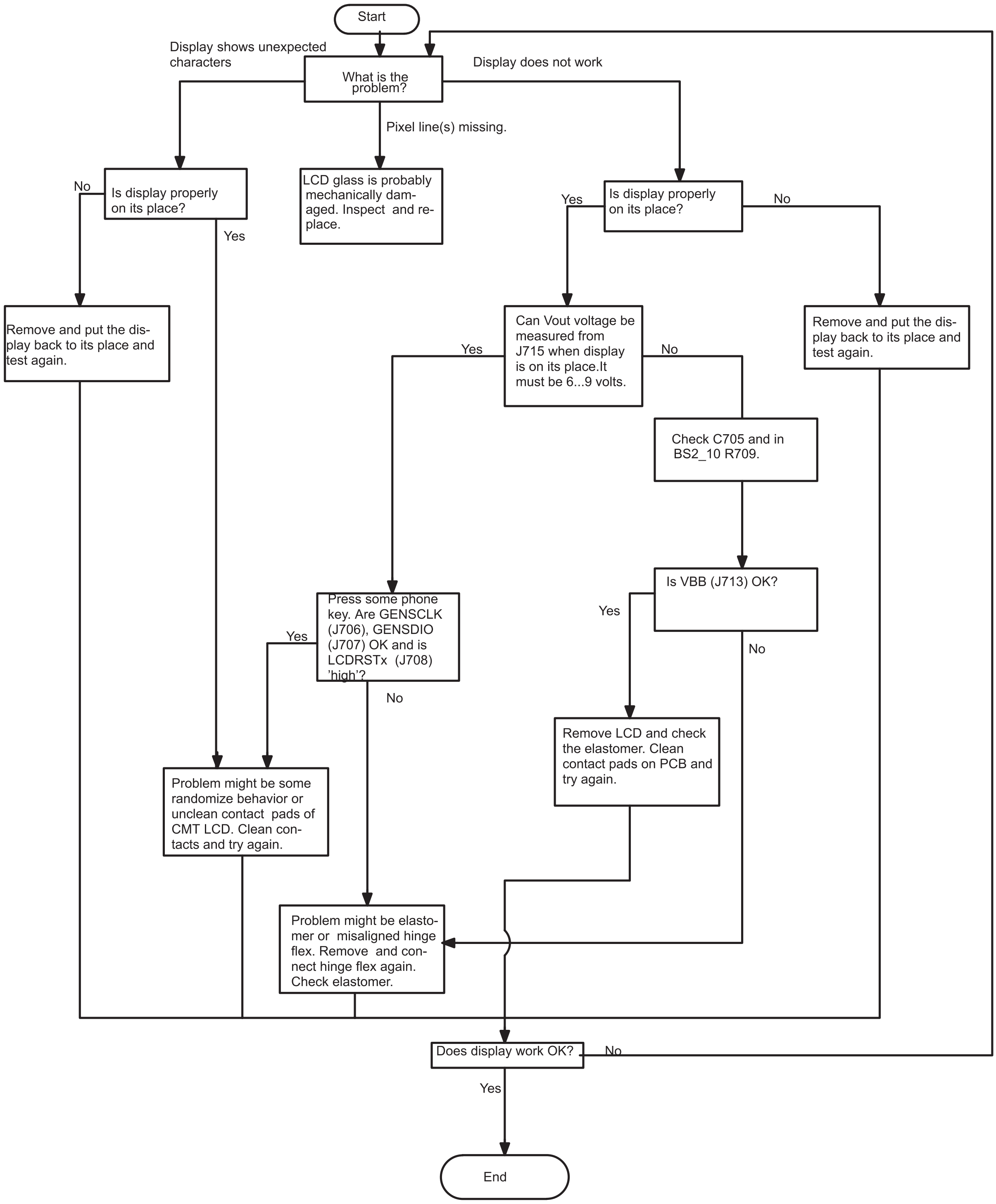


Figure 36. Flow chart for the troubleshooting of CMT LCD module.

– Testing equipment: Multimeter and oscilloscope.

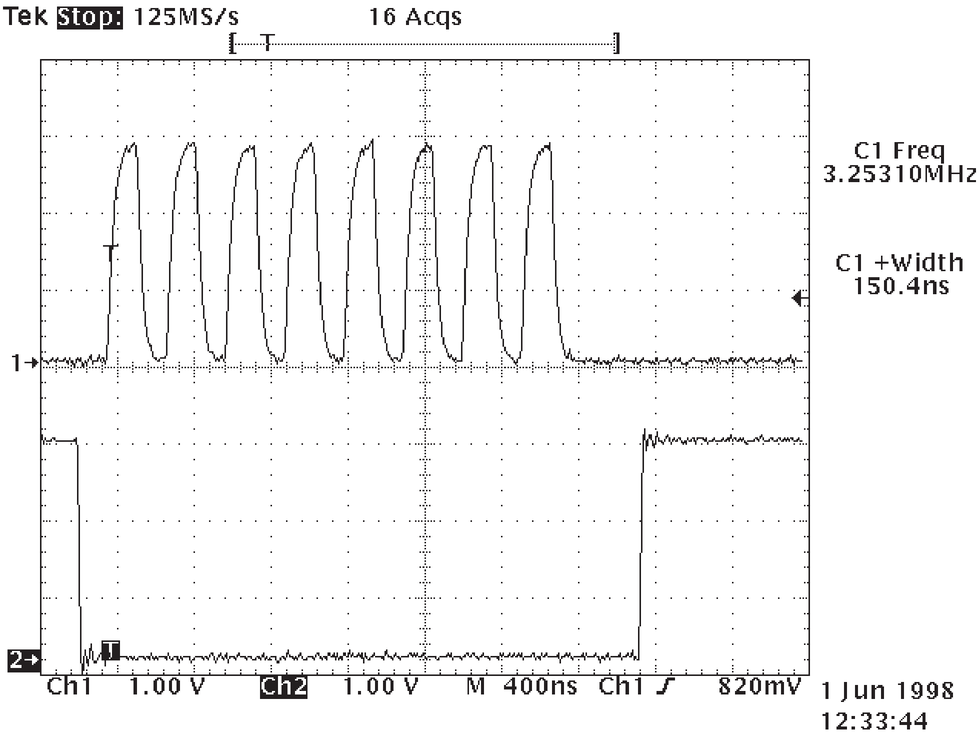


Figure 37. GENSCLK (J706) and LCDCSx (pin 5/H700) , LCD active after pressing a key.

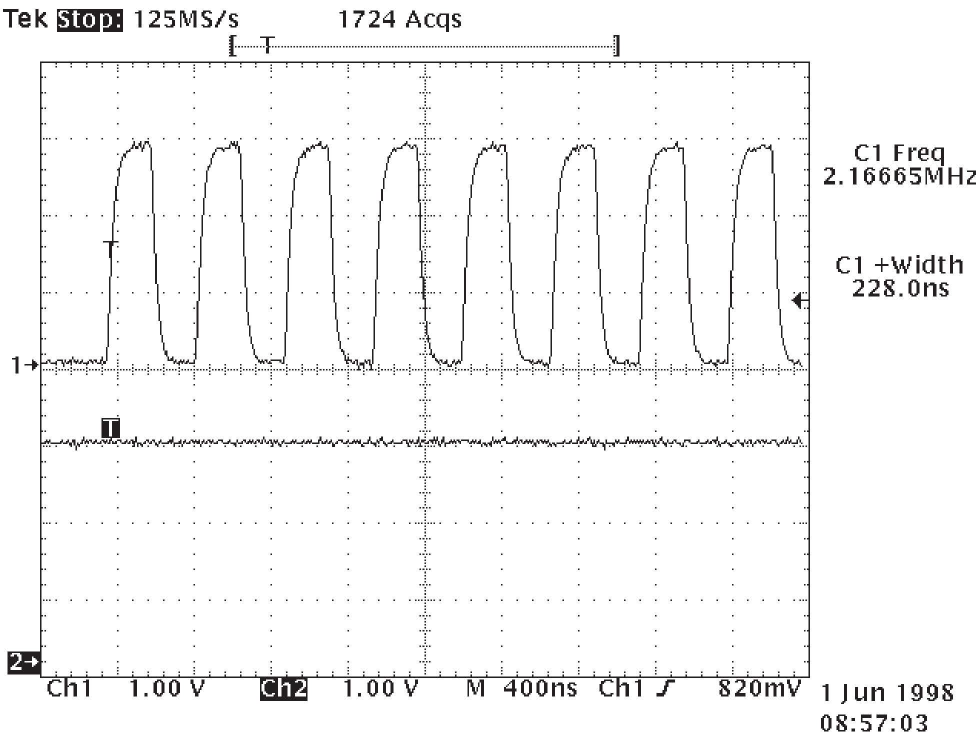


Figure 38. GENSCLK (J706) and LCDCSx (pin 5/H700), LCD inactive, serial bus used for communication between MAD and CCONT.

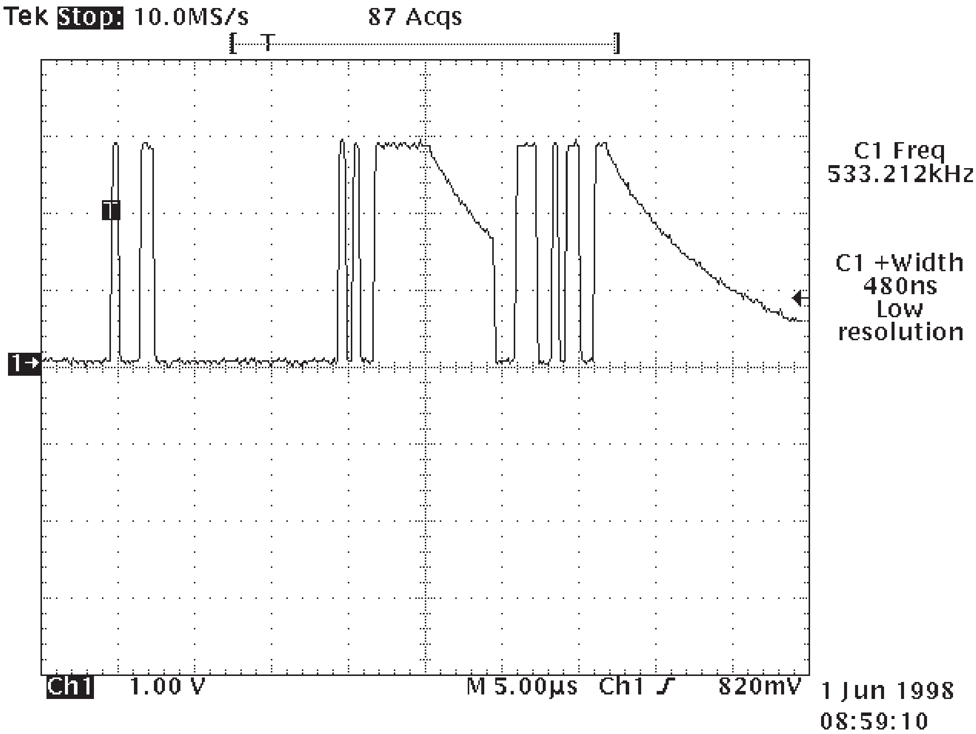


Figure 39. GENSDIO (J707)

PDA LCD Display Troubleshooting

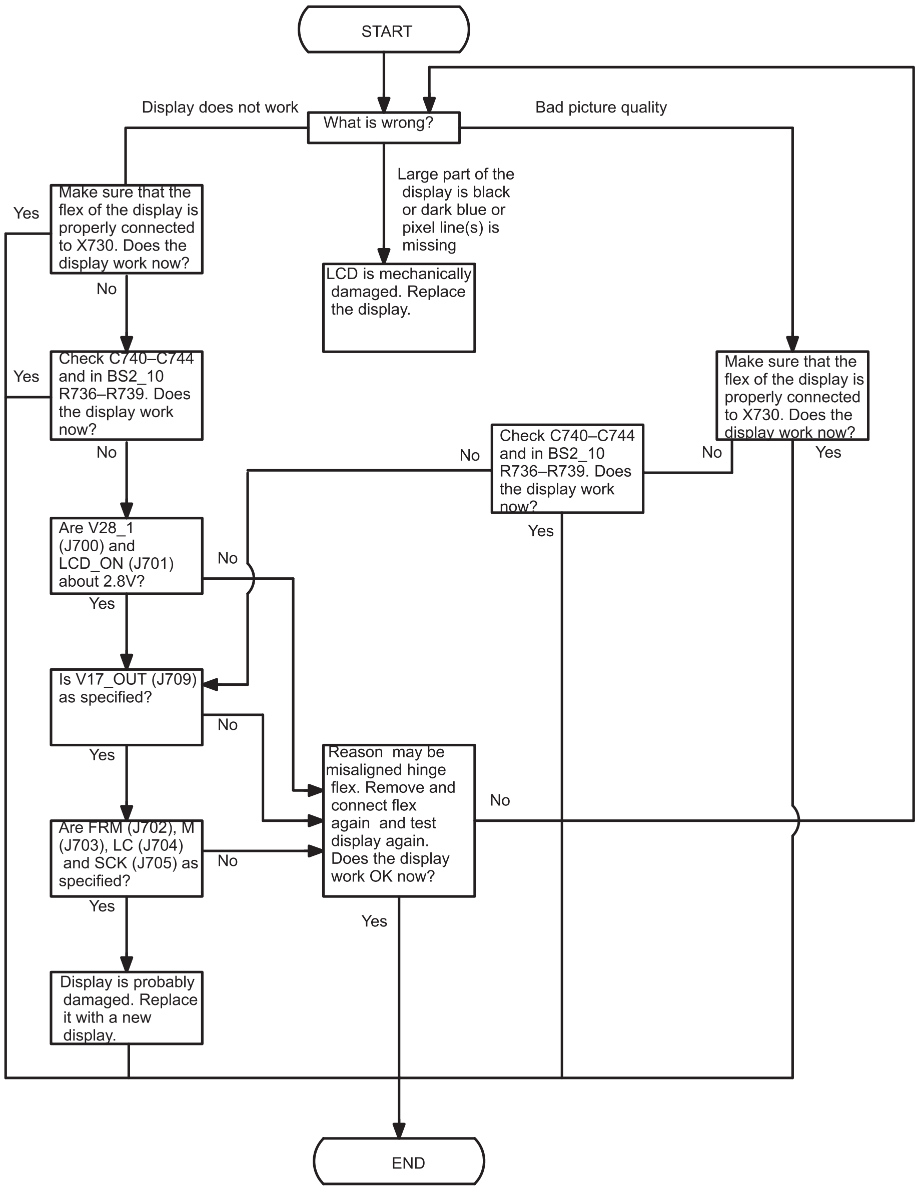


Figure 40. Flowchart for troubleshooting of the PDA LCD.

– Testing equipment: Multimeter and oscilloscope.

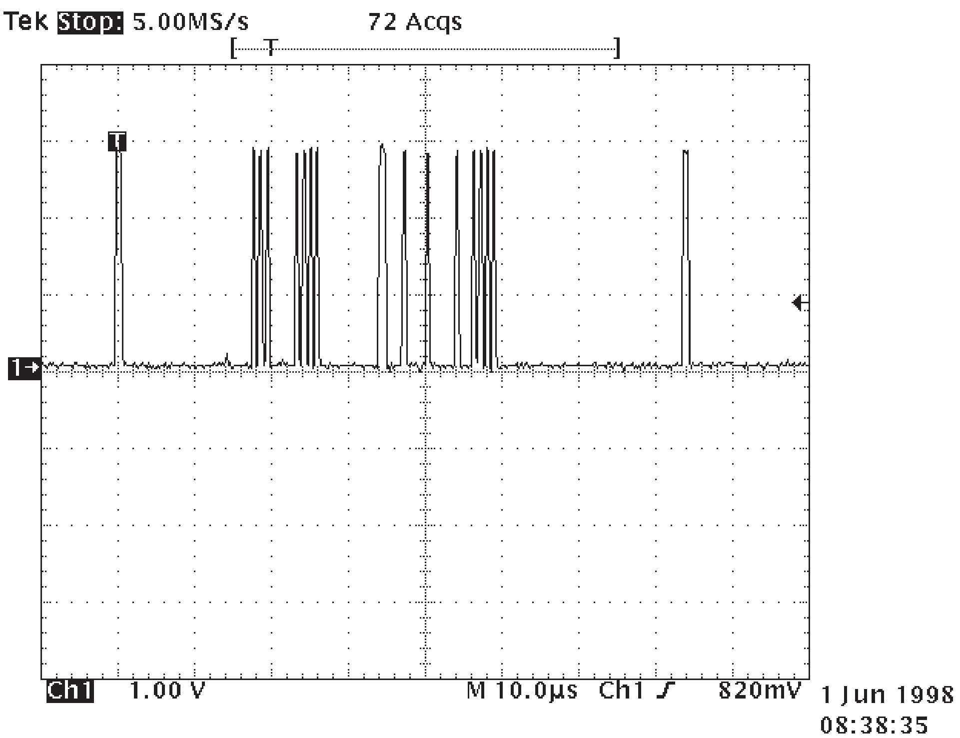


Figure 41. LCDD0 (J712)

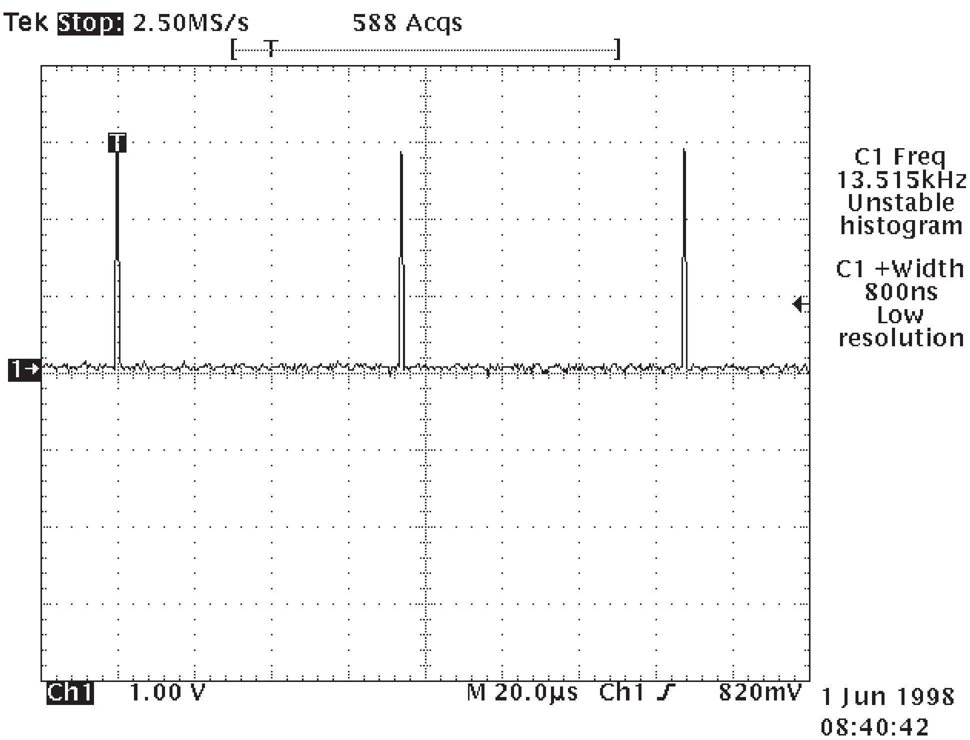


Figure 42. LC (J704)

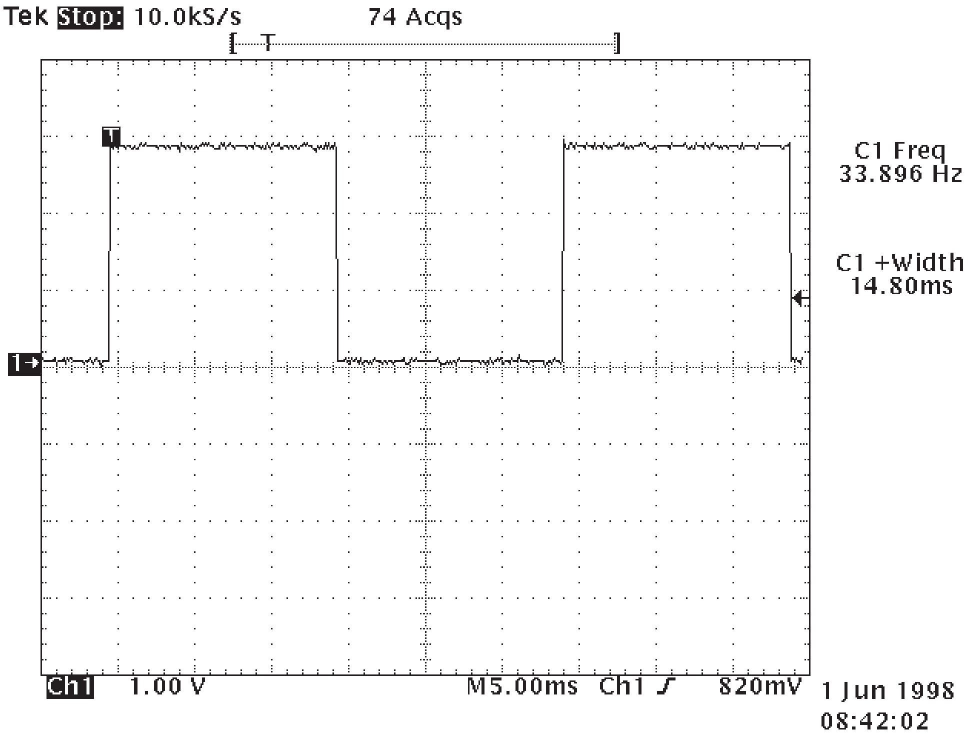


Figure 43. M (J703)

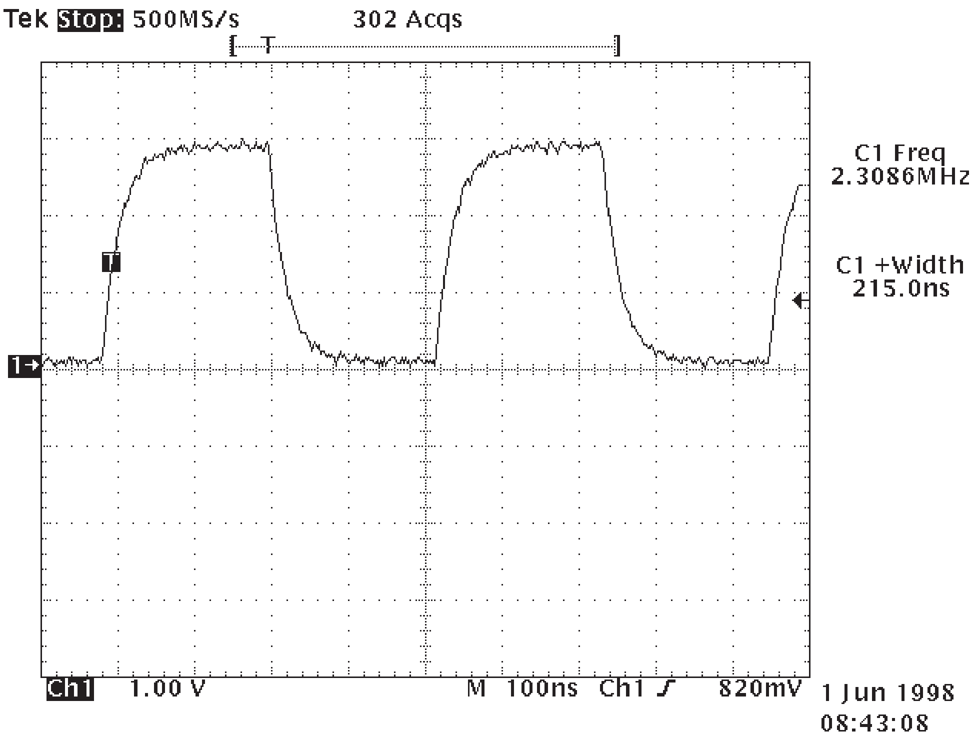


Figure 44. SCK (J705)

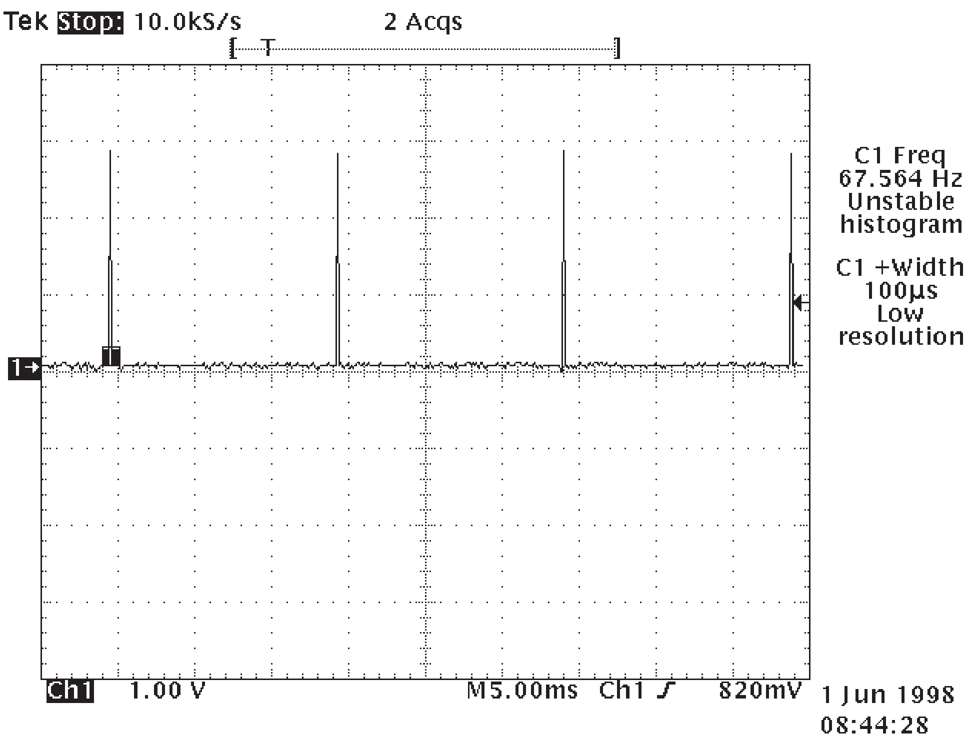


Figure 45. FRM (J702)

CMT Backlighting Circuit Troubleshooting

When troubleshooting the CMT backlighting circuit, remember that backlighting goes off after a certain period from the last key pressing.

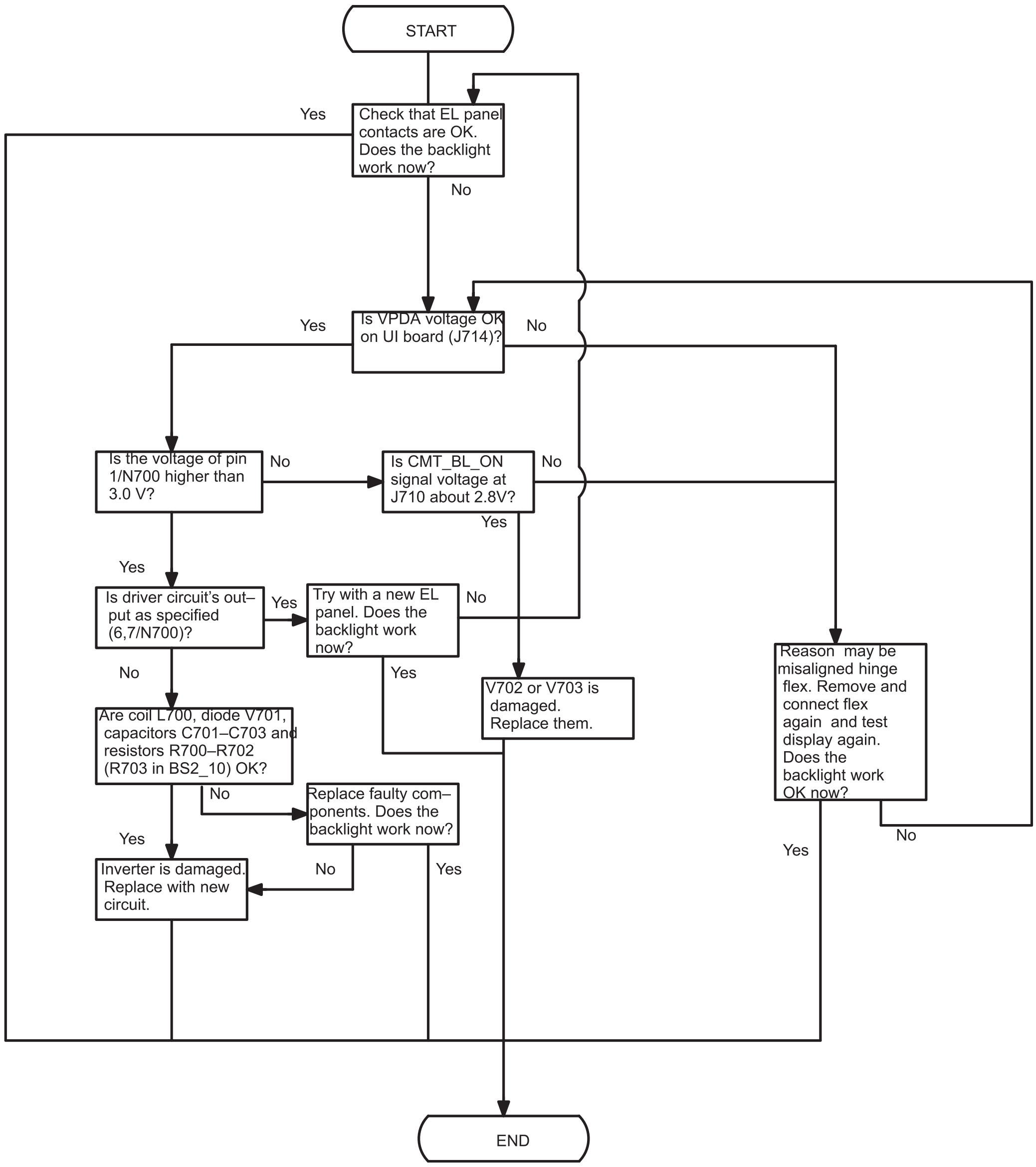


Figure 46. Flowchart for troubleshooting of the CMT backlighting circuit.

PDA LCD Backlighting Circuit Troubleshooting

For PDA backlighting troubleshooting you can use test mode and WinTesla SW to set the backlighting on all the time.

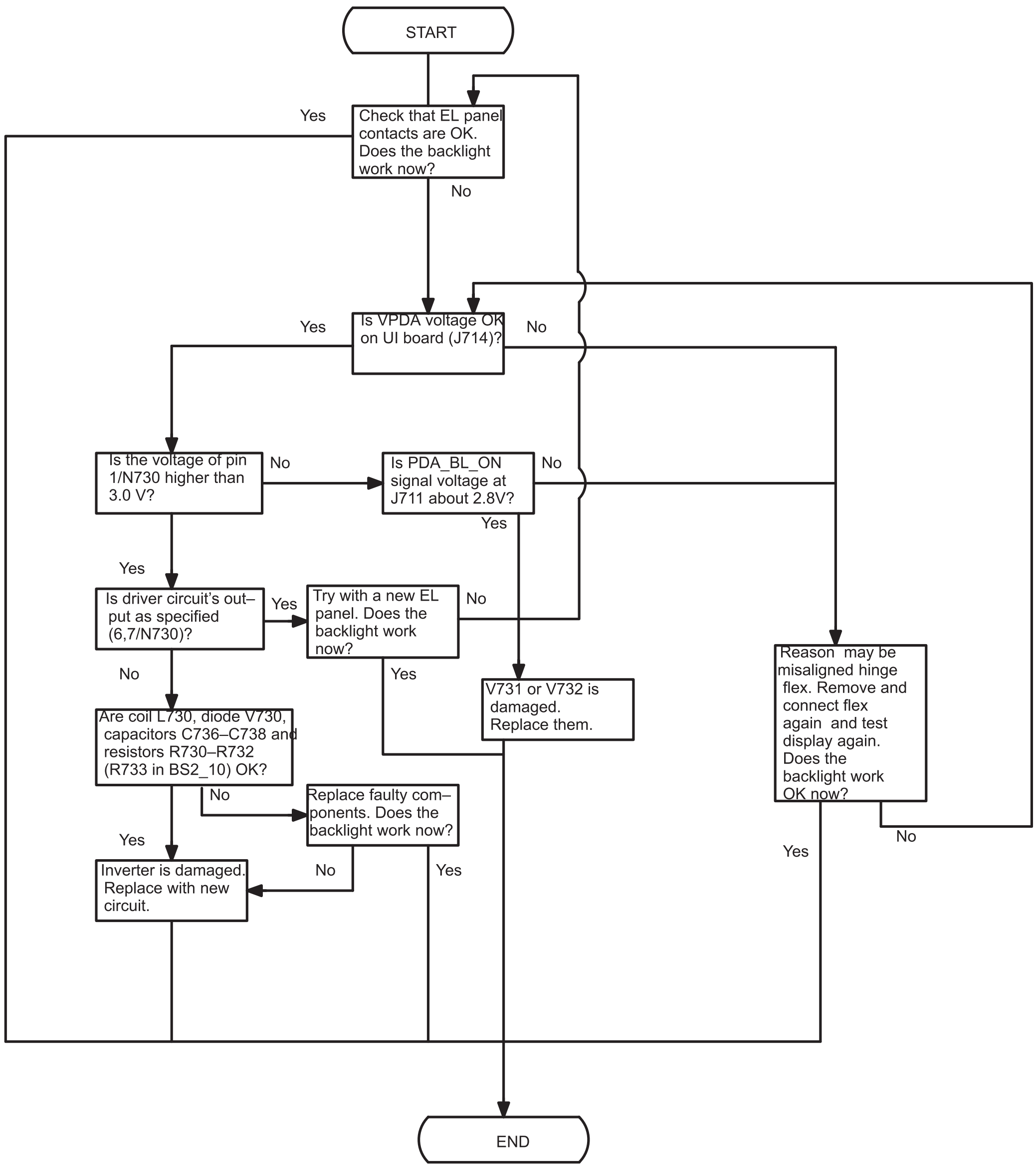


Figure 47. Flowchart for troubleshooting of the PDA backlighting circuit.

– Testing equipment: Multimeter and oscilloscope. Note that voltage rating of the oscilloscope and probe must be over 250 V peak–to–peak.

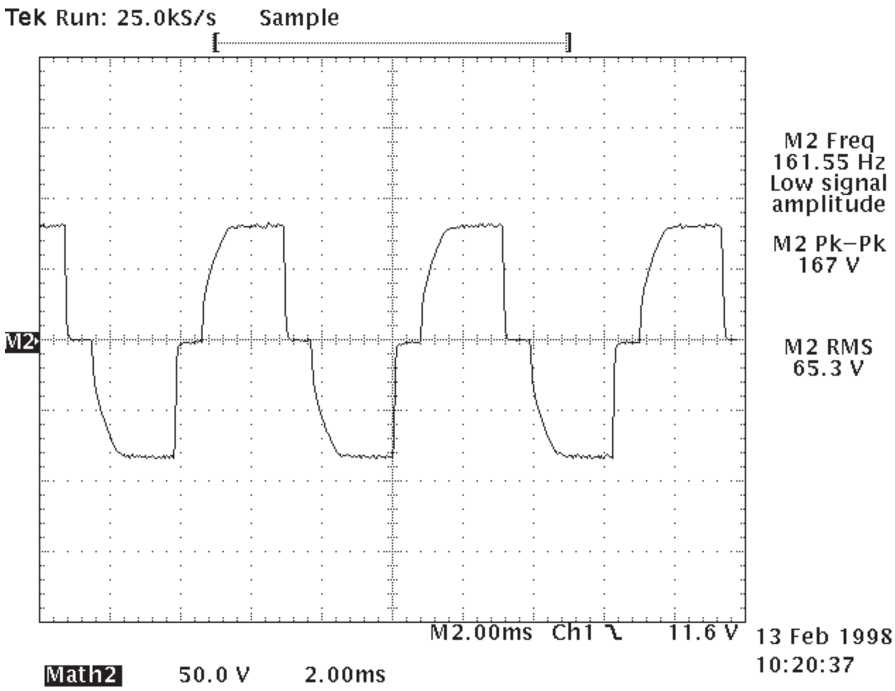


Figure 48. Example of a typical EL driver output waveform, measured between pins 6 and 7 of the driver.

Chapter 8

Service Tools

AMENDMENT RECORD SHEET

Amendment Number	Date	Inserted By	Comments
	02/99		Original

CONTENTS -Service Tools

Service Battery BBS-5

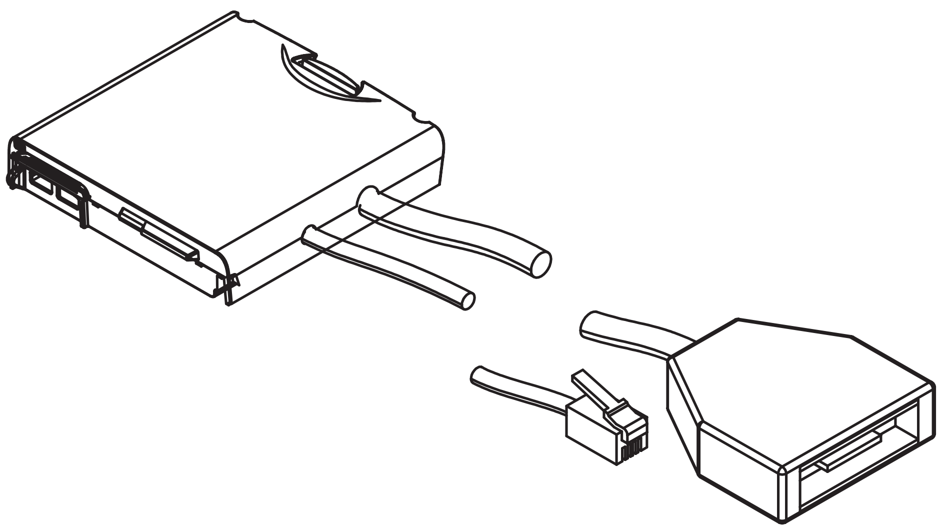
The service battery BBS-5 is used in place of the normal battery of the communicator during service to supply a controlled operating voltage from JBE-1, JBP-8 or FLA-7.

NOTE: DO NOT connect BBS-5 straight to a voltage source . The service battery is also required when flashing the phone.

Product Code

Service Battery BBS-5: 0770117

View of BBS-5



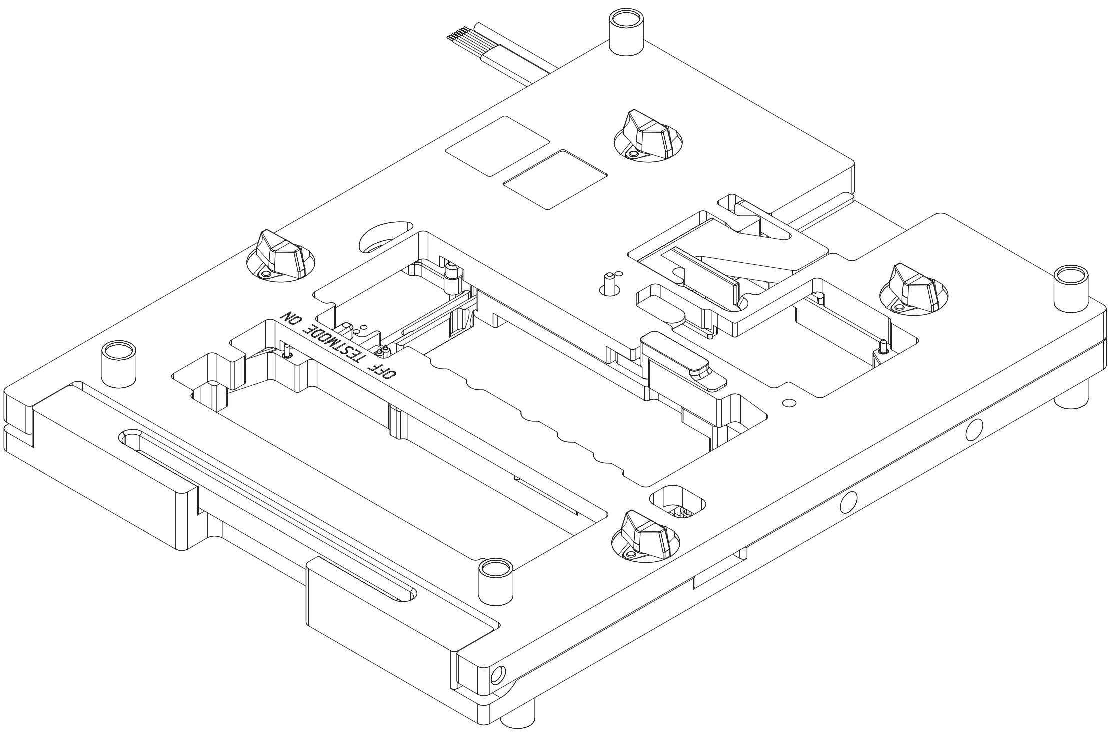
Module Jig MJS-4

The module jig MJS-4 is used for RAE-2 module testing and repairing. There are slots for each module in the jig. The jig includes connections for charger, power supply, external RF, audios and FBUS/MBUS. Slots for Memory card and SIM card are also included. This equipment is powered by a laboratory source.

Product Code

Module Jig MJS-4: 0770116

View of MJS-4



Note: The nominal supply voltage for MJS-4 is +4.0 V.
The supply voltage must not exceed +4.1 V.

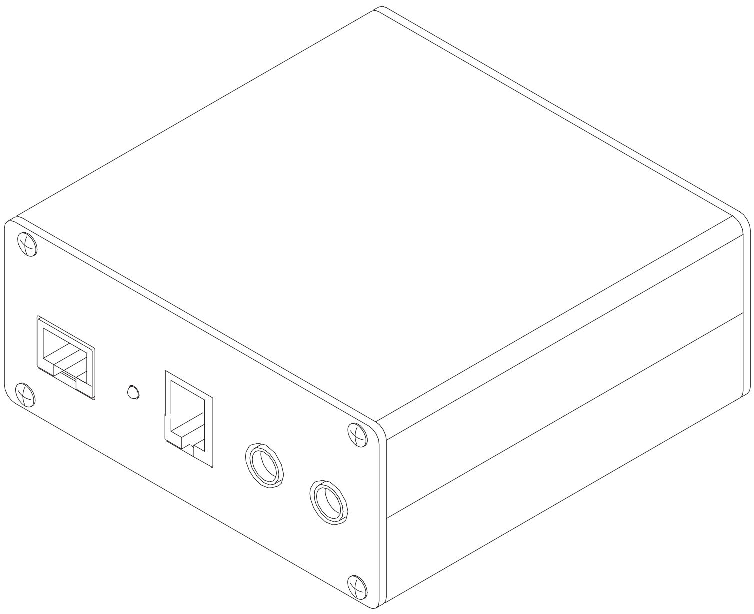
Flash Loading Adapter FLA-7

The flash loading adapter FLA-7 is used with the service battery BBS-5 and service cable SCH-8. Power is supplied to the FLA-7 from the ACL-3 charger. Power for the FPS-4 can be connected via the FLA-7 by SCF-7 DC power cable. The adapter is connected to the flash prommer FPS-4S by the AXS-5 cable and to the security box TDF-4 by the XCM-1 cable.

Product Code

Flash Loading Adapter FLA-7: 0770119

View of FLA-7



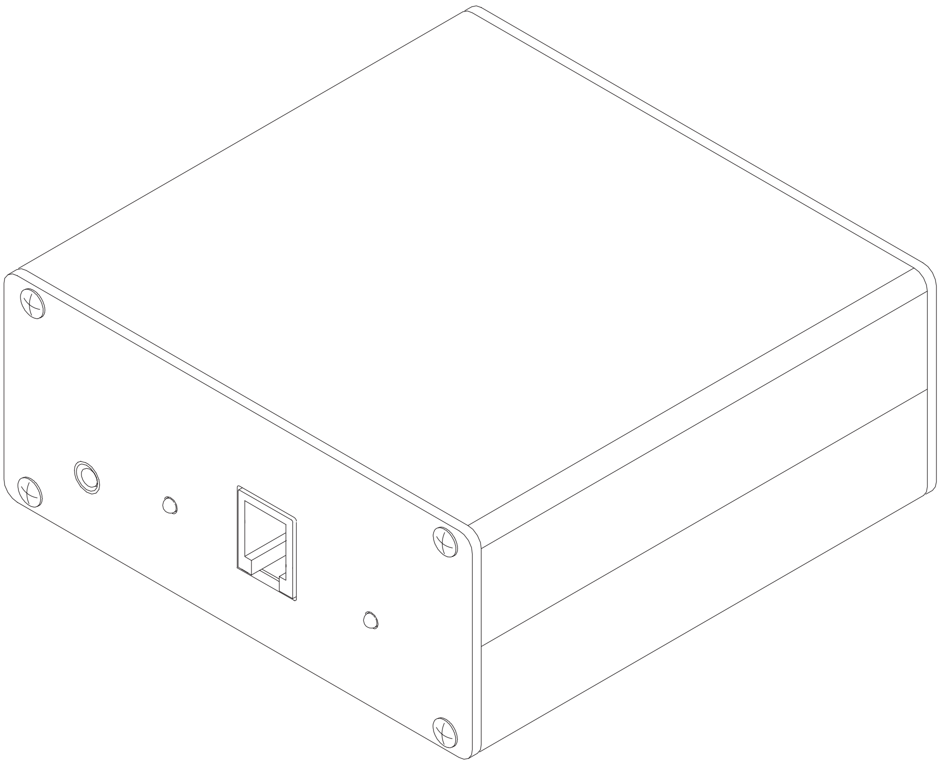
Calibration Unit JBE-1

The calibration unit JBE-1 is used for power management calibrations of a RAE-2 communicator. The calibration unit is also a voltage source for the service battery BBS-5. This equipment is powered by a laboratory source.

Product Code

Calibration Unit JBE-1:	0770118

View of JBE-1



Note: The nominal supply voltages for JBE-1 are

+7,0 V for normal service activities and

10,5 V for calibrations.

The supply voltage must not exceed +12,0 V

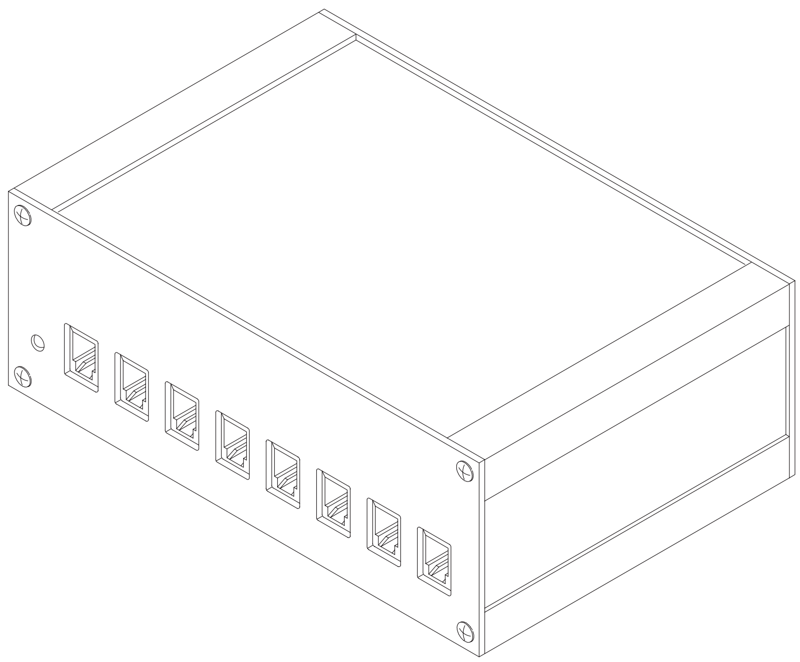
Power Junction Unit JBP-8

The power junction unit JBP-8 is used to provide power for eight BBS-5 service batteries at the same time. This is how eight PDA memories of RAE-2 phone can be updated at the same time. This equipment is powered by a laboratory source.

Product Code

Power Junction Unit JBP-8	0770141

View of JBP-8



Note: The nominal supply voltage for JBP-8 is +4,0 V.
The supply voltage must not exceed +4.1 V.

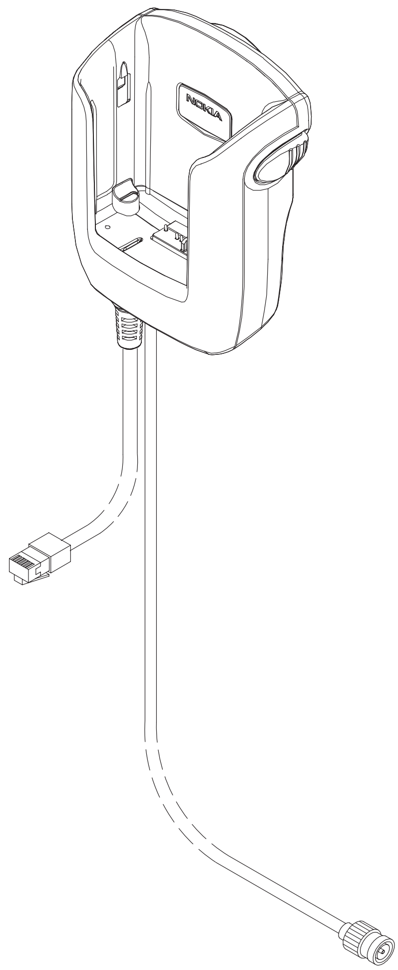
Service Car Kit HCR-2

The service car kit HCR-2 is modified from CRH-2 car kit of RAE-2 phone. HCR-2 is used as interface between RAE-2 phone and service software while doing RF tuning

Product Code

Service Car Kit HCR-2	0770146

View of HCR-2



Flash Prommer FPS-4S (Sales Pack)

The flash prommer FPS-4S is used to update the main software of the phone. Updating is done by first loading the new MCU software from the PC to the flash prommer, and then loading the new SW from the prommer to the phone. When updating more than one phone in succession, the MCU software only needs to be loaded to the prommer once.

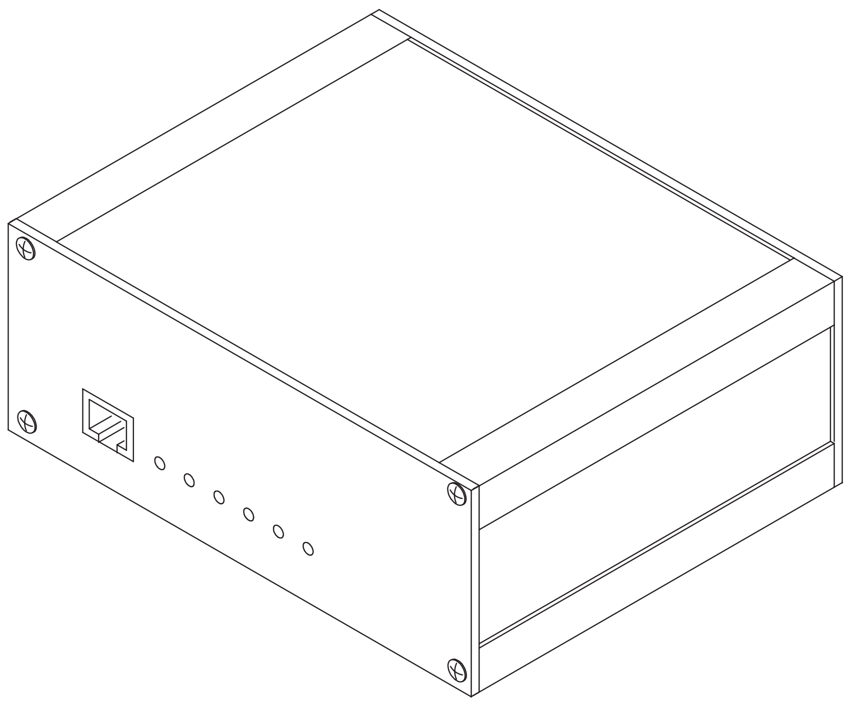
The sales pack includes:

- Charger ACL-3E	0680015
- Printer Cable	0730029
- D9 - D9 Cable AXS-4	0730090
- Installation software for FPS-4	8400041

Product Code

Flash Prommer FPS-4S: 0080178

View of FPS-4S



Security Box TDF-4

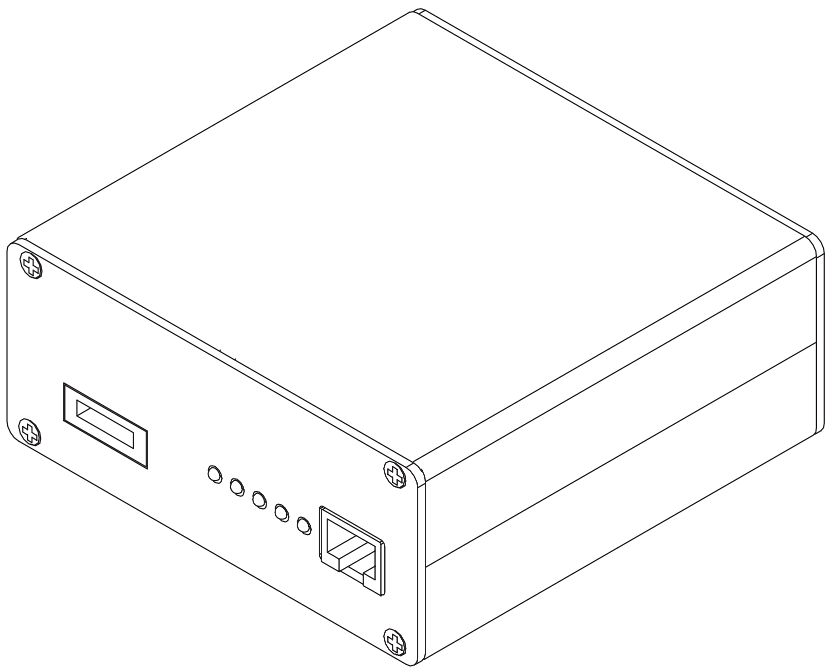
The security box TDF-4 is required for updating MCU software, and infra red testing.

Note2: The infra red module JLP-1 is not included in the TDF-4 sales package

Product Code

Security Box TDF-4: 0770106

View of TDF-4



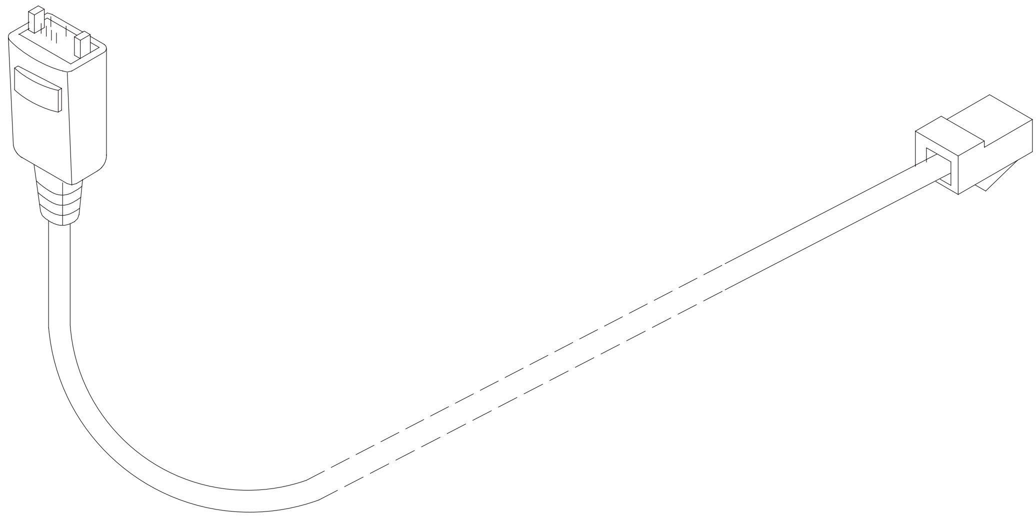
Service Cable SCH-8

The service cable SCH-8 is used between the phone and the modular T-adapter or between the phone and the flash loading adapter FLA-7.

Product Code

Service Cable SCH-8: 0730137

View of SCH-8



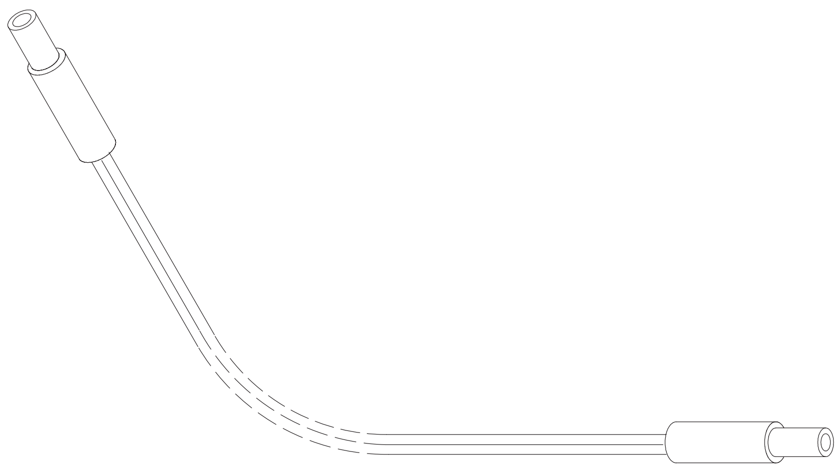
DC Power Cable SCF-7

The DC power cable SCF-7 is used for connecting power from ACL-3 charger via FLA-7 to FPS-4.

Product Code

DC Power Cable SCF-7: 0730141

View of SCF-7



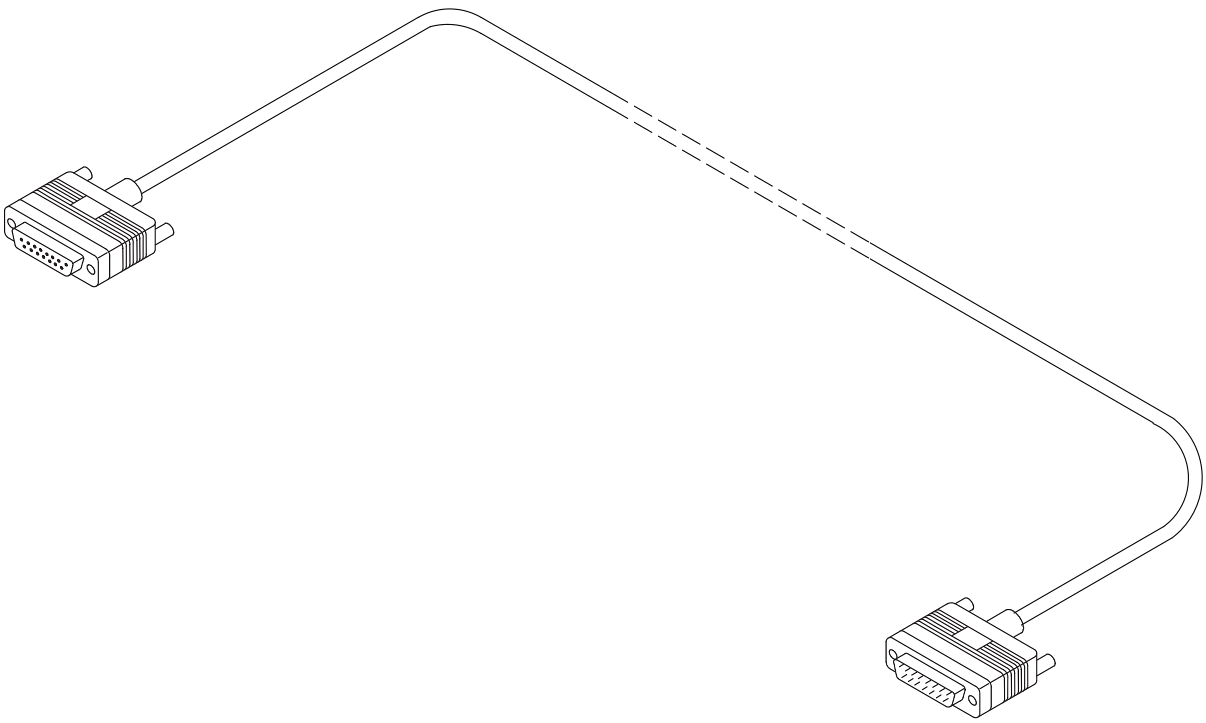
D15-D15 Cable AXS-5

The D15-D15 cable AXS-5 is used to connect two 15 pin D connectors. e.g. between FLA-7 and FPS-4S.

Product Code

D15-D15 Cable AXS-5: 0730091

View of AXS-5



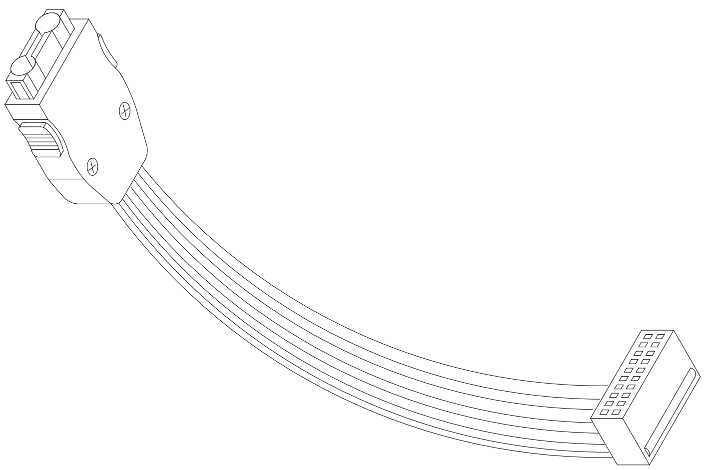
JTAG Cable DKS-6

The JTAG cable DKS-6 is used for connecting the JTAG tap pod to a service battery BBS-5.

Product Code

JTAG Cable DKS-6:	0730139

View of DKS-6



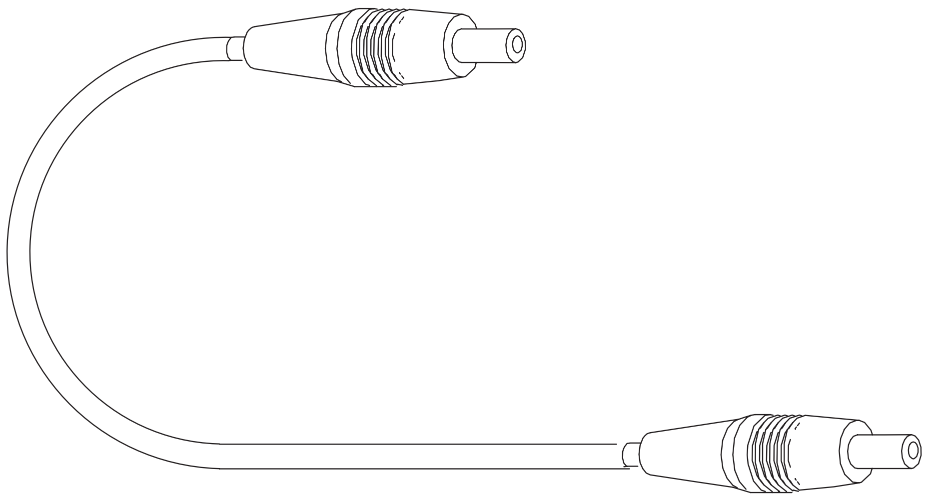
DC Cable SCB-3

The DC cable SCB-3 is used to connect the calibration unit JBE-1 to the charger connection Vin of the RAE-2 phone when doing the charger calibration service procedure.

Product Code

DC Cable SCB-3:	0730114

View of SCB-3



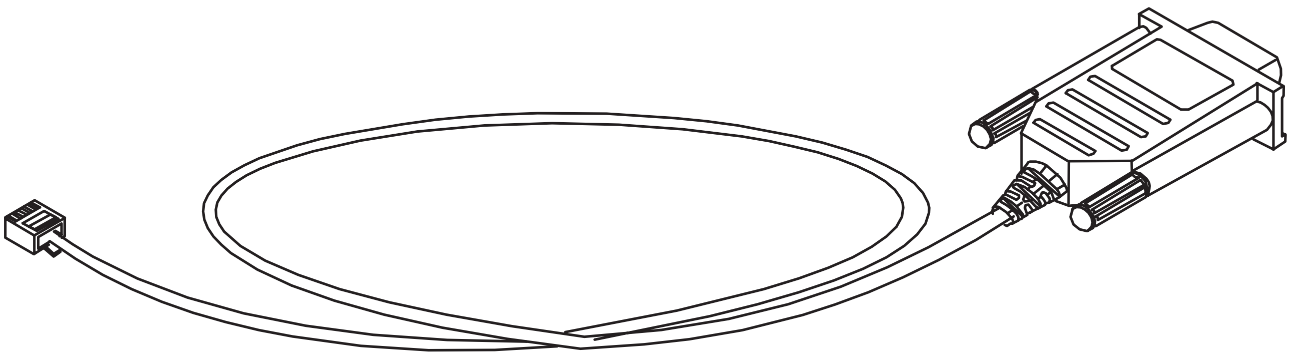
MBUS Cable DAU-9S

The MBUS cable DAU-9S has a modular connector, and is used with the service car kit HCR-2 and the module jig MJS-4 with a modular T-adapter.

Product Code

MBUS Cable DAU-9S:	0730108

View of DAU-9S



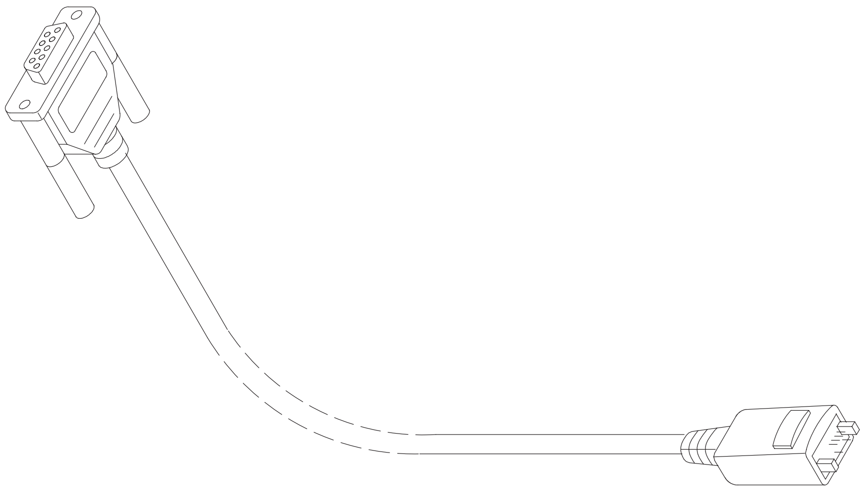
MBUS Cable DAU-9C

The MBUS cable DAU-9C has a RAE-2 phone system connector, and is used between the phone and external devices (laptops, PCs).

Product Code

MBUS Cable DAU-9C: 0730138

View of DAU-9C



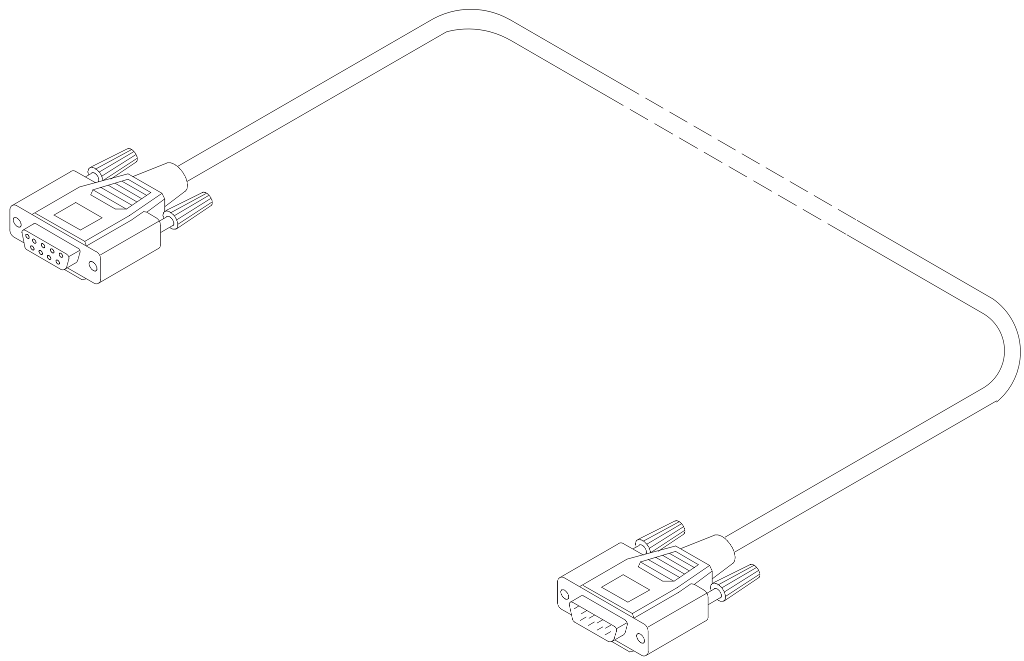
D9-D9 Cable AXS-4

The D9-D9 cable AXS-4 is used to connect two 9 pin D connectors. e.g. between PC and TDF-4 security box.

Product Code

D9 - D9 Cable AXS-4: 0770036

View of AXS-4



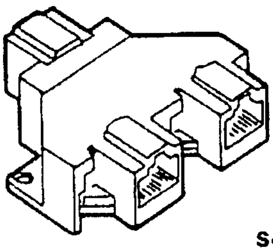
Modular T-adapter

The modular T-adapter is a suitable branching unit to provide the needed parallel modular connections.

Product Code

Modular T-adapter: 4626134

View of Modular T-adapter



S4626134

SW Security Device PKD-1

SW security device is a piece of hardware enabling the use of the service software when connected to the parallel (LPT) port of the PC. Without the dongle present it is not possible to use the service software. Printer or any such device can be connected to the PC through the dongle if needed.

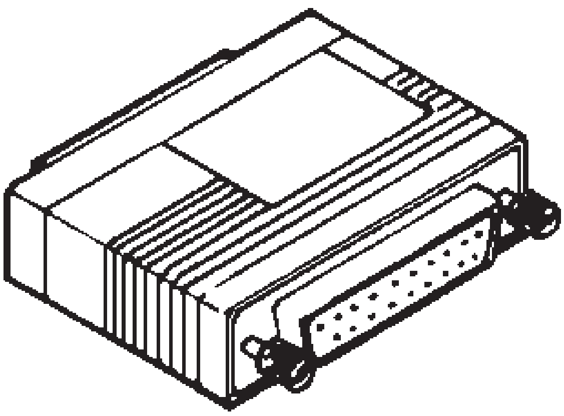
Caution: Make sure that you have switched off the PC and the printer before making connections!

Caution: Do not connected the PKD-1 to the serial port. You may damage your PKD-1!

Product Code

SW Security Device PKD-1: 0750018

View of SW Security Device



G0750018

Protection Key PKD-4F

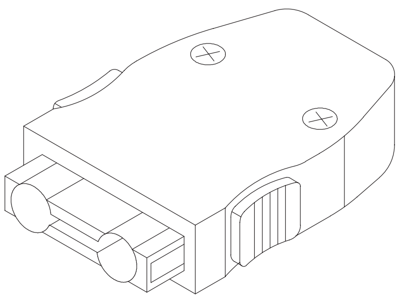
This protection key is needed for the delivery of the PDA flash voltage. Without it the PDA flash circuits do not receive a programming voltage and the update fails. The PKD-4F is connected to the JTAG connector of the BBS-5 service battery.

Caution: PKD-4F IS ALLOWED TO BE CONNECTED ONLY WHILE UPDATING PDA SOFTWARE!

Product Code

Protection Key PKD-4F:	0750124

View of PKD-4F



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Chapter 09

Mechanical Parts and Disassembly

AMENDMENT RECORD SHEET

Amendment Number	Date	Inserted By	Comments
	02/99		Original

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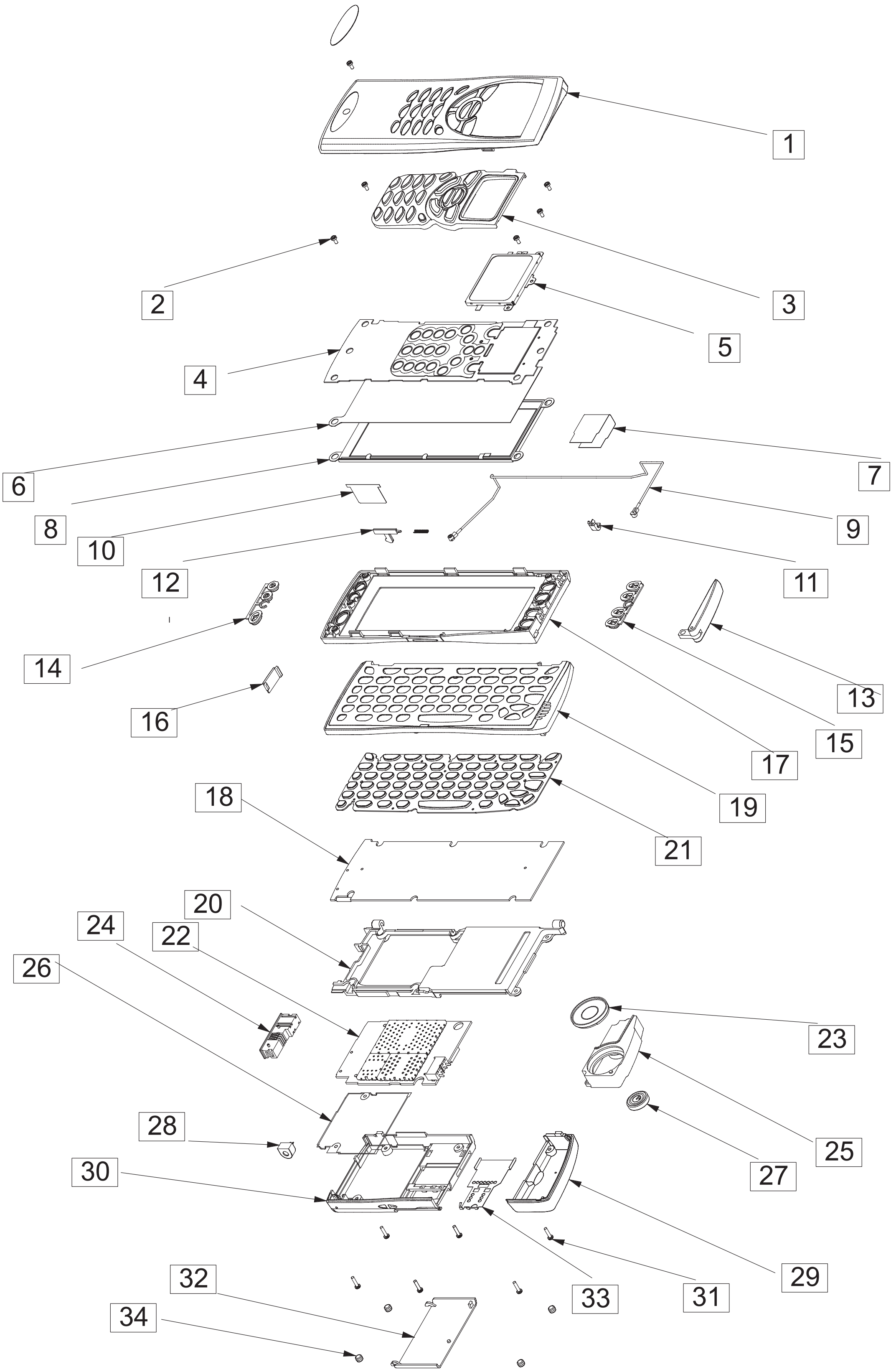
RAE–2 Exploded diagram below



List of Mechanic Parts

Item	Code	Description	Specifications / Ratings
1	9456203	Front cover with lens	
2	6190033	Screw M1,6x5 6 pcs	6x M1,6X5
3	9790326	Phone keypad	
4	0201097	Phone UI PCB	
5	4850063	Phone LCD	
6	4850801	PDA Display ELbacklight	
7	9855044	Hingle flex	
8	4850049	PDA LCD	
9	9780234	Coaxial cable	
10	9460251	Flex cover	
11	9460248	Hinge end	
12A	9460249	Latch	
12B	6402165	Spring	
13	0660183	Antenna	
14	9790330	Function keypad left	
15	9790320	Function keypad right	
16	9451258	IR window	
17	9456209	Screen frame	
18	0201096	PDA PCB	
19	9367026	Keypad frame	
20	9547007	Chassis	
21	9790313	QWERTY keypad	Note: English language keypad
22	**	CMT PCB	Not available as spare part
23	5140119	HF speaker	
24	5469091	System connector	
25	9467029	Audio holder	
26	9510421	Metal gasket	
27	5140067	Earpiece	
28	5140133	Microphone	
29	9451261	Audio cover	
30	9456156	Back cover	
31	6190013	Screws	6 x M1,6x7
32	9451257	Card cover	
33	9510425	Card shield	
34	9470052	Plug	4 pcs

LCD / UI Module Disassembly

1. Remove battery.
2. Remove cover label (A) and screw (B).
3. Gently lift off front cover starting from both sides in the bottom end of the phone or by pulling the top end of front cover.
4. Remove phone keymat.
5. Remove 5 screws (C) and 2 washers (D).
6. Disconnect flex connectors by releasing connector clips. Connectors will be opened by lifting the clip up.
7. Unplug the coaxial cable.
8. Unclip UI PCB from PDA LCD by lifting up 3 metal clips (E).
9. Remove phone LCD. Do not try to remove phone LCD without opening the metal clip. Elastomer might be damaged.
10. Remove UI PCB, display EL backlight, PDA LCD and function keypads.
    Note 1: Latch and spring, spring flies away quite easily.
    Note 2: PDA LCD is connected to screen frame with tapes. Always use new tapes when re–assembling.
11. Remove antenna. Use a knife or a small screwdriver to lift plastic clip which blocks the antenna.
12. Re–assemble in reverse order and observe the following points:
    –Check that coaxial cable goes behind guide pin and does not get trapped under front cover.
    See further details in figure1

–Note that torque of the screws must be 10 Ncm.

–Assembly flex cover so that mat side is inside the phone.

The correct way to assembly coaxial cable is described in the next page.

Figure1. Correct way to assemble the coaxial cable in the lid part.

System Module Disassembly

1. Remove battery.
2. Remove four plugs (34) and six screws (31).
3. Remove audio cover, audio holder and back cover, be careful not to touch sensitive parts of earpiece.
4. Unplug the coaxial cable.
5. Remove CMT PCB, system connector and IR window. CMT PCB might be very tightly connected, use necessary force to remove it.
6. Open chassis. Disconnect flex connector by releasing connector clip. Connector will be opened by lifting the clip up.
7. Remove PDA PCB.
8. Remove chassis; at first from the lower hinge, easiest position is to put the hinge almost 180° angle, and remove the chassis then. Be careful not to damage coaxial cable.
9. Remove QWERTY keypad and keypad frame. Do not touch carbon connections surfaces on QWERTY keypad.
10. Re–assemble in reverse order and observe following points:
    –Re–assemble chassis first to the upper hinge and check coaxial cable.
    –Re–assemble PDA PCB and connect flex connector when chassis is open.
    –Coaxial cable must go under the hinge flex and between two bulbs on keypad frame. See picture. (figure 4)
    –Check that coaxial cable does not get trapped.
    –Check that coaxial cable goes to CMT PCB between two bulbs. See pictures.(figure 2 and figure 3)
    –Notice that torque of screws must be 15 Ncm.
11. Figures 2 to 4 : The correct way to assemble coaxial cable.

Figure 2. Correct way to assemble coaxial cable between the guiding pins.

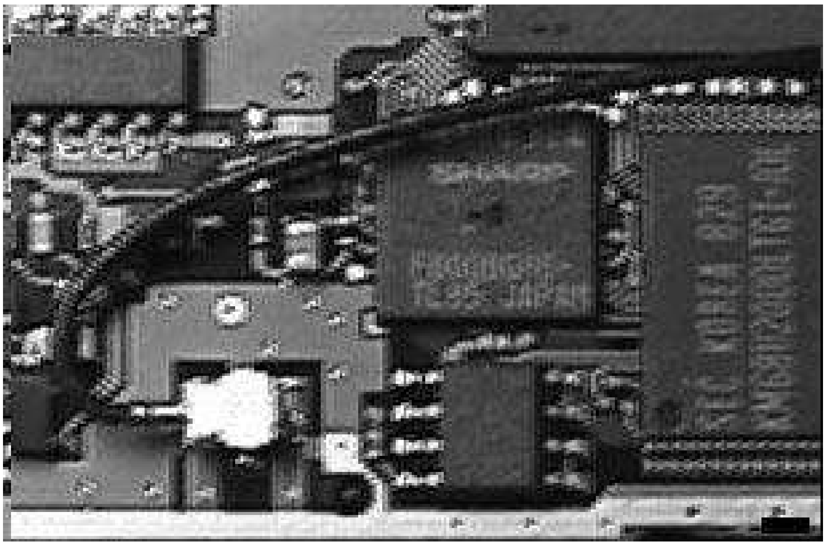


Figure 3.

Figure 3. Correct way to assemble coaxial cable on CMT PCB.

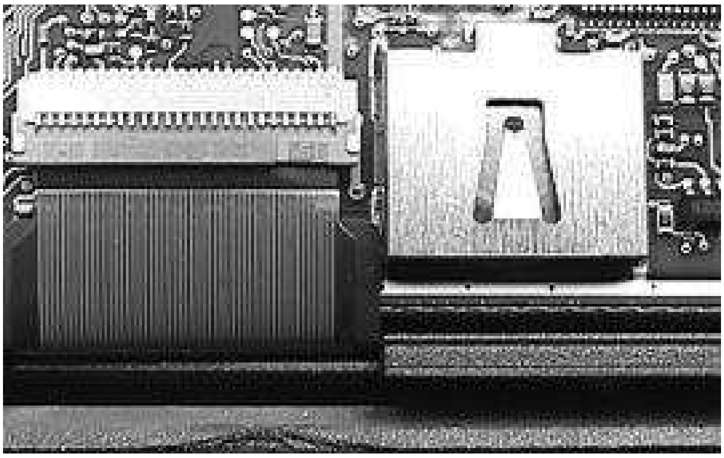


Figure 4. Correct way to assemble coaxial cable under hinge flex cover.

Chapter 10

Schematic Diagrams of RAE–2 PDA Phone

AMENDMENT RECORD SHEET

Amendment Number	Date	Inserted By	Comments
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Schematic Diagrams

LIST OF CONTENTS / SCHEMATIC DIAGRAMS

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Chapter 11

Parts Lists

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CONTENTS – User Interface

GSM Module Parts List

0201095 BS8 GSM CMT MODULE EDMS Issue: 6.2

Item	Code	Description	Value/Type	
R103	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R104	1430796	Chip resistor	47 k	5 % 0.063 W 0402
R120	1430810	Chip resistor	180 k	5 % 0.063 W 0402
R121	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R122	1620019	Res network	0w06 2x10k j	0404
R123	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R124	1430718	Chip resistor	47	5 % 0.063 W 0402
R125	1430718	Chip resistor	47	5 % 0.063 W 0402
R128	1430718	Chip resistor	47	5 % 0.063 W 0402
R131	1422881	Chip resistor	0.22	5 % 1 W 1218
R136	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R140	1620025	Res network 0w06 2x100k j	0404	0404
R141	1430796	Chip resistor	47 k	5 % 0.063 W 0402
R142	1430718	Chip resistor	47	5 % 0.063 W 0402
R151	1430690	Chip jumper		0402
R152	1430690	Chip jumper		0402
R170	1825005	Chip varistor vwm14v vc30v	0805	0805
R171	1430071	Chip resistor	22 k	5 % 0.063 W 0603
R172	1825003	Chip varistor vwm5.5v vc15.5	0805	0805
R173	1430726	Chip resistor	100	5 % 0.063 W 0402
R190	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R191	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R195	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R201	1430812	Chip resistor	220 k	5 % 0.063 W 0402
R202	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R203	1430812	Chip resistor	220 k	5 % 0.063 W 0402
R211	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R213	1430744	Chip resistor	470	5 % 0.063 W 0402
R215	1620029	Res network 0w06 2x4k7 j	0404	0404
R216	1620023	Res network 0w06 2x47k j	0404	0404
R240	1620017	Res network 0w06 2x100r j	0404	0404
R251	1620025	Res network 0w06 2x100k j	0404	0404
R252	1430740	Chip resistor	330	5 % 0.063 W 0402
R254	1620027	Res network 0w06 2x47r j	0404	0404
R256	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R257	1430796	Chip resistor	47 k	5 % 0.063 W 0402
R259	1430796	Chip resistor	47 k	5 % 0.063 W 0402
R260	1430788	Chip resistor	22 k	5 % 0.063 W 0402
R261	1430788	Chip resistor	22 k	5 % 0.063 W 0402
R263	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R271	1430796	Chip resistor	47 k	5 % 0.063 W 0402
R272	1620031	Res network 0w06 2x1k0 j	0404	0404

R280	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R500	1430740	Chip resistor	330	5 % 0.063 W 0402
R501	1430700	Chip resistor	10	5 % 0.063 W 0402
R502	1430700	Chip resistor	10	5 % 0.063 W 0402
R503	1620029	Res network 0w06 2x4k7 j	0404	0404
R504	1430144	Chip jumper		0603
R505	1430744	Chip resistor	470	5 % 0.063 W 0402
R506	1430144	Chip jumper		0603
R507	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R508	1430764	Chip resistor	3.3 k	5 % 0.063 W 0402
R509	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R510	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R511	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R512	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R513	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R514	1430714	Chip resistor	33	5 % 0.063 W 0402
R515	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R516	1430776	Chip resistor	8.2 k	5 % 0.063 W 0402
R517	1430740	Chip resistor	330	5 % 0.063 W 0402
R518	1430748	Chip resistor	680	5 % 0.063 W 0402
R519	1430776	Chip resistor	8.2 k	5 % 0.063 W 0402
R520	1430744	Chip resistor	470	5 % 0.063 W 0402
R521	1430714	Chip resistor	33	5 % 0.063 W 0402
R522	1430730	Chip resistor	150	5 % 0.063 W 0402
R523	1430700	Chip resistor	10	5 % 0.063 W 0402
R524	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R525	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R526	1430734	Chip resistor	220	5 % 0.063 W 0402
R527	1430784	Chip resistor	15 k	5 % 0.063 W 0402
R528	1430780	Chip resistor	12 k	5 % 0.063 W 0402
R529	1430730	Chip resistor	150	5 % 0.063 W 0402
R530	1430710	Chip resistor	22	5 % 0.063 W 0402
R531	1430808	Chip resistor	150 k	5 % 0.063 W 0402
R532	1430780	Chip resistor	12 k	5 % 0.063 W 0402
R533	1430700	Chip resistor	10	5 % 0.063 W 0402
R534	1430780	Chip resistor	12 k	5 % 0.063 W 0402
R535	1430710	Chip resistor	22	5 % 0.063 W 0402
R536	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R538	1430808	Chip resistor	150 k	5 % 0.063 W 0402
R539	1430780	Chip resistor	12 k	5 % 0.063 W 0402
R540	1430796	Chip resistor	47 k	5 % 0.063 W 0402
R542	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R543	1430710	Chip resistor	22	5 % 0.063 W 0402
R544	1430832	Chip resistor	2.7 k	5 % 0.063 W 0402
R545	1430710	Chip resistor	22	5 % 0.063 W 0402
R546	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R547	1430788	Chip resistor	22 k	5 % 0.063 W 0402

R548	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R549	1430780	Chip resistor	12 k	5 % 0.063 W 0402
R550	1430774	Chip resistor	6.8 k	5 % 0.063 W 0402
R551	1430812	Chip resistor	220 k	5 % 0.063 W 0402
R552	1430776	Chip resistor	8.2 k	5 % 0.063 W 0402
R553	1430740	Chip resistor	330	5 % 0.063 W 0402
R554	1430766	Chip resistor	3.9 k	5 % 0.063 W 0402
R555	1430740	Chip resistor	330	5 % 0.063 W 0402
R556	1430752	Chip resistor	820	5 % 0.063 W 0402
R557	1430726	Chip resistor	100	5 % 0.063 W 0402
R558	1430740	Chip resistor	330	5 % 0.063 W 0402
R559	1430726	Chip resistor	100	5 % 0.063 W 0402
R560	1430690	Chip jumper		0402
R570	1430700	Chip resistor	10	5 % 0.063 W 0402
R622	1430718	Chip resistor	47	5 % 0.063 W 0402
R677	1430726	Chip resistor	100	5 % 0.063 W 0402
R690	1820031	NTC resistor	330	10 % 0.12 W 0805
R691	1430744	Chip resistor	470	5 % 0.063 W 0402
C104	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C105	2610003	Tantalum cap.	10 u	20 % 10 V
3.2x1.6x1.6				
C106	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C108	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C120	2320592	Ceramic cap.	2.2 n	5 % 50 V 0402
C121	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C127	2310784	Ceramic cap.	100 n	10 % 25 V 0805
C128	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C129	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C130	2610003	Tantalum cap.	10 u	20 % 10 V
3.2x1.6x1.6				
C131	2610005	Tantalum cap.	10 u	20 % 16 V
3.5x2.8x1.9				
C132	2312403	Ceramic cap.	2.2 u	10 % 10 V 1206
C133	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C134	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C135	2610003	Tantalum cap.	10 u	20 % 10 V
3.2x1.6x1.6				
C136	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C137	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C138	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C139	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C140	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C160	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C161	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C170	2604127	Tantalum cap.	1.0 u	20 % 35 V
3.5x2.8x1.9				
C171	2320546	Ceramic cap.	27 p	5 % 50 V 0402

C172	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C173	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C174	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C175	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C176	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C177	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C178	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C179	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C180	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C181	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C182	2320778	Ceramic cap.	10 n	10 % 16 V 0402
C183	2320805	Ceramic cap.	100 n	10 % 10 V 0402
C201	2320778	Ceramic cap.	10 n	10 % 16 V 0402
C202	2320778	Ceramic cap.	10 n	10 % 16 V 0402
C203	2320778	Ceramic cap.	10 n	10 % 16 V 0402
C204	2320778	Ceramic cap.	10 n	10 % 16 V 0402
C205	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C206	2320778	Ceramic cap.	10 n	10 % 16 V 0402
C207	2320778	Ceramic cap.	10 n	10 % 16 V 0402
C208	2320778	Ceramic cap.	10 n	10 % 16 V 0402
C209	2320778	Ceramic cap.	10 n	10 % 16 V 0402
C211	2320778	Ceramic cap.	10 n	10 % 16 V 0402
C212	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C213	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C221	2320778	Ceramic cap.	10 n	10 % 16 V 0402
C231	2320778	Ceramic cap.	10 n	10 % 16 V 0402
C240	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C241	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C250	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C251	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C252	2312296	Ceramic cap.		Y5 V 1210
C253	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C254	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C255	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C256	2312296	Ceramic cap.		Y5 V 1210
C257	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C258	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C259	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C260	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C261	2310784	Ceramic cap.	100 n	10 % 25 V 0805
C262	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C263	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C264	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C270	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C271	2610003	Tantalum cap.	10 u	20 % 10 V
3.2x1.6x1.6				
C272	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805

C273	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C274	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C275	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C280	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C281	2320778	Ceramic cap.	10 n	10 % 16 V 0402
C282	2320779	Ceramic cap.	100 n	10 % 16 V 0603
C500	2320518	Ceramic cap.	1.8 p	0.25 % 50 V 0402
C501	2320778	Ceramic cap.	10 n	10 % 16 V 0402
C502	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C503	2320534	Ceramic cap.	8.2 p	0.25 % 50 V 0402
C504	2320530	Ceramic cap.	5.6 p	0.25 % 50 V 0402
C505	2320550	Ceramic cap.	39 p	5 % 50 V 0402
C506	2320514	Ceramic cap.	1.2 p	0.25 % 50 V 0402
C507	2320532	Ceramic cap.	6.8 p	0.25 % 50 V 0402
C508	2320534	Ceramic cap.	8.2 p	0.25 % 50 V 0402
C509	2320530	Ceramic cap.	5.6 p	0.25 % 50 V 0402
C510	2320508	Ceramic cap.	1.0 p	0.25 % 50 V 0402
C511	2320550	Ceramic cap.	39 p	5 % 50 V 0402
C512	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C513	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C514	2320536	Ceramic cap.	10 p	5 % 50 V 0402
C515	2320540	Ceramic cap.	15 p	5 % 50 V 0402
C516	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C517	2320536	Ceramic cap.	10 p	5 % 50 V 0402
C518	2320536	Ceramic cap.	10 p	5 % 50 V 0402
C519	2320536	Ceramic cap.	10 p	5 % 50 V 0402
C520	2320536	Ceramic cap.	10 p	5 % 50 V 0402
C521	2320548	Ceramic cap.	33 p	5 % 50 V 0402
C522	2320530	Ceramic cap.	5.6 p	0.25 % 50 V 0402
C523	2320530	Ceramic cap.	5.6 p	0.25 % 50 V 0402
C524	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C525	2320536	Ceramic cap.	10 p	5 % 50 V 0402
C526	2320522	Ceramic cap.	2.7 p	0.25 % 50 V 0402
C527	2320508	Ceramic cap.	1.0 p	0.25 % 50 V 0402
C528	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C529	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C530	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C531	2320592	Ceramic cap.	2.2 n	5 % 50 V 0402
C532	2320526	Ceramic cap.	3.9 p	0.25 % 50 V 0402
C533	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C534	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C535	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C536	2320779	Ceramic cap.	100 n	10 % 16 V 0603
C537	2310784	Ceramic cap.	100 n	10 % 25 V 0805
C538	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C539	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C540	2320560	Ceramic cap.	100 p	5 % 50 V 0402

C541	2320536	Ceramic cap.	10 p	5 % 50 V 0402
C542	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C543	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C544	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C545	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C546	2320552	Ceramic cap.	47 p	5 % 50 V 0402
C547	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C548	2310784	Ceramic cap.	100 n	10 % 25 V 0805
C549	2320552	Ceramic cap.	47 p	5 % 50 V 0402
C550	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C551	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C552	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C553	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C554	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C556	2320554	Ceramic cap.	56 p	5 % 50 V 0402
C558	2310181	Ceramic cap.	1.5 n	5 % 50 V 1206
C559	2310784	Ceramic cap.	100 n	10 % 25 V 0805
C560	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C562	2320596	Ceramic cap.	3.3 n	5 % 50 V 0402
C563	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C564	2320554	Ceramic cap.	56 p	5 % 50 V 0402
C565	2611691	Tantalum cap.	470 u	20 % 10 V
7.3x4.3x4.1				
C566	2611691	Tantalum cap.	470 u	20 % 10 V
7.3x4.3x4.1				
C567	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C568	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C569	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C571	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C572	2610024	Tantalum cap.	2.2 u	20 % 16 V
3.2x1.6x1.6				
C573	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C574	2320554	Ceramic cap.	56 p	5 % 50 V 0402
C575	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C576	2320554	Ceramic cap.	56 p	5 % 50 V 0402
C577	2320554	Ceramic cap.	56 p	5 % 50 V 0402
C579	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C580	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C581	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C582	2320540	Ceramic cap.	15 p	5 % 50 V 0402
C583	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C584	2310248	Ceramic cap.	4.7 n	5 % 50 V 1206
C585	2320548	Ceramic cap.	33 p	5 % 50 V 0402
C586	2320554	Ceramic cap.	56 p	5 % 50 V 0402
C587	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C588	2320592	Ceramic cap.	2.2 n	5 % 50 V 0402
C589	2320602	Ceramic cap.	4.7 p	0.25 % 50 V 0402

C590	2320534	Ceramic cap.	8.2 p	0.25 % 50 V 0402
C591	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C592	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C593	2320554	Ceramic cap.	56 p	5 % 50 V 0402
C595	2320532	Ceramic cap.	6.8 p	0.25 % 50 V 0402
C596	2320532	Ceramic cap.	6.8 p	0.25 % 50 V 0402
C597	2320536	Ceramic cap.	10 p	5 % 50 V 0402
C598	2320602	Ceramic cap.	4.7 p	0.25 % 50 V 0402
C599	2320554	Ceramic cap.	56 p	5 % 50 V 0402
C601	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C618	2320483	Ceramic cap.	68 n	10 % 16 V 0603
C627	2610023	Tantalum cap.	4.7 u	20 % 10 V 3.5x2.8x1.2
L103	3203701	Ferrite bead 33r/100mhz 0805		0805
L170	3203701	Ferrite bead 33r/100mhz 0805		0805
L171	3203701	Ferrite bead 33r/100mhz 0805		0805
L172	3640035	Filt z>450r/100m 0r7max 0.2a 0603		0603
L173	3640035	Filt z>450r/100m 0r7max 0.2a 0603		0603
L174	3640035	Filt z>450r/100m 0r7max 0.2a 0603		0603
L500	3645121	Chip coil	6 n	5 % Q=32/800M 0603
L501	3641626	Chip coil	220 n	2 % Q=30/100 MHz 0805
L502	3608326	Chip coil	330 n	5 % Q=33/50 MHz 1206
L503	3645121	Chip coil	6 n	5 % Q=32/800M 0603
L504	3641626	Chip coil	220 n	2 % Q=30/100 MHz 0805
L505	3643039	Chip coil	220 n	5 % Q=35/100 MHz 0805
L506	3645131	Chip coil	8 n	5 % Q=8/100M 0603
L507	3643039	Chip coil	220 n	5 % Q=35/100 MHz 0805
L508	3645131	Chip coil	8 n	5 % Q=8/100M 0603
L509	3645175	Chip coil	12 n	5 % Q=12/100 MHz 0603
L510	3203705	Ferrite bead 0.015r 42r/100m 0805		0805
L511	3648808	Chip coil		10 % Q=50 1206
L512	3645161	Chip coil	150 n	5 % Q=14/100 MHz 0603
L513	3643025	Chip coil	56 n	5 % Q=40/200 MHz 0805
L514	3645157	Chip coil	100 n	10 % Q=12/100 MHz 0603
L515	3645157	Chip coil	100 n	10 % Q=12/100 MHz 0603

L516	3203709	Ferrite bead 0.5r 120r/100m 0402		0402
G601	4350143	Vco 1006–1031mhz 2.8v 10ma gsm		
G690	4510217	VCTCXO	13.000 M	+–5PPM 2.8V
F170	5119019	SM, fuse f 1.5a 32v 0603		
Z500	4512075	Dupl 890–915/935–960mhz 15.0x8.2		15.0x8.2
Z601	4511049	Saw filter	947.5+–12.5 M	3.1x3.1
Z602	4511015	Saw filter	902.5+–12.5 M	/3.8DB 4X4
Z650	4510137	Saw filter	71+–0.09 M	14.2x8.4
Z701	4510009	Cer.filt 13+–0.09mhz 7.2x3.2		7.2x3.2
V104	4113651	Trans. supr.	QUAD	6 V SOT23–5
V116	4110067	Schottky diode	MBR0520L	20 V 0.5 A SOD123
V140	4219904	Transistor x 2	UMX1	npn 40 V SOT363
V170	4113651	Trans. supr.	QUAD	6 V SOT23–5
V190	4113651	Trans. supr.	QUAD	6 V SOT23–5
V195	4110014	Sch. diode x 2	BAS70–07	70 V 15 mA SOT143
V201	4110014	Sch. diode x 2	BAS70–07	70 V 15 mA SOT143
V270	4210100	Transistor	BC848W	npn 30 V SOT323
V271	4113601	Emi filter emif01–5250sc5 sot23–5		SOT23–5
V502	4551001	Dir.coupler 0.8–1ghz 3.5x1.8x1.2		3.5x1.8x1.2
V503	4110014	Sch. diode x 2	BAS70–07	70 V 15 mA SOT143
V660	4210066	Transistor	BFR93AW	npn 12 V 35 mA
SOT323				
V700	4110018	Cap. diode	BB135	30 V SOD323
V702	4210100	Transistor	BC848W	npn 30 V SOT323
D100	4340523	IC, 1xbilater. switch sot3	TC7S66FU	SOT353
D200	4370421	Mad2 rom4 v14 f721727 c10		UBGA176
D210	4340507	IC, flash mem.		CSP48
D220	4340499	IC, SRAM		STSOP32
D230	4342264	IC, EEPROM		SO8S
D250	4370371	Cobba	gj b09 bb asic	UBGA
N110	4370391	Ccont2h	dct3 bb asic	TQFP64
N120	4370165	Chaps	charger control	SO16
N201	4340164	IC, regulator	TK11247	4.75 V 180 mA SSO6
N500	4370451	Rf9117e6	pw amp	890–915mhz
N600	4370253	Crfu1a rx+tx uhf gsm v5 sot401–1		SOT401–1
N690	4370351	Summa v2 rx,tx,pll,pcontr. tqfp48		TQFP48
X150	5409089	SM, sim conn 2x3pol p2.54 1a h1.		H1.5
X160	5469087	SM, battery conn 2dc+2af 12vdc 2		2A
X171	5429011	SM, coax conn f 50r 100v 0.3a 3g		3GHZ
X190	5469095	SM, conn 2x25 m p0.5 str. pcb/pc		PCB/PCB
X191	5469093	SM, mmc conn 7pol p2.5 5vdc 100m		100MA
A500	9517021	RF shield large dmc01227 rae–		RAE–2
A501	9517022	RF shield medium dmc01228 rae–		RAE–2
A502	9517023	RF shield small dmc01229 rae–		RAE–2
	9854299	PCB BS8	73.70X50.90X1.3	M8 8/PA

PDA Module Parts List

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Item	Code	Description	Value/Type	
R300	1430693	Chip resistor	5.6	5 % 0.063 W 0402
R301	1430726	Chip resistor	100	5 % 0.063 W 0402
R302	1430693	Chip resistor	5.6	5 % 0.063 W 0402
R303	1430693	Chip resistor	5.6	5 % 0.063 W 0402
R304	1430693	Chip resistor	5.6	5 % 0.063 W 0402
R310	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R400	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R401	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R403	1430742	Chip resistor	390	5 % 0.063 W 0402
R405	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R407	1430842	Chip resistor	680 k	1 % 0.063 W 0402
R408	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R428	1430690	Chip jumper		0402
R430	1430700	Chip resistor	10	5 % 0.063 W 0402
R431	1430784	Chip resistor	15 k	5 % 0.063 W 0402
R432	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R433	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R434	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R440	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R460	1430744	Chip resistor	470	5 % 0.063 W 0402
R461	1430298	Chip resistor	1.0 M	2 % 0.063 W 0603
R462	1430061	Chip resistor	511 k	1 % 0.063 W 0603
R463	1430031	Chip resistor	100 k	1 % 0.063 W 0603
R465	1430842	Chip resistor	680 k	1 % 0.063 W 0402
R466	1430187	Chip resistor	47 k	1 % 0.063 W 0402
R467	1430842	Chip resistor	680 k	1 % 0.063 W 0402
R468	1430187	Chip resistor	47 k	1 % 0.063 W 0402
R469	1430122	Chip resistor	4.7 M	5 % 0.063 W 0603
R493	1430842	Chip resistor	680 k	1 % 0.063 W 0402
R494	1430842	Chip resistor	680 k	1 % 0.063 W 0402
R495	1430842	Chip resistor	680 k	1 % 0.063 W 0402
R802	1430726	Chip resistor	100	5 % 0.063 W 0402
R803	1430722	Chip resistor	68	5 % 0.063 W 0402
R804	1430726	Chip resistor	100	5 % 0.063 W 0402
R805	1430722	Chip resistor	68	5 % 0.063 W 0402
R806	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R808	1430714	Chip resistor	33	5 % 0.063 W 0402
R809	1430714	Chip resistor	33	5 % 0.063 W 0402
R810	1430720	Chip resistor	56	5 % 0.063 W 0402
R811	1430726	Chip resistor	100	5 % 0.063 W 0402
R812	1430722	Chip resistor	68	5 % 0.063 W 0402
R813	1430726	Chip resistor	100	5 % 0.063 W 0402

R814	1430722	Chip resistor	68	5 % 0.063 W 0402
R815	1430726	Chip resistor	100	5 % 0.063 W 0402
R816	1430722	Chip resistor	68	5 % 0.063 W 0402
R818	1430726	Chip resistor	100	5 % 0.063 W 0402
R819	1430722	Chip resistor	68	5 % 0.063 W 0402
R821	1430726	Chip resistor	100	5 % 0.063 W 0402
R822	1430722	Chip resistor	68	5 % 0.063 W 0402
R844	1430726	Chip resistor	100	5 % 0.063 W 0402
R845	1430726	Chip resistor	100	5 % 0.063 W 0402
R846	1430726	Chip resistor	100	5 % 0.063 W 0402
R847	1430726	Chip resistor	100	5 % 0.063 W 0402
R848	1430726	Chip resistor	100	5 % 0.063 W 0402
R849	1430726	Chip resistor	100	5 % 0.063 W 0402
R850	1430726	Chip resistor	100	5 % 0.063 W 0402
R851	1430722	Chip resistor	68	5 % 0.063 W 0402
R852	1430726	Chip resistor	100	5 % 0.063 W 0402
R853	1430722	Chip resistor	68	5 % 0.063 W 0402
R855	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R856	1430714	Chip resistor	33	5 % 0.063 W 0402
R857	1430796	Chip resistor	47 k	5 % 0.063 W 0402
R885	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R886	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R887	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R888	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R890	1430796	Chip resistor	47 k	5 % 0.063 W 0402
R891	1430691	Chip resistor	2.2	5 % 0.063 W 0402
R892	1430691	Chip resistor	2.2	5 % 0.063 W 0402
C300	2610003	Tantalum cap.	10 u	20 % 10 V
3.2x1.6x1.6				
C301	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C302	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C401	2320481	Ceramic cap.	5R 1 u	10 % 0603
C402	2320481	Ceramic cap.	5R 1 u	10 % 0603
C403	2320805	Ceramic cap.	100 n	10 % 10 V 0402
C404	2320805	Ceramic cap.	100 n	10 % 10 V 0402
C405	2320805	Ceramic cap.	100 n	10 % 10 V 0402
C406	2320805	Ceramic cap.	100 n	10 % 10 V 0402
C407	2320805	Ceramic cap.	100 n	10 % 10 V 0402
C408	2320805	Ceramic cap.	100 n	10 % 10 V 0402
C409	2320805	Ceramic cap.	100 n	10 % 10 V 0402
C410	2320805	Ceramic cap.	100 n	10 % 10 V 0402
C411	2320805	Ceramic cap.	100 n	10 % 10 V 0402
C413	2320805	Ceramic cap.	100 n	10 % 10 V 0402
C414	2320604	Ceramic cap.	18 p	5 % 50 V 0402
C415	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C416	2320805	Ceramic cap.	100 n	10 % 10 V 0402
C417	2320604	Ceramic cap.	18 p	5 % 50 V 0402

C430	2320592	Ceramic cap.	2.2 n	5 % 50 V 0402
C431	2320588	Ceramic cap.	1.5 n	5 % 50 V 0402
C432	2320805	Ceramic cap.	100 n	10 % 10 V 0402
C433	2320576	Ceramic cap.	470 p	5 % 50 V 0402
C434	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C435	2320576	Ceramic cap.	470 p	5 % 50 V 0402
C436	2320548	Ceramic cap.	33 p	5 % 50 V 0402
C437	2320576	Ceramic cap.	470 p	5 % 50 V 0402
C438	2320540	Ceramic cap.	15 p	5 % 50 V 0402
C439	2320572	Ceramic cap.	330 p	5 % 50 V 0402
C440	2320805	Ceramic cap.	100 n	10 % 10 V 0402
C441	2320805	Ceramic cap.	100 n	10 % 10 V 0402
C442	2320805	Ceramic cap.	100 n	10 % 10 V 0402
C443	2320805	Ceramic cap.	100 n	10 % 10 V 0402
C444	2320805	Ceramic cap.	100 n	10 % 10 V 0402
C445	2320805	Ceramic cap.	100 n	10 % 10 V 0402
C446	2320805	Ceramic cap.	100 n	10 % 10 V 0402
C447	2320805	Ceramic cap.	100 n	10 % 10 V 0402
C448	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C470	2310003	Ceramic cap.	470 n	10 % 16 V 0805
C471	2610003	Tantalum cap.	10 u	20 % 10 V
3.2x1.6x1.6				
C472	2611695	Tantalum cap.	100 u	20 % 6.0x3.2x2.6
C473	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C474	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C475	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C476	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C477	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C478	2320107	Ceramic cap.	10 n	5 % 50 V 0603
C479	2320618	Ceramic cap.	4.7 n	5 % 25 V 0402
C480	2310791	Ceramic cap.	33 n	20 % 50 V 0805
C481	2611683	Tantalum cap.	33 u	10 % 35 V
7.3x4.3x2.9				
C482	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C483	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C484	2320107	Ceramic cap.	10 n	5 % 50 V 0603
C485	2320801	Ceramic cap.	100 n	20 % Y5 V 0603
C486	2611697	Tantalum cap.	33 u	20 % 10 V
6.0x3.2x2.6				
C487	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C488	2320779	Ceramic cap.	100 n	10 % 16 V 0603
C489	2320572	Ceramic cap.	330 p	5 % 50 V 0402
C490	2320778	Ceramic cap.	10 n	10 % 16 V 0402
C491	2320778	Ceramic cap.	10 n	10 % 16 V 0402
C492	2320801	Ceramic cap.	100 n	20 % Y5 V 0603
C493	2320778	Ceramic cap.	10 n	10 % 16 V 0402
C494	2320588	Ceramic cap.	1.5 n	5 % 50 V 0402

C495	2320592	Ceramic cap.	2.2 n	5 % 50 V 0402
C496	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C800	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C801	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C802	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C803	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C804	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C807	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C808	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C809	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C815	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C819	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C820	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C821	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C822	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C850	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C851	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C852	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C853	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C854	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C855	2320805	Ceramic cap.	100 n	10 % 10 V 0402
C880	2611691	Tantalum cap.	470 u	20 % 10 V 7.3x4.3x4.1
C881	2611691	Tantalum cap.	470 u	20 % 10 V 7.3x4.3x4.1
C882	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C883	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C884	2320781	Ceramic cap.	47 n	20 % 16 V 0603
C885	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C886	2320552	Ceramic cap.	47 p	5 % 50 V 0402
C887	2320552	Ceramic cap.	47 p	5 % 50 V 0402
C888	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C889	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C890	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C891	2320572	Ceramic cap.	330 p	5 % 50 V 0402
C892	2320805	Ceramic cap.	100 n	10 % 10 V 0402
C893	2320560	Ceramic cap.	100 p	5 % 50 V 0402
L455	3640473	Chip coil		20 % 245 mA 4.8x4.8x2.3
L456	3640517	Chip coil		20 % 0.79 A 1210
B430	4510003	Crystal	32.768 k	+–20PPM 8x3.8
V870	4113651	Trans. supr.	QUAD	6 V SOT23–5
V871	4110014	Sch. diode x 2	BAS70–07	70 V 15 mA SOT143
V872	4211202	DM MosFet		p–ch 50 V 0.13 A SOT23
V873	4200603	Transistor	BCX17	pnp 45 V 500 mA SOT23

V880	4210100	Transistor	BC848W	npn 30 V SOT323
D440	4340525	IC, flash mem.		CSP64
D441	4340525	IC, flash mem.		CSP64
D442	4340525	IC, flash mem.		CSP64
D443	4340571	Dram 1mx16 60ns 2v7	csp40	CSP40
N300	4860031	Tfdu4100 irda tx/rx>2.7v 115kbits		115KBITS
N400	4370447	IC, MCU		PBGA256
N450	4370477	Phaser21 pda power asic	tqfp64	TQFP64
N496	4340405	IC, comparat. 2–8v sot23	LMC7215IM5	SOT23–5
N880	4340303	IC, af amp 1.1w 2.0–5.5v so	LM4861	SO8S
S390	5309001	Reed relay 0.5a 08–15.5at d2.5x1		d2.5x15
X451	9510424	Backup battery holder dmd03475		
X800	5460029	SM, fpc conn 51pol p0.3 90deg l.		L.C
X830	5469097	SM, conn 2x25 f p0.5 str. pcb/pc		PCB/PCB
	9854301	PCB BS1 143.0X49.3X0.8 M8		4/PA

UIF Module Parts List

0201097 BS2 UI MODULE EDMS Issue: 2.13

Item	Code	Description	Value/Type	
R700	1430122	Chip resistor	4.7 M	5 % 0.063 W 0603
R701	1430830	Chip resistor	1.0 M	5 % 0.063 W 0402
R702	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R704	1620031	Res network 0w06 2x1k0 j	0404	0404
R705	1620031	Res network 0w06 2x1k0 j	0404	0404
R706	1620031	Res network 0w06 2x1k0 j	0404	0404
R707	1620031	Res network 0w06 2x1k0 j	0404	0404
R708	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R730	1430122	Chip resistor	4.7 M	5 % 0.063 W 0603
R731	1430830	Chip resistor	1.0 M	5 % 0.063 W 0402
R732	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R734	1820033	NTC resistor		0805
R735	1430145	Chip resistor	100 k	1 % 0.063 W 0402
C701	2312207	Ceramic cap.	10.F n	10 % 250 V 0805
C702	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C703	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C704	2320779	Ceramic cap.	100 n	10 % 16 V 0603
C705	2320779	Ceramic cap.	100 n	10 % 16 V 0603
C706	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C707	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C708	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C709	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C710	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C711	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C712	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C713	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C714	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C731	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C732	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C733	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C734	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C735	2611705	Tantalum cap.	220 n	20 % 50 V
3.2x1.6x1.6				
C736	2312207	Ceramic cap.	10.F n	10 % 250 V 0805
C737	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C738	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C739	2310003	Ceramic cap.	470 n	10 % 16 V 0805
C740	2604022	Tantalum cap.	0.1 u	20 % 35 V
3.2x1.6x1.6				
C741	2604022	Tantalum cap.	0.1 u	20 % 35 V
3.2x1.6x1.6				
C742	2604054	Tantalum cap.	0.47 u	20 % 35 V

3.5x2.8x1.9				
C743	2604022	Tantalum cap.	0.1 u	20 % 35 V
3.2x1.6x1.6				
C744	2604022	Tantalum cap.	0.1 u	20 % 35 V
3.2x1.6x1.6				
C745	2320544	Ceramic cap.	22 p	5 % 50 V 0402
L700	3640493	Chip coil		10 % 72 mA SMD
L730	3640491	Chip coil		20 % 104 mA SMD
V700	4110078	Schdix2 bas70–05w	70v 70ma	SOT323
V701	4115841	Diode FAST	200 V TRR<60 ns	SC59
V702	4210052	Transistor	DTC114EE	npn RB V EM3
V703	4211477	MosFet	p–ch 16 V 16V1 A	SOT143
V730	4115841	Diode FAST	200 V TRR<60 ns	SC59
V731	4211477	MosFet	p–ch 16 V 16V1 A	SOT143
V732	4210052	Transistor	DTC114EE	npn RB V EM3
N700	4340489	Hv823 hv el lamp driver 400mw		SO8
N730	4340489	Hv823 hv el lamp driver 400mw		SO8
X700	5460029	SM, fpc conn 51pol p0.3 90deg l.		L.C
X730	5469083	SM, fpc conn 18pol p0.5 0.4a l.c		
X790	5429011	SM, coax conn f 50r 100v 0.3a 3g		3GHZ
X791	9510427	Antenna contact dmd03810		RAE–2
	9795052	Keydome sheet dmd03766		rae–2
	9854300	PCB BS2	145.25X51.0X0.6	M4 4/PA

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Chapter 12

QUICK GUIDE

Contents

Quick guide

FOR YOUR SAFETY Read these simple guidelines. Breaking the rules may be dangerous or illegal. Further detailed information is given in this manual.

ROAD SAFETY COMES FIRST Do not use the communicator while driving; park the vehicle first.

INTERFERENCE All wireless phones may get interference which could affect performance.

SWITCH OFF IN HOSPITALS Follow any regulations or rules. Switch off the phone near medical equipment.

SWITCH OFF IN AIRCRAFT Wireless phones can cause interference. Using them on aircraft is illegal.

SWITCH OFF WHEN REFUELLING Do not use the phone at a refuelling point. Do not use near fuel or chemicals.

SWITCH OFF NEAR BLASTING Do not use the phone where blasting is in progress. Observe restrictions, and follow any regulations or rules.

USE SENSIBLY Use only in the normal position (to ear). Do not touch the antenna unnecessarily.

USE QUALIFIED SERVICE Only qualified service personnel must install or repair equipment.

ACCESSORIES AND BATTERIES Use only approved accessories and batteries. Do not connect incompatible products.

MAKING CALLS VIA THE PHONE Close the cover and ensure the phone is switched on and in service. Enter the phone number, including the area code, then press ”CALL”. To end a call press ”END CALL”. To answer a call press ”CALL” .

EMERGENCY CALLS Close the device cover. Ensure the phone is switched on and in service. Hold for several seconds, to clear the display. Enter the emergency number, then press ”CALL”. Give your location. Do not end the call until told to do so.

MAKE BACKUP COPIES Remember to make backup copies of all important data.

CONNECTING TO OTHER DEVICES When connecting to any other device, read its user’s guide for detailed safety instructions. Do not connect incompatible products.

INFRARED PRECAUTIONS Do not point the IR beam at anyone’s eye or allow it to interfere with other IR devices.

First start–up

The Nokia 9110 Communicator can send and receive calls and messages only when the phone is switched on, has a valid SIM card fitted, and is located in the service area of the cellular network. However, emergency calls to the international emergency number 112 may be made without the SIM card in some networks. Please, check with your network operator.

1 Close the device cover and ensure that the phone is switched off. If it is on, press the power on/off switch

2 If the battery is connected to the communicator, remove the battery: press the catch at the top of the battery and lift the battery away from the battery cavity.

3 Slide the SIM card into the SIM card slot: ensure that the gold contacts of the SIM card are facing down and that the bevelled corner of the card is on the right.

Note: Keep all miniature SIM cards out of small children's reach.

4 When the SIM card is properly inserted into the SIM card slot, the bevelled corner will remain visible.

5 When you are sure that the SIM card is correctly installed, replace the battery. If there is little or no charge in the battery, it is recommended that you connect the communicator to the charger and start charging the battery before continuing with the start–up procedure. See below.

6 Open the cover of the communicator. You will see a welcome screen while the communicator performs a self–test.

7 After the self–test is complete, you will see a list of countries on the display, see figure 4. Scroll the dark grey selection frame using the arrow keys on the keyboard over the name of your home country. Press thebutton on the right side of the display next to the command **OK**. Thecapital of your home country will be set as your home city.

8 Write the current date in the input field using the format *dd.mm.yy*, forexample *22.03.98*, and press **OK**.

Note: The battery does not fit into place if the SIMcard is not correctly installed. Do not force the battery into place! Check that you have inserted the SIM card into the slot as described above. If the SIM card is incorrectly installed, remove it by pulling it away from the slot, and insert it again.

9 Write the current time using the 24–hour format *hh:mm*, for example 17:25, and press **OK**.

10 Enter your contact information in the user data card and press OK. The first start–up is now completed.

After the start–up, do not immediately remove the battery, as the battery charges the backup battery that supplies power to the real–time clock of the communicator.

To charge the battery

1 Connect the charger lead to the bottom of the communicator:

2 Connect the charger to the proper voltage AC wall outlet. While charging is in progress, the battery charge indicator scrolls on the display.

To use the battery

Use only batteries approved by the communicator manufacturer and recharge the battery only with the chargers approved by the manufacturer. With approved chargers and accessories, the battery can be charged continuously. The battery need not be fully discharged before recharging. When a charger is not in use, disconnect it from the power source. Do not leave the battery connected to a charger for longer than a week, since excessive charging may shorten its life. If left unused, a fully charged battery will discharge itself over time.

The battery can be charged and discharged hundreds of times, but it will eventually wear out. When the operating time (talk–time and standby time) is noticeably shorter than normal, it is time to buy a new battery.

Note: The communicator can be used normally during charging.

Temperature extremes will affect the ability of your battery to charge: allow it to cool down or warm up first.

Battery operation time is affected by the following: whether both the phone and the communicator interface are on, radio signal strength, various phone settings, the use of the backlight, and the length of the screen blanker period.

It is recommended always to keep a charged battery in the communicator. Keeping the battery charged maximises the lifetime of the backup battery supplying power to the real–time clock of the communicator. In case the backup battery is drained, it will be automatically charged the next time a charged battery is reconnected to the communicator.

Always close the device cover before removing the battery. Closing the cover will save all data.

Note

Use the battery only for its intended purpose.

Never use any charger or battery that is damaged or worn out.

Do not short–circuit the battery. Accidental short–circuiting can occur when a metallic object (coin, clip or pen) causes direct connection of the + and –terminals of the battery (metal strips on the back of the battery), for example, when you carry a spare battery in your pocket or purse. Short–circuiting the terminals may damage the battery or the connecting object.

Leaving the battery in hot or cold places, such as in a closed car in summer or winter conditions, will reduce the capacity and lifetime of the battery. Always try to keep the battery between +15°C (+59°F) and +25°C (+77°F). A communicator with a hot or cold battery may temporarily not work, even when the battery is fully charged. The performance of Lithium–ion batteries is particularly limited in temperatures below 0°C (+32°F).

Do not dispose of batteries in a fire!

Batteries must be recycled or disposed of properly. Batteries must not be disposed of in municipal waste.

Communicator

To switch on the communicator interface:

The communicator interface is switched on simply by opening the cover. The application that was active the last time the communicator was used is shown on the display. When you close the cover, the communicator interface switches off its display and saves all data.

Display elements

The indicators show the currently active application along with other information about the communicator, e.g. battery level and field strength.

The commands always relate to the four command buttons. In this guide, commands are in **bold** and items shown on the display are in *italics*.

When this guide instructs you, for example, to press **Open**, it means that you must press the command button next to the command name.

When the search field is shown at the bottom of the display, you can search for items by using the keyboard to enter text into the search field.

The scroll bar indicates that there are more items than currently shown on the display. You can scroll the display with the arrow keys of the keyboard.

When the selection frame is shown, one item is always automatically selected. You can select other items by moving the selection frame with the arrow keys on the keyboard. After the correct item has been selected, press the command you wish to apply to the item, for example, **Open** or **Delete**.

The Menu button opens up a new set of options.

The Zoom button magnifies the view on the display.

The Backlight button switches the display light on and off.

To connect to a PC

You can connect your communicator to a suitable PC using the PC Suite for Nokia 9110 Communicator program, which is found on the CD–ROM supplied in the communicator sales package. With the PC Suite you can synchronise contact information, calendar and To–do list between your communicator and a PC, transfer and backup data, and install various software on your communicator. You need only to connect your communicator to a PC; everything else is done on the PC.

The PC Suite for Nokia 9110 Communicator works with Windows 95/98 and NT.

When connecting your communicator to a PC, you can also select whether to use the infrared or the cable connection.

To use the PC Suite with an infrared connection

1 Make sure that the infrared port of the communicator faces the infrared port of the PC.

2 Start the PC Suite software on the PC.

3 Start the Infrared activation application on your communicator and press Activate. See ”System” in this guide.

To use the PC Suite with a cable connection

1 Connect the 9–pin end of the RS–232 cable to the COM port of the PC, and the other end to the connector at the bottom of the communicator.

2 Start the PC Suite software on the PC.

To use the Nokia Communicator Server

If you have Windows 3.11 or Apple Macintosh, use the Nokia Communicator Server program for PC connectivity. The Windows version of the Nokia Communicator Server is found on the diskette in the sales package, and the Apple Macintosh version is on the CD–ROM.

With the Nokia Communicator Server you can use the communicator applications that require PC connectivity. You need to connect your communicator to a PC and start the necessary application on the communicator.

Contacts

Contacts is used to manage contact information, such as phone numbers and addresses. The entries in the Contacts directory are called contact cards. The Contacts directory is used by all the communications applications: Telephone, Fax, SMS and Mail.

To make a contact card

1 Press the Contacts application button on the communicator keyboard to start the Contacts application.

2 Press New and write the necessary contact information in the empty contact card.

Caution: Beware of viruses. Only install on the communicator software you have obtained from sources that offer adequate protection against viruses.

Telephone

Telephone is used for making and receiving voice calls and adjusting the Telephone settings. To start the Telephone application, press the Tel. application button on the keyboard.

To make a call

There are two ways to make a call via the communicator interface:

1 Select a contact from the Telephone directory by moving the selection frame over the contact's name, and press **Call**. If the contact has only one phone number, the number is called directly.

If the contact has several phone numbers, a pop–up box opens, listing the phone numbers. Choose a number from the list and press **Call**. Or,

2 Type the phone number in the search field with the keyboard and press Call.

To answer a call

You can answer a call either via the phone or the communicator interface.

When you receive a phone call, a note appears on the communicator interface display. Press **Answer** to answer the call, or press **End call** to dismiss the call.

Flight profile

The flight profile prevents you from accidentally turning on your phone in an aircraft.

To set on the flight profile

1 Press Settings in the Telephone main view.

2 Choose *Profiles* and press Change.

3 Select *Profile in use*, press Change and scroll to *Flight*.

4 Press OK.

With the flight profile active, you may read previously downloaded mail, write mail, notes, short messages, faxes, or update your calendar. Once you have left the aircraft, you can turn off the flight profile by pressing **Exit profile**, turn on the phone by pressing , and your short messages, faxes and mail will be sent automatically.

When the communicator is in the flight profile, emergency calls must be made from the phone:

1 Press ”CALL” . The phone display will read FLIGHT PROFILE ACTIVE.

2 While the FLIGHT PROFILE ACTIVE text is visible (for approximately five seconds) you can dial the emergency number, e.g. 112.

3 Press ”CALL”.

IMPORTANT! Never use the phone when in an aircraft. If the aircraft personnel allow use of the communicator interface, you MUST activate the flight profile. The flight profile will allow use of the communicator interface only and will prevent use of the phone.

Be aware that all communications applications, Telephone, Fax, SMS, Mail, and Internet, require use of the phone.

Fax

To start the Fax application, press the Fax button on the communicator keyboard.

Fax sending and receiving requires that fax calls are supported by the network you are using and that the fax service is activated for your SIM card. Contact your service provider for details.

To send a fax

1 Press Write fax, and write the fax message.

2 Press Recipient. The Fax directory opens.

3 Select a recipient and press Select.

4 Press Send to send the fax.

To read a received fax

Faxes are received automatically. There are two ways to read a received fax:

1 When you receive a note informing you that you have received a fax, press View. To read the fax later, press Cancel. Or,

2 Select the Received faxes folder and press Open. Select the fax and press Open.

Use the arrow keys to scroll up and down in the fax, or from left to right. To zoom the fax, press **View**, and then **Zoom in** or **Zoom out**.

Short messages

To start the short message application, press the SMS application button on the communicator keyboard.

Short message sending and receiving requires that the Short Message Service (SMS) is available in the network you are using and activated for your SIM card. Contact your service provider for details.

Before you can send short messages, you must store the SMS message centre number in the settings of the SMS application.

To send a message

1 Press Write message and write the message contents.

2 Press Recipient. The SMS directory opens.

3 Select a recipient and press Select.

4 Press Send. If your message is longer than 160 characters, it will be sent as several short messages, provided that your network support this function.

To read a received message

There are two ways to read a received message:

1 When you receive a note informing you that you have received a message, press **View**. To read the message later, press **Cancel**. Or,

2 Select the Received messages folder and press Open. Select the message and press **Open**.

Internet

Internet access requires that you have obtained an Internet access point from an Internet service provider and configured the Internet settings correctly.

Contact your dealer for details.

1 Press the Internet application button on the communicator keyboard.

2 Choose one of the applications and press Select.

The connection to the Internet is established via a data call. This requires that data calls are supported by the network you are using and that this service is activated for your SIM card. Contact your service provider for details.

To close the connection to the Internet, press **Hang up** in the Internet main view.

Mail

Mail enables you to send and receive e–mail. Mail is compliant with the

Internet standards SMTP, IMAP4, POP3, MIME1 and MIME2. Before using this application, be sure to enter the correct Mail settings.

1 Press Write mail and write the message.

2 Press Recipient. The Mail directory opens.

3 Select a contact and press Select. If the contact has several mail addresses, choose the address from the pop–up box and press **Select**.

4 The Mail envelope opens. In the Mail envelope you can check the sending information and add more recipients by pressing **Add recipient** or entering addresses manually.

5 Press Send.

The Mail application main view shows the Remote mailbox. The Remote mailbox, which receives all your mail, is located on a remote computer.

1 Move the selection frame over the Remote mailbox and press Connect. The communicator connects to the Remote mailbox. All mail in the Remote mailbox is shown. An unread message has the icon next to it.

2 Fetch all new mail by pressing Fetch new, or fetch individual messages by selecting the message(s) and pressing **Fetch selected**. All fetched mail goes to the Received mail folder of the communicator.

3 When you have fetched all the mail messages you want, disconnect from the Remote mailbox by pressing **Hang up**. If you have pressed **Fetch new**, the connection is closed automatically after the message(s) have been fetched.

4 In the Mail application, select the Received mail folder and press Open. Select a message and press **Open** again to read the message.

World Wide Web

The World Wide Web application is a hypertext–based system for finding and accessing resources on the Internet.

To open a WWW page

1 Write the URL address of the page in the input field, or select a page from the Bookmarks list in the WWW main view.

2 Press Go.

3 A data call is made to your Internet access point. After a connection has been established, the chosen page is fetched from the Internet and shown on the display.

4 To follow a hyperlink, select it with the selection frame and press Go.

Telnet and Terminal

These applications allow your communicator to connect to computers, like mainframe computers, which provide terminal services through the Internet (Telnet) or direct dial–in terminal services (Terminal). Both applications emulate the VT100 terminal.

To connect to a Telnet or Terminal host

1 Press Define and define a new host (press New) or edit an existing host (press **Edit**).

2 Return to the Telnet or Terminal main view, select a host and press Connect.

3 To send or copy texts between the host computer and the communicator, press **Send text** or **Capture text**. The command is available once you have connected to the host.

4 To disconnect from the host, press Hang up.

Note: The Telnet application canbe installed to your communicator from the CD–ROM included in the sales package.

Text Web

With Text Web you can fetch information from the Internet, using SMS. You can also access services provided by your network operator and Nokia. To define services

1 Press Settings in the Text Web main view.

2 Press New to open an empty service information card, or press Edit to modify an existing service. Enter the title of the service, the server number, and the service number.

To fetch information

1 In the Text Web main view, scroll to one of the service access points that you have defined and press **Select**.

2 Enter in the space provided a keyword that describes the type of information you are looking for.

3 Press Send. When you receive a reply from the service provider, the TTML browser opens up. Press the arrow keys on the keyboard to move from one hotspot to another. To follow a hyperlink, press **Fetch**.

Notes

Notes is used for writing texts and managing documents stored on the communicator.

To start the Notes application, press the Notes application button on the communicator keyboard.

To write a note

1 Press Write note in the Notes main view. If you want to format the text, press **Style**.

To read documents

1 Select a folder in the Notes main view and press Open.

2 Select a document and press Open.

To send a document

1 Press Send in the opened Note editor.

2 Select one of the following options and press Select:

To send as a fax, select *Send as fax*.

To send as a short message, select *Send as short message*.

To send as e–mail, select *Send as mail*.

Calendar

To start the Calendar application, press the Calendar application button onthe communicator keyboard.

Monthly schedule

The monthly schedule is the main view of the Calendar. The daily events list on

the right side of the display can be edited in the daily schedule.

Weekly schedule

To check the weekly schedule, press **Week** in the monthly or the daily schedule. The weekly schedule shows the timetable of the selected week.

Daily schedule

The daily schedule is opened by pressing **Day** in the monthly or the weekly schedule. The daily schedule displays the events of the selected day. To adjust the details of the selected event, press **Details**.

To book events

You can book events in other communicators or remote calendar servers.

1 Select an event in the daily schedule or write a new one.

2 Press Calendar booking in the Details view and select whether to make the booking as a request or a reservation.

3 Press Send as SMS to open the SMS directory where you can select the recipient.

4 Press Send to send the booking.

System

To start one of the System applications, press the System application button on the communicator keyboard, choose an application and press **Select**.

The Install/Remove software and Backup/restore applications require the use of either the PC Suite or the Nokia Communicator Server.

To lock the communicator

1 Open the Security application and press Lock system.

2 Enter your lock code if prompted.

To unlock the communicator

1 Enter your lock code in the input field.

2 Press OK.

Infrared activation

If you want to use the PC Suite for Nokia 9110 Communicator program with the infrared connection, or you want to transfer data between your communicator and another device via the infrared, you need to use the Infrared activation application.

1 Make sure that the infrared port of the communicator faces the infrared port of the PC or another device.

2 Open the Infrared activation application on the communicator.

3 Press Activate. When transferring data between two communicators, the activation is done in the communicator that receives the data.

4 To end the infrared connection, press Disable.

Digital camera connectivity

The Digital camera connectivity application enables you to transfer images between your communicator and a digital still camera via the infrared connection.

1 Open the Digital camera connectivity application and press Image list.

2 If you are transferring files from your communicator, select the UPF image(s) you want to transfer.

3 Make sure that the infrared port of your communicator faces the infrared port of the other device.

4 Press Send to send the images from your communicator, or press Receive to start transferring images from the other device to your communicator.

To use the communicator as a fax modem

The communicator can be used as a PC fax modem. This requires that data calls are supported by the network you are using and that this service is activated for your SIM card. Contact your service provider for details.

1 Open the Fax modem application, press Settings and select either the cable or the infrared connection. The infrared connection is recommended.

2 Connect the communicator to a PC.

3 Press Activate. When the communicator is used as a fax modem, the communications features of the communicator are disabled.

4 To stop using the communicator as a fax modem, press Disable.

To remove data

Data removal enables you to remove data from your communicator.

1 Select one of the data groups: *All device data*, *Calendar data*, *Documents*,

Contacts and speed dials.

2 Press Delete. Before the data is removed, you will be prompted for your lock code.

To start one of the Extras applications, press the button on the communicator keyboard, select an application and press **Select**.

Calculator

Write the calculation in the input field with the keyboard. Press Enter to perform the calculation. Previous calculations are shown in the list above the input field.

Clock

The Clock shows the time and date in your home city and country, as well as in several other cities and countries throughout the world. The time and date can be adjusted in the Clock settings.

Alarm clock

Press **Alarm clock** in the Clock main view to access the Alarm clock. Adjust the alarm time with the **+** and **–** command buttons. The alarm occurs according to the home city time.

Composer

The Composer enables you to compose ringing tones. To compose a new tune, press **Compose**.

Voice recorder

The Voice recorder enables you to record telephone conversations, voicememos, and other sounds. You can also listen to your recordings and other sound files.

Help

Press the button on the communicator keyboard. The application icon in the indicator area on the left side of the screen remains in view, reminding you of the application from where the help was launched.

To view the help topics for the current application, press **Application help**.

To view general help topics about the communicator, press **General help**.

To exit the help, press **Close**.

Phone

To switch on the phone:

1 Close the device cover, if it is open.

2 Press and hold to switch on the phone.

If you are prompted for the PIN code, enter your PIN code, which is provided with the SIM card, and press the key directly under the **OK** text on the display.

As with any other radio transmitting device, do not touch the antenna unnecessarily when the phone is switched on. Contact with the antenna affects call quality and may cause the phone to operate at a higher power level than otherwise needed.

To make and answer calls

To make a call, enter the area code and the phone number, then press ”CALL”.

To answer a call press ”CALL”.

To end a call press ”END CALL” .

IMPORTANT! Do not switch on the phone when wireless phone use is prohibited or when it may cause interference or danger.

Keys

— Switches between different operating environments.

— Scroll through menus, submenus or settings. When a call is active, pressing the scroll keys adjusts the volume level. 0 ... 9

— The number and alphabet keys. To call your voice mailbox, press and hold **1**.

— Used for special purposes in certain functions.

— The function of these two selection keys depends on the text

shown on the bottom line of the display.

Accessories guide

The Nokia 9110 Communicator accessories have been designed for different users and communication needs. For availability of approved accessories, please check with your local dealer.

Use only batteries, chargers, and accessories approved by the communicator manufacturer for use with this particular communicator model. The use of any other types will invalidate any approval or warranty applying to the communicator, and may be dangerous.

Memory Card

The postage stamp sized Memory Card DTS–4 provides 4 MB of removable storage for the communicator. The memory card increases the available memory for data and software applications. For further information, see chapter 3 “Special features” of the User’s manual.

Note: Keep all memory cards out of small children’s reach.

Headset

The Headset HDC–8 offers private headset audio operation. With the remote control button, which is located in the microphone part of the headset, you can answer and later end a call. The Headset connects directly to the connector at the bottom of the communicator.

Advanced Desktop Stand

The Advanced Desktop Stand DCH–7 enables charging of the battery of the communicator, when the communicator is placed in the stand. The advanced feature of the stand is the easy connection to a computer. The stand also has a slot for charging batteries separately from the communicator. This is especially convenient for charging spare batteries.

To charge the communicator battery with the desktop stand

1 Plug the Performance Travel Charger into the stand.

2 Place the communicator in the desktop stand connector end first.

3 Plug the charger into a mains outlet.

To charge a spare battery with the desktop stand

1 Plug the Performance Travel Charger into the stand.

2 Insert the battery in the second slot the golden contacts first. Push the battery slightly backwards. Ensure that the battery clicks into place.

3 Plug the charger into a mains outlet. Check that the light on the left of the stand is on. The red light indicates charging, and the steady green light indicates that the battery is charged.

4 To remove the battery, reverse the procedure

To connect to a PC

With the communicator in the desktop stand, you can connect to a PC with the RS–232 adapter cable DLR–2.

1 Plug the adapter cable into the connector at the back of the stand.

2 Connect the other end of the cable to the PC.

Note: If the communicator is also charging in the desk stand, the charging of the spare battery will cease until the battery in the communicator is charged.

3 Place the communicator in the desktop stand connector end first.

4 Start the PC Suite for Nokia 9110 Communicator program on the PC.

Convenient data transfer

You can also synchronise data between your communicator and a compatible PC organiser program with a single press of the button. For more information, see the CD–ROM supplied with your communicator.

Advanced HF Car Kit

The Advanced HF Car Kit CARK–99 offers a convenient handsfree option for using the communicator in a car. The handsfree microphone and external loudspeaker are always on when the communicator is placed in its holder. The car kit provides automatic charging and improves network reception for your communicator. Battery charging times are the same as those for the charger ACP–9. The car kit must be installed by qualified personnel.

Note: For correct button operation, the ACP–9 charger must be connected to the desk stand.

To place the communicator in the holder

1 Close the cover of the communicator and turn the antenna to a closed position.

2 Insert the communicator in the car kit holder connector end first.

3 In order not to damage the connectors, press the communicator down gently until it is securely held by the locking mechanism.

Handset Kit

The optional Handset Kit HSU–1 is a simple handset with no display or keypad.

It provides privacy for conversation and comfort in a car environment while your communicator is connected to the car antenna for better reception. However, do not use the handset while in motion.

To make a call with the car kit

1 Key in the desired number with the keypad.

2 Press . For a private call, lift the handset if installed.

To answer a call

1 Press , or, if the handset is installed, lift the handset.

If you set the Automatic answer feature on in the Car profile, the communicator will automatically answer incoming calls.

To switch from handset operation to handsfree operation

Press the **Options** selection key once and replace the handset in 5 seconds. If you do not press **Options** before replacing the handset, the call will end.

To end a call

Press , or, if the handset is installed, replace the handset.

To connect to a computer

With the RS–232 adapter cable DLR–2 you can connect the communicator to a laptop computer for fax modem use or PC Suite operation.

1 Close the device cover and place the communicator securely in the car kit holder.

2 Insert the plug of the adapter cable into the connector of the holder. The connector is located at the bottom of the holder.

Note: The car kit does not include an antenna. Ask your car kit dealer for available products.

3 Connect the other end of the adapter cable to the serial port of the computer.

4 Start the necessary application on the computer. If you want to use the communicator as a fax modem, see chapter 11 “System: Fax modem” of the User’s manual.

Ignition sense

The ignition sense feature allows the communicator to be automatically switched on or off whenever the communicator is in the charging holder and the vehicle is started or switched off. This prevents the communicator from draining the car battery, if accidentally left on for a long period of time. If installed, the ignition sense is always available. If you do not wish to enable the ignition sense, ask your dealer to leave it uninstalled.

When the ignition is turned off, the message *Phone will power off, if not used* is displayed. The communicator will be switched off after 15 seconds unless

you press any key or take the communicator from the holder during this time.

Car radio mute

This feature mutes the car radio during a phone call, if supported by the car radio. Ask your dealer to connect the car radio mute during installation.

Antenna motor control

If installed, this feature will activate the electrical motor of the mobile antenna.

Carrying Case

The convenient Carrying Case (CBR–4, CBR–5) protects the communicator wherever you are, and keeps the communicator always at hand.

Mobile Charger

The Mobile Charger LCH–9 provides an easy and convenient way to charge the communicator battery in a vehicle. It is suitable for most vehicles' cigarette lighter sockets. Plug the lead from the Mobile Charger into the bottom connector of the communicator.

Other available accessories

High Power Battery BLN–3 — This is a powerful slim Lithium–ion battery. It provides the same capacity as the battery supplied with your communicator.

RS–232 Adapter Cable DLR–2 — The cable provides a convenient way to connect your communicator to a PC or to a printer.

Performance Travel Charger ACP–9 — This charger is a lightweight and durable charger which functions over most mains voltages. The communicator can be operated normally during charging. Charging time is typically 2 hours, depending on how drained the battery is. To charge the communicator, connect the charger lead to the bottom connector of the communicator and plug the charger into the mains.

Upgrade HF Car Kit — The Upgrade HF Car Kit CARK–102 offers an easy way to upgrade from CARK–74, which is compatible with the Nokia 8100 series and 3110 wireless phones, to CARK–99.

Note: Use only the ACP–9 and LCH–9 chargers with the communicator.

Nokia Wireless Data Forum

Nokia Wireless Data Forum is a Web service that offers support for Nokia 9110 Communicator and the other Nokia wireless data products. The Web site contains documents, drivers, manuals, information on compatibility issues, etc.

The main focus of the Nokia Wireless Data Forum is to serve corporate and business users. It provides, for example, references on solutions that have been tailored for the needs of corporate customers.

Nokia Wireless Data Forum can be found at http://www.forum.nokia.com
Club Nokia Careline

You can contact the Club Nokia Careline for help or questions you may have concerning the Nokia 9110 Communicator and its functions.

Free support is available for Club Nokia Careline members for the first membership year. Before calling you have to register with Club Nokia either via http://club.nokia.com or by sending the invitation, enclosed in the sales package, to Club Nokia.

Please look up the serial number of your device before calling. It is visible when you remove the battery from the device. The serial number appears on the sticker attached to the device. You also need to note your Club Nokia membership number.

The Club Nokia Careline is available Monday–Friday 9.00 am to 5.30 pm local time, but not on national holidays. Nokia reserves the right to changes without prior notice.

Club Nokia Careline phone numbers

Non–members

If you are not a member of Club Nokia you can call +32 70 23 30 58 (charge for international call) from all the countries mentioned above.

You can also contact your dealer when you have a problem.

Country Careline number Tariff per minute

Austria 0660 7420 charge for local call

Belgium 0800 965 76 charge for local call

Czech Republic +3270 233 412 charge for international call

Denmark 8001 5437 charge for local call

Finland 0800 113 275 charge for local call

France 0800 901 953 charge for local call

Germany 0130 860 355 charge for local call

Greece 00800 3222 303 charge for local call

Hungary 00800 125 31 charge for local call

Ireland 1800 55 32 75 charge for local call

Italy 1677 803 06 charge for local call

Luxembourg 0800 2493 charge for local call

Netherlands 0602 248 98 charge for local call

Norway 8001 1475 charge for local call

Poland 00800 3211 231 charge for local call

Portugal 0505 329 930 charge for local call

Spain 9009 832 30 charge for local call

Sweden 0207 945 38 charge for local call

Switzerland 0800 557 749 charge for local call

Turkey 00800 3291 303 charge for local call

UK 0800 898 397 charge for local call

Care and maintenance

Your Nokia 9110 Communicator is a product of superior design and craftsmanship and should be treated with care. The suggestions below will help you fulfil any warranty obligations and enjoy this product for many years.

When using your communicator, battery, charger OR any accessory: Keep it and all its parts and accessories out of small children's reach. Keep it dry. Precipitation, humidity and liquids contain minerals that will corrode electronic circuits.

Do not use or store it in dusty, dirty areas. Its moving parts can be damaged.

Do not store it in hot areas. High temperatures can shorten the life of electronic devices, damage batteries, and warp or melt certain plastics.

Do not store it in cold areas. When the communicator warms up (to its normal temperature), moisture can form inside the communicator, which may damage electronic circuit boards.

Do not attempt to open it. Non–expert handling of the device may damage it. Do not drop, knock or shake it. Rough handling can break internal circuit boards.

Do not use harsh chemicals, cleaning solvents, or strong detergents to clean it. Wipe it with a soft cloth slightly dampened in a mild soap–and–water solution.

Do not paint it. Paint can clog the device's moving parts and prevent proper operation.

Use only the supplied or an approved replacement antenna. Unauthorised antennas, modifications or attachments could damage the communicator and may violate regulations governing radio devices.

If the communicator, battery, charger or any accessory is not working properly, take it to your nearest qualified service facility. The personnel there will assist you and, if necessary, arrange for service.

Important safety information

Traffic safety

Do not use a communicator while driving a vehicle. If using a communicator, park the vehicle first. Always secure the communicator in its holder; do not place the communicator on the passenger seat or where it can break loose in a collision or sudden stop.

The use of an alert device to operate a vehicle’s lights or horn on public roads is not permitted.

Remember, road safety always comes first!

Operating environment

Remember to follow any special regulations in force in any area and alwaysswitch off the phone of your communicator whenever it is forbidden to use it, or when it may cause interference or danger.

When connecting the communicator or any accessory to another device, read its user’s guide for detailed safety instructions. Do not connect incompatible products.

As with other mobile radio transmitting equipment, users are advised that for the satisfactory operation of the equipment and for the safety of personnel, it is recommended that the equipment should only be used in the normal operating position (held to your ear with the antenna pointing over your shoulder).

Do not point the infrared beam at anyone’s eye or allow it to interfere with other infrared devices.

Electronic devices

Most modern electronic equipment is shielded from radio frequency (RF) signals. However, certain electronic equipment may not be shielded against the RF signals from your communicator.

Pacemakers: Pacemaker manufacturers recommend that a minimum separation of 20 cm (6 inches) be maintained between a handheld wireless phone and a pacemaker to avoid potential interference with the pacemaker.

These recommendations are consistent with the independent research by and recommendations of Wireless Technology Research. Persons with pacemakers:

Should always keep the communicator more than 20 cm (6 inches) from their pacemaker when the phone is switched on;

Should not carry the communicator in a breast pocket;

Should use the ear opposite the pacemaker to minimise the potential for interference.

If you have any reason to suspect that interference is taking place, switch off the phone of your communicator immediately.

Hearing aids: Some digital wireless phones may interfere with some hearing aids.

In the event of such interference, you may want to consult your service provider.

Other medical devices: Operation of any radio transmitting equipment,including communicators, may interfere with the functionality of inadequately protected medical devices. Consult a physician or the manufacturer of the medical device to determine if they are adequately shielded from external RF energy or if you have any questions. Switch off the phone of your communicator in health care facilities when any regulations posted in these areas instruct you to do so. Hospitals or health care facilities may be using equipment that could be sensitive to external RF energy.

Vehicles: RF signals may affect improperly installed or inadequately shielded electronic systems in motor vehicles (e.g. electronic fuel injection systems, electronic anti–skid (anti–lock) braking systems, electronic speed control systems, air bag systems). Check with the manufacturer or its representative regarding your vehicle. You should also consult the manufacturer of any equipment that has been added to your vehicle.

Posted facilities: Switch off the phone of your communicator in any facility where posted notices so require.

Potentially explosive atmospheres Switch off the phone of your communicator when in any area with a potentiallyexplosive atmosphere and obey all signs and instructions. Sparks in such areas could cause an explosion or fire resulting in bodily injury or even death.

Users are advised to switch off the phone when at a refuelling point (service station). Users are reminded of the need to observe restrictions on the use of radio equipment in fuel depots (fuel storage and distribution areas), chemical plants or where blasting operations are in progress.

Areas with a potentially explosive atmosphere are often but not always clearly marked. They include below deck on boats; chemical transfer or storage facilities; vehicles using liquified petroleum gas (such as propane or butane); areas where the air contains chemicals or particles, such as grain, dust or metal powders; and any other area where you would normally be advised to turn off your vehicle engine.

Vehicles

Only qualified personnel should service the communicator, or install the communicator in a vehicle. Faulty installation or service may be dangerous and may invalidate any warranty which may apply to the unit.

Check regularly that all wireless phone equipment in your vehicle is mounted and operating properly.

Do not store or carry flammable liquids, gases or explosive materials in the same compartment as the communicator, its parts or accessories.

For vehicles equipped with an air bag, remember that an air bag inflates with great force. Do not place objects, including both installed or portable wireless

equipment in the area over the air bag or in the air bag deployment area. If in–vehicle wireless equipment is improperly installed and the air bag inflates, serious injury could result.

Switch off the phone of your communicator before boarding an aircraft. The use of wireless telephones in an aircraft may be dangerous to the operation of the aircraft, disrupt the wireless telephone network and may be illegal. Failure to observe these instructions may lead to suspension or denial of telephone services to the offender, or legal action or both.

Emergency calls

IMPORTANT!

The Nokia 9110 Communicator, like any wireless phone, operates using radio signals, wireless and landline networks as well as user–programmed functions which cannot guarantee connection in all conditions. Therefore you should never rely solely upon any wireless phone for essential communications (e.g. medical emergencies).

Remember, to make or receive any calls the phone must be switched on and in a service area with adequate signal strength. Emergency calls may not be possible on all wireless phone networks or when certain network services and/ or phone features are in use. Check with local service providers.

To make an emergency call

1 If the device cover is open, close the cover.

2 If the phone is not on, switch it on (press the key). Some networks may require that a valid SIM card is properly inserted in the communicator.

3 Press and hold the key for several seconds to ready the phone for calls and to end possible active data or fax calls.

4 Key in the emergency number for your present location (e.g. 112 or other official emergency number). Emergency numbers vary by location.

5 Press the key.

If certain features are in use (call barring, fixed dialling, closed user group, system lock, etc.), you may first need to turn those features off before you can make an emergency call. Consult the User’s manual and your local cellular service provider.

When making an emergency call, remember to give all the necessary information as accurately as possible. Remember that your communicator may be the only means of communication at the scene of an accident – do not cut off the call until given permission to do so.

To use this guide

The wireless phone described in this guide is approved for use in the GSMnetworks.

A number of features included in this manual are called network services.

They are special services provided by wireless service providers. Before you cantake advantage of any of these network services, you must subscribe to theservice(s) you require from your home service provider and obtain instructionsfor their use. You can then activate these functions as described in this manual. The manual activation commands for various services are not presented in this manual (e.g. using the and characters for activating or deactivating services). The Nokia 9110 Communicator is, nevertheless, capable of handling commands given in that form. For these commands, please consult with your service providers.

WARNING! This apparatus is intended for use when supplied with power from a Lithium–ion battery and chargers ACP–9E, ACP–9X and ACP–9A. Other usage will invalidate any approval given to this apparatus and may be dangerous.

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Chapter 13

Accessories

AMENDMENT RECORD SHEET

Amendment Number	Date	Inserted By	Comments
	02/99		Original

CONTENTS

Units and Accessories

All RAE–2N accessories are non–serviceable.

Table 1. List of Units and Accessories

Name of unit or accessory	Type code	Notes
Battery	BLN–3	1030 mAh, Li–Ion
Performanace Travel Charger	ACP–9	
Headset	HDC–8	
Advanced Deskstop Stand	DCH–7	Includes synchronization button for PC connection
RS–232 Adapter Cable	DLR–2	
Carrying Case	CBR–4	
Memory Card	DTS–4	Removable memory card. MMC
Advanced HF Car Kit	CARK–99	
Privacy Handset	HSU–1	
Mobile Charger	LCH–9	
Upgrade HF Car Kit	CARK–102	

Headset HDC-8

Connect the HDC–8 to the bottom connector of phone, and it is ready to use. The push button at microphone part can be used for answering and ending the call.

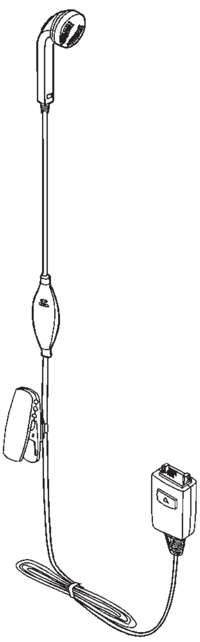


Figure 1. HDC–8

Technical Summary

HDC–8 headset contains a microphone, a speaker, EMI–components and CONTROL button . Headset will be connected straight to the bottom connector of the phone.

Headset can be used also with the car kit.

List of Modules

Headset HDC–8

Desktop Charger DCH–7

Desktop charger DCH–7 is designed for the charging of the RAE–2 PDA and a spare battery.

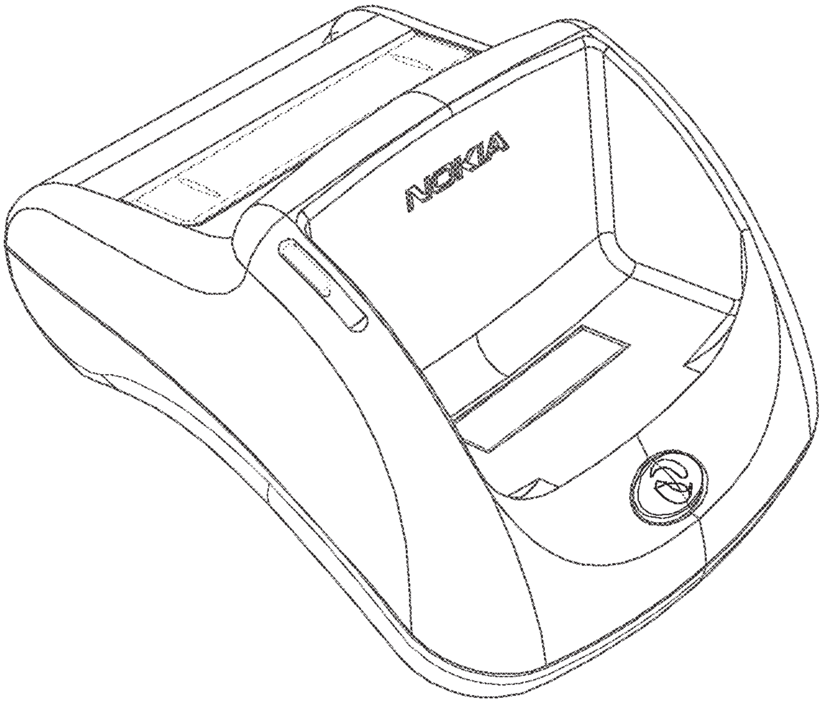


Figure 2. DCH–7 Desk Stand

Technical Summary

The desktop charger DCH–7 is a two–slot stand designed to be placed on a desk–top. The front slot holds and charges the phone, and the rear slot holds and charges a spare battery.

The desk stand includes red and green LEDs to show the status of the spare battery charging in the rear slot.

The desk stand supports charging of 4.1V and 4.2V lithium–ion batteries.

The desk stand is powered by an external ACP–9A/E/U/X performance travel charger. When a RAE–2 is placed in the front slot it is charged at the same rate as if the external charger was connected directly to the phone. When a spare battery is placed in the rear slot, it is charged at a slower rate. Charging of the spare battery is delayed until the phone has finished charging.

The front slot provides data connection between the deskstand connected PC and the RAE–2. The host PC is connected by Nokia data cable to the rear of the desk stand. The PC must have the Nokia ”Share” software running for the data transfer to the PC to be successful.

Rear Connector View Desk Stand

The rear connector allows for the Nokia PC data cable to be connected to the Spock whilst in the desk stand. The cable is connected to the rear of the desk stand and the desk stand provides routing of the signals to the Spock phone.

The rear connector provides for connection of the charger to the desk stand.

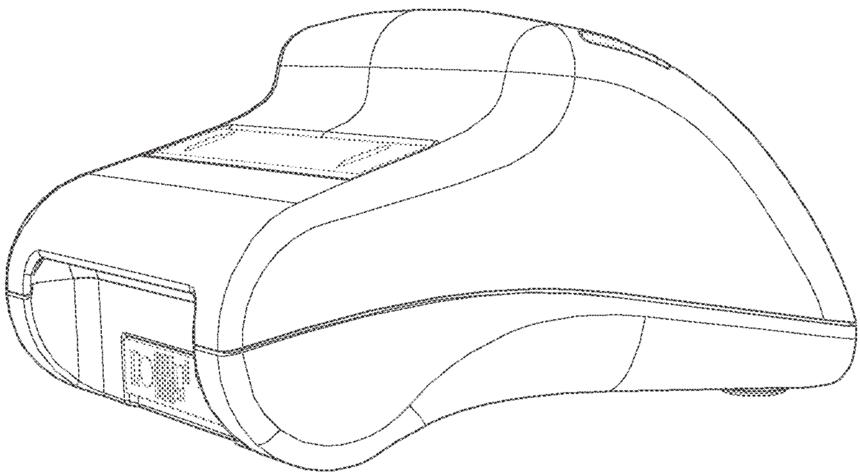


Figure 3. DCH–7 Deskstand

The desk stand provides a convenient push button, called a ”Share” button to initiated the phone to PC data synchronization. The data transfer from the phone to the PC is then achieved via the phone serial data link [Fbus]. The Nokia Data cable is required for connection of the desk stand to the PC.

Interconnection Diagram

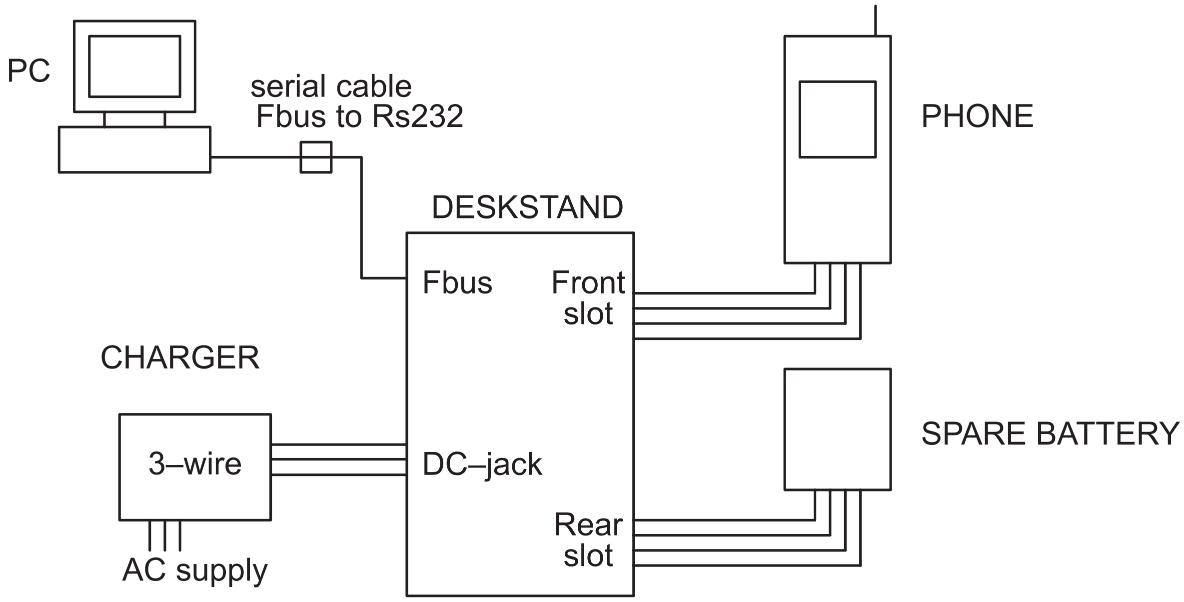
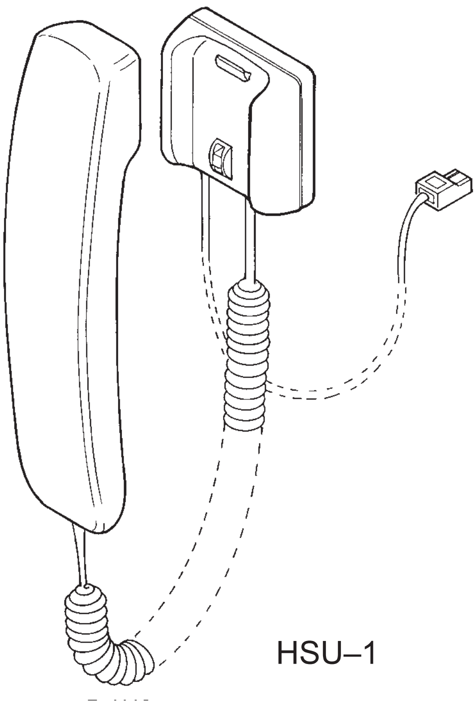


Figure 4. Interconnection Diagram

Handset HSU–1

The main function of the HSU–1 Audio Handset is to form an electroacoustic interface between the user and the phone environment.



HSU–1

Technical Summary

The HSU–1 Audio Handset consists of handset with coil cord and of cradle. In the handset there is earphone and microphone with corresponding amplifiers. There is also a simply interface for controlling these functions. Electronics consist of DG–1 handset module. Mechanical dimensions are small and mechanics consists of A–cover, B– cover and coil cord with the cradle. The HSU–1 Audio Handset has a volume potentiometer.

Use of Handset

The HSU–1 Audio Handset is designed to be a dummy handset with no display and no keyboard. Its use is to form an electroacouistical connection between the user and DCT – environment. When not in use the handset is on the cradle. During the use the handset is lifted from the cradle and audio paths are opened.

Memory Card MMC DTS–4

The PDA includes a synchronous serial interface that is compatible with the Multimedia Card Bus (MMC) Protocol. The MMC is a changeable Flash or ROM memory card with variable memory size. The MMC connector is located on the BS8 Module..

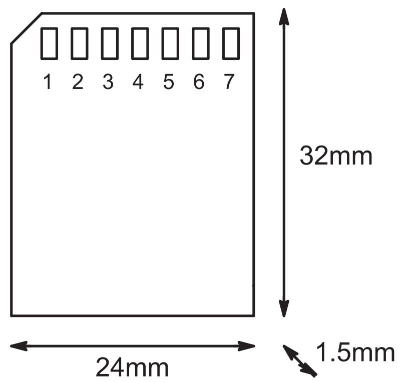
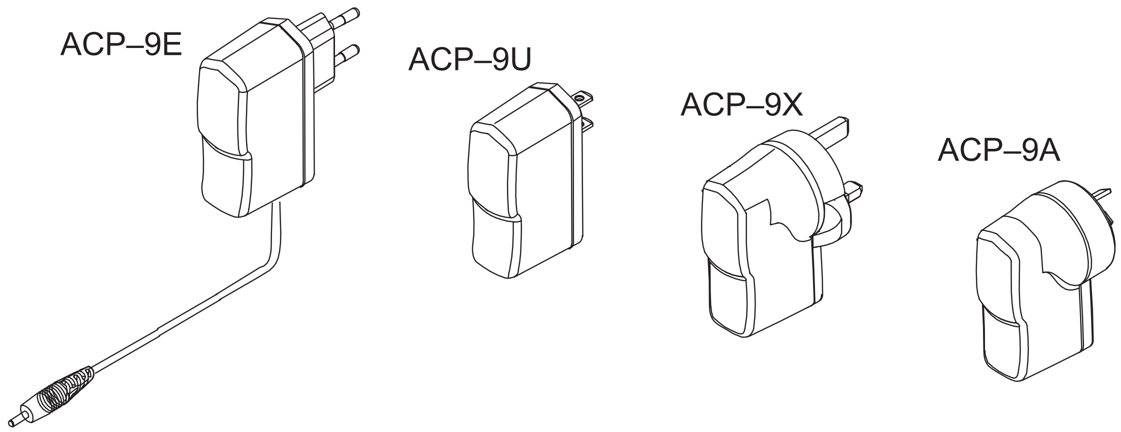


Figure 5. DTS–4 Dimensions

Fast Travel Charger ACP–9

Operating within the voltage range 90 V...264 V AC (50 Hz...60 Hz), the Fast Travel Charger is practically current independent in normal office and household use. Like the standard charger, it is compatible with all battery options and is available for different wall sockets.

The Fast Travel Charger can also be used with basic stand and desktop stand.



Product Codes

Fast Travel Charger (Euro plug) 90–264 Vac	ACP–9E	0675149
Fast Travel Charger (US plug) 90–264 Vac	ACP–9U	0675151
Fast Travel Charger (UK plug) 90–264 Vac	ACP–9X	0675150
Fast Travel Charger (Australia) 90–264 Vac	ACP–9A	0675152
Output cable PCC–1 (supplied with ACP–9):		*0730076*

Specification

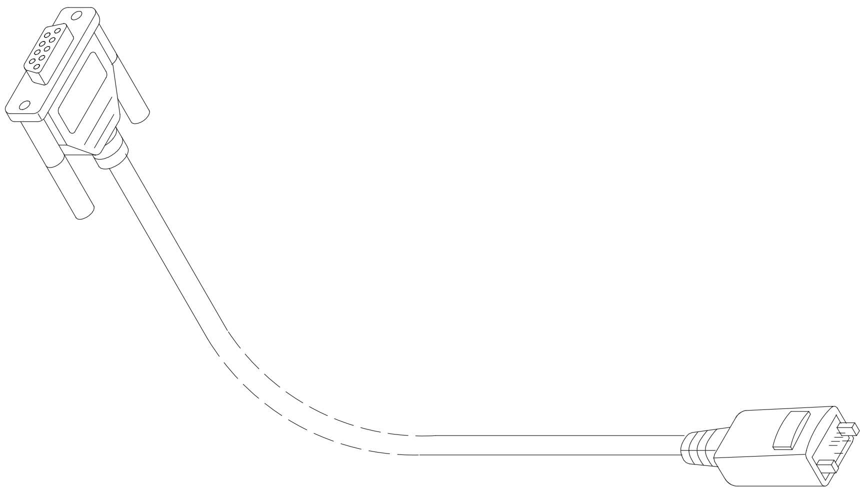
Output connectors: *3.5 mm DC plug, 3–pole (+, –, control)*

Protection: *output current limiting, max. 850 mA*
output voltage limiting, max. 9.3 V (unloaded)

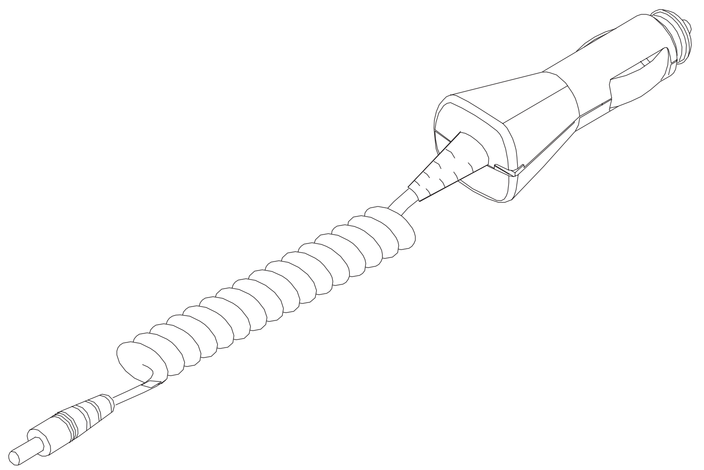
Output voltage/current (typ): *8.4 V / 800 mA*

RS232 Adapter Cable DLR–2 (073077)

Purpose	Connects an external computer with RAE–1N (via PAR–1) see below
Cable length	950mm ± 25 mm (3 wire, ⌀3.5 mm)
D connector	D9 connector female
Stereo connector	Stereo plug (⌀2.5 mm) with ⌀3.5 mm strain relief



Cigarette Lighter Charger LCH–9 (0675005)



Purpose	charging adapter for car environment; input voltage 9...32 V
Charger type	Switching mode power supply
Operation	quick charge (< 0.5–2.5 h), trickle charge
Protection	input fused, output current limit
Connectors	output: 3.8 mm standard DC plug; input: D 21 / 23 mm
Weight	<120 g
Cable	2 m curly cable

NOTE! The current version of LCH–2 does not indicate (led illumination) in a correct way what is the status of the charging with Li batteries.

For quick car installation, the user can utilise the Cigarette Lighter Charger LCH–2, Power Adapter PAR–1, and RS232 serial cable DLR–1 Mobile

Holder MBR–1 cannot be used in this context.

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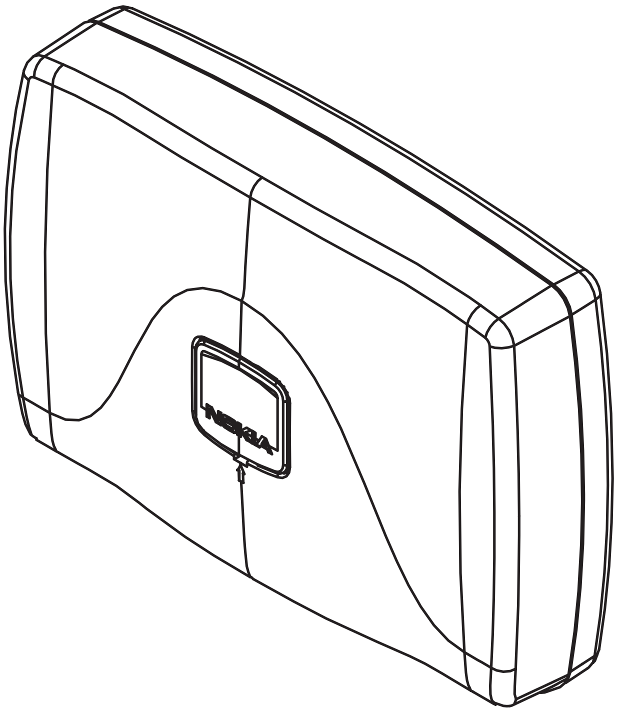
HFU–2

CONTENTS

Introduction

The HFU–2 is a handsfree unit for DCT3 compatible handportable phones. It provides rapid charging for the phone, a possibility to use HF–operation and connections to the data–card and handset unit. The HF box can be connected directly to the Mobile holder MCC–1 via the external cable.



Technical Summary

The HFU–2 has connections to car battery, car ignition sense, car radio muting, antenna motor control, data–card, handset HSU–1, external speaker and microphone. The unit has a System–connector that provides an interface to the Mobile holder MCC–1 via the external cable.

The unit consists of a rapid charger, HF–microphone– and speaker amplifiers, interface to handset, – datacard and –phone, voltage regulators and control circuit (microprocessor).

The HFU–2 is always connected to the car battery. To save the car battery, HFU–2 goes in to the sleep mode if the car is not running and/or the phone is not connected.

List of Modules

Name of module	Type code	Material code	Notes
HF unit	HFU–2	0694049	Advanced handsfree unit
HF module	ED2	0200948	ED2 Advanced hadsfree module
Assembly parts	MHFU–2	0261602	Mechanical Parts

Operation

Phone not connected (sleep mode):

When the phone is not connected the current consumption of the device has been minimized. The switching mode power supply (SMPS) and audio circuits has been turned off. HFU–2 is only waiting a phone to be connected.

Phone connected (active mode):

When the phone is connected to the HFU–2 it goes into the active mode. In the active mode the device provides charging current to the phone. It also can provide hands free call option using the external speaker and the external microphone or micspeaker unit. If more private call wants to be made, the phone itself can be used as a handset without losing the external antenna connection or with handset (option).

The phone controls all functions of HFU–2. In the active mode the HFU–2 sends all state transitions to phone via mbus.

HFU–2 also provides car radio mute function during call.

HFU–2 can control the mobile antenna motor if it is installed to the car.

Supply Voltage and Power Consumption

Conn. / pin	Line Symbol	Minimum	Typical / Nominal	Maximum	Unit / Notes
X300 / 6	GND		0		VDC
X300 / 1	VB	8.0		16	VDC (working)
X300 / 1	VB	10.8	13.5	16	VDC (spec. fulfill)
X300 / 1	VB	0.05	1	2	IDC/A (operating)
X300 / 1	VB	0.2	0.8	1	IDC/mA (sleep mode)

Charging voltage limits within current specifications fulfilled

Conn. / pin	Line Symbol	Minimum	Typical / Nominal	Maximum	Unit / Notes
X200 / 7	GND	0	0	0.1	VDC
X200 / 2	+10VA	9.50	10.0	10.55	VDC
X200 / 2	+10VA		11	200	IDC / mA

Conn. / pin	Line Symbol	Minimum	Typical / Nominal	Maximum	Unit / Notes
X100 / 5,6,11	GND	0	0	0.1	VDC
X100 / 8,9	V_IN	3		8.5	VDC
X100 / 12	VB	8		16	VDC / car battery
X100 / 12	VB			500	IDC / mA

Audio Specifications, electrical

	Minimum	Typical / Nominal	Maximum	Unit / Notes
Max speaker output power at distortion=1%, 1 kHz sine	3.0	3.1		W / Rload = 8 ohm
HF–speaker amplifier gain	27	29	31	dB
PSRR, XEAR line	–60	–68		dB
CMRR, XEAR–SGND to speaker	–50	–55		dB
HF–mic amplifier gain	27	30	33	dB
Mic level at XMIC–SGND, (clipping level)	2000		2800	mVpp
Mic distortion at XMIC–SGND, at Vo = 100 mVrms, 1 kHz		0.15	0.4	%
Noise voltage, HFMIC			5	uVrms psofometric
PSRR, XMIC	–60	–67		dB
Crosstalk XEAR–SGND to XMIC		– 55	– 45	dB / electrical, 1kHz

HFS–12 Audio Specifications, acoustic

	Minimum	Typical / Nominal	Maximum	Unit / Notes
Electroacoustic transfer function (RX) dBPa/1V/0.5m	11	15	19	dBPa / 1V at system connector is theoretical level
Speaker distortion level at XEAR–SGND, d=5%		354		mVrms
HF–speaker: SPL, approximate over 500 ... 3000 Hz	87 –4	89 –2	91 0	dB / 1W / 1m dBPa / 0.5W at 0,5m
Equivalent input noise, XEAR			10	uVrms psofometric
Total noise, HF speaker		200	400	uVrms psofometric

HFM–8 Audio Specifications, acoustic

	Minimum	Typical / Nominal	Maximum	Unit / Notes
Electroacoustic transfer function (TX) dBV/dBPa/0.5m	–28	–24	–20	dBV/–5dBPa/0.5m
Total noise, XMIC–SGND		140	300	uVrms psofometric

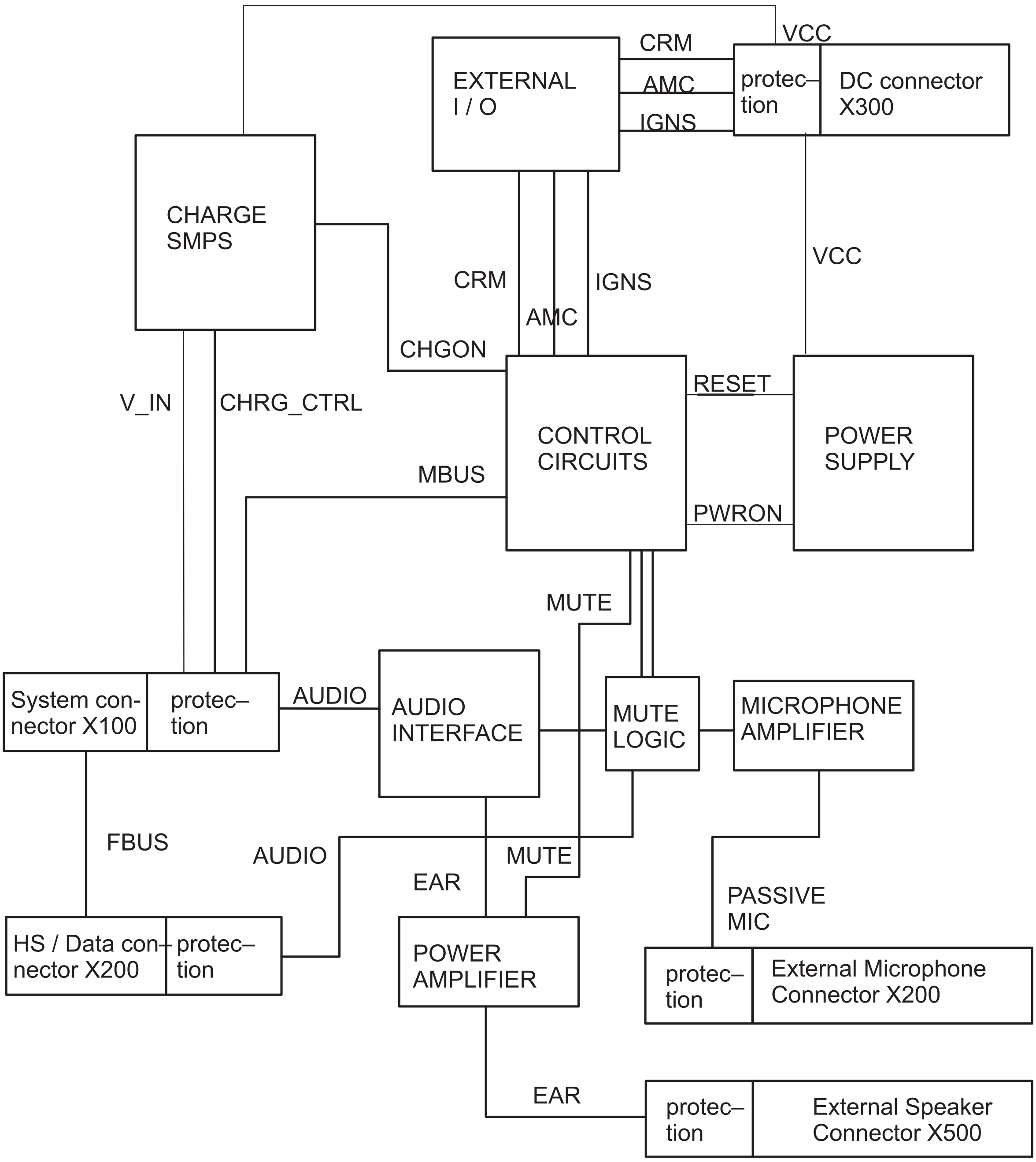
Audio signal levels

Signal name / conn. / pin	Minimum	Typical / Nominal	Maximum	Unit / Notes
XEAR / X100 / 4		80	354	mVrms
SGND / X100 / 3		0		mVrms
XMIC / X100 / 2		60	990	mVrms
HFMIC / X400 / 2		2.0		mVrms
SPEAKER / X500 / 1 & 2		0.75	5	V rms

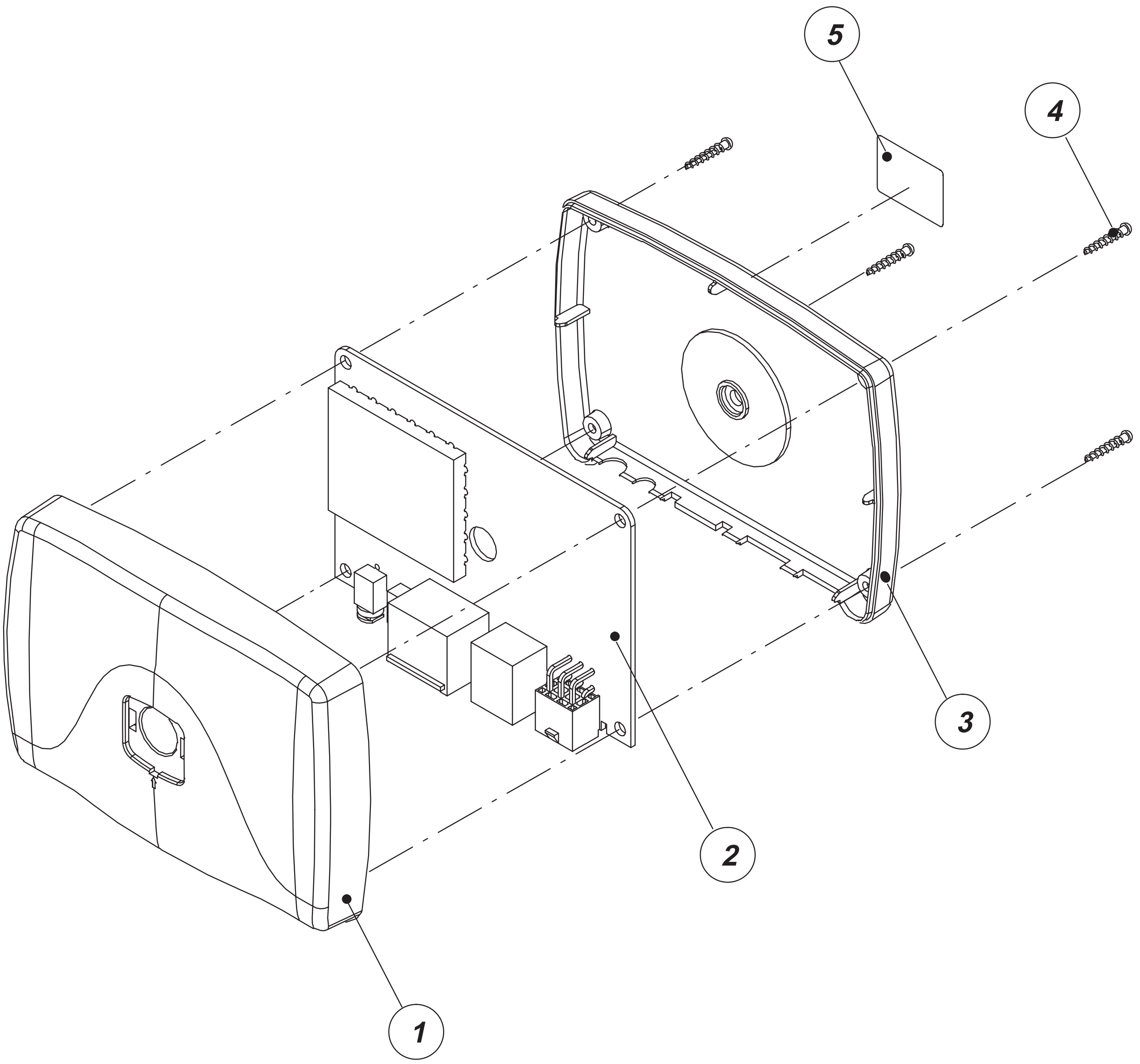
Signals and Connections

Connector Name	Code	Notes	Specifications / Ratings
System connector	X100	Charge, Mbus, Fbus, audio lines, VB	Modular 15 pin.
Handset / Data connector	X200	Mbus, Fbus, Handset audio– lines, Hshook, 10V	Modular 10 pin.
Car connector	X300	+VB, –VB, ign. sense, car radio mute, antenna motor control	2 X 3 Power conn.
HFMIC connector	X400	External microphone	2.5 mm jack
EXT. SPEAKER connector	X500	External speaker	3.2 mm jack

Block Diagram



Exploded View of HFU–2



Parts list of ED2 (EDMS Issue 5.1) Code: 0200948

ITEM	CODE	DESCRIPTION	VALUE	TYPE
R200	1415960	Melf resistor	33.2 k	1 % 0.2 W 0204
R201	1412409	Chip resistor	1.5 k	5 % 0.1 W 0805
R202	1430051	Chip resistor	4.7 k	5 % 0.063 W 0603
R203	1413829	Chip resistor	10	5 % 0.1 W 0805
R204	1413829	Chip resistor	10	5 % 0.1 W 0805
R205	1419007	Chip resistor	0.22	2 % 1210
R206	1413635	Chip resistor	100 k	5 % 0.1 W 0805
R207	1416393	Melf resistor	221 k	1 % 0.2 W 0204
R209	1430001	Chip resistor	100	5 % 0.063 W 0603
R210	1415791	Melf resistor	100	1 % 0.2 W 0204
R211	1413716	Chip resistor	220 k	5 % 0.1 W 0805
R212	1416273	Melf resistor	150 k	1 % 0.2 W 0204
R213	1430065	Chip resistor	10 k	5 % 0.063 W 0603
R214	1430089	Chip resistor	120 k	5 % 0.063 W 0603
R215	1430105	Chip resistor	560 k	5 % 0.063 W 0603
R216	1415664	Melf resistor	27.4 k	1 % 0.2 W 0204
R218	1412328	Chip resistor	820	5 % 0.1 W 0805
R219	1416798	Melf resistor	681	1 % 0.2 W 0204
R222	1410003	Chip resistor	33 k	1 % 0.1 W 0805
R223	1410001	Chip resistor	22 k	1 % 0.1 W 0805
R224	1414283	Chip resistor	100 k	1 % 0.1 W 0805
R225	1414283	Chip resistor	100 k	1 % 0.1 W 0805
R226	1413716	Chip resistor	220 k	5 % 0.1 W 0805
R227	1430051	Chip resistor	4.7 k	5 % 0.063 W 0603
R228	1430087	Chip resistor	100 k	5 % 0.063 W 0603
R233	1430015	Chip resistor	470	5 % 0.063 W 0603
R240	1430001	Chip resistor	100	5 % 0.063 W 0603
R245	1415960	Melf resistor	33.2 k	1 % 0.2 W 0204
R246	1414406	Chip resistor	5.6 k	5 % 0.1 W 0805
R270	1430087	Chip resistor	100 k	5 % 0.063 W 0603
R300	1430071	Chip resistor	22 k	5 % 0.063 W 0603
R301	1430087	Chip resistor	100 k	5 % 0.063 W 0603
R302	1430087	Chip resistor	100 k	5 % 0.063 W 0603
R303	1430071	Chip resistor	22 k	5 % 0.063 W 0603
R304	1412409	Chip resistor	1.5 k	5 % 0.1 W 0805
R306	1430071	Chip resistor	22 k	5 % 0.063 W 0603
R307	1430087	Chip resistor	100 k	5 % 0.063 W 0603
R310	1412261	Chip resistor	100	5 % 0.1 W 0805
R311	1430073	Chip resistor	27 k	5 % 0.063 W 0603
R312	1430073	Chip resistor	27 k	5 % 0.063 W 0603
R313	1430065	Chip resistor	10 k	5 % 0.063 W 0603
R315	1430065	Chip resistor	10 k	5 % 0.063 W 0603
R316	1430051	Chip resistor	4.7 k	5 % 0.063 W 0603

R317	1430087	Chip resistor	100 k	5 % 0.063 W 0603
R319	1430079	Chip resistor	47 k	5 % 0.063 W 0603
R321	1430071	Chip resistor	22 k	5 % 0.063 W 0603
R323	1414536	Chip resistor	200 k	1 % 0.1 W 0805
R324	1410003	Chip resistor	33 k	1 % 0.1 W 0805
R325	1430035	Chip resistor	1.0 k	5 % 0.063 W 0603
R327	1414536	Chip resistor	200 k	1 % 0.1 W 0805
R328	1410003	Chip resistor	33 k	1 % 0.1 W 0805
R331	1430065	Chip resistor	10 k	5 % 0.063 W 0603
R332	1430055	Chip resistor	6.8 k	5 % 0.063 W 0603
R333	1430055	Chip resistor	6.8 k	5 % 0.063 W 0603
R334	1414536	Chip resistor	200 k	1 % 0.1 W 0805
R335	1410003	Chip resistor	33 k	1 % 0.1 W 0805
R336	1430095	Chip resistor	220 k	5 % 0.063 W 0603
R337	1430095	Chip resistor	220 k	5 % 0.063 W 0603
R350	1430035	Chip resistor	1.0 k	5 % 0.063 W 0603
R351	1430065	Chip resistor	10 k	5 % 0.063 W 0603
R352	1430047	Chip resistor	3.3 k	5 % 0.063 W 0603
R353	1430065	Chip resistor	10 k	5 % 0.063 W 0603
R380	1430095	Chip resistor	220 k	5 % 0.063 W 0603
R400	1430043	Chip resistor	2.2 k	5 % 0.063 W 0603
R402	1430073	Chip resistor	27 k	5 % 0.063 W 0603
R403	1415939	Melf resistor	22.1 k	1 % 0.2 W 0204
R404	1430095	Chip resistor	220 k	5 % 0.063 W 0603
R405	1430167	Chip resistor	47	5 % 0.063 W 0603
R406	1430047	Chip resistor	3.3 k	5 % 0.063 W 0603
R407	1430035	Chip resistor	1.0 k	5 % 0.063 W 0603
R408	1415939	Melf resistor	22.1 k	1 % 0.2 W 0204
R409	1430043	Chip resistor	2.2 k	5 % 0.063 W 0603
R410	1430043	Chip resistor	2.2 k	5 % 0.063 W 0603
R411	1415939	Melf resistor	22.1 k	1 % 0.2 W 0204
R412	1415939	Melf resistor	22.1 k	1 % 0.2 W 0204
R415	1415939	Melf resistor	22.1 k	1 % 0.2 W 0204
R416	1415939	Melf resistor	22.1 k	1 % 0.2 W 0204
R417	1430087	Chip resistor	100 k	5 % 0.063 W 0603
R421	1430035	Chip resistor	1.0 k	5 % 0.063 W 0603
R422	1415939	Melf resistor	22.1 k	1 % 0.2 W 0204
R423	1415939	Melf resistor	22.1 k	1 % 0.2 W 0204
R425	1430087	Chip resistor	100 k	5 % 0.063 W 0603
R426	1430142	Chip resistor	4.7	5 % 0.063 W 0603
R427	1430142	Chip resistor	4.7	5 % 0.063 W 0603
R429	1430167	Chip resistor	47	5 % 0.063 W 0603
R430	1430167	Chip resistor	47	5 % 0.063 W 0603
R431	1414533	Chip resistor	56 k	1 % 0.1 W 0805
R432	1415230	Melf resistor	11.0 k	1 % 0.2 W 0204
R433	1414276	Chip resistor	47 k	1 % 0.1 W 0805
R434	1414276	Chip resistor	47 k	1 % 0.1 W 0805

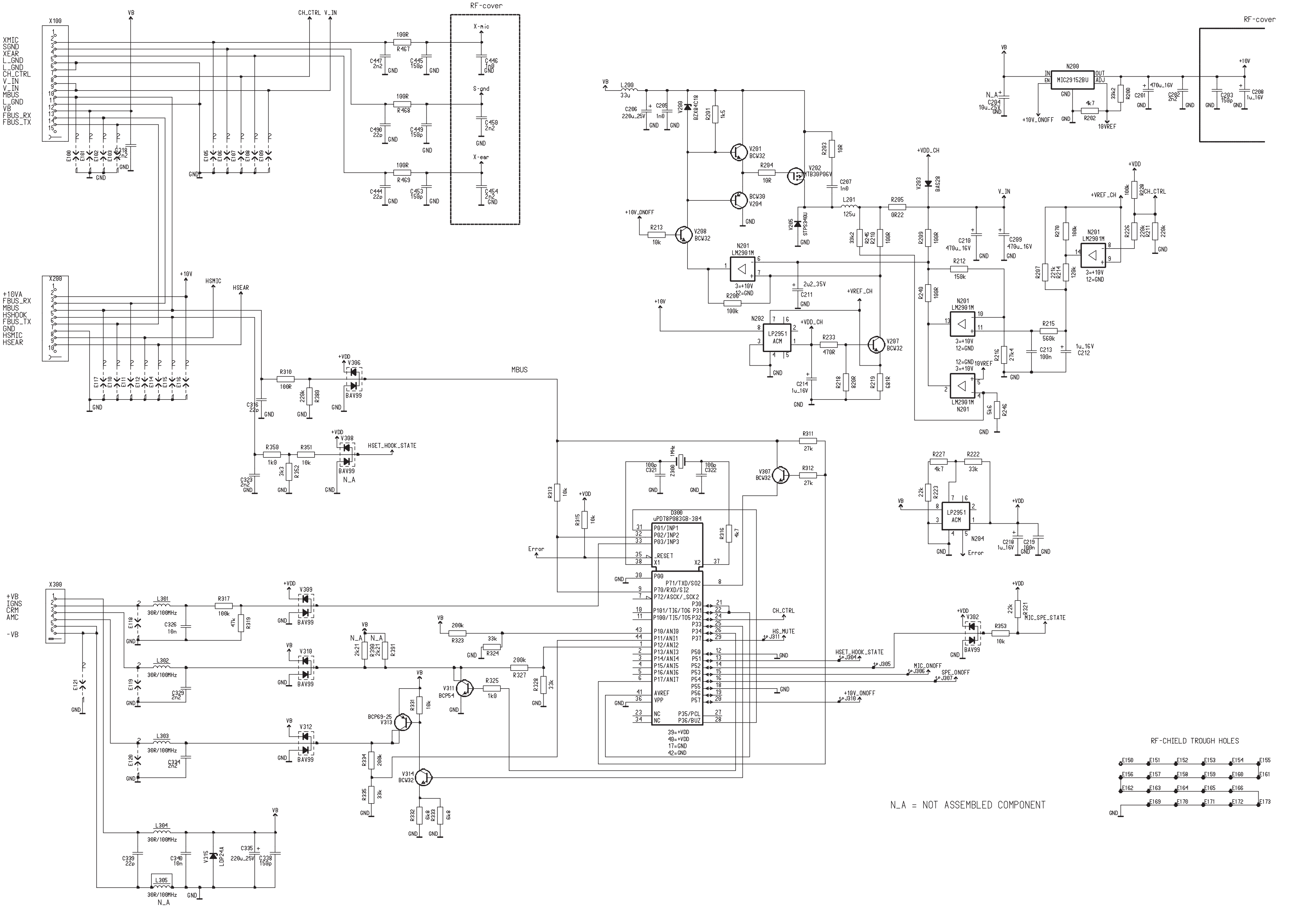
R435	1430095	Chip resistor	220 k	5 % 0.063 W 0603
R436	1430159	Chip resistor	22	5 % 0.063 W 0603
R437	1414276	Chip resistor	47 k	1 % 0.1 W 0805
R438	1430043	Chip resistor	2.2 k	5 % 0.063 W 0603
R439	1415230	Melf resistor	11.0 k	1 % 0.2 W 0204
R440	1416266	Melf resistor	140 k	1 % 0.2 W 0204
R441	1415939	Melf resistor	22.1 k	1 % 0.2 W 0204
R442	1415939	Melf resistor	22.1 k	1 % 0.2 W 0204
R443	1430071	Chip resistor	22 k	5 % 0.063 W 0603
R444	1430167	Chip resistor	47	5 % 0.063 W 0603
R446	1430039	Chip resistor	1.5 k	5 % 0.063 W 0603
R447	1430071	Chip resistor	22 k	5 % 0.063 W 0603
R449	1430043	Chip resistor	2.2 k	5 % 0.063 W 0603
R465	1415939	Melf resistor	22.1 k	1 % 0.2 W 0204
R466	1430055	Chip resistor	6.8 k	5 % 0.063 W 0603
R467	1430001	Chip resistor	100	5 % 0.063 W 0603
R468	1430001	Chip resistor	100	5 % 0.063 W 0603
R469	1430001	Chip resistor	100	5 % 0.063 W 0603
R471	1430053	Chip resistor	5.6 k	5 % 0.063 W 0603
R472	1430053	Chip resistor	5.6 k	5 % 0.063 W 0603
R473	1430053	Chip resistor	5.6 k	5 % 0.063 W 0603
C201	2503072	Electrol. cap.	470 u	20 % 16 V 10x16
C202	2320091	Ceramic cap.	2.2 n	5 % 50 V 0603
C203	2320063	Ceramic cap.	150 p	5 % 50 V 0603
C205	2320083	Ceramic cap.	1.0 n	5 % 50 V 0603
C206	2505261	Electrol. cap.	220 u	20 % 25 V 8.5x11.5
C207	2320083	Ceramic cap.	1.0 n	5 % 50 V 0603
C208	2604209	Tantalum cap.	1.0 u	20 % 16 V 3.2x1.6x1.6
C209	2503072	Electrol. cap.	470 u	20 % 16 V 10x16
C210	2503072	Electrol. cap.	470 u	20 % 16 V 10x16
C211	2604093	Tantalum cap.	2.2 u	20 % 35 V 6.0x3.2x2.5
C212	2604209	Tantalum cap.	1.0 u	20 % 16 V 3.2x1.6x1.6
C213	2310784	Ceramic cap.	100 n	10 % 25 V 0805
C214	2604209	Tantalum cap.	1.0 u	20 % 16 V 3.2x1.6x1.6
C218	2604209	Tantalum cap.	1.0 u	20 % 16 V 3.2x1.6x1.6
C219	2310784	Ceramic cap.	100 n	10 % 25 V 0805
C220	2604209	Tantalum cap.	1.0 u	20 % 16 V 3.2x1.6x1.6
C221	2604209	Tantalum cap.	1.0 u	20 % 16 V 3.2x1.6x1.6
C301	2320091	Ceramic cap.	2.2 n	5 % 50 V 0603
C304	2320091	Ceramic cap.	2.2 n	5 % 50 V 0603
C306	2320091	Ceramic cap.	2.2 n	5 % 50 V 0603
C308	2320091	Ceramic cap.	2.2 n	5 % 50 V 0603
C309	2320063	Ceramic cap.	150 p	5 % 50 V 0603
C316	2320043	Ceramic cap.	22 p	5 % 50 V 0603
C318	2320091	Ceramic cap.	2.2 n	5 % 50 V 0603
C321	2320059	Ceramic cap.	100 p	5 % 50 V 0603
C322	2320059	Ceramic cap.	100 p	5 % 50 V 0603

C323	2320091	Ceramic cap.	2.2 n	5 % 50 V 0603
C326	2320107	Ceramic cap.	10 n	5 % 50 V 0603
C329	2320091	Ceramic cap.	2.2 n	5 % 50 V 0603
C334	2320091	Ceramic cap.	2.2 n	5 % 50 V 0603
C335	2505261	Electrol. cap.	220 u	20 % 25 V 8.5x11.5
C338	2320063	Ceramic cap.	150 p	5 % 50 V 0603
C339	2320043	Ceramic cap.	22 p	5 % 50 V 0603
C340	2320107	Ceramic cap.	10 n	5 % 50 V 0603
C400	2320069	Ceramic cap.	270 p	5 % 50 V 0603
C402	2320079	Ceramic cap.	680 p	5 % 50 V 0603
C403	2320063	Ceramic cap.	150 p	5 % 50 V 0603
C404	2320043	Ceramic cap.	22 p	5 % 50 V 0603
C405	2320091	Ceramic cap.	2.2 n	5 % 50 V 0603
C406	2320091	Ceramic cap.	2.2 n	5 % 50 V 0603
C407	2320083	Ceramic cap.	1.0 n	5 % 50 V 0603
C408	2320063	Ceramic cap.	150 p	5 % 50 V 0603
C409	2320063	Ceramic cap.	150 p	5 % 50 V 0603
C410	2320043	Ceramic cap.	22 p	5 % 50 V 0603
C412	2604209	Tantalum cap.	1.0 u	20 % 16 V 3.2x1.6x1.6
C413	2320091	Ceramic cap.	2.2 n	5 % 50 V 0603
C414	2320107	Ceramic cap.	10 n	5 % 50 V 0603
C415	2604209	Tantalum cap.	1.0 u	20 % 16 V 3.2x1.6x1.6
C416	2320063	Ceramic cap.	150 p	5 % 50 V 0603
C417	2320107	Ceramic cap.	10 n	5 % 50 V 0603
C418	2310784	Ceramic cap.	100 n	10 % 25 V 0805
C419	2310784	Ceramic cap.	100 n	10 % 25 V 0805
C420	2320083	Ceramic cap.	1.0 n	5 % 50 V 0603
C421	2604209	Tantalum cap.	1.0 u	20 % 16 V 3.2x1.6x1.6
C422	2320083	Ceramic cap.	1.0 n	5 % 50 V 0603
C423	2320107	Ceramic cap.	10 n	5 % 50 V 0603
C425	2320083	Ceramic cap.	1.0 n	5 % 50 V 0603
C427	2320043	Ceramic cap.	22 p	5 % 50 V 0603
C428	2604209	Tantalum cap.	1.0 u	20 % 16 V 3.2x1.6x1.6
C429	2310784	Ceramic cap.	100 n	10 % 25 V 0805
C430	2320063	Ceramic cap.	150 p	5 % 50 V 0603
C431	2320063	Ceramic cap.	150 p	5 % 50 V 0603
C432	2310784	Ceramic cap.	100 n	10 % 25 V 0805
C433	2320063	Ceramic cap.	150 p	5 % 50 V 0603
C434	2320063	Ceramic cap.	150 p	5 % 50 V 0603
C435	2310791	Ceramic cap.	33 n	20 % 50 V 0805
C436	2320043	Ceramic cap.	22 p	5 % 50 V 0603
C437	2320091	Ceramic cap.	2.2 n	5 % 50 V 0603
C438	2320091	Ceramic cap.	2.2 n	5 % 50 V 0603
C439	2320091	Ceramic cap.	2.2 n	5 % 50 V 0603
C440	2320043	Ceramic cap.	22 p	5 % 50 V 0603
C441	2320091	Ceramic cap.	2.2 n	5 % 50 V 0603
C442	2320091	Ceramic cap.	2.2 n	5 % 50 V 0603

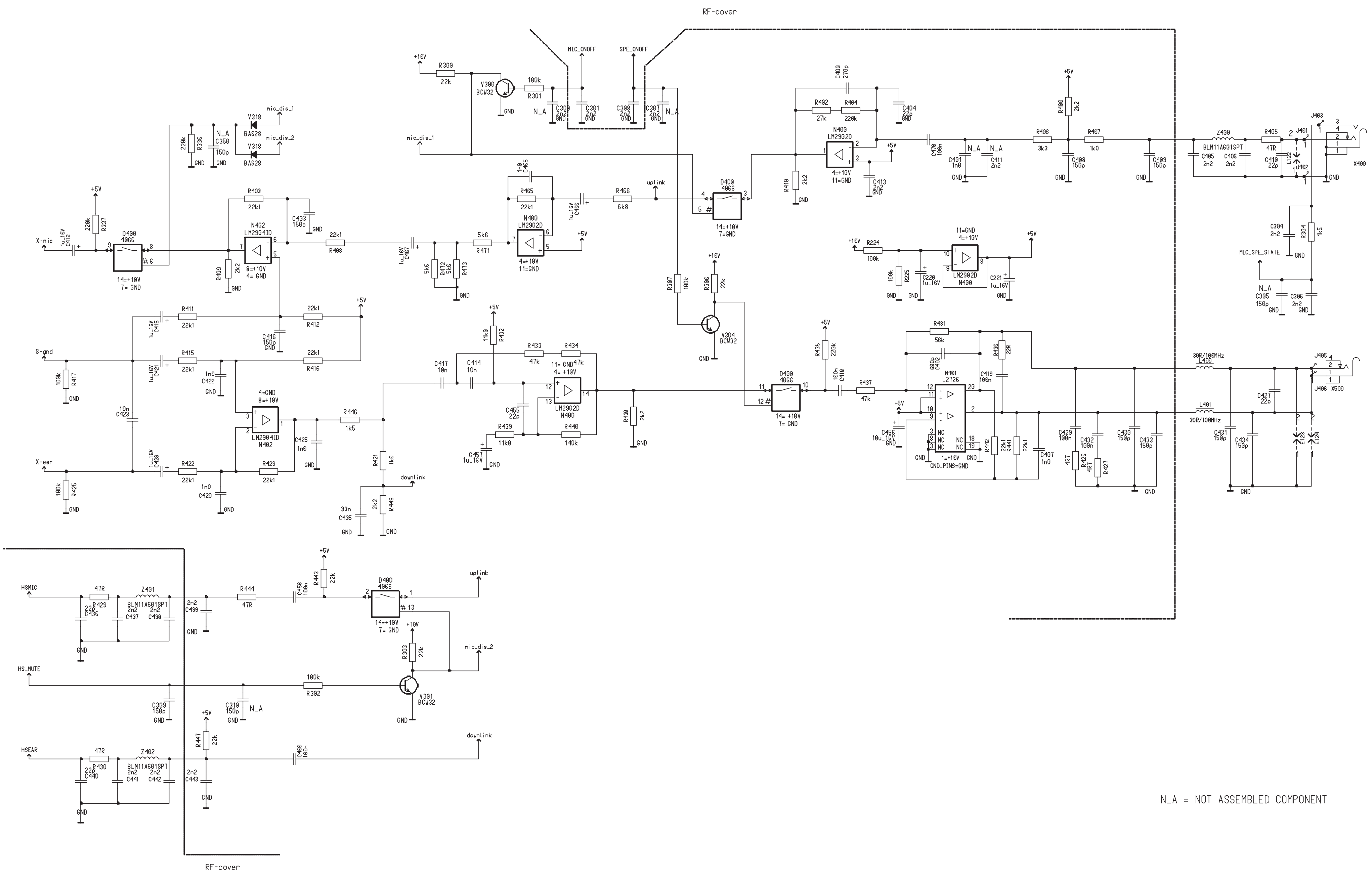
C443	2320091	Ceramic cap.	2.2 n	5 % 50 V 0603
C444	2320043	Ceramic cap.	22 p	5 % 50 V 0603
C445	2320063	Ceramic cap.	150 p	5 % 50 V 0603
C446	2320083	Ceramic cap.	1.0 n	5 % 50 V 0603
C447	2320091	Ceramic cap.	2.2 n	5 % 50 V 0603
C449	2320063	Ceramic cap.	150 p	5 % 50 V 0603
C450	2320091	Ceramic cap.	2.2 n	5 % 50 V 0603
C453	2320063	Ceramic cap.	150 p	5 % 50 V 0603
C454	2320091	Ceramic cap.	2.2 n	5 % 50 V 0603
C455	2320043	Ceramic cap.	22 p	5 % 50 V 0603
C456	2604431	Tantalum cap.	10 u	20 % 16 V 6.0x3.2x2.5
C457	2604209	Tantalum cap.	1.0 u	20 % 16 V 3.2x1.6x1.6
C458	2310784	Ceramic cap.	100 n	10 % 25 V 0805
C460	2310784	Ceramic cap.	100 n	10 % 25 V 0805
C465	2320083	Ceramic cap.	1.0 n	5 % 50 V 0603
C466	2604209	Tantalum cap.	1.0 u	20 % 16 V 3.2x1.6x1.6
C467	2604209	Tantalum cap.	1.0 u	20 % 16 V 3.2x1.6x1.6
C470	2310784	Ceramic cap.	100 n	10 % 25 V 0805
C490	2320043	Ceramic cap.	22 p	5 % 50 V 0603
L200	3609001	Coil	100 u	10 % Q=20/796 kHz Q20/796 kHz 8X11
L201	3609001	Coil	100 u	10 % Q=20/796 kHz Q20/796 kHz 8X11
L301	3641262	Ferrite bead 30r/100mhz 2a	1206	1206
L302	3641262	Ferrite bead 30r/100mhz 2a	1206	1206
L303	3641262	Ferrite bead 30r/100mhz 2a	1206	1206
L304	3641262	Ferrite bead 30r/100mhz 2a	1206	1206
L400	3641262	Ferrite bead 30r/100mhz 2a	1206	1206
L401	3641262	Ferrite bead 30r/100mhz 2a	1206	1206
Z300	4507733	Cer.reson 1.0mhz+–0.5% 8.0x5.0smd		8.0x5.0smd
Z400	3640035	Filt z>450r/100m 0r7max 0.2a 0603		0603
Z401	3640035	Filt z>450r/100m 0r7max 0.2a 0603		0603
Z402	3640035	Filt z>450r/100m 0r7max 0.2a 0603		0603
V200	4110195	Zener diode	BZX84	5 % 18 V 0.3 W SOT23
V201	4200917	Transistor	BC848B/BCW32	npn 30 V 100 mA SOT23
V202	4211423	MosFet	MTB30	D2PAK
V203	4108639	Diode x 2	BAS28	75 V 250 mA SOT143
V204	4200909	Transistor	BC858B/BCW30	pnp 30 V 100 mA SOT23
V205	4110074	Schottky diode	STPS340U	40 V 3 A SOD6
V207	4200917	Transistor	BC848B/BCW32	npn 30 V 100 mA SOT23
V208	4200917	Transistor	BC848B/BCW32	npn 30 V 100 mA SOT23
V300	4200917	Transistor	BC848B/BCW32	npn 30 V 100 mA SOT23
V301	4200917	Transistor	BC848B/BCW32	npn 30 V 100 mA SOT23
V302	4100285	Diode x 2	BAV99	70 V 200 mA SER.SOT23
V304	4200917	Transistor	BC848B/BCW32	npn 30 V 100 mA SOT23
V306	4100285	Diode x 2	BAV99	70 V 200 mA SER.SOT23
V307	4200917	Transistor	BC848B/BCW32	npn 30 V 100 mA SOT23

V309	4100285	Diode x 2	BAV99	70 V 200 mA SER.SOT23
V310	4100285	Diode x 2	BAV99	70 V 200 mA SER.SOT23
V311	4210096	Transistor	BCP54	npn 45 V 1.5 A SOT223
V312	4100285	Diode x 2	BAV99	70 V 200 mA SER.SOT23
V313	4210020	Transistor	BCP69–25	pnp 20 V 1 A SOT223
V314	4200917	Transistor	BC848B/BCW32	npn 30 V 100 mA SOT23
V315	4100218	Trans. supr.	LDP24A	100 V 30A/40 ms AG
V318	4108639	Diode x 2	BAS28	75 V 250 mA SOT143
D300	4370315	IC, MCU		QFP44
D400	4309431	IC, 4 x bi.switch	4066	SO14S
N200	4340127	Mic29152 reg ld adj 1.5a to263–5		TO263–5
N201	4305733	IC, 4 x comp	LM2901	SO14S
N202	4340067	IC, regulator	LP2951	3.3 V 100 mA
N204	4340067	IC, regulator	LP2951	3.3 V 100 mA
N400	4301182	IC, 2 x op.amp.	LM2902	SO14S
N401	4340125	L2726 2xop.amp pw5w1a 4–28v so20w		SO20W
N402	4301199	IC, 2 x op.amp.	LM2904	SO8S
S001	9510365	RF shield dmd02481 hfu–1		
X100	5400087	Modular jack 15pol f p2.04 90deg		90DEG
X200	540Y031	Use code 5400103		
X300	540Y021	Use code 5400093		
X400	5409057	Jack 2.5mm+sw+lock f 4pol str. s		SM
X500	5409059	Jack 3.5mm+sw+lock f 3pol str. s		SM
	9854195	PCB ED2 110.0X75.01.6 D 4/PA		
	9854195	PC board	ED2	110.0x75.01.6 d 4/pa

Block Diagram of Power & Charging (Version 5 Edit 94) for layout version 05

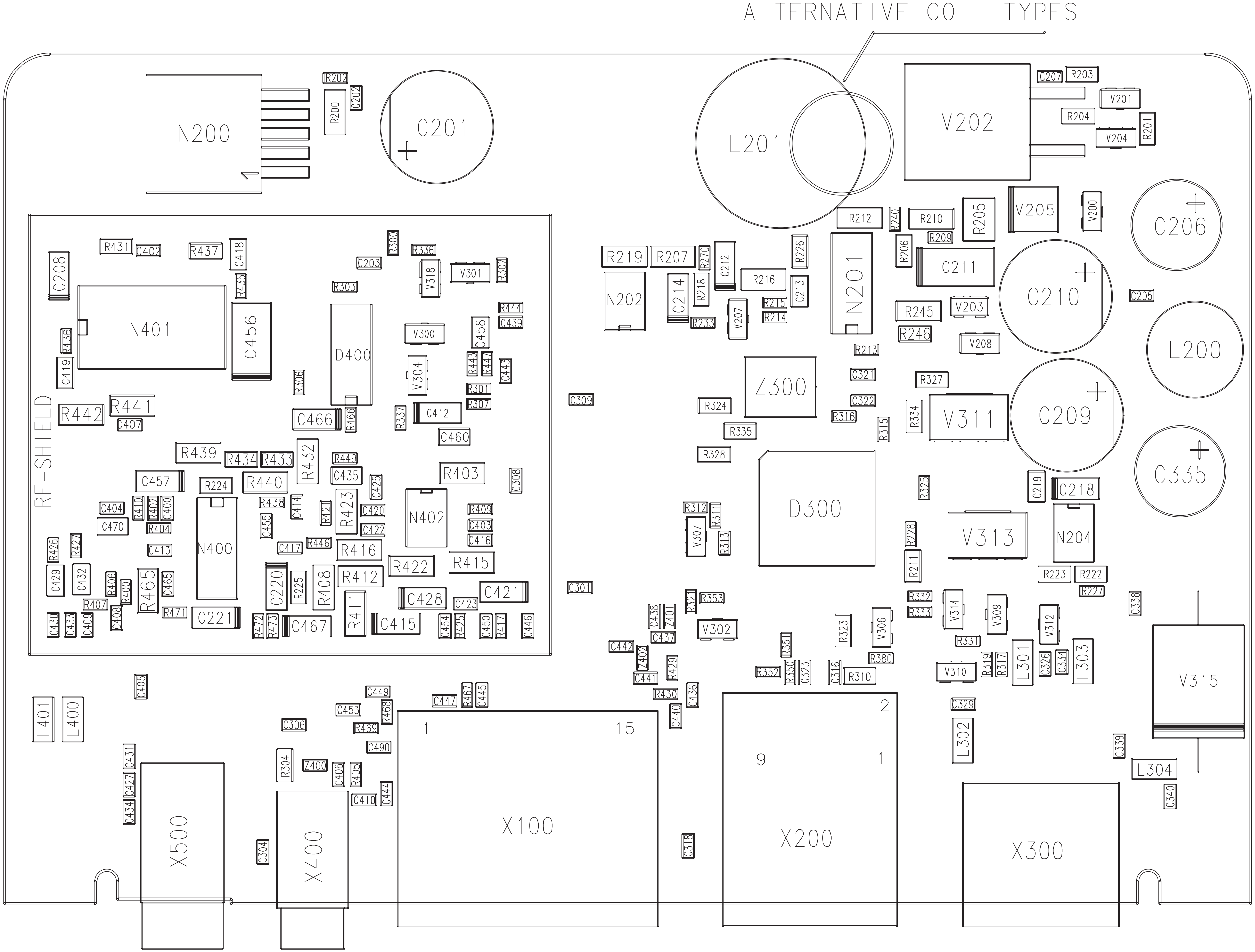


Circuit Diagram of Audio (Version 5 Edit 87) for layout version 05



N_A = NOT ASSEMBLED COMPONENT

Layout Diagram of ED2 (Version 05)



Loopset LPS-1/2

Original 10/98

AMENDMENT RECORD SHEET

Amendment Number	Date	Inserted By	Comments
	10/98	OJuntune	Original

CONTENTS

Loopset LPS-1/2

Introduction

Hearing impaired people, who use hearing aids (HA), have problems in using cellular phones. They can't identify speech, partly due to poor S/N–ratio and partly because of interference. Most HA have poor protection for interferences. By using the Loopset the interference problems are minimized. LPS–1 is designed for 5100 and 6100 series phones. LPS–2 is compatible with Communicator N9110 .

The Loopset has been developed for hearing aid users to allow them to use mobile phones. It is based on induction technology. These kind of induction devices are widely used with hearing aids, but never before implemented with cellular phones.

All hearing aids have support for induction loop, ie. they have a little telecoil inside. This coil can capture the signal supplied to the loop. Standard hearing aids have two operation modes; M–mode for normal microphone use and T–mode for telecoil use

The T–mode is used in places where the inductive loop has been assembled, for example in public halls, churches and places of assembly. The reason for T–mode use is much better S/N–ratio.

The Loopset provides clear acoustic quality. Automatic gain control (AGC) in the Loopset ensures that there is the correct field strength in the Loopset. The Loopset also dampens backgroud noise to make it easier to converse in a noisy environment, in the car for instance.

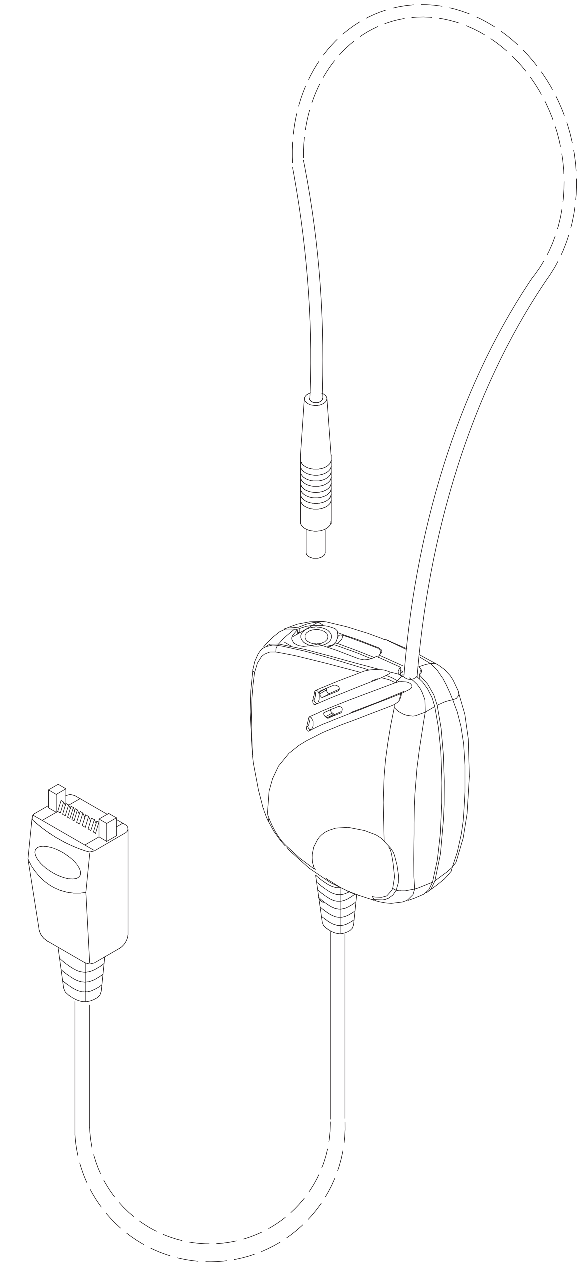
The Loopset can be used with all the mobile phones, which supports normal headset and vibra alarm. Vibra is needed just for call indication. The earpiece of a headset is replaced by a wireloop. Loopset has also integrated microphone.

The earpiece of a headset is replaced by a wireloop. Loopset has also integrated microphone.

The function is very simple and the use is environmentally friendly. Loopset is passed around the neck. The system doesn't disturb anybody due to the silent service. When the phone is set to auto–answer mode, a user don't have to do anything but switch the hearing aid to T–mode.

Loopset is an economic and simple solution for hearing aid users. Most hearing aids are compatible to this kind of wireless handsfree.

Basic Specification



List of Modules

Name of module	Type name	Material code	Note
LPS–1 Product	LPS–1	0630146	
LPS–1 Module	LPS–1	0201179	
Assembly parts	MLPS1	0261661	
LPS–2 Product	LPS–2	0630201	
Assembly parts	MLPS2	0261898	

Recommended batteries:

Type	Size	Min Vout	Max Vout	Rated capacity	Rated Time of Lopset. Speech in 1.0h days (4,2%). Consumption 8mA of the current.
Zinc Air Hearing Aid Battery	675 (LR44)	1.15	1,40	550 mAh	68 day (and hour).
Mercuric Hearing Aid Battery	675 (LR44)	1.25	1,45	280 mAh	35 day (and hour).
Alkaline Battery	LR44	1.25	1,45	150 mAh	19 day (and hour).

Technical Specifications

The Nokia LPS–1 Loopset is powered by three hearing aid batteries and comes pre–packaged with six zinc air batteries.

The ”auto answer” feature of the phone allows the users to be ”hands free” while using either the Nokia LPS–1 Loopset or headset accessories.

The interface between Loopset and phone is similier to a headset. Except the hight impedance input.

Name of function	Specification
Supply voltage	2,7 ... 4,5 V
Supply current	current peak<16 mA (nominal 5–6mA)

Unit	Max. dimensions (mm) (W x H x D)	Notes
LPS–1	41x36x18	Weight 60g

Functional Description

Modes of Operation

When the Loopset is identified the audio of the phone will be routed to the Loopset and the identification voltage is turned ON. Mic bias voltage 1.5 V is turned ON only in call state.

When the phone is turned off also the Loopset is in off–mode.

Loopset detection

In XMIC line there is a (47 + 2.2) kΩ pull–up in phone. A microphone is a low resistance pull down compared to that.

When there is no call going, AUXOUT is in high impedance state and XMIC is pulled up. When loopset is connected, XMIC is pulled down. XMIC is connected to HeadsetInt line (in MAD), so an interrupt is given due to both connection and disconnection.

During a call there is bias voltage (1.5 V) in AUXOUT. The state of HeadsetInt can't be sure. It is better to disable loopset interrupt during a call and poll from EAD line (AD converter in CCONT) to see if loopset is disconnected. Actually disconnection of a headset without remote control switch could be seen in HookInt, but headset with the switch could not.

Loop Adapter

Connection resistance must be under 3mΩ.

Magnetic Loop

The magnet field is based on the IEC 118–4 and BS 6083 part 4 standard.

Specification

Reception Specifications

Type of Function	Specification	Notes
Impedance	100k ohm +/– 5 % at 1 kHz	
Frequency responce	See figure 1	
Magnetic field	100mA/m (RMS) $\pm$3dB ref. 1kHz=0dB 400mA/m +12dB,125 ms RMS–peaks	The strength of the magnetic field measured next to the ear. (or measured in the horizontal plate and 170mm trip from the curve of the loop.)
Loop Current	700mA(RMS) $\pm$3dB ref. 1kHz =>0dB 2,8A (RMS), 125 ms RMS peaks =>+12dB	
Automatis Gain Control	Response time <35 ms Resetting time 0,5–5dB/s	
Signal to Noise Ratio	48 dB	nominal level (46 mVrms)/ 1kHz

Ratings

Determined as defined by IEC 268 using signal limited to frequency range 300 ... 3400 Hz.

Automatic Gain Control (AGC

Automatic gain control value is >30 decibels

Magnetic Field frequency response window

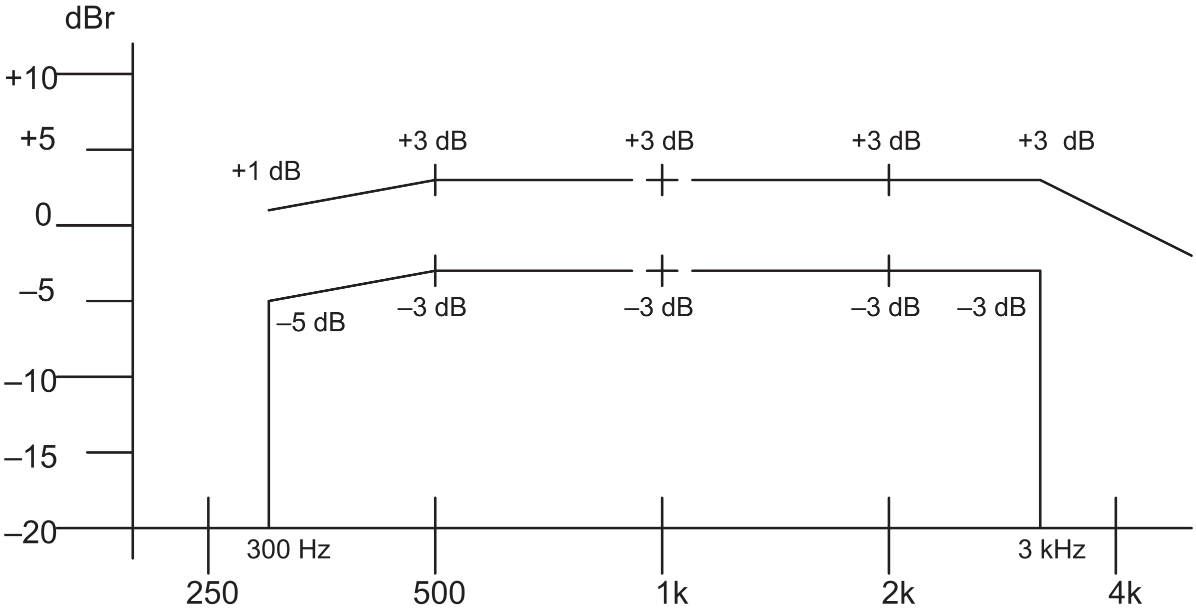


Figure 1. Magnetic field frequency response window of Loopset.

Functional Blocks

Table 1. Transmission Specifications

Object	Specification	Notes
Output impedance	1600 ohm +/– 30% 1kHz	
Frequency response	See Figure 2	
Sensitivity	–48 dB +6/–3 dB at 1kHz	0dBv/PA
Sensitivity dBm0	–13 dBm0 +6/–3 dBm0 at 1kHz	0dBv/PA – 4,7 dBPA
Sensitivity	–59 dB +6/–3 dB at 1kHz	0dBv/PA.
Sensitivity dBm0	–24 dBm0 +6/–3 dBm0 at 1kHz	
Directivity mic (acuctic)	OMNI–directional	
Signal to Noise Ratio	55 dB	1Pa/1kHz

Distortion and noise

Total distortion: at the — Max 3 % 300...3400Hz with sound pressure 0 dBPa microphone.

Microphone response window

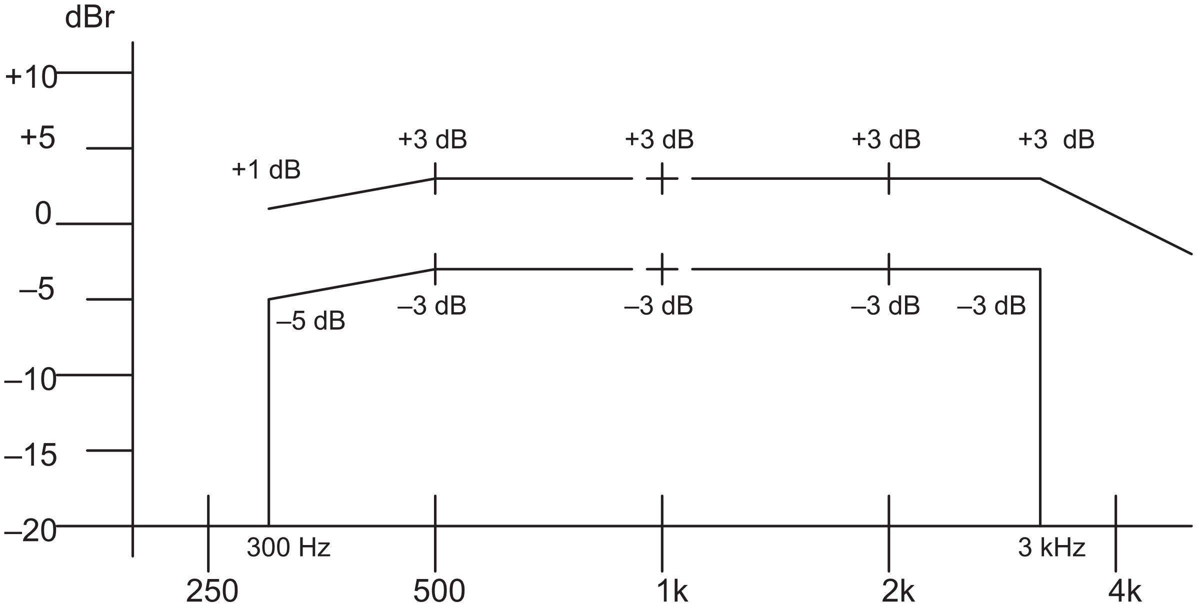


Figure 2. Mic response window of Loopset.

External Signals and Connections

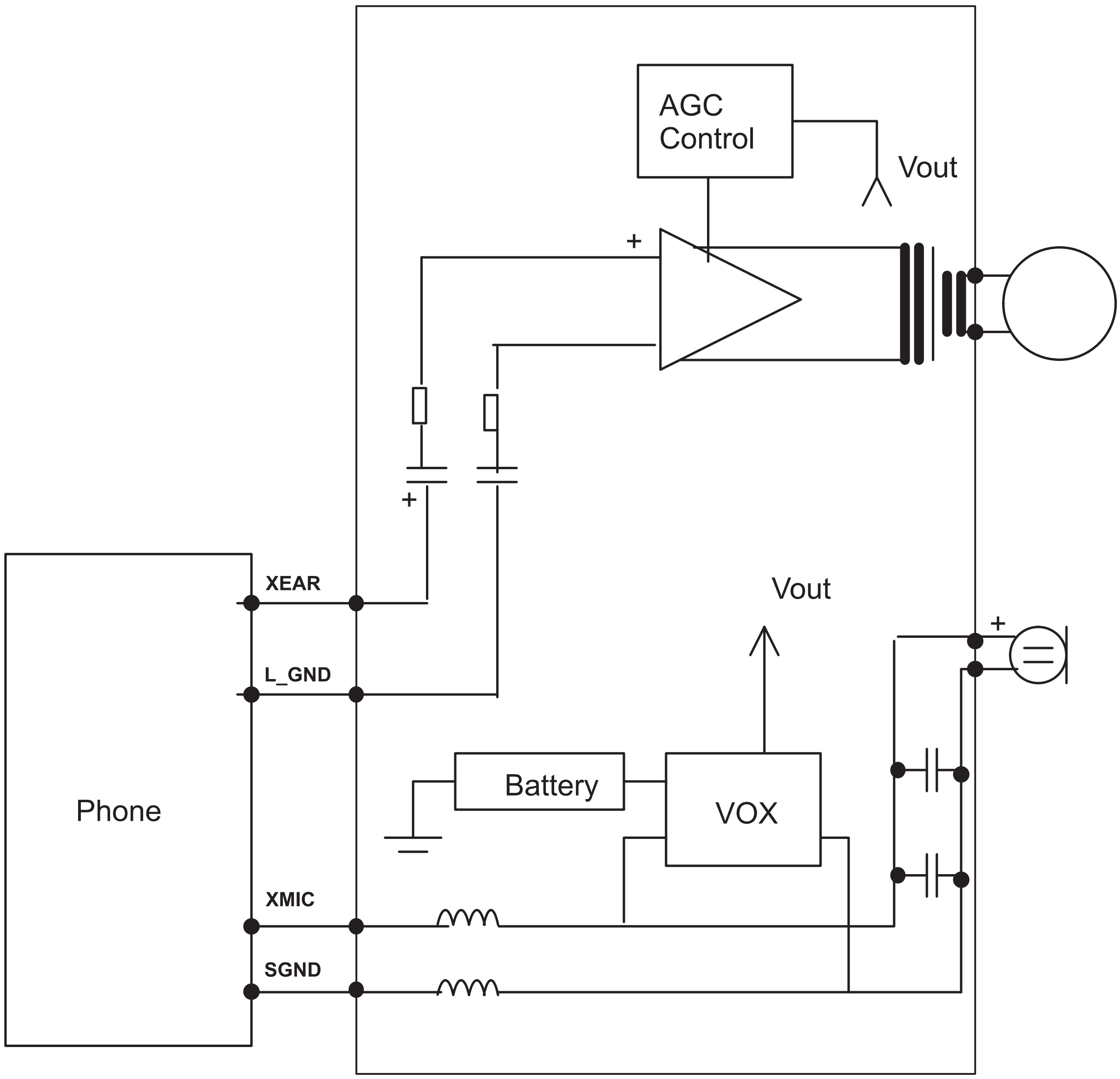
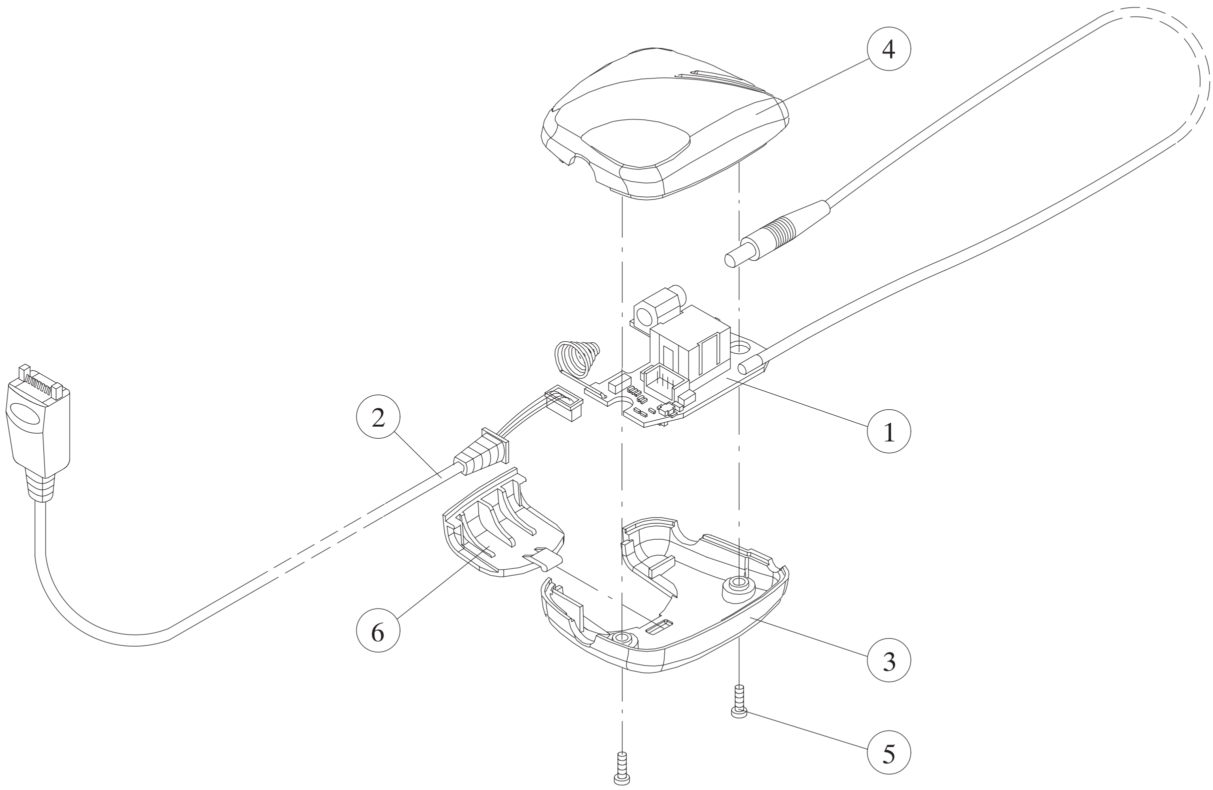


Figure 3. Combined Loopset and system connector audio signals

Table 2. X100 connector signals

Pin	Pin in x100	Name	Function	Min	Typ	Max	Unit	Description
1	**1**	**XMIC**	Headset microphone input (from accessory to phone)		1.6		kΩ	Headset source AC impedance
				100		400	µA	Bias current
						200	mV-p–p	Maximum signal level
			Headset detection (from accessory to phone)	1.47		2.9	V	No headset (ref. **SGND**).
				0		1.33	V	Headset connected (ref. **SGND**).
2	**2**	**SGND**	Audio signal ground. Separated from phone **GND** (from phone to accessory)		380 10		Ω nF	Resistance to phone ground (DC) (in phone) Series output capacitance
3	**3**	**XEAR**	Analog audio input (from phone to accessory)		47		Ω	Output AC impedance (ref. **GND**)
					10		nF	Series output capacitance
				16	100 k		Ω	Load AC impedance to **SGND**: Headset
					1.0		V	Max. input level. No load
4	**–**	**———**	Not Connected					—————————————
5	**–**	**———**	Not Connected					—————————————
6	**–**	**———**	Not Connected					—————————————
7	**4**	**L_GND**	Ground for Xear signals					

Exploded View of LPS-1/2



Assembly parts of LPS-1/2

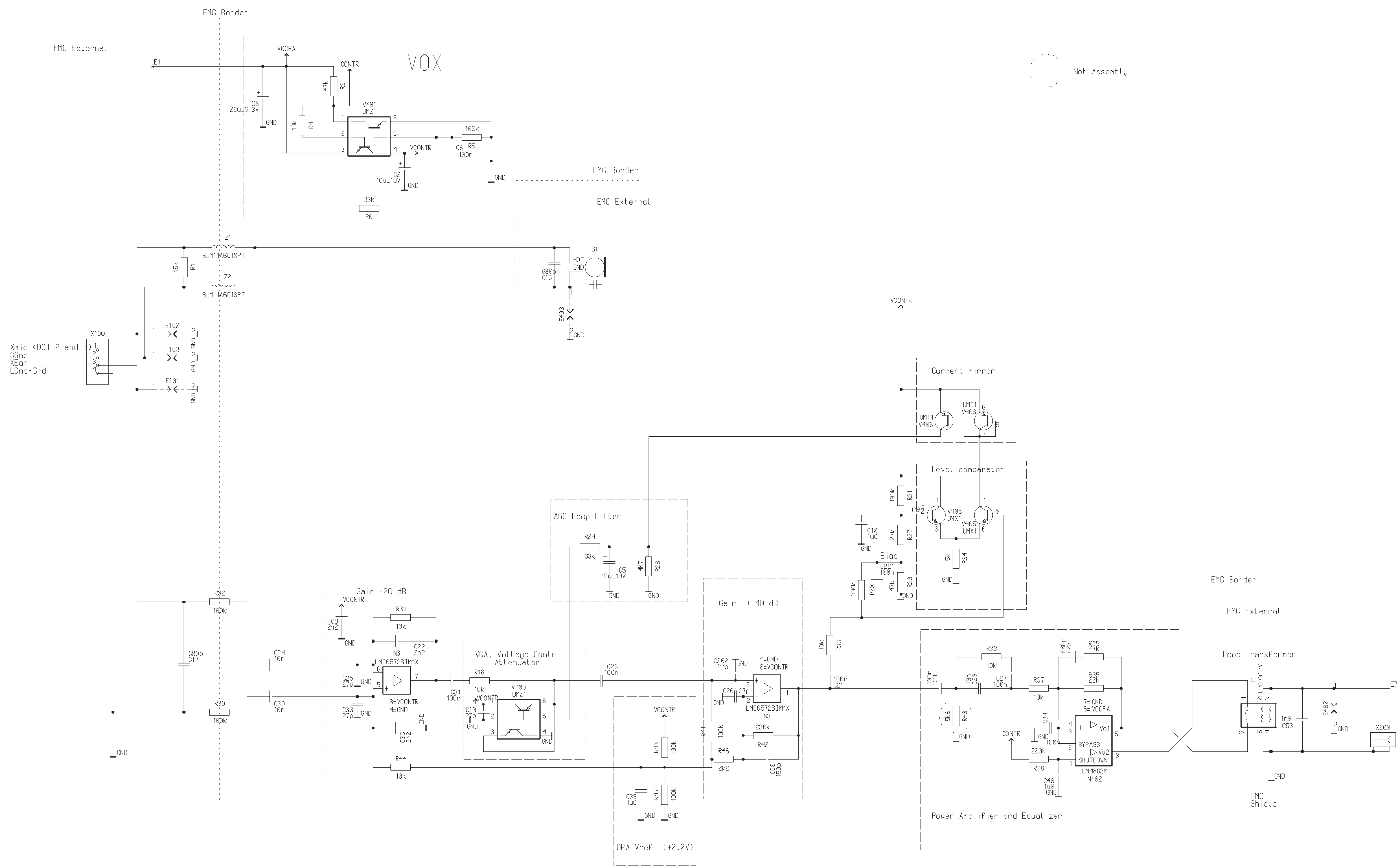
ITEM	Q'TY	CODE	DESCRIPTION	VALUE, TYPE
1		0201179	Module	lps-1
2		9780224	Loop set Cable LPS–1	DMD02438
alt		9780241	Loop set Cable LPS–2	DMD04474
3		9451016	B–cover	DMD02639
4		9451015	A–cover	DMD02638
5	2	6290021	PT-screw	1,8x8 feznTX6
6		9451246	Battery lid	DMD03654

Parts List of LPS–1 (Version 6.1) Code: 0201179

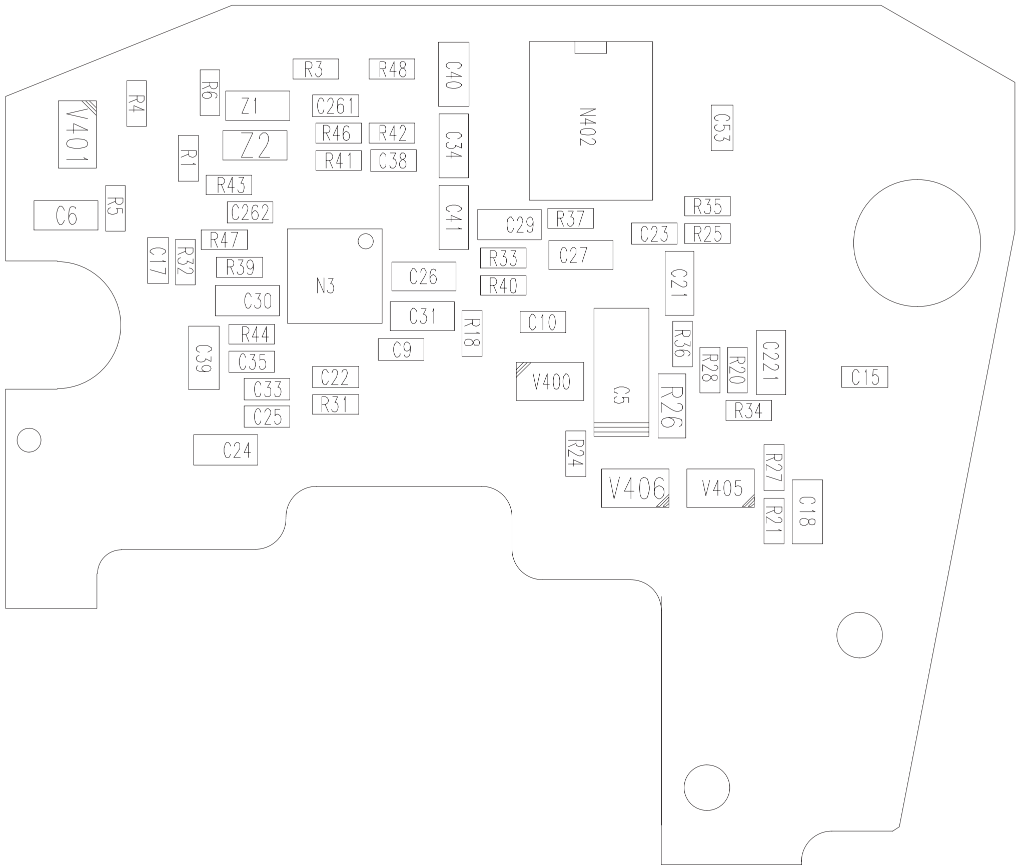
ITEM	CODE	DESCRIPTION	VALUE	TYPE
R001	1430784	Chip resistor	15 k	5 % 0.063 W 0402
R003	1430796	Chip resistor	47 k	5 % 0.063 W 0402
R004	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R005	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R006	1430792	Chip resistor	33 k	5 % 0.063 W 0402
R018	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R020	1430796	Chip resistor	47 k	5 % 0.063 W 0402
R021	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R024	1430792	Chip resistor	33 k	5 % 0.063 W 0402
R025	1430796	Chip resistor	47 k	5 % 0.063 W 0402
R026	1430122	Chip resistor	4.7 M	5 % 0.063 W 0603
R027	1430790	Chip resistor	27 k	5 % 0.063 W 0402
R028	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R031	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R032	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R033	1430780	Chip resistor	12 k	5 % 0.063 W 0402
R034	1430784	Chip resistor	15 k	5 % 0.063 W 0402
R035	1430788	Chip resistor	22 k	5 % 0.063 W 0402
R036	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R037	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R039	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R041	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R042	1430812	Chip resistor	220 k	5 % 0.063 W 0402
R043	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R044	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R046	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R047	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R048	1430812	Chip resistor	220 k	5 % 0.063 W 0402
C002	2610003	Tantalum cap.	10 u	20 % 10 V
3.2x1.6x1.6				
C005	2610003	Tantalum cap.	10 u	20 % 10 V
3.2x1.6x1.6				
C006	2320779	Ceramic cap.	100 n	10 % 16 V 0603
C008	2610101	Tantalum cap.	22 u	20 % 3.5x2.8x1.9
C009	2320592	Ceramic cap.	2.2 n	5 % 50 V 0402
C010	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C015	2320580	Ceramic cap.	680 p	5 % 50 V 0402
C017	2320580	Ceramic cap.	680 p	5 % 50 V 0402
C018	2320469	Ceramic cap.		Y5 V 0603
C021	2320779	Ceramic cap.	100 n	10 % 16 V 0603
C022	2320592	Ceramic cap.	2.2 n	5 % 50 V 0402
C023	2320580	Ceramic cap.	680 p	5 % 50 V 0402
C024	2320107	Ceramic cap.	10 n	5 % 50 V 0603

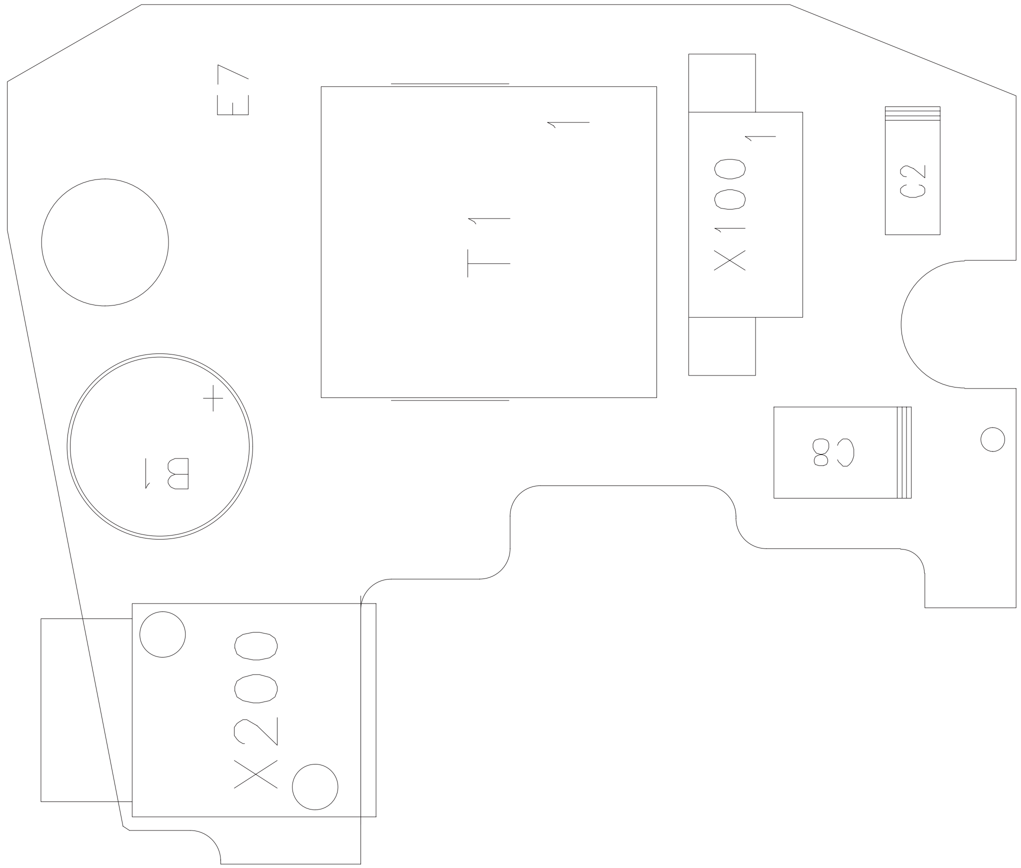
C025	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C026	2320779	Ceramic cap.	100 n	10 % 16 V 0603
C027	2320779	Ceramic cap.	100 n	10 % 16 V 0603
C029	2320107	Ceramic cap.	10 n	5 % 50 V 0603
C030	2320107	Ceramic cap.	10 n	5 % 50 V 0603
C031	2320779	Ceramic cap.	100 n	10 % 16 V 0603
C033	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C034	2320779	Ceramic cap.	100 n	10 % 16 V 0603
C035	2320592	Ceramic cap.	2.2 n	5 % 50 V 0402
C038	2320564	Ceramic cap.	150 p	5 % 50 V 0402
C039	2320469	Ceramic cap.		Y5 V 0603
C040	2320469	Ceramic cap.		Y5 V 0603
C041	2320779	Ceramic cap.	100 n	10 % 16 V 0603
C053	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C221	2320779	Ceramic cap.	100 n	10 % 16 V 0603
C261	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C262	2320546	Ceramic cap.	27 p	5 % 50 V 0402
B001	5140117	Cond mic 45+–	3DB 33PF 2K	D5.8/9.D5.8/9.0
Z001	3640035	Filt z>450r/100m 0r7max 0.2a 0603		0603
Z002	3640035	Filt z>450r/100m 0r7max 0.2a 0603		0603
T001	3640073	Af–transformer for manual p&p smd		SMD
V400	4219922	Transistor x 2		UM6
V401	4219922	Transistor x 2		UM6
V405	4219904	Transistor x 2	UMX1	npn 40 V SOT363
V406	4219908	Transistor x 2		SOT363
N003	4340379	IC, 2xop amp 2.7/3v ssoLMC6572BIMM		SSOP8
N402	4340331	IC, Power amp.	LM4862	P W SO8S
X100	5409067	SM,	pin header 1x04 p1.25 1a	STR.
X200	5400125	SM,	pcb conn 4mm	f 90degree
	6400039	Battery spring		dmd03655
	9854251	PCB	LPS1 28.2X33.1X1.0	M4 24/PA

Circuit Diagram of LPS–1 module (Version 03 Edit 145)

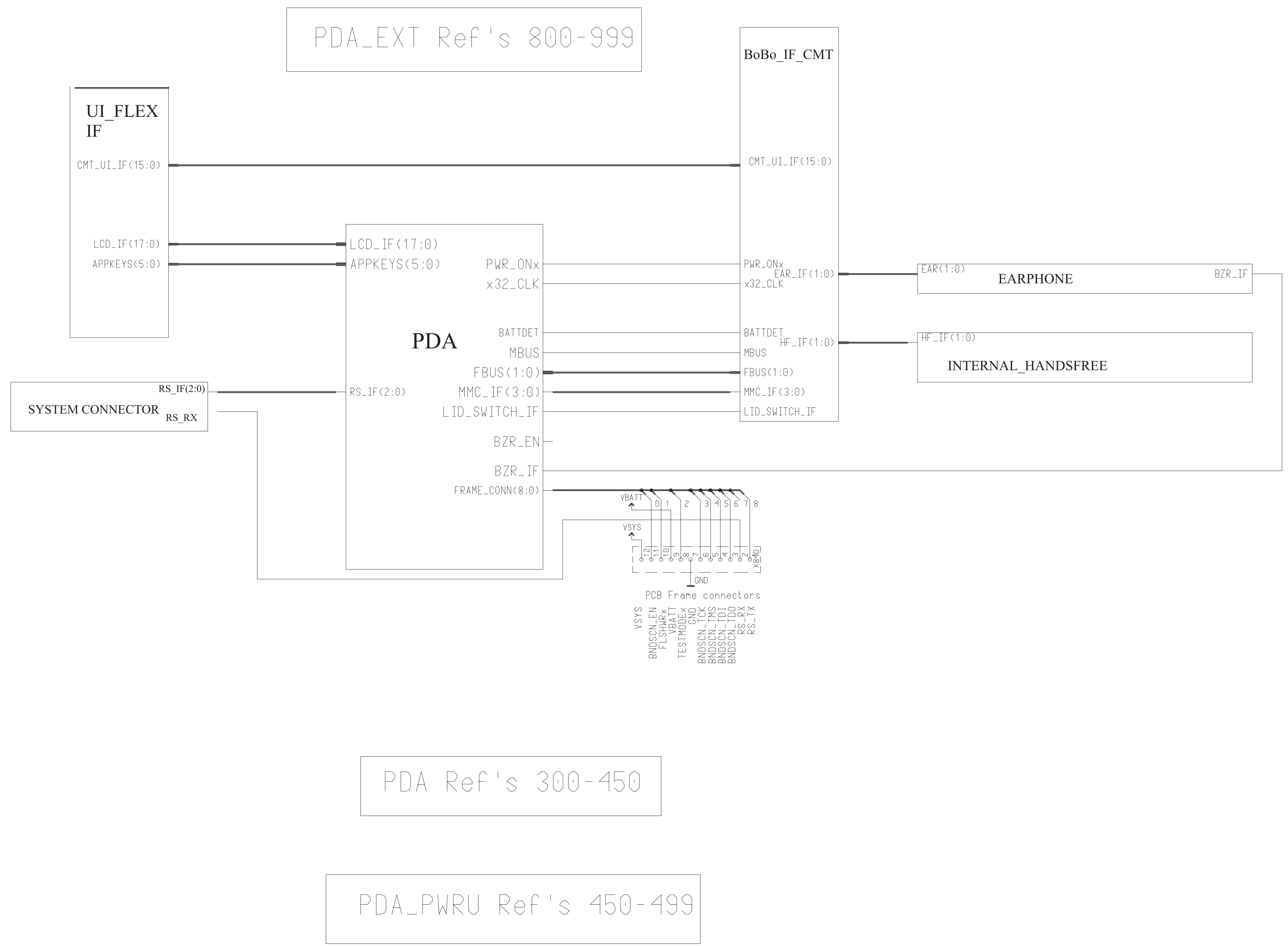


Layout Diagram LPS–1 module (Version 03 Edit 145)

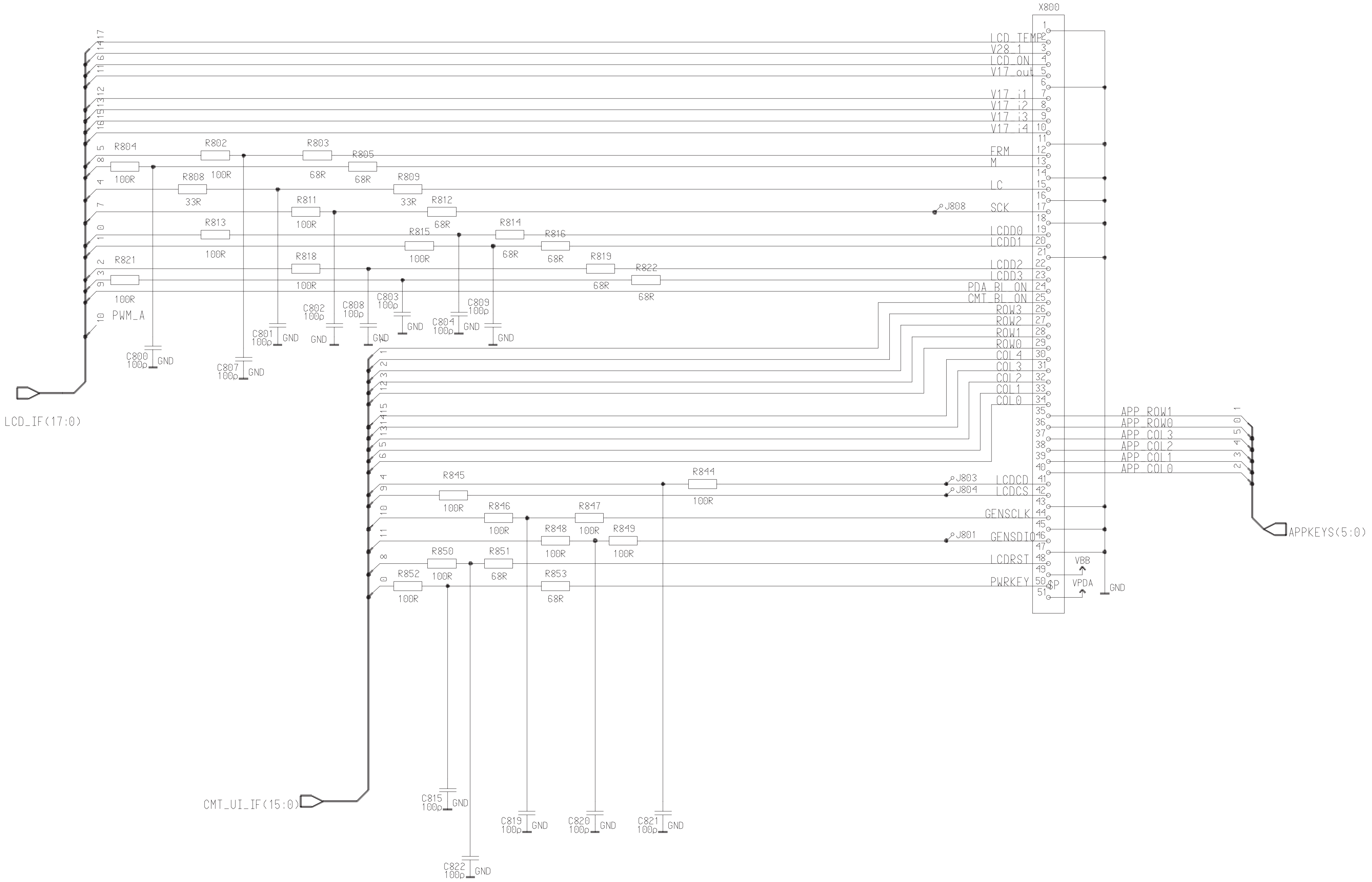




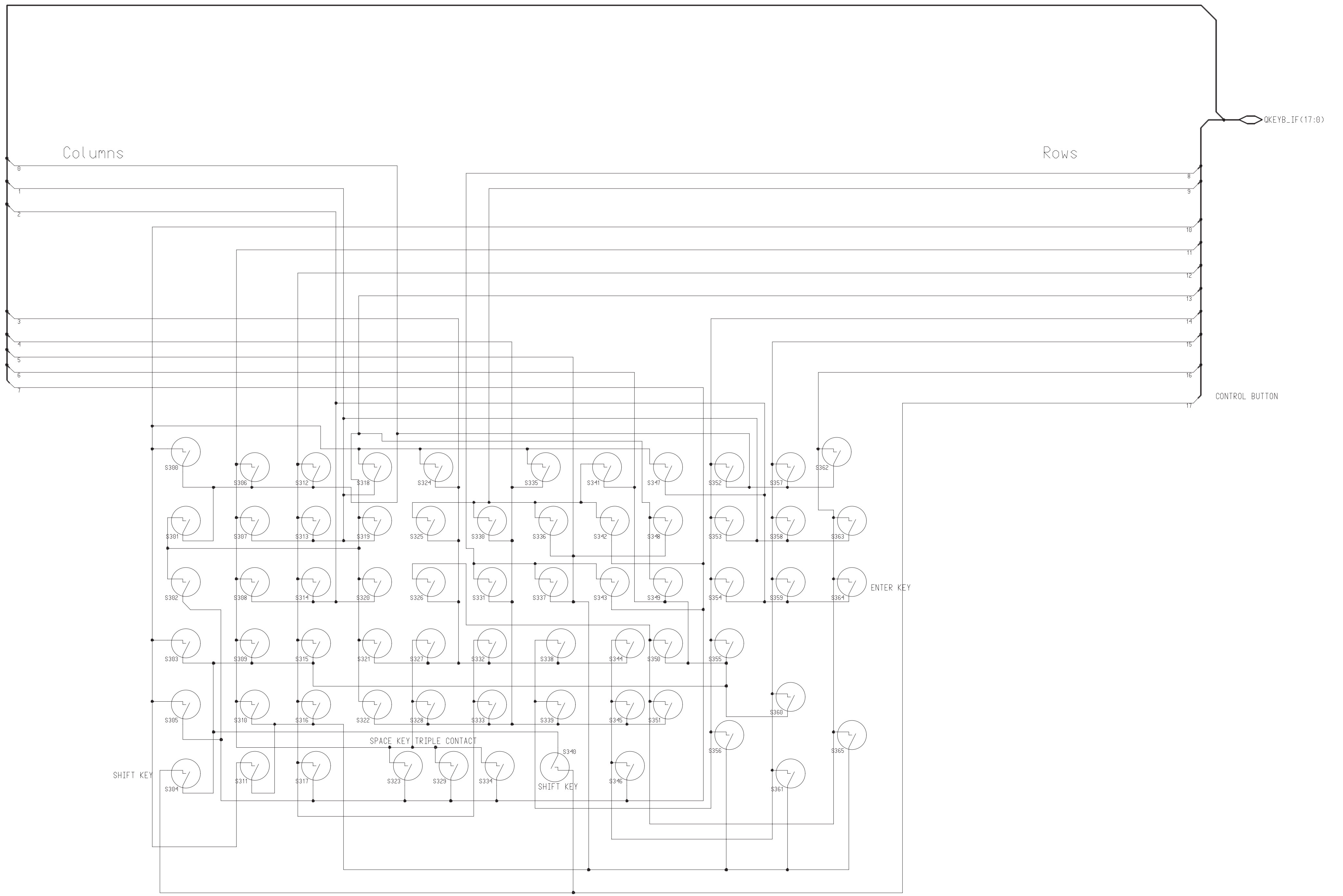
Block Diagram of PDA (0.0 edit 103 v _10)



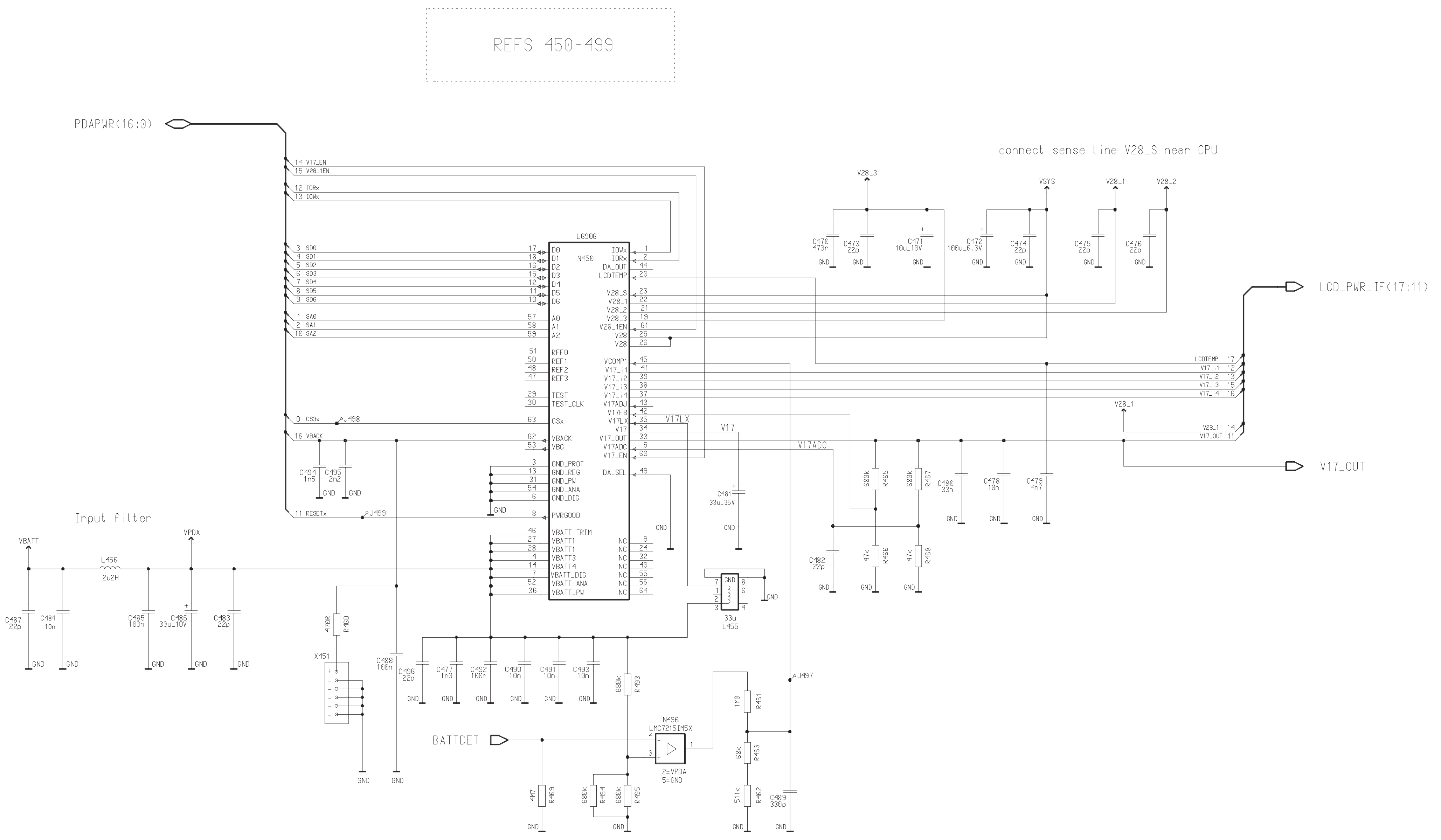
Circuit Diagram of UI FLEX IF (0.0 Edit 72) for ver_10



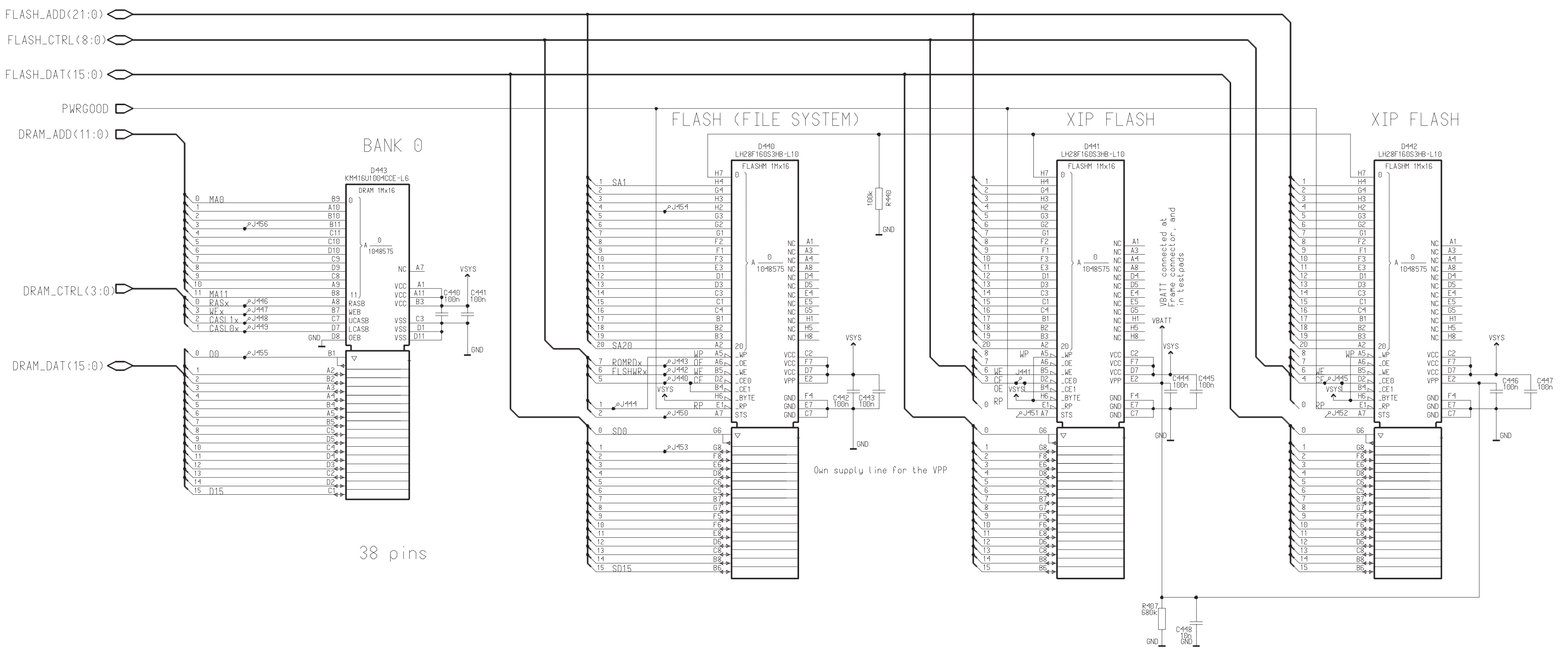
Circuit Diagram of PDA QWERTY Keyboard (0.0 Edit 23) for ver_10



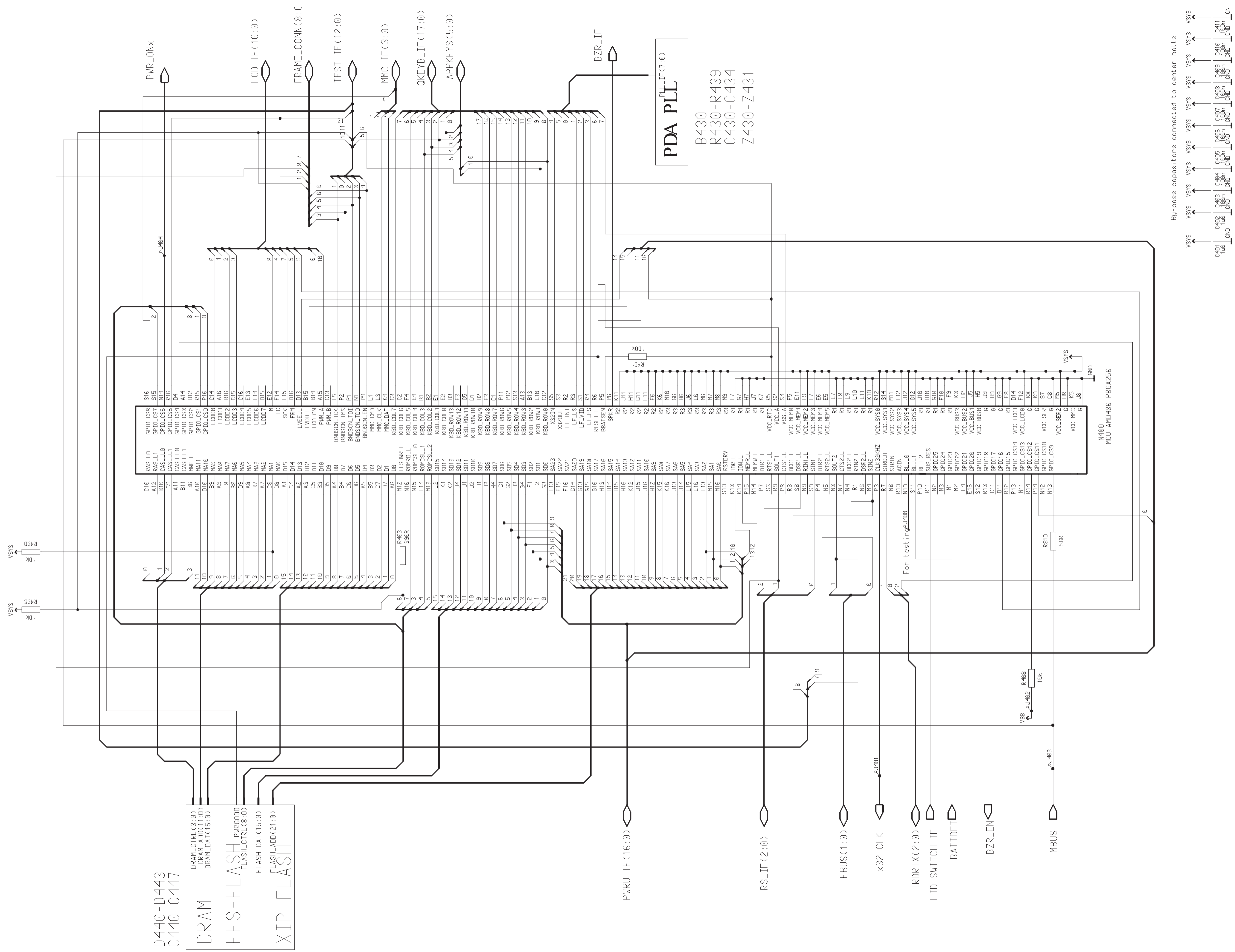
Circuit Diagram of BS1 PDA PWRU (0.0 Edit 137) for ver_10



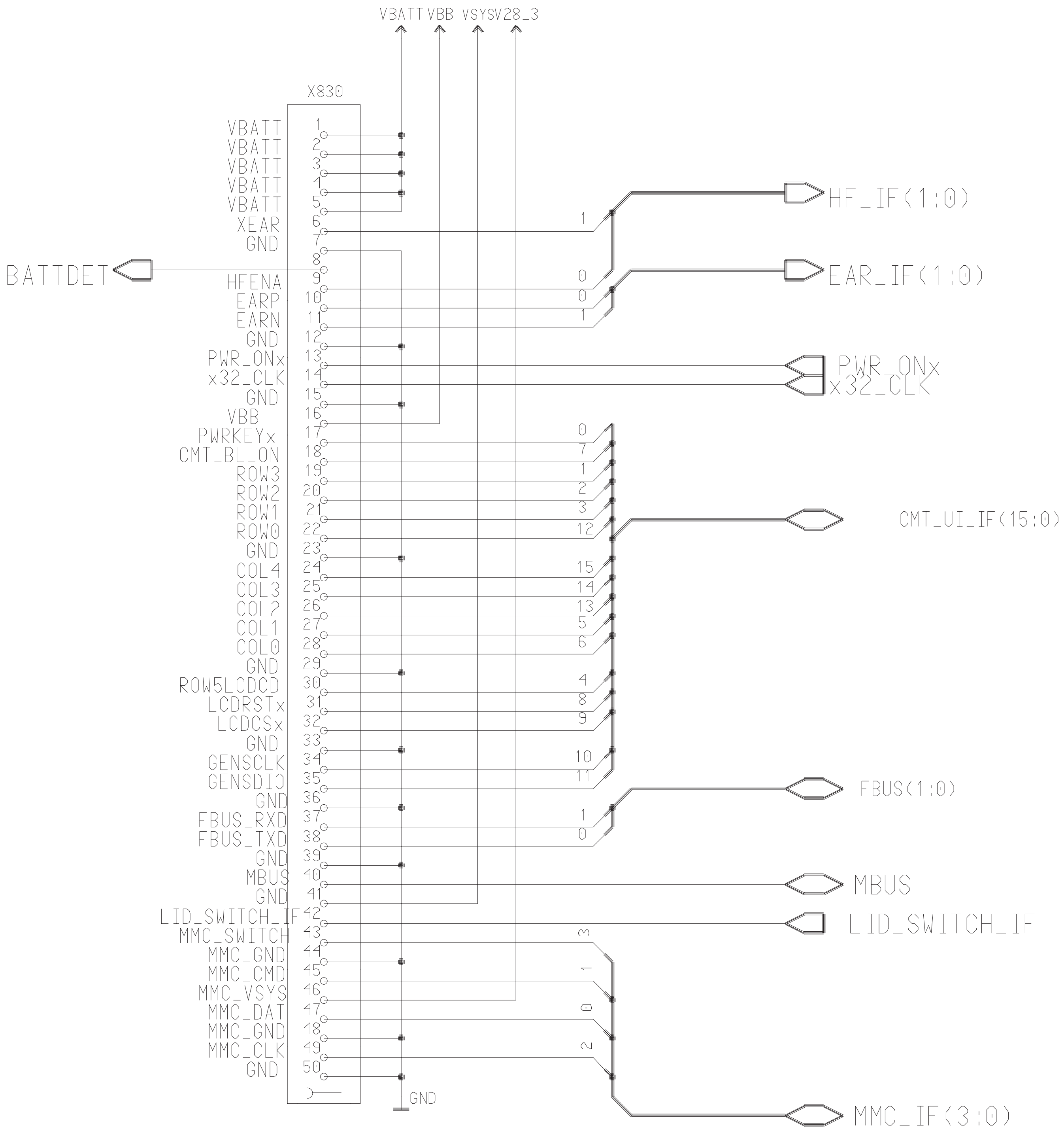
Circuit Diagram of BS1 PDA MEM (0.0 Edit 64) for ver_10



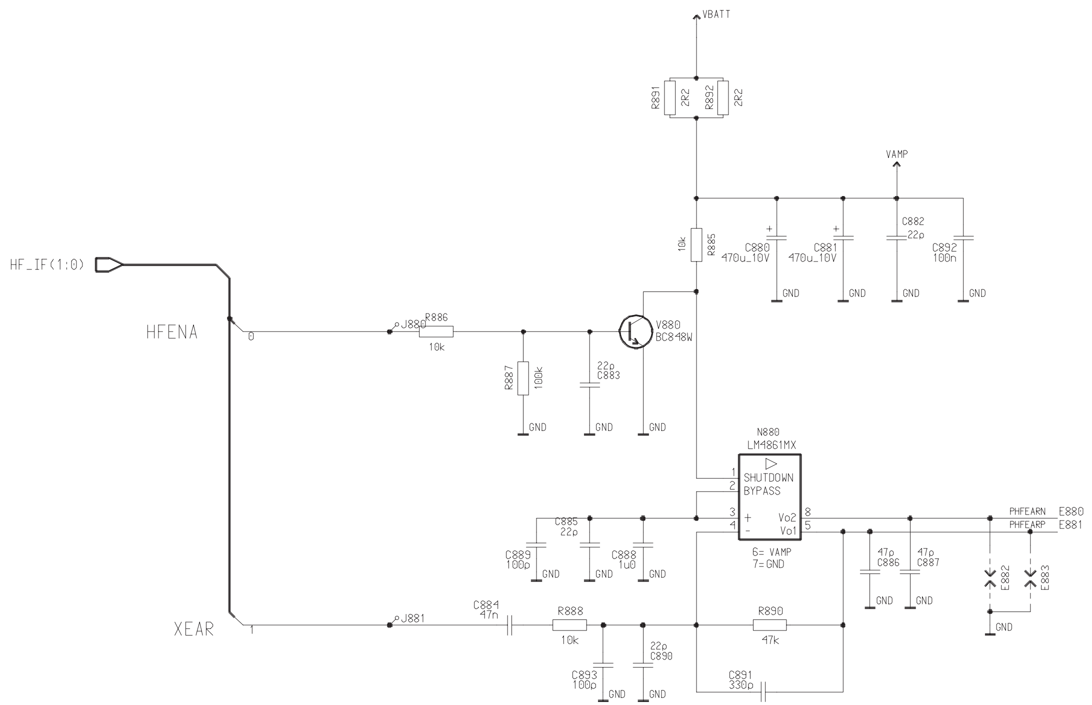
Circuit Diagram of BS1 PDA MCU Block (0.0 Edit 192) for ver_10



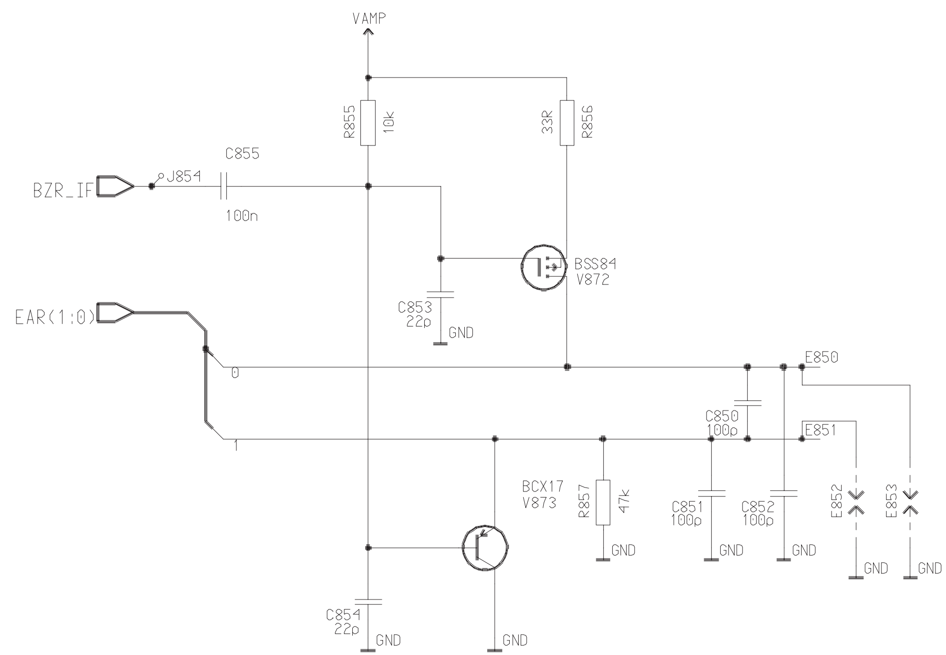
Circuit Diagram of BS1 PDA B0B0 (0.0 Edit 55) for ver_10



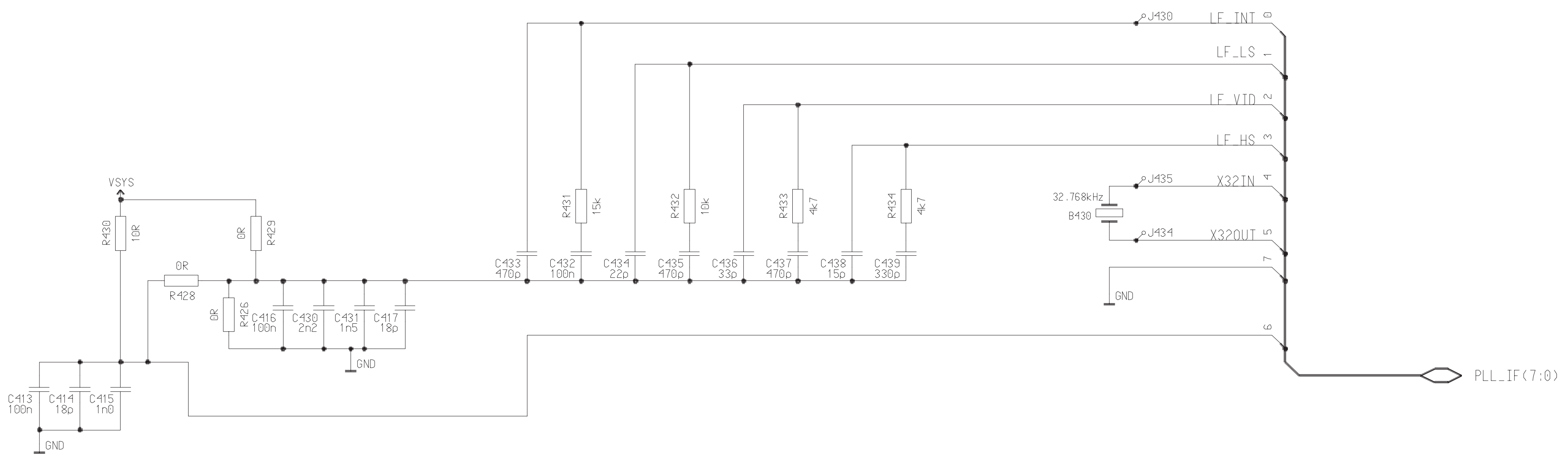
Circuit Diagram of BS1 PDA Internal HF IF (0.0 Edit 83) for ver_10



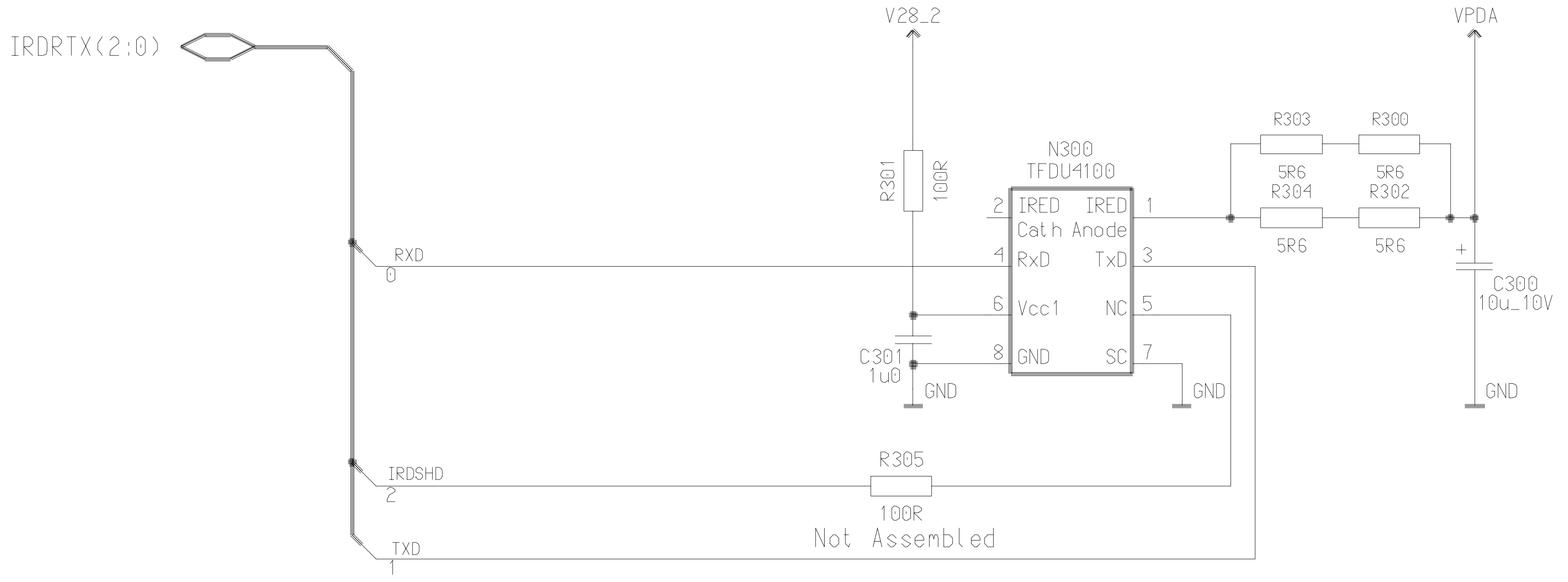
Circuit Diagram of BS1 PDA Earphone (0.0 Edit 25) for ver_10



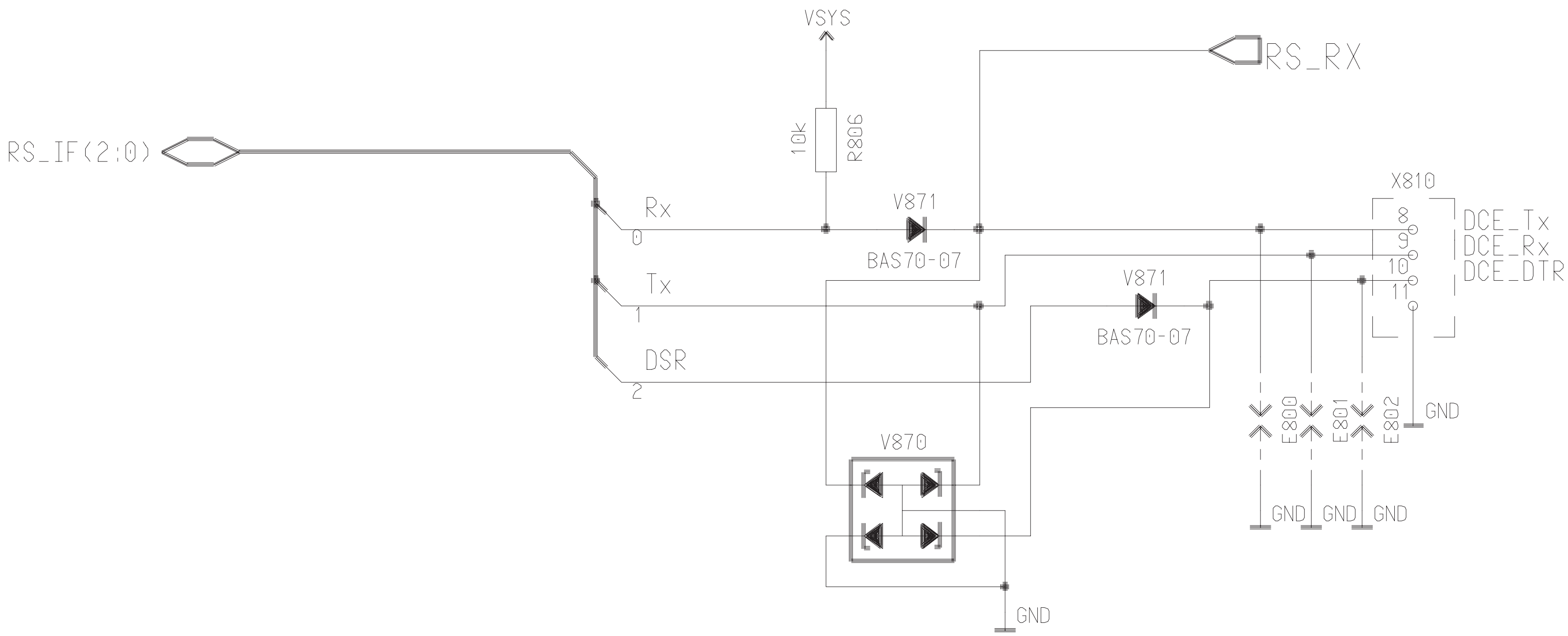
Circuit Diagram of BS1 PDA PLL (0.0 Edit 42) for ver_10



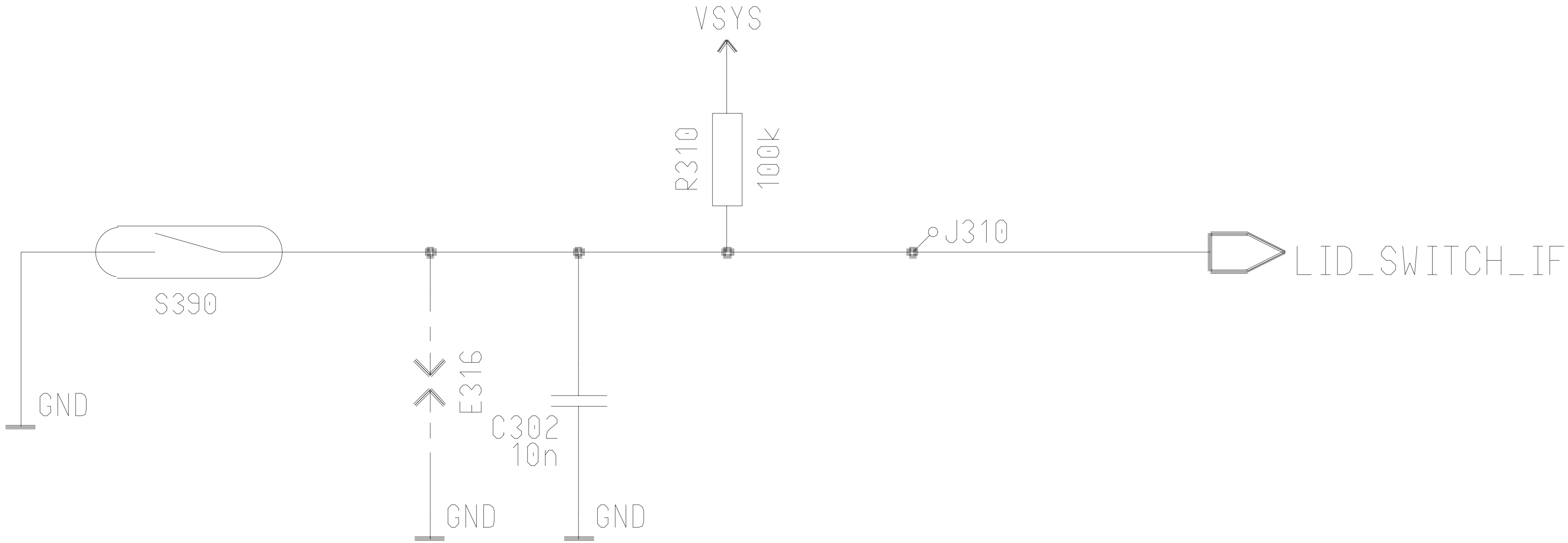
Circuit Diagram of BS1 PDA IRDA (0.0 Edit 27) for ver_10



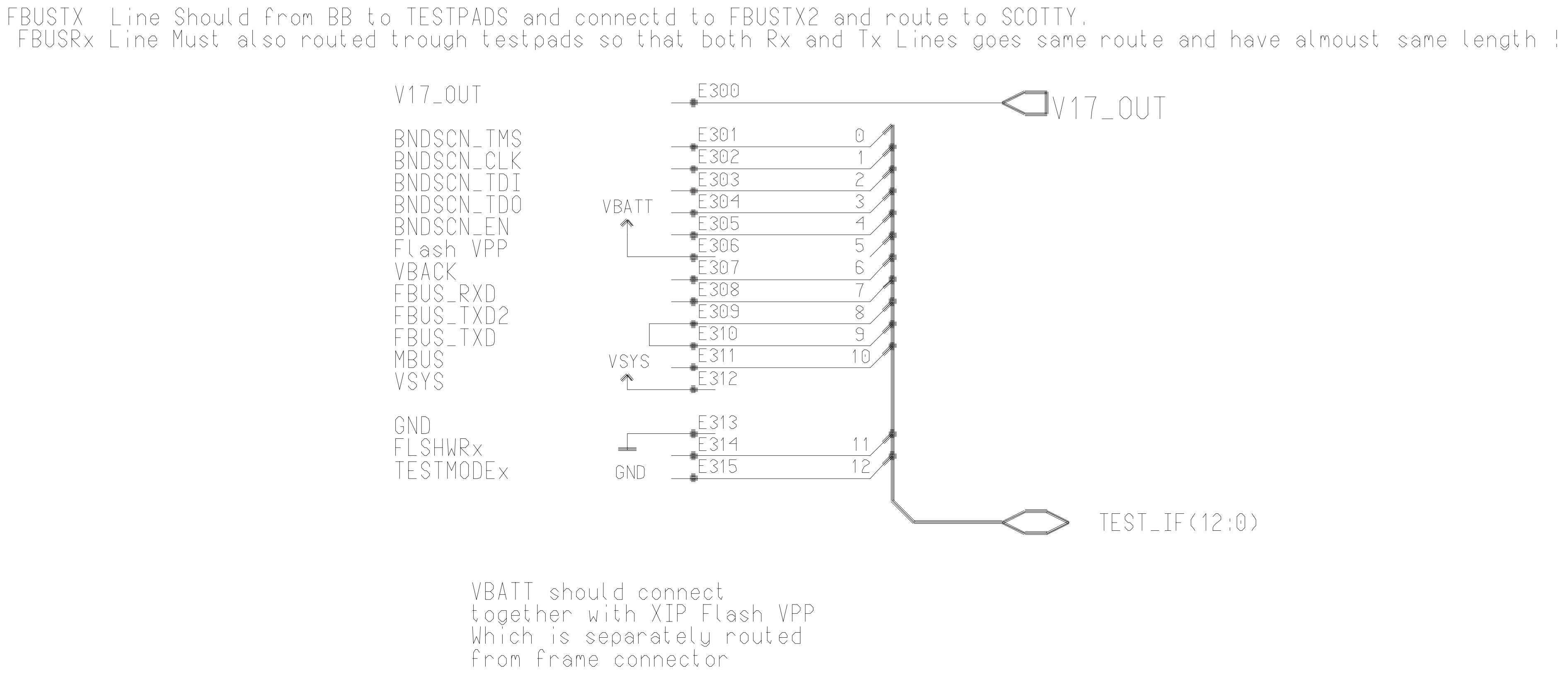
Circuit Diagram of BS1 System Connector Pads (0.0 Edit 26) for ver_10



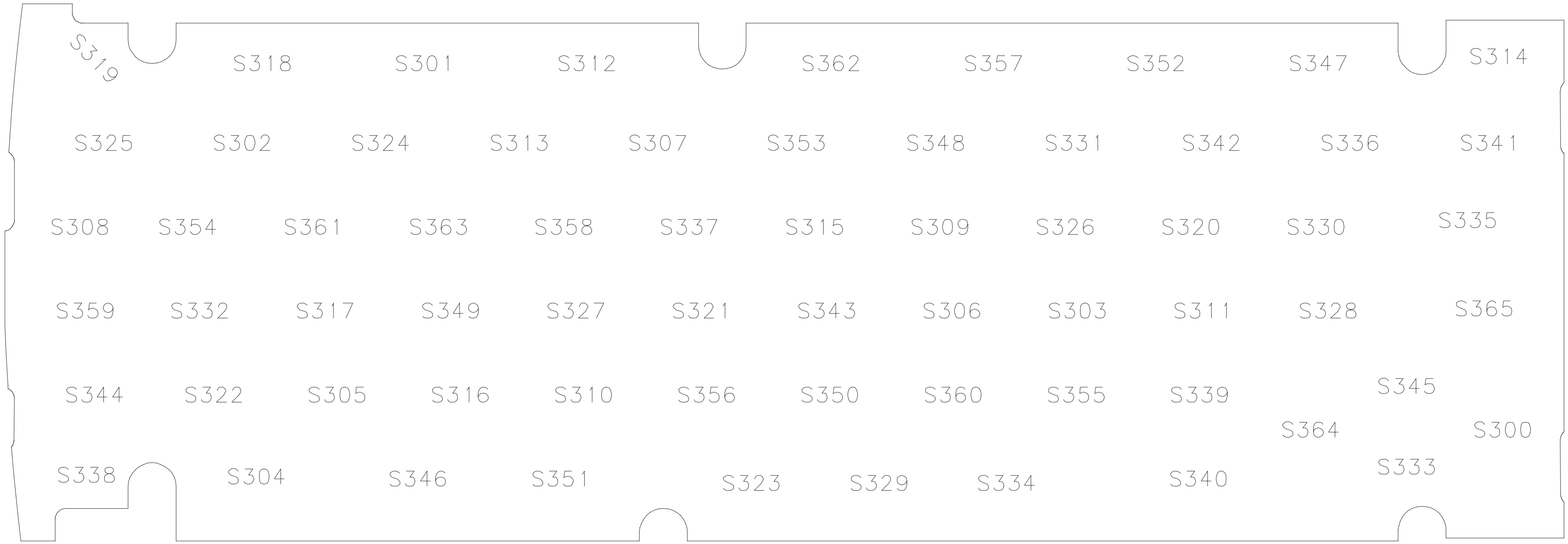
Circuit Diagram of BS1 Lid Switch (0.0 Edit 26) for ver_10



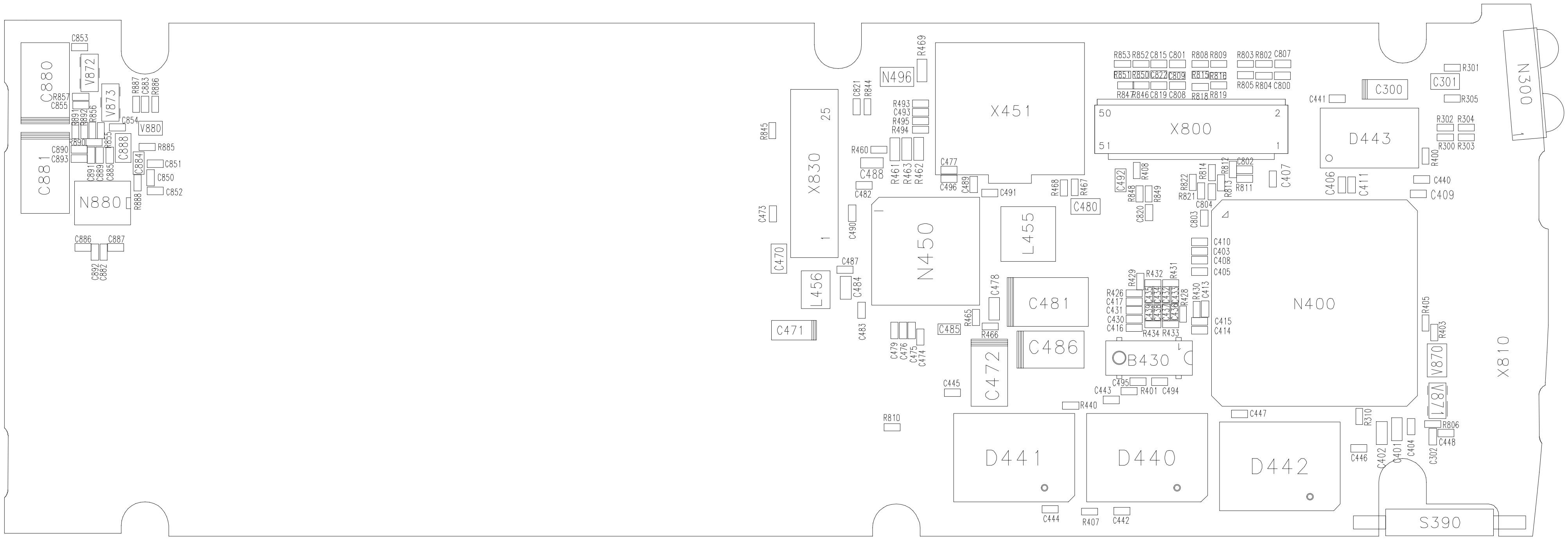
Circuit Diagram of BS1 PDA Test Pads (0.0 Edit 39) for ver_10



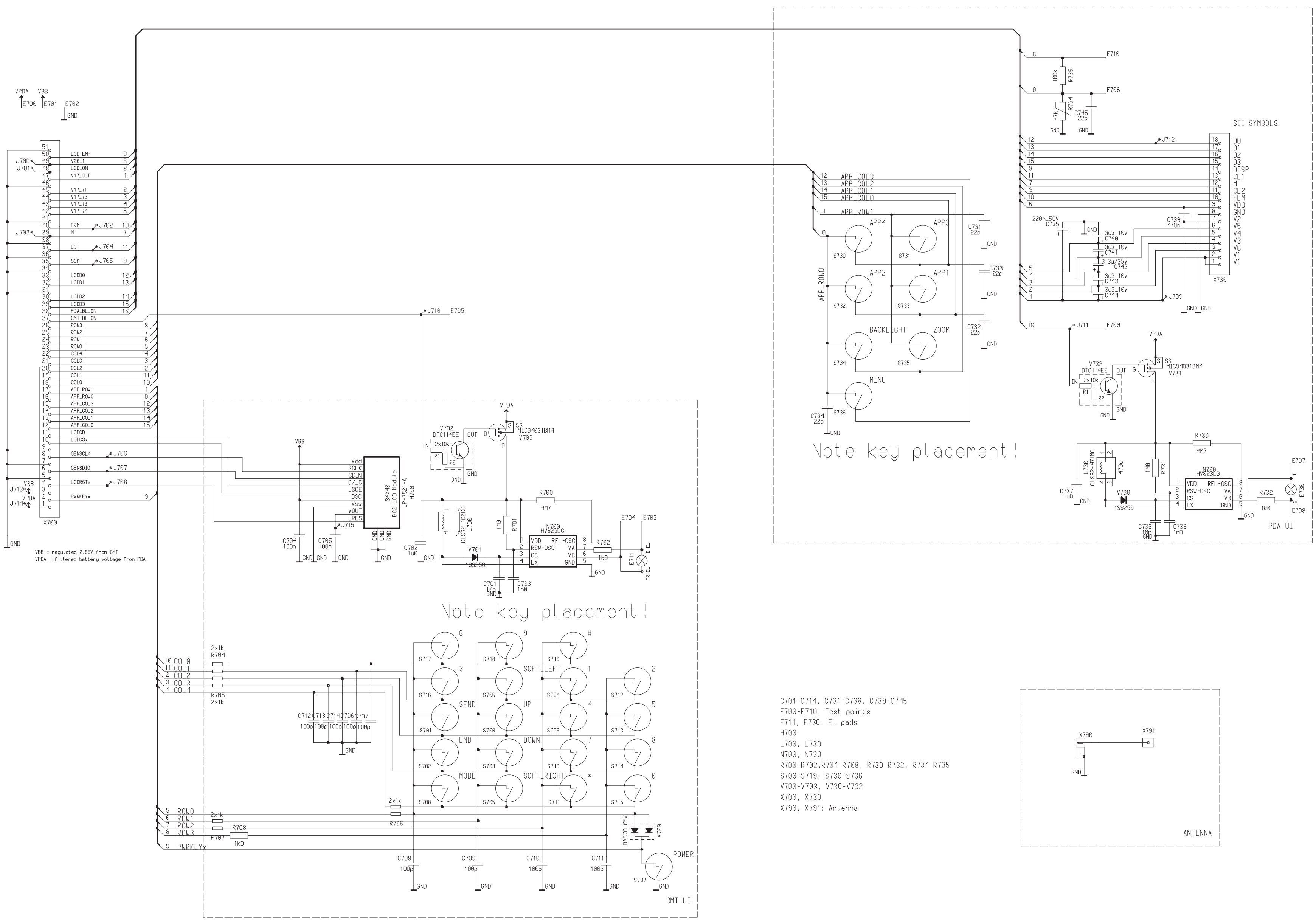
Parts Placement Diagram of BS1 PDA 1/2 (0.0) _10



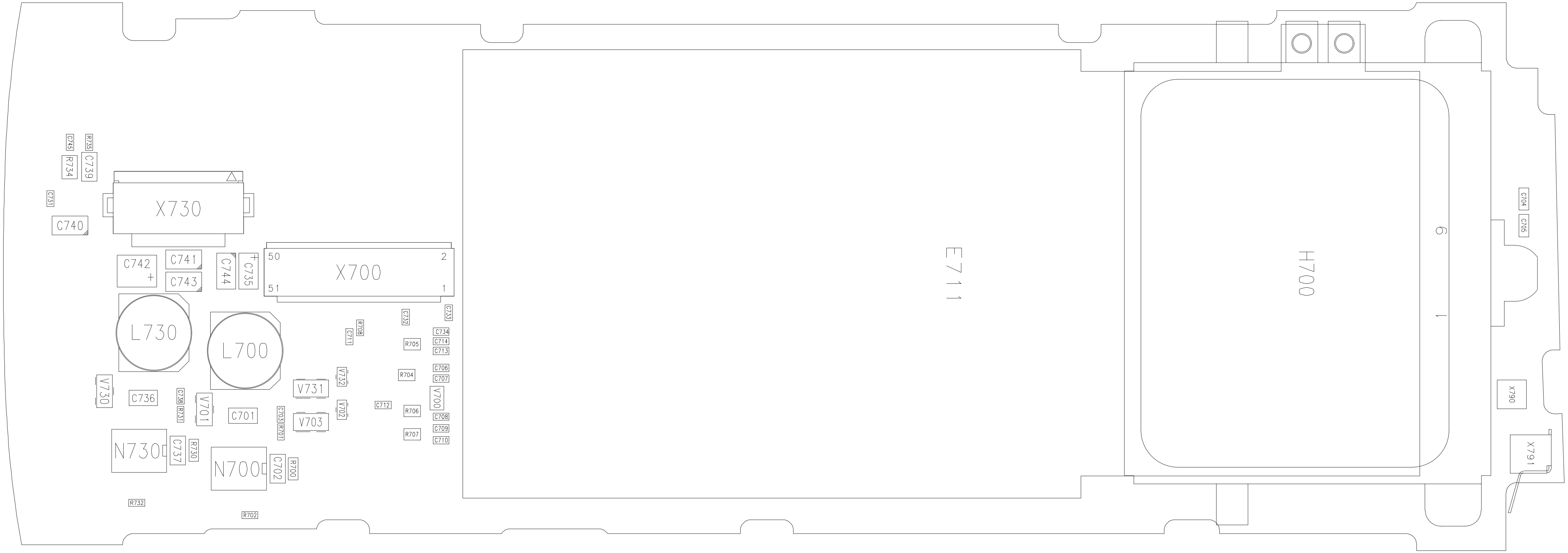
Parts Placement Diagram of BS1 PDA 2/2 (0.0) _10



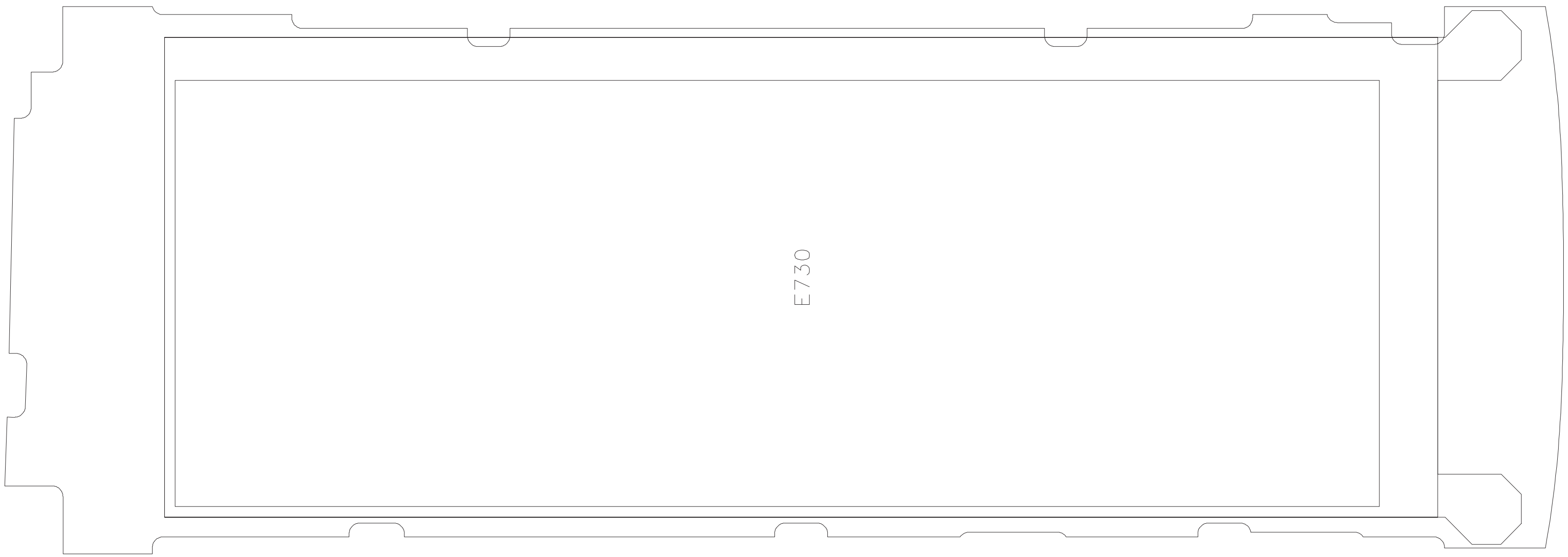
Circuit Diagram of BS2 (0.0 Edit 116) _09



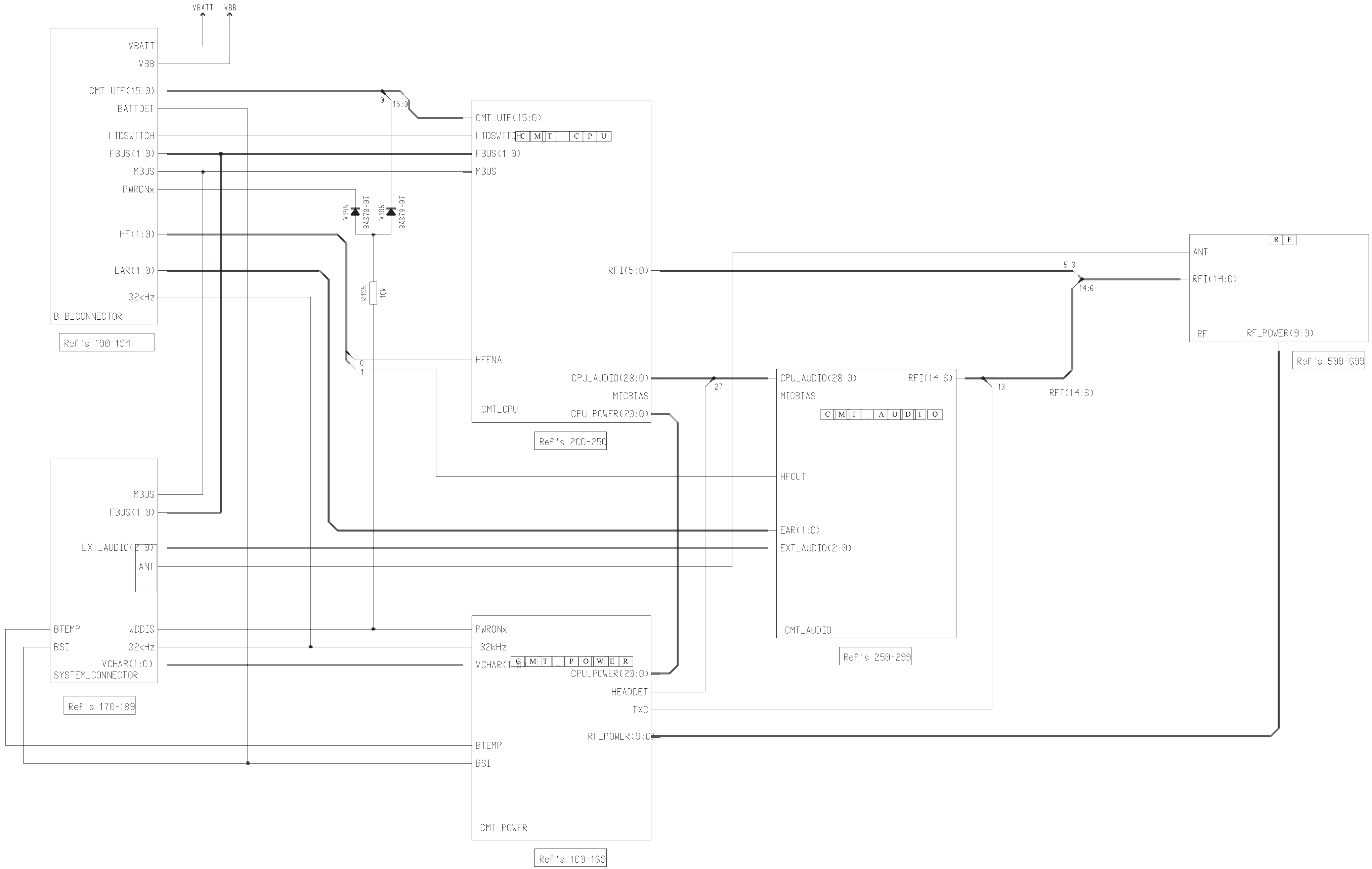
Parts Placement Diagram of BS2 1/2) _09



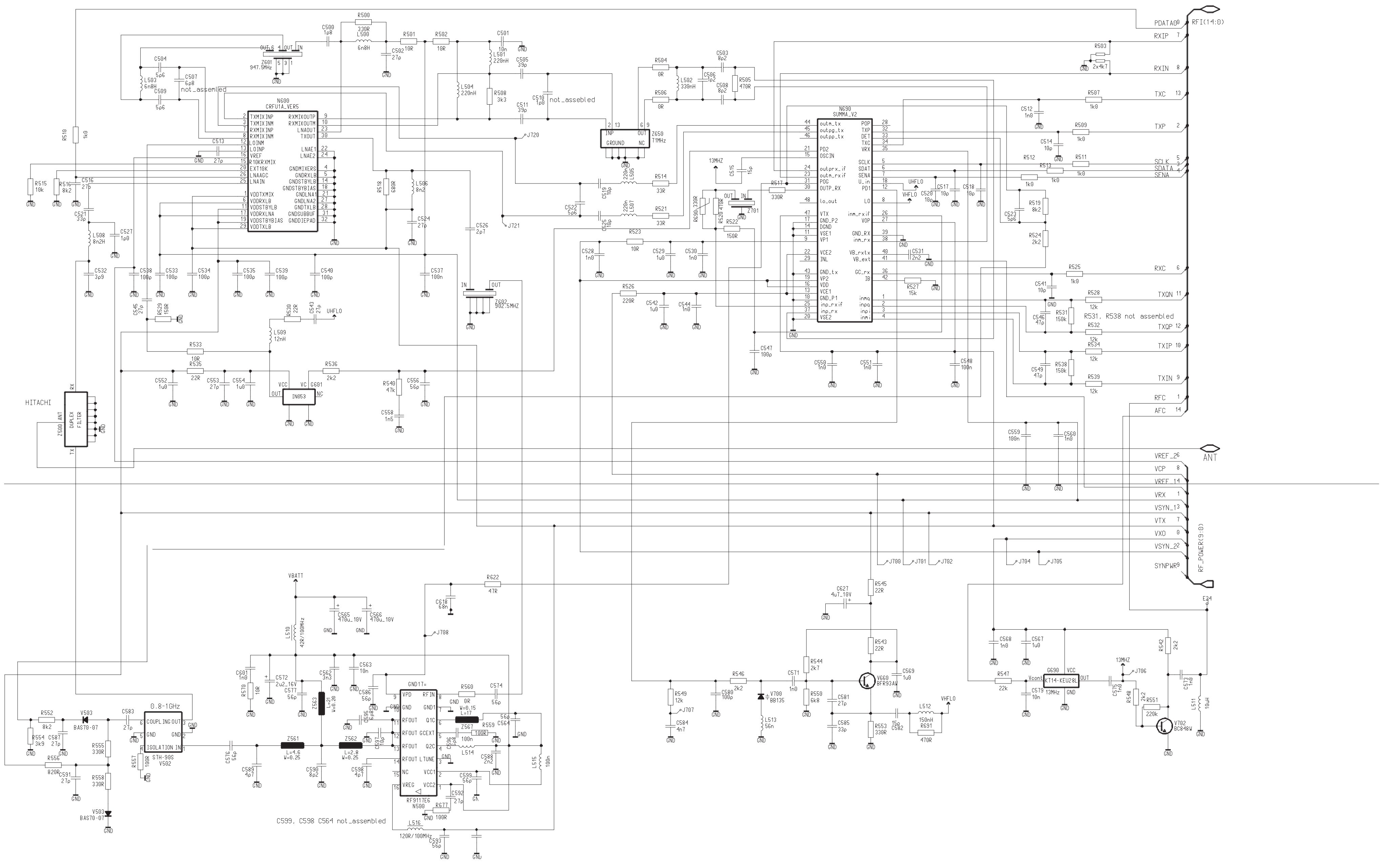
Parts Placement Diagram of BS2 2/2 (0.0) _09



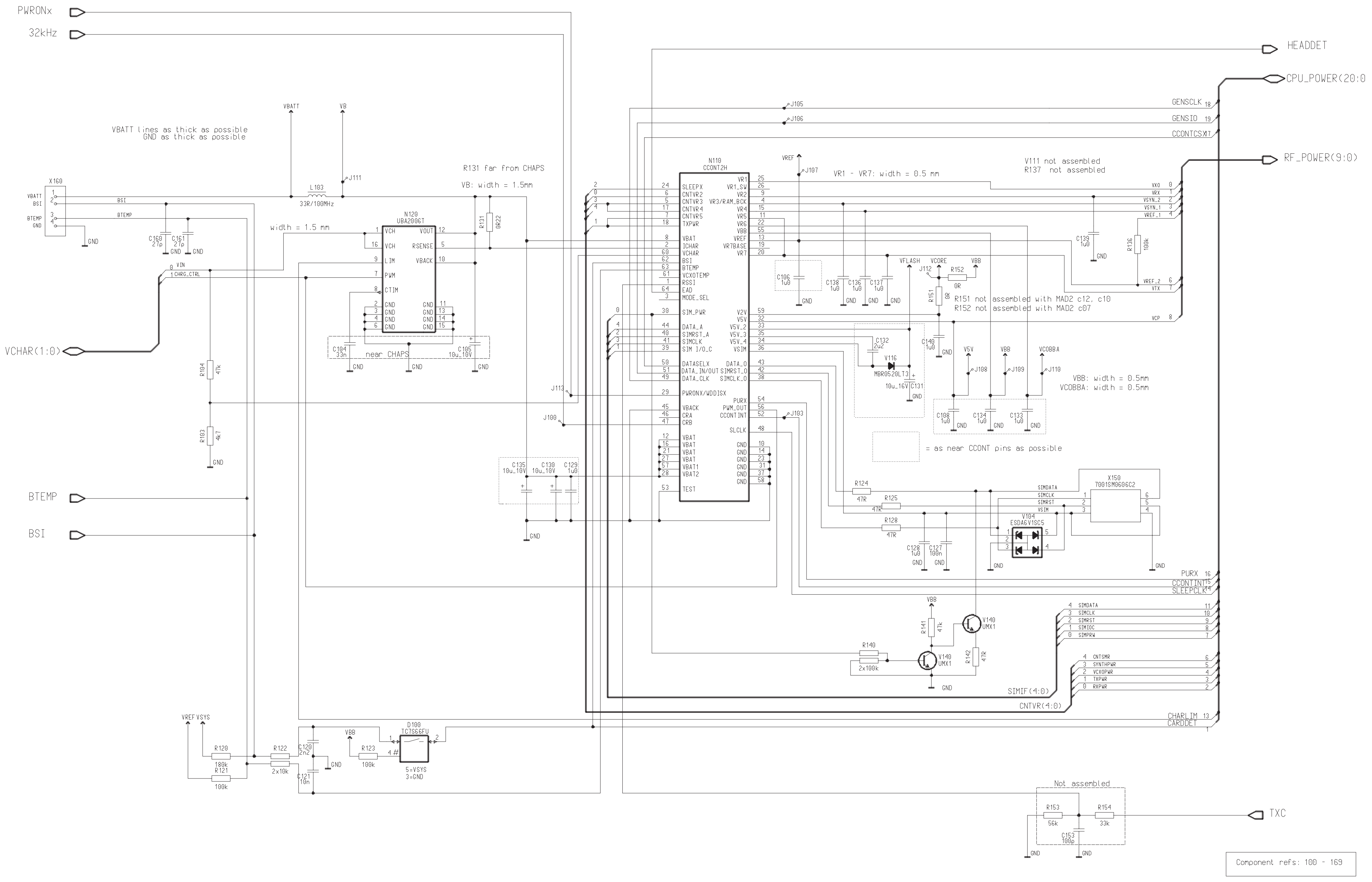
Block Diagram of BS8 (3.0 edit 57) v _09



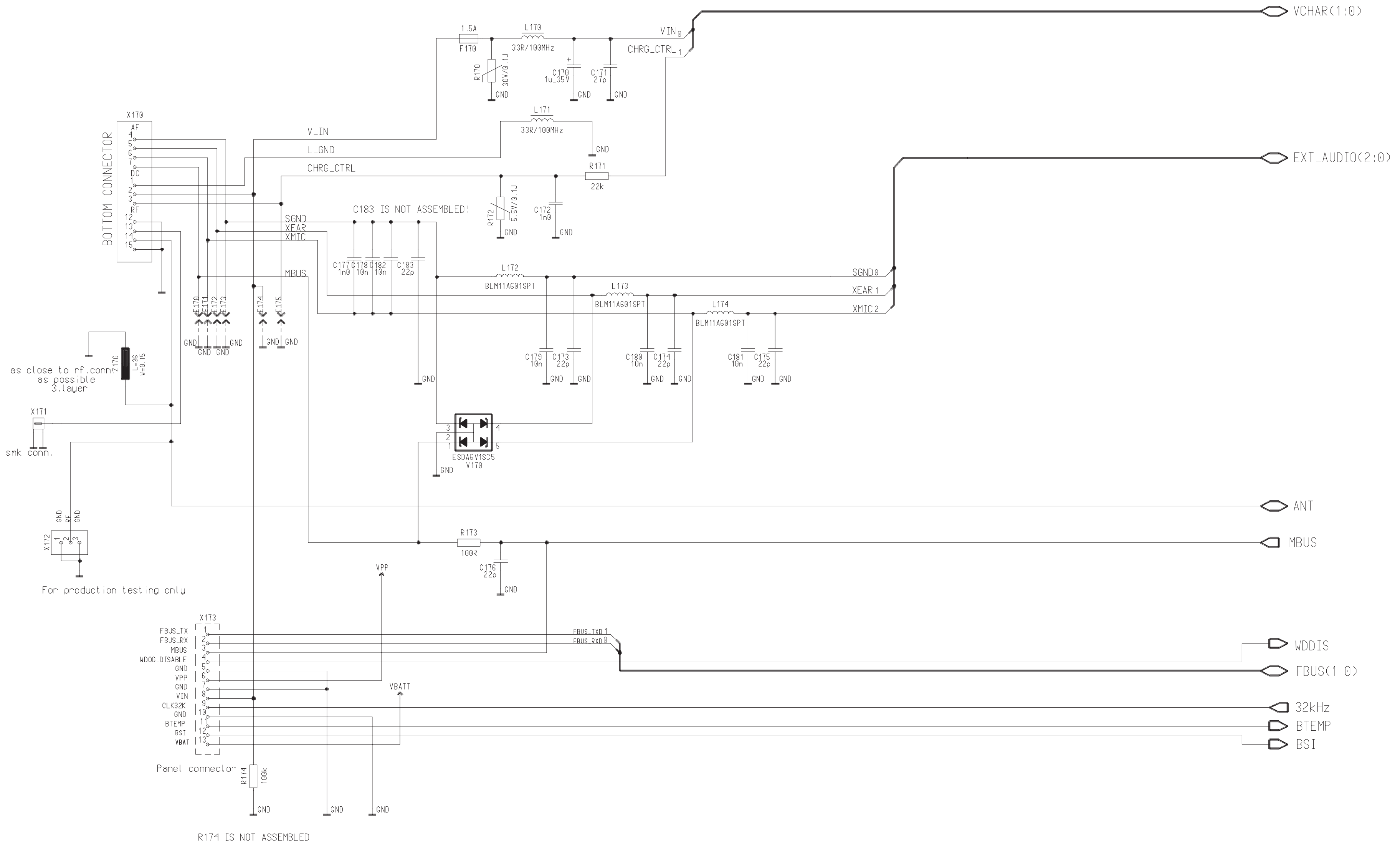
Circuit Diagram of BS8 GSM RF (2.0 Edit 104) _09



Circuit Diagram of BS8 CMT Power (3.1 Edit 111) _09

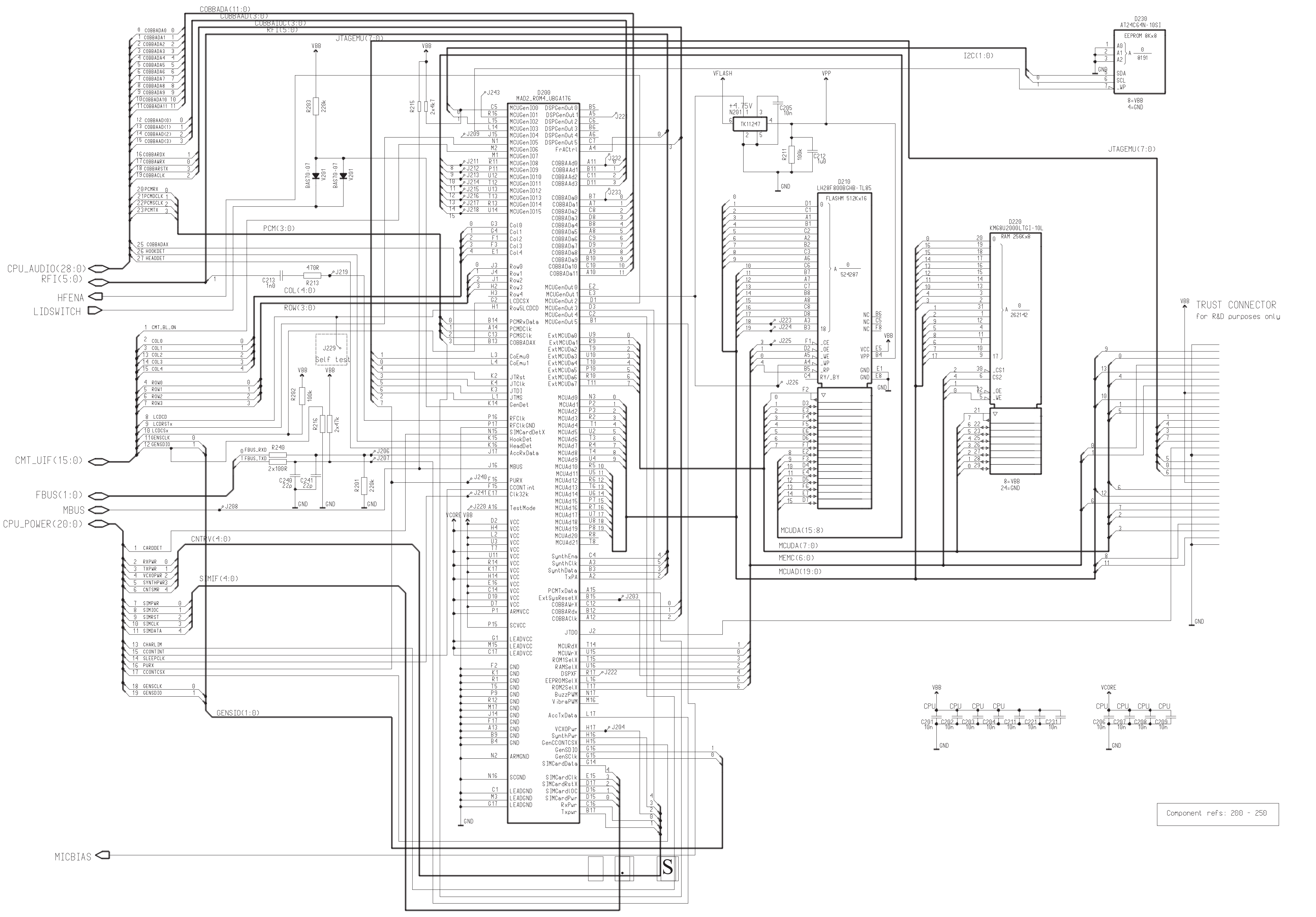


Circuit Diagram of BS8 System Connector (3.1 Edit 61) _09

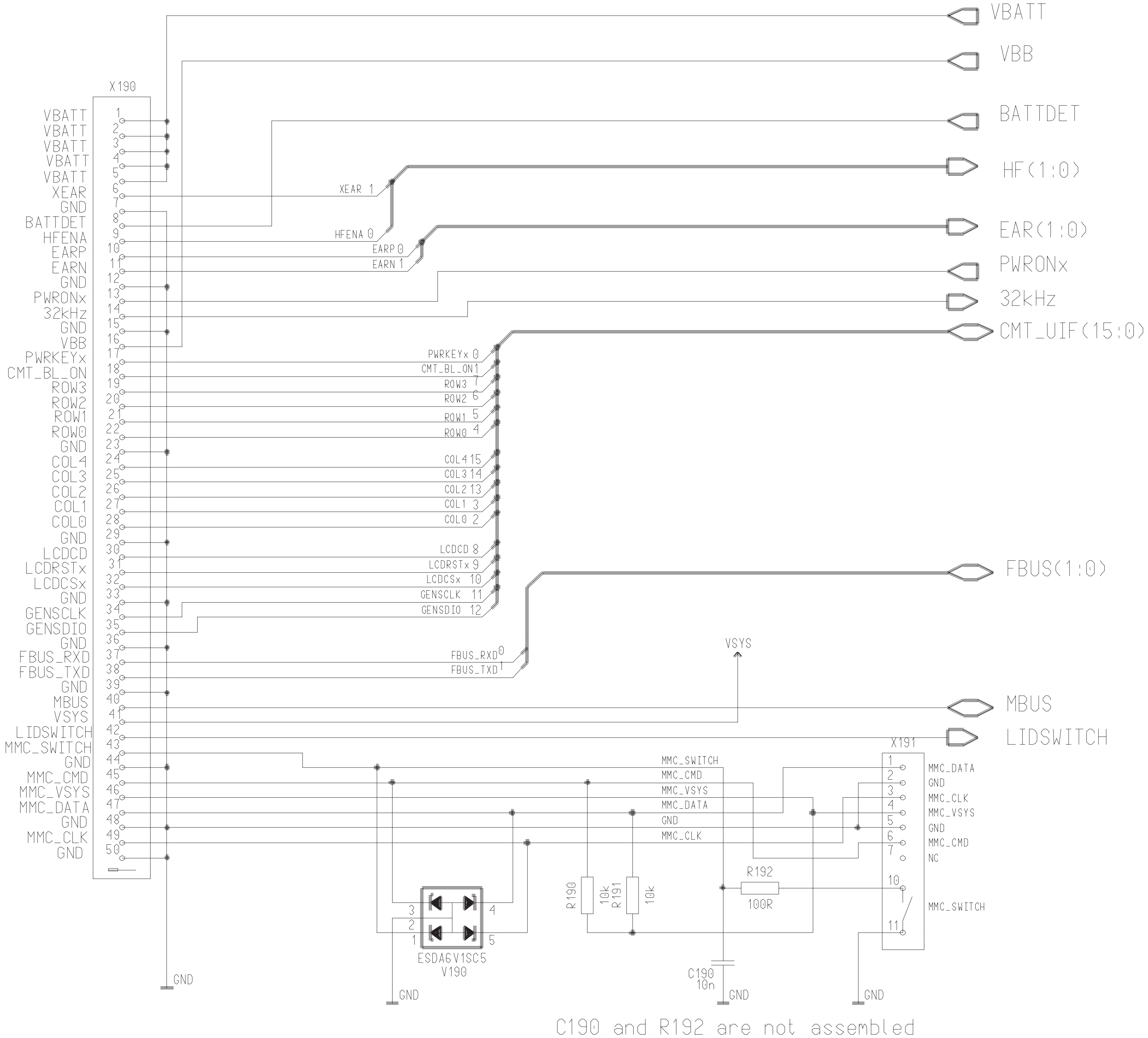


Component refs: 170 - 189

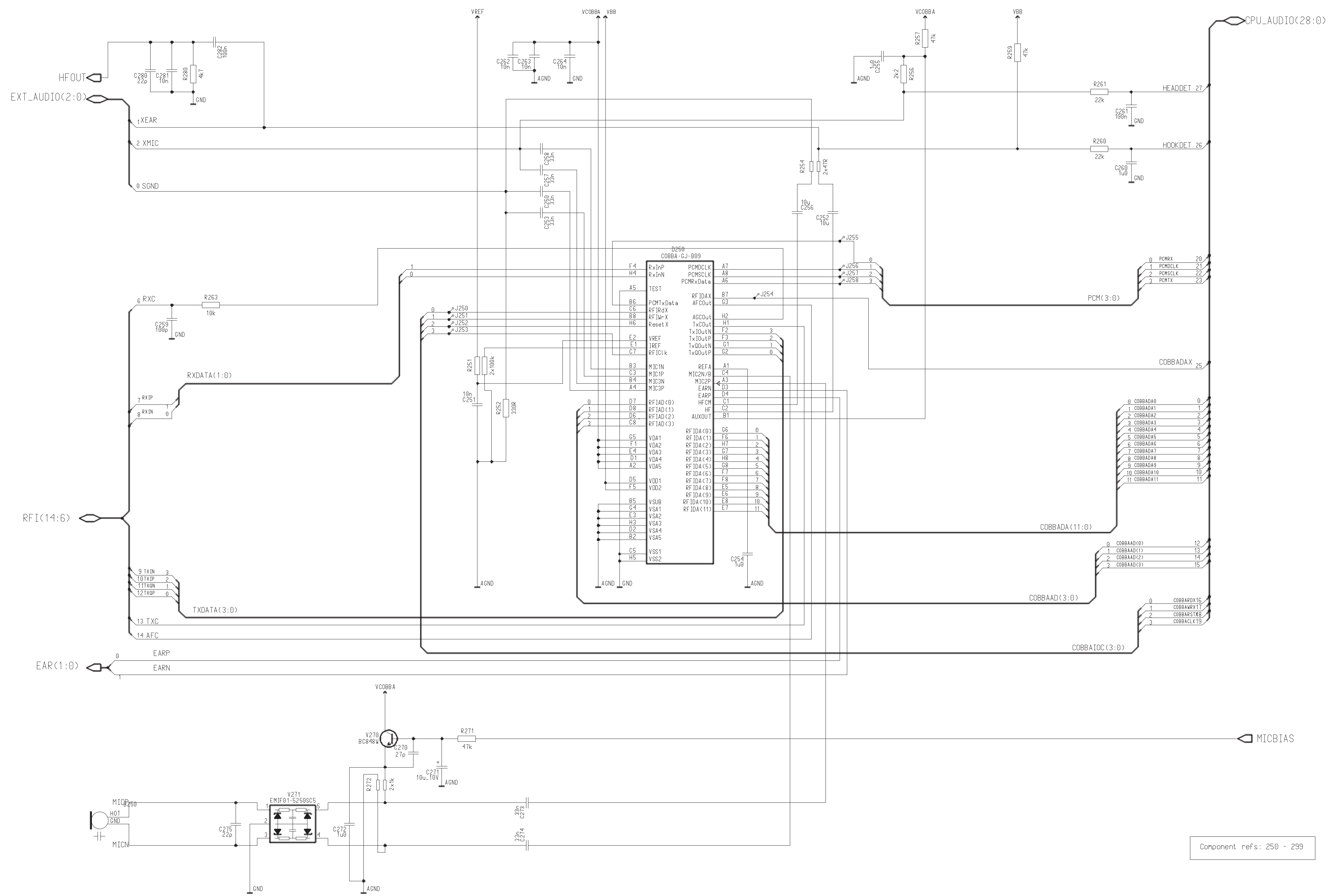
Circuit Diagram of BS8 CMT CPU (3.1 Edit 124) _09



Circuit Diagram of BS8 Baseband Connector (3.1 Edit 50) _09



Circuit Diagram of BS8 CMT Audio (3.1 Edit 79) _09



Parts Placement Diagram of BS2 _09