4. FUNCTIONAL DESCRIPTION

General

4.1 The 1603 SM is a SONET add/drop multiplexer that operates at either the OC3 (155.52 Mb/s) line rate, the OC12 (622.08 Mb/s) line rate, or the OC48 (2488.32Mb/s) line rate. The OC3/OC12 system can be configured for linear (terminal, add/drop or repeater) operation or Unidirectional Path Switched Ring (UPSR) operation for DS3, DS1, and STSn traffic and ATM VP ring functionality(VSCC501) for ATM traffic. The system configuration is software controlled and hardware specific. The OC48 configuration operates in the path switched mode only.
4.2 From the hardware perspective, the 1603 SM system consists of a mechanical shelf (SP101) that can be populated with a variety of plug-in units, depending on customer requirements. With the exception of the Ethernet LIF901 units and the LAN interface on NEP602, all plug-in units are temperature hardened for extended temperature operation.
4.3 The initial 1603 SM product used a slightly different mechanical shelf, the ADM150. The ADM150 shelf and the SP101 shelf have identical characteristics, except for the following:

- The ADM150 has an A-B switched power supply configuration. The SP101 has three power supplies in a load sharing arrangement.
- When using a drop group for synchronization purposes, the ADM150 must use drop group 1. The SP101 can use any of the three drop groups.
- The mechanical layout of the ADM150 does not permit installation of the Connnectorized DS1 Input/Output Panel (DS1CP). The SP101 supports the DS1CP I/O panels.
- The ADM150 shelf can only support one drop group equipped with either the LIF50x or LIF40x units. The remaining drop groups must either be equipped with DS1 asynchronous interfaces or left blank.

4.4 From a software perspective, the 1603 SM is shipped with a customer-specified software release designed to support features applicable to the installed hardware. This is described in greater detail later in this section.

ATM Transport Configuration

4.5 The 1603 SM system with OC3, OC12, or OC48 high speed interfaces may be initially equipped, or may be upgraded in-service, to provide ATM cell routing capability. The upgrade requires the VSCC501 cross-connect unit, the COA505, COA506 or the new COA60x Craft/Orderwire/Alarm unit, the HIFB0x or HIFC0x for STS3c-mapped OC3c line rate. The OC48 upgrade requires R09.00 or later system software.
4.6 The VSCC501 supports ATM payloads mapped into bandwidth at the STS1 or STS3c signal rate (see Figure 2). The ATM cell streams are transported internally by the VSCC501 to the ATM ROUTER function where individual ATM VP level cross-connections can be established. External to the VSCC501, there are different options available for providing transport of the STS1 or STS3c rate cell streams to and from the VSCC501. At the high speed interface modules the STS1 or STS3c payloads are path terminated to provide the

corresponding ATM cell data. At the drop interfaces, the ATM cell data is provided through SONET STS1 or STS3c path terminatation, DS3 path termination, or is based on Ethernet to ATM adaptation, all of which depends on the interfaces that are equipped.

Figure 2. VSCC Functional Block Diagram

4.7 The ATM VP cell routing function supports two high speed ports (East and West) and three configurable drop ports. The two ATM high speed ports are connected to any single STS1 or STS3c path from each of the high speed interface units.

4.8 The Line Group 1 high speed port can be provisioned to use either an STS1 or STS3c of the high speed bandwidth for transmitting and receiving ATM cell data. The Line Group 2 high speed port can be provisioned to use single STS1 or STS3c path to transmit and receive ATM cell data from the Line Group 2 high speed interface. For ring systems, Line Group 1 and Line Group 2 must be the same (STS1 or STS3c). The HIF10x/50x high speed units support STS1 ATM payloads only. All high speed OC12 units support STS1 or STS3c ATM payloads.

4.9 The SONET drop ports (OC3 or EC1 signals) may be provisioned to use an STS1 or STS3c (OC3 only) path to provide the corresponding bandwidth ATM cell stream to the VSCC501. Once a drop STS3c path is used for ATM payload, then no other drop STS1 or STS3c bandwidth is available on the VSCC501 for ATM traffic either in the same drop group or other drop groups.

4.10 The LIF901 drop unit converts Ethernet packets to ATM cells for either the STS1 or STS3c bandwidths. The LIF901 can map the ATM cells to either an ATM cell stream that is then routed directly to the VSCC501, or to a SONET path termination on the LIF901. In the first method (VSCC501 only), the ATM cell stream can be provisioned for STS1 or STS3 bandwidth. Once a drop STS3c path is used for ATM payload, then no other drop STS1 or STS3c bandwidth is available on the VSCC501 for ATM traffic either in the same drop group or other drop groups. In the second method, the SONET STS1 or STS3c payload is cross-connected to the LIF901 and the SONET payload is path terminated on the LIF901, and the ATM cells are then converted to Ethernet packets. In this case no ATM cell routing is performed on the VSCC501, and other cross-connect units such as the VSCC30x or VSCC101 (STS1 paths only) may be used.

4.11 The LIFB01 supports an ATM mapped DS3 payload and can map the ATM cells from the DS3 interface to either an ATM cell stream that is then routed directly to the VSCC501, or to a SONET path termination on the LIFB01. In the first method (VSCC501 only) the ATM cell stream is mapped using STS1 bandwidth. In the second method the SONET STS1 payload is cross-connected to the LIFB01 and the SONET payload is path terminated on the LIFB01, and the ATM cells are then mapped to the DS3 interface.

4.12 The ATM VP cell routing function of the VSCC501 implements both linear (Figure 3) and VP path switched unidirectional ring connections (Figure 4). The VP path switched uni-ring function is similar to the SONET VT uni-ring function; the fundamental difference is the ATM uni-ring protection mechanism switches ATM VP cell streams instead of SONET VTs. The STS1 or STS3c SONET paths, which transport these ATM cell streams between adjacent 1603 SMs with ATM cross-connects, are terminated at each ATM VP cross-connect, even though the ATM VP cell stream is not.

4.13 The centralized ATM VP cross-connect does not contain policing, traffic shaping, or ATM cell address translation functions. These functions are included in the ATM-specific drop modules, the LIF901 and the LIFB01.

Figure 3. Linear Network

Figure 4. Unidirectional Ring Network

ATM VP Unidirectional Rings with VSCC501

4.14 The VSCC501 provides ATM cell routing, ATM OAM and VP unidirectional ring protection switching functionality for the 1603 SM. The ATM VP uni-ring protection feature is implemented almost completely by the VSCC501 cross-connect module.

4.15 Unidirectional ring VP cross-connects are made up of ring constructs. These ring constructs can be a bridge, a selector, or drop-and-continue connections. A bridge construct (Figure 5) is a pair of one-way connections that must have the same source at the drop side. A bridge must also have its two destinations to the same time slot in opposite line sides.

Figure 5. Bridge Cross-Connect

4.16 A selector construct (Figure 6) is a pair of mutually exclusive one-way drop cross-connections that must have the same destination at the drop side. A selector must also have its source from the same time slots in opposite line sides.

Figure 6. Selector Cross-Connect

4.17 A 2WAYPR cross-connect (Figure 7) consists of a bridge and a selector that involve the same VP number on the drop and the line side ports. A 2WAYBR cross-connect consists of a one-way add, a drop-and-continue, and a selector, all of which involve the same VP number on the drop and the line side ports. The one-way is toward the source of the drop-and-continue cross-connect.

Figure 7. 2WAYPR and 2WAYBR Cross-Connect

4.18 The ATM cell streams can be made up of a mixture of unprotected VP connections. Unprotected VP connections are established using the ATM VP linear cell routing commands and uni-ring protected VP connections are established using the ATM VP uni-ring cell routing commands. Linear cross-connect commands are also used for provisioning through connections at intermediate NEs around the ring.

4.19 In the add direction, when a 2WAYPR VP connection is provisioned for ATM VP uni-ring protection switching, the non-idle cells from the incoming drop interface are duplicated, and a copy of each cell is routed to both Line Group 1 and Line Group 2 outgoing high speed interfaces.

4.20 In the drop direction, when a VP connection is provisioned for ATM VP uni-ring protection, the VSCC501 simultaneously monitors both the overall ATM cell streams and the ATM cells belonging to the protected VP connection from both Line Group 1 and Line Group 2 high speed interfaces.

4.21 The VSCC501 selects one of the redundant, ATM VP streams for routing to the drop interface on a per VP basis. The detection of ATM cell stream level fault events (Loss of Cell Delineation) or VP level fault events (VP AIS) initiates a VP level uni-ring switch for VPs provisioned for VP uni-ring protection. The source of these VP cell streams is switched from the faulty high speed interface to the redundant high speed interface.

4.22 The VP level uni-ring selectors can independently select each individual VP connection from either of the high speed interfaces. Therefore, all, none, or any subset of the VPs making up a dropped ATM VP cell stream can be sourced from the Line Group 1 high speed interface, with the remainder sourced from the Line Group 2 high speed interface.

4.23 For uni-ring VP connections, the VSCC501 continuously monitors both incoming ATM cell streams for relevant VP uni-ring switching triggers. The VSCC501 concurrently examines switching trigger conditions at two levels, the ATM cell stream level and the ATM VP level.

4.24 The ATM cell stream level trigger, monitored by the VSCC501, is Loss of Cell Delineation (LCD). This status is detected by the VSCC501 for each incoming ATM cell stream from both

high speed interfaces. An LCD fault event in the cell stream from one high speed interface initiates an attempt to switch all uni-ring protected VP connections to the ATM cell stream from the other redundant high speed interface.

4.25 The ATM VP level trigger, monitored by the VSCC501, is the VP AIS, which is an F4 end-to-end (VCI = 4) OAM flow. This status is detected by the VSCC501 individually for each VP. A fault event in the ATM VP level trigger on the cell stream from one high speed interface initiates an attempt to switch that single uni-ring protected VP connection to the cell stream from the other redundant high speed interface.

ATM Traffic Management

4.26 The 1603 SM ATM routing capabilities allow many different types of networks to use these capabilities. However, to get the most effective use from the 1603 SM ATM traffic, bandwidth utilization must be considered.

4.27 With the 1603 SM there are several interfaces that support ATM cell mapping that could be a source of ATM traffic into a ring or other type of network. The OC3 drop and EC1 (STS1 electrical) interfaces support ATM mapping. However, these interfaces are similar to the line group OC3 and OC12 interfaces in that they do not provide any traffic management functions. All the ATM cells arriving at these interfaces are forwarded to the ATM router on the cross-connect unit. If more cells arrive than can be routed to outgoing interfaces, then congestion occurs and the cells that cannot be routed are discarded. Traffic management for this situation has to occur at the source of the ATM traffic, external to the 1603 SM.

4.28 Interfaces on the 1603 SM that provide traffic management are the ATM mapped DS3 and Ethernet ATM interfaces. These interfaces can be provisioned to limit the amount of ATM traffic forwarded to the ATM router. By providing management at each interface, then the overall traffic entering the network can be managed. Enough flexibility is built into the provisioning to allow for different types of traffic and a wide range of control.

Usage Parameter Control/Network Parameter Control/Source Control

4.29 The control of ATM cell traffic is implemented using standard ATM Usage Parameter Control (UPC) and Network Parameter Control (NPC) capabilities. Usage Parameter Control is defined as a set of actions taken by an ATM switch to monitor and control traffic at a UNI interface in terms of the traffic offered to the network over an ATM connection. Network Parameter Control is defined as the set of actions taken by an ATM switch to monitor and control traffic at an NNI interface in terms of traffic offered to the network from another network over an ATM connection. In the 1603 SM, the UPC/NPC function monitors ATM traffic received on a VP connection and verifies that the VP connection adheres to the assigned usage limits at a UNI/NNI, respectively. If a connection violates the usage limits, the violating cells are provisionally tagged or discarded. These actions are collectively and commonly referred to as policing.

4.30 The same UPC/NPC ATM traffic management mechanisms are also used to describe and manage the generation of ATM VP cells at ATM connection origination points. Use of the UPC/NPC ATM cell algorithms at ATM cell origination points, differs only in that there is no need for the ATM cell discard function at the origination NE. The scheduling algorithm ensures that the ATM cell generation characteristics are compliant with the provisioned ATM VP usage limits.

ATM Cell Policing and Scheduling

4.31 ATM cell policing and scheduling functions use one or more instances of the Generic Cell Rate Algorithm (GCRA). The GCRA is an algorithm for generating or measuring compliance to provisioned ATM VP usage limits. The same GCRA can be described as either a virtual scheduling algorithm or as a continuous-state leaky bucket algorithm. The flowcharts for both GCRA algorithms are shown in Figure 8. Once policing or scheduling is activated on a VP connection, each cell is evaluated or scheduled based on the GCRA algorithm assigned to that VP. In policing applications, cells, which do not conform to the provisioned policing algorithm, are tagged (CLP changed from 0 to 1) or discarded, depending on the provisioning of the ATM VP connection.

Figure 8. Equivalent Versions of the Generic Cell Rate Algorithm

4.32 Multiple instances of the GCRA with possibly different Increment (I) and Limit (L) parameters may be applied to the cell flow. A cell is then conforming only if it conforms to all instances of the GCRA. The state of a particular instance of the GCRA is updated only by the cells that conform to that instance of the GCRA.

Path Profile Types

4.33 Path profile types organize the parameters necessary to support the GCRA algorithms for the various ATM service categories or traffic models. The 1603 SM supports six different traffic profiles of which four are relevant to policing at intermediate NEs, and two are relevant to ATM connection sources. The parameters that make up the path profiles are combinations of Peak Cell Rate (PCR) , a Cell Delay Variation Tolerance (CDVT) , Sustained Cell Rate (SCR) and Maximum Burst Size (MBS). Table C lists the six path profile types.

Table C. Profile Types for ATM Cell Policing

PROFILE TYPE	PCR0[1]	PCR0+1[2]	CDVT [3]	SCR [4]	SCR+1 [5]	MBS0 [6]	MBS0+1 [7]	GCRA [8]
1	-	X	X	-	-	-	-	1
2	-	X	X	-	X	-	X	2
3	-	X	X	X	-	X	-	2
4	X	X	X	-	-	-	-	2
5 [9]	-	X	-	-	-	-	-	1
6 [9]	-	X	-	-	X	-	X	2

[1]PCR0 = Peak Cell Rate of High Priority Cells (CLP=0)
[2]PCR0+1 = Peak Cell Rate of All Cells (CLP=0 and 1)
[3]CDVT = Cell Delay Variation Tolerance
[4]SCR = Sustained Cell Rate of High Priority Cells (CLP=0
[5]SCR+1 = Sustained Cell Rate of All Cells (CLP=0 and 1)
[6]MBS0 = Maximum Burst Size of High Priority Cells (CLP=0)
[7]MBS0+1 = Maximum Burst Size of All Cells (CLP=0 and 1)
[8]GCRA = Number of Instances of the GCRA Algorithm in the Profile Type
[9]Profile Types For ATM Cell Sources

4.34 Policing an ATM VP connection at the DS3 ATM interface is implemented using one of Profile Types 1 through 4 listed in Table C. An ATM VP connection source in the Ethernet ATM unit is described using Profile Type 5 or Profile Type 6. Each profile type uses two or more parameters specified in Table C. All profile types that use more than one parameter, exhibit an

order in which the parameters are applied. This order is represented in Table C by assigning the first parameter evaluated in the leftmost column and listing the remaining parameters in descending order of evaluation from left to right. Therefore, the Peak Cell Rate of cells with a cell loss priority of 0 (high priority cells) are evaluated for conformance first, the Peak Cell Rate of all cells (PCR0+1) next and so on.

Peak Cell Rate

4.35 Peak cell rate is specified in cells per second. Appropriate values for peak cell rate depend on whether the service offering is based on the maximum ATM cell rate of the ATM link that the ATM connection transits, or the maximum user payload promised to the subscriber.

4.36 When provisioning peak cell rates for ATM VP connections on the DS3 ATM unit, the cell rate should be selected such that the ATM VP connection is policed at a rate equal to or greater than the maximum cell generation rate of the ATM VP connection source (source of ATM cells into the DS3 ATM interface) and that the connection is policed at less than the capacity of the ATM connection path (cells exiting the DS3 ATM interface towards the ATM router). The maximum generation cell rate of the ATM VP connection source could be determined by either the source itself (established by the source contract), or the bandwidth of the ATM link to the source (established by the maximum utilized bandwidth of the link to the source). The capacity of the ATM connection path toward the ATM router can be established in two ways. The first is where the capacity is established by contract (e.g., a customer subscribes to 1.544 Mbits/sec path using the DS3 ATM interface). The second is where the capacity is established by the ATM link itself (e.g., a customer has an STS1 connection to the service provider of which the entire bandwidth is intended for use).

4.37 When provisioning peak cell rates for ATM VP connection sources on the Ethernet ATM unit, the cell rate should be selected so that the ATM cells are generated at a rate that does not exceed the capacity of the ATM connection path. The capacity of the ATM connection path can be established in two ways. The first is where the capacity is established by contract (e.g., a customer subscribes to 5 Mbits/sec). The second is where the capacity is established by the ATM link itself (e.g., entire bandwidth of an STS1 connection is intended for use by the ATM connection).

4.38 Table D shows the relationship between some familiar transmission rates (TDM and ATM) and appropriate ATM peak cell rates. The top portion of Table D lists peak cell rates for various ATM links used to transport ATM cells. The bottom portion of Table D lists peak cell rates for various ATM services (or subscriptions). When using data from this table, keep in mind that an ATM link can carry more that than one ATM service. For 1603 SM, an ATM service is associated with each individual VP.

4.39 The values in Table D satisfy the requirements of standards organizations and provide excellent guidance for the provisioning of this parameter. These values include estimated bandwidth needed for OAM cells in addition to the user cells, shown in different columns in Table D. The 1603 SM allows the peak and sustained cell rate parameters to be provisioned to any value between 100 and 353,207 cells per second, inclusive. This allows the service provider the freedom to offer these standard application rates, as well as other ones not currently specified by standards organizations.

Table D. ATM Peak and Sustained Cell Rates

APPLICATION	PCR OR SCR VALUE [1]	ATM CELL BANDWIDTH	USER CELLS [1]	OAM CELLS [1]	USER PAYLOAD [3][4]

		[2][3]			
ATM MAPPED LINKS					
56 kbit Link	133	56,000	131	2	50,304
n x 56 kbit Link	n x 133	n x 56,000	n x 131	n x 2	n x 50,304
DS0 Link	152	64,000	150	2	57,600
n x DS0 Link	n x 152	n x 64,000	n x 150	n x 2	n x 57,600
Framed DS1 Link	3,622	1,536,000	3,593	29	1,379,712
n x Framed DS1 Link	n x 3,622	n x 1,536,000	n x 3,593	n x 29	n x 1,379,712
Unframed DS1 Link	3,642	1,544,000	3,613	29	1,387,392
n x Unframed DS1 Link	n x 3,642	n x 1,544,000	n x 3,613	n x 29	n x 1,387,392
DS3 PLCP Link	96,000	40,704,000	95,254	746	36,577,536
DS3 Direct Mapping Link	104,268	44,209,694	103,448	820	39,724,032
STS1 Link	114,113	48,384,000	113,219	894	43,476,176
STS3c Link	353,207	149,760,000	350,467	2,740	134,579,000
SERVICES USING ATM					
56 kbit User	152	64,448	150	2	57,600
n x 56 kbit User	n x 152	n x 64,448	n x 150	n x 2	n x 57,600
DS0 User	173	73,352	171	2	65,664
n x DS0 User (n=1-23)	n x 173	n x 73,352	n x 171	n x 2	n x 65,664
n x 256 kbit/second User (n=7-47) [5]	n x 690	n x 292,560	n x 682	n x 8	n x 261,888
DS1 User	4,140	1,755,360	4107	33	1,577,088
n x DS1 User (n=1-23) (n=24-85)	n x 4,140	n x 1,755,360	n x 4107	n x 33	n x 1,577,088
DS3 User (CBR)	119,910	50,841,840	118,979	931	45,687,936
n x DS3 User (CBR) (n=1-2)	n x 119,910	n x 50,841,840	n x 118,979	n x 931	n x 45,687,936
DS3 User (VBR)	120,060	50,905,440	119,128	932	45,745,152
10 Mbit Ethernet [6]	26,623	11,288,000	26,416	207	11,200,338
10 Mbit Ethernet [7]	26,905	11,408,000	26,695	209	11,319,067
10 Mbit Ethernet Maximum	34,673	14,701,000	34,404	269	14,587,200

100 Mbit Ethernet [6]	266,229	112,880,000	264,159	2,070	112,003,381
100 Mbit Ethernet [7]	269,049	114,080,000	266,959	2,090	113,190,666
100 Mbit Ethernet Maximum	346,727	147,010,000	344,037	2,690	145,872,000
n x 1 Mbit Ethernet Average	n x 2627	n x 1,113,424	n x 2605	n x 22	n x 1,000,320
n x 1 Mbit Ethernet Average link utilization	n x 2358	n x 1,000,000	n x 2338	n x 20	n x 987,792

[1]Cells per second.
[2]Total or average.
[3]Bits per second.
[4]Maximum or maximum average.
[5]Telcordia excludes values which are divisible by 6.
[6]Maximum median.
[7]Maximum average.

Cell Delay Variation Tolerance

4.40 Cell Delay Variation Tolerance (CDVT) is a parameter associated with ATM cell policing profile types. It is not used by ATM cell sources. This parameter establishes the maximum variation in cell delay that is tolerated when policing an ATM connection. ATM cells on a policed VP connection that are non-compliant with the provisioned CDVT are tagged or discarded.
4.41 A summary of standard CDVT values is summarized in Table E. The 1603 SM supports all of the CDVT values shown.

Table E. Required NPC and UPC CDVT Values

CDVT FOR DS3 BASED UNI [1]	CDVT FOR DS3 BASED NNI [2]	CDVT FOR STS3c OR STS12c BASED UNI [1]	CDVT FOR STS3c OR STS12c BASED NNI [2]
-	-	50 microseconds	50 microseconds
100 microseconds	100 microseconds	100 microseconds	100 microseconds
150 microseconds	150 microseconds	150 microseconds	150 microseconds
200 microseconds	200 microseconds	200 microseconds	200 microseconds
250 microseconds	250 microseconds	250 microseconds	250 microseconds
350 microseconds	350 microseconds	-	350 microseconds
500 microseconds	500 microseconds	-	500 microseconds
-	700 microseconds	-	700 microseconds
-	1,000 microseconds	-	1,000 microseconds
-	1,400 microseconds	-	-
-	2,000 microseconds	-	-

[1]UPC function.
[2]NPC function

4.42 For STS1 based UNI and NNI interfaces, data from Table E for the DS3 can be used

(requirements documents do not provide specifications for the STS1 signal).
4.43 As of January 1999, there are no requirement documents that specify which CDVT values to use for a given application. The appropriate value of CDVT is dependent on the characteristics of both the service and the network. The size of the network, the number of subscribers and the ATM bandwidth utilization affect CDVT. A guideline for selecting CDVT is that the CDVT value can be lowest near the ATM source and higher when located many ATM NEs from the ATM source. Data from Table E can be used with the DS3 ATM based VP connections, any of the possible values in the table can be specified, but the first two columns were intended for the DS3 applications.

Maximum Burst Size

4.44 Maximum Burst Size (MBS) is a parameter associated with variable bit rate (VBR) service categories. MBS is not used by constant bit rate (CBR) service categories. The MBS parameter establishes the maximum number of cells, in a burst of ATM cells, that are allowed to exceed the sustained cell rate and achieve the peak cell rate. Maximum burst size is used in conjunction with Sustained Cell Rate (SCR) to attempt to more efficiently utilize network resources.
4.45 Selecting appropriate values for maximum burst size depends on both the network and the service offering. In general, the criteria used to establish a useful maximum burst size is to set the maximum burst size to a value that allows one or more complete information units (packets, PDUs, etc.) to enter or transit the ATM network at the peak cell rate, without causing a degradation in overall network performance. The 1603 SM supports the fixed set of maximum burst size options listed in Table F.

Table F. Maximum Burst Sixe (MBS) Values Supported by the 1603 SM

MAXIMUM BURST SIZE	SERVICE INFORMATION UNIT
32 Cells	Maximum Length Ethernet Packet (1518 Byte)
50 Cells	
100 Cells	
150 Cells	
210 Cells	Maximum Length Subscriber Interface Protocol (SIP) Level 3 Protocol Data Unit (L3_PDU)

Sustained Cell Rate

4.46 Sustained Cell Rate (SCR) is a parameter associated with variable bit rate (VBR) service categories. SCR is not used by constant bit rate (CBR) service categories. The SCR parameter establishes the average rate of a connection in cells per second. Sustained cell rate is used in conjunction with maximum burst size to attempt to more efficiently utilize network resources. Allowed SCR values result in the same relationships between service offerings and sustained cell rate values as with peak cell rate relationships. Therefore, the methods described in paragraphs 4.35 through 4.39 and values from Table D can be used to establish the appropriate sustained cell rate values as well as appropriate peak cell rate values.
4.47 While the sustained cell rate values in Table D satisfy values required by standards organizations and provides guidance for the provisioning of this parameter, the 1603 SM allows the sustained cell rate parameter to be set to any value between 100 and 353,207, inclusive. However, service providers must make certain that the sustained cell rate is always less than the peak cell rate. The flexible range of values for sustained cell rate allows service providers

the freedom to establish service offerings other than the ones specified by standards organizations.

Service Categories

4.48 Table G lists the correspondence between standardized ATM service categories and the 1603 SM profile types. The ATM Forum has defined several variations of CBR and VBR traffic that are listed in Table G for reference.

Table G. Profile Type to Service Category Cross-Reference

PROFILE TYPE	ATM FORUM TRAFFIC MANAGEMENT 4.0	ATM FORUM UNI 3.1
1	CBR.1 [1]	CBR.A, VBR.B [1][2]
2	VBR.1 [2]	VBR.C [2]
3	VBR.2, VBR.3 [2]	VBR.2, VBR.3 [2]
4		CBR.B, VBR.A [1][2]
[1]CBR = Constant Bit Rate. *[2]VBR = Variable Bit Rate.*		

Traffic Descriptors

4.49 A traffic descriptor is a mechanism used to associate an ATM policing or scheduling profile with an ATM VP connection in 1603 SM. A service provider can create a traffic descriptor for each ATM service offering. An example of an ATM service offering would be a DS1 equivalent rate CBR service. Other obvious potential traffic descriptors would be for service offerings of CBR and VBR service categories at DS0, n x DS0, DS1, n x DS1 or DS3 bandwidths.

4.50 Each NE supports 32 unique traffic descriptors that can be used with each individual DS3 ATM VP and Ethernet ATM VP. Every VP used with the DS3 ATM interface is not required to have a traffic descriptor associated with it. If none is specified, then no policing is performed on that VP. For every Ethernet ATM VP, a traffic descriptor is required.

4.51 The same traffic descriptor can be used for many VPs. Refer to Table H for information provisioned with each descriptor.

Table H. Traffic Descriptior Provisioning

FIELD	DESCRIPTION	ALLOWED VALUES
DESCRIPTOR NAME	User name associated with traffic descriptor	1..32 Noncase-sensitive Alphanumeric characters
PROFILE TYPE	Profile indication	PT1, PT2, PT3, PT4, PT5, PT6
PCR0	Peak Cell Rate of High Priority Cells (CLP=0) in cells per second	100..353207
PCR0+1	Peak Cell Rate of All Cells (CLP=0 and 1) in cells per second	100..353207
CDVT	Cell Delay Variation Tolerance in microseconds	50, 100, 150, 200, 250, 350, 500, 700, 1000, 1400, 2000
SCR0	Sustained Cell Rate of High Priority Cells (CLP=0) in cells per second	100..353207

SCR0+1	Sustained Cell Rate of All Cells (CLP=0 and 1) in cells per second	100..353207
MBS0	Maximum Burst Size of High Priority Cells (CLP=0) in number of cells	32, 50, 100, 150, 210
MBS0+1	Maximum Burst Size of All Cells (CLP=0 and 1) in number of cells	32, 50, 100, 150, 210
Discard Non-conformant Cells	Discard or tag non-conformant cells (applicable to DS3 ATM only)	Y (Yes), N (No)

ATM VP Connection Policing with the DS3 ATM Interface

4.52 The DS3 ATM interface is never an ATM source. This interface is always an ATM policing point (although policing can be disabled). The DS3 ATM interface uses traffic descriptors with profile types 1, 2, 3 or 4 (refer to Table C). Profile types 1 and 4 are used for constant bit rate services and profile types 2 and 3 are used for variable bit rate services.

4.53 Refer to Table D for peak and sustained cell rates for typical service offerings for the DS3 ATM interface. These services originated elsewhere and are being carried by the DS3 ATM interface into the network through a VP connection. This connection may ultimately be transported using several ATM mapped links in the network to its destination.

4.54 The DS3 ATM interface can support 512 VP connections. Policing at the DS3 ATM interface can be used to enforce ATM cell conformance on each VP for the end service being provided (bottom portion of Table D) or to enforce the bandwidth capabilities of the links used to transport the service to its destination (top portion of Table D). When operating the DS3 ATM interface at the maximum ATM bandwidth, the DS3 can be provisioned to operate in either the DS3 PLCP or DS3 direct mapping ATM formats. The maximum peak and sustained cell rates of these two link formats are different. Table D shows the maximum ATM cell rates each of these link formats support.

4.55 Constant bit rate traffic descriptors are used for applications where the ATM subscriber wishes to utilize all of the provisioned bandwidth available for a given rate. Therefore, the policed peak cell rate of the link to the subscriber establishes the maximum ATM bandwidth. Peak cell rates for all cells (PCR0+1) and cell delay variation tolerance (CDVT) must be specified for constant bit rate connections using profile type 1. Peak cell rates for high priority cells (PCR0), peak cell rates for all cells (PCR0+1) and cell delay variation tolerance (CDVT) must be specified for constant bit rate connections using profile type 4.

4.56 Variable bit rate traffic descriptors are used for applications where the ATM subscriber knows the traffic generated by the ATM source has an average rate, which is far less than the peak rate. Network providers can attempt to more efficiently utilize network resources for these subscribers by defining and assigning a variable bit rate traffic descriptor to the associated VP's. Peak cell rates for all cells (PCR0+1), cell delay variation tolerance (CDVT), sustained cell rate for all cells (SCR0+1) and maximum burst size (MBS0+1) for all cells must be specified for variable bit rate connections using profile type 2. Peak cell rates for all cells (PCR0+1), cell delay variation tolerance (CDVT), sustained cell rate for high priority cells (SCR0) and maximum burst size for high priority cells (MBS0) must be specified for variable bit rate connections using profile type 3.

4.57 When establishing variable bit rate traffic descriptors for the DS3 ATM interface, values for maximum burst size must be provisioned. The maximum burst size values supported are listed in Table F. The DS3 ATM interface supports traffic descriptors with maximum burst sizes for either all cells (profile type 2) or for high priority cells (profile type 3). The performance of the DS3 ATM interface when experiencing bursty traffic can be enhanced by selecting larger maximum burst sizes. However, these larger maximum burst sizes increase the likelihood of network ATM cell loss due to the temporary congestion that bursty traffic generates.
4.58 Cell delay variation tolerance must be specified for all policing traffic descriptors. Table E lists the values for CDVT, which DS3 ATM interfaces are required to support. All of the CDVT values specified in Table E are supported by 1603 SM.

ATM VP Connection Sourcing for the Ethernet ATM Interface

4.59 An Ethernet ATM interface is always an ATM source interface. Therefore, an Ethernet ATM interface uses traffic descriptors with profile types 5 or 6. Profile type 5 is used for constant bit rate services and profile type 6 is used for variable bit rate services.
4.60 Refer to Table D for peak and sustained cell rates for typical service offerings that can be offered using the Ethernet ATM interfaces. The range of appropriate peak and sustained cell rates depend on whether the unit is provisioned to interface one, two, three, or four 10Mbit Ethernet interfaces or a single 100 Mbit Ethernet interface.
4.61 Traffic descriptors can be used to enforce ATM cell conformance to the Ethernet bandwidth being provided (bottom portion of Table D) or to enforce the bandwidth capabilities of the links used to transport the service to its destination (top portion of Table D). The Ethernet ATM unit can be provisioned for STS1 or STS3c link bandwidth to carry ATM traffic from the combined Ethernet interfaces. The ATM cells can be sent to the ATM router or directly mapped into a STS1 or STS3c path.
4.62 When the Ethernet ATM unit is provisioned with one, to four active 10 Mbit Ethernet interfaces, the absolute maximum ATM cell bandwidth, which can be generated by any single 10 Mbit Ethernet, is approximately 14.701 Mbits. Therefore, one, two or three 10 Mbit Ethernet interfaces can be interfaced using a STS1 link. However, if all four 10 Mbit Ethernet interfaces are provisioned at the maximum bandwidth, the 48.384 Mbits/second STS1 link bandwidth could be exceeded. In this case, an STS3c path must be used.
4.63 When the Ethernet ATM unit is provisioned as a single 100 Mbit Ethernet interface, the absolute maximum ATM cell bandwidth generated by the single 100 Mb/s Ethernet is approximately 147.010 Mb/s. When provisioning a peak cell rate up to 48.384 Mb/s an STS1 path can be used. However, when provisioning peak cell rates resulting in ATM bandwidths between 48.384 Mb/second and 147.010 Mb/s an STS3c must be used.
4.64 Constant bit rate traffic descriptors are used for applications where the ATM subscriber wishes to use all of the provisioned bandwidth available. Therefore, the policed peak cell rate of the link to the subscriber establishes the maximum ATM bandwidth. Peak cell rates for all cells (PCR0+1) must be specified for constant bit rate connections using profile type 5.
4.65 Variable bit rate traffic descriptors are used for applications where the ATM subscriber knows the traffic generated by the ATM source has an average rate that is far less than the peak rate. Network providers can attempt to more efficiently utilize network resources for these subscribers, by defining and assigning a variable bit rate traffic descriptor to these subscribers. Peak cell rates for all cells (PCR0+1), sustained cell rate for all cells (SCR0+1) and maximum burst size for all cells (MBS0+1) must be specified for variable bit rate connections using profile type 6.

4.66 When establishing variable bit rate traffic descriptors for an Ethernet ATM interface, values for maximum burst size must be provisioned. The maximum burst size values supported are listed in Table F. The performance of the Ethernet ATM interface when experiencing bursty traffic can be enhanced by selecting larger maximum burst sizes. However, these larger maximum burst sizes increase the likelihood of network ATM cell loss due to the temporary congestion that bursty traffic generates.

Traffic Routing Description (OC3 Configuration)

4.67 Figure 9 is a block diagram of a 1603 SM system configured with high speed interface (HIF) line groups, VT/STS cross-connects (VSCC), and low speed drop group interfaces. The optical carrier (OC3) signals are interfaced to the system using the line groups.

Figure 9. 1603 SM OC3 Functional Block Diagram

4.68 Both Line Group 1 and Line Group 2 OC3 interfaces contain transmit and receive functions. The HIF plug-in unit converts the incoming OC3 optic signals into 155.52-Mb/s electrical signals. The HIF also contains framing circuits and the pointer processor. The pointer processor may be provisioned for VT/DS1, STS1, or STS3c (HIFB0x/C0x) payload processing. If provisioned for VT/DS1, the pointer processor reads in the STS1 pointers, sets them to zero and reflects the difference into the VT pointers. If provisioned for STS1 or STS3c payload, it reads in the STS1/STS3c pointer, and adjusts (offsets) the pointer on output (non-terminated STS1/STS3c only) to account for differences between line rate and the Network Element (NE) clock.

4.69 The VT/STS1/STS3c cross-connect (VSCC30x or VSCC501) is a nonblocking (i.e., any port to any port) VT-based cross-connect. The VSCC provides symmetrical grooming to/from Line Group 1, Line Group 2, and the three drop groups. Each of the OC3 payload STS1 signals can be provisioned for either VT/DS1 or STS1 grooming. The entire OC3 payload can be provisioned for STS3.

NOTE: *The 1603 SM can be equipped with either fixed-path cross-connects or the variable (software-provisionable) cross-connect. However, only the variable cross-connects support Time Slot Interchange (TSI) functionality. The variable cross-connect also supports local grooming, which means an STS1 or VT1.5 in one drop group can be cross-connected to a different STS1 or VT1.5 in another drop group.*

4.70 Figure 10 shows an OC3 configuration using the variable cross-connects. When cross-connecting STS1 signals, the VSCC can connect any of the three STS1 payload signals from either Line Group 1 or Line Group 2 interfaces to the other high speed port or to one of the three possible STS1 drop groups. The drop groups are configured for the different interface requirements. When cross-connecting VTs, the variable cross-connect can connect different combinations of the 84 possible VTs from either Line Group 1 or Line Group 2 interfaces to other VT locations in the other high speed port or in the three drop groups.

Figure 10. OC3 Time Slot Interchange Matrix

NOTE: *If the 1603 SM is equipped with fixed-path cross-connects, VT1.5 signals must be cross-connected in STS1 bundles (i.e., 28 DS1 signals). However, if the 1603 SM is equipped with the variable cross-connect, VT1.5 signals can be cross-connected individually, provided STS1 cross-connections have not already been made.*

Traffic Routing Description (OC12 Configuration)

4.71 As shown in Figure 11, the OC12 configuration block diagram is almost identical to OC3, except the line groups are equipped with OC12 HIF interfaces and the cross-connects are designed for OC12 operation. The HIF units perform the 622.08 Mb/s optical-to-electrical conversion, perform the interface functions for the SONET overhead, perform the STS1 pointer processing, and convert the payload to 12 serial STS1 equivalent signals. The signal is then routed to the OC12 cross-connect unit.

Figure 11. 1603 SM OC12 Functional Block Diagram

4.72 The OC12 cross-connect units (Figure 12) provide non-blocking STS1 or STS3c grooming from any port to any port: East, West, Drop, and Drop-to-Drop. Additionally, any three STS1 signals from the East, West, and Drops may be selected for VT grooming (i.e., to support up to 84 DS1 low speed interfaces). The VSCC provides VT pointer processing prior to the VT cross-connect function. The OC12 VSCC is compatible with all drop group interfaces.

NOTE: *OC12 line group interfaces, OC3 drop group interfaces, and the quad DS3/EC1 interfaces require the VSCC30x/VSCC501 cross-connect.*

Figure 12. OC12 Time Slot Interchange Matrix

Traffic Routing Description (OC48 Configuration)

4.73 As shown in Figure 13, the OC48 configuration block diagram is almost identical to OC3/12, except the line groups are equipped with OC48 HIF interfaces. The HIF units perform the 2.4 Gb/s optical-to-electrical conversion, perform the interface functions for the SONET overhead, perform the STS1 pointer processing, and convert the payload to 48 serial STS1 equivalent signals. The first twelve STS1s are routed to the crossconnect unit and the remaining 36 STS1s are routed to the opposite HIF unit through a flat ribbon cable.

Figure 13. 1603 SM OC48 Functional Block Diagram

4.74 The cross-connect unit (Figure 14) provides nonblocking STS1 and/or STS12c, or STS3c grooming (first twelve STS1s) from any port to any port: East, West, Drop, and Drop-to-Drop. Additionally, any three STS1 signals from the East, West, and Drops may be selected for VT grooming (i.e., to support up to 84 DS1 low speed interfaces). The VSCC provides VT pointer processing prior to the VT cross-connect function. The VSCC is compatible with all drop interfaces.

Figure 14. OC48 Time Slot Interchange Matrix

Traffic Routing Description (Drop Groups)

4.75 The 1603 SM provides three low speed drop groups. Each drop group can be equipped to provide one of the following:

- Four to 28 asynchronous DS1 interfaces
- OC3 interface
- DS3 Transmultiplexer interface
- DS3 interface
- EC1 (STS1) interface
- Software provisionable (DS3 or EC1) interface
- Software provisionable (DS3 or EC1) quad interface
- Quad Ethernet LAN interface
- DS3 ATM mapped interface

NOTE: *The SP101 shelf can support up to three drop groups equipped with the LIF40x units.*

However, only one drop group can be equipped with the LIF40x, if the older ADM150 shelf is used. The remaining two drop groups on the ADM150 shelf must be equipped with asynchronous DS1s or left blank.
NOTE: *The ADM150 shelf can only support one drop group equipped with the quad DS3/EC1 interface. The remaining two drop groups must be equipped with asynchronous DS1 or left blank. All three drop groups on the SP101 shelf can be equipped with the quad DS3/EC1 interface.*
4.76 For DS1 operation (see Figure 15), the drop group consists of a Drop Module Interface (DMI) unit that works in conjunction with one or more Virtual Tributary Group (VTG) units. The external (facility) connections are made using an input/output panel that is optional depending on shelf type and customer preferences (e.g., the DS1WW with wire-wrap pins or the DS1CP with 64-pin AMP Champ connectors).
Figure 15. 1603 SM T1 (DS1) Drop Group Components
4.77 The Drop Module Interface (DMI) plug-in unit divides the STS1 signal into seven virtual tributaries. Each VTG plug-in unit contains four DS1 circuits. This is where the VT pointers are terminated and any differences in frequency are fed into a fractional bit-leaking circuit to ensure a low jitter DS1 signal output. The resulting 28 DS1 signals are fed to an external termination input/output panel.
4.78 For EC1 (STS1) or DS3 transmultiplexer operation (see Figure 16), the drop group consists of Low Speed Interface (LIF) plug-in units that work in conjunction with one or more pairs of Line Driver/Receiver (LDR) plug-in units. The input/output panel for STS1 or DS3 connections is the CIOP101.
Figure 16. 1603 SM EC1 (STSx-1) Drop Group Components
4.79 The redundant EC1 Low Speed Interface (LIF) plug-in units are connected to redundant Line Driver/Receiver (LDR) plug-in units. The two (A and B) LDR units are connected to a common (drop group) coaxial cable connector input/output panel.
4.80 The Quad STS1/DS3 interface unit is only compatible with the OC12 cross-connect. It provides the interface between the four serial STS1 payloads from the OC12 cross-connect unit and the Line Driver Receiver Unit. The Quad LIF unit is software provisionable for STS1 or DS3 functionality per facility interface.
NOTE: *The LIF50x is not compatible with the fixed cross-connect (VSCC20x) or the OC3 cross-connect (VSCC101). The LIF50x requires the OC12 cross-connect (VSCC30x/VSCC501). The VSCC30x/VSCC501 is compatible with both the OC3 and OC12 high speed interface line groups.*
4.81 The Quad Ethernet LAN interface is a single double-wide unit that plugs into both A and B slots of a drop group. This unit is non-redundant. Line/Driver Receiver (LDR) units are not used in conjunction with the Quad Ethernet LAN interface. The 10/100BaseT/Tx cables plug directly into the front of the LIF unit. If multiple Ethernet LIF units are used, the RJ45 connector patch panel can be used to simplify cabling issues.
4.82 The ATM mapped DS3 interface units are 1:1 protected and work in conjunction with a pair of LDR units. The DS3 cables are connected to a CIOP101 coax panel (see Figure 16).
4.83 Figure 17 shows the traffic path between the high speed line group plug-in units, the cross-connect units and the low speed drop units. For a fully redundant system, two of each unit are mounted in the 1603 SM shelf. However, the system can operate in nonredundant mode by equipping the shelf with only one of each plug-in unit type. When low speed interfaces (DS1, EC1 or DS3) are not needed (e.g., repeater NE operation), the drop group plug-in units are not installed.
NOTE: *When configured for OC48 operation, the HIFG0x must be used. This high speed*

interface plug-in unit is a double slot card that uses both the HIF-A and HIF-B slots of a Line Group resulting in nonredundant operation of the 1603 SM shelf. The HIFG0x in Line Group 1 is connected to the HIFG0x in Line Group 2 using a flat ribbon cable routed through the front panel of the HIFG0x.

***NOTE:** Details for equipping the 1603 SM system in a nonredundant configuration are in the Unit Selection portion of the Application Engineering section of this manual.*

Figure 17. 1603 SM Plug-in Traffic Path

4.84 In addition to traffic carrying units, the 1603 SM has common equipment plug-in units (not shown in Figure 17). The Network Element Processor (NEP) and a Craft, Orderwire and Alarm (COA) plug-in unit are nonredundant. If either unit fails, the system maintains a stable operational state and traffic is not affected. However, certain OAM &P functions are unavailable until the defective unit is replaced or the problem is resolved. The other common equipment plug-in units are the power converters (PWR) and the clock (CLK) plug-in units.

Protection Switching Circuitry Descriptions

A/B Equipment Protection Switching

4.85 The 1603 SM provides an equipment protection switching function. The equipment protection mechanism varies with the type of equipment it is protecting. Some equipment is protected by switching all signals simultaneously to working and protected equipment. This enables the same payload to be transmitted identically to the tail-end working and protected equipment. Equipment protection switching requires the equipment be switched as functional groups. Each group is switched independently of other groups, and all units within a single group are switched simultaneously as a single entity. Table I summarizes the unit switching arrangement.

Table I. Plug-in Unit Protection Switching Arrangement*

PLUG-IN UNIT	SWITCHING ARRANGEMENT
OC3/OC12 High Speed Line Group	The HIFs independently switches between Side A and Side B plug-in units for unit or facility failures.
VT/STS1 Cross-Connects	Fixed path cross-connects (VSCC20x) are passive and both Side A and Side B units are required for normal operation (i.e., no switching). Variable cross-connects (VSCC101, VSCC30x, and VSCC501) independently switch between Side A and Side B plug-in units for unit failure.
OC3 Low Speed Interfaces	The LIF40x unit switches independently between Side A and Side B plug-in units for unit or facility failures.
Single EC1 Low Speed Interfaces	Switches between Side A and Side B pairs of plug-in units. If either the LIF20x unit or the LDR unit fails on one side, the system switches to the alternative pair (both LIF and LDR) on the other side. Both LDR units are connected to a common, drop group CIOP101 I/O panel. No

	switching occurs as a result of loss of the common external input signal.
Single DS3 Low Speed Interfaces	Switches between Side A and Side B pairs of plug-in units. If either the LIF30x unit or the LDR unit fails on one side, the system switches to the alternative pair (both LIF and LDR) on the other side. Both LDR units are connected to a common, drop group CIOP101 I/O panel. No switching occurs as a result of loss of the common external input signal.
Single DS3 Transmultiplexer Low Speed Interfaces	The LIF601 plug-in units switch independently of the LDR units. If an LIF601 unit fails on one side, the system switches to the alternate side LIF601 plug-in unit. If an LIF601 unit fails, the LDR unit does not switch sides, only their A/B inputs. However, if an LDR unit fails, the system switches between Side A and Side B of only the affected pair. The LIF601 units do not switch.
Single DS3 ATM mapped DS3	The LIFB01 plug-in units switch independently of the LDR units. If an LIFB01 unit fails on one side, the system switches to the alternate side LIFB01 plug-in unit. If an LIFB01 unit fails, the LDR unit does not switch sides, only their A/B inputs. However, if an LDR unit fails, the system switches between Side A and Side B of only the affected pair. The LIFB01 units do not switch.
Quad DS3 or Quad EC1 Provisionable Low Speed Interfaces	The Quad DS3/EC1 LIF50x unit supports four pairs of LDR units. Each pair consists of an A and B unit. The LIF50x plug-in units switch independently of the LDR units. If an LIF50x unit fails on one side, the system switches to the alternate side LIF50x plug-in unit. If an LIF50x unit fails, the LDR units do not switch sides, only their A/B inputs. However, if an LDR unit fails, the system switches between Side-A and Side-B of only the affected pair. The rest of the LDR units do not switch.
Single DS3 or EC1 Provisionable Low Speed Interface	Same arrangement as Quad, except the LIF701 plug-in unit is used and there is only one pair of LDR units.
DS1 Low Speed Interfaces	The DMI plug-in units independently switch between Side A and Side B plug-in units if a unit fails. Each drop group VTG plug-in units are common to the corresponding DMI plug-in units (A and B sides). If a single VTG unit fails, the system independently switches traffic (as a

	group of four DS1 circuits) to the protection VTG unit. No switching occurs for loss of DS1 input signals. (See the following DS1 Protection Equipment Switching for details)
Clocks	Independently switches between Side A and Side B for unit failures.
Power Converters	Failure of a PWRA01 power converter does not result in any switching. The failed unit shuts down and the remaining units carry the system load. The HIF plug-in units have on-board power converters. Failure of an on-board power converter forces a switch between Side A and Side B HIF plug-in units.
** The equipment does not allow repeated active/protection switches to occur more often than 30 seconds. This prevents unwanted and uncontrolled switching due to intermittent failures.*	

DS1 Equipment Protection Switching

4.86 The 1603 SM can support up to 84 DS1 circuits with 28 DS1 circuits per low speed drop group. Each DS1 drop group consists of Drop Module Interface (DMI) plug-in units (A and B sides) and eight Virtual Tributary Group (VTG) plug-in units. Each VTG provides four DS1 ports. Both DMI plug-in units (A and B sides) support the same set of VTG plug-in units.

NOTE: *The following section refers to VTG units. The VTG102 is identical to the VTG101, except the VTG102 has an LED to indicate when traffic is switching to the protection unit. This feature is supported as of Release 5.00. VTG102 units can be installed in a drop group equipped with VTG101 units. The VTG301 can be used in place of either a VTG101 or VTG102, and the VTG301 has additional functionality (DS1 enhanced performance monitoring). A DMI301 is required to use a VT301G unit within a drop group.*

4.87 The DMI plug-in unit divides the STS1 signal into seven virtual tributaries that are connected to a 1-for-7 switch on the facilities' side of the VTG plug-in unit. Figure 18 shows how the facilities' 1-for-7 DS1 protection works. The first unit installed in the 1603 SM system is the Protection (VTG) unit, followed sequentially by VTG No. 1-7. Each of the seven primary VTG units relies on the previous VTG to provide a path back to the protection VTG unit during fault conditions. If a single VTG plug-in unit fails, the system independently switches traffic (as a group of four DS1 circuits) to the protection VTG unit.

NOTE: *If any of the VTG-1 through VTG-7 slots is equipped with a VTG301, then the VTG-P protection slot must have a VTG301, too.*

Figure 18. 1603 SM DS1 (Facility) Protection, 1-for-7

4.88 The VTG units should be installed in a sequential manner, starting with slot VTG-P and VTG-1. Figure 19 shows a drop group fully equipped with VTG plug-in units. In addition, a drop group can be partially equipped with VTG plug-in units, as shown in Figure 20.

Figure 19. Fully Equipped VTG Drop Group

Figure 20. Partially Equipped VTG Drop Group (Correct)

NOTE: *If a VTG plug-in unit fails, the system independently switches traffic (as a group of four DS1 circuits) to the protection VTG unit. The protection unit (VTG-P slot) takes over until the defective VTG is replaced. The failed VTG can be removed without interrupting service.*

NOTE: *If two VTGs fail simultaneously, the first to fail receives the protection bus, regardless of*

its location in the drop group numbered slots, unless the protection bus is one of the failures.

4.89 There must always be a VTG plug-in unit, which can be out-of-service (OOS), adjacent to (to the left of) any in-service (IS) VTG. The protection bus does not work for an in-service VTG missing an adjacent VTG. Figure 21 shows a partially equipped drop group with two units removed (2 and 5) and two OOS (3 and 6). The arrangement works since the IS units (1, 4, and 7) have adjacent units. (The OOS units 3 and 6 do not require protection.)

Figure 21. Partially Equipped VTG Drop Group (Allowed)

4.90 Figure 22 shows an incorrectly configured drop group. Three units (3, 4, and 6) are in-service, but adjacent units (2 and 5) are missing; therefore, the protection bus does not function for failures of VTG-3 or VTG-6.

Figure 22. Partially Equipped VTG Drop Group (Not Allowed)

4.91 If a VTG301 or VTG102 in slots 1 through 7 experiences a unit failure, the ALM LED will light. The traffic going to this slot is rerouted to the protection slot VTG. As shown in Figure 23, the PSA LED on the failed VTG301 (VTG-3) glows yellow. The PSA LED on the protection slot VTG301 (VTG-P) glows green. If a second VTG301 (VTG-6) fails in this drop group before the first VTG301 is replaced, then the ALM LED on the second failed VTG301 will light, but the PSA LED will not light since the protection slot VTG is already occupied (traffic from the second failed VTG301 will be dropped).

NOTE: *Since the first failure (VTG-3) is covered by the protection unit, then the second failure (VTG-6) that has dropped traffic should be resolved, first. Once traffic is restored on VTG-6, then resolve the first failed VTG. This will minimize traffic outage.*

Figure 23. PSA LED Operation (single failure view)

VT Numbering

4.92 The 1603 SM software supports two AID numbering schemes for T1 and VT1.5 signals. The T1 and the VT1.5 sequential numbering schemes are the original methods implemented by Alcatel. The VT1.5 and T1 grouped numbering scheme is the method recently adopted by Telcordia. Table J lists the schemes, either of which the customer can choose.

Table J. VTG Numbering Schemes*

VTG UNIT	CIRCUIT NUMBER	T1 SEQUENTIAL NUMBERING	VT1.5 SEQUENTIAL NUMBERING	VT1.5 AND T1 GROUPED NUMBERING
1	1	1	1	1-1
	2	2	8	1-2
	3	3	15	1-3
	4	4	22	1-4
2	1	5	2	2-1
	2	6	9	2-2
	3	7	16	2-3
	4	8	23	2-4
3	1	9	3	3-1
	2	10	10	3-2
	3	11	17	3-3
	4	12	24	3-4
4	1	13	4	4-1

	2	14	11	4-2
	3	15	18	4-3
	4	16	25	4-4
5	1	17	5	5-1
	2	18	12	5-2
	3	19	19	5-3
	4	20	26	5-4
6	1	21	6	6-1
	2	22	13	6-2
	3	23	20	6-3
	4	24	27	6-4
7	1	25	7	7-1
	2	26	14	7-2
	3	27	21	7-3
	4	28	28	7-4
** T1 is synonymous with DS1, and the T1 sequential numbering corresponds to the wire-wrap pin numbering of the DS1WW input/output panel mounted on the rear of the shelf assembly.*				