9. SYNCHRONIZATION

Introduction To Synchronization

9.1 A SONET island is defined as a group of SONET NEs interconnected with STS and/or OC-N signals. In such an island, all the NEs must be synchronous to each other. Since connections to the outside world are with asynchronous DS1 and/or DS3 signals, it is not necessary for the clocking of the island to be synchronous with anything in the outside world. Therefore, a single SONET island NE can use one of its own NE's clock as a master, and slave the rest of the island NEs to the master NE. It is also common, but not mandatory, to use an external BITS clock to synchronize one of the NEs. The remaining NEs are slaved from this NE.
9.2 If the DS1 traffic across the SONET island contains DS0 level data of the Digital Data Service (DDS) type, then special considerations apply. The DDS requires that the DS1 equipment at both ends of the DS1 path must be traceable back to the same clock. Usually, this is accomplished by having the DS1 equipment at both ends traceable back to Stratum 1 clocks. When this is the case, it is also necessary for the SONET transport network to be traceable back to a Stratum 1 clock. Otherwise, the pointer adjustments in the SONET transport will cause dribbling bit errors in the DDS circuits. For DS1 traffic that is just voice or modem data (not DDS data), the controlled slip buffers in the Class 5 switch will mask the effects (i.e., make it undetectable) of pointer adjustments of a SONET island that is not traceable to a Stratum 1 clock.
9.3 When two or more SONET islands are interconnected, it is necessary that the interconnected islands be synchronous to each other. This is usually achieved by one or more BITS clocks that are each traceable back to a stratum 1 perfect clock.
9.4 To support flexible interconnect of NEs, the 1603 SM is capable of being provisioned to obtain its synchronization from many different sources. The priority of these various sources is also provisionable. Automatic switching selects the highest priority available source. The possible sources are: BITS Primary, BITS Secondary, Line Group 1, Line Group 2, Drop Group 1, Drop Group 2, and Drop Group 3. Drop Groups can only be used as synchronization inputs if equipped for STS or OC3 signals. Last, and of lowest priority, is the internal clock. The 1603 SM uses a stratum 3 quality internal clock with holdover capability. Holdover is defined as the ability of a clock, which has lost all external synchronizing input and is using stored data acquired during normal operation, to control its output.
9.5 The priority of these inputs to the NE for synchronization is determined by the way they are entered by the SYNCN commands and are referred to as NESYNC. In many networks this provisioning of priority is sufficient to maintain network synchronization even during equipment and facility faults without the use of synchronization messaging. Synchronization messaging is a 1603 SM feature that may be used to enhance distribution of synchronization in some network configuration situations (typically rings). When turned on, it can override the priorities that have been set as described, taking into account network level status as well as the individual NE status.
9.6 The NE also provides synchronization outputs that may be used by other NEs or BITS

clocks. These BITS outputs are referred to as BITSSYNC.

Synchronization Messaging Overview

9.7 The quality level (frequency accuracy) of an OC-N, STS1 (EC1), or BITS reference frequency is described by a message contained within the signal (refer to Table X). For the OC-N and STS1 signals, the message is contained in the S1 overhead four bit nibble. For a BITS reference frequency signal it is submultiplexed onto the framing bit of a DS1 ESF (Extended SuperFrame) frame format. The 1603 SM is capable of reading the incoming messages and writing messages to the outgoing signals for these different signal types. It can be provisioned to ignore incoming messages. It can send no outgoing messages, dynamically determined outgoing messages, or fixed outgoing messages. In typical operation the NE processor makes decisions based upon provisioned reference priorities, weighted by incoming messages. It decides what to use as the local NE synchronization reference and what type of messages to send out on the BITS sync ports and the OC-N and STS1 traffic ports. The objective is to automatically preserve network synchronization during faults while also avoiding timing loops within the network.

9.8 The provisioning of synchronization reference priorities and sync messaging is highly dependent upon the network topology and the number and types of available BITS clocks. In some cases the BITS clocks are all separately traceable to a stratum 1 reference. In other cases one BITS clock is intended to be the reference for another BITS clock through the SONET transmission system itself. In most cases today, the BITS clocks do not yet have sync messaging capability. The 1603 SM can accommodate BITS clocks without sync messaging but future BITS clocks with sync messaging will provide more robust synchronization topologies. Because of the large number of possible situations, only a few common examples will be described. Many situations will have to be engineered with the help of the Alcatel Technical Assistance Center.

Table X. Synchronization Status Message Definitions

DESCRIPTION	ACRONYM	QUALITY LEVEL	DS1 ESF FDL MSG	OC-N S1 NIBBLE
PRS Traceable	PRS	1	0000010011111111	0001
Synchronized - Traceability Unknown	STU	2	0000100011111111	0000
Traceable Stratum 2 in Holdover	ST2	3	0000110011111111	0111
Traceable Stratum 3 in Holdover	ST3	4	0001000011111111	1010
Traceable SONET Clock Self-Timed	SIC	5	0010001011111111	1100
Traceable Stratum 4 Free Run	ST4	6	0010100011111111	N/A
Do not use for sync	DUS	7	0011000011111111	1111
Reserved for network synchronization	RES	User	0100000011111111	1110

use				

Timing Loops

9.9 A timing loop is a condition where a clock derives timing from itself, usually through intermediate clocks. Clocks in a timing loop are no longer Primary Reference Source (PRS) traceable and drive each other off-frequency. Furthermore, there is no resulting alarm specifically associated with the timing loop.
NOTE: *The Primary Reference Source (PRS) is typically understood to mean a Stratum 1 atomic clock.*

Timing Loops versus Holdover

9.10 Synchronization Planning guidelines seek to avoid or at least minimize possible synchronization impairments; however, it is not possible to avoid all impairments. Holdover and timing loops have the potential to impact traffic performance. A compromise must be made when designing the synchronization distribution network between the possibility of creating a timing loop and the possibility of a clock entering holdover. The greater weight should be given to avoid the creation of a timing loop. The timing loops are worse than holdover for several reasons.
9.11 No alarms are associated with the creation or existence of a timing loop. When a timing loop occurs, the performance of the clocks in the loop degrades and there is no indication that the problem exists. Often the existence of a timing loop goes unnoticed until traffic is adversely effected. In addition, due to the lack of alarms, troubleshooting the location of the timing loop is difficult. Conversely, a clock that enters holdover generates an alarm indicating that a problem exists and roughly identifies the location of the fault.
9.12 When a clock is in a timing loop, the performance is worse than when a clock is in holdover. The feedback that occurs during a timing loop causes the clocks to be driven off frequency at an increasing rate. For approximately one hour after a timing loop occurs, the performance may be better than holdover. However, after that (approximately an hour) time interval, the performance in a timing loop rapidly degrades to much worse than if in holdover.

Theory of Operation

GENERAL

9.13 There are two major synchronization functions in the 1603 SM. The first function is to align, in phase and frequency (synchronize), the NE clock signals to a synchronization reference. The NE clock signals are used to drive the hardware that transports data inside the NE and that create the output data streams on all the external SONET facilities. This function is referred to as Network Element Synchronization or NESYNC. The second major function is to synchronize the timing output on the NE's BITS output facilities to a synchronization reference. This function is referred to as BITS Output Synchronization or BITSSYNC. For the NE to provide the best performance, each of these two functions should use the best available reference from those provisioned by the customer.
9.14 Each circuit card that handles a facility input that can be used for synchronization, has special hardware to recover a clock from the input data stream. This special hardware is also used to recover the synchronization quality level information that may be contained in the S1

byte for SONET facilities or the ESF datalink message for BITS facilities. The reference selection process uses status information about the recovered clock, such as whether it is failed or the phase movement is unacceptable, and the quality level associated with that reference in order to make a selection decision. This recovered clock information and associated quality level is maintained for each provisioned NESYNC and BITSSYNC reference.

9.15 Each reference has an associated input quality level. This input quality level always matches the quality level received in the SONET S1 byte or ESF datalink message when synchronization input messaging processing has been enabled using the facility ENT/ED TL1 command. If synchronization input messaging on a particular SONET facility is disabled, the associated quality level is set internally to Traceability Unknown (quality level 2). If synchronization input messaging on a BITS facility has been disabled, the associated quality level can be provisioned to a fixed quality level, with the default of Traceability Unknown (quality level 2). Also, when input messaging is disabled on a BITS input facility, the user can explicitly set the associated input quality level for that facility using the ENT/ED command to specify the INQUAL parameter.

9.16 Each change in the input synchronization message value is validated before being acted upon. This validation period helps filter out transient conditions in the synchronization network, and also provides for phase settling resulting from synchronization reconfiguration actions upstream of the NE. The validation of the change, selection of the appropriate reference, and update of the output synchronization messages typically occurs within ten seconds.

NETWORK ELEMENT SYNCHRONIZATION

9.17 The upper half of Figure 87 shows the behavior for Network Element Synchronization, or NESYNC. For NESYNC, up to six references can be considered in the selection process. The user can specify up to five references as candidates for synchronization, and the sixth reference, which is the internal oscillator on the clock unit circuit card, is always present. The user specifies the relative priority of the references that are candidates for synchronization, from highest priority to lowest. The internal oscillator, or holdover, is always considered the lowest priority reference. Transmission of the recovered clocks to the clock unit circuit card is enabled for each reference the user has specified for synchronization. If synchronization input messaging is enabled for a reference, the received quality level information will be polled, otherwise a fixed input quality level is used internally by the NE. If the status of the recovered clock is good, and the associated input quality level is valid, then that reference is considered in the reference selection process.

9.18 In the reference selection process, the quality level information takes higher precedence over the priority order. Therefore the highest quality level, highest priority reference is selected as the source for synchronization for the Network Element. For example, if the primary reference has an associated quality level of 2 (Traceability Unknown) and the secondary reference has an associated quality level of 1 (Stratum 1 Traceable), then the secondary reference will be selected. If both primary and secondary references have an associated quality level of 1, then the primary reference will be selected.

Figure 87. Synchronization Messages (NE Sync and BITS Output)

9.19 All of the SONET rate clock signals internal to the NE are synchronized to the selected reference for NESYNC. This means that the outgoing data streams on SONET facilities are traceable for synchronization to the selected reference. This leads to the general rule that a SONET output facility's synchronization status message should indicate the synchronization traceability of the selected reference. However, there are some exceptions:

- The BITS outputs may not be traceable to the selected NE reference.
- Output synchronization messaging may be disabled, in which case, the transmitted synchronization status message indicates Traceability Unknown (level 2).
- The output synchronization message may be set to Don't Use for Synchronization (level 7) using the ENT/ED facility command.
- The facility that has been selected as the source of NE synchronization has to be handled specially to avoid the creation of a timing loop with the adjacent NE. To preclude a timing loop, the output synchronization status message on this facility is set to Don't Use for Synchronization (level 7).
- The output message may not reflect the selected references associated quality level when a facility is being used as a synchronization source for a BITS output (refer to the BITS Output Synchronization section).

BITS OUTPUT SYNCHRONIZATION

9.20 The lower half of Figure 87 shows the behavior for BITS Output Synchronization, or BITSSYNC. Each BITS output behaves independently, but the behavior described is the same for both outputs. For BITSSYNC, only two references are considered in the selection process. The user can specify a single SONET optical reference as a candidate for synchronization. The second reference, which is the timing currently used for NE synchronization (NEREF), is always present. NEREF is always considered the lowest priority reference. Transmission of the recovered clocks to the clock unit circuit card is enabled for the SONET reference that the user has specified for synchronization. If synchronization input messaging has been enabled on that facility, the received quality level information will be polled, otherwise a fixed input quality level is used internally by the NE. If the status of the recovered clock is good, and the associated input quality level is valid, then that reference is considered a valid synchronization reference for a BITS output.
9.21 Starting in R06.00.00, each BITS output can function independently of the other. The provisioning, reference selection, and output message behavior are handled separately internal to the NE. Provisioning both BITS outputs the same causes the reference selection and output message behavior to have the same results.
9.22 In the reference selection process, dynamic selection based on quality level information changes does not occur. If the primary reference is valid, it is selected as the source of synchronization for the BITS output. If the primary reference is a SONET reference, and that reference is failed, DS1 AIS is output on the BITS output. If the user has not provisioned a SONET reference for the BITS output, then NEREF is used for synchronization. Changes in the associated input quality level for the selected reference results in changes in associated output quality level for the BITS output facility.
9.23 The outgoing data stream on the BITS facility is normally traceable for synchronization to the selected reference. This leads to the general rule that a BITS output facility's synchronization status message should indicate the synchronization traceability of the selected reference for BITSSYNC. However, there are some exceptions:

- Output synchronization messages may be disabled on an ESF mode BITS output facility, in which case the transmitted synchronization status message indicates Traceability Unknown (level 2).
- The output synchronization message for an ESF mode BITS output facility may be set to Don't Use for Synchronization (level 7) using the ENT/ED facility command.
- The SF mode BITS facilities cannot transmit messages, and have unique behavior to

compensate for this. Since SF mode BITS facilities cannot transmit a synchronization message, DS1 AIS is used as an indication of when the synchronization traceability of the selected source is at or below a threshold set using the ENT/ED-BITS command with the AISQUAL parameter. This threshold represents the quality level, which the equipment connected to the BITS output should not use for synchronization. For example, if the BITS output is going to a Timing Signal Generator (TSG) that has internal Stratum 2 (quality level 3) holdover capability, then the TSG should not continue to use the DS1 reference it receives from the 1603 SM, when that reference has an associated quality level of 4 (Stratum 3). To accomplish this, the NE should be provisioned with the AISQUAL set to 4. This will cause the NE to generate DS1 AIS when the selected source for the BITS output has an associated quality level of 4, which in turn will cause the TSG to enter holdover if no other references are available to it.

- The BITS input facilities are not allowed to be references for the BITS output facilities because of the high probability of creating a timing loop. The user cannot directly specify a BITS input facility as the candidate for synchronization, but this situation can be encountered indirectly. It is perfectly acceptable to have NEREF as the only reference source for a BITS output. It is also allowed to have a BITS input facility as a candidate for the NE synchronization (NEREF). To avoid timing loops, when the BITS output facility has NEREF as the selected source for synchronization, and the NE has currently selected a BITS input, the BITS output is set to DS1 AIS.

9.24 There is an additional special behavior that aids in the avoidance of timing loops in the network. A TSG collocated with the NE may use the NE's BITS output as a reference and provide synchronization back to the NE through the BITS input facility. In this configuration, timing flows transparently through the NE to the BITS, and is then returned to the NE. The NE attempts to recognize this condition by matching the associated quality level between the BITS output facility and the BITS input facility. If these levels match, it is assumed that the TSG has selected the NE's BITS output and is returning that same timing to the NE, in which case the NE transmits the "Don't Use for Synchronization" message for the output message on the facility that is the selected source of synchronization for BITSSYNC.

Practical Applications

Linear TM/ADM Network Synchronization - BITS

9.25 The 1603 SM provides the ability to transport network synchronization. Figure 88 shows a two-node linear network with two 1603 SM NEs configured as terminal multiplexers. In this application, NE A is the master BITS site and is provided with redundant synchronization inputs from the Building Integrated Timing Supply (BITS) through DS1s. The 1603 SM synchronizes its optical carrier outputs to the DS1 source.

Figure 88. Synchronization Between Two 1603 SM NEs

9.26 NE B is at another site and derives synchronization from the optical carrier inputs and delivers this synchronization through DS1s to the local BITS. The BITS clock is responsible for synchronization quality, holdover, and jitter control. NE B derives its transmit timing from the local BITS.

9.27 The previous example referred to 1603 SM NEs in the terminal multiplexer configuration. If a 1603 SM NE is configured as an add/drop multiplexer (ADM), synchronization is transported in both directions. Figure 89 shows how NE A in the previous example works if configured as an

ADM. Figure 90 shows how NE B in the previous example works if configured as an ADM.
Figure 89. ADM with Source BITS Configuration
Figure 90. ADM with Sink BITS Configuration
9.28 Figure 91 is an example of loop timing (also referred to as line timing) between two 1603 SM NEs. NE C is not equipped with a BITS source and is configured for loop timing. NE C derives its incoming clock from the optical carrier inputs and delivers the synchronization clock to the 1603 SM internal Stratum 3 clock. The 1603 SM internal clock provides the equivalent of the BITS function (i.e., tracks the long term average input frequency, provides holdover for loss of good input synchronization and jitter control). NE C provides its transmit timing from the Internal Stratum 3 clock.
Figure 91. Loop Timed Synchronization Between Two 1603 SM NEs

Synchronization Provisioning

9.29 Figure 92 shows a three-node linear network consisting of two 1603 SM NEs configured as terminal multiplexers and one 1603 SM NE configured as an add/drop multiplexer. NE A is equipped with redundant Internal Stratum 3 Clocks in addition to redundant DS1 inputs from the BITS source. The DS1 input synchronization sources are monitored for failure (loss of signal, AIS) by the 1603 SM and the reference priorities are software provisionable. The 1603 SM NE synchronization should be provisioned to select the Primary BITS input as first choice, the Secondary BITS input as second choice, and the internal Stratum 3 Clock as third choice.
Figure 92. Downstream Synchronization Between Three NEs
9.30 NE B should be provisioned to provide synchronization to the BITS source (output synchronization) from the interface facing NE A. For loss of a good synchronization signal, the 1603 SM inserts an AIS signal into the DS1s connected to the BITS to indicate a loss of synchronization reference. The NE synchronization at NE B is provisioned the same as NE A.
9.31 NE C should be provisioned as synchronization from the interface facing NE B for first choice and the Internal Stratum 3 Clock as second choice.

UPSR Network Synchronization for R03.01 (for R04.00 and Later, see Synchronization Switching Based On Sync Messaging)

9.32 Synchronization for 1603 SM Unidirectional Path Switched Ring (UPSR) networks is accomplished using one of two preferred methods. In Figure 93, the rings are divided into two subnetworks for synchronization, with both subnetworks synchronized from the same master. One subnetwork consists of NEs A, B, and C. The other subnetwork consists of NEs A, D, and E. The subnetworks are provisioned the same as their linear counterparts. In this example, NE A operates as the master BITS source for both subnetworks. NEs B and D operate in an ADM synchronization mode with local BITS. NEs C and E operate in loop timed mode.
Figure 93. UPSR Synchronization
9.33 Figure 94 shows the second preferred method of ring synchronization. This method does not divide the ring into two subnetworks. Instead, synchronization is sent one way around the entire ring. For example, NE A is the master BITS (source). NE B is looped timed from NE A, NE C is looped timed from NE B, NE E is looped timed from NE C, and NE D is looped timed from NE E. NEs B, C, D, and E are provisioned for internal clock synchronization if their loop timing fails. For a ring break, the NE beyond the break goes into internal clock mode and the rest of the ring synchronizes to that internal clock.

Figure 94. UPSR Synchronization

Synchronization through Drop Groups

9.34 The 1603 SM system is software provisionable to obtain synchronization through one of the three drop groups. However, this requires a synchronous interface, such as STS1 or OC3. The synchronization drop group can also be used for normal traffic.
NOTE: *The ADM150 shelf supports synchronization through Drop Group 1, if equipped with the CLK202 or CLK203 plug-in unit. The SP101 shelf can support synchronization from any of the three drop groups, if equipped with the CLK202 or CLK203 plug-in unit.*

Synchronization Switching Based on Sync Messages

9.35 Facilities are provisioned into clock reference priority tables to support network element synchronization and BITS output synchronization. Prior to Release 04.00, switching of references within the two tables was performed on the basis of facility status (i.e., changes in status result in evaluation of the references in the priority table to select the highest priority available [working] reference). Release 04.00 and later releases include the synchronization messages supported in the S1 byte (lower nibble) of SONET facilities and in the data link code words of Extended SuperFrame (ESF) BITS. For more details, see the Theory of Operation section.
NOTE: *CLK202 or CLK203 is required for synchronization messages.*
9.36 The following paragraphs describe how sync messaging works before and after a cable cut fault. Both linear network and ring network configurations are addressed using one and two BITS references. The related figures show timing distribution in the network prior to the fault.

Sync Messaging in a Linear Network with One BITS

9.37 In a linear network with a BITS at one end (Figure 95), there is no particular advantage in using sync messaging. NE 1 would be provisioned to use the BITS input as first choice and its internal stratum 3 clock in holdover as its second choice. All other NEs would be provisioned to loop time using the timing coming from the direction of NE 1.
Figure 95. Linear Network with One BITS
9.38 In the event of a fault (e.g., between 2 and 3), NE 3 goes into holdover. NE 3 then provides timing to 4 and 5. When the failure is repaired, NE 3 switches back to timing coming from the direction of 1, and all NEs are again timed from the BITS.

Sync Messaging in a Linear Network with Two BITS

9.39 There are two primary applications to consider for the linear network with two BITS. The first is when BITS A is to send the reference timing for BITS B by way of the SONET system; the second is where BITS B gets its reference input from some external network, and the SONET system does not have to distribute timing from one BITS to the other. These cases are shown in Figure 96. For both cases, assume that both BITS are of the type available (i.e., no sync messaging capabilities). Both BITS A and B are using an external Primary Reference System (PRS), which is typically a Stratum 1 clock.
NOTE: *In the future, when BITS are available with sync messaging, the operation can be slightly different from the following descriptions. Such future BITS will make network*

synchronization even more robust.

Figure 96. Linear Network with Two BITS

9.40 In the first application, timing is distributed as shown in Figure 96. NE 1 is provisioned to use sync messaging and the BITS input as first choice and timing from NE 5 as second choice. NEs 2, 3, and 4 are provisioned to use sync messaging and pass timing from direction of NE 1 on down the line toward NE 5; timing from NE 5 is selected as a second choice.

9.41 NE 5 is provisioned for sync messaging and to pass the timing received from direction of NE 1 to its sync output, then to the sync input port of BITS B. An output from BITS B is fed back into NE 5 that is provisioned to use it as a timing reference for the whole NE as first priority and timing from NE 1 as second priority.

9.42 Under typical (no-failure) conditions, the possible timing information and sync messages sent from NE 5 toward NE 1 are never used. However, in the event of a failure (e.g., between NEs 2 and 3), the sync messaging software causes BITS B to go into holdover and NEs 4 and 3 to derive timing from BITS B. NE 5 continues to be timed from BITS B. NEs 1 and 2 continue to be timed from BITS A. When the failure is repaired, the software causes NEs 3, 4, and 5 to retime from the direction of NE 1 and BITS B to come out of holdover and be referenced from BITS A.

NOTE: *For NE 5 to perform in this manner, it requires prior provisioning of the AIS quality parameter using the ENT/ED-BITS command.*

9.43 Provisioning for NE 5 is different in the second application. It is not usually provisioned to provide a reference frequency output and that signal is not usually fed to the BITS B input. NEs 2, 3, and 4 are provisioned for sync messaging, with the timing from the direction of NE 1 as first choice, and from the direction of NE 5 as second choice. NE 5 is provisioned for timing from NE 1 as first choice and for timing from BITS B as second choice. For a failure between NEs 2 and 3, the BITS B does not go into holdover because it is still receiving a valid reference input through an external path; in this case, the sync messaging software in NEs 5, 4, and 3 switches to timing from BITS B. When the failure is cleared, NEs 3, 4, and 5 revert to being timed from BITS A. In summary, this case uses the BITS B as a backup timing source during failures.

Sync Messaging in a Ring Network with One BITS

9.44 In a ring network (Figure 97), sync messaging should always be turned on in all NEs. NE 1 is provisioned to use the BITS input as its timing reference. It sends its timing and messages both ways around the ring. All other NEs use the timing sent just one way around the ring under typical conditions. The ring NEs are provisioned to use ring timing coming in the Line Group 1 direction as first choice and timing coming in the other Line Groups direction as second choice. For example, if a fault occurs between NE 2 and NE 3, NE 2 continues to use timing coming in the NE 1 to NE 2 direction. However, the sync messaging software in NEs 3 and 4 switches their timing reference to the timing coming in the direction of NE 1 to NE 4 to NE 3. The net result is that all NEs on the ring are still timed from the BITS at NE 1, even during the failure.

Figure 97. Ring Network with One BITS

Sync Messaging in a Ring Network with Two BITS

9.45 There are two primary applications to be considered for the ring network with two BITS (Figure 98). The first is when BITS A is to send the reference timing for BITS B by way of the SONET system; the second is where BITS B gets its reference input from some external network and the SONET system does not have to distribute timing from one BITS to the other.

For both cases, assume that both BITS are of the type available (i.e., no sync messaging capabilities).

NOTE: *In the future when BITS are available with sync messaging, the operation can be slightly different from the following descriptions.*

Figure 98. Ring Network with Two BITS

9.46 In the first application, timing is distributed as shown in Figure 98. All NEs are provisioned to use sync messaging. NE A is provisioned with the BITS input as its timing. It passes timing both ways onto the ring. NEs B, C, and D are timed from the Line Group 1 direction, with Line Group 2 as second choice. NE C is provisioned to provide BITS output timing. The sync messaging software ensures that for any ring break all the ring NEs are still timed from BITS A. It also ensures that BITS B always gets a reference input from BITS A, even with a ring fault.

9.47 Provisioning for NEs A and C is different in the second application. They are not usually provisioned to provide a reference frequency output and that signal is not usually fed to the BITS B input. BITS B is provisioned to provide timing to all NEs in the ring in the event BITS A fails. This setup also allows BITS B to provide timing to a partial network for failure situations. For a single ring failure between NE B and NE C, NEs A, B, and D continue to receive timing from BITS A. NE C uses timing from BITS B. For a second failure (simultaneous with the first) between NEs A and D, NE D also times from BITS B and traffic between NEs C and D is preserved.

Composite Clock Synchronization

9.48 The 1603 SM composite clock (CCLK) circuitry (Figure 99) generates a 64-kHz composite clock format output signal. This CCLK output is useful in remote environments where there is no external (office) composite clock. A typical application would include Digital Data Service (DDS) applications through a channel bank.

Figure 99. Composite Clock Functions

NOTE: *The 1603 SM shelf has been designed to support possible future features such as DS0 interface line shelves. The 1603 SM shelf has input pins for two external (independent) 64-kHz composite clock sources, as well as a set of clock test connections for both 8-kHz and 64-kHz testing using a standard test set. None of the connections are currently supported.*

9.49 Each of the CLK20x plug-in units generates a composite clock. CLK-A provides the primary (CCLK PRI) and CLK-B provides the secondary (CCLK SEC). These composite clocks are fed from the A clock to the B clock. In the event of clock failure, A/B switching is performed and the composite clock output is maintained. However, if clock unit is removed, the composite clock output will fail.