Logic components

review

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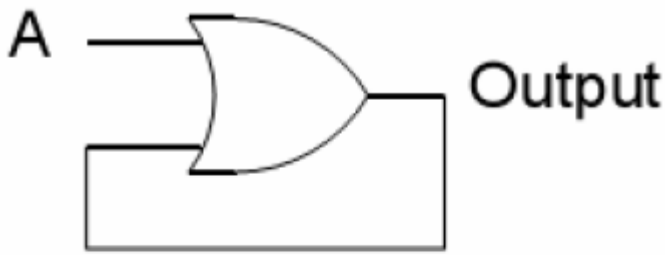
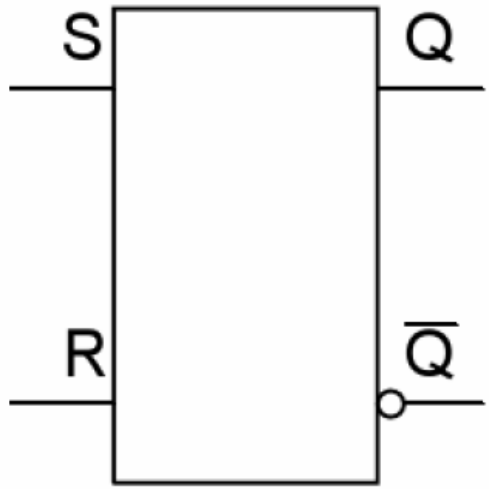
LATCH

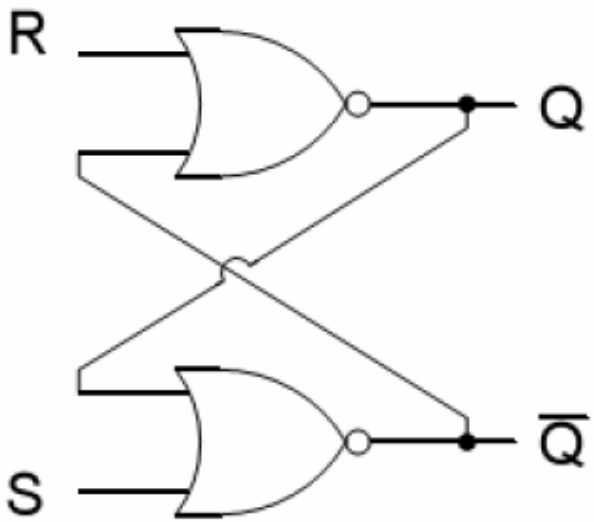


A	Output
0	?
1	1

? = LATCH

S-R Latch

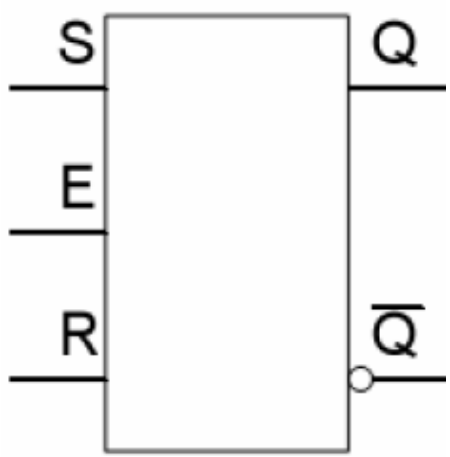


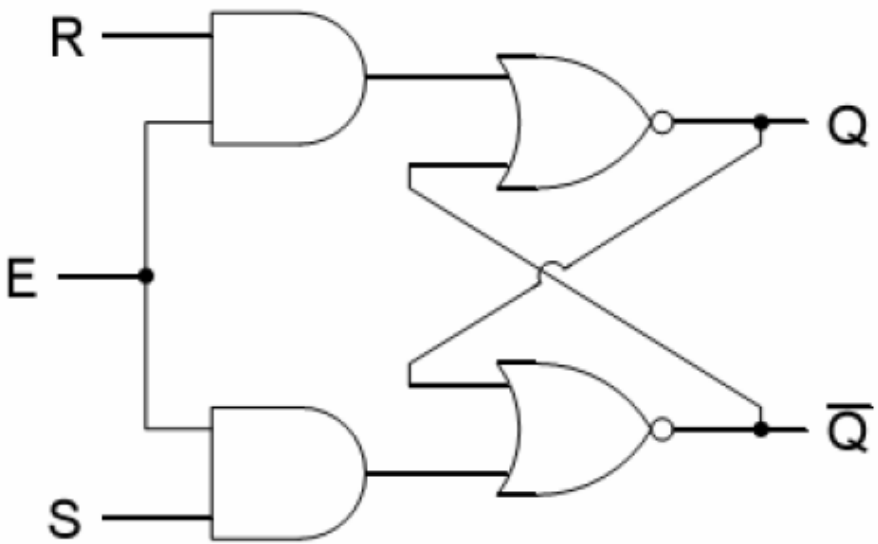


S	R	Q	$\overline{Q}$
0	0	latch	latch
0	1	0	1
1	0	1	0
1	1	0	0

illegal

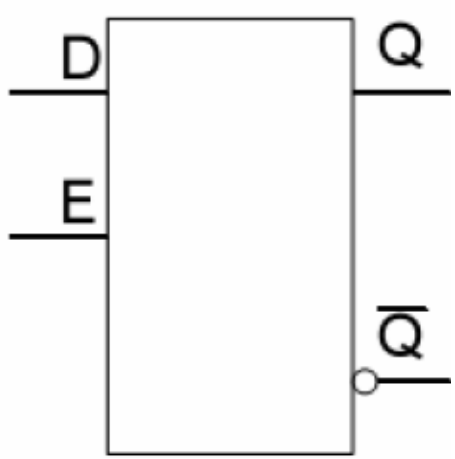
Gated S-R Latch

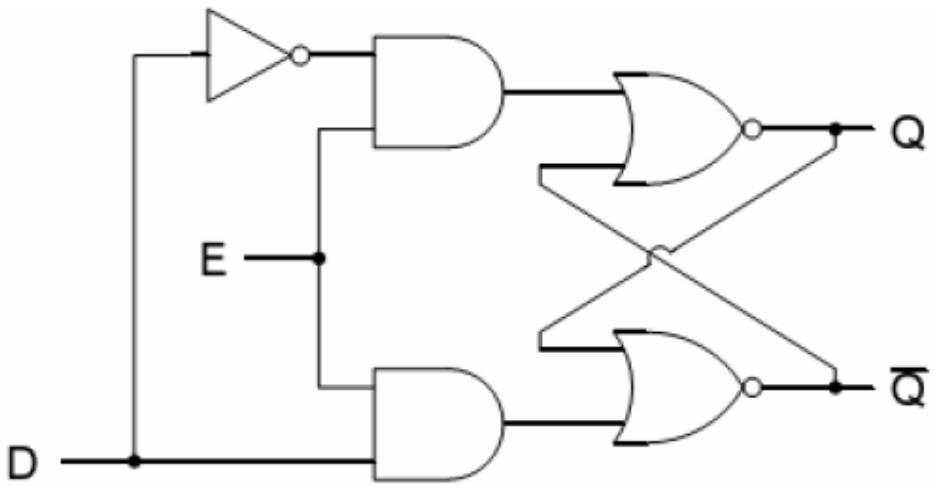




E	S	R	Q	$\overline{Q}$
0	0	0	latch	latch
0	0	1	latch	latch
0	1	0	latch	latch
0	1	1	latch	latch
1	0	0	latch	latch
1	0	1	0	1
1	1	0	1	0
1	1	1	0	0

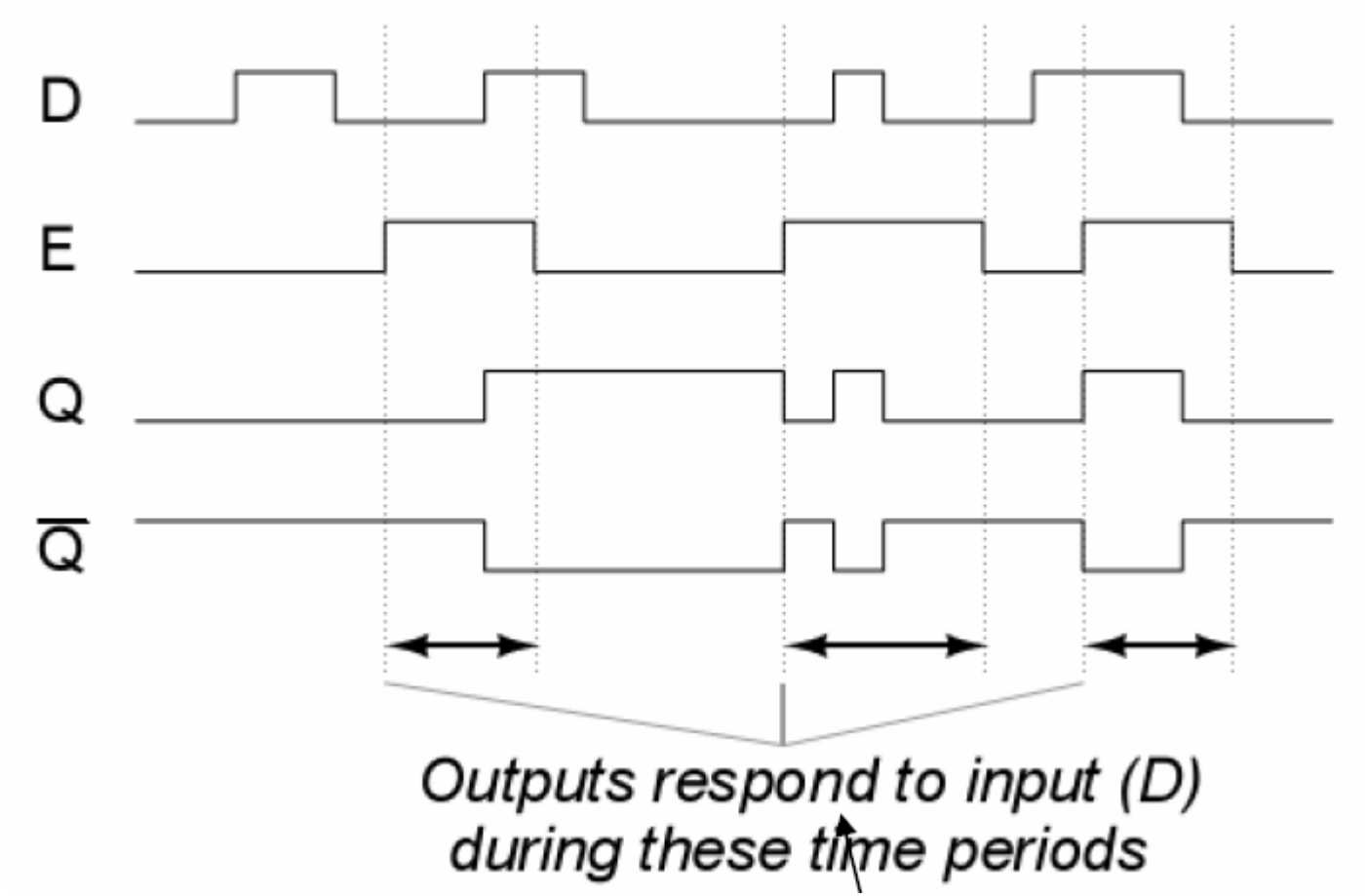
D Latch



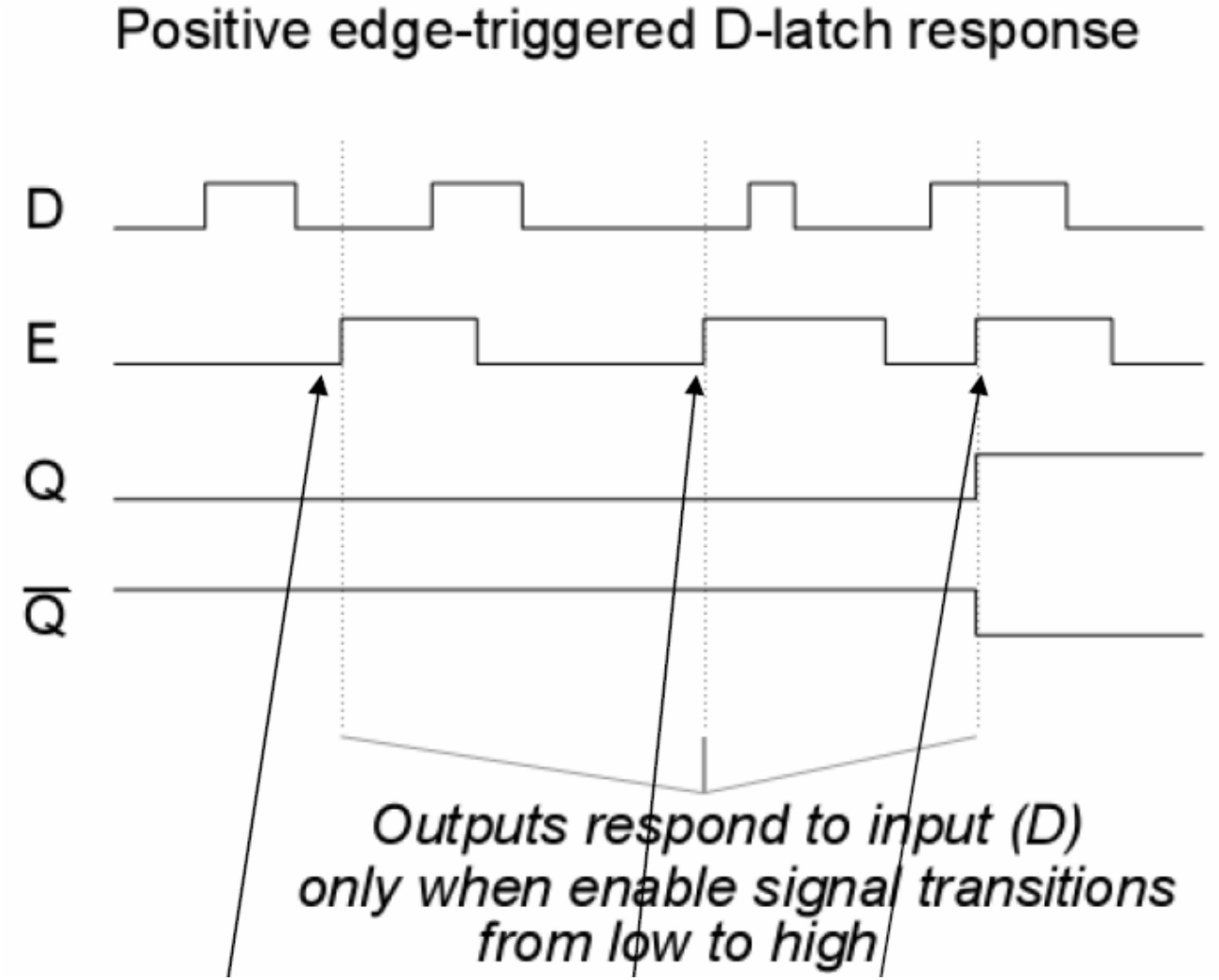


E	D	Q	$\overline{Q}$
0	0	latch	latch
0	1	latch	latch
1	0	0	1
1	1	1	0

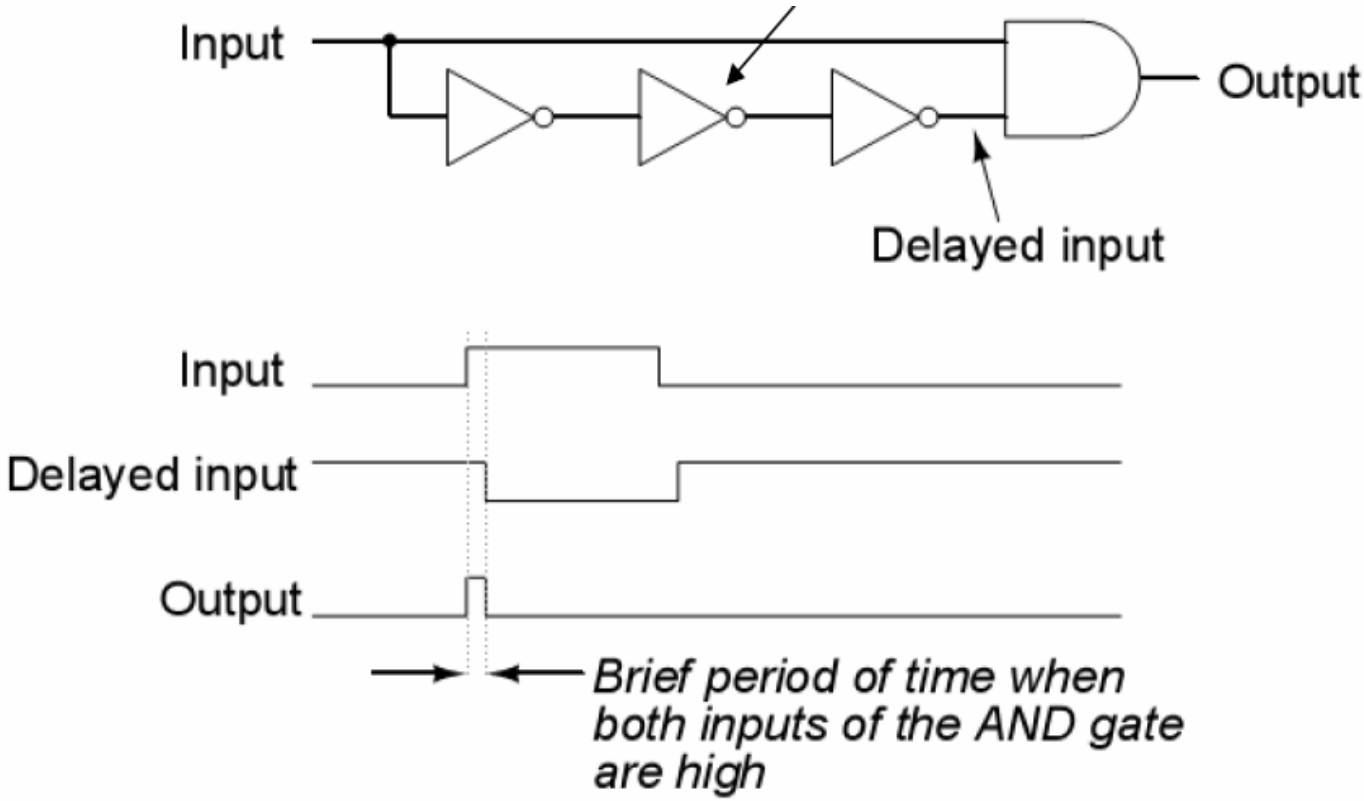
Regular D-latch response



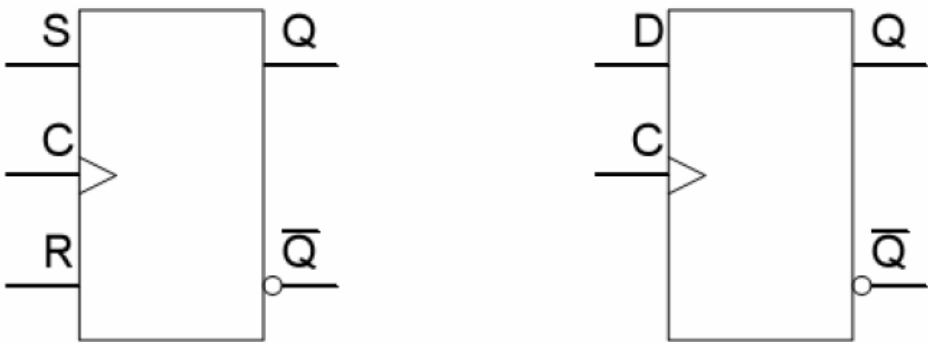
Flip Flop

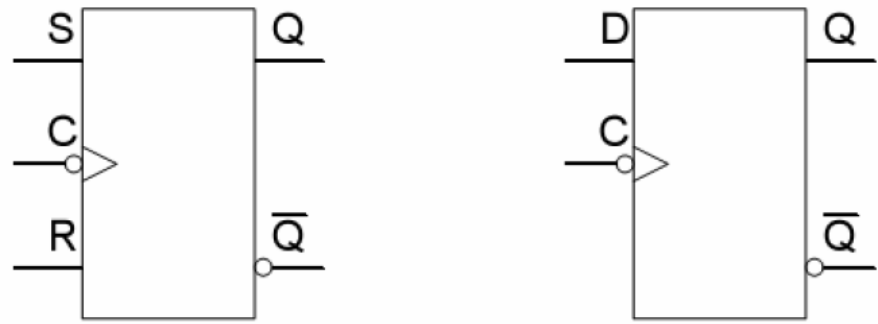

Positive edge-triggered D-latch response
D
E
Q
$\overline{Q}$
Outputs respond to input (D)
only when enable signal transitions
from low to high

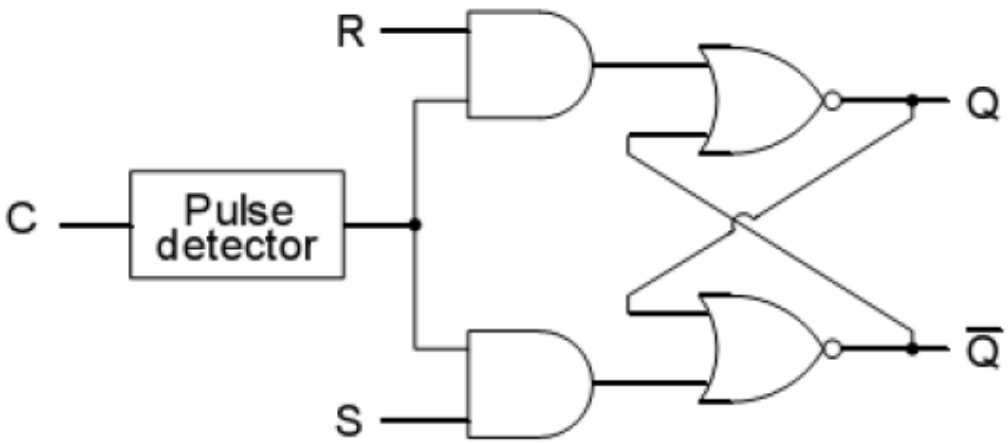
Pulse creator



S-R flip flop, D flip flop

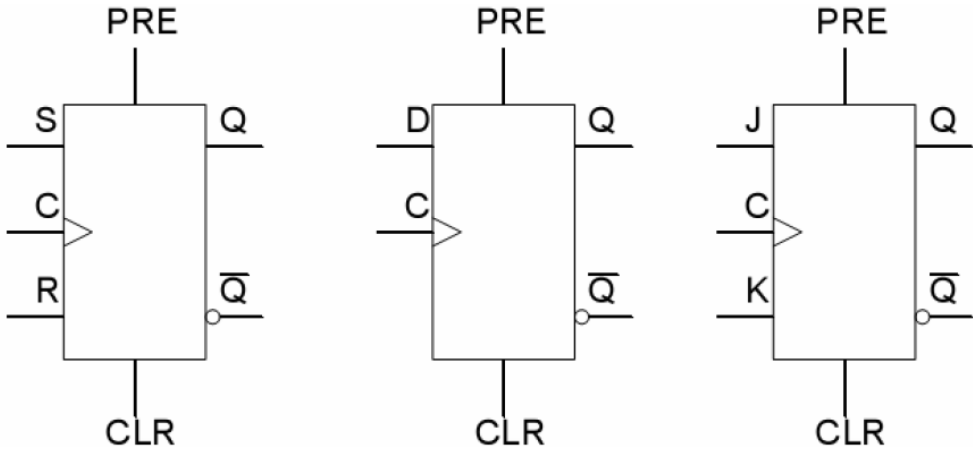


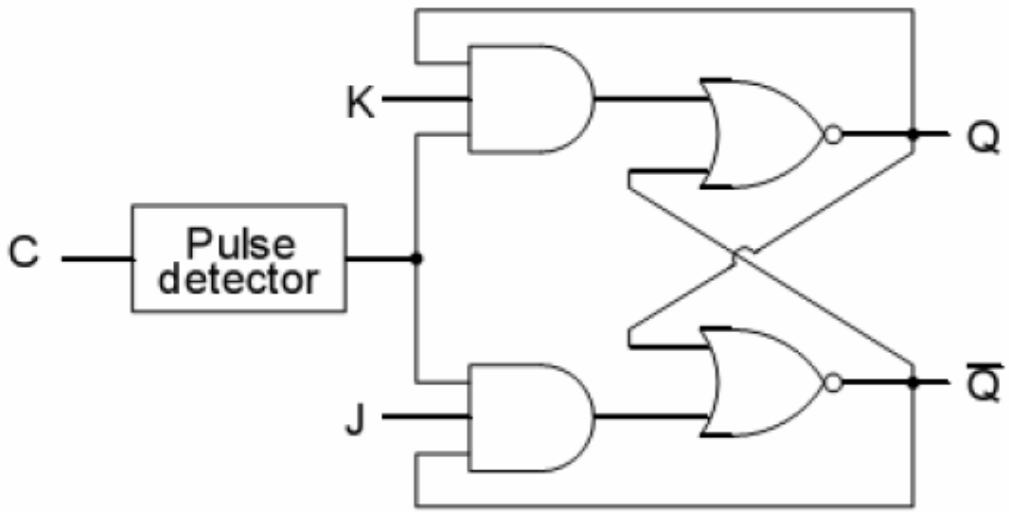




C	S	R	Q	$\overline{Q}$
⌐¬	0	0	latch	latch
⌐¬	0	1	0	1
⌐¬	1	0	1	0
⌐¬	1	1	0	0
x	0	0	latch	latch
x	0	1	latch	latch
x	1	0	latch	latch
x	1	1	latch	latch

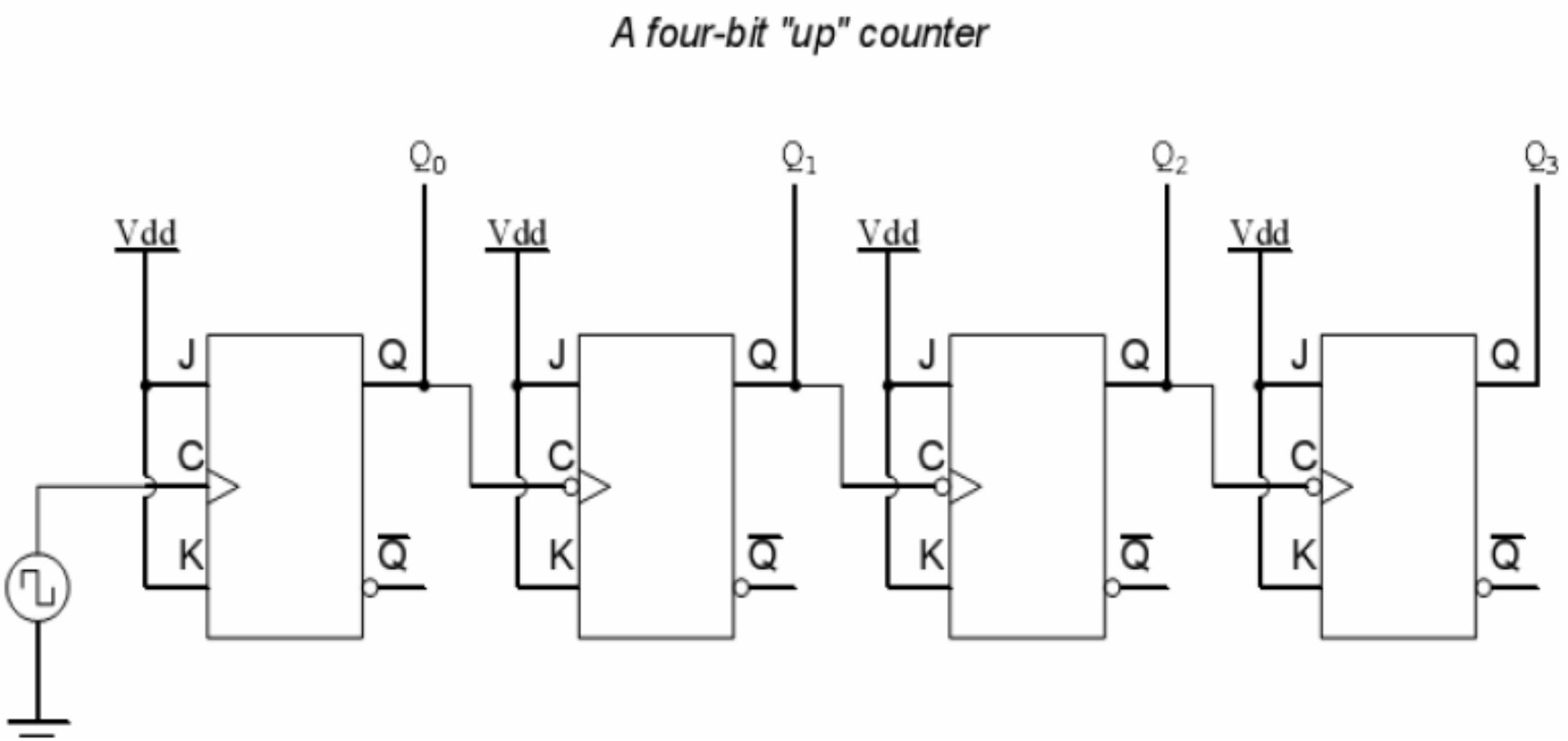
J-K flip flop



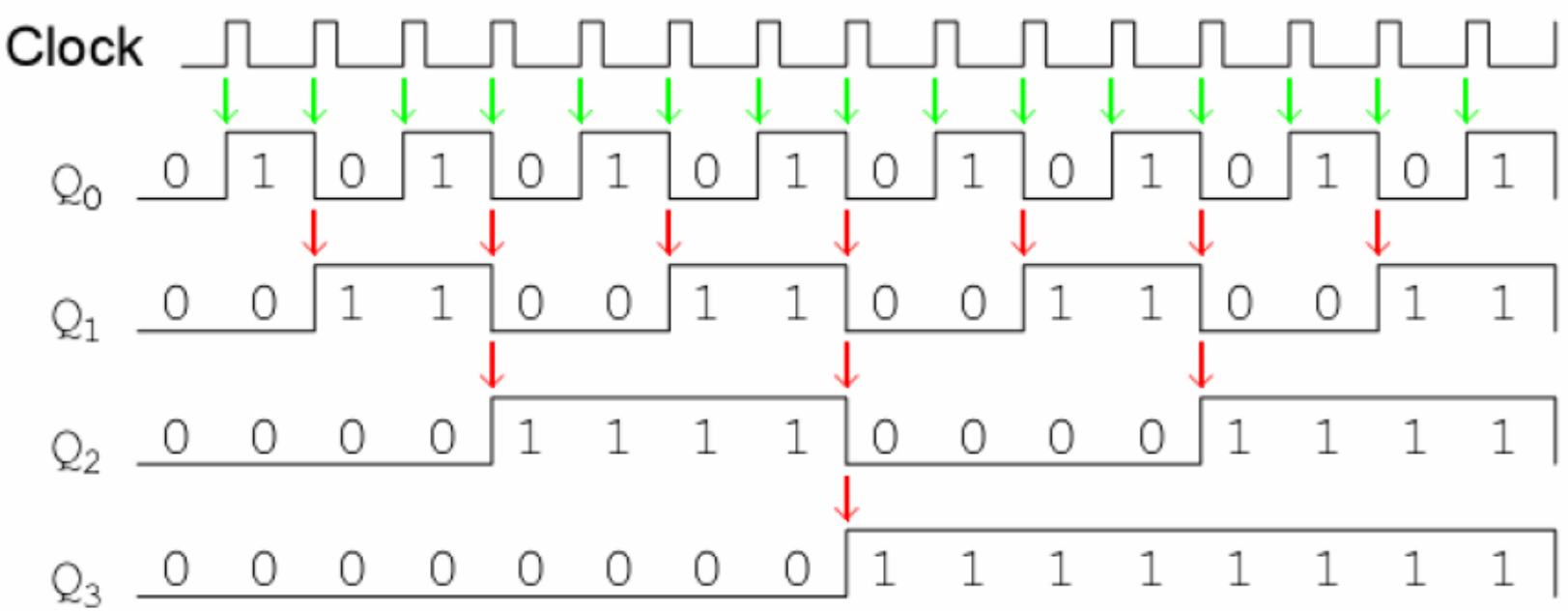


C	J	K	Q	$\overline{Q}$
⌐	0	0	latch	latch
⌐	0	1	0	1
⌐	1	0	1	0
⌐	1	1	toggle	toggle
x	0	0	latch	latch
x	0	1	latch	latch
x	1	0	latch	latch
x	1	1	latch	latch

Example


A four-bit "up" counter
Q0
Q1
Q2
Q3
Vdd
Vdd
Vdd
Vdd
J
Q
C
K
Q̄
J
Q
C
K
Q̄
J
Q
C
K
Q̄
J
Q
C
K
Q̄

Result


Clock
Q0 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1
Q1 0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1
Q2 0 0 0 0 1 1 1 1 0 0 0 0 1 1 1 1
Q3 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1