TÊN ĐỒ ÁN: THIỆT KẾ MẠCH FIFO8x4

Giáo viên phụ trách: Lâm Đức Khải

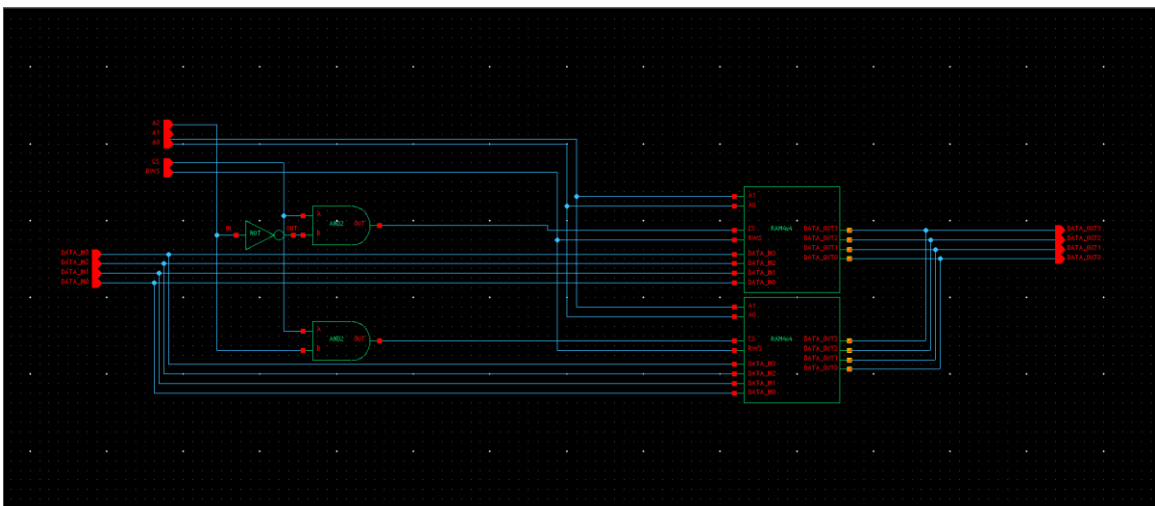| Thành viên	Họ và tên	Mã số sinh viên
1	Mai Anh Phong	18520127
2	Lưu Quyết Thắng	18520151

MỤC LỤC

MỤC 1: Theory

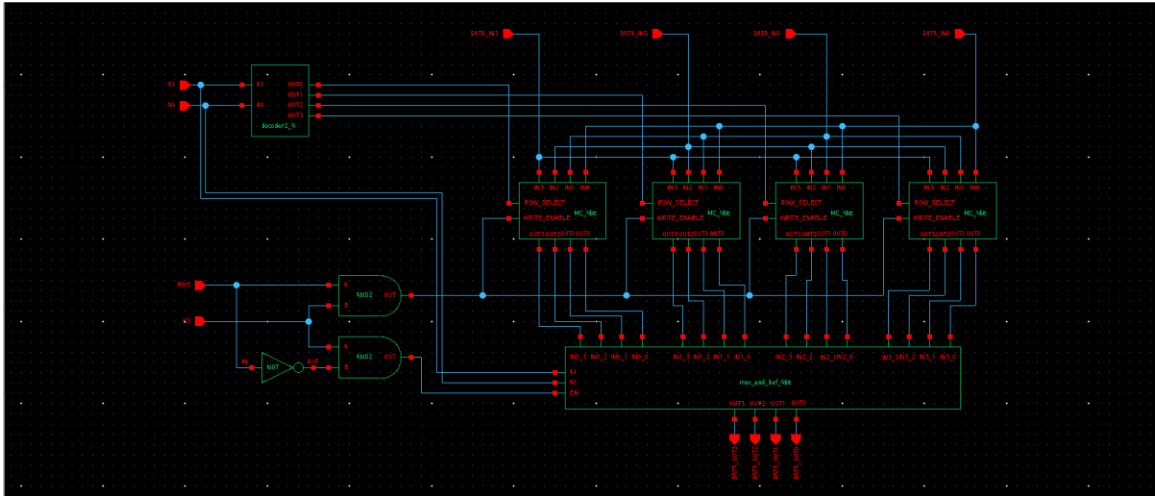**MỤC 2: Schematic design**

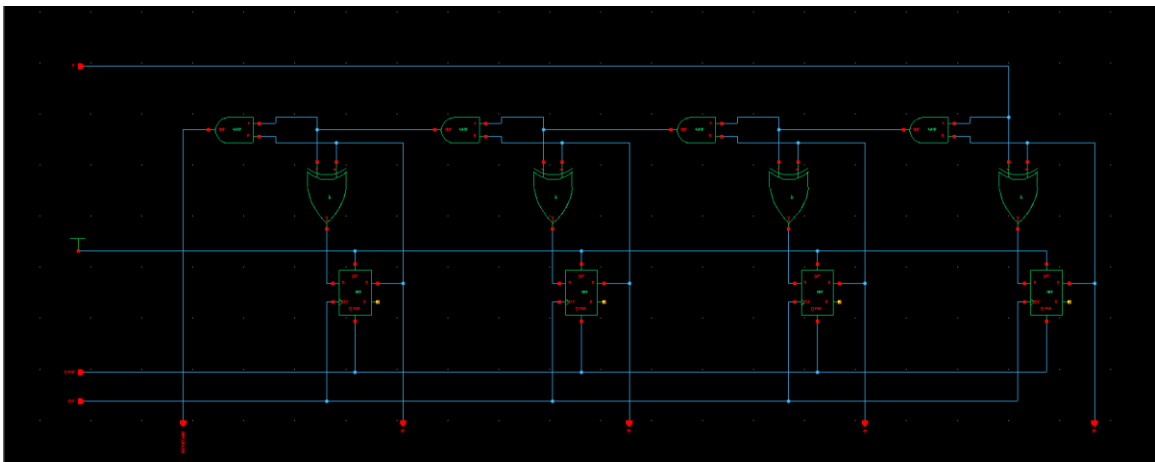**2.1. Schematic FIFO8x4**
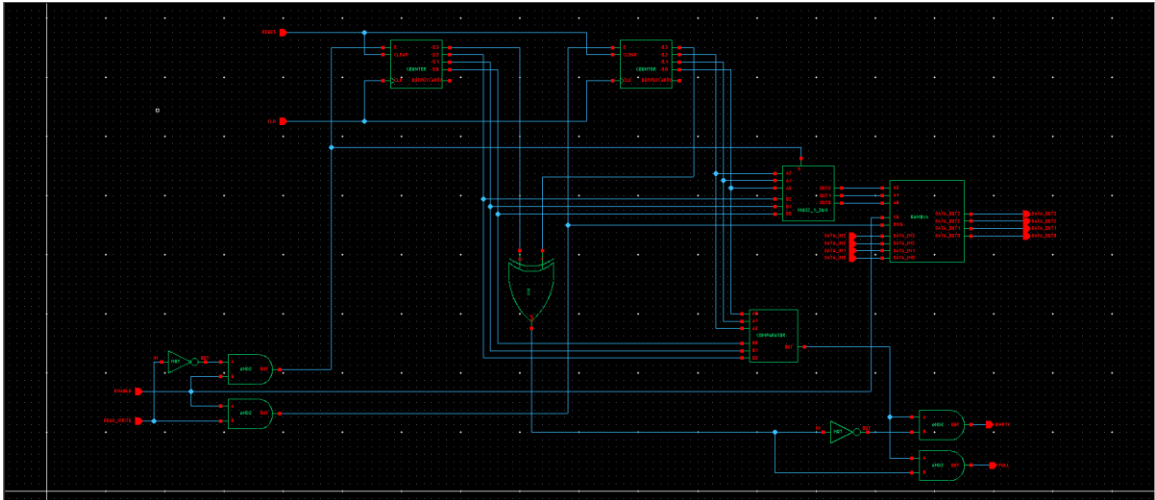
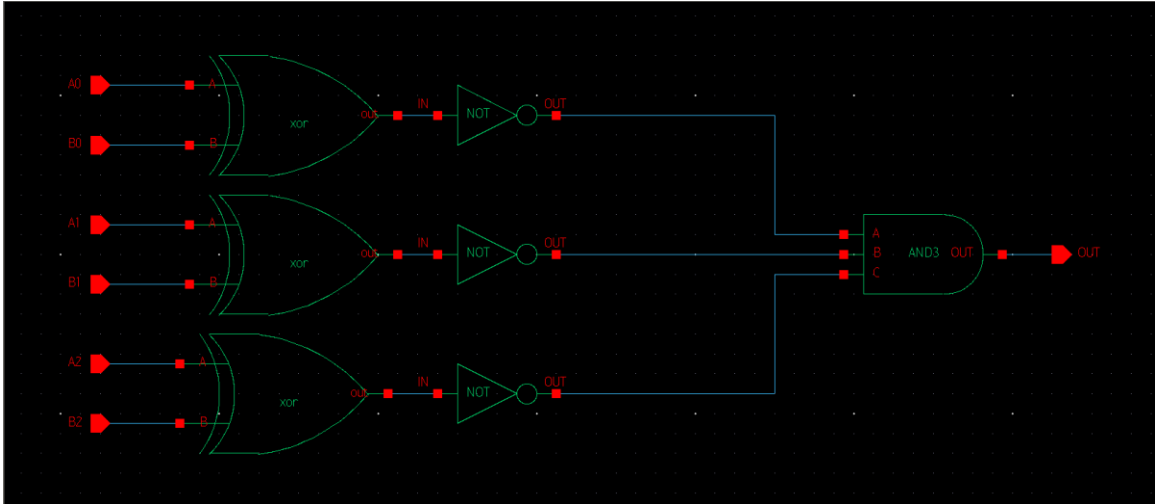## 2.2. Schematic RAM8x4

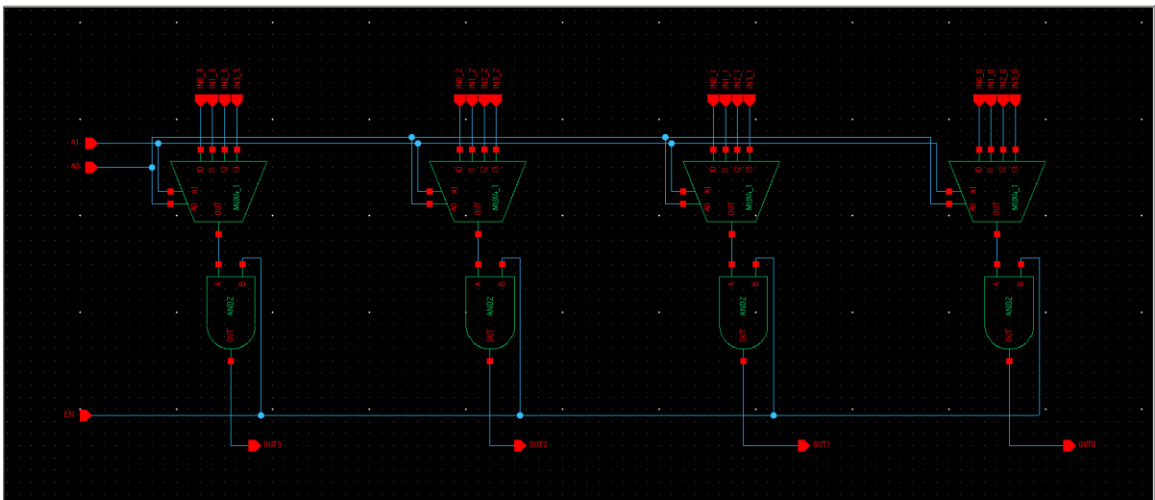*RAM8x4 được thiệt kế từ RAM4x4.*

2.3. Schematic Counter 4BIT
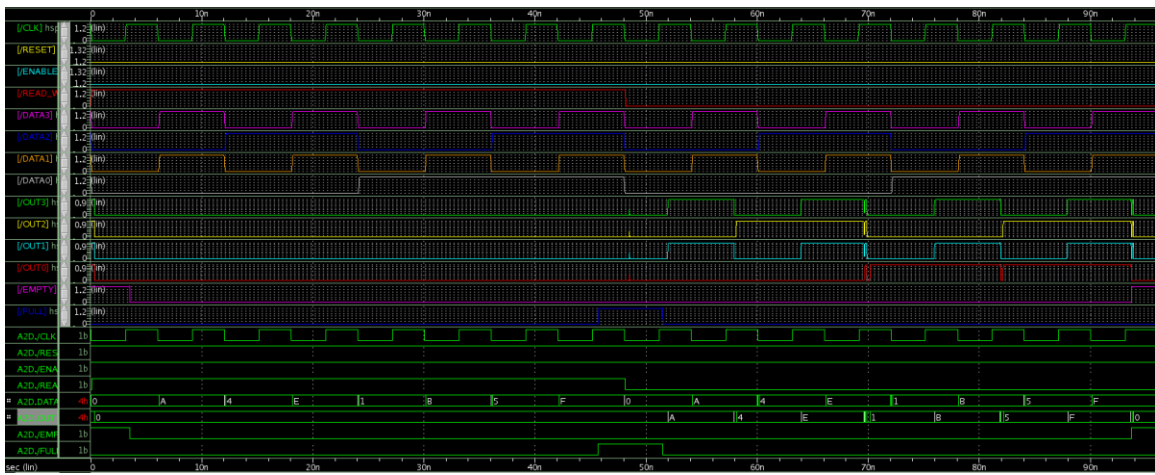

2.4. Schematic Comparator 3BIT
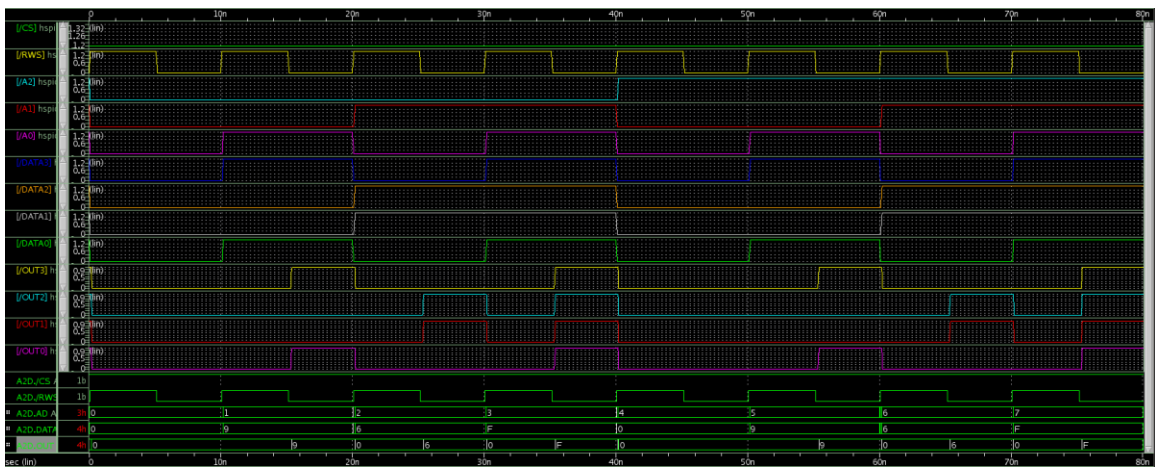
2.5. Schematic MUX41 4BIT

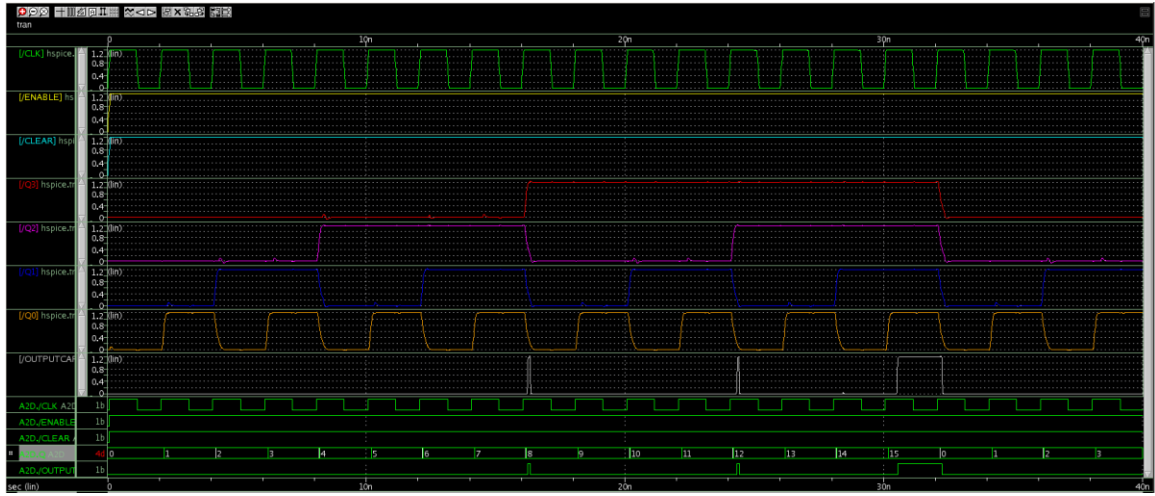## MỤC 3: HSPICE pre-layout simulation results and comments
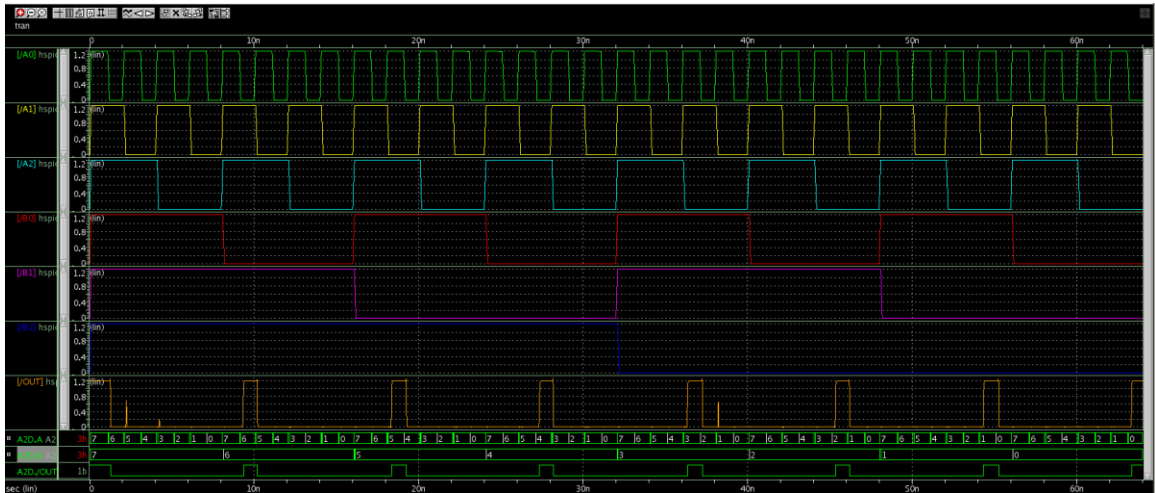
3.1. HSPICE pre-layout FIFO8x4

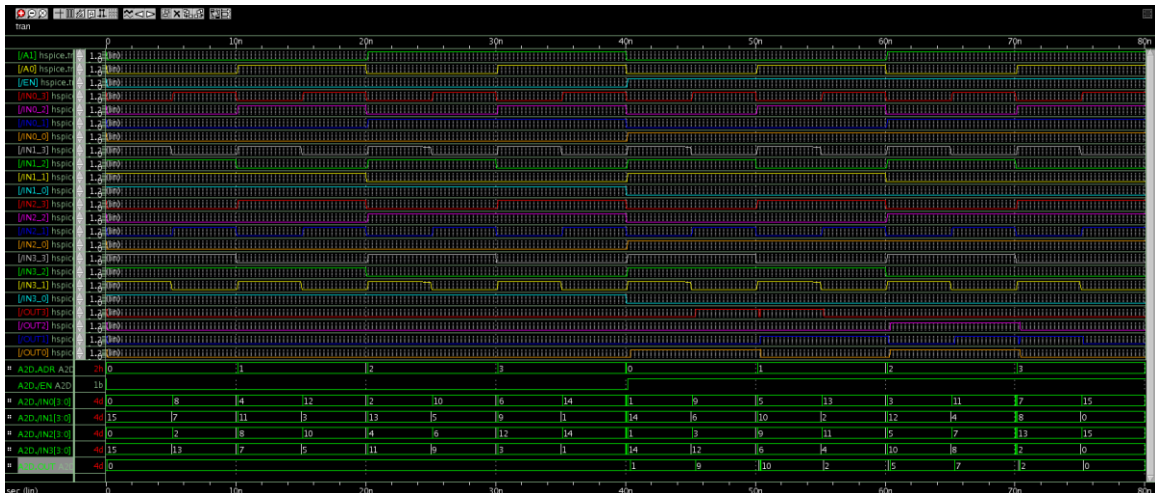## 3.2. HSPICE pre-layout RAM8x4

3.3. HSPICE pre-layout Counter 4BIT
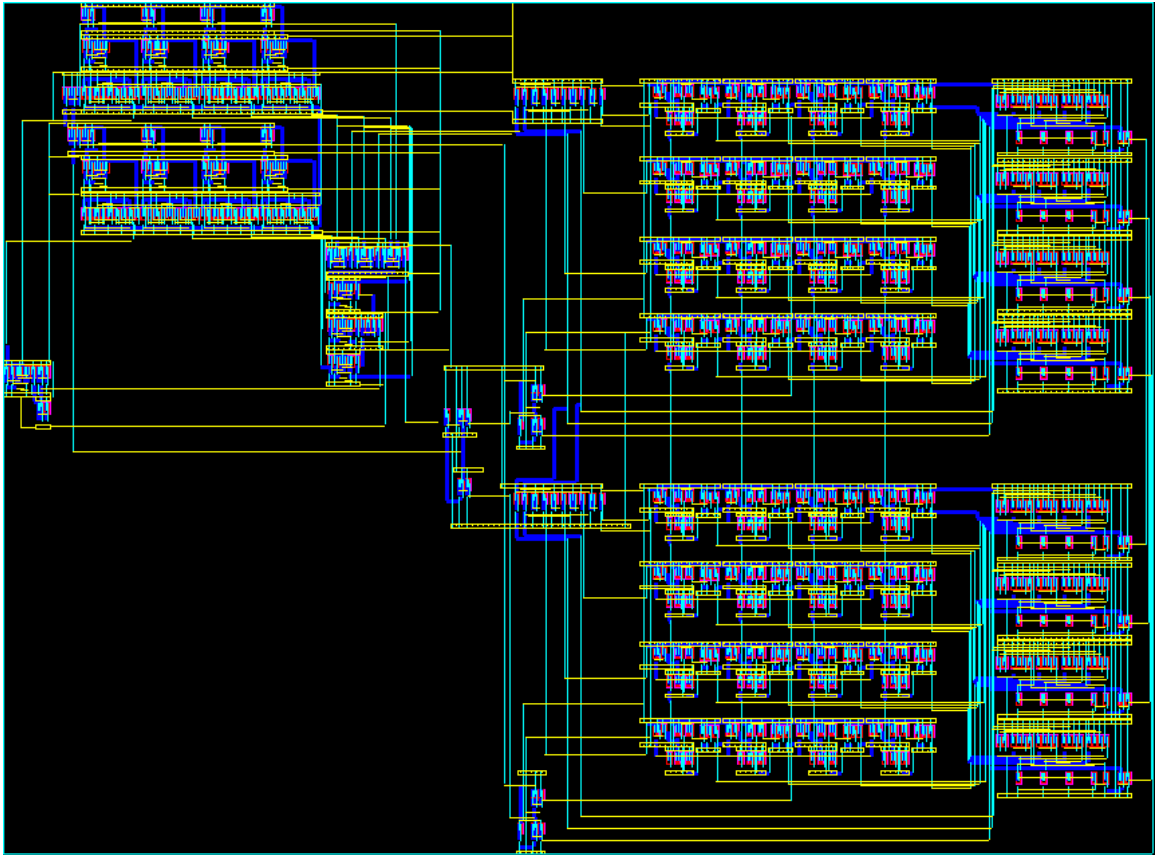

3.4. HSPICE pre-layout Comparator 3BIT
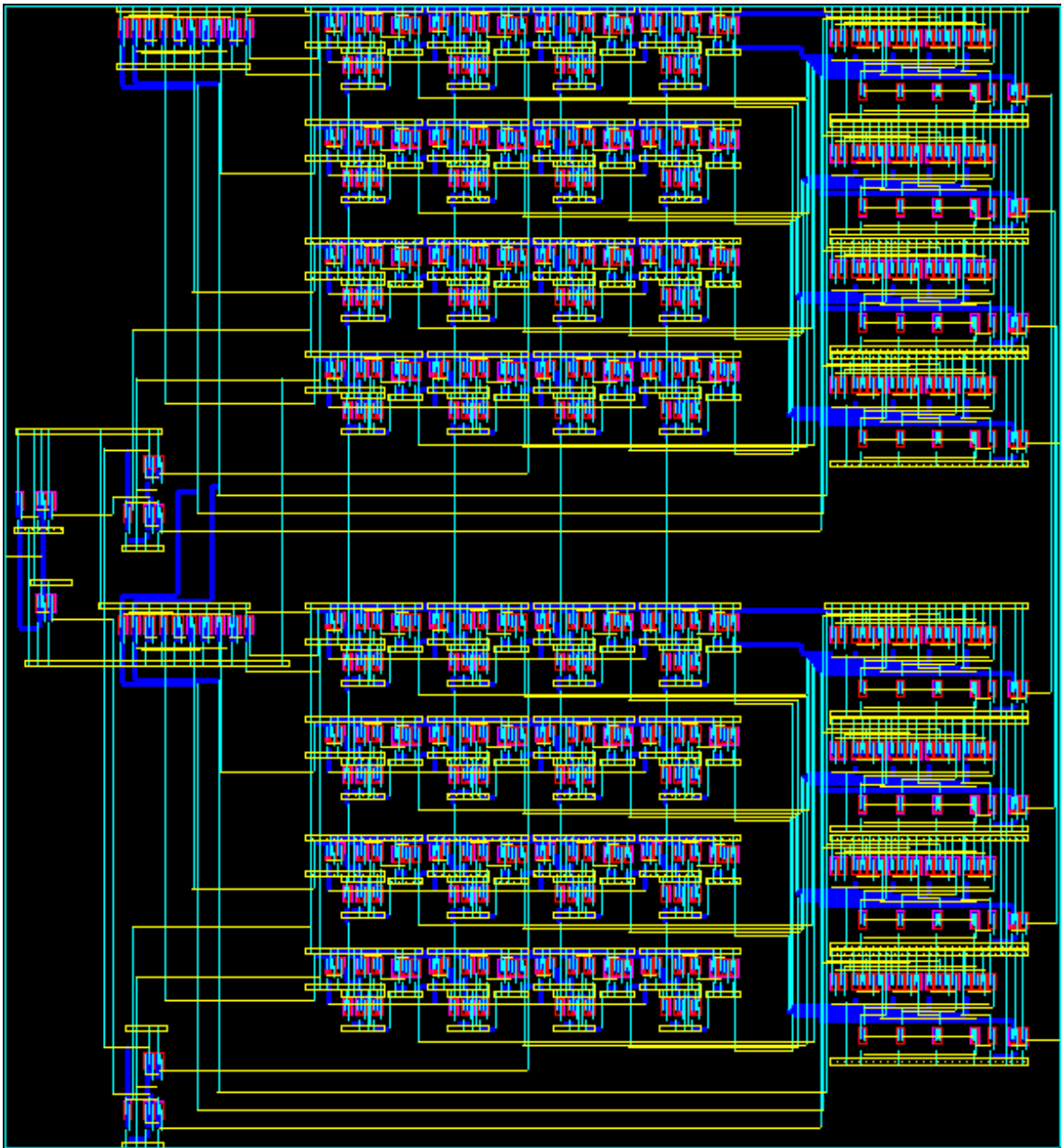

3.5. HSPICE pre-layout MUX41 4BIT

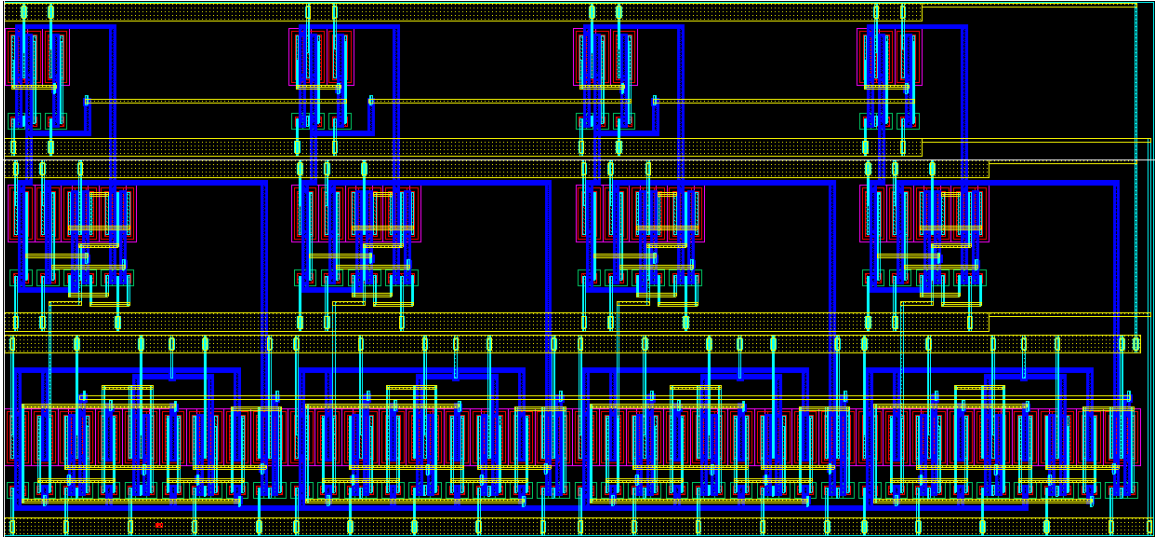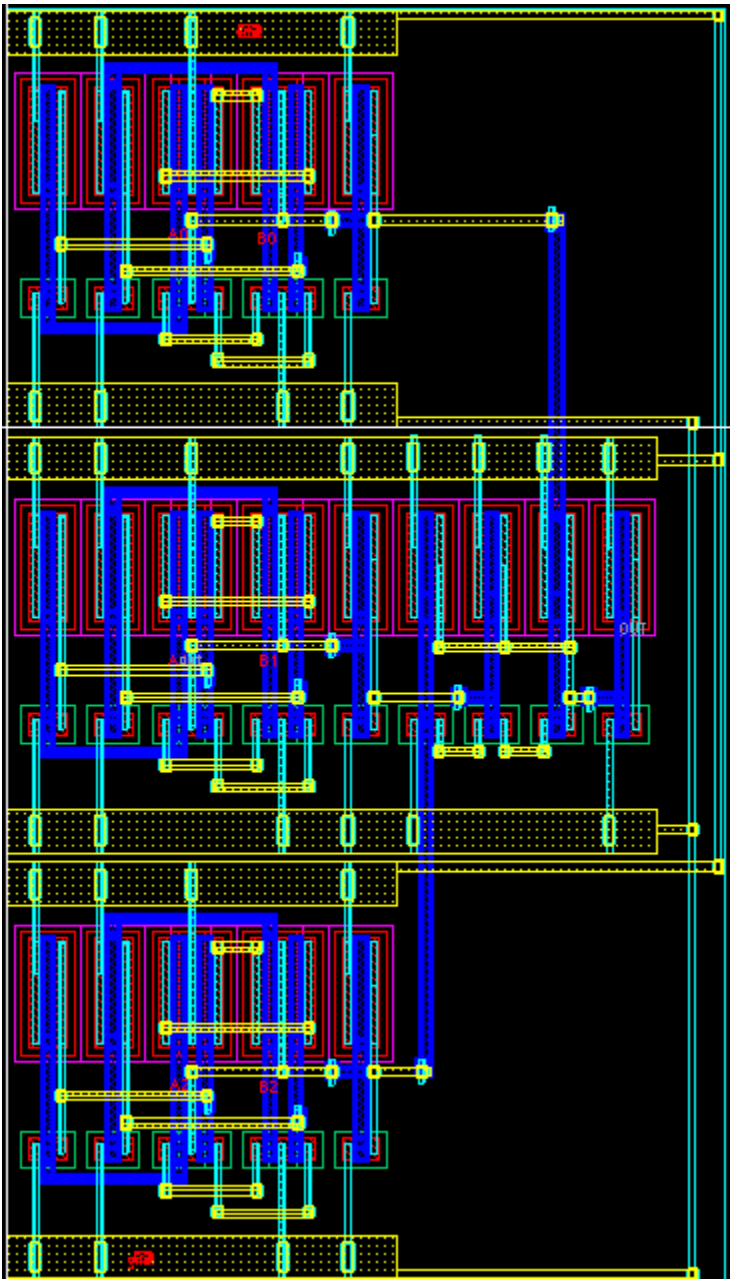# MỤC 4: Layout design

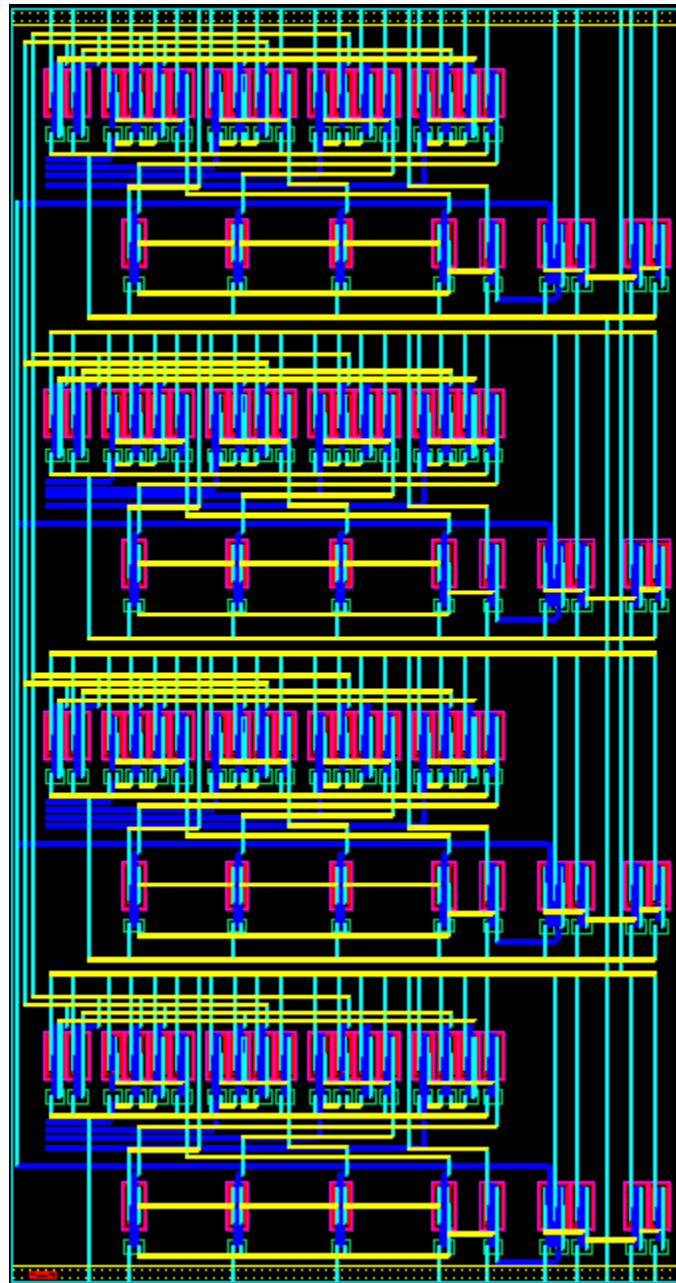## 4.1. Layout FIFO8x4

4.2. Layout RAM8x4

4.3. Layout Counter 4BIT

4.4. Layout Comparator 3BIT

4.5. Layout MUX41 4BIT

MỤC 5: DRC, LVS , Area check results

5.1. FIFO8x4

Kết quả đạt được : No rule violation ở tất cả các khối.

Hình 5.1. 1 DRC FIFO8x4

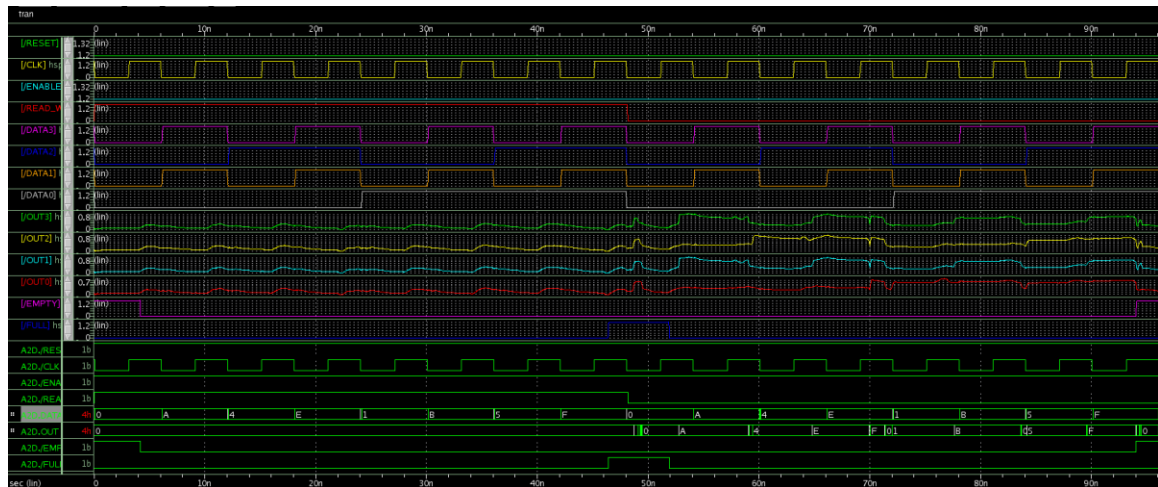*Hình 5.1 2 LVS FIFO8x4*

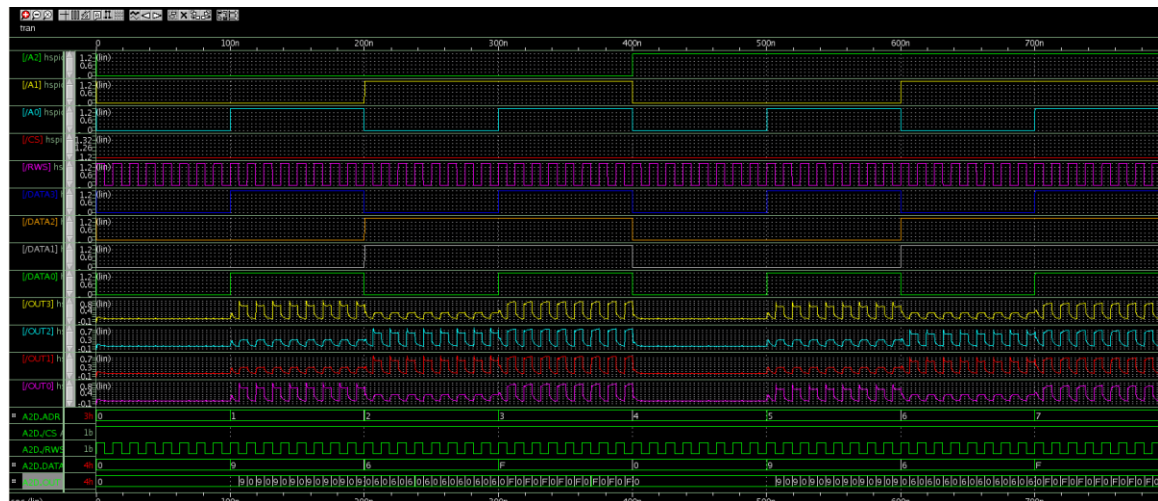*Hình 5.1 3 LPE FIFO8x4*

Hình 5.1 4. Starrc FIFO8x4

CHƯƠNG 6: HSPICE post-layout

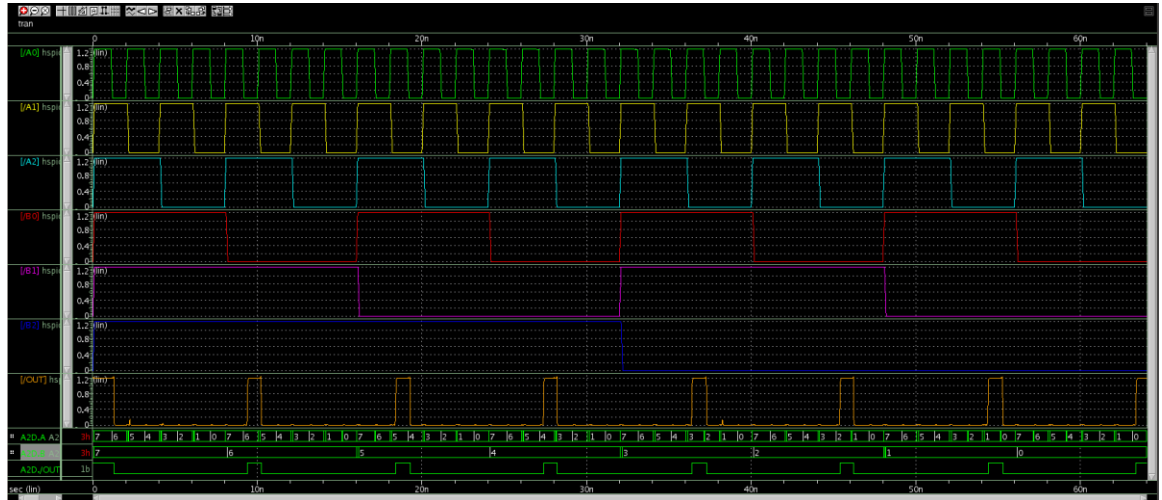## 6.1. HSPICE post-layout FIFO8x4

6.2. HSPICE post-layout RAM8x4

6.3. HSPICE post-layout Counter 4BIT

6.4. HSPICE post-layout Comparator 3BIT

6.5. HSPICE post-layout MUX41 4BIT