HEF4894B

12-stage shift-and-store register LED driver Rev. 8 — 22 November 2011

Product data sheet

1. **General description**

The HEF4894B is a 12-stage serial shift register. It has a storage latch associated with each stage for strobing data from the serial input (D) to the parallel LED driver outputs (QP0 to QP11). Data is shifted on positive-going clock (CP) transitions. The data in each shift register stage is transferred to the storage register when the strobe (STR) input is HIGH. Data in the storage register appears at the output whenever the output enable (OE) input signal is HIGH.

Two serial outputs (QS1 and QS2) are available for cascading a number of HEF4894B devices. Serial data is available at QS1 on positive-going clock edges to allow high-speed operation in cascaded systems with a fast clock rise time. The same serial data is available at QS2 on the next negative going clock edge. This is used for cascading HEF4894B devices when the clock has a slow rise time.

It operates over a recommended V_{DD} power supply range of 3 V to 15 V referenced to V_{SS} (usually ground). Unused inputs must be connected to V_{DD}, V_{SS}, or another input.

Features and benefits 2.

- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Specified from -40 °C to +85 °C and -40 °C to +125 °C
- Complies with JEDEC standard JESD 13-B

3. **Ordering information**

Ordering information

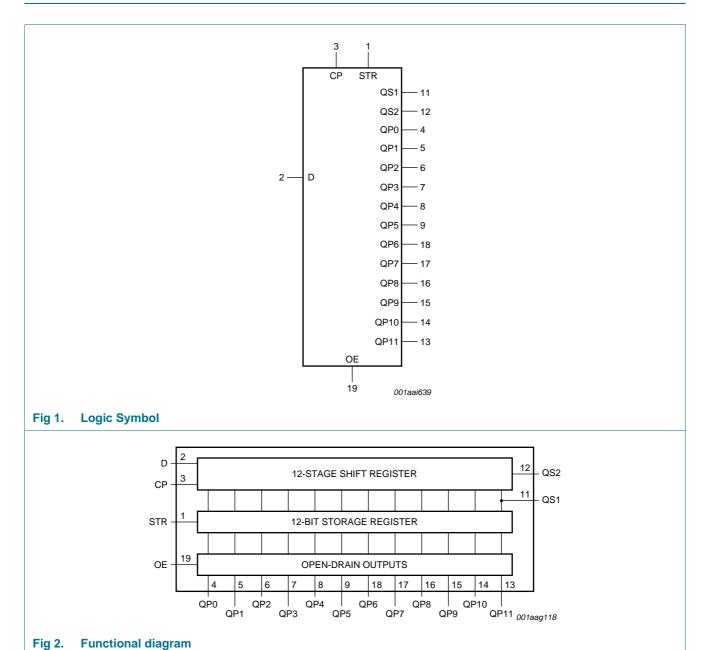
All types operate from $-40 \,^{\circ}\text{C}$ to $+125 \,^{\circ}\text{C}$.

Type number	Package	Package Package								
	Name	Description	Version							
HEF4894BP	DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1							
HEF4894BT	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1							
HEF4894BTT	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1							

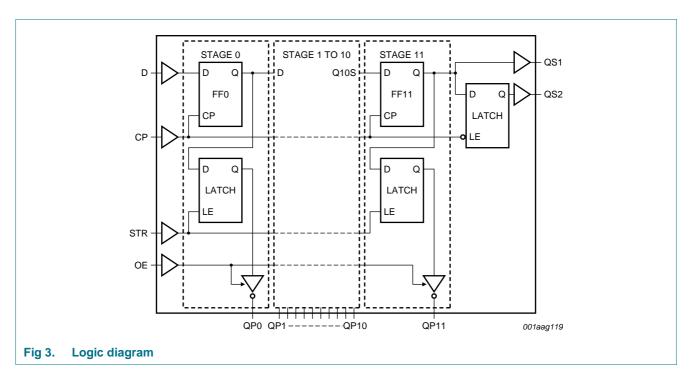


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4. Functional diagram

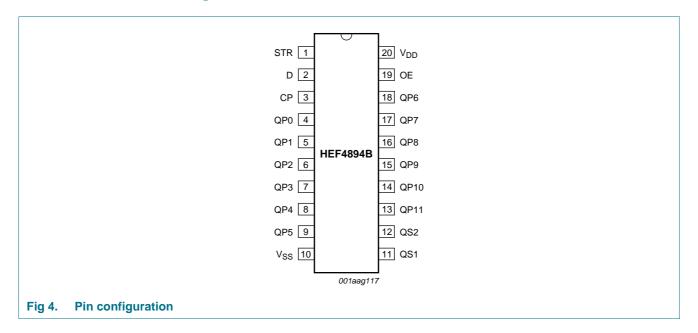


12-stage shift-and-store register LED driver



5. Pinning information

5.1 Pinning



12-stage shift-and-store register LED driver

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
D	2	serial input
QP0 to QP11	4, 5, 6, 7, 8, 9, 18, 17, 16, 15, 14, 13	parallel output
QS1	11	serial output
QS2	12	serial output
СР	3	clock input
STR	1	strobe input
OE	19	output enable input
V_{DD}	20	supply voltage
V_{SS}	10	ground (0 V)

6. Functional description

Table 3. Function table[1]

At the positive clock edge the information in the 10th register stage is transferred to the 11th register stage and the QS output

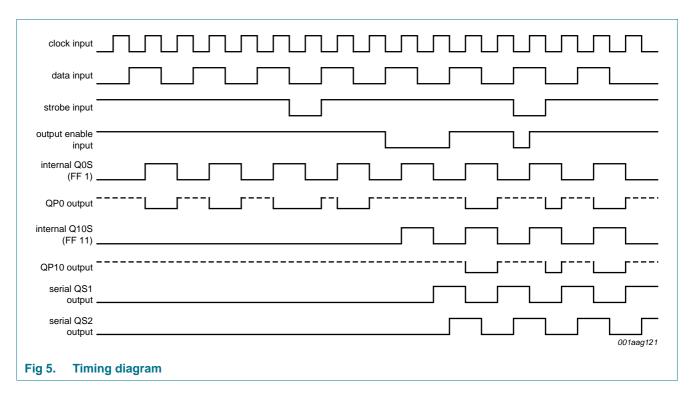
Control			Input	Parallel outp	out	Serial outpu	Serial output		
CP	OE	STR	D	QP0	QPn	QS1[2]	QS2[3]		
\uparrow	L	X	X	Z	Z	Q10S	no change		
\downarrow	L	X	X	Z	Z	no change	Q11S		
\uparrow	Н	L	Х	no change	no change	Q10S	no change		
\uparrow	Н	Н	L	Z	QPn – 1	Q10S	no change		
\uparrow	Н	Н	Н	L	QPn – 1	Q10S	no change		
	Н	Н	Н	no change	no change	no change	Q11S		

^[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; ↑ = LOW-to-HIGH clock transition; ↓ = HIGH-to-LOW clock transition; Z = high-impedance OFF-state.

^[2] Q10S = the data in register stage 10 before the LOW to HIGH clock transition.

^[3] Q11S = the data in register stage 11 before the HIGH to LOW clock transition.

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7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		-0.5	+18	V
I _{IK}	input clamping current	$V_I < -0.5 \text{ V or } V_I > V_{DD} + 0.5 \text{ V}$	-	±10	mΑ
V_{I}	input voltage		-0.5	$V_{DD} + 0.5$	V
l _{OK}	output clamping current	QSn outputs; $V_O < -0.5 \text{ V or } V_O > V_{DD} + 0.5 \text{ V}$	-	±10	mA
		QPn outputs; V _O < 0.5 V	-	40	mA
I _I	input leakage current		-	±10	mA
lo	output current	QSn outputs	-	±10	mA
		QPn outputs	-	40	mA
T _{stg}	storage temperature		-65	+150	°C
T _{amb}	ambient temperature		-40	+125	°C
P _{tot}	total power dissipation	$T_{amb} = -40 ^{\circ}\text{C}$ to +125 $^{\circ}\text{C}$			
		DIP20 package	<u>[1]</u> -	750	mW
		SO20 package	[2] _	500	mW
		TSSOP20 package	[3] _	500	mW
Р	power dissipation	per output	-	100	mW

^[1] For DIP20 package: P_{tot} derates linearly with 12 mW/K above 70 °C.

HEF4894B

^[2] For SO20 package: Ptot derates linearly with 8 mW/K above 70 °C.

^[3] For TSSOP20 package: Ptot derates linearly with 5.5 mW/K above 60 °C.

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8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V_{DD}	supply voltage		3	-	15	V
VI	input voltage		0	-	V_{DD}	V
T _{amb}	ambient temperature	in free air	-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	$V_{DD} = 5 V$	-	-	3.75	μs/V
		V _{DD} = 10 V	-	-	0.5	μs/V
		V _{DD} = 15 V	-	-	0.08	μs/V

9. Static characteristics

Table 6. Static characteristics

 $V_{SS} = 0$ V; $V_I = V_{SS}$ or V_{DD} ; unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD}	T _{amb} =	–40 °C	T _{amb} =	+25 °C	T _{amb} =	+85 °C	T _{amb} = -	⊦125 °C	Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	HIGH-level	$ I_{O} < 1 \mu A$	5 V	3.5	-	3.5	-	3.5	-	3.5	-	V
	input voltage		10 V	7.0	-	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	11.0	-	V
V _{IL}	LOW-level	$ I_{O} < 1 \mu A$	5 V	-	1.5	-	1.5	-	1.5	-	1.5	V
	input voltage		10 V	-	3.0	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	-	4.0	V
V _{OH}	HIGH-level	QSn outputs;	5 V	4.95	-	4.95	-	4.95	-	4.95	-	V
	output voltage	$ I_{O} < 1 \mu A$	10 V	9.95	-	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	14.95	-	V
	LOW-level output voltage	QSn outputs;	5 V	-	0.05	-	0.05	-	0.05	-	0.05	V
		$ I_{O} < 1 \mu A$	10 V	-	0.05	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	-	0.05	V
		QPn outputs; $ I_O < 20 \text{ mA}$	5 V	-	0.75	-	0.75	-	1.5	-	1.5	V
			10 V	-	0.75	-	0.75	-	1.5	-	1.5	V
			15 V	-	0.75	-	0.75	-	1.5	-	1.5	V
I_{OH}	HIGH-level	QSn outputs										
	output current	$V_0 = 2.5 \text{ V}$	5 V	-	-1.7	-	-1.4	-	-1.1	-	-1.1	mΑ
		$V_0 = 4.6 \text{ V}$	5 V	-	-0.64	-	-0.5	-	-0.36	-	-0.36	mΑ
		$V_0 = 9.5 V$	10 V	-	-1.6	-	-1.3	-	-0.9	-	-0.9	mΑ
		V _O = 13.5 V	15 V	-	-4.2	-	-3.4	-	-2.4	-	-2.4	mΑ
I _{OL}	LOW-level	QSn outputs										
	output current	$V_0 = 0.4 \text{ V}$	5 V	0.64	-	0.5	-	0.36	-	0.36	-	mΑ
		$V_{O} = 0.5 \ V$	10 V	1.6	-	1.3	-	0.9	-	0.9	-	mA
		V _O = 1.5 V	15 V	4.2	-	3.2	-	2.4	-	2.4	-	mA
l _l	input leakage current		15 V	-	±0.1	-	±0.1	-	±1.0	-	±1.0	μА

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 Table 6.
 Static characteristics ...continued

 $V_{SS} = 0$ V; $V_{I} = V_{SS}$ or V_{DD} ; unless otherwise specified.

Symbol	Parameter	Conditions	V _{DD}	T _{amb} = -40 °C		T _{amb} = +25 °C		$T_{amb} = +85 ^{\circ}C$		T _{amb} = +125 °C		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
I _{OZ} OFF-state output current		QPn output is HIGH; V _O = 15 V	5 V	-	2	-	2	-	15	-	15	μΑ
	output current		10 V	-	2	-	2	-	15	-	15	μΑ
		VO = 13 V	15 V	-	2	-	2	-	15	-	15	μΑ
I _{DD}	supply current	I _O = 0 A	5 V	-	5	-	5	-	150	-	150	μΑ
			10 V	-	10	-	10	-	300	-	300	μΑ
			15 V	-	20	-	20	-	600	-	600	μΑ
C _I	input capacitance		-	-	-	-	7.5	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

 $V_{SS} = 0 \text{ V}$; $T_{amb} = 25 \text{ °C}$ unless otherwise specified. For test circuit see <u>Figure 10</u>.

Symbol	Parameter	Conditions	V _{DD}	Extrapolation formula	Min	Тур	Max	Unit
t _{PHL}	HIGH to LOW	CP to QS1;	5 V	132 ns + (0.55 ns/pF)C _L	-	160	320	ns
	propagation delay	see Figure 6	10 V	53 ns + (0.23 ns/pF)C _L	-	65	130	ns
			15 V	37 ns + (0.16 ns/pF)C _L	-	45	90	ns
		CP to QS2;	5 V	92 ns + (0.55 ns/pF)C _L	-	120	240	ns
		see Figure 6	10 V	39 ns + (0.23 ns/pF)C _L	-	50	100	ns
		15 V	32 ns + (0.16 ns/pF)C _L	-	40	80	ns	
t _{PLH}	LOW to HIGH	CP to QS1;	5 V	102 ns + (0.55 ns/pF)C _L	-	130	260	ns
	propagation delay	see Figure 6	10 V	44 ns + (0.23 ns/pF)C _L	-	55	110	ns
			15 V	32 ns + $(0.16 \text{ ns/pF})C_L$	-	40	80	ns
		CP to QS2;	5 V	102 ns + $(0.55 \text{ ns/pF})C_L$	-	130	260	ns
		see <u>Figure 6</u>	10 V	49 ns + $(0.23 \text{ ns/pF})C_L$	-	60	120	ns
			15 V	$37 \text{ ns} + (0.16 \text{ ns/pF})C_L$	-	45	90	ns
t_{PZL}	OFF-state to LOW	CP to QPn; see <u>Figure 6</u>	5 V		-	240	480	ns
	propagation delay		10 V		-	80	160	ns
			15 V		-	55	110	ns
		STR to QPn;	5 V		-	140	280	ns
		see <u>Figure 7</u>	10 V		-	70	140	ns
			15 V		-	55	110	ns
t_{PLZ}	LOW to OFF-state	CP to QPn;	5 V		-	170	340	ns
	propagation delay	see <u>Figure 6</u> and <u>7</u>	10 V		-	75	150	ns
			15 V		-	60	120	ns
		STR to QPn;	5 V		-	100	200	ns
		see Figure 7	10 V		-	40	100	ns
			15 V		-	35	70	ns

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 Table 7.
 Dynamic characteristics ...continued

 $V_{SS} = 0 \text{ V}$; $T_{amb} = 25 ^{\circ}\text{C}$ unless otherwise specified. For test circuit see <u>Figure 10</u>.

Symbol	Parameter	Conditions	V_{DD}		Extrapolation formula	Min	Тур	Max	Unit
t _{en}		OE to QPn;	5 V	[2]		-	100	200	ns
		see Figure 8	10 V			-	55	110	ns
			15 V			-	50	100	ns
t _{dis}		OE to QPn;	5 V	[2]		-	80	160	ns
		see Figure 8	10 V			-	40	80	ns
			15 V			-	30	60	ns
t _t	transition time	QS1, QS2;	5 V	[1][3]	35 ns + (1.00 ns/pF)C _L	-	85	170	ns
		see Figure 6	10 V		19 ns + (0.42 ns/pF)C _L	-	40	80	ns
			15 V		16 ns + (0.28 ns/pF)C _L	-	30	60	ns
t_{W}	pulse width	CP; LOW and HIGH; see <u>Figure 6</u>	5 V			60	30	-	ns
			10 V			30	15	-	ns
			15 V			24	12	-	ns
		STR; HIGH; see <u>Figure 7</u>	5 V			80	40	-	ns
			10 V			60	30	-	ns
			15 V			24	12	-	ns
t _{su}	set-up time	D to CP;	5 V			60	30	-	ns
		see Figure 9	10 V			20	10	-	ns
			15 V			15	5	-	ns
t _h	hold time	D to CP;	5 V			+5	-15	-	ns
		see <u>Figure 9</u>	10 V			20	5	-	ns
			15 V			20	5	-	ns
f _{clk(max)}	maximum clock	CP; see Figure 6	5 V			5	10	-	MHz
	frequency	_	10 V			11	22	-	MHz
			15 V			14	28	-	MHz

^[1] The typical values of the propagation delay and transition times are calculated from the extrapolation formulas shown (C_L in pF).

Table 8. Dynamic power dissipation

 P_D can be calculated from the formulas shown. $V_{SS} = 0$ V; $t_r = t_f \le 20$ ns; $T_{amb} = 25$ °C.

Symbol	Parameter	V_{DD}	Typical formula	Where			
,	dynamic power	5 V	$P_D = 1200 \times f_i + \Sigma (f_o \times C_L) \times V_{DD}^2 \mu W$	f_i = input frequency in MHz;			
	dissipation	10 V	$P_D = 5550 \times f_i + \Sigma (f_o \times C_L) \times V_{DD}^2 \mu W$	f _o = output frequency in MHz; C _L = output load capacitance in pF;			
		15 V	$P_D = 15000 \times f_i + \Sigma (f_o \times C_L) \times V_{DD}^2 \mu W$	$\Sigma(f_o \times C_L)$ = sum of the outputs; V_{DD} = supply voltage in V.			

^[2] t_{en} is the same as t_{PZL} and t_{dis} is the same as t_{PLZ} .

^[3] t_t is the same as t_{TLH} and t_{THL} .

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11. Waveforms

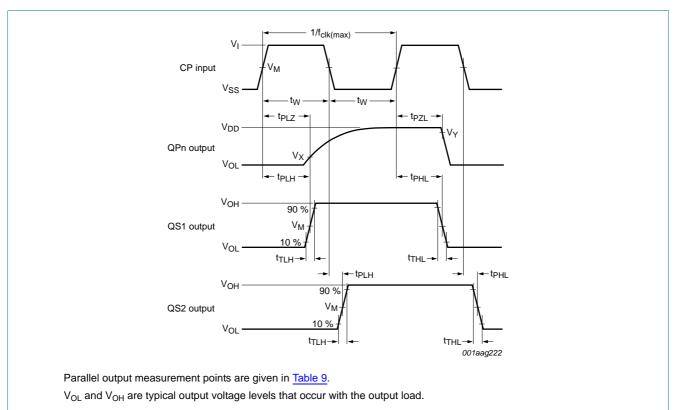
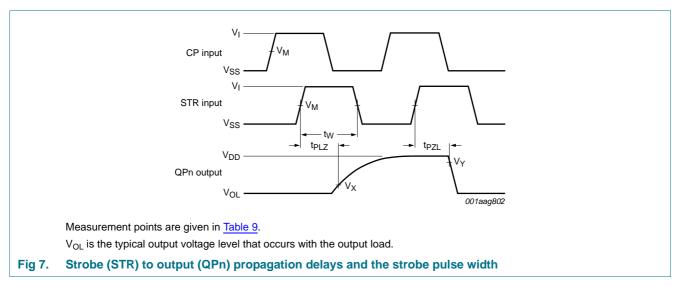


Fig 6. Propagation delay clock (CP) to output (QPn, QS1, QS2), clock pulse width and maximum clock frequency

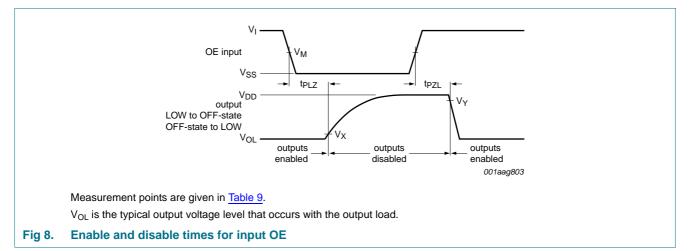
Table 9. Measurement points

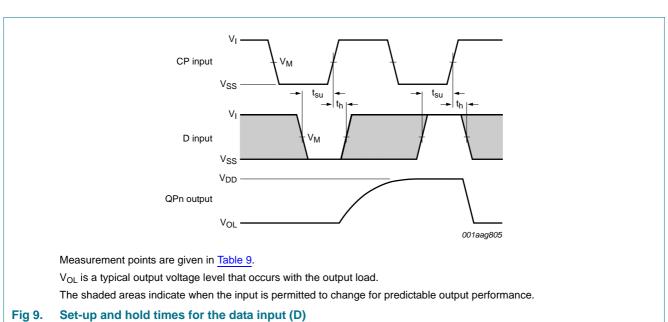
Supply	Input	Output		
V_{DD}	V _M	V _M	V _X	V _Y
5 V to 15 V	0.5V _{DD}	0.5V _{DD}	0.1V _O	0.9V _O



HEF4894B

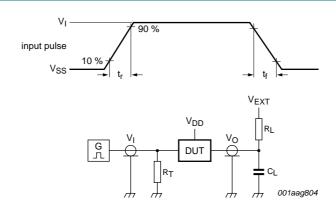
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Test data is given in Table 10.

Definitions for test circuit:

DUT = Device Under Test;

R_L = Load resistance;

C_L = load capacitance;

 R_T = Termination resistance should be equal to output impedance of Z_0 of the pulse generator;

 V_{EXT} = External voltage for measuring switching times.

Fig 10. Test circuit for measuring switching times

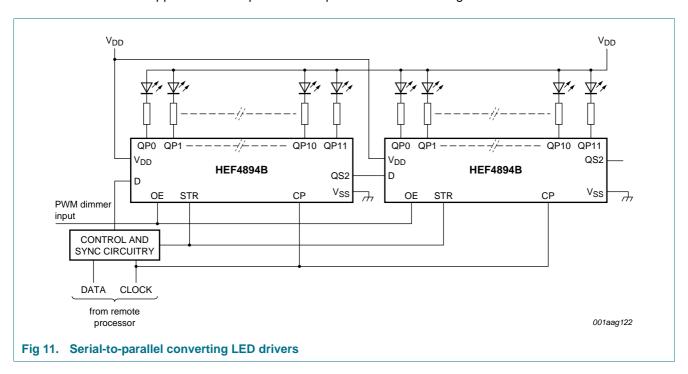
Table 10. Test data

Supply	Input		V _{EXT}		Load		
V_{DD}	VI	t _r , t _f	t _{PLZ} , t _{PZL}	t _{PLH} , t _{PHL}	CL	R _L	
5 V to 15 V	V_{DD}	≤ 20 ns	V_{DD}	open	50 pF	1 kΩ	

12-stage shift-and-store register LED driver

12. Application information

Application example: serial-to-parallel data converting LED driver.

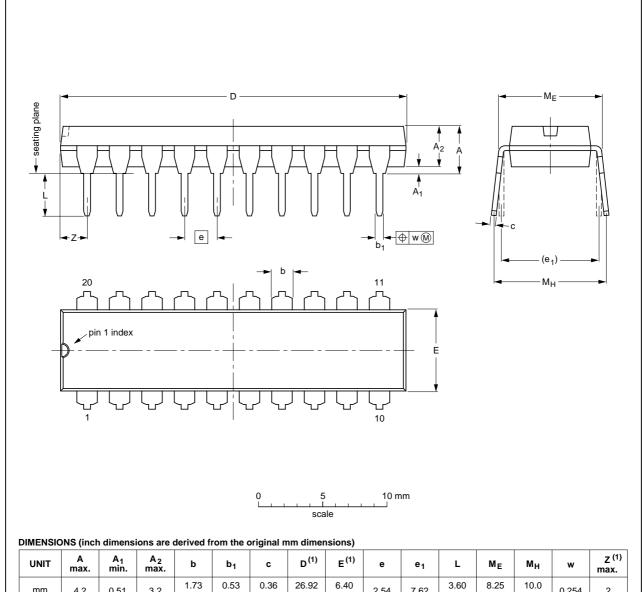


12-stage shift-and-store register LED driver

13. Package outline

DIP20: plastic dual in-line package; 20 leads (300 mil)

SOT146-1



	•					•									
UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	С	D ⁽¹⁾	E ⁽¹⁾	е	e ₁	L	ME	Мн	w	Z ⁽¹⁾ max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2
inches	0.17	0.02	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE		REFER	EUROPEAN	ISSUE DATE			
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE	
SOT146-1		MS-001	SC-603			99-12-27 03-02-13	

Fig 12. Package outline SOT146-1 (DIP20)

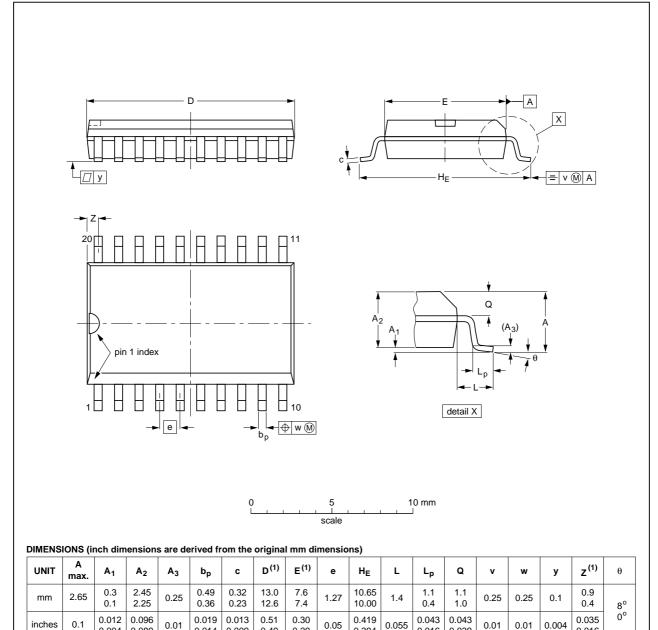
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SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

0.014

0.009

0.49

OUTLINE		REFER	EUROPEAN	ISSUE DATE			
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE	
SOT163-1	075E04	MS-013				99-12-27 03-02-19	

0.394

0.016

0.039

Fig 13. Package outline SOT163-1 (SO20)

0.004

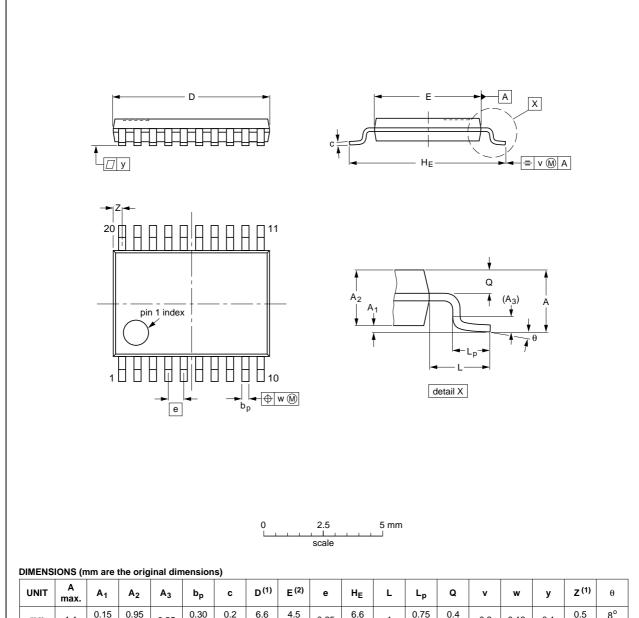
0.089

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TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1



UNIT	A max.	A ₁	A ₂	A ₃	bp	С	D ⁽¹⁾	E ⁽²⁾	е	HE	L	Lp	ø	v	w	у	Z ⁽¹⁾	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE		REFER	EUROPEAN	ISSUE DATE			
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE	
SOT360-1		MO-153				99-12-27 03-02-19	

Fig 14. Package outline SOT360-1 (TSSOP20)

12-stage shift-and-store register LED driver

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4894B v.8	20111122	Product data sheet	-	HEF4894B v.7
Modifications:	 Section App 	olications removed		
	 <u>Table 6</u>: I_{OH} 	minimum values changed t	o maximum	
HEF4894B v.7	20100813	Product data sheet	-	HEF4894B v.6
HEF4894B v.6	20100408	Product data sheet	-	HEF4894B v.5
HEF4894B v.5	20091222	Product data sheet	-	HEF4894B v.4
HEF4894B v.4	20080827	Product data sheet	-	HEF4894B_CNV v.3
HEF4894B_CNV v.3	19950101	Product specification	-	HEF4894B_CNV v.2
HEF4894B_CNV v.2	19950101	Product specification	-	-

12-stage shift-and-store register LED driver

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design
- [2] The term 'short data sheet' is explained in section "Definitions"
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

15.2 Definitions

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12-stage shift-and-store register LED driver

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