COMP3211/COMP9211 Computer Architecture

Lab 3 Pipelined Processor

The lab is the extension of your work of Lab 2.

Goals

1. Build a simple pipelined processor.
2. Learn how to model, debug, and evaluate your design.

Tasks:

Task 1: (20 marks)

Based on the single-cycle processor you built in Lab 2, build a pipelined processor model and the pipeline can also handle data hazards for the conditional branch instruction BNE.

Task 2: (20 marks)

Verify the function of your model and determine the minimal clock cycle time of the pipeline.

For each task, you need also to design how to effectively present your work during the peer assessment. For example, your presentation for Task 1 may focus on techniques of building the pipeline model; while for Task 2, your presentation may focus on the strategy of verification and results.

Due Time: your TLB class in Week 7.

Peer Assessment Scheme:

Your work on the lab tasks will be assessed by your peer students and tutor. Similar for Labs 1 & 2, for this lab

- Your TLB class is randomly divided into (up to) two assessement groups, each capped at 12 students. This is to allow sufficient time for the assessment. For a small TLB class, only one assessment group may be required.

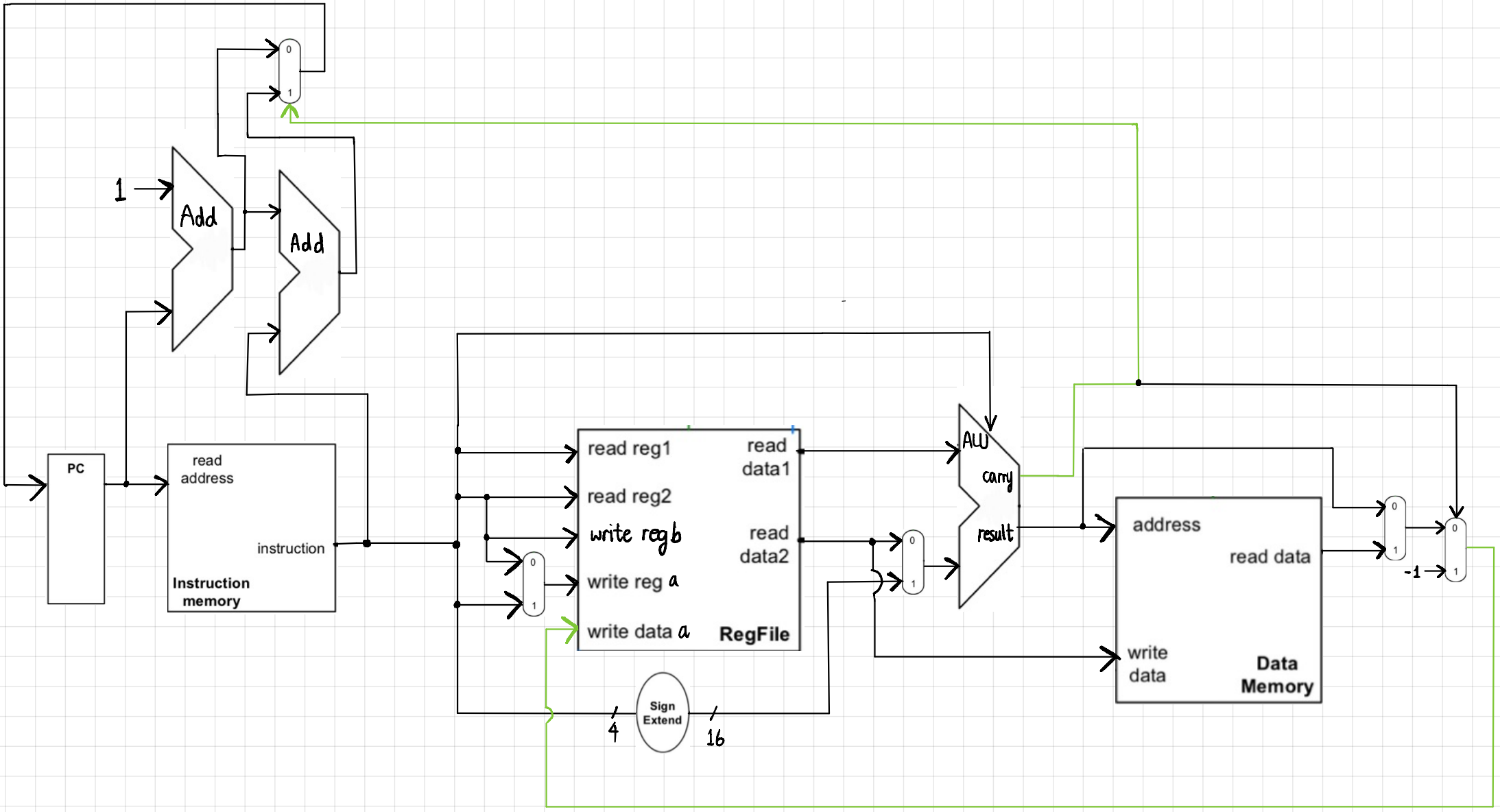
For the f2f classes, the assessement will be conducted in the on-campus classroom and for the online class, the assessment will be conducted in a MS Teams meeting.
The arrangment for each assessment group will be available in the Files folder of your class Teams channel.

- During assessment, each student is given 6 mins for presentation and 2 mins for Q&A.
    - The presentation covers three areas: design idea, HDL model, simulation results, and any discussion required for each task.
- Your work is assessed based on three categories (Presentation, Completion, and Quality). Among the three categories, Completion is rated in 0-7 and the other two each are rated in 0-5. Optionally you can add comments (your comments will be anonymously available individual assessees). See the guideline below:
    - Presentation (0-5)
        - Clarity (2)
        - Logic (2)
        - Timing management (1)
    - Completion (0-7)
        - For Task 1
            - Design (3)
            - HDL model (4)
        - For Task 2
            - Validation (5)
            - Discussion (2)
    - Quality (0-5)
        - You can give marks based on different aspects demonstrated in the lab work, for example, an interesting design idea, a clever modeling strategy, good design analysis, thorough evaluation, and adequate discussion.

The link of an assessment form will be available in your MS teams channel.

- Your tutor will organize and steer the lab session.
  By the end of the lab class, all students are required to submit their assessment forms. Your participation to the assessment will be taken into account to the overall lab participation marks.

- Your marks are determined by
    - 80% from peers, and
    - 20% from tutor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address
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read reg1
read reg2
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write reg a
write data a
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RegFile
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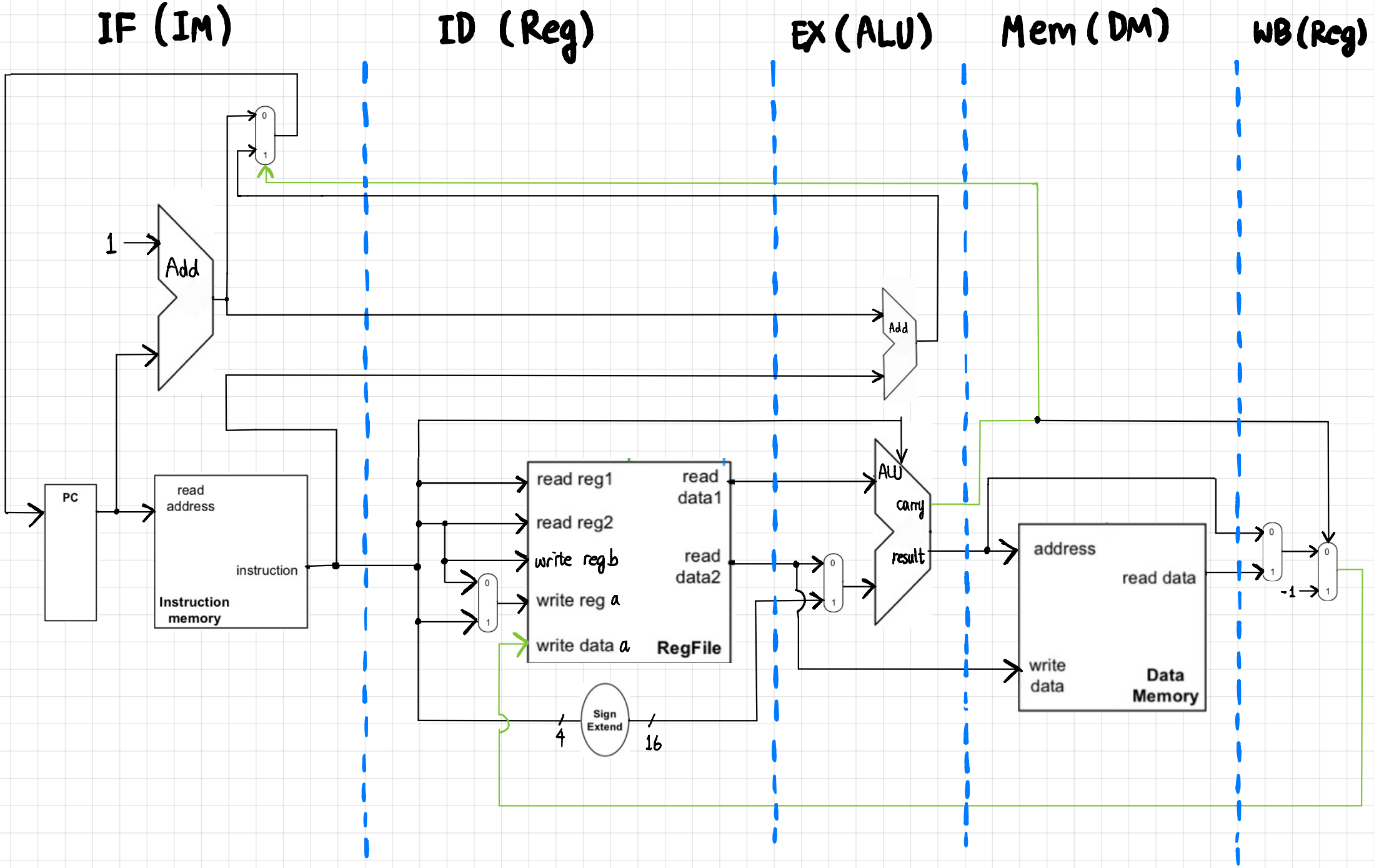
IF (IM)
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EX (ALU)
Mem (DM)
WB (Reg)
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instruction
Instruction memory
read reg1
read reg2
write reg b
write reg a
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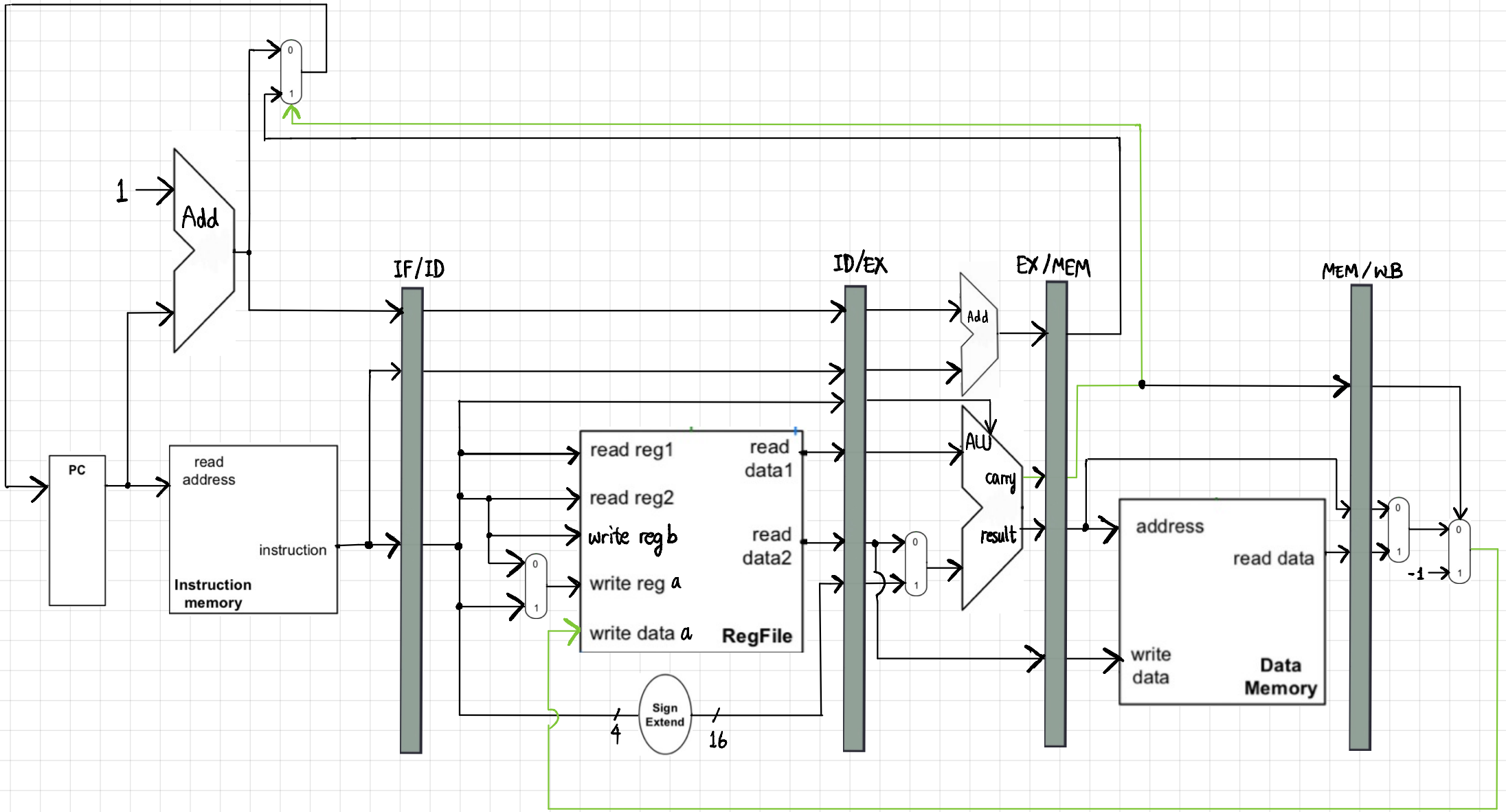
read data2
RegFile
Sign Extend
4
16
ALU
carry
result
address
read data
write data
Data Memory
-1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read reg1
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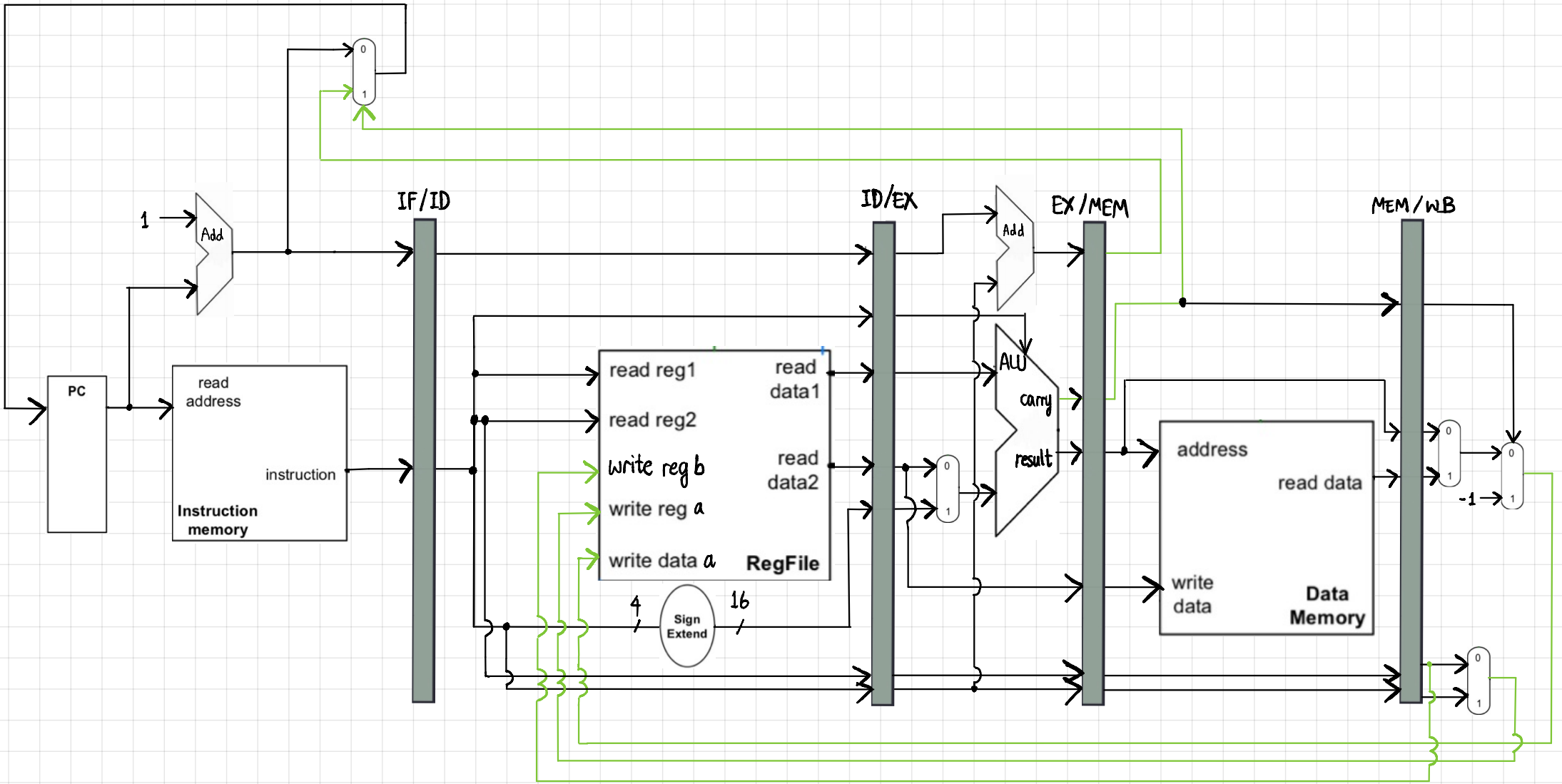
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write reg b
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write data a
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carry
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address
read data
write data
Data Memory
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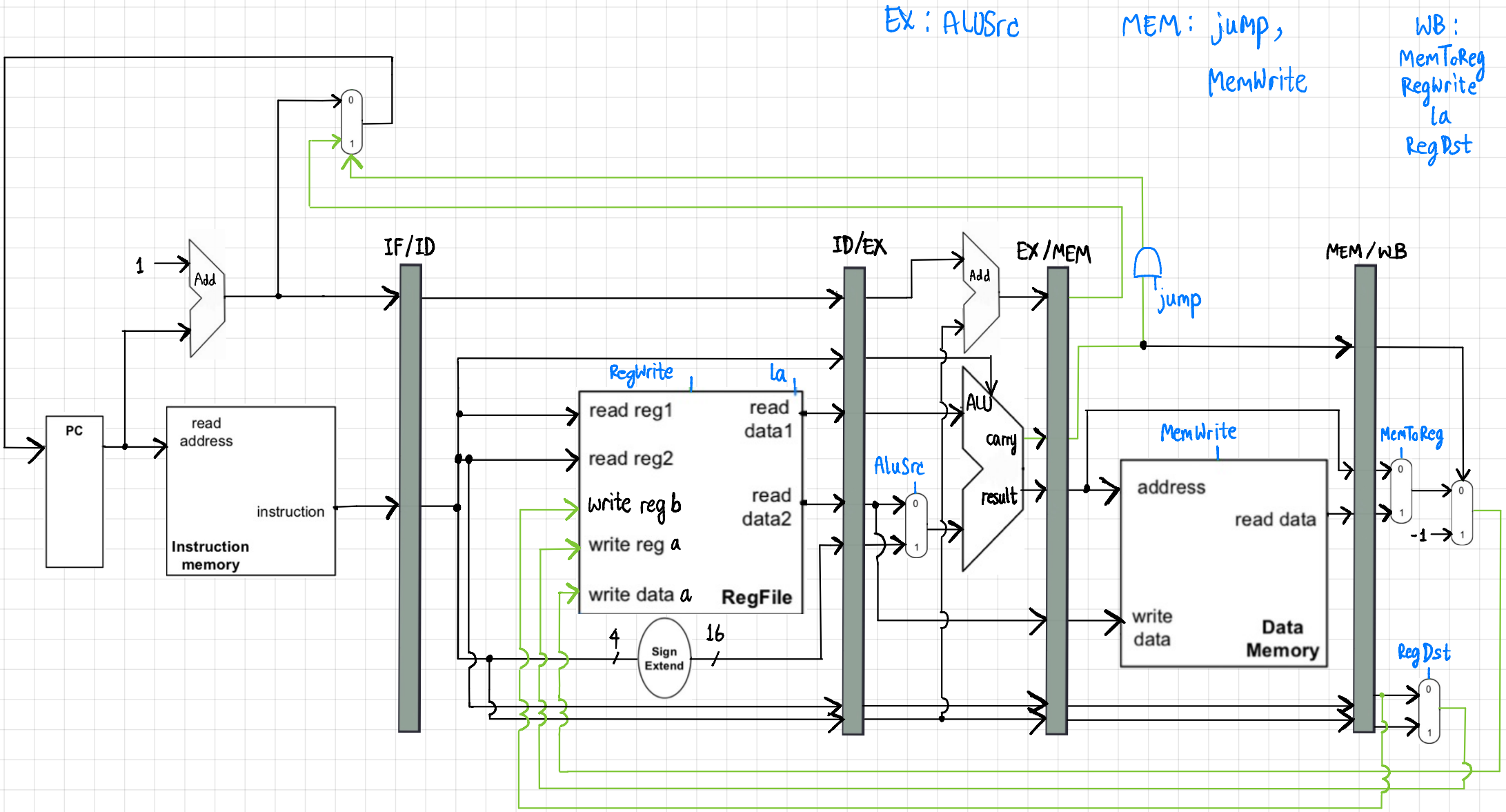
EX : ALUSrc
MEM : jump, MemWrite
WB : MemToReg RegWrite la RegDst
IF/ID
ID/EX
EX/MEM
MEM/WB
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instruction
Instruction memory
RegWrite
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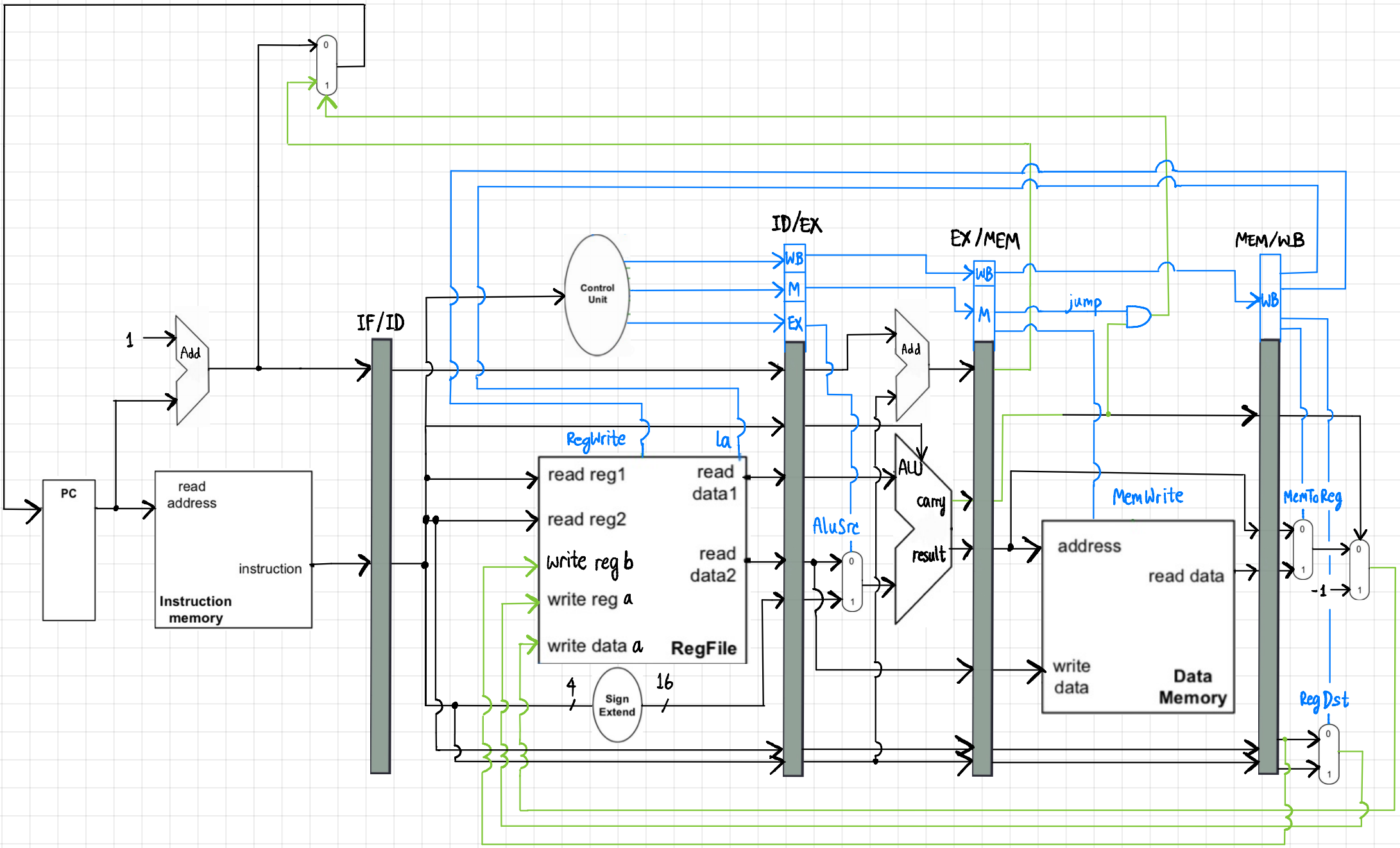
read reg1
read reg2
write reg b
write reg a
write data a
read data1
read data2
RegFile
4
Sign Extend
16
AluSrc
ALU
carry
result
Add
jump
MemWrite
address
read data
write data
Data Memory
MemToReg
-1
RegDst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Instruction
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Unit
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EX/MEM
WB
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MEM/WB
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read reg2
write reg b
write reg a
write data a
read
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data2
RegFile
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Memory
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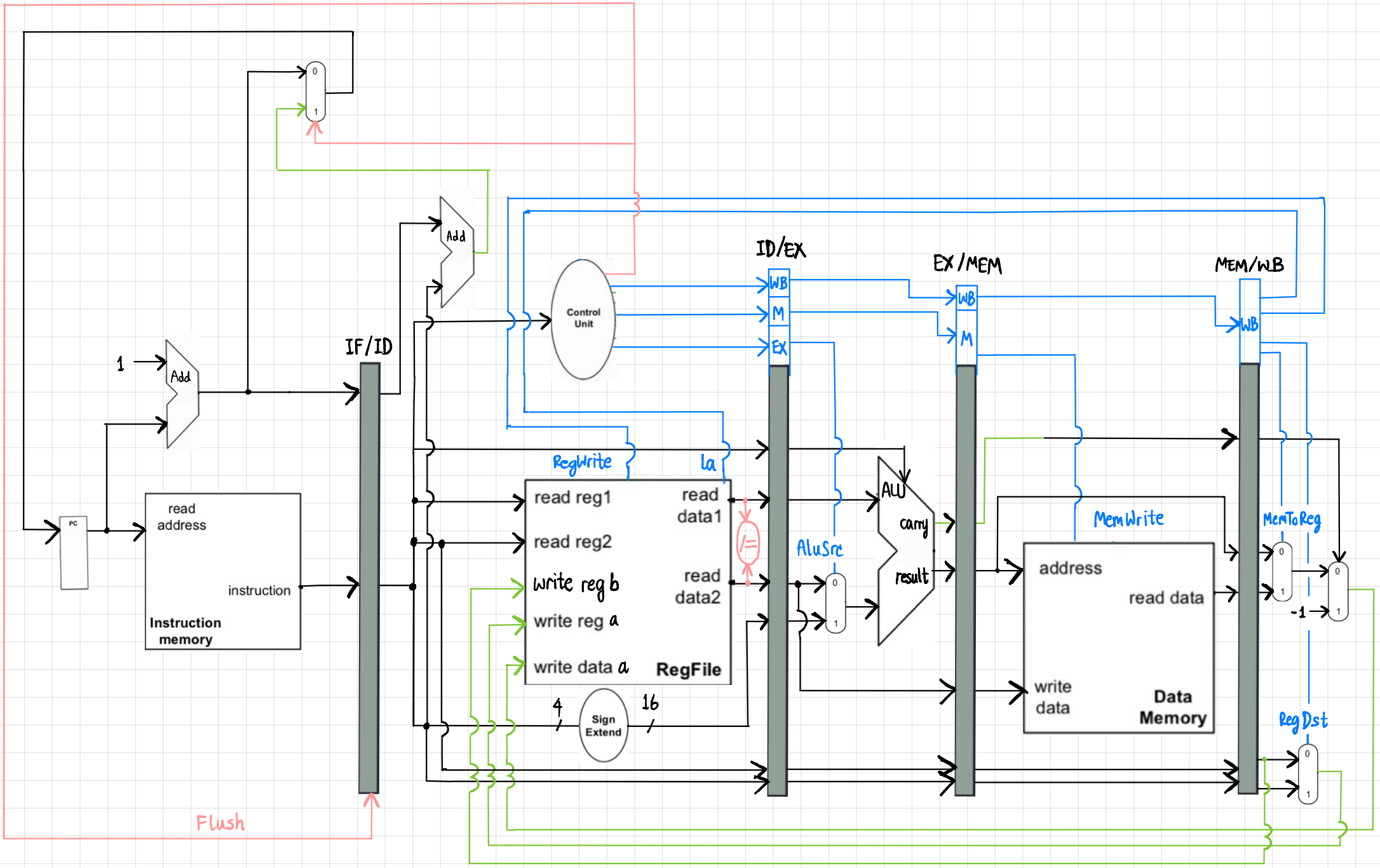
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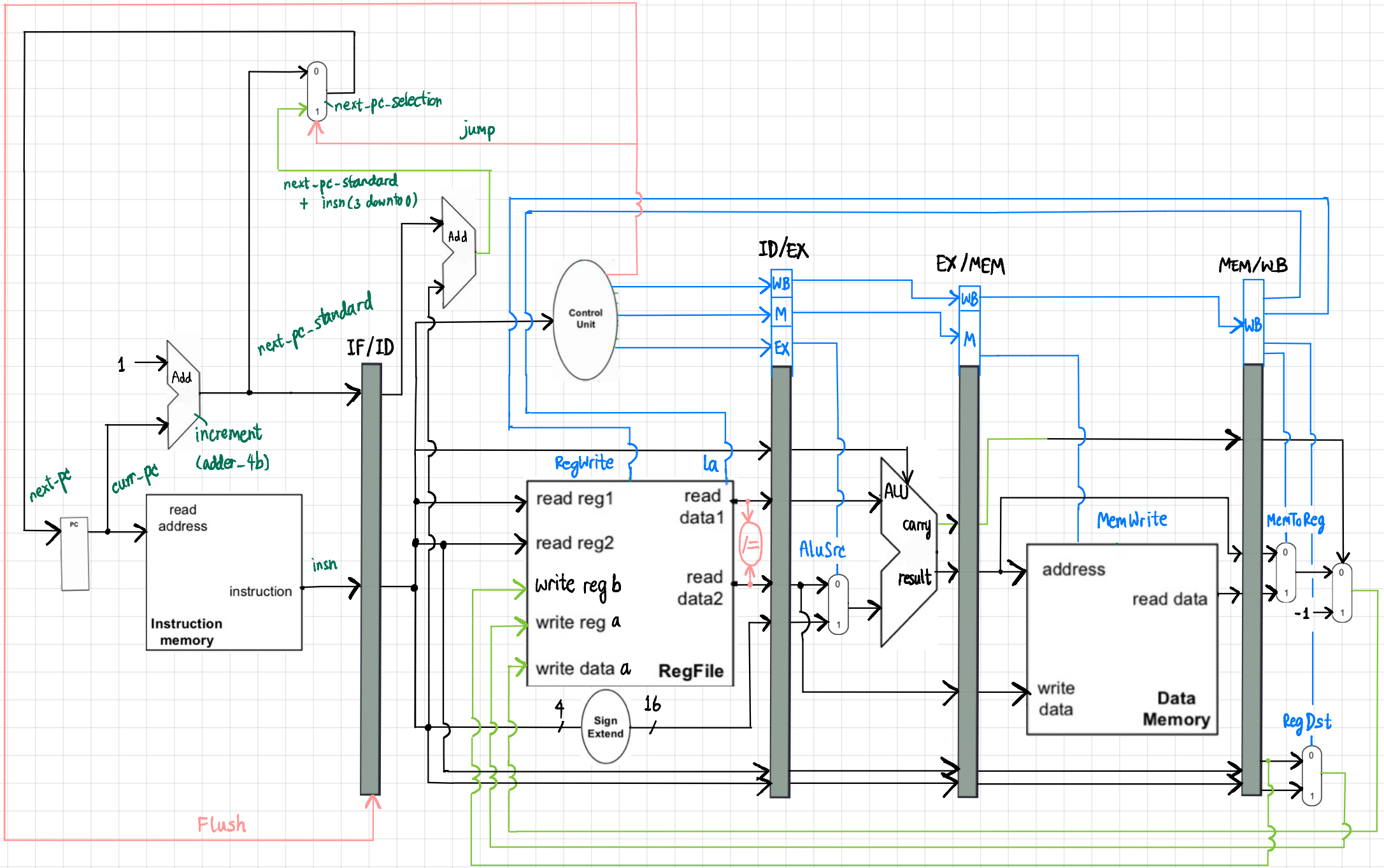
next-pc-selection
jump
next-pc-standard
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Add
next-pc-standard
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increment
(adder_4b)
next-pc
curr-pc
PC
read
address
instruction
Instruction
memory
insn
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Flush
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EX/MEM
MEM/WB
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RegFile
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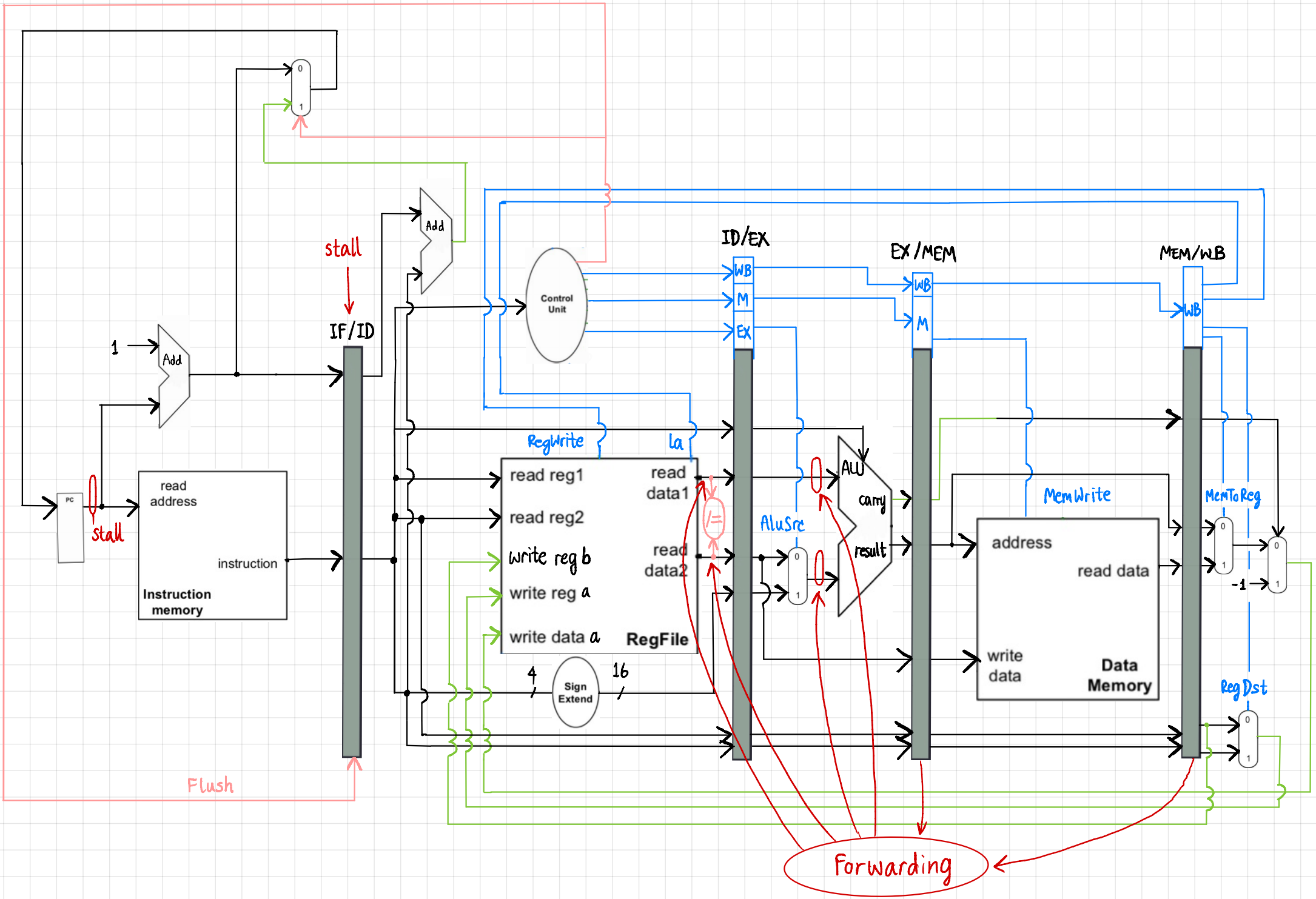
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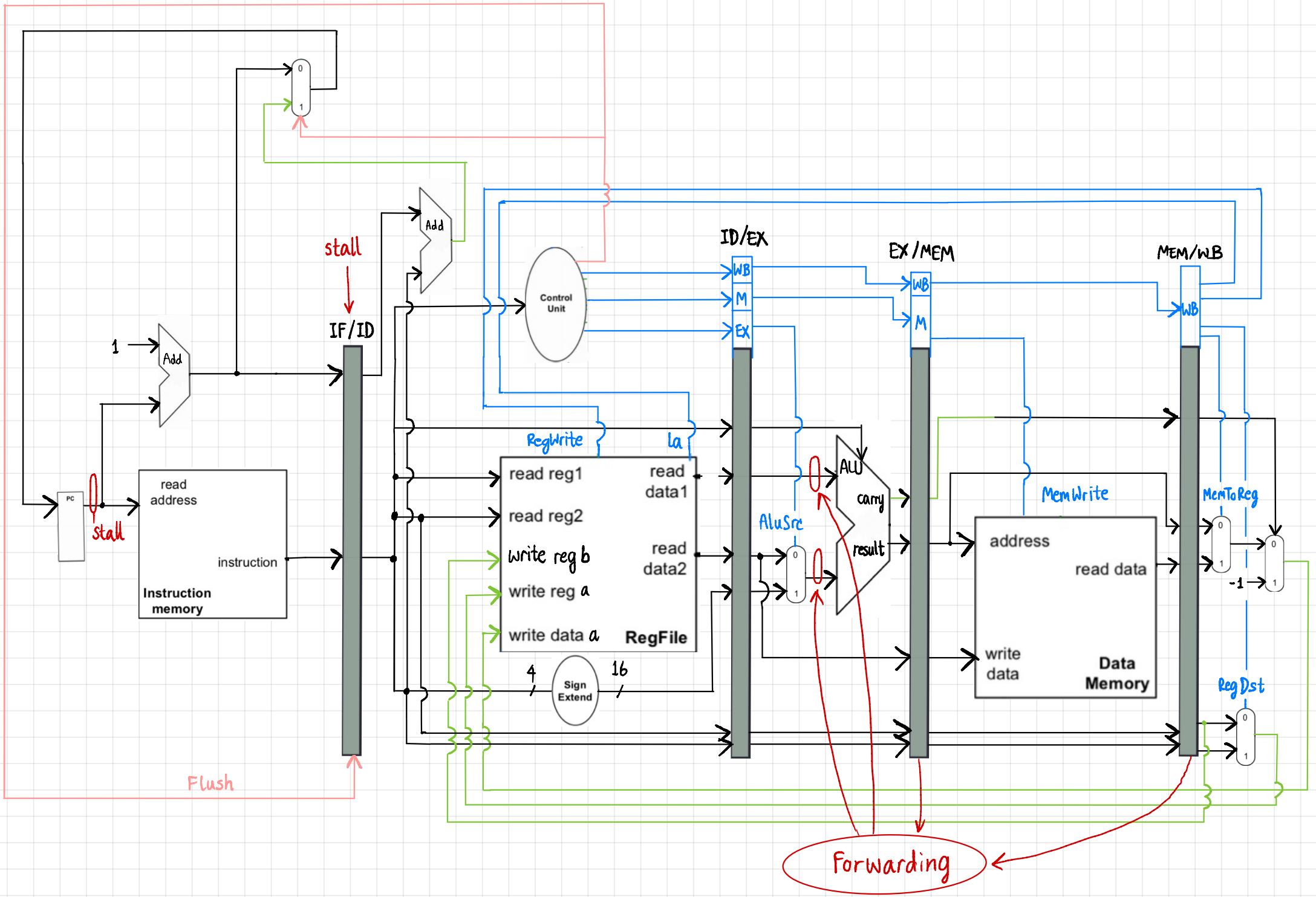
Forwarding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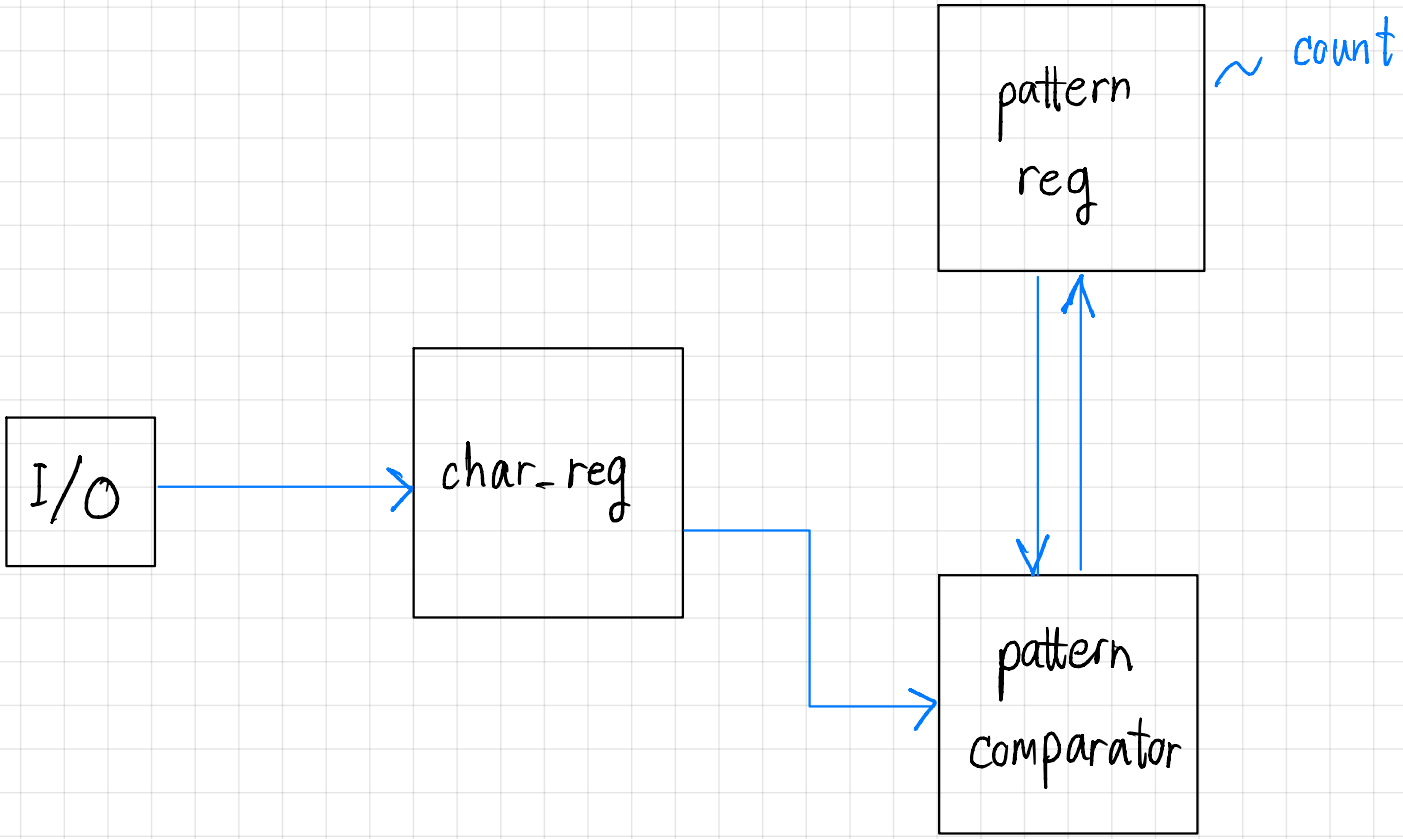
pattern
reg
count
I/O
char_reg
pattern
comparator