COMP3211/COMP9211 Computer Architecture

Lab 2 Single Cycle Processor

Goals

1. Study how to model a single cycle processor core using HDL.
2. Build simple single cycle processor.

The lab is based on an existing single cycle core model (in VHDL) created by a previous research student Ms. Lih Wen Koh (a similar Verilog model written by Dr. Sajid Hussain is also available on the course website). The block diagram of the core is given in single_cycle_core.pdf. All the related HDL files can be found in single_cycle_core.zip (available on the Labs page). The instructions to create a VHDL project and run simulation with Xilinx Vivado for the processor are given below. The same procedure can also be applied to the Verilog model.

1. Build the single cycle core project

- Download and unzip single_cycle_core.zip to a suitable location on your computer and unzip it to a folder.
- Start Xilinx Vivado and create a new project.
- Add single_cycle_core.vhdl and other vhdl files in the folder to the project, as shown in Figure 1.

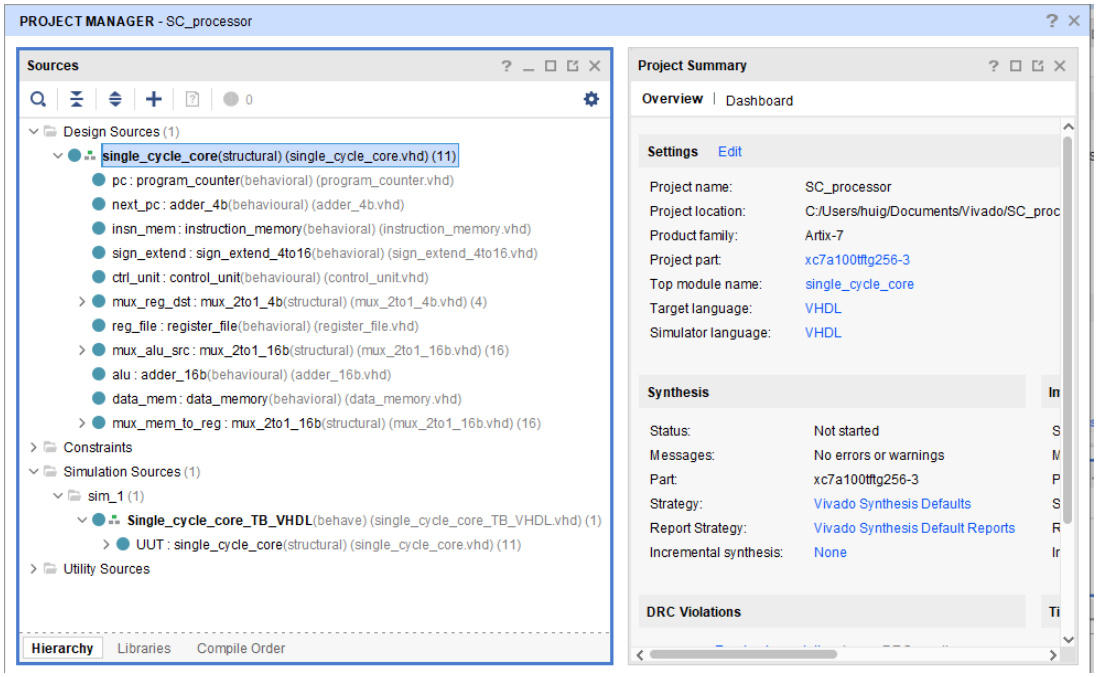


Figure 1

2. Simulation

- Click Simulate Behavioral Model.
- In the simulation window, add signals you are interested to the waveform window, as detailed below.
    - Expand the model hierarchy in the Scope box. There will be a list of corresponding signals displayed in the Objects box.
    - Drag signals you want to investigate from the box to the waveform viewer, as shown in Figure 2.
    - Rerun the simulation to generate the waveforms for all signals selected, as shown in Figure 3.
- Save the simulation to a .wcfg file. You can use this file as the configuration for future simulation.

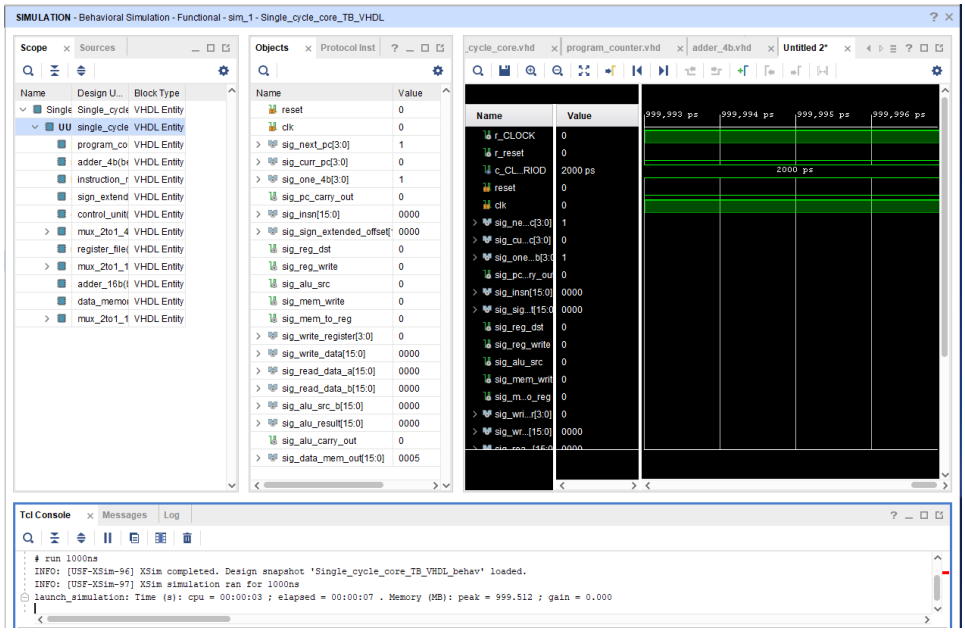


Figure 2

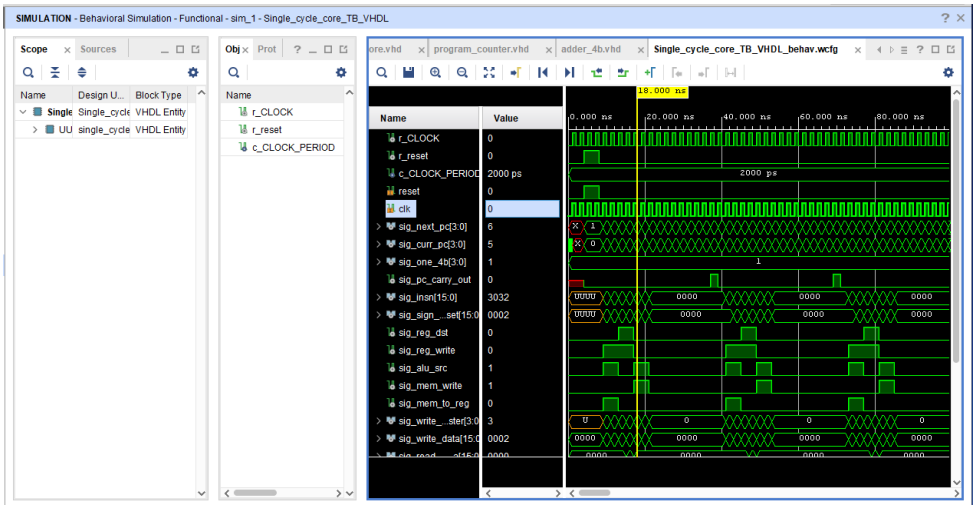


Figure 3

3. Task

- Study the HDL code in the single_cycle_core project.
- Modify the design to include the following three instructions:
    - Branch-on-Not-Equal instruction, BNE Rs, Rt, imme. When the values in registers Rs and Rt are not the same, PC = PC+4+imm, otherwise PC=PC+4.
    - Load-array-element instruction, *LA Rd, Rs+, Rt*, that loads a word from memory location (*Rs) that is bounded by Rt. When Rs<=Rt*, register Rd = MEM(Rs), Rs=Rs+1, otherwise, Rd = -1; PC = PC+4.
    - Rotate-Shift-Left instruction, *SLRi Rd, Rs, imme*, that rotate-left-shifts the contents in *Rs* imme bits.
- Verify your design.

Due Time: Your TLB class in Week 4

Lab presentation for **peer assessment.** The assessment scheme is the same as that for Lab 1 and is copied below.

Assessment Scheme:

Your work will be assessed by your peer students and tutor. For the assessment,

- Your TLB class is randomly divided into (up to) two assessement groups, each capped at 12 students. This is to allow sufficient time for the assessment. For a small TLB class, one assessment group may only be required.

  For f2f classes, the assessement will be conducted in an on-campus classroom and for online classes, the assessment will be conducted in a MS Teams meeting.
  The arrangment for each assessment group will be available in the Files folder of your class Teams channel.

- During assessment, each student is given 6 mins for presentation and 2 mins for Q&A.
    - The presentation covers three areas: design idea, HDL model, simulation results, and any discussion required for each task.
- Your work is assessed based on three categories (Presentation Completion and Quality). Among the three categories, Completion is rated in 0-7 and the other two each are rated in 0-5. Optionally you can add comments (see the guide marks provided):
    - Presentation (0-5)
        - Clarity (2)
        - Logic (2)
        - Timing management (1)

- Completion (0-7)
  - HDL model (2)
  - Valid simulation results (3)
  - Discussion (2)
- Quality (0-5)
  - You can give marks based on different aspects demonstrated in the lab work, for example, an interesting design idea, a clever modeling strategy, good design analysis, thorough evaluation, and adequate discussion.

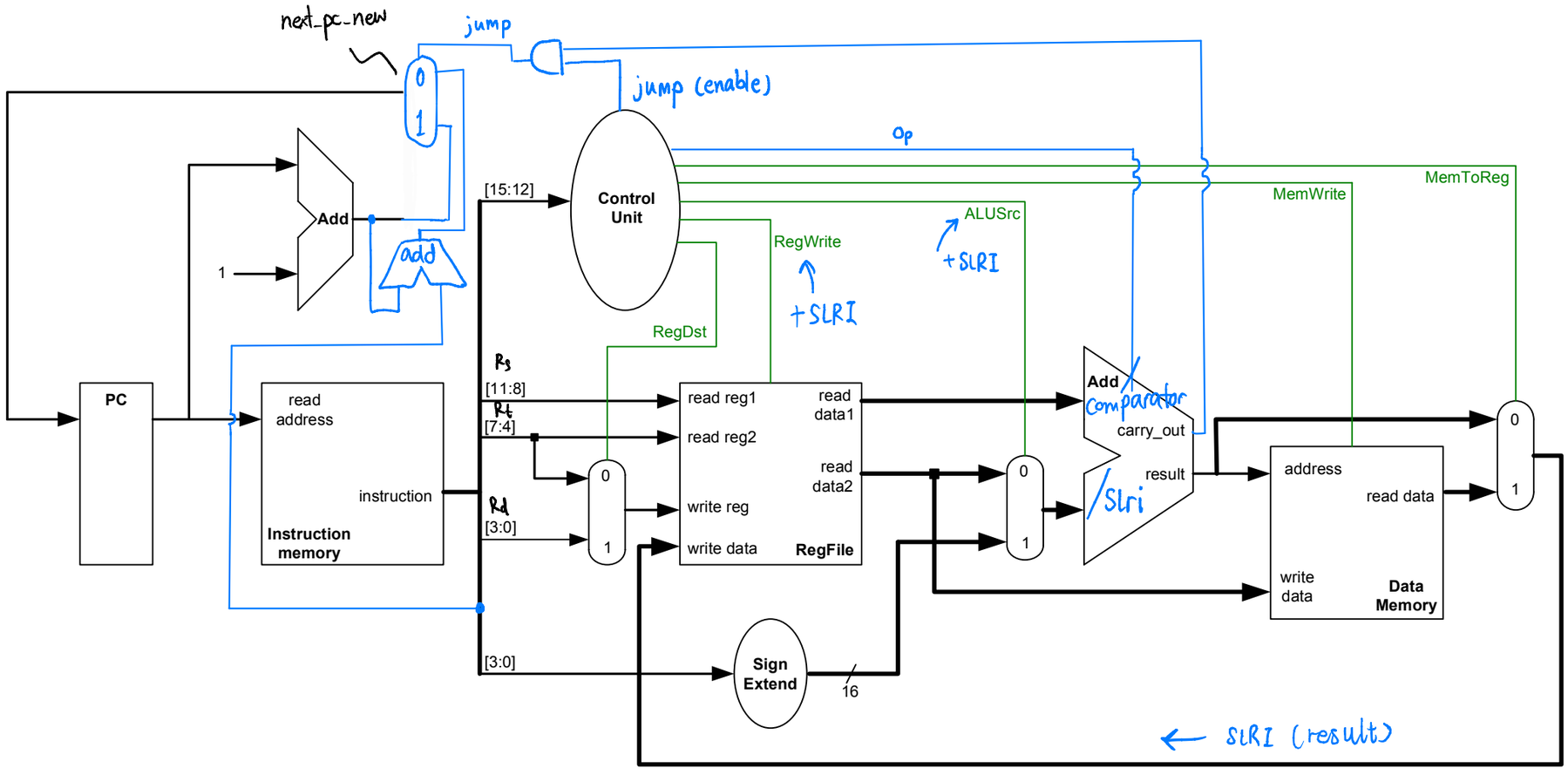
The link of an assessment form will be available in your MS teams channel.

- Your tutor will organize and steer the lab session.
  By the end of the lab class, all students are required to submit their assessment forms. Your participation to the assessment will be taken into account to the overall lab participation marks.

- Your marks are determined by
  - 80% from peers, and
  - 20% from tutor

BNE + SLRI

BLOCK DIAGRAM OF A SINGLE-CYCLE PROCESSOR CORE



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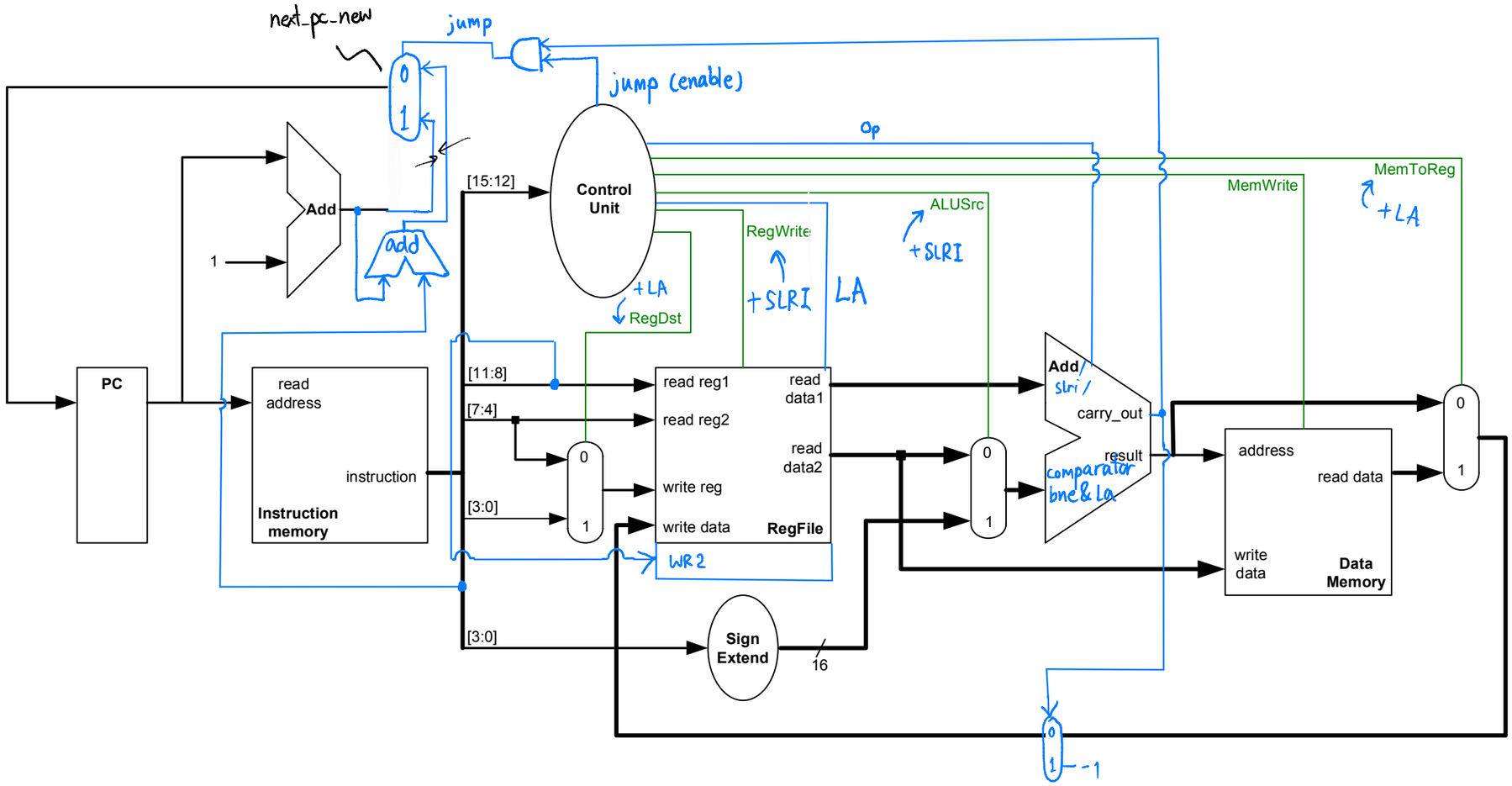
BLOCK DIAGRAM OF A SINGLE-CYCLE PROCESSOR CORE



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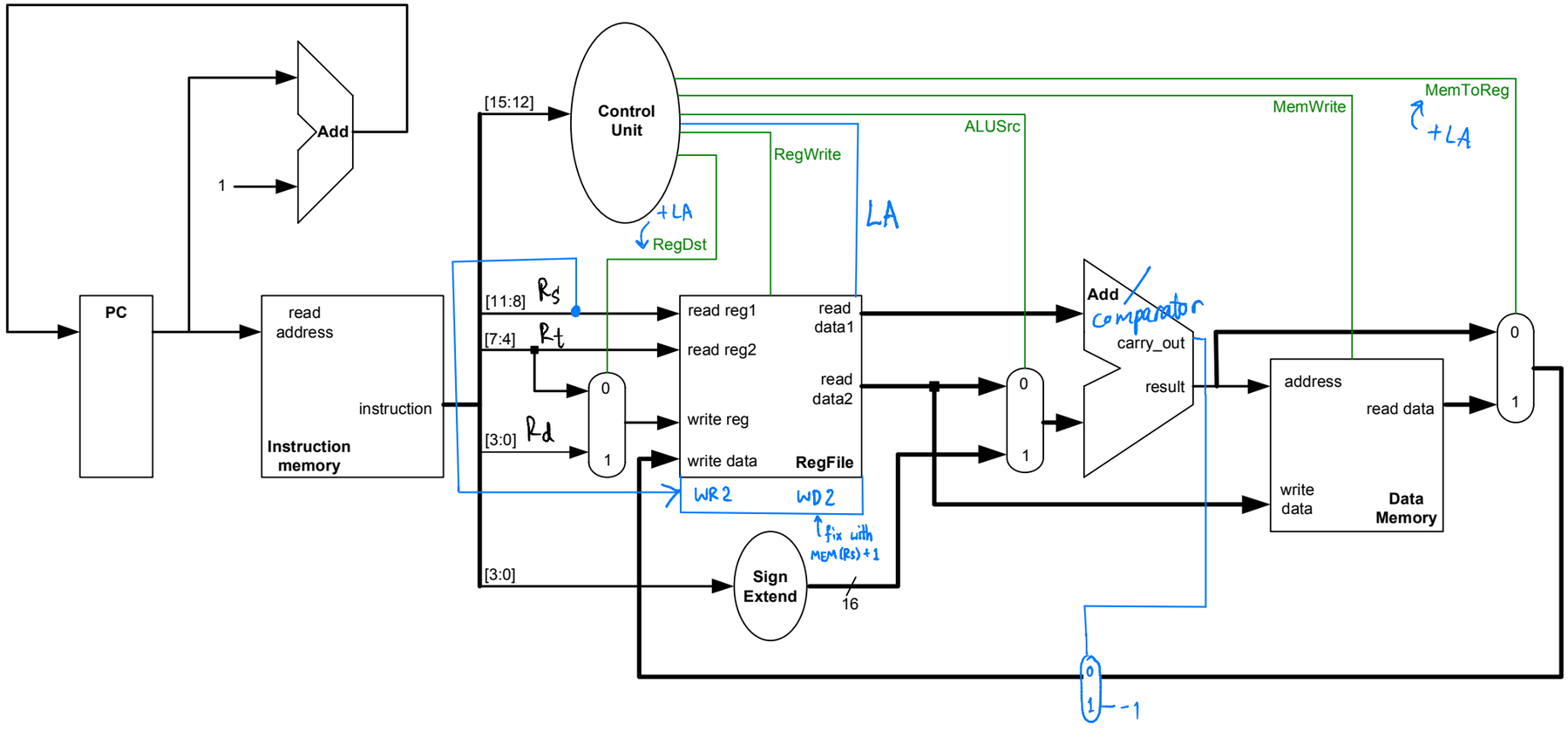
Rs < Rt else Rd = -1

LA Rd, Rs+, Rt

BLOCK DIAGRAM OF A SINGLE-CYCLE PROCESSOR CORE



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