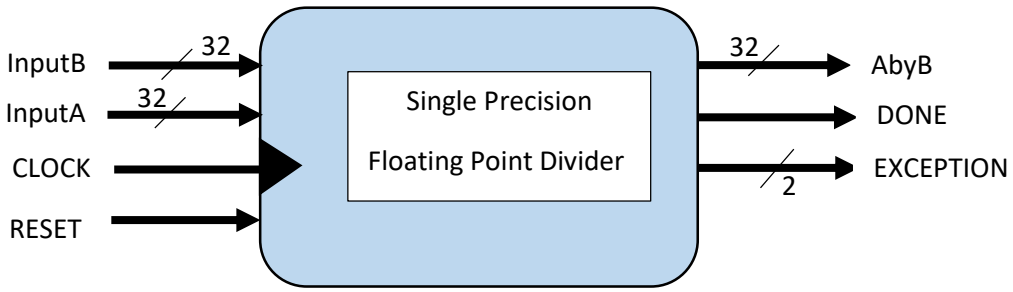
**Birla Institute of Technology and Science Pilani, Pilani Campus**
**CS F342 Computer Architecture**
**First Semester 2021-22**

## Assignment

**Marks: 15**
**Due Date:** 21st October, 2021
**Team Size:** up-to 4 members per team
**Submission:** Online

### Floating Point Divider

The aim of the Assignment is to implement a floating point divider. The floating point number used is the single precision 32-bit floating point number defined by IEEE-754. The Verilog HDL code should be functionally correct. Each module should be developed by the students from scratch. Don't use any piece of code from internet and/or borrow it from other teams. You can choose any algorithm/architecture to accomplish the task. Testing is an important aspect and one should pay sufficient time on building an efficient test bench through suitable test cases for the design module. Modelling style is left to the designer. ***Sub-normal numbers should be taken care***.




```
module fpdiv(AbyB,DONE,EXCEPTION,InputA,InputB,CLOCK,RESET);
input CLOCK,RESET ; // Active High Synchronous Reset
input [31:0] InputA,InputB ;
output [31:0]AbyB;
output DONE ; // '0' while calculating, '1' when the result is ready
output [1:0]Exception; // Used to output exceptions
endmodule
```

| Exception Code | Meaning |
|---|---|
| 00 | Divide by Zero |
| 01 | Under Flow |
| 10 | Over Flow |
| 11 | Invalid Operands |

**Broad Evaluation Guidelines:** Check points for your submission.

1. The HDL code shall be functionally correct.
2. Proper and sufficient test cases should be applied in the test bench.
3. Analysis of the results is important. Rather results itself.

**Do's and Don'ts**

- ☑ Literature review: design strategy and testing strategy.
- ☑ Discuss among the team, divide the tasks and solve as a team.
- ☑ Prepare an effective report.
- ☑ Equal contributions expected from every team member.
- ☒ Copying code entirely or partially from internet or other teams.
- ☒ Share your ideas with other teams before the assignment submission.
- ☒ Reporting false results and inappropriate data in the report.
- ☒ Burdening only a few people in the team.

**Useful Online Links:**

Online Converter: https://www.binaryconvert.com/convert_float.html
Division Algorithms: https://web.stanford.edu/class/ee486/doc/chap5.pdf
IEEE 754: https://www.ias.ac.in/public/Volumes/reso/021/01/0011-0030.pdf

**Submission:** The evaluation is done through a script. Therefore, please don't change the name of the module, inputs (not even case). Internal signals, parameters and other sub-module names are left to the designer. Use comment lines appropriately to explain the purpose of each module.

**The submission link will be notified to you in due time. You can form your own groups. There is no need to notify us about the same**

For further clarification you may contact the undersigned through e-mail.

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