

# Flea3

## **GigE Digital Camera**

**Technical Reference** 

Version 6.0

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Point Grey Research® Inc.

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#### **FCC Compliance**

This device complies with Part 15 of the FCC rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesirable operation.

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## **Table of Contents**

1 W	elcome to Flea3 GigE	1
1	1 Flea3 GigE Specifications	1
	1.1.1 FL3-GE-03S1M (Mono) Imaging Performance	. 4
	1.1.2 FL3-GE-03S1C (Color) Imaging Performance	5
	1.1.3 FL3-GE-03S2M (Mono) Imaging Performance	. 6
	1.1.4 FL3-GE-03S2C (Color) Imaging Performance	7
	1.1.5 FL3-GE-08S2M (Mono) Imaging Performance	. 8
	1.1.6 FL3-GE-08S2C (Color) Imaging Performance	9
	1.1.7 FL3-GE-13S2M (Mono) Imaging Performance	. 10
	1.1.8 FL3-GE-13S2C (Color) Imaging Performance	11
	1.1.9 FL3-GE-14S3M (Mono) Imaging Performance	. 12
	1.1.10 FL3-GE-14S3C (Color) Imaging Performance	. 13
	1.1.11 FL3-GE-20S4M (Mono) Imaging Performance	14
	1.1.12 FL3-GE-20S4C (Color) Imaging Performance	. 15
	1.1.13 FL3-GE-28S4M (Mono) Imaging Performance	16
	1.1.14 FL3-GE-28S4C (Color) Imaging Performance	. 17
	1.1.15 FL3-GE-50S5M (Mono) Imaging Performance	18
	1.1.16 FL3-GE-50S5C (Color) Imaging Performance	. 19
	1.1.17 Flea3 GigE (Mono) Comparison	20
1	.2 Analog-to-Digital Conversion	21
1	3 Flea3 GigE Mechanical Properties	. 22
	1.3.1 Physical Description	. 22
	1.3.2 Camera Dimensions	. 23
	1.3.3 Tripod Adapter Dimensions	. 24
	1.3.4 Lens Mounting	24
	1.3.4.1 Back Flange Distance	25
	1.3.5 Dust Protection	25
	1.3.6 Mounting with the Case or Mounting Bracket	. 25
	1.3.7 Infrared Cut-Off Filters	. 26
1	4 Handling Precautions and Camera Care	26
	1.4.1 Case Temperature and Heat Dissipation	. 27
1	5 Camera Interface and Connectors	. 28
	1.5.1 Ethernet Connector	. 28
	1.5.2 Interface Cables	. 28
	1.5.3 Interface Card	. 28



1.5.4 General Purpose Input/Output (GPIO)	28
2 Getting Started with Flea3 GigE	30
2.1 Before You Install	30
2.1.1 Will your system configuration support the camera?	
2.1.2 Do you have all the parts you need?	30
2.1.3 Do you have a downloads account?	30
2.2 Installing Your Interface Card and Software	31
2.3 Installing Your Camera	32
2.4 Controlling the Camera	
2.4.1 Using FlyCapture	
2.4.2 GenlCam Applications	34
2.4.3 GigE Vision Bootstrap Registers	34
2.5 Configuring Camera Setup	34
2.5.1 Configuring Camera Drivers	34
2.5.2 Configuring the IP Address	35
2.5.3 Allocating Bandwidth	36
2.5.3.1 Packet Size	36
2.5.3.2 Packet Delay	37
2.5.3.3 Determining Bandwidth Requirements	37
2.5.4 Configuring Other Network Settings	38
2.5.4.1 Stream Channel Destination Address	38
2.5.4.2 Heartbeat	39
3 General Camera Operation	40
3.1 Powering the Camera	40
3.2 GenlCam Device Control	40
3.3 User Sets	41
3.3.1 GenlCam User Set Control	41
3.4 On-Camera Frame Buffer	42
3.5 Non-Volatile Flash Memory	43
3.6 Camera Firmware	43
3.6.1 Determining Firmware Version	43
3.6.2 Upgrading Camera Firmware	43
4 Input/Output Control	44
4.1 General Purpose Input/Output (GPIO)	44
4.2 GPIO Modes	44
4.2.1 GPIO Mode 0: Input	44
4.2.2 GPIO Mode 1: Output	44
4.2.3 GPIO Mode 2: Asynchronous (External) Trigger	45



4.2.4 GPIO Mode 3: Strobe	45
4.2.5 GPIO Mode 4: Pulse Width Modulation (PWM)	45
4.3 GenlCam Digital Input/Output Control	45
4.4 Programmable Strobe Output	46
4.4.1 Example: Setting a GPIO Pin to Strobe (Using the FlyCapture API)	46
4.5 Pulse Width Modulation (PWM)	47
4.6 Serial Communication	47
4.7 Debouncer	48
4.8 GPIO Electrical Characteristics	48
4.8.1 GPIO0 (Opto-Isolated Input) Circuit	49
4.8.2 GPIO1 (Opto-Isolated Output) Circuit	49
4.8.3 GPIO 2/3 (Bi-Directional) Circuit	51
5 Video Formats, Modes and Frame Rates	53
5.1 Video Modes Overview	53
5.1.1 Video Mode Descriptions	54
5.1.2 Calculating Maximum Possible Frame Rate	55
5.2 Pixel Formats	55
5.2.1 Raw	56
5.2.2 Mono	56
5.2.3 RGB	56
5.2.4 YUV	56
5.2.5 Y16 (16-bit Mono) Image Acquisition	57
5.2.6 Y8 or Y16 Raw Bayer Output	57
5.3 Supported Formats, Modes and Frame Rates	57
5.3.1 FL3-GE-03S1 Video Modes and Frame Rates	57
5.3.2 FL3-GE-03S2 Video Modes and Frame Rates	58
5.3.3 FL3-GE-08S2 Video Modes and Frame Rates	59
5.3.4 FL3-GE-13S2 Video Modes and Frame Rates	60
5.3.5 FL3-GE-14S3 Video Modes and Frame Rates	61
5.3.6 FL3-GE-20S4 Video Modes and Frame Rates	62
5.3.7 FL3-GE-28S4 Video Modes and Frame Rates	63
5.3.8 FL3-GE-50S5 Video Modes and Frame Rates	65
5.4 GenlCam Image Format Control	66
6 Image Acquisition	68
6.1 Asynchronous Triggering	68
6.1.1 External Trigger Timing	68
6.1.2 Camera Behavior Between Triggers	69
6.1.3 Changing Video Modes While Triggering	69



6.1.4 Example: Asynchronous Hardware Triggering (Using the FlyCapture API)	
6.1.5 Asynchronous Software Triggering	70
6.2 Trigger Modes	71
6.2.1 Trigger Mode 0 ("Standard External Trigger Mode")	71
6.2.2 Trigger Mode 1 ("Bulb Shutter Mode")	71
6.2.3 Trigger Mode 3 ("Skip Frames Mode")	72
6.2.4 Trigger Mode 4 ("Multiple Exposure Preset Mode")	73
6.2.5 Trigger Mode 5 ("Multiple Exposure Pulse Width Mode")	74
6.2.6 Trigger Mode 13 ("Low Smear Trigger Mode")	75
6.2.7 Trigger Mode 14 ("Overlapped Exposure/Readout Mode")	76
6.2.8 Trigger Mode 15 ("Multi-Shot Trigger Mode")	77
6.3 GenlCam Acquisition Control	78
7 Imaging Parameters and Control	80
7.1 Overview of Imaging Parameters	80
7.2 GenlCam Analog Control	81
7.3 Brightness	82
7.3.1 Example: Setting Brightness Using the FlyCapture API	82
7.4 Gain	82
7.4.1 Example: Setting Gain Using the FlyCapture API	82
7.5 Saturation	83
7.5.1 Example: Setting Saturation Using the FlyCapture API	83
7.6 Hue	84
7.6.1 Example: Setting Hue Using the FlyCapture API	84
7.7 Sharpness	84
7.7.1 Example: Setting Sharpness Using the FlyCapture API	84
7.8 Gamma and Lookup Table	85
7.8.1 Example: Setting Gamma Using the FlyCapture API	86
7.9 White Balance	87
7.9.1 Example: Setting White Balance Using the FlyCapture API	88
7.10 Shutter	88
7.10.1 Extended Shutter Times	89
7.10.2 Example: Setting Shutter Using the FlyCapture API	89
7.11 Bayer Color Processing	90
7.11.1 Accessing Raw Bayer Data	91
7.11.2 Example: Accessing Raw Bayer Data using FlyCapture2	91
7.12 Image Flip/Mirror	91
7.13 Auto Exposure	91
7.13.1 Example: Setting Auto Exposure Using the FlyCapture API	92



7.14 High Dynamic Range (HDR) Imaging	93
7.15 Embedded Image Information	93
8 Troubleshooting	95
8.1 Support	95
8.2 Camera Diagnostics	95
8.3 Status Indicator LED	95
8.4 Test Pattern	96
8.4.1 Image Format Control—Test Image	96
8.5 Blemish Pixel Artifacts	96
8.5.1 Pixel Defect Correction	97
8.6 Vertical Smear Artifact	97
8.6.1 Smear Reduction	97
Appendix A: GenlCam Features	99
A.1 Device Control	99
A.2 Analog Control	99
A.3 Image Format Control	100
A.4 Acquisition Control	102
A.5 Digital Input Output Control	103
A.6 Transport Layer Control	103
A.7 User Set Control	107
Appendix B: GigE Vision Bootstrap Registers	
Appendix C: Control and Status Registers	110
C.1 Using Control and Status Registers	110
C.1.1 Modes	110
C.1.2 Values	110
C.1.3 Register Memory Map	111
C.1.4 Config ROM	112
C.1.4.1 Root Directory	112
C.1.4.2 Unit Directory	112
C.1.4.3 Unit Dependent Info	113
C.1.5 Calculating Base Register Addresses using 32-bit Offsets	114
C.1.6 Absolute Value Registers	114
C.1.6.1 Setting Absolute Value Register Values	115
C.1.6.2 Absolute Value Offset Addresses	115
C.1.6.3 Units of Value for Absolute Value CSR Registers	116
C.1.6.4 Determining Absolute Value Register Values	116
C.2 Inquiry Registers	117
C.2.1 Basic Functions Inquiry Registers	117



C.2.2 Feature Presence Inquiry Registers	118
C.2.3 Feature Elements Inquiry Registers	120
C.2.4 Video Format Inquiry Registers	122
C.2.5 Video Mode Inquiry Registers	122
C.2.6 Video Frame Rate Inquiry Registers	124
C.3 General Camera Operation	128
C.3.1 Memory Channel Registers	128
C.3.1.1 MEMORY_SAVE: 618h	129
C.3.1.2 MEM_SAVE_CH: 620h	129
C.3.1.3 CUR_MEM_CH: 624h	130
C.3.2 Device Information CSRs	130
C.3.2.1 SERIAL_NUMBER: 1F20h	130
C.3.2.2 MAIN_BOARD_INFO: 1F24h	131
C.3.2.3 VOLTAGE: 1A50h – 1A54h	131
C.3.2.4 CURRENT: 1A58h – 1A5Ch	131
C.3.2.5 TEMPERATURE: 82Ch	132
C.3.2.6 CAMERA_POWER: 610h	132
C.3.2.7 PIXEL_CLOCK_FREQ: 1AF0h	132
C.3.2.8 HORIZONTAL_LINE_FREQ: 1AF4h	132
C.3.3 Camera Memory	132
C.3.3.1 DATA_FLASH_CTRL: 1240h	132
C.3.3.2 DATA_FLASH_DATA: 1244h	133
C.3.3.3 IMAGE_RETRANSMIT: 634h	133
C.3.4 Firmware Information	134
C.3.4.1 FIRMWARE_VERSION: 1F60h	134
C.3.4.2 FIRMWARE_BUILD_DATE: 1F64h	134
C.3.4.3 FIRMWARE_DESCRIPTION: 1F68-1F7Ch	134
C.4 Input/Output Control	134
C.4.1 GPIO_CTRL_PIN: 1110h-1140h	135
C.4.2 GPIO_XTRA_PIN: 1114h-1144h	136
C.4.3 GPIO_STRPAT_CTRL: 110Ch	136
C.4.4 GPIO_STRPAT_MASK_PIN: 1118h-1148h	137
C.4.5 GPIO_XTRA: 1104h	137
C.4.6 Strobe Output Registers	138
C.4.7 Serial Input/Output Registers	139
C.4.8 DEBOUNCER_CTRL	143
C.4.8.1 DEBOUNCER_INQ: 0x11fch	143
C.4.8.2 DEBOUNCER_X_CTRL: 0x111c - 0x118c	144



C.5.1 FRAME_RATE: 83Ch	C.5 Video Format, Mode, and Frame Rate Settings	144
C.5.3 CURRENT_VIDEO_MODE: 604h  C.5.4 CURRENT_VIDEO_FORMAT: 608h  .146  C.5.5 FORMAT_7_RESZE_INQ: 1AC8h  C.5.6 Inquiry Registers for Custom Video Mode Offset Addresses  .147  C.5.6.1 Image Size and Position  .148  C.5.6.2 COLOR_CODING_ID and COLOR_CODING_INQ  .148  C.5.6.3 FRAME_INTERVAL_INQ  .149  C.5.7 Pixel Formats  .149  C.5.7.1 DATA_DEPTH: 630h  .150  C.6.4 Synchronous Trigger Settings  .150  C.6.1 TRIGGER_MODE: 830h  .150  C.6.2 TRIGGER_DELAY: 8344h  .151  C.6.3 SOFTWARE_TRIGGER: 62Ch  C.7.2 LUT: 80000h – 80048h (IIDC 1.32)  C.7.3 WHITE_BALANCE: 80Ch  C.7.3 WHITE_BALANCE: 80Ch  C.7.4 MAYER_TILE_MAPPING: 1040h  C.7.5 MIRROR_IMAGE_CTRL: 1054h  C.7.5 MIRROR_IMAGE_CTRL: 1054h  C.7.7 AUTO_EXPOSURE: 804h  C.7.7 AUTO_EXPOSURE: 804h  C.7.7.1 AUTO_EXPOSURE: 804h  C.7.7.2 AUTO_EXPOSURE: RANGE: 1098h  C.7.7.3 HORD_EXPOSURE: RANGE: 1098h  C.7.7.3 HORD_EXPOSURE: RANGE: 1098h  C.7.7.4 HORD_EXPOSURE: RANGE: 1098h  C.7.7.5 HORD_EXPOSURE: RANGE: 1098h  C.7.7.6 SHOTTER: 11054h  C.8.1 Camera Diagnostics  163  C.8.1 Camera Diagnostics  164  C.8.1.1 INITIALIZE: 000h  C.8.1.2 TIME_FROM_INITIALIZE: 12E0h  C.8.1.3 LINK_UP_TIME: 12E4h  C.8.1.4 XMIT_FAILURE: 12FCh  C.8.1.5 VMODE_ERROR_STATUS: 628h	C.5.1 FRAME_RATE: 83Ch	145
C.5.4 CURRENT_VIDEO_FORMAT: 608h  C.5.5 FORMAT_7_RESIZE_INQ: 1AC8h  C.5.6 Inquiry Registers for Custom Video Mode Offset Addresses  147  C.5.6.1 Image Size and Position  148  C.5.6.2 COLOR_CODING_ID and COLOR_CODING_INQ  149  C.5.6.3 FRAME_INTERVAL_INQ  149  C.5.7 Pixel Formats  149  C.5.7.1 DATA_DEPTH: 630h  149  C.5.7.2 BAYER_MONO_CTRL: 1050h  150  C.6.4 Saynchronous Trigger Settings  150  C.6.1 TRIGGER_MODE: 830h  150  C.6.2 TRIGGER_DELAY: 834h  151  C.6.3 SOFTWARE_TRIGGER: 62Ch  152  C.7.1 Imaging Parameters  152  C.7.1 Imaging Parameters  152  C.7.1 Imaging Parameters: 800h-888h  152  C.7.2 LUT: 80000h = 80048h (IIDC 1.32)  154  C.7.3 WHITE_BALANCE: 80Ch  157  C.7.4 BAYER_TILE_MAPPING: 1040h  157  C.7.5 SHUTTER: 81Ch  158  C.7.7 AUTO_EXPOSURE: 804h  C.7.7 AUTO_EXPOSURE: 804h  C.7.7.3 AUTO_EXPOSURE: 804h  C.7.7.3 AUTO_EXPOSURE: RANGE: 1098h  160  C.7.7.3 AUTO_EXPOSURE: RANGE: 1098h  161  C.7.9 FRAME_INFO: 12F8h  162  C.8 Troubleshooting  163  C.8.1.1 INITIALIZE: 000h  164  C.8.1.2 TIME_FROM_INITIALIZE: 12E0h  164  C.8.1.1 SINN_UP_TIME: 12E4h  C.8.1.1 SUMODE_ERROR_STATUS: 628h  165	C.5.2 CURRENT_FRAME_RATE: 600h	146
C.5.5 FORMAT_7_RESIZE_INQ: 1AC8h       146         C.5.6 Inquiry Registers for Custom Video Mode Offset Addresses       147         C.5.6.1 Image Size and Position       148         C.5.6.2 COLOR_CODING_ID and COLOR_CODING_INQ       148         C.5.7.2 PARAME_INTERVAL_INQ       149         C.5.7.1 DATA_DEPTH: 630h       149         C.5.7.1 DATA_DEPTH: 630h       150         C.5.7.2 BAYER_MONO_CTRL: 1050h       150         C.6.4 Synchronous Trigger Settings       150         C.6.1 TRIGGER_MODE: 830h       150         C.6.2 TRIGGER_DELAY: 834h       151         C.6.3 SOFTWARE_TRIGGER: 62Ch       152         C.7.1 Imaging Parameters       152         C.7.2 LUT: 80000h — 80048h (IIDC 1.32)       154         C.7.3 WHITE_BALANCE: 80Ch       157         C.7.4 BAYER_TILE_MAPPING: 1040h       157         C.7.5 SHUTTER: 81Ch       158         C.7.6 SHUTTER: 81Ch       158         C.7.7 AUTO_EXPOSURE: 804h       159         C.7.7.1 AUTO_EXPOSURE: 804h       159         C.7.7.2 AUTO_SHUTTER_RANGE: 1088h       160         C.7.7.2 AUTO_SHUTTER_RANGE: 1088h       160         C.7.9 FRAME_INFO: 12F8h       162         C.8 Tombleshooting       163         C.8.1 Camera Diagno	C.5.3 CURRENT_VIDEO_MODE: 604h	146
C.5.6 Inquiry Registers for Custom Video Mode Offset Addresses	C.5.4 CURRENT_VIDEO_FORMAT: 608h	146
C.5.6.1 Image Size and Position	C.5.5 FORMAT_7_RESIZE_INQ: 1AC8h	146
C.5.6.2 COLOR_CODING_ID and COLOR_CODING_INQ       148         C.5.6.3 FRAME_INTERVAL_INQ       149         C.5.7 Pixel Formats       149         C.5.7.1 DATA_DEPTH: 630h       149         C.5.7.2 BAYER_MONO_CTRL: 1050h       150         C.6 Asynchronous Trigger Settings       150         C.6.1 TRIGGER_MODE: 830h       150         C.6.2 TRIGGER_DELAY: 834h       151         C.6.3 SOFTWARE_TRIGGER: 62Ch       152         C.7 Controlling Imaging Parameters       152         C.7.1 Imaging Parameters: 800h-888h       152         C.7.2 LUT: 80000h - 80048h (IIDC 1.32)       154         C.7.3 WHITE_BALANCE: 80Ch       157         C.7.4 BAYER_TILE_MAPPING: 1040h       157         C.7.5 MIRROR_IMAGE_CTRL: 1054h       158         C.7.6 SHUTTER: 81Ch       158         C.7.7 AUTO_EXPOSURE: 804h       158         C.7.7.1 AUTO_EXPOSURE: 804h       159         C.7.7.2 AUTO_SHUTTER RANGE: 1098h       160         C.7.7.3 AUTO_GAIN_RANGE: 100h       161         C.7.8 HDR: 1800h - 1884h       161         C.7.9 FRAME_INFO: 12F8h       162         C.8.1 Camera Diagnostics       163         C.8.1.1 INITIALIZE: 000h       164         C.8.1.2 TIME_FROM_INITIALIZE: 12E0h	C.5.6 Inquiry Registers for Custom Video Mode Offset Addresses	147
C.5.6.3 FRAME_INTERVAL_INQ	C.5.6.1 Image Size and Position	148
C.5.7 Pixel Formats       149         C.5.7.1 DATA_DEPTH: 630h       149         C.5.7.2 BAYER_MONO_CTRL: 1050h       150         C.6 Asynchronous Trigger Settings       150         C.6.1 TRIGGER_MODE: 830h       150         C.6.2 TRIGGER_DELAY: 834h       151         C.6.3 SOFTWARE_TRIGGER: 62Ch       152         C.7 Controlling Imaging Parameters       152         C.7.1 Imaging Parameters: 800h-888h       152         C.7.2 LUT: 80000h - 80048h (IIDC 1.32)       154         C.7.3 WHITE_BALANCE: 80Ch       157         C.7.4 BAYER_TILE_MAPPING: 1040h       157         C.7.5 MIRROR_IMAGE_CTRL: 1054h       158         C.7.6 SHUTTER: 81Ch       158         C.7.7 AUTO_EXPOSURE: 804h       159         C.7.7.1 AUTO_EXPOSURE: 804h       159         C.7.7.2 AUTO_SHOTTER_RANGE: 1088h       160         C.7.7.3 AUTO_GAIN_RANGE: 1098h       160         C.7.7.3 AUTO_GAIN_RANGE: 1000h       161         C.7.8 HDR: 1800h - 1884h       161         C.7.9 FRAME_INFO: 12F8h       162         C.8.1 Camera Diagnostics       163         C.8.1.2 TIME_FROM_INITIALIZE: 12E0h       164         C.8.1.3 LINK_UP_TIME: 12E4h       164         C.8.1.4 XMIT_FAILURE: 12FCh       164	C.5.6.2 COLOR_CODING_ID and COLOR_CODING_INQ	148
C.5.7.1 DATA_DEPTH: 630h	C.5.6.3 FRAME_INTERVAL_INQ	149
C.5.7.2 BAYER_MONO_CTRL: 1050h       150         C.6 Asynchronous Trigger Settings       150         C.6.1 TRIGGER_MODE: 830h       150         C.6.2 TRIGGER_DELAY: 834h       151         C.6.3 SOFTWARE_TRIGGER: 62Ch       152         C.7 Controlling Imaging Parameters       152         C.7.1 Imaging Parameters: 800h-888h       152         C.7.2 LUT: 80000h – 80048h (IIDC 1.32)       154         C.7.3 WHITE_BALANCE: 80Ch       157         C.7.4 BAYER_TILE_MAPPING: 1040h       157         C.7.5 MIRROR_IMAGE_CTRL: 1054h       158         C.7.6 SHUTTER: 81Ch       158         C.7.7 AUTO_EXPOSURE: 804h       159         C.7.7.1 AUTO_EXPOSURE RANGE: 1088h       160         C.7.7.2 AUTO_SHUTTER_RANGE: 1098h       160         C.7.7.3 AUTO_GAIN_RANGE: 1040h       161         C.7.8 HDR: 1800h – 1884h       161         C.7.9 FRAME_INFO: 12F8h       162         C.8.1 Camera Diagnostics       163         C.8.1.1 INITIALIZE: 000h       164         C.8.1.2 TIME_FROM_INITIALIZE: 12E0h       164         C.8.1.3 LINK_UP_TIME: 12E4h       164         C.8.1.4 XMIT_FAILURE: 12FCh       164         C.8.1.5 VMODE_ERROR_STATUS: 628h       165	C.5.7 Pixel Formats	149
C.6 Asynchronous Trigger Settings       150         C.6.1 TRIGGER_MODE: 830h       150         C.6.2 TRIGGER_DELAY: 834h       151         C.6.3 SOFTWARE_TRIGGER: 62Ch       152         C.7 Controlling Imaging Parameters       152         C.7.1 Imaging Parameters: 800h-888h       152         C.7.2 LUT: 80000h – 80048h (IIDC 1.32)       154         C.7.3 WHITE_BALANCE: 80Ch       157         C.7.4 BAYER_TILE_MAPPING: 1040h       157         C.7.5 MIRROR_IMAGE_CTRL: 1054h       158         C.7.6 SHUTTER: 81Ch       158         C.7.7 AUTO_EXPOSURE: 804h       159         C.7.7.1 AUTO_EXPOSURE_RANGE: 1088h       160         C.7.7.2 AUTO_SHUTTER_RANGE: 1098h       160         C.7.7.3 AUTO_GAIN_RANGE: 1040h       161         C.7.9 FRAME_INFO: 12F8h       162         C.8 Troubleshooting       163         C.8.1 Camera Diagnostics       163         C.8.1.1 INITIALIZE: 000h       164         C.8.1.2 TIME_FROM_INITIALIZE: 12E0h       164         C.8.1.3 LINK_UP_TIME: 12F4h       164         C.8.1.5 VMODE_ERROR_STATUS: 628h       165	C.5.7.1 DATA_DEPTH: 630h	149
C.6.1 TRIGGER_MODE: 830h       150         C.6.2 TRIGGER_DELAY: 834h       151         C.6.3 SOFTWARE_TRIGGER: 62Ch       152         C.7 Controlling Imaging Parameters       152         C.7.1 Imaging Parameters: 800h-888h       152         C.7.2 LUT: 80000h – 80048h (IIDC 1.32)       154         C.7.3 WHITE_BALANCE: 80Ch       157         C.7.4 BAYER_TILE_MAPPING: 1040h       157         C.7.5 MIRROR_IMAGE_CTRL: 1054h       158         C.7.6 SHUTTER: 81Ch       158         C.7.7 AUTO_EXPOSURE: 804h       159         C.7.7.1 AUTO_EXPOSURE_RANGE: 1088h       160         C.7.7.2 AUTO_SHUTTER_RANGE: 1098h       160         C.7.7.3 AUTO_GAIN_RANGE: 1000h       161         C.7.8 HDR: 1800h – 1884h       161         C.7.9 FRAME_INFO: 12F8h       162         C.8 Troubleshooting       163         C.8.1.1 INITIALIZE: 000h       164         C.8.1.2 TIME_FROM_INITIALIZE: 12E0h       164         C.8.1.3 LINK_UP_TIME: 12E4h       164         C.8.1.5 VMODE_ERROR_STATUS: 628h       165	C.5.7.2 BAYER_MONO_CTRL: 1050h	150
C.6.2 TRIGGER_DELAY: 834h       151         C.6.3 SOFTWARE_TRIGGER: 62Ch       152         C.7 Controlling Imaging Parameters       152         C.7.1 Imaging Parameters: 800h-888h       152         C.7.2 LUT: 80000h – 80048h (IIDC 1.32)       154         C.7.3 WHITE_BALANCE: 80Ch       157         C.7.4 BAYER_TILE_MAPPING: 1040h       157         C.7.5 MIRROR_IMAGE_CTRL: 1054h       158         C.7.6 SHUTTER: 81Ch       158         C.7.7 AUTO_EXPOSURE: 804h       159         C.7.7.1 AUTO_EXPOSURE_RANGE: 1088h       160         C.7.7.2 AUTO_SHUTTER_RANGE: 1088h       160         C.7.7.3 AUTO_GAIN_RANGE: 10A0h       161         C.7.8 HDR: 1800h – 1884h       161         C.7.9 FRAME_INFO: 12F8h       162         C.8 Troubleshooting       163         C.8.1 Camera Diagnostics       163         C.8.1.2 TIME_FROM_INITIALIZE: 12E0h       164         C.8.1.3 LINK_UP_TIME: 12E4h       164         C.8.1.4 XMIT_FAILURE: 12FCh       164         C.8.1.5 VMODE_ERROR_STATUS: 628h       165	C.6 Asynchronous Trigger Settings	150
C.6.3 SOFTWARE_TRIGGER: 62Ch       152         C.7 Controlling Imaging Parameters       152         C.7.1 Imaging Parameters: 800h-888h       152         C.7.2 LUT: 80000h – 80048h (IIDC 1.32)       154         C.7.3 WHITE_BALANCE: 80Ch       157         C.7.4 BAYER_TILE_MAPPING: 1040h       157         C.7.5 MIRROR_IMAGE_CTRL: 1054h       158         C.7.6 SHUTTER: 81Ch       158         C.7.7 AUTO_EXPOSURE: 804h       159         C.7.7.1 AUTO_EXPOSURE: 804h       150         C.7.7.2 AUTO_SHUTTER_RANGE: 1088h       160         C.7.7.3 AUTO_GAIN_RANGE: 1098h       160         C.7.7.3 AUTO_GAIN_RANGE: 1000h       161         C.7.8 HDR: 1800h – 1884h       161         C.7.9 FRAME_INFO: 12F8h       162         C.8 Troubleshooting       163         C.8.1.1 INITIALIZE: 000h       164         C.8.1.2 TIME_FROM_INITIALIZE: 12E0h       164         C.8.1.3 LINK_UP_TIME: 12E4h       164         C.8.1.4 XMIT_FAILURE: 12FCh       164         C.8.1.5 VMODE_ERROR_STATUS: 628h       165	C.6.1 TRIGGER_MODE: 830h	150
C.7 Controlling Imaging Parameters	C.6.2 TRIGGER_DELAY: 834h	151
C.7.1 Imaging Parameters: 800h-888h       152         C.7.2 LUT: 80000h – 80048h (IIDC 1.32)       154         C.7.3 WHITE_BALANCE: 80Ch       157         C.7.4 BAYER_TILE_MAPPING: 1040h       157         C.7.5 MIRROR_IMAGE_CTRL: 1054h       158         C.7.6 SHUTTER: 81Ch       158         C.7.7 AUTO_EXPOSURE: 804h       159         C.7.7.1 AUTO_EXPOSURE RANGE: 1088h       160         C.7.7.2 AUTO_SHUTTER_RANGE: 1098h       160         C.7.7.3 AUTO_GAIN_RANGE: 10A0h       161         C.7.8 HDR: 1800h – 1884h       161         C.7.9 FRAME_INFO: 12F8h       162         C.8 Troubleshooting       163         C.8.1.1 INITIALIZE: 000h       164         C.8.1.2 TIME_FROM_INITIALIZE: 12E0h       164         C.8.1.3 LINK_UP_TIME: 12E4h       164         C.8.1.4 XMIT_FAILURE: 12FCh       164         C.8.1.5 VMODE_ERROR_STATUS: 628h       165	C.6.3 SOFTWARE_TRIGGER: 62Ch	152
C.7.2 LUT: 80000h – 80048h (IIDC 1.32)       154         C.7.3 WHITE_BALANCE: 80Ch       157         C.7.4 BAYER_TILE_MAPPING: 1040h       157         C.7.5 MIRROR_IMAGE_CTRL: 1054h       158         C.7.6 SHUTTER: 81Ch       158         C.7.7 AUTO_EXPOSURE: 804h       159         C.7.7.1 AUTO_EXPOSURE_RANGE: 1088h       160         C.7.7.2 AUTO_SHUTTER_RANGE: 1098h       160         C.7.7.3 AUTO_GAIN_RANGE: 1040h       161         C.7.9 FRAME_INFO: 12F8h       162         C.8 Troubleshooting       163         C.8.1 Camera Diagnostics       163         C.8.1.1 INITIALIZE: 000h       164         C.8.1.2 TIME_FROM_INITIALIZE: 12E0h       164         C.8.1.3 LINK_UP_TIME: 12E4h       164         C.8.1.4 XMIT_FAILURE: 12FCh       164         C.8.1.5 VMODE_ERROR_STATUS: 628h       165	C.7 Controlling Imaging Parameters	152
C.7.3 WHITE_BALANCE: 80Ch       157         C.7.4 BAYER_TILE_MAPPING: 1040h       157         C.7.5 MIRROR_IMAGE_CTRL: 1054h       158         C.7.6 SHUTTER: 81Ch       158         C.7.7 AUTO_EXPOSURE: 804h       159         C.7.7.1 AUTO_EXPOSURE_RANGE: 1088h       160         C.7.7.2 AUTO_SHUTTER_RANGE: 1098h       160         C.7.7.3 AUTO_GAIN_RANGE: 10A0h       161         C.7.8 HDR: 1800h - 1884h       161         C.7.9 FRAME_INFO: 12F8h       162         C.8 Troubleshooting       163         C.8.1 Camera Diagnostics       163         C.8.1.1 INITIALIZE: 000h       164         C.8.1.2 TIME_FROM_INITIALIZE: 12E0h       164         C.8.1.3 LINK_UP_TIME: 12E4h       164         C.8.1.4 XMIT_FAILURE: 12FCh       164         C.8.1.5 VMODE_ERROR_STATUS: 628h       165	C.7.1 Imaging Parameters: 800h-888h	152
C.7.4 BAYER_TILE_MAPPING: 1040h       157         C.7.5 MIRROR_IMAGE_CTRL: 1054h       158         C.7.6 SHUTTER: 81Ch       158         C.7.7 AUTO_EXPOSURE: 804h       159         C.7.7.1 AUTO_EXPOSURE_RANGE: 1088h       160         C.7.7.2 AUTO_SHUTTER_RANGE: 1098h       160         C.7.7.3 AUTO_GAIN_RANGE: 10A0h       161         C.7.8 HDR: 1800h – 1884h       161         C.7.9 FRAME_INFO: 12F8h       162         C.8 Troubleshooting       163         C.8.1 Camera Diagnostics       163         C.8.1.1 INITIALIZE: 000h       164         C.8.1.2 TIME_FROM_INITIALIZE: 12E0h       164         C.8.1.3 LINK_UP_TIME: 12E4h       164         C.8.1.4 XMIT_FAILURE: 12FCh       164         C.8.1.5 VMODE_ERROR_STATUS: 628h       165	C.7.2 LUT: 80000h – 80048h (IIDC 1.32)	154
C.7.5 MIRROR_IMAGE_CTRL: 1054h       158         C.7.6 SHUTTER: 81Ch       158         C.7.7 AUTO_EXPOSURE: 804h       159         C.7.7.1 AUTO_EXPOSURE_RANGE: 1088h       160         C.7.7.2 AUTO_SHUTTER_RANGE: 1098h       160         C.7.7.3 AUTO_GAIN_RANGE: 10A0h       161         C.7.8 HDR: 1800h – 1884h       161         C.7.9 FRAME_INFO: 12F8h       162         C.8 Troubleshooting       163         C.8.1 Camera Diagnostics       163         C.8.1.2 TIME_FROM_INITIALIZE: 12E0h       164         C.8.1.3 LINK_UP_TIME: 12E4h       164         C.8.1.4 XMIT_FAILURE: 12FCh       164         C.8.1.5 VMODE_ERROR_STATUS: 628h       165	C.7.3 WHITE_BALANCE: 80Ch	157
C.7.6 SHUTTER: 81Ch       158         C.7.7 AUTO_EXPOSURE: 804h       159         C.7.7.1 AUTO_EXPOSURE_RANGE: 1088h       160         C.7.7.2 AUTO_SHUTTER_RANGE: 1098h       160         C.7.7.3 AUTO_GAIN_RANGE: 10A0h       161         C.7.8 HDR: 1800h – 1884h       161         C.7.9 FRAME_INFO: 12F8h       162         C.8 Troubleshooting       163         C.8.1 Camera Diagnostics       163         C.8.1.1 INITIALIZE: 000h       164         C.8.1.2 TIME_FROM_INITIALIZE: 12E0h       164         C.8.1.3 LINK_UP_TIME: 12E4h       164         C.8.1.4 XMIT_FAILURE: 12FCh       164         C.8.1.5 VMODE_ERROR_STATUS: 628h       165	C.7.4 BAYER_TILE_MAPPING: 1040h	157
C.7.7 AUTO_EXPOSURE: 804h       159         C.7.7.1 AUTO_EXPOSURE_RANGE: 1088h       160         C.7.7.2 AUTO_SHUTTER_RANGE: 1098h       160         C.7.7.3 AUTO_GAIN_RANGE: 10A0h       161         C.7.8 HDR: 1800h – 1884h       161         C.7.9 FRAME_INFO: 12F8h       162         C.8 Troubleshooting       163         C.8.1 Camera Diagnostics       163         C.8.1.1 INITIALIZE: 000h       164         C.8.1.2 TIME_FROM_INITIALIZE: 12E0h       164         C.8.1.3 LINK_UP_TIME: 12E4h       164         C.8.1.4 XMIT_FAILURE: 12FCh       164         C.8.1.5 VMODE_ERROR_STATUS: 628h       165	C.7.5 MIRROR_IMAGE_CTRL: 1054h	158
C.7.7.1 AUTO_EXPOSURE_RANGE: 1088h       160         C.7.7.2 AUTO_SHUTTER_RANGE: 1098h       160         C.7.7.3 AUTO_GAIN_RANGE: 10A0h       161         C.7.8 HDR: 1800h – 1884h       161         C.7.9 FRAME_INFO: 12F8h       162         C.8 Troubleshooting       163         C.8.1 Camera Diagnostics       163         C.8.1.1 INITIALIZE: 000h       164         C.8.1.2 TIME_FROM_INITIALIZE: 12E0h       164         C.8.1.3 LINK_UP_TIME: 12E4h       164         C.8.1.4 XMIT_FAILURE: 12FCh       164         C.8.1.5 VMODE_ERROR_STATUS: 628h       165	C.7.6 SHUTTER: 81Ch	158
C.7.7.2 AUTO_SHUTTER_RANGE: 1098h       160         C.7.7.3 AUTO_GAIN_RANGE: 10A0h       161         C.7.8 HDR: 1800h – 1884h       161         C.7.9 FRAME_INFO: 12F8h       162         C.8 Troubleshooting       163         C.8.1 Camera Diagnostics       163         C.8.1.1 INITIALIZE: 000h       164         C.8.1.2 TIME_FROM_INITIALIZE: 12E0h       164         C.8.1.3 LINK_UP_TIME: 12E4h       164         C.8.1.4 XMIT_FAILURE: 12FCh       164         C.8.1.5 VMODE_ERROR_STATUS: 628h       165	C.7.7 AUTO_EXPOSURE: 804h	159
C.7.7.3 AUTO_GAIN_RANGE: 10A0h       161         C.7.8 HDR: 1800h – 1884h       161         C.7.9 FRAME_INFO: 12F8h       162         C.8 Troubleshooting       163         C.8.1 Camera Diagnostics       163         C.8.1.1 INITIALIZE: 000h       164         C.8.1.2 TIME_FROM_INITIALIZE: 12E0h       164         C.8.1.3 LINK_UP_TIME: 12E4h       164         C.8.1.4 XMIT_FAILURE: 12FCh       164         C.8.1.5 VMODE_ERROR_STATUS: 628h       165	C.7.7.1 AUTO_EXPOSURE_RANGE: 1088h	160
C.7.8 HDR: 1800h – 1884h       161         C.7.9 FRAME_INFO: 12F8h       162         C.8 Troubleshooting       163         C.8.1 Camera Diagnostics       163         C.8.1.1 INITIALIZE: 000h       164         C.8.1.2 TIME_FROM_INITIALIZE: 12E0h       164         C.8.1.3 LINK_UP_TIME: 12E4h       164         C.8.1.4 XMIT_FAILURE: 12FCh       164         C.8.1.5 VMODE_ERROR_STATUS: 628h       165	C.7.7.2 AUTO_SHUTTER_RANGE: 1098h	160
C.7.8 HDR: 1800h – 1884h       161         C.7.9 FRAME_INFO: 12F8h       162         C.8 Troubleshooting       163         C.8.1 Camera Diagnostics       163         C.8.1.1 INITIALIZE: 000h       164         C.8.1.2 TIME_FROM_INITIALIZE: 12E0h       164         C.8.1.3 LINK_UP_TIME: 12E4h       164         C.8.1.4 XMIT_FAILURE: 12FCh       164         C.8.1.5 VMODE_ERROR_STATUS: 628h       165	C.7.7.3 AUTO_GAIN_RANGE: 10A0h	161
C.8 Troubleshooting       163         C.8.1 Camera Diagnostics       163         C.8.1.1 INITIALIZE: 000h       164         C.8.1.2 TIME_FROM_INITIALIZE: 12E0h       164         C.8.1.3 LINK_UP_TIME: 12E4h       164         C.8.1.4 XMIT_FAILURE: 12FCh       164         C.8.1.5 VMODE_ERROR_STATUS: 628h       165		
C.8.1 Camera Diagnostics       163         C.8.1.1 INITIALIZE: 000h       164         C.8.1.2 TIME_FROM_INITIALIZE: 12E0h       164         C.8.1.3 LINK_UP_TIME: 12E4h       164         C.8.1.4 XMIT_FAILURE: 12FCh       164         C.8.1.5 VMODE_ERROR_STATUS: 628h       165	C.7.9 FRAME_INFO: 12F8h	162
C.8.1.1 INITIALIZE: 000h       164         C.8.1.2 TIME_FROM_INITIALIZE: 12E0h       164         C.8.1.3 LINK_UP_TIME: 12E4h       164         C.8.1.4 XMIT_FAILURE: 12FCh       164         C.8.1.5 VMODE_ERROR_STATUS: 628h       165	C.8 Troubleshooting	163
C.8.1.2 TIME_FROM_INITIALIZE: 12E0h       164         C.8.1.3 LINK_UP_TIME: 12E4h       164         C.8.1.4 XMIT_FAILURE: 12FCh       164         C.8.1.5 VMODE_ERROR_STATUS: 628h       165	C.8.1 Camera Diagnostics	163
C.8.1.3 LINK_UP_TIME: 12E4h       164         C.8.1.4 XMIT_FAILURE: 12FCh       164         C.8.1.5 VMODE_ERROR_STATUS: 628h       165	C.8.1.1 INITIALIZE: 000h	164
C.8.1.3 LINK_UP_TIME: 12E4h       164         C.8.1.4 XMIT_FAILURE: 12FCh       164         C.8.1.5 VMODE_ERROR_STATUS: 628h       165	C.8.1.2 TIME_FROM_INITIALIZE: 12E0h	164
C.8.1.5 VMODE_ERROR_STATUS: 628h		
C.8.1.5 VMODE_ERROR_STATUS: 628h		



C.8.1.7 TEST_PATTERN: 104Ch	165
C.8.2 PIXEL_DEFECT_CTRL: 1A60h	165
Contacting Point Grey Research	167
Revision History	168



## **List of Tables**

Table 1.1: Temperature Sensor Specifications	27
Table 4.1: GPIO pin assignments (as shown looking at rear of camera)	44
Table 5.1: FL3-GE-03S1M Maximum Frame Rates	57
Table 5.2: FL3-GE-03S1C Maximum Frame Rates	58
Table 5.3: FL3-GE-03S2M Frame Rates	58
Table 5.4: FL3-GE-03S2C Frame Rates	59
Table 5.5: FL3-GE-08S2M Frame Rates	59
Table 5.6: FL3-GE-08S2C Frame Rates	60
Table 5.7: FL3-GE-13S2M Frame Rates	60
Table 5.8: FL3-GE-13S2C Frame Rates	61
Table 5.9: FL3-GE-14S3M Frame Rates	61
Table 5.10: FL3-GE-14S3C Frame Rates	62
Table 5.11: FL3-GE-20S4M Frame Rates	62
Table 5.12: FL3-GE-20S4C Frame Rates	63
Table 5.13: FL3-GE-28S4M Frame Rates	63
Table 5.14: FL3-GE-28S4C Frame Rates	64
Table 5.15: FL3-GE-50S5M Frame Rates	65
Table 5.16: FL3-GE-50S5C Frame Rates	65
Table 8.1: LED During Camera Power-up and Operation	95
Table C.1: CSR Mode Control Descriptions	110
Table C.2: Custom Video Mode Inquiry Register Offset Addresses	147



## **List of Figures**

Figure 1.1: FL3-GE-03S1M Quantum Efficiency	4
Figure 1.2: FL3-GE-03S1C Quantum Efficiency	5
Figure 1.3: FL3-GE-03S2M Quantum Efficiency	e
Figure 1.4: FL3-GE-03S2C Quantum Efficiency	7
Figure 1.5: FL3-GE-08S2M Quantum Efficiency	8
Figure 1.6: FL3-GE-08S2C Quantum Efficiency	9
Figure 1.7: FL3-GE-13S2M Quantum Efficiency	10
Figure 1.8: FL3-GE-13S2C Quantum Efficiency	11
Figure 1.9: FL3-GE-14S3M Quantum Efficiency	12
Figure 1.10: FL3-GE-14S3C Quantum Efficiency	13
Figure 1.11: FL3-GE-20S4M Quantum Efficiency	14
Figure 1.12: FL3-GE-20S4C Quantum Efficiency	15
Figure 1.13: FL3-GE-28S4M Quantum Efficiency	16
Figure 1.14: FL3-GE-28S4C Quantum Efficiency	17
Figure 1.15: FL3-GE-50S5M Quantum Efficiency	18
Figure 1.16: FL3-GE-50S5C Quantum Efficiency	19
Figure 1.17: FL3-GE Mono Quantum Efficiency	20
Figure 1.18: FL3-GE Mono Dynamic Range	20
Figure 1.19: Camera Dimensional Diagram	23
Figure 1.20: Tripod Adapter Dimensional Diagram	24
Figure 1.21: IR filter transmittance graph	26
Figure 2.1: Point Grey GigE Configurator	36
Figure 4.1: Debouncer Filtering Invalid Signals	48
Figure 4.2: Optical input circuit	49
Figure 4.3: Optical output circuit	50
Figure 4.4: GPIO2/3 Circuit	51
Figure 5.1: 2x Vertical and 2x Horizontal Binning	53
Figure 6.1: External trigger timing characteristics	68
Figure 6.2: Relationship Between External Triggering and Video Mode Change Request	69
Figure 6.3: Software trigger timing	70
Figure 6.4: Trigger Mode 0 ("Standard External Trigger Mode")	71
Figure 6.5: Trigger Mode 1 ("Bulb Shutter Mode")	72
Figure 6.6: Trigger Mode 3 ("Skip Frames Mode")	73
Figure 6.7: Trigger Mode 4 ("Multiple Exposure Preset Mode")	74
Figure 6.8: Trigger Mode 5 ("Multiple Exposure Pulse Width Mode")	



Figure 6.9: Trigger Mode 13 ("Low Smear Trigger Mode")	76
Figure 6.10: Trigger Mode 14 ("Overlapped Exposure/Readout Mode")	77
Figure 6.11: Trigger Mode 15 ("Multi-Shot Trigger Mode")	78
Figure 7.1: Example Bayer Tile Pattern	90
Figure 8.1: Test Pattern Sample Image	96



### **About This Manual**

This manual provides the user with a detailed specification of the Flea3 GigE camera system. The user should be aware that the camera system is complex and dynamic – if any errors or omissions are found during experimentation, please contact us. (See Contacting Point Grey Research on page 167.)

This document is subject to change without notice.



All model-specific information presented in this manual reflects functionality available in the model's firmware version.

For more information see Camera Firmware on page 43.

#### Where to Find Information

Chapter	What You Will Find
1. Welcome	General camera specifications and specific model specifications (page 1) Camera properties, including diagrams (page 22)
2. Getting Started	Preparation for installing the camera (page 30) Installation instructions (page 32) Introduction to camera controls (page 33)
3. General Operation	Powering the camera (page 40) Device Information (page 40) User Configuration sets (page 41) On-camera frame buffer (page 42) Flash memory (page 43) Firmware (page 43)
4. Input/Output Control	GPIO Modes (page 44) Programmable Strobe Output (page 46) Pulse Width Modulation (page 47) Serial Communication (page 47) Debouncer (page 48) GPIO Electrical Characteristics (page 48)
5. Video Formats, Modes, and Frame Rates	Overview and descriptions of Video Modes (page 53) Calculating Frame Rate (page 55) Supported Formats, Modes, and Frame Rates for each model (page 57) Image Format Control (page 66)
6. Image Acquisition and Transmission	Asynchronous Triggering (page 68) and Supported Trigger Modes (page 71)



Chapter	What You Will Find
7. Image Parameters and Control	Brightness (page 82) Shutter (page 88) Gain (page 82) Auto Exposure (page 91) High Dynamic Range (page 93) Gamma and Lookup Table (page 85) Saturation (page 83) Hue (page 84) Sharpness (page 84) White Balance (page 87) Bayer Color Processing (page 90) Image Flip/Mirror (page 91) Embedded Image Information (page 93)
8. Troubleshooting	How to get support (page 95) Status LED (page 95) Test Pattern (page 96) Blemish Pixels (page 96) Vertical Smear (page 97)
Appendices	GenlCam Features (page 99), GigE Vision Bootstrap Registers (page 108), and Using Control and Status Registers (page 110)
Contacting Point Grey	How to reach Point Grey Research Inc. (page 167)

### **Document Conventions**

This manual uses the following to provide you with additional information:



A note that contains information that is distinct from the main body of text. For example, drawing attention to a difference between models; or a reminder of a limitation.



A note that contains a warning to proceed with caution and care, or to indicate that the information is meant for an advanced user. For example, indicating that an action may void the camera's warranty.

If further information can be found in our Knowledge Base, a list of articles is provided.

#### **Related Knowledge Base Articles**

Title	Article
Title of the Article	Link to the article on the Point Grey website

If there are further resources available, a link is provided either to an external website, or to the FlyCapture2 SDK.

#### **Related Resources**

Title	Link
Title of the resource	Link to the resource



## 1 Welcome to Flea3 GigE

The fully redesigned, next generation Flea3 camera series builds on the success of the ultra-compact Flea2 by adding new Sony image sensors to the line-up. The Flea3 also offers a host of new features, including enhanced opto-isolated GPIO; an on-camera frame buffer; non-volatile flash memory for user data storage; new trigger modes; and improved imaging performance.

### 1.1 Flea3 GigE Specifications

MODEL	VERSION	MP	IMAGING SENSOR
FL3-GE-03S1C-C	Color	0.2.04.0	■ Sony ICX618 CCD, 1/4", 5.6 μm
FL3-GE-03S1M-C	Mono	0.3 MP	■ Global Shutter ■ 648x488 at 120 FPS
FL3-GE-03S2C-C	Color	0.3 MP	■ Sony ICX424 CCD, 1/3", 7.4 μm ■ Global Shutter
FL3-GE-03S2M-C	Mono	U.S IVII	■ 648x488 at 82 FPS
FL3-GE-08S2C-C	Color	0.8 MP	■ Sony ICX204 CCD, 1/3", 4.65 µm ■ Global Shutter
FL3-GE-08S2M-C	Mono	U.8 IVIP	■ 1032x776 at 31 FPS
FL3-GE-13S2C-C FL3-GE-13S2C-CS	Color	1.3 MP	■ Sony ICX445 CCD, 1/3", 3.75 µm ■ Global Shutter
FL3-GE-13S2M-C FL3-GE-13S2M-CS	Mono	1.5 IVIP	■ 1288x964 at 31 FPS
FL3-GE-14S3C-C	Color	1.4 MP	■ Sony ICX267 CCD, 1/2", 4.65 µm ■ Global Shutter
FL3-GE-14S3M-C	Mono	1.4 WIF	■ 1384x1032 at 18 FPS
FL3-GE-20S4C-C	Color	2.0 MP	■ Sony ICX274 CCD, 1/1.8", 4.4 µm ■ Global Shutter
FL3-GE-20S4M-C	Mono	2.0 1017	■ 1624x1224 at 15 FPS
FL3-GE-28S4C-C	Color	2.8 MP	■ Sony ICX687 CCD, 1/1.8", 3.69 µm ■ Global Shutter
FL3-GE-28S4M-C	Mono	2.0 IVIP	■ 1928x1448 at 14 FPS
FL3-GE-50S5C-C	Color	5.0 MP	■ Sony ICX655 CCD, 2/3", 3.45 µm ■ Global Shutter
FL3-GE-50S5M-C	Mono	J.U IVIF	■ 2448x2048 at 8 FPS



	All Flea3 GigE Models	
A/D Converter	12-bit	
Video Data Output	8, 12, 16 and 24-bit digital data	
Image Data Formats	Y8, Y16, Mono8, Mono12, Mono16, Raw8, Raw12, Raw16 (all models); RGB, YUV411, YUV422, YUV 444 (color models)	
Partial Image Modes	Pixel binning and region of interest (ROI) modes	
Image Processing	Gamma, lookup table, hue, saturation, and sharpness	
Gain	Automatic/Manual/One-Push Gain modes	
Gaill	0 dB to 24 dB	
Gamma	0.50 to 4.00	
White Balance	Automatic/manual modes, programmable via software	
High Dynamic Range	Cycle 4 gain and exposure presets	
Color Processing	On-camera in YUV or RGB format, or on-PC in Raw format	
Digital Interface	Gigabit Ethernet interface with screw locks for camera control and data	
Transfer Rates	10/100/1000 Mbit/s	
GPIO	8-pin Hirose HR25 GPIO connector for power, trigger, strobe, PWM, and serial I/O, 1 opto-isolated input, 1 opto-isolated output, 2 bi-directional I/O pins	
<b>External Trigger Modes</b>	IIDC Trigger Modes 0, 1, 3, 4, 5, 13 (FL3-GE-13S2 only), 14 and 15	
Synchronization	Via external trigger or software trigger	
	Global Shutter	
Shutter	Automatic/Manual/One-Push/Extended Shutter modes	
	0.03 ms to 32 seconds (extended shutter mode)	
Image Buffer	32 MB frame buffer	
Memory Channels	2 memory channels for custom camera settings	
Flash Memory	1 MB	
Dimensions	29 mm x 29 mm x 30 mm excluding lens holder, without optics (metal case)	
Mass	38 grams (without optics)	
Power Consumption	12-24 V, <2.5 W, via GPIO	
Camera Specification	GigE Vision v1.2	
Camera Control	via FlyCapture SDK, CSRs, or third party software	
Camera Updates	In-field firmware updates	
Lens Mount	C-mount (FL3-GE-13S2 also available with CS-mount)	
Operating Temperature	0° to 45°C	
Storage Temperature	-30° to 60°C	



	All Flea3 GigE Models		
<b>Emissions Compliance</b>	CE, FCC, RoHS		
Operating System	Windows 7, Linux Ubuntu		
Warranty	Two years		

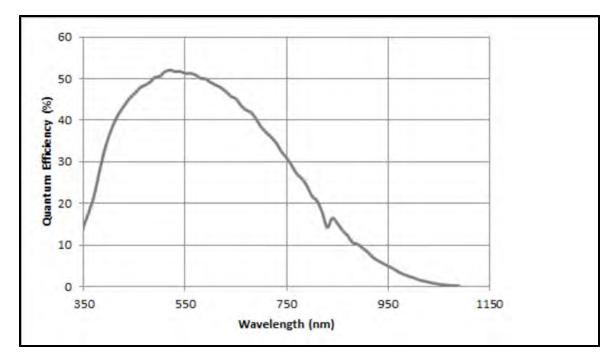


### 1.1.1 FL3-GE-03S1M (Mono) Imaging Performance

Specification	Mode 0
Full Well Depth	15800 e- at zero gain
Dynamic Range 62 dB	
Read Noise 12 e- at zero gain	
Measurements taken at maximum resolution	

Quantum Efficiency		
Peak QE Wavelength	520 nm	
Peak QE Value	52%	

Figure 1.1: FL3-GE-03S1M Quantum Efficiency

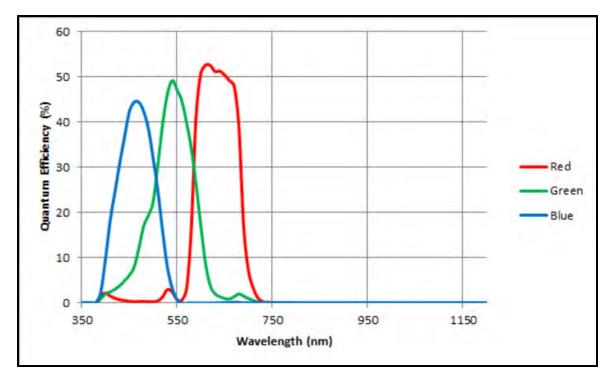


#### 1.1.2 FL3-GE-03S1C (Color) Imaging Performance

Specification	Mode 0
Full Well Depth	18500 e- at zero gain
Dynamic Range	52 dB
Read Noise 15 e- at zero gain	
Measurements taken at maximum resolution	

Quantum Efficiency		
Peak QE Wavelength Red 610 nm, Green 540 nm, Blue 470 r		
Peak QE Value	Red 52%, Green 49%, Blue 44%	

Figure 1.2: FL3-GE-03S1C Quantum Efficiency

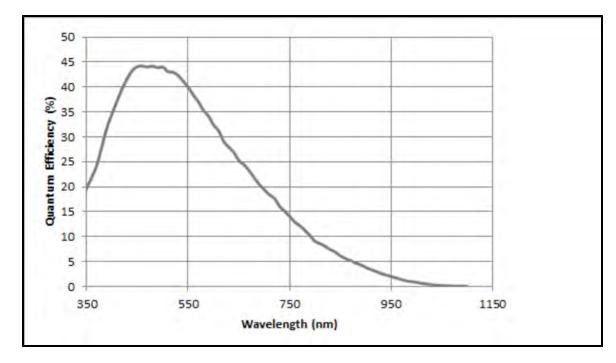


### 1.1.3 FL3-GE-03S2M (Mono) Imaging Performance

Specification	Mode 0
Full Well Depth	14200 e- at zero gain
Dynamic Range 59 dB	
Read Noise 14.4 e- at zero gain	
Measurements taken at maximum resolution	

Quantum Efficiency		
Peak QE Wavelength	479 nm	
Peak QE Value	44%	

Figure 1.3: FL3-GE-03S2M Quantum Efficiency

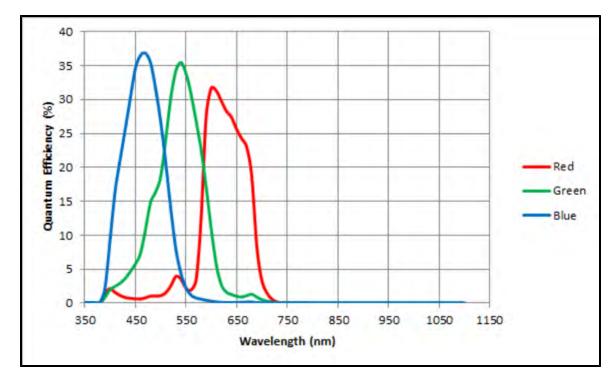


#### 1.1.4 FL3-GE-03S2C (Color) Imaging Performance

Specification	Mode 0	
Full Well Depth	<b>Depth</b> 13700 e- at zero gair	
Dynamic Range 60 dB		
<b>Read Noise</b> 12.7 e- at zero gain		
Measurements taken at maximum resolution		

Quantum Efficiency		
Peak QE Wavelength Red 609 nm, Green 539 nm, Blue 469		
Peak QE Value	Red 31%, Green 35%, Blue 37%	

Figure 1.4: FL3-GE-03S2C Quantum Efficiency

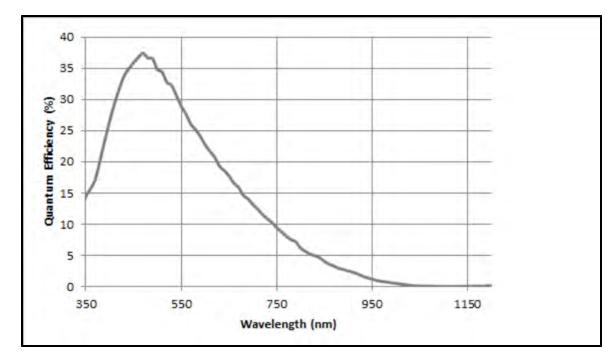


### 1.1.5 FL3-GE-08S2M (Mono) Imaging Performance

Specification	Mode 0	
Full Well Depth	Depth 12400 e- at zero gair	
Dynamic Range 60 dB		
<b>Read Noise</b> 11.6 e- at zero gain		
Measurements taken at maximum resolution		

Quantum Efficiency		
Peak QE Wavelength 470 nm		
Peak QE Value	37%	

Figure 1.5: FL3-GE-08S2M Quantum Efficiency

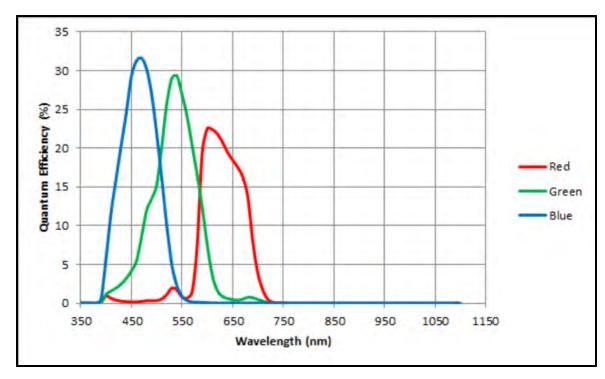


#### 1.1.6 FL3-GE-08S2C (Color) Imaging Performance

Specification	Mode 0	
Full Well Depth	oth 11900 e- at zero gain	
Dynamic Range 60 dB		
<b>Read Noise</b> 11.5 e- at zero gain		
Measurements taken at maximum resolution		

Quantum Efficiency		
Peak QE Wavelength Red 609 nm, Green 539 nm, Blue 469		
Peak QE Value	Red 22%, Green 29%, Blue 31%	

Figure 1.6: FL3-GE-08S2C Quantum Efficiency

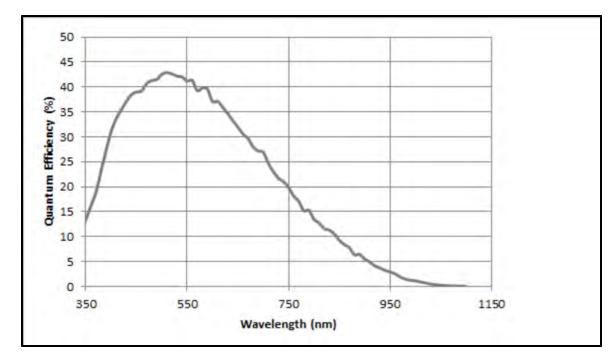


### 1.1.7 FL3-GE-13S2M (Mono) Imaging Performance

Specification	Mode 0	
Full Well Depth	7900 e- at zero gain	
Dynamic Range	58 dB	
<b>Read Noise</b> 8.3 e- at zero gain		
Measurements taken at maximum resolution		

Quantum Efficiency		
Peak QE Wavelength 519 nm		
Peak QE Value	42%	

Figure 1.7: FL3-GE-13S2M Quantum Efficiency

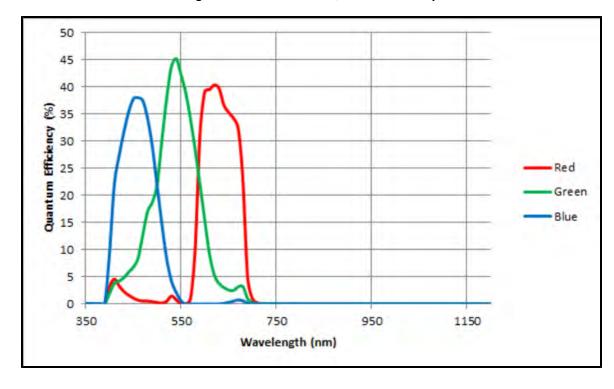


#### 1.1.8 FL3-GE-13S2C (Color) Imaging Performance

Specification	Mode 0	
Full Well Depth	8400 e- at zero gain	
Dynamic Range 60 dB		
<b>Read Noise</b> 8.5 e- at zero gain		
Measurements taken at maximum resolution		

Quantum Efficiency		
Peak QE WavelengthRed 620 nm, Green 540 nm, Blue 460 r		
Peak QE Value	Red 40%, Green 45%, Blue 38%	

Figure 1.8: FL3-GE-13S2C Quantum Efficiency

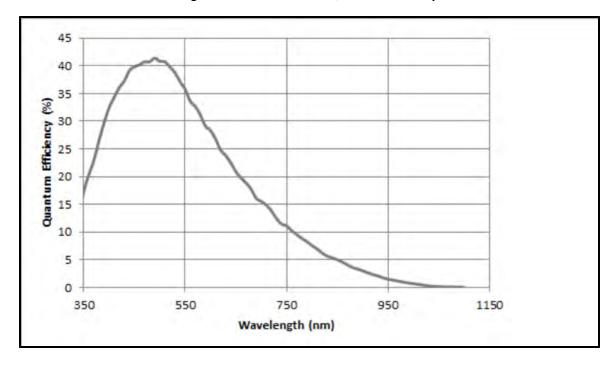


#### 1.1.9 FL3-GE-14S3M (Mono) Imaging Performance

Specification	Mode 0	
Full Well Depth	th 11700 e- at zero gair	
Dynamic Range 59 dB		
Read Noise 11 e- at zero gain		
Measurements taken at maximum resolution		

Quantum Efficiency		
Peak QE Wavelength	489 nm	
Peak QE Value	41%	

Figure 1.9: FL3-GE-14S3M Quantum Efficiency

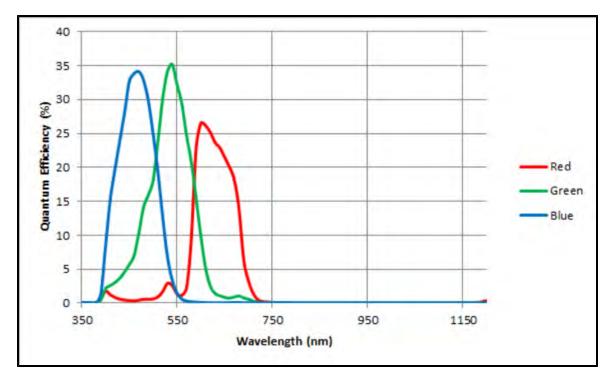


#### 1.1.10 FL3-GE-14S3C (Color) Imaging Performance

Specification	Mode 0
Full Well Depth	11400 e- at zero gain
Dynamic Range 59 dB	
Read Noise 11 e- at zero gain	
Measurements taken at maximum resolution	

Quantum Efficiency		
Peak QE Wavelength	Red 600 nm, Green 540 nm, Blue 470 nm	
Peak QE Value	Red 26%, Green 35%, Blue 34%	

Figure 1.10: FL3-GE-14S3C Quantum Efficiency

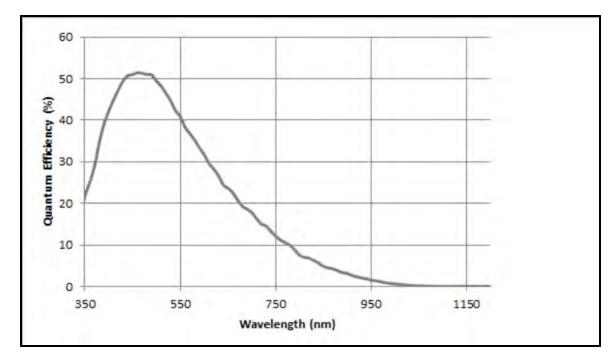


### 1.1.11 FL3-GE-20S4M (Mono) Imaging Performance

Specification	Mode 0	
Full Well Depth	7400 e- at zero gair	
Dynamic Range	9 59 dB	
<b>Read Noise</b> 8.4 e- at zero gain		
Measurements taken at maximum resolution		

Quantum Efficiency		
Peak QE Wavelength	460 nm	
Peak QE Value	51%	

Figure 1.11: FL3-GE-20S4M Quantum Efficiency

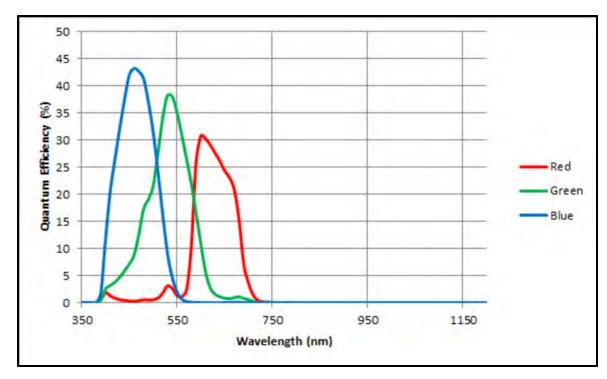


#### 1.1.12 FL3-GE-20S4C (Color) Imaging Performance

Specification	Mode 0	
Full Well Depth	8100 e- at zero gain	
Dynamic Range	60 dB	
<b>Read Noise</b> 7.2 e- at zero gain		
Measurements taken at maximum resolution		

Quantum Efficiency		
Peak QE WavelengthRed 600 nm, Green 530 nm, Blue 460		
Peak QE Value	Red 30%, Green 38%, Blue 43%	

Figure 1.12: FL3-GE-20S4C Quantum Efficiency



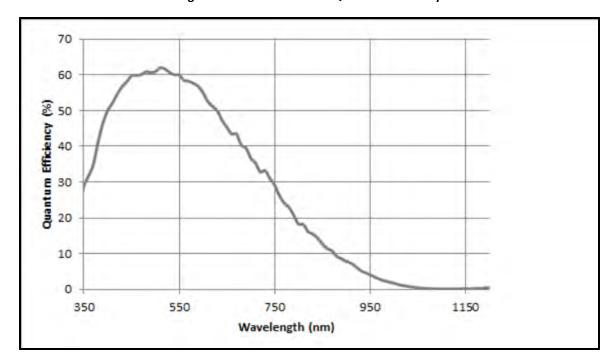
#### 1.1.13 FL3-GE-28S4M (Mono) Imaging Performance

Preliminary results; subject to change.

Specification	Mode 0	
Full Well Depth	8700 e- at zero gain	
Dynamic Range	58 dB	
Read Noise 10 e- at zero gain		
Measurements taken at maximum resolution		

Quantum Efficiency		
Peak QE Wavelength 510 nm		
Peak QE Value	62%	

Figure 1.13: FL3-GE-28S4M Quantum Efficiency



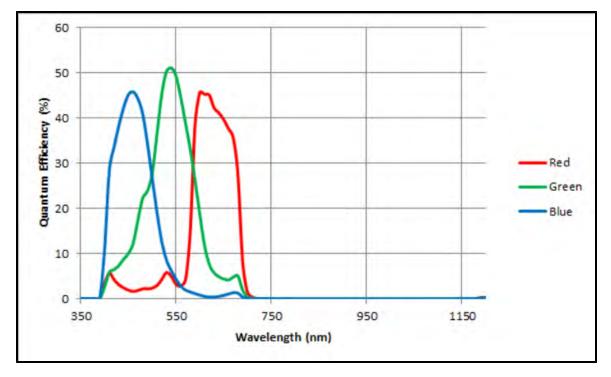
### 1.1.14 FL3-GE-28S4C (Color) Imaging Performance

Preliminary results; subject to change.

Specification	Mode 0	
Full Well Depth	8700 e- at zero gain	
Dynamic Range	59 dB	
<b>Read Noise</b> 10 e- at zero gain		
Measurements taken at maximum resolution		

Quantum Efficiency		
Peak QE WavelengthRed 600 nm, Green 540 nm, Blue 460		
Peak QE Value	Red 45%, Green 51%, Blue 46%	

Figure 1.14: FL3-GE-28S4C Quantum Efficiency

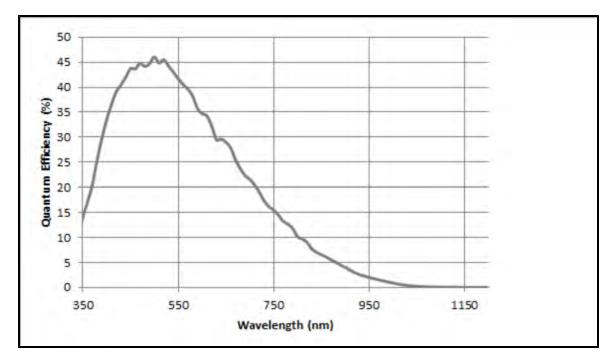


### 1.1.15 FL3-GE-50S5M (Mono) Imaging Performance

Specification	Mode 0	
Full Well Depth	6100 e- at zero gain	
Dynamic Range	56 dB	
<b>Read Noise</b> 9.3 e- at zero gain		
Measurements taken at maximum resolution		

Quantum Efficiency		
Peak QE Wavelength	500 nm	
Peak QE Value	46%	

Figure 1.15: FL3-GE-50S5M Quantum Efficiency

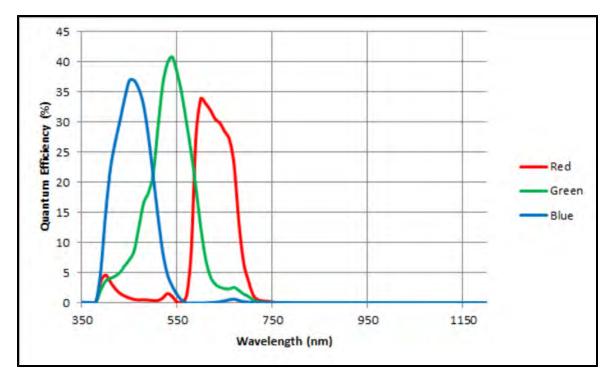


#### 1.1.16 FL3-GE-50S5C (Color) Imaging Performance

Specification	Mode 0
Full Well Depth	5900 e- at zero gain
Dynamic Range	57 dB
Read Noise	8.2 e- at zero gain
Measurements taken at maximum resolution	

Quantum Efficiency	
Peak QE Wavelength	Red 600 nm, Green 540 nm, Blue 460 nm
Peak QE Value	Red 34%, Green 41%, Blue 37%

Figure 1.16: FL3-GE-50S5C Quantum Efficiency



#### 1.1.17 Flea3 GigE (Mono) Comparison

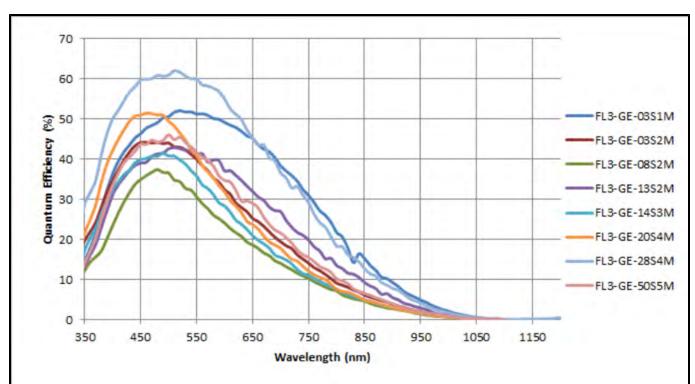
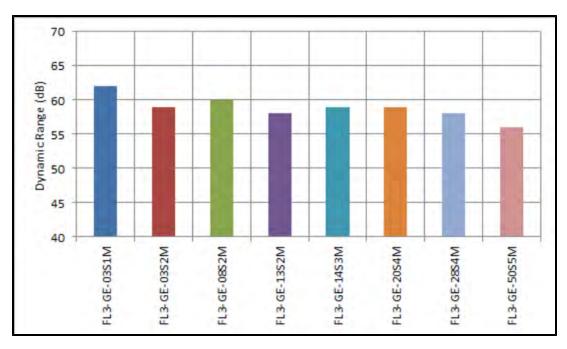


Figure 1.17: FL3-GE Mono Quantum Efficiency





## 1.2 Analog-to-Digital Conversion

The camera sensor incorporates an A/D converter to digitize the images produced by the CCD. The 12-bit conversion produces 4,096 possible digital image values between 0 and 65,520, left-aligned across a 2-byte data format. The four unused bits are padded with zeros.

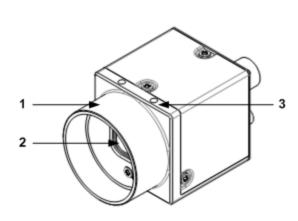
The following table illustrates the most important aspects of the ADC.

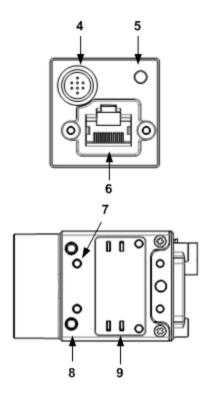
Resolution	12-bit, 50 MHz
Pixel Gain Amplifier	-3 dB to 6 dB, 3 dB steps
Variable Gain Amplifier	6 dB to 42 dB, 10-bit
Black Level Clamp	0 LSB to 255.75 LSB, 0.25 LSB steps



# 1.3 Flea3 GigE Mechanical Properties

# 1.3.1 Physical Description





### 1. Lens holder (C-mount)

See Lens Mounting on page 24

### 2. Glass/IR filter system

See Dust Protection on page 25 and Infrared Cut-Off Filters on page 26

#### 3. M2x2.5 mounting holes

See Mounting with the Case or Mounting Bracket on page 25

### 4. General purpose I/O connector

See General Purpose Input/Output (GPIO) on page 44 and GPIO Electrical Characteristics on page 48

#### 5. Status LED

See Status Indicator LED on page 95

### 6. GigE connector

See Ethernet Connector on page 28.

#### 7. M2x2.5 mounting holes

### 8. M3x2.5 mounting holes

See Mounting with the Case or Mounting Bracket on page 25

### 9. Camera label

Contains camera information such as model name, serial number and required compliance information.



### 1.3.2 Camera Dimensions

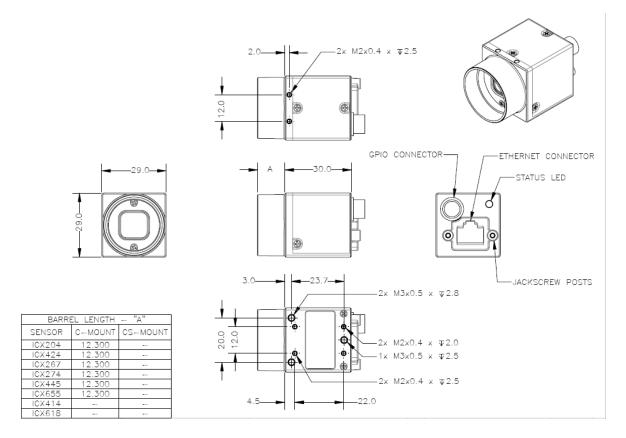


Figure 1.19: Camera Dimensional Diagram



To obtain 3D models, contact support@ptgrey.com.

# 1.3.3 Tripod Adapter Dimensions

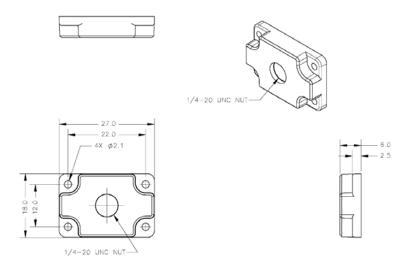


Figure 1.20: Tripod Adapter Dimensional Diagram

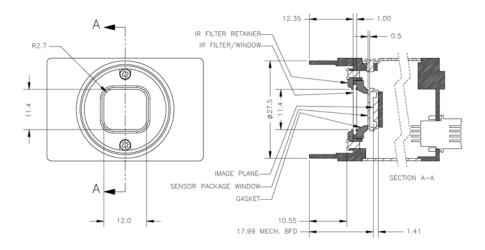
# 1.3.4 Lens Mounting

Lenses are not included with individual cameras.

### **Related Knowledge Base Articles**

Title	Article	
Selecting a lens for your camera	Knowledge Base Article 345	

The lens mount is compatible with C-mount lenses. Correct focus cannot be achieved using a CS-mount lens on a C-mount camera.



The FL3-GE-13S2 model is also available with a CS-mount.



### 1.3.4.1 Back Flange Distance

The Back Flange Distance (BFD) is offset due to the presence of both a 1 mm infrared cutoff (IRC) filter and a 0.5 mm sensor package window. These two pieces of glass fit between the lens and the sensor image plane. The IRC filter is installed on color cameras. In monochrome cameras, it is a transparent piece of glass. The sensor package window is installed by the sensor manufacturer. Both components cause refraction, which requires some offset in flange back distance to correct.

The resulting BFD is 17.99 mm.

For more information about the IRC filter, see Infrared Cut-Off Filters on next page.

### 1.3.5 Dust Protection

The camera housing is designed to prevent dust from falling directly onto the sensor's protective glass surface. This is achieved by placing a piece of clear glass (monochrome camera models) or an IR cut-off filter (color models) that sits above the surface of the sensor's glass. A removable plastic retainer keeps this glass/filter system in place. By increasing the distance between the imaging surface and the location of the potential dust particles, the likelihood of interference from the dust (assuming non-collimated light) and the possibility of damage to the sensor during cleaning is reduced.



- Cameras are sealed when they are shipped. To avoid contamination, seals should not be broken until cameras are ready for assembly at customer's site.
- Use caution when removing the protective glass or filter. Damage to any component of the optical path voids the Hardware Warranty.
- Removing the protective glass or filter alters the optical path of the camera, and may result in problems obtaining proper focus with your lens.

### **Related Knowledge Base Articles**

Title	Article
Removing the IR filter from a color camera	Knowledge Base Article 215
Selecting a lens for your camera	Knowledge Base Article 345

## 1.3.6 Mounting with the Case or Mounting Bracket

#### **Using the Case**

The case is equipped with the following mounting holes:

- Two (2) M2 x 2mm mounting holes on the top of the case
- Three (3) M3 x 2.5mm mounting holes on the bottom of the case
- Four (4) M2 x 2mm mounting holes on the bottom of the case that can be used to attach the camera directly to a custom mount or to the tripod mounting bracket

#### **Using the Mounting Bracket**

The tripod mounting bracket is equipped with two (2) M3 and one (1) M2 mounting holes.



### 1.3.7 Infrared Cut-Off Filters

Point Grey color camera models are equipped with an additional infrared (IR) cut-off filter. This filter can reduce sensitivity in the near infrared spectrum and help prevent smearing. The properties of this filter are illustrated in the results below.

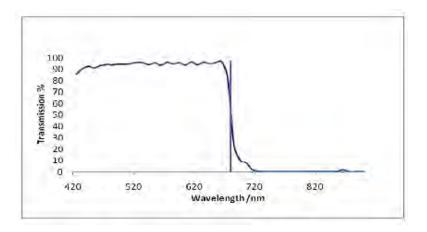


Figure 1.21: IR filter transmittance graph

In monochrome models, the IR filter is replaced with a transparent piece of glass.

The following are the properties of the IR filter/protective glass:

Туре	Reflective
Material	Schott D 263 T
Physical Filter Size	14 mm x 14 mm
Glass Thickness	1.0 mm
<b>Dimensional Tolerance</b>	+/-0.1 mm
Coating Filters	Scott D 263 T

For more information, see Dust Protection on previous page.

### **Related Knowledge Base Articles**

Title	Article	
Removing the IR filter from a color camera	Knowledge Base Article 215	

# 1.4 Handling Precautions and Camera Care



Do not open the camera housing. Doing so voids the Hardware Warranty described at the beginning of this manual.



Your Point Grey digital camera is a precisely manufactured device and should be handled with care. Here are some tips on how to care for the device.

- Avoid electrostatic charging.
- When handling the camera unit, avoid touching the lenses. Fingerprints will affect the quality of the image produced by the device.
- To clean the lenses, use a standard camera lens cleaning kit or a clean dry cotton cloth. Do not apply excessive force.
- Extended exposure to bright sunlight, rain, dusty environments, etc. may cause problems with the electronics and the optics of the system.
- Avoid excessive shaking, dropping or any kind of mishandling of the device.

### **Related Knowledge Base Articles**

Title	Article
Solving problems with static electricity	Knowledge Base Article 42
Cleaning the imaging surface of your camera	Knowledge Base Article 66

### 1.4.1 Case Temperature and Heat Dissipation

You must provide sufficient heat dissipation to control the internal operating temperature of the camera.

The camera is equipped with an on-board temperature sensor. It allows you to obtain the temperature of the camera board-level components. The sensor measures the ambient temperature within the case. This value can be accessed using the Device Temperature GenlCam feature.

**Table 1.1: Temperature Sensor Specifications** 

Accuracy	0.5°C
Range	-25°C to +85°C
Resolution	12 bits



As a result of packing the camera electronics into a small space, the outer case of the camera can become very warm to the touch when running in some high data rate video modes. This is expected behavior and will not damage the camera electronics.

To reduce heat, use a cooling fan to set up a positive air flow around the camera, taking into consideration the following precautions:

- Mount the camera on a heat sink, such as a camera mounting bracket, made out of a heat-conductive material like aluminum.
- Make sure the flow of heat from the camera case to the bracket is not blocked by a non-conductive material like plastic.
- Make sure the camera has enough open space around it to facilitate the free flow of air.



# 1.5 Camera Interface and Connectors

### 1.5.1 Ethernet Connector

The 8-pin RJ-45 Ethernet jack is equipped with two (2) M2 screwholes for secure connection. Pin assignments conform to the Ethernet standard. For information about the orange and green status LEDs on each side of the connector, see Status Indicator LED on page 95.

### 1.5.2 Interface Cables

Category 5e or 6 cables up to 100 meters in length should be used for connecting the camera to the network interface card on the host system. Point Grey sells a 5-meter Category 5e cable for this purpose.

To purchase a recommended cable from Point Grey, visit the Point Grey Webstore or the Products Accessories page.

### 1.5.3 Interface Card

The camera must connect to an interface card. This is sometimes called a host adapter, a bus controller, or a network interface card (NIC).

A 1000 BASE-T NIC is recommended for streaming images on the Ethernet network between the camera and host system.)



For optimal video streaming and camera control performance, we recommend an Intel Pro chipset on a PCIe interface.

To purchase a compatible card from Point Grey, visit the Point Grey Webstore or the Products Accessories page.

# 1.5.4 General Purpose Input/Output (GPIO)

The camera has an 8-pin GPIO connector on the back of the case; refer to the diagram below for wire color-coding. The connector is a Hirose HR25 8 pin connector (Mfg P/N: HR25-7TR-8SA). Male connectors (Mfg P/N: HR25-7TP-8P) can be purchased from Digikey (P/N: HR702-ND).

Diagram	Pin	Function	Description
	1	10	Opto-isolated input (default Trigger in)
	2	01	Opto-isolated output
	3	102	Input/Output/serial transmit (TX)
2 3 4	4	103	Input/Output/serial receive (RX)
(S 6 0)	5	GND	Ground for bi-directional IO, V <sub>EXT</sub> , +3.3 V pins
8	6	OPTO_GND	Ground for opto-isolated IO pins
	7	V <sub>EXT</sub>	Allows the camera to be powered externally
	8	+3.3 V	Power external circuitry up to 150 mA



Point Grey sells a 12 V wall-mount power supply equipped with a HR25 8-pin GPIO wiring harness for connecting to the camera (**Part No. ACC-01-9006**). For more information, see the <u>miscellaneous product accessories page</u> on the Point Grey website.

For more information on camera power, see Powering the Camera on page 40

For more information on configuring input/output with GPIO, see Input/Output Control on page 44.

For details on GPIO circuits, see GPIO Electrical Characteristics on page 48.



# 2 Getting Started with Flea3 GigE

### 2.1 Before You Install

# 2.1.1 Will your system configuration support the camera?

**Recommended System Configuration** 

Operating System	CPU	RAM	Video	Ports	Software
Windows 7, Linux Ubuntu	Intel Core 2 Dual	2 GB	PCI Express 128 MB	GigE	Microsoft Visual Studio 2005 SP1 and SP1 Update for Vista (to compile and run example code)

### 2.1.2 Do you have all the parts you need?

To install your camera you will need the following components:

- Interface card (on page 28)
- Ethernet cable (on page 28)
- 8-pin GPIO connector (on page 44)
- C-mount Lens (on page 24)

Point Grey sells a number of the additional parts required for installation. To purchase, visit the <u>Point Grey Webstore</u> or the <u>Products Accessories</u> page.

# 2.1.3 Do you have a downloads account?

The Point Grey downloads page has many resources to help you operate your camera effectively, including:

- Software (required for installation)
- Drivers (required for installation)
- Firmware updates and release notes
- Dimensional drawings and CAD models
- Documentation

To access the downloads resources you must have a downloads account.

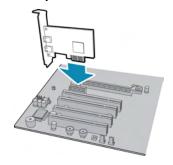
- 1. Go to the Point Grey downloads page.
- 2. Under Register (New Users), complete the form, then click Submit.

After you submit your registration, you will receive an email with instructions on how to activate your account.



# 2.2 Installing Your Interface Card and Software

#### 1. Install your Interface Card



Ensure the card is installed per the manufacturer's instructions.

Alternatively, use your PC's built-in host controller, if equipped.

Open the Windows Device Manager. Ensure the card is properly installed under **Network Adaptors**. An exclamation point (!) next to the card indicates the driver has not yet been installed.

#### 2. Install the FlyCapture® Software



For existing users who already have FlyCapture installed, we recommend ensuring you have the latest version for optimal performance of your camera. If you do not need to install FlyCapture, use the DriverControlGUI to install and enable drivers for your card.

- a. Login to the Point Grey downloads page.
- b. Select your Camera and Operating System from the drop-down lists and click the Search button.
- c. Click on the **Software** search results to expand the list.
- d. Under FlyCapture v2x, click the appropriate link to begin the download and installation.

After the download is complete, the FlyCapture setup wizard begins. If the wizard does not start automatically, double-click the .exe file to open it. Follow the steps in each setup dialog.

#### 3. Enable the Drivers for the card

During the FlyCapture installation, you are prompted to select your interface driver.

In the Interface Driver Selection dialog, select the I will use GigE cameras.

This selection ensures the Point Grey Image Filter driver is installed and enabled. The Image Filter Driver operates as a network service between GigE Vision cameras and the Microsoft built-in UDP stack to filter out GigE Vision stream protocol (GVSP) packets. Use of the filter driver is recommended, as it can reduce CPU load and improve image streaming performance.

Alternatively, Point Grey GigE Vision cameras can communicate directly with the Microsoft UDP stack.



GigE Vision cameras on Linux systems use native Ubuntu drivers.

To uninstall or reconfigure the driver at any time after setup is complete, use the DriverControlGUI (page 34).



#### 4. Configure IP Settings

After installation is complete, the Point Grey GigE Configurator opens. This tool allows you to configure the IP settings of the camera and network card.

If the GigE Configurator does not open automatically, open the tool from **Start>Point Grey Research>FlyCapture2>Utilities>GigE Configurator**. If prompted to enable GigE enumeration, select **Yes**.

- a. In the **left pane**, select the Local Area Connection corresponding to the network interface card (NIC) to which the camera is connected.
- b. In the **right pane**, review maximum transmission unit (MTU). If not 9000, enable jumbo frames on the NIC by clicking **Open Network Connections**. (While most NICs support 9000-byte jumbo frames, this feature is often disabled by default.)

# 2.3 Installing Your Camera

#### 1. Install the Tripod Mounting Bracket



The ASA and ISO-compliant tripod mounting bracket attaches to the camera using the included metal screws.

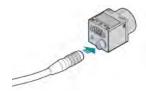


Cameras with metal cases should use metal screws; cameras with plastic cases should use plastic screws. Using improper screws may cause damage to the camera.

#### 2. Attach a Lens

Unscrew the dust cap from the C-mount lens holder to install a lens.

### 3. Plug in the GPIO connector



GPIO is used for power, trigger, pulse width modulation, serial input output, and strobe.

The wiring harness must be compatible with a Hirose HR25 8-pin female GPIO connector.

#### 4. Connect the interface Card and Cable to the Camera



Plug the interface cable into the host controller card and the camera. The cable jack screws can be used for a secure connection.

#### 5. Configure IP Settings

In the GigE Configurator:

a. In the **left pane**, select your GigE Vision camera. (Note: there may be a delay of several seconds before the camera is detected by the GigE Configurator on startup.)



- Under "Current IP Configuration," review the IP address. By default, a dynamic IP address is assigned to the camera according to the DHCP protocol. If DHCP addressing fails, a link-local address is assigned. If necessary, change the IP address of the camera to be on the same subnet as the NIC. If the subnets do not match, the camera is marked "BAD" on the left pane.
- Under "Packet Size Discover," click **Discover Maximum Packet Size** and note the value.
- b. Close the GigE Configurator.

#### 6. Confirm Successful Installation and Configure Packet Size

- a. Run the FlyCap2 program: Start-> Point Grey Research->FlyCapture2-> FlyCap2
- b. In the camera selection dialog, select the GigE camera that was installed and click Configure Selected.
- c. In the Camera Control dialog, click Custom Video Modes. By default, Packet Size is set to 1400 bytes. We recommend increasing this value to the size noted in the GigE Configurator, as maximizing packet size reduces processing overhead.

The FlyCap2 program can be used to test the camera's image acquisition capabilities through the Ethernet connection.

Changes to your camera's installation configuration can be made using utilities available in the FlyCapture2 SDK (see Configuring Camera Setup on next page).

# 2.4 Controlling the Camera

The camera's features can be accessed using various controls, including:

- FlyCapture2 SDK including API examples and the FlyCap program
- GenICam Applications

Examples of the controls are provided throughout this document. Additional information can be found in the appendices.

# 2.4.1 Using FlyCapture

The user can monitor or control features of the camera through FlyCapture API examples provided in the FlyCapture SDK, or through the FlyCap2 Program.

### FlyCap2 Program

The FlyCap2 application is a generic, easy-to-use streaming image viewer included with the FlyCapture2 SDK that can be used to test many of the capabilities of your compatible Point Grey camera. It allows you to view a live video stream from the camera, save individual images, adjust the various video formats, frame rates, properties and settings of the camera, and access camera registers directly. Consult the FlyCapture SDK Help for more information.

### **Custom Applications Built with the FlyCapture API**

The FlyCapture SDK includes a full Application Programming Interface that allows customers to create custom applications to control Point Grey Imaging Products. Included with the SDK are a number of source code examples to



help programmers get started.

FlyCapture API examples are provided for C, C++, C#, and VB.NET languages. There are also a number of precompiled examples.

### 2.4.2 GenlCam Applications

The camera includes an XML device description file for interfacing with third-party GenlCam-compliant APIs. This file can be accessed via First URL bootstrap register 200h (page 108). A full listing of features that are included in the XML file is provided in GenlCam Features on page 99.

Not all operations can be controlled using the XML file; those not included are controlled via Control and Status Registers (CSRs). These registers conform to the IIDC v1.32 standard. A full listing of CSRs is provided in the Appendix Control and Status Registers on page 110.

Throughout this document, GenlCam features are referenced with their applicable operation; where no GenlCam feature is available in the XML file, the CSR is referenced.

### 2.4.3 GigE Vision Bootstrap Registers

The camera is programmed with a number of GigE Vision-compliant bootstrap registers for storing camera metadata and controlling network management settings. For a listing of all GigE Vision bootstrap registers on the camera, see GigE Vision Bootstrap Registers on page 108.

# 2.5 Configuring Camera Setup

After successful installation of your camera and interface card, you can make changes to the setup. Use the tools described below to change the IP Address or the driver for your interface card.

For information on updating your camera's firmware post installation, see Camera Firmware on page 43.

# 2.5.1 Configuring Camera Drivers

Point Grey provides the Image Filter Driver for use with GigE Vision cameras. This driver operates as a network service between the camera and the Microsoft built-in UDP stack to filter out GigE vision stream protocol (GVSP) packets. The filter driver is installed and enabled by default as part of the FlyCapture SDK installation process. Use of the filter driver is recommended, as it can reduce CPU load and improve image streaming performance.

Alternatively, Point Grey GigE Vision cameras can operate without the filter driver by communicating directly with the Microsoft UDP stack.



GigE Vision cameras on Linux systems use native Ubuntu drivers.

For more information about the image filter driver, see the FlyCapture SDK Help.



To manage and update drivers use the DriverControlGUI utility provided in the FlyCapture SDK. To open the DriverControlGUI:

### Start Menu-->Programs-->Point Grey Research-->FlyCapture2-->Utilities-->DriverControlGUI

Select the interface from the tabs in the top left. Then select your interface card to see the current setup.

For more information about using the DriverControlGUI, see the online help provided in the tool.

### 2.5.2 Configuring the IP Address

When a new camera is first powered and initialized, a dynamic IP address is assigned to the camera according to the DHCP protocol. If DHCP addressing fails, a link-local address is assigned. You can re-configure the IP address for using the GigE Vision bootstrap registers (page 108) or the GenICam features (page 99).

Alternatively, the Point Grey GigE Configurator is a tool included with the camera software and drivers package that allows you to set the internet protocol (IP) configuration for any GigE interface cards or Point Grey GigE Vision cameras connected to your system. Using the GigE Configurator, you can:

- Set the IP address for the current connection.
- Program a persistent IP address for the camera.
- Configure the default IP addressing behavior of the camera on startup using a persistent IP, DHCP or LLA.
- Enable Jumbo Frames on the GigE NIC.

Both your camera and host adapter must have an IP address on the same subnet. This can be assigned in three ways:

- **Persistent**—Both the adapter and the camera have a fixed IP address that will not change. Generally the address is within a closed network range of 192.168.X.X. The adapter and the camera must be on the same subnet.
- **Dynamic (DHCP)**—Both the camera and the adapter are set to automatically obtain an IP address. This means that the IP address will dynamically change (within a range) every time the camera or computer is restarted. It may take up to one minute for the IP address to resolve and the camera to enumerate.
- **Default (LLA)**—Both the camera and the adapter use a default IP address from the link-local address block 169.254.x.x.

The camera assigns its current IP address in the following sequence:

- 1. **Persistent**—Uses the defined IP address. If not available, then;
- 2. **DHCP**—Attempts to find a dynamic IP address. If not available, then;
- 3. LLA—Uses the default IP address.

The GigE Configurator can automatically force an IP address refresh. This detects the IP address of the Network Interface card and automatically sets the camera's IP address relative to the card.

The FlyCap2 program can be used to test your camera settings and verify operation. From the camera selection window, you can also automatically force an IP address refresh.

To open the Point Grey GigE Configurator:

Start > Point Grey Research > FlyCapture2 > Utilities > GigEConfigurator



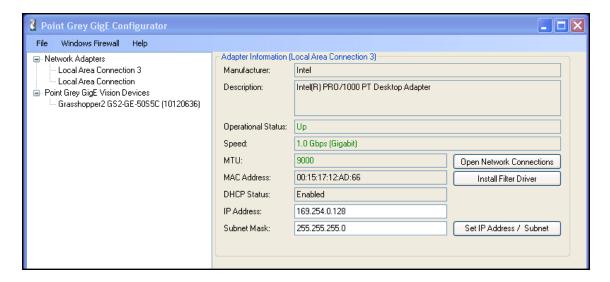


Figure 2.1: Point Grey GigE Configurator

For more information, refer to the online Help file included with the tool.

### 2.5.3 Allocating Bandwidth

The User Datagram Protocol (UDP) used by the GigE Vision standard provides no guaranteed transmission or fixed timing mechanism. Therefore, bandwidth must be managed by adjusting packet size and packet delay, based on desired resolution and frame rate.

### 2.5.3.1 Packet Size

The stream channel packet size (SCPS) sets the size, in bytes, of the packet to be sent out by the camera. IP, UDP and GVSP headers are included in this size. The default packet size is 1400 bytes.

Packet size influences the number of interrupts generated which affects CPU usage. The larger the packet size, the fewer the interrupts for the same amount of data. To minimize CPU usage, increase the packet size.

The upper limit depends on your host adapter, your Ethernet switches (if used), and the camera.



From the GigE Configurator with your camera selected, click Discover Maximum Packet Size. This will test the network to see the maximum size that can be sent and received through all your network components. Set your camera's and host adaptor's packet size to be less than or equal to this maximum.

### To adjust the packet size:

From the GigE Configurator with your adapter selected, click Open Network Connections to open the Windows Adapter Properties. Adjust the packet size of your host adapter to ~9000 (the standard jumbo packet size). If your adapter does not support such a large packet (or MTU) size, then you will experience slightly higher CPU usage.

Packet size for the camera can be adjusted using the FlyCap2 demo program, the GevSCPSPacketSize GenlCam feature, or the GigE Vision Bootstrap registers (page 108). The FlyCapture SDK also supports configuring the SCPS. For more information, consult the FlyCapture SDK Help.



Changing the packet size may impact throughput depending on the packet delay setting.

### 2.5.3.2 Packet Delay

The stream channel packet delay (SCPD) indicates the number of ticks (at the frequency of the Timestamp Tick Frequency) to insert between each packet. The default packet delay is 400.

The Point Grey Timestamp Tick Frequency is normally 125,000,000 ticks/second, but can be verified by the the GevTimestampTickFrequency GenlCam feature, or the Timestamp Tick Frequency Bootstrap register (page 108).

The packet delay acts like a gap between packets during transmission. This delay allows the host to process the current packet before the arrival of the next one. When you increase the packet delay value from zero, you reduce the effective bandwidth assigned to the camera and thereby also reduce the possibility of dropped frames.



Increasing the packet delay is recommended when running multiple cameras through an Ethernet switch.

Increasing the packet delay may require the frame rate to be reduced to meet the available maximum bandwidth. Achieving a desired frame rate may require decreasing the packet delay.

#### To adjust the packet delay:

Packet delay for the camera can be adjusted using the FlyCap2 demo program, the GevSCPD GenlCam feature (page 99), or the GigE Vision bootstrap registers (page 108). The FlyCapture SDK also supports configuring the SCPD. For more information, consult the FlyCapture SDK Help.

### 2.5.3.3 Determining Bandwidth Requirements

The maximum bandwidth available is 125 MB. This includes image data, control data and image resends, which occur when frames are being dropped. Each image and each packet has a certain amount of overhead that will use some bandwidth. Therefore, when calculating your bandwidth requirements, you should not attempt to use the full maximum of 125 MB.



If the packet size and packet delay combination exceeds the available bandwidth, frames will be dropped.

### To calculate your bandwidth requirements:

Determine your required resolution, frame rate, and pixel format (bytes per pixel)

(Height x Width x Frame Rate x Bytes per Pixel)/1000000 = Bandwidth in MB

For example, for an image that is VGA, 82 FPS, Mono8:

640 (H) x 480 (W) x 82 (FPS) x 1 (BPP) = 
$$^2$$
5 MB

Once you have calculated your required bandwidth, you can allocate an amount to each camera by adjusting the packet size and packet delay. Allocating a specific amount to each camera helps to avoid dropped packets due to a



data burst. You would do this in a set up with multiple cameras, or in a situation where the system bandwidth might be limited or shared due to hardware architecture.

Here are some packet size/packet delay combinations you can use with any image size, pixel format combination. Frame rate will be limited depending on total bandwidth.

To allocate 25 MB ~20% of bandwidth	To allocate 55 MB ~45% of bandwidth
Packet Size = 9000	Packet Size = 9000
Packet Delay = 5900	Packet Delay = 1800
Packet Size = 1400	Packet Size = 1400
Packet Delay = 900	Packet Delay = 255

### **Bandwidth Requirements for Multiple Cameras**

Multiple cameras can be set up in two ways: 1) Each camera is connected directly to a single Ethernet port; or, 2) multiple cameras are connected to a single port through an Ethernet switch.

If using the first method, each camera has the full bandwidth allocation available to it. If using the second method, the combination of all cameras on a switch cannot exceed the available bandwidth.

### **Related Knowledge Base Articles**

Title	Article
Setting Up Multiple GigE Cameras	Knowledge Base Article 390

## 2.5.4 Configuring Other Network Settings

The following GigE Vision bootstrap registers can be used for configuring the camera on the network. All registers are implemented according to the GigE Vision standard. A listing of all network-related bootstrap registers supported on the camera is provided in GigE Vision Bootstrap Registers on page 108.

### 2.5.4.1 Stream Channel Destination Address

The stream channel destination address (SCDA) register is used to specify the streaming destination IP address. The default SCDA is the IP address of the network or computer to which the camera is connected. It can be set within a range so that the camera sends data as a multicast. As long as switches in the path between the sender and receivers support and are configured for multicasting, multiple receivers can listen to the data stream from the camera.

Multicast addresses are between 224.0.0.0 and 239.255.255.255.



For more information on multicast address assignments, see <a href="http://tools.ietf.org/html/rfc3171">http://tools.ietf.org/html/rfc3171</a>,

SCDA can be controlled using the GevSCDA GenlCam feature (page 99) or the GigE Vision bootstrap registers (page 108).



#### 2.5.4.2 Heartbeat

The heartbeat is a mandatory GigE Vision feature to monitor the connection between an application and the camera. The application must continually reset the heartbeat timer, or the camera will assume an error has occurred and shut down the connection.

In general, the FlyCapture API manages the heartbeat at a low level; however the following two features are controllable: Heartbeat Timeout and Heartbeat Disable.

#### **Heartbeat Timeout**

Heartbeat timeout is the time, in milliseconds, that the camera will wait between resets from the application. Heartbeat timeout can be set between 500 ms and 10 seconds. The default setting is 3000 ms (3 seconds). If there is no communication between the camera and the application for longer than the timeout value, the connection is shut down.

Heartbeat timeout can be controlled using the GevHeartbeatTimeout GenlCam feature (page 99) or the GigE Vision bootstrap registers (page 108). The FlyCapture SDK also supports configuring heartbeat timeout. For more information, consult the FlyCapture SDK Help.

#### **Heartbeat Disable**

The heartbeat is enabled by default. Heartbeat disable allows the heartbeat function in the camera to be disabled.

The heartbeat can be disabled using the GevGVCPHeartbeatDisable GenICam feature (page 99) or the GigE Vision bootstrap registers (page 108). The FlyCapture SDK also supports configuring the heartbeat. For more information, consult the FlyCapture SDK Help.



# 3 General Camera Operation

# 3.1 Powering the Camera

The power consumption specification is: 12-24 V, <2.5 W, via GPIO.

Power must be provided through the GPIO interface. For more information, see General Purpose Input/Output (GPIO) on page 44. The required input voltage is 12 - 24 V DC.

Point Grey sells a 12 V wall-mount power supply equipped with a HR25 8-pin GPIO wiring harness for connecting to the camera (**Part No. ACC-01-9006**). For more information, see the <u>miscellaneous product accessories page</u> on the Point Grey website.

The camera does not transmit images for the first 100 ms after power-up. The auto-exposure and auto-white balance algorithms do not run while the camera is powered down. It may therefore take several (n) images to get a satisfactory image, where n is undefined.

When the camera is power cycled (power disengaged then re-engaged), the camera will revert to its default factory settings, or if applicable, the last saved memory channel. For more information, see User Sets on next page.

# 3.2 GenlCam Device Control

Information about the camera is available with the following GenlCam features:

Name	Display Name	Description	Value
DeviceVendorName	Vendor Name	Name of the manufacturer	Point Grey Research
DeviceModelName	Model Name	Model name of the device	Flea3 GigE <model number=""></model>
DeviceVersion	Device Version	FPGA version	
DeviceFirmwareVersion	Device Firmware Version	Firmware version	
DeviceID	Device ID	Camera Serial Number	
DeviceScanType	Device Scan Type	Scan type of the sensor	Areascan (2D sensor)
DeviceTemperature	Device Temperature (C)	Device temperature in degrees Celsius	
DeviceReset	Device Reset	Resets the device to its initial state and default settings	Write Only
DeviceUserID	Device User ID	User defined name	
DeviceMaxThroughput	Device Max Throughput	Indicates maximum data in bytes from the camera each second	

There are also control and status registers available to monitor the camera. For more information, see Device Information CSRs on page 130.



# 3.3 User Sets

The camera can save and restore settings and imaging parameters via on-board configuration sets, also known as memory channels. This is useful for saving default power-up settings, such as gain, shutter, video format and frame rate, and others that are different from the factory defaults.

User Set 0 stores the factory default settings that can always be restored. Two additional user sets are provided for custom default settings. The camera will initialize itself at power-up, or when explicitly reinitialized, using the contents of the last saved user set. Attempting to save user settings to the (read-only) factory defaults user set will cause the camera to switch back to using the factory defaults during initialization.

The following camera settings are saved in user sets.

Acquisition Frame Rate (page 78)	Image Data Format
Current Frame Rate (page 53)	Image Position and Image Size (page 66)
Current Video Mode and Format (page 66)	Frame Information (page 93)
Camera Power (page 40)	Trigger Mode and Trigger Delay (page 78)
Brightness (page 82)	Hue (page 84)
Auto Exposure (page 91)	Saturation (page 83)
Sharpness (page 84)	Shutter (including Auto Shutter Range, and Shutter Delay) (page 88)
White Balance (page 87)	Gain (including Auto Gain Range) (page 82)
Gamma (page 85)	GPIO Pin Modes (page 45)
GPIO PWM Modes (page 47)	GPIO Strobe Modes (page 46)
Pixel Coding (page 66)	Stream Channel Packet Size (page 36)
GVCP Configuration (includes Heartbeat Disable)	Stream Channel Packet Delay (page 37)
Heartbeat Timeout (page 39)	Auto Iris

### 3.3.1 GenlCam User Set Control

Name	Display Name	Description	Value
CurrentUserSet	Current User Set	Indicates the user set that is currently in use. At initialization time, the camera loads the most recently saved user set	0 (default) 1 2
UserSetSelector	User Set Selector	Selects the user set to load or save	Default User Set 1 User Set 2
UserSetLoad	User Set Load	Loads the user set specified by the User Set Selector to the device and makes it active	Write Only
UserSetSave	User Set Save	Saves the user set specified by the User Set Selector to the non-volatile memory of the device	Write Only
DefaultUserSet	Default User Set	Selects the default user set as the default start up set	Default User Set 1 User Set 2



# 3.4 On-Camera Frame Buffer

The camera has 32 MB of memory that can be used for temporary image storage. This may be useful in cases such as:

- Retransmission of an image is required due to data loss or corruption.
- Multiple camera systems where there is insufficient bandwidth to capture images in the desired configuration.

All images pass through the frame buffer mechanism. This introduces relatively little delay in the system because the camera does not wait for a full image to arrive in the buffer before starting transmission but rather lags only a few lines behind.

The user can cause images to accumulate by enabling the frame buffer. This effectively disables the transmission of images in favor of accumulating them in the frame buffer. The user is then required to use the remaining elements of the interface to cause the transmission of the images.

The buffer system is circular in nature, storing only the last 32 MB worth of image data. The number of images that this accommodates depends on the currently configured image size.

The standard user interaction involves the following steps:

#### 1. Configure the imaging mode.

This first step involves configuring the format, mode and frame rate for acquiring images. This can be done by either directly manipulating the registers or using the higher level functionality associated with the software library being used. Depending on the software package, this may involve going so far as to configure the camera, perform bandwidth negotiation and grab an image. In cases where bandwidth is restricted, the user will want to disable transmission and free the bandwidth after the camera is configured.

#### 2. Enable frame buffer accumulation

The second step involves enabling the frame buffer. Enabling this results in images being accumulated in the frame buffer rather than immediately being transmitted.

#### 3. Negotiate bandwidth with the camera

Having accumulated some number of images on the camera, bandwidth will have to be renegotiated if it has not been done already. In most cases, this will involve effectively starting the camera in the imaging mode configured in step (1).

### 4. Disable isochronous transmission and enable buffered image transfer

To transfer buffered images, isochronous data transmission must be disabled, and transfer data enabled.

### 5. Transmit images off of the camera

The final step involves setting One Shot/Multi-shot in order to cause the camera to transmit one or more images from the frame buffer over the data interface.

Although it is possible to repeatedly transmit the same image, there is no way to access images that are older than the last image transmitted.

Whether by enabling trigger or disabling isochronous data, switching out of a free running mode leaves the last image transmitted in an undefined state.

The frame buffer is volatile memory that is erased after power cycling. To store images on the camera after power cycling, use Non-Volatile Flash Memory on next page. Accessing flash memory is significantly slower than accessing the frame buffer, and storage is limited.

For information on controlling the frame buffer register, see IMAGE\_RETRANSMIT: 634h on page 133



# 3.5 Non-Volatile Flash Memory

The camera has 1 MB of non-volatile memory for users to store data.

### **Related Knowledge Base Articles**

Title	Article	
Storing data in on-camera flash memory	Knowledge Base Article 341	

For information on using the flash memory register, see DATA\_FLASH\_CTRL: 1240h on page 132

### 3.6 Camera Firmware

Firmware is programming that is inserted into the programmable read-only memory (programmable ROM) of most Point Grey cameras. Firmware is created and tested like software. When ready, it can be distributed like other software and installed in the programmable read-only memory by the user.

The latest firmware versions often include significant bug fixes and feature enhancements. To determine the changes made in a specific firmware version, consult the Release Notes.

Firmware is identified by a version number, a build date, and a description.

### **Related Knowledge Base Articles**

Title	Article
PGR software and firmware version numbering scheme/standards	Knowledge Base Article 96
Determining the firmware version used by a PGR camera	Knowledge Base Article 94
Should I upgrade my camera firmware or software?	Knowledge Base Article 225

# 3.6.1 Determining Firmware Version

To determine the firmware version number of your camera:

- In FlyCapture, open the Camera Control dialog and click on Camera Information.
- If you're implementing your own code, use flycaptureGetCameraRegister().
- Query the GenlCam feature DeviceFirmwareVersion.

## 3.6.2 Upgrading Camera Firmware

Camera firmware can be upgraded or downgraded to later or earlier versions using the UpdatorGUI program that is bundled with FlyCapture2 available from the Point Grey downloads site.

Before upgrading firmware:

- Install the FlyCapture 2 SDK, downloadable from the Point Grey downloads site.
- Ensure that FlyCapture2.dll is installed in the same directory as UpdatorGUI3.
- Download the firmware file from the <u>Point Grey downloads site</u>.



# 4 Input/Output Control

# 4.1 General Purpose Input/Output (GPIO)

The camera has an 8-pin GPIO connector on the back of the case; refer to the diagram below for wire color-coding. The connector is a Hirose HR25 8 pin connector (Mfg P/N: HR25-7TR-8SA). Male connectors (Mfg P/N: HR25-7TP-8P) can be purchased from Digikey (P/N: HR702-ND).

**Diagram** Pin **Function Description** 1 10 Opto-isolated input (default Trigger in) 2 01 Opto-isolated output 3 102 Input/Output/serial transmit (TX) 4 Input/Output/serial receive (RX) 103 Ground for bi-directional IO,  $V_{EXT}$ , +3.3 V pins 5 GND OPTO GND 6 Ground for opto-isolated IO pins 7 Allows the camera to be powered externally 8 Power external circuitry up to 150 mA +3.3 V

Table 4.1: GPIO pin assignments (as shown looking at rear of camera)

Power must be provided through the GPIO interface. The required input voltage is 12 - 24 V DC.

Point Grey sells a 12 V wall-mount power supply equipped with a HR25 8-pin GPIO wiring harness for connecting to the camera (**Part No. ACC-01-9006**). For more information, see the <u>miscellaneous product accessories page</u> on the Point Grey website.

For details on GPIO circuits, see GPIO Electrical Characteristics on page 48.

# 4.2 **GPIO Modes**

# 4.2.1 GPIO Mode 0: Input

When a GPIO pin is put into GPIO Mode 0 it is configured to accept external trigger signals. See Serial Communication on page 47.

# 4.2.2 GPIO Mode 1: Output

When a GPIO pin is put into GPIO Mode 1 it is configured to send output signals.



Do **not** connect power to a pin configured as an output (effectively connecting two outputs to each other). Doing so can cause damage to camera electronics.



# 4.2.3 GPIO Mode 2: Asynchronous (External) Trigger

When a GPIO pin is put into GPIO Mode 2, and an external trigger mode is enabled (which disables isochronous data transmission), the camera can be asynchronously triggered to grab an image by sending a voltage transition to the pin. See Asynchronous Triggering on page 68.

### 4.2.4 GPIO Mode 3: Strobe

A GPIO pin in GPIO Mode 3 will output a voltage pulse of fixed delay, either relative to the start of integration (default) or relative to the time of an asynchronous trigger. A GPIO pin in this mode can be configured to output a variable strobe pattern. See Programmable Strobe Output on next page.

# 4.2.5 GPIO Mode 4: Pulse Width Modulation (PWM)

When a GPIO pin is set to GPIO Mode 4, the pin will output a specified number of pulses with programmable high and low duration. See Pulse Width Modulation (PWM) on page 47.

# 4.3 GenICam Digital Input/Output Control

Name	Display Name	Description	Value
LineSelector	+ Line Selector	Selects the physical line (or GPIO pin) of the external device connector to configure.	Line 0 Line 1 Line 2 Line 3
LineMode	Line Mode	Controls whether the physical line is used to Input or Output a signal. Choices are dependent on which line is selected.	Input Trigger Strobe Output
LineSource	Line Source	Selects which input or output signal to output on the selected line. Line Mode must be Output.	Exposure Active External Trigger Active
LineInverter	Line Inverter	Controls the invertion of the signal of the selected input or output line	True False
StrobeEnabled	Strobe Enabled	Enables/disables strobe	True False
UserOutputValue	User Output Value	Sets the value of the user output selector	True = High False = Low
LineStatus	Line Status	Returns the current status of the selected input or output line	True = High False = Low
LineStatusAll	Line Status All	Returns the current status of all available line signals at time of polling in a single bitfield	



# 4.4 Programmable Strobe Output

The camera is capable of outputting a strobe pulse off select GPIO pins that are configured as outputs. The start of the strobe can be offset from either the start of exposure (free-running mode) or time of incoming trigger (external trigger mode). By default, a pin that is configured as a strobe output will output a pulse each time the camera begins integration of an image.

The duration of the strobe can also be controlled. Setting a strobe duration value of zero produces a strobe pulse with duration equal to the exposure (shutter) time.

Multiple GPIO pins, configured as outputs, can strobe simultaneously.

Connecting two strobe pins directly together is not supported. Instead, place a diode on each strobe pin.

The camera can also be configured to output a variable strobe pulse pattern. The strobe pattern functionality allows users to define the frames for which the camera will output a strobe. For example, this is useful in situations where a strobe should only fire:

- Every Nth frame (e.g. odd frames from one camera and even frames from another); or
- N frames in a row out of T (e.g. the last 3 frames in a set of 6); or
- Specific frames within a defined period (e.g. frames 1, 5 and 7 in a set of 8)

### **Related Knowledge Base Articles**

Title	Article
Buffering a GPIO pin strobe output signal using an optocoupler to drive external devices	Knowledge Base Article 200
GPIO strobe signal continues after isochronous image transfer stops	Knowledge Base Article 212
Setting a GPIO pin to output a strobe signal pulse pattern	Knowledge Base Article 207

# 4.4.1 Example: Setting a GPIO Pin to Strobe (Using the FlyCapture API)

The following FlyCapture 2.x code sample uses the C++ interface to do the following:

- Configures GPIO1 as the strobe output pin.
- Enables strobe output.
- Specifies an active high (rising edge) strobe signal.
- Specifies that the strobe signal begin 1 ms after the shutter opens.
- Specifies the duration of the strobe as 1.5 ms.

#### Assuming a Camera object cam:

```
StrobeControl mStrobe;
mStrobe.source = 1;
mStrobe.parameter = 0;
mStrobe.onOff = true;
```



```
mStrobe.polarity = 1;
mStrobe.delay = 1.0f;
mStrobe.duration = 1.5f
cam.SetStrobeControl(&mStrobe);
```

# 4.5 Pulse Width Modulation (PWM)

When a GPIO pin is set to PWM (GPIO Mode 4), the pin will output a specified number of pulses with programmable high and low duration.

The pulse is independent of integration or external trigger. There is only one real PWM signal source (i.e. two or more pins cannot simultaneously output different PWMs), but the pulse can appear on any of the GPIO pins.

The units of time are generally standardized to be in ticks of a 1.024 MHz clock. A separate GPIO pin may be designated as an "enable pin"; the PWM pulses continue only as long as the enable pin is held in a certain state (high or low).



The pin configured to output a PWM signal (PWM pin) remains in the same state at the time the 'enable pin' is disabled. For example, if the PWM is in a high signal state when the 'enable pin' is disabled, the PWM pin remains in a high state. To re-set the pin signal, you must re-configure the PWM pin from GPIO Mode 4 to GPIO Mode 1.

For information on using PWM registers, see GPIO\_CTRL\_PIN: 1110h-1140h on page 135 and GPIO\_XTRA\_PIN: 1114h-1144h on page 136.

# 4.6 Serial Communication

The camera is capable of serial communications at baud rates up to 115.2 Kbps via the on-board serial port built into the camera's GPIO connector. The serial port uses TTL digital logic levels. If RS signal levels are required, a level converter must be used to convert the TTL digital logic levels to RS voltage levels.

### **Related Knowledge Base Articles**

Title	Article	
Configuring and testing the RS-232 serial port	Knowledge Base Article 151	

### **SIO Buffers**

Both the transmit and receive buffers are implemented as circular buffers that may exceed the 255 byte maximum.

- The transmit buffer size is 512 B.
- The receive buffer size is 8 KB.

Block reads and writes are both supported. Neither their length nor their address have to be 32-bit aligned or divisible by 4.



## 4.7 Debouncer

By default, Point Grey cameras will reject a trigger signal that has a pulse width of less than 16 ticks of the pixel clock. With the debouncer the user can define a debounce value. Once the debouncer is enabled and defined, the camera will reject a trigger signal with a pulse width less than the defined debounce value.

It is recommended to set the debounce value slightly higher than longest expected duration of an invalid signal to compensate for the quality of the input clock signal.

The debouncer is available on GPIO input pins. For the debouncer to take effect, the associated GPIO pin must be in Input mode (GPIO Mode 0) (page 135). The debouncer works in all trigger modes, except trigger mode 3 Skip Frames.



Each GPIO has its own input delay time (page 48). The debouncer time adds additional delay to the signal on the pin.

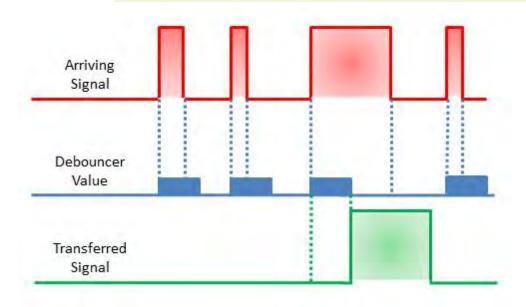


Figure 4.1: Debouncer Filtering Invalid Signals

For information on using the Debouncer registers, see DEBOUNCER\_CTRL on page 143.

# 4.8 GPIO Electrical Characteristics

Opto-isolated **input** pins require an external pull up resistor to allow triggering of the camera by shorting the pin to the corresponding opto ground (OPTO\_GND). Non opto-isolated input pins are internally pulled high using weak pull-up resistors to allow triggering by shorting the pin to GND. Inputs can also be directly driven from a 3.3 V or 5 V logic output.

The inputs are protected from over voltage.



When configured as **outputs**, each line can sink 10 mA of current. To drive external devices that require more, consult <u>Knowledge Base Article 200</u> for information on buffering an output signal using an optocoupler.

The  $V_{EXT}$  pin (Pin 7) allows the camera to be powered externally. The voltage limit is 12-24 V, and current is limited to 1 A.

The **+3.3V** pin is fused at 150 mA. External devices connected to Pin 8 should not attempt to pull anything greater than that.



To avoid damage, connect the OPTO\_GND pin first before applying voltage to the GPIO line.

# 4.8.1 GPIO0 (Opto-Isolated Input) Circuit

The figure below shows the schematic for the opto-isolated input circuit.

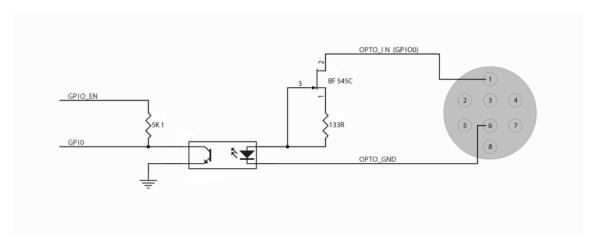


Figure 4.2: Optical input circuit

- Logical 0 input voltage: 0 VDC to +1 VDC (voltage at OPTO IN)
- Logical 1 input voltage: +1.5 VDC to +30 VDC (voltage at OPTO IN)
- Maximum input current: 8.3 mA
- Behavior between 1 VDC and 1.5 VDC is undefined and input voltages between those values should be avoided
- Input delay time: 4 μs

# 4.8.2 GPIO1 (Opto-Isolated Output) Circuit

The figure below shows the schematic for the opto-isolated output circuit. The maximum current allowed through the opto-isolated output circuit is 25 mA.



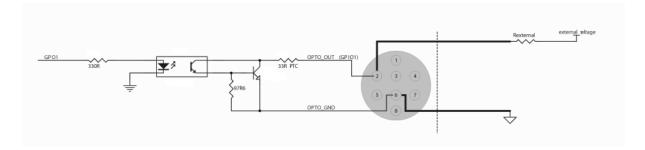


Figure 4.3: Optical output circuit

The following table lists the switching times for the opto-isolator in the output pin, assuming an output VCC of 5 V and a  $1 \text{ k}\Omega$  resistor.

Parameter	Value
Delay Time	9 μs
Rise Time	16.8 μs
Storage Time	0.52 μs
Fall Time	2.92 μs

The following table lists several external voltage and resistor combinations that have been tested to work with the opto-isolated output.

External Voltage	External Resistor	OPTO_OUT Voltage	OPTO_OUT Current
3.3 V	1 kΩ	0.56 V	2.7 mA
5 V	1 kΩ	0.84 V	4.2 mA
12 V	2.4 kΩ	0.91 V	4.6 mA
24 V	4.7 kΩ	1.07 V	5.1 mA



# 4.8.3 GPIO 2/3 (Bi-Directional) Circuit

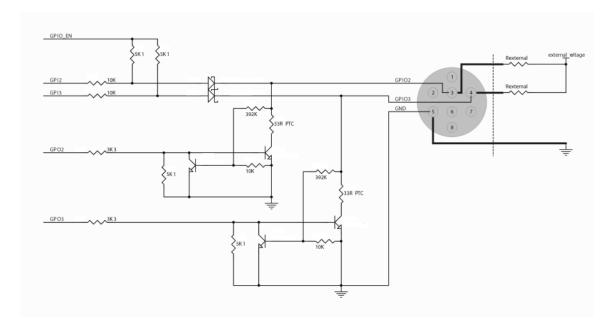


Figure 4.4: GPIO2/3 Circuit

### **Input Side**

- Logical 0 input voltage: 0 VDC to +0.5 VDC (voltage at GPIO2/3)
- Logical 1 input voltage: +1.5 VDC to +30 VDC (voltage at GPIO2/3)
- Behavior between 0.5 VDC and 1.5 VDC is undefined and input voltages between those values should be avoided



To avoid damage, connect the ground (GND) pin first before applying voltage to the GPIO line.

### **Output Side**

The maximum output current allowed through the bi-directional circuit is 25 mA (limit by PTC resistor), and the output impedance is 40  $\Omega$ .

The following table lists several external voltage and resistor combinations that have been tested to work with the bidirectional GPIO when configured as output.

External Voltage	External Resistor (R <sub>external</sub> )	GPIO2/3 Voltage
3.3 V	1 kΩ	0.157 V
5 V	1 kΩ	0.218 V
12 V	1 kΩ	0.46 V
24 V	1 kΩ	0.86 V

The following table lists the switching times for a standard GPIO pin, assuming an output VCC of 5V and a 1 k $\Omega$  resistor.



Parameter	Value
Delay Time	0.28 μs
Rise Time	0.06 μs
Storage Time	0.03 μs
Fall Time	0.016 μs



# 5 Video Formats, Modes and Frame Rates

## 5.1 Video Modes Overview

The camera implements a number of video modes, all of which allow the user to select a specific region of interest (ROI) of the image. Some modes also aggregate pixel values using a process known as "binning". Specifying an ROI may increase frame rate. Modes that perform binning may increase image intensity.

On Point Grey cameras, binning refers to the aggregation of pixels. Analog binning is aggregation that occurs before the analog to digital conversion. Digital binning is aggregation that occurs after the analog to digital conversion. Unless specified otherwise, color data is maintained in binning modes.

The figures below illustrate how binning works. 2x vertical binning aggregates two adjacent vertical pixel values to form a single pixel value. 2x horizontal binning works in the same manner, except two adjacent horizontal pixel values are aggregated.

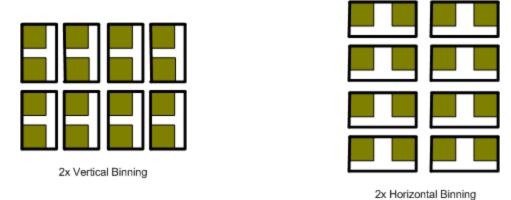


Figure 5.1: 2x Vertical and 2x Horizontal Binning

In most cases, pixels are added once they are binned. Additive binning usually results in increased image intensity. Another method is to average the pixel values after aggregation. Binning plus averaging results in little or no change in the overall image intensity.

Changing the size of the image or the pixel encoding format requires the camera to be stopped and restarted. Ignoring the time required to do this in software (tearing down, then reallocating, image buffers, write times to the camera, etc.), the maximum amount of time required for the stop/start procedure is slightly more than one frame time.

Moving the ROI position to a different location does not require the camera to be stopped (isochronous transmission disabled) and restarted (iso enabled), unless the change is illegal (e.g. moving the ROI outside the imaging area).



Pixel correction (page 96) is not done in any of the binning modes.

### **5.1.1** Video Mode Descriptions

Mode	Models	Description	Frame Rate Increase	Brightness Increase	SNR Improved
0	All	ROI No Binning	Yes	No	No
1	All	2X/2X Additive Binning	No	Yes	Yes
4	All Color Models	2X/2X Subsampling	Yes	No	No
5	FL3-GE-20S4C/M FL3-GE-28S4C/M FL3-GE-50S5C/M	4X/4X Additive Binning	Yes for Mono No for Color	Yes	Yes
6	FL3-GE-20S4C FL3-GE-28S4C FL3-GE-50S5C	4X/4X Binning Mono output	Yes	No	No
7	All	ROI No Binning Slower pixel clock, Extended Shutter	No	No	Yes

#### Mode 0

Mode 0 allows only for specifying a region of interest, and does not perform any binning. This mode uses a faster pixel clock compared to Mode 7, which can result in faster frame rates when ROI height is reduced.

#### Mode 1

Mode 1 implements 2X vertical and 2X horizontal additive binning. On color models, both horizontal and vertical binning are performed as subsampling on the FPGA of the camera. In Mono, YUV and RGB color encoding formats, subsampling occurs after color processing. On monochrome models, vertical binning is performed on the sensor, and horizontal binning is performed on the FPGA. This mode results in a resolution that is both half the width and half the height of the original image. Mode 1 may result in an increase in brightness and improved signal-to-noise ratio, however no frame rate increase is achieved.

### Mode 4

Mode 4 implements 2X vertical binning and 2X horizontal subsampling, and is available on color models only. Horizontal subsampling is performed prior to color processing. Although image quality may be poorer than in Mode 1, a frame rate increase is possible in this mode.

### Mode 5

Mode 5 implements a combination of 4X horizontal and 4X vertical additive binning, resulting in a resolution that is both one quarter the width and one quarter the height of the original image. In color models, all binning is performed after the analog to digital conversion. In monochrome models, vertical binning is performed before the analog to digital conversion, while horizontal binning is performed after the conversion to digital. Mode 5 may result in an increase in brightness and improved signal-to-noise ratio. On monochrome models frame rate will increase; however, on color models, no frame rate increase is achieved.



#### Mode 6

Mode 6 implements a combination of 4X horizontal and 4X vertical binning. This mode is available on color models only, and produces only monochrome output. Vertical binning is performed prior to color processing, and horizontal binning is performed after color processing. Although image quality may be poorer than in Mode 5, a frame rate increase is possible in this mode.

#### Mode 7

Mode 7 allows only for specifying a region of interest, and does not perform any binning. This mode uses a slower pixel clock, and is recommended for longer extended shutter times and/or improved imaging performance. There may be no frame rate increase when ROI size is reduced.

### 5.1.2 Calculating Maximum Possible Frame Rate

The maximum achievable frame rate for each camera on the network depends on available bandwidth, pixel format (bit depth) and resolution, and can be determined using the following formula:

Achievable\_frame\_rate = Available\_bandwidth / Bit\_depth / Resolution

Available bandwidth, in turn, depends on packet size (page 36) and packet delay (page 37). For information about calculating available bandwidth, see Determining Bandwidth Requirements on page 37.

For example, to calculate the maximum achievable frame rate of a camera operating at 1288x964 resolution, 8 bit/pixel format, packet size 1400 bytes and packet delay 1000 ticks:

Achievable frame rate = 182 Mb/s (page 37) / 8 bit/pixel / (1288x964)

Achievable frame rate = 18.3 FPS

# 5.2 Pixel Formats

Pixel formats are an encoding scheme by which color or monochrome images are produced from raw image data. Most pixel formats are numbered 8, 12, or 16 to represent the number of bits per pixel.

The camera's ADC (page 21), which digitizes the images, is configured to a fixed bit output. If the pixel format selected has fewer bits per pixel than the ADC output, the least significant bits are dropped. If the pixel format selected has greater bits per pixel than the ADC output, the least significant bits are padded with zeros.

Pixel Format	Bits per Pixel
Mono 8, Raw 8	8
Mono 12, Raw 12, YUV 411	12
Mono 16, Raw 16, YUV 422	16
RGB 8, YUV 444	24



### 5.2.1 Raw

Raw is a pixel format where image data is Bayer RAW untouched by any on board processing. Selecting a Raw format bypasses the FPGA/color core which disables image processing, such as gamma/LUT and color encoding, but allows for faster frame rates.

### 5.2.2 Mono

Mono is a pixel format where image data is monochrome. Color cameras using a mono format enable FPGA/color core image processing such as access to gamma/LUT.

Y8 and Y16 are also monochrome formats with 8 and 16 bits per pixel respectively.

### 5.2.3 RGB

RGB is a color-encoding scheme that represents the intensities of red, green, and blue channels in each pixel. Each color channel uses 8 bits of data. With 3 color channels, a single RGB pixel is 24 bits.

### 5.2.4 YUV

YUV is a color-encoding scheme that assigns both brightness (Y) and color (UV) values to each pixel. Each Y, U, and V value comprises 8 bits of data. Data transmission can be in 24, 16, or 12 bits per pixel. For 16 and 12 bits per pixel transmissions, the U and V values are shared between pixels to free bandwidth and possibly increase frame rate.

YUV444 is considered a high resolution format which transmits 24 bits per pixel. Each Y, U, and V value has 8 bits.

YUV422 is considered a medium resolution format which transmits 16 bits per pixel. Each Y value has 8 bits, but the U and V values are shared between 2 pixels. This reduces the bandwidth of an uncompressed video signal by one-third with little to no visual difference.

YUV411 is considered a low resolution format which transmits 12 bits per pixel. Each Y value has 8 bits, but the U and V values are shared between 4 pixels. The reduces bandwidth by one half compared to YUV444, but also reduces the color information being recorded.

YUV can be either packed or planar. Packed is when the Y, U, and V components are stored in a single array (macropixel). Planar is when the Y, U, and V components are stored separately and then combined to form the image. Point Grey cameras use packed YUV.

**Related Knowledge Base Articles** 

Title	Article	
Understanding YUV data formats	Knowledge Base Article 313	



### 5.2.5 Y16 (16-bit Mono) Image Acquisition

The camera can output Y16 (16 bits-per-pixel) mono images. Because the camera's A/D converter is less than 16 bits, unused bits are zero.

### **Related Knowledge Base Articles**

Title	Article
Method for converting signal-to-noise ratio (SNR) to/from bits of data	Knowledge Base Article 170

The PGM file format can be used to correctly save 16-bit images. Although the availability of photo manipulation/display applications that can correctly display true 16-bit images is limited, XV in Linux and Adobe Photoshop are two possibilities.

## 5.2.6 Y8 or Y16 Raw Bayer Output

When operating in Y8 or Y16 mode, color models can output either grayscale or raw Bayer data.



Selecting a half-width, half-height image size and monochrome pixel format, such as 800x600 Y8, using a non-Format 7 mode provides a monochrome binned image. In some cases, enabling raw Bayer output in mono mode provides a raw Bayer region of interest of 800x600, centered within the larger pixel array. This has an effect on the field of view.

# 5.3 Supported Formats, Modes and Frame Rates

The tables on the following pages show the supported pixel formats and mode combinations, along with achievable frame rates at varying resolutions, for each camera model.

In some cases, enabling Jumbo Frames on the NIC can help to achieve maximum frame rates. Jumbo Frames can be enabled using the GigE Configurator (page 35).

### 5.3.1 FL3-GE-03S1 Video Modes and Frame Rates

#### Table 5.1: FL3-GE-03S1M Maximum Frame Rates

### Mode 0

Pixel Format	648 x 488	640 x 480	320 x 240	160 x 120
All Formats	120	120	195	290

#### Mode 1

Pixel Format	324 x 244	320 x 240	160 x 120
All Formats	196	196	285

### Mode 7

Pixel Format	648 x 488	640 x 480	320 x 240	160 x 120
All Formats	60	60	60	60





Images acquired by color cameras using Mono8, Mono12 or Mono16 modes are converted to greyscale on the camera. Users interested in accessing the raw Bayer data to apply their own color conversion algorithm or one of the FlyCapture library algorithms should refer to Accessing Raw Bayer Data on page 91.

Table 5.2: FL3-GE-03S1C Maximum Frame Rates

#### Mode 0

Pixel Format	648 x 488	640 x 480	320 x 240	160 x 120
8-bit (Mono8, Raw8)	120	120	195	290
12-bit (Mono12, Raw12, YUV411)	88	90	195	290
16-bit (Mono 16, Raw16, YUV422)	66	68	195	290
24-bit (YUV444, RGB8)	45	46	172	290

#### Mode 1

Pixel Format	324 x 244	320 x 240	160 x 120
All Formats	120	120	195

#### Mode 4

Pixel Format	324 x 244	320 x 240	160 x 120
All Formats	196	196	285

#### Mode 7

Pixel Format	648 x 488	640 x 480	320 x 240	160 x 120
8-, 12-, 16-bit (Mono, Raw, YUV411, YUV422)	60	60	60	60
24-bit (YUV444, RGB8)	45	46	60	60

### 5.3.2 FL3-GE-03S2 Video Modes and Frame Rates

Table 5.3: FL3-GE-03S2M Frame Rates

#### Mode 0

Pixel Format	648 x 488	640 x 480	320 x 240	160 x 120
8-, 12-bit (Mono)	82	82	136	200
16-bit (Mono)	66	68	136	200

#### Mode 1

Pixel Format	324 x 244	320 x 240	160 x 120
All Formats	140	140	200

### Mode 7

Pixel Format	648 x 488	640 x 480	320 x 240	160 x 120
All Formats	60	60	98	146





#### Table 5.4: FL3-GE-03S2C Frame Rates

### Mode 0

Pixel Format	648 x 488	640 x 480	320 x 240	160 x 120
8-, 12-bit (Mono, Raw, YUV411)	82	82	136	200
16-bit (Mono, Raw, YUV422)	66	68	136	200
24-bit (YUV444, RGB)	45	46	136	200

#### Mode 1

	Pixel Format	324 x 244	320 x 240	160 x 120
Ī	All Formats	82	82	136

#### Mode 4

Pixel Format	324 x 244	320 x 240	160 x 120
All Formats	140	140	200

#### Mode 7

Pixel Format	648 x 488	640 x 480	320 x 240	160 x 120
8-, 12-, 16-bit (Mono, Raw, YUV411, YUV422)	60	60	98	146
24-bit (YUV444, RGB8)	45	46	98	146

### 5.3.3 FL3-GE-08S2 Video Modes and Frame Rates

#### Table 5.5: FL3-GE-08S2M Frame Rates

#### Mode 0

Pixel Format	1032 x 776	640 x 480	320 x 240	160 x 120
8-, 12-bit (Mono)	31	42	60	78
16-bit (Mono)	27	42	60	78

#### Mode 1

Pixel Format	516 x 388	320 x 240	160 x 120
All Formats	50	60	74

#### Mode 7

Pixel Format	1032 x 776	640 x 480	320 x 240	160 x 120
All Formats	20	27	38	50





#### Table 5.6: FL3-GE-08S2C Frame Rates

#### Mode 0

Pixel Format	1032 x 776	640 x 480	320 x 240	160 x 120
8-, 12-bit (Mono, Raw, YUV411)	31	42	60	78
16-bit (Mono, Raw, YUV422)	27	42	60	78
24-bit (YUV444, RGB)	18	42	60	78

#### Mode 1

Pixel Format	516 x 388	320 x 240	160 x 120
All Formats	31	42	60

#### Mode 4

Pixel Format	516 x 388	320 x 240	160 x 120
All Formats	50	60	74

#### Mode 7

Pixel Format	1032 x 776	640 x 480	320 x 240	160 x 120
8-, 12-, 16-bit (Mono, Raw, YUV411, YUV522)	20	27	38	50
24-bit (YUV444, RGB)	18	27	38	50

### 5.3.4 FL3-GE-13S2 Video Modes and Frame Rates

#### Table 5.7: FL3-GE-13S2M Frame Rates

#### Mode 0

Pixel Format	1288 x 964	1280 x 960	640 x 480	320 x 240	160 x 120
Mono8	31	31	52	82	116
Mono12	23	23	52	82	116
Mono16	17	17	52	82	116

### Mode 1

Pixel Format	644 x 482	640 x 480	320 x 240	160 x 120
All Formats	58	58	88	120

### Mode 7

Pixel Format	1288 x 964	1280 x 960	640 x 480	320 x 240	160 x 120
All Formats	16	16	27	42	58





#### Table 5.8: FL3-GE-13S2C Frame Rates

#### Mode 0

Pixel Format	1288 x 964	1280 x 960	640 x 480	320 x 240	160 x 120
8-bit (Mono, Raw)	31	31	52	82	116
12-bit (Mono, Raw, YUV411)	23	23	52	82	116
16-bit (Mono, Raw, YUV422	17	17	52	82	116
24-bit (YUV444, RGB)	11.5	11.5	46	82	116

#### Mode 1

Pixel Format	644 x 482	640 x 480	320 x 240	160 x 120
All Formats	31	31	52	82

#### Mode 4

Pixel Format	644 x 482	640 x 480	320 x 240	160 x 120
8-, 12-, 16-bit (Mono)	58	58	88	120
8-, 12-, 16-bit (Raw, YUV411, YUV422)	54	54	82	112
24-bit (YUV444, RGB)	46	46	82	112

#### Mode 7

Pixel Format	1288 x 964	1280 x 960	640 x 480	320 x 240	160 x 120
8-, 12-, 16-bit (Mono, Raw, YUV411, YUV422)	16	16	27	42	58
24-bit (YUV444, RGB)	11.5	11.5	27	42	58

### 5.3.5 FL3-GE-14S3 Video Modes and Frame Rates

#### Table 5.9: FL3-GE-14S3M Frame Rates

### Mode 0

Pixel Format	1384 x 1032	1280 x 960	640 x 480	320 x 240	160 x 120
Mono8	18	19	30	42	52
Mono12	18	19	30	42	52
Mono16	15	17	30	42	52

#### Mode 1

Pixel Format	692 x 512	640 x 480	320 x 240	160 x 120
All Formats	31	32	42	48

#### Mode 7

Pixel Format	1384 x 1032	1280 x 960	640 x 480	320 x 240	160 x 120
8-, 12-bit (Mono)	17	18	29	40	48
16-bit (Mono)	15	17	29	40	48





#### Table 5.10: FL3-GE-14S3C Frame Rates

### Mode 0

Pixel Format	1384 x 1032	1280 x 960	640 x 480	320 x 240	160 x 120
8-, 12-bit (Mono, Raw, YUV411)	18	19	30	42	52
16-bit (Mono, Raw, YUV422)	15	17	30	42	52
24-bit (YUV444, RGB)	10	11.5	30	42	52

### Mode 1

Pixel Format	692 x 516	640 x 480	320 x 240	160 x 120
All Formats	18	19	30	42

#### Mode 4

Pixel Format	692 x 516	640 x 480	320 x 240	160 x 120
All Formats	31	32	42	48

#### Mode 7

Pixel Format	1384 x 1032	1280 x 960	640 x 480	320 x 240	160 x 120
8-, 12-bit (Mono, Raw, YUV411)	17	18	29	40	48
16-bit (Mono, Raw, YUV422)	15	17	29	40	48
24-bit (YUV444, RGB)	10	11.5	29	40	48

## 5.3.6 FL3-GE-20S4 Video Modes and Frame Rates

#### Table 5.11: FL3-GE-20S4M Frame Rates

### Mode 0

Pixel Format	1624 x 1224	1600 x 1200	1280 x 960	640 x 480	320 x 240	160 x 120
8-bit (Mono)	15	15	19	32	48	66
12-bit (Mono)	14	15	19	32	48	66
16-bit (Mono)	11	11	17	32	48	66

### Mode 1

Pixel Format	812 x 612	640 x 480	320 x 240	160 x 120
All Formats	28	32	48	65

### Mode 5

Pixel Format	404 x 306	320 x 240	160 x 120
All Formats	46	50	62

Pixel Format	1624 x 1224	1600 x 1200	1280 x 960	640 x 480	320 x 240	160 x 120
8-bit (Mono)	15	15	19	32	48	66
12-bit (Mono)	14	15	19	32	48	66
16-bit (Mono)	11	11	17	32	48	66





Images acquired by color cameras using Mono8, Mono12 or Mono16 modes are converted to greyscale on the camera. Users interested in accessing the raw Bayer data to apply their own color conversion algorithm or one of the FlyCapture library algorithms should refer to Accessing Raw Bayer Data on page 91.

Table 5.12: FL3-GE-20S4C Frame Rates

### Mode 0

Pixel Format	1624 x 1224	1600 x 1200	1280 x 960	640 x 480	320 x 240	160 x 120
8-bit (Mono, Raw)	15	15	19	32	48	66
12-bit (Mono, Raw, YUV411)	14	15	19	32	48	66
16-bit (Mono, Raw, YUV422)	11	11	17	32	48	66
24-bit (YUV444, RGB)	7	7.5	11.5	32	48	66

### Mode 1

Pixel Format	812 x 612	640 x 480	320 x 240	160 x 120
All Formats	15	19	32	48

#### Mode 4

Pixel Format	812 x 612	640 x 480	320 x 240	160 x 120
All Formats	28	32	48	65

#### Mode 5

Pixel Format	404 x 306	320 x 240	160 x 120
All Formats	15	19	32

#### Mode 6

Pixel Format	404 x 306	320 x 240	160 x 120
All Formats	46	50	62

#### Mode 7

Pixel Format	1624 x 1224	1600 x 1200	1280 x 960	640 x 480	320 x 240	160 x 120
8-bit (Mono, Raw)	15	15	19	32	48	66
12-bit (Mono, Raw, YUV411)	14	15	19	32	48	66
16-bit (Mono, Raw, YUV422)	11	11	17	32	48	66
24-bit (YUV444, RGB)	7	7.5	11.5	32	48	66

### 5.3.7 FL3-GE-28S4 Video Modes and Frame Rates

#### Table 5.13: FL3-GE-28S4M Frame Rates

Pixel Format	1928 x 1448	1600 x 1200	1280 x 960	640 x 480	320 x 240	160 x 120
8-bit (Mono)	15	17	19	28	36	44
12-bit (Mono)	10	15	19	28	36	44
16-bit (Mono)	7.5	11	17	28	36	44



#### Mode 1

Pixel Format	964 x 724	640 x 480	320 x 240	160 x 120
All Formats	27	32	38	44

#### Mode 5

Pixel Format	480 x 362	320 x 240	160 x 120
All Formats	45	45	45

#### Mode 7

Pixel Format	1928 x 1448	1600 x 1200	1280 x 960	640 x 480	320 x 240	160 x 120
8-bit (Mono)	9	10.5	12	18	23	28
12-bit (Mono)	9	10.5	12	18	23	28
16-bit (Mono)	7.5	10.5	12	18	23	28



Images acquired by color cameras using Mono8, Mono12 or Mono16 modes are converted to greyscale on the camera. Users interested in accessing the raw Bayer data to apply their own color conversion algorithm or one of the FlyCapture library algorithms should refer to Accessing Raw Bayer Data on page 91.

Table 5.14: FL3-GE-28S4C Frame Rates

### Mode 0

Pixel Format	1928 x 1448	1600 x 1200	1280 x 960	640 x 480	320 x 240	160 x 120
8-, 12-, 16-bit (Mono, Raw, YUV411, YUV422)	15	17	19	28	36	44
24-bit (YUV444, RGB)	10.5	15	19	28	36	44

#### Mode 1

Pixel Format	964 x 724	640 x 480	320 x 240	160 x 120
All Formats	15	19	28	36

#### Mode 4

Pixel Format	964 x 724	640 x 480	320 x 240	160 x 120
All Formats	27	32	38	44

#### Mode 5

Pixel Format	480 x 362	320 x 240	160 x 120
All Formats	14	19	28

#### Mode 6

Pixel Format	480 x 362	320 x 240	160 x 120
All Formats	45	45	45

Pixel Format	1928 x 1448	1600 x 1200	1280 x 960	640 x 480	320 x 240	160 x 120
All Formats	9	10.5	12	18	23	28



### 5.3.8 FL3-GE-50S5 Video Modes and Frame Rates

Table 5.15: FL3-GE-50S5M Frame Rates

#### Mode 0

Pixel Format	2448 x 2048	1600 x 1200	1280 x 960	640 x 480	320 x 240	160 x 120
8-bit (Mono)	8	12	14	23	32	40
12-bit (Mono)	5.75	12	14	23	32	40
16-bit (Mono)	4.25	11	14	23	32	40

### Mode 1

Pixel Format	1224 x 1024	640 x 480	320 x 240	160 x 120
All Formats	13	22	30	36

#### Mode 5

Pixel Format	612 x 512	320 x 240	160 x 120
All Formats	21	28	32

#### Mode 7

Pixel Format	2448 x 2048	1600 x 1200	1280 x 960	640 x 480	320 x 240	160 x 120
8-, 12-bit (Mono)	5.25	8	9.5	15	21	27
16-bit (Mono)	4.25	8	9.5	15	21	27



Images acquired by color cameras using Mono8, Mono12 or Mono16 modes are converted to greyscale on the camera. Users interested in accessing the raw Bayer data to apply their own color conversion algorithm or one of the FlyCapture library algorithms should refer to Accessing Raw Bayer Data on page 91.

Table 5.16: FL3-GE-50S5C Frame Rates

#### Mode 0

Pixel Format	2448 x 2048	1600 x 1200	1280 x 960	640 x 480	320 x 240	160 x 120
8-bit (Mono, Raw)	8	12	14	23	32	40
12-bit (Mono, Raw, YUV411)	5.75	12	14	23	32	40
16-bit (Mono, Raw, YUV422)	4.25	11	14	23	32	40
24-bit (YUV444, RGB)	2	7.5	11.5	23	32	40

#### Mode 1

Pixel Format	1224 x 1024	640 x 480	320 x 240	160 x 120
All Formats	8	14	22	32

Pixel Format	1224 x 1024	640 x 480	320 x 240	160 x 120
8-, 12-, 16-bit (Mono, Raw, YUV411, YUV422)	13	22	30	36
24-bit (YUV444, RGB)	11.5	22	30	36



#### Mode 5

Pixel Format	612 x 512	320 x 240	160 x 120
All Formats	8	14	22

#### Mode 6

Pixel Format	612 x 512	320 x 240	160 x 120
All Formats	21	28	32

### Mode 7

Pixel Format	2448 x 2048	1600 x 1200	1280 x 960	640 x 480	320 x 240	160 x 120
8-, 12-bit (Mono, Raw, YUV411)	5.25	8	9.5	15	21	27
16-bit (Mono, Raw, YUV422)	4.25	8	9.5	15	21	27
24-bit (YUV444, RGB)	2	7.5	9.5	15	21	27

# 5.4 GenlCam Image Format Control

Name	Display Name	Description	Value
SensorWidth	Sensor Width	Effective width of the sensor in pixels	
SensorHeight	Sensor Height	Effective height of the sensor in pixels	
MaxWidth	Max Width	Maximum width of the image in pixels	
MaxHeight	Max Height	Maximum height of the image in pixels	
Width	Width	Width of the image provided by the device in pixels	
Height	Height	Height of the image provided by the device in pixels	
OffsetX	Offset X	Vertical offset from the origin to the AOI in pixels	
OffsetY	Offset Y	Horizontal offset from the origin to the AOI in pixels	
ReverseX	Reverse X	Flip horizontally the image sent by the device. The AOI is applied after the flip	True False
PixelFormat	Pixel Format	Format of the pixel data (not all cameras support all formats)	Mono8, Mono12, Mono16, Raw8, Raw12, Raw16, RGB, YUV411, YUV422
PixelCoding	Pixel Coding	Coding of the pixels in the image	Mono Raw YUV RGB
PixelSize	Pixel Size	Size of a pixel in bits	8/12/16/24



Name	Display Name	Description	Value
PixelColorFilter	Pixel Color Filter	Type of color filter that is applied to the image	
TestImageSelector	Test Image Selector	Selects the type of test image that is sent by the camera	Off Test Image 1 Test Image 2
VideoMode	Video Mode	Current video mode	0 8
PixelBigEndian	Pixel BigEndian	Set the pixel endianess for pixel format Mono16	True False
BinningHorizontal	Binning Horizontal	Number of horizontal pixels to combine together	
BinningVertical	Binning Vertical	Number of vertical pixels to combine together	
PixelDynamicRangeMin	Dynamic Range Min	Indicates the minimum pixel value transferred from the camera	
PixelDynamicRangeMax	Dynamic Range Max	Indicates the maximum pixel value transferred from the camera	



# 6 Image Acquisition

# 6.1 Asynchronous Triggering

The camera supports asynchronous triggering, which allows the start of exposure (shutter) to be initiated by an external electrical source (hardware trigger) or camera register write (software trigger).

Flea3 GigE Supported Trigger Modes			
Model		Mode	More Information
All	0	Standard	page 71
All	1	Bulb	page 71
All	3	Skip Frames	page 72
All	4	Multi Exposure Preset	page 73
All	5	Multi Exposure Pulse Width	page 74
FL3-GE-13S2 FL3-GE-28S4	13	Low Smear	page 75
All	14	Overlapped	page 76
All	15	Multishot	page 77

# 6.1.1 External Trigger Timing

The time from the external trigger firing to the start of shutter is shown below:

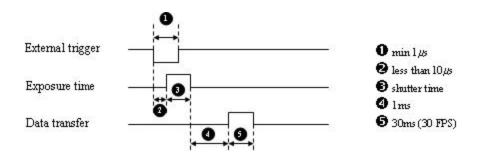


Figure 6.1: External trigger timing characteristics

It is possible for users to measure this themselves by configuring one of the camera's GPIO pins to output a strobe pulse (see Programmable Strobe Output on page 46) and connecting an oscilliscope up to the input trigger pin and the output strobe pin. The camera will strobe each time an image acquisition is triggered; the start of the strobe pulse represents the start of exposure.



### 6.1.2 Camera Behavior Between Triggers

When operating in external trigger mode, the camera clears charges from the sensor at the horizontal pixel clock rate determined by the current frame rate. For example, if the camera is set to 10 FPS, charges are cleared off the sensor at a horizontal pixel clock rate of 15 KHz. This action takes place following shutter integration, until the next trigger is received. At that point, the horizontal clearing operation is aborted, and a final clearing of the entire sensor is performed prior to shutter integration and transmission.

## 6.1.3 Changing Video Modes While Triggering

You can change the video format and mode of the camera while operating in trigger mode. Whether the new mode that is requested takes effect in the next triggered image depends on the timing of the request and the trigger mode in effect. The diagram below illustrates the relationship between triggering and changing video modes.

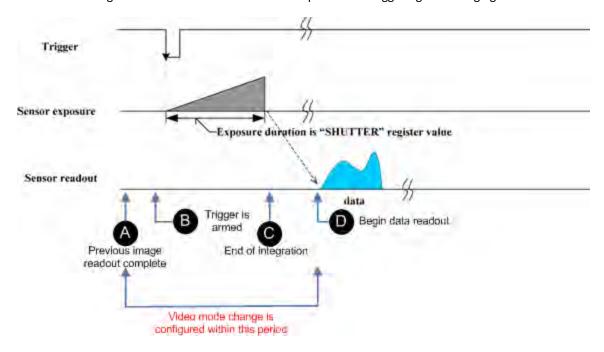


Figure 6.2: Relationship Between External Triggering and Video Mode Change Request

When operating in trigger mode 0 (page 71) or trigger mode 1 (page 71), video mode change requests made before point A on the diagram are honored in the next triggered image. The camera will attempt to honor a request made after point A in the next triggered image, but this attempt may or may not succeed, in which case the request is honored one triggered image later. In trigger mode 14 (page 76), point B occurs before point A. The result is that, in most cases, there is a delay of one triggered image for a video mode request, made before the configuration period, to take effect. In trigger mode 15 (page 77), change requests made after point A for any given image readout are honored only after a delay of one image.

# 6.1.4 Example: Asynchronous Hardware Triggering (Using the FlyCapture API)

The following FlyCapture 2.x code sample uses the C++ interface to do the following:



- Sets the trigger mode to Trigger Mode 0.
- Configures GPIO0 as the trigger input source.
- Enables triggered acquisition.
- Specifies the trigger signal polarity as an active high (rising edge) signal.

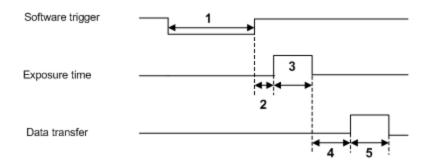
Assuming a Camera object cam:

```
TriggerMode mTrigger;
mTrigger.mode = 0;
mTrigger.source = 0;
mTrigger.parameter = 0;
mTrigger.onOff = true;
mTrigger.polarity = 1;
cam.SetTriggerMode(&mTrigger);
```

## 6.1.5 Asynchronous Software Triggering

Shutter integration can be initiated by setting the Trigger Source to Software in the GenICam features.

The time from a software trigger initiation to the start of shutter is shown below:



- Register write request to register write response
- 2. Approx. 6 us
- 3. Shutter time
- 4. 1 ms
- 5. 30 ms (30 FPS)

Figure 6.3: Software trigger timing

The time from when the software trigger is written on the camera to when the start of integration occurs can only be approximated. The "write success" response is only sent from the camera to the host system once the internal trigger pulse is initiated. We then add the trigger latency (time from the trigger pulse to the start of integration) to this, which is approximately 6 us for a camera capturing 640x480 images.



This timing is solely from the camera perspective. It is virtually impossible to predict timing from the user perspective due to latencies in the processing of commands on the host PC.



# **6.2** Trigger Modes

# 6.2.1 Trigger Mode 0 ("Standard External Trigger Mode")

Trigger Mode 0 is best described as the standard external trigger mode. When the camera is put into Trigger Mode 0, the camera starts integration of the incoming light from external trigger input falling/rising edge. The Exposure Timedescribes integration time. No parameter is required. The camera can be triggered in this mode by using the GPIO pins as external trigger or by using a software trigger.

It is not possible to trigger the camera at full frame rate using Trigger Mode 0; however, this is possible using Trigger Mode 14.

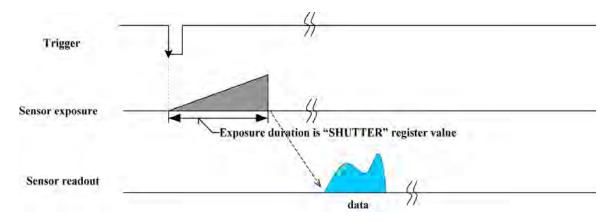


Figure 6.4: Trigger Mode 0 ("Standard External Trigger Mode")

GenICam—Acquisition Control		
Acquisition Mode	Continuous	
Trigger Selector	Exposure Start	
Trigger Mode	On	
Trigger Source	Line x (GPIO pin)	
Trigger Activation	Rising or Falling edge	
Trigger Delay	0	
Exposure Mode	Timed	
Exposure Time	Integration Time	
Exposure Auto	Off	

Registers—TRIGGER_MODE 830h			
Presence	[0]	1	
ON	[6]	1	
Polarity	[7]	Low/High	
Source	[8-10]	GPIO Pin	
Value	[11]	Low/High	
Mode	[12-15]	Trigger_Mode_0	
Parameter	[20-31]	None	

# 6.2.2 Trigger Mode 1 ("Bulb Shutter Mode")

Also known as Bulb Shutter mode, the camera starts integration of the incoming light from external trigger input. Integration time is equal to low state time of the external trigger input.



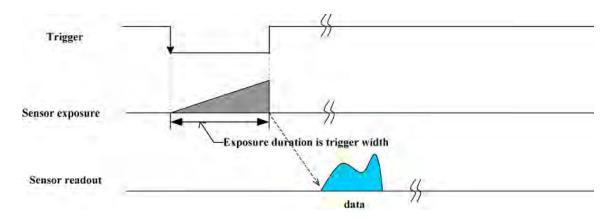


Figure 6.5: Trigger Mode 1 ("Bulb Shutter Mode")

GenICam—Acquisition Control			
Acquisition Mode	Continuous		
Trigger Selector	Exposure Start		
Trigger Mode	On		
Trigger Source	Line x (GPIO pin)		
Trigger Activation	Rising or Falling edge		
Trigger Delay	0		
Exposure Mode	Timed		
Exposure Time	Integration Time		
Exposure Auto	Off		

Registers—TRIGGER_MODE 830h			
Presence	[0]	1	
ON	[6]	1	
Polarity	[7]	Low/High	
Source	[8-10]	GPIO Pin	
Value	[11]	Low/High	
Mode	[12-15]	Trigger_Mode_1	
Parameter	[20-31]	None	

# 6.2.3 Trigger Mode 3 ("Skip Frames Mode")

Trigger Mode 3 allows the user to put the camera into a mode where the camera only transmits one out of N specified images. This is an internal trigger mode that requires no external interaction. Where N is the parameter set in the Trigger Mode, the camera will issue a trigger internally at a cycle time that is N times greater than the current frame rate. As with Trigger Mode 0, the Shutter value describes integration time.



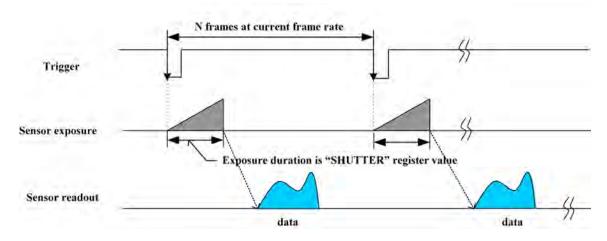


Figure 6.6: Trigger Mode 3 ("Skip Frames Mode")



The debouncer (page 48) does not work in trigger mode 3.

GenICam—Acquisition Control			
Acquisition Mode	MultiFrame		
Acquisition Frame Count	N		
Trigger Selector	Exposure Start		
Trigger Mode	Off		
Trigger Source	Line x (GPIO pin)		
Trigger Activation	Rising or Falling edge		
Trigger Delay	0		
Exposure Mode	Timed		
Exposure Time	Integration Time		
Exposure Auto	Off		

Registers—TRIGGER_MODE 830h		
Presence	[0]	1
ON	[6]	1
Polarity	[7]	Low/High
Source	[8-10]	GPIO Pin
Value	[11]	Low/High
Mode	[12-15]	Trigger_Mode_3
Parameter	[20-31]	N 1 out of N images is transmitted.  Cycle time N times greater than current frame rate

# 6.2.4 Trigger Mode 4 ("Multiple Exposure Preset Mode")

Trigger Mode 4 allows the user to set the number of triggered images to be exposed before the image readout starts. In the case of Trigger Mode 4, the shutter time is controlled by the Shutter value; the minimum resolution of the duration is therefore limited by the shutter resolution.

In the figure below, the camera starts integration of incoming light from the first external trigger input falling edge and exposes incoming light at shutter time. Repeat this sequence for N (parameter) external trigger inputs edge then finish integration. Parameter is required and shall be one or more  $(N \ge 1)$ .



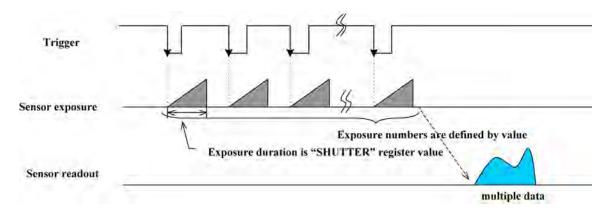


Figure 6.7: Trigger Mode 4 ("Multiple Exposure Preset Mode")

GenICam—Acquisition Control			
Acquisition Mode	MultiFrame		
Acquisition Frame Count	N ≥ 1		
Trigger Selector	Exposure Start		
Trigger Mode	On		
Trigger Source	Line x (GPIO pin)		
Trigger Activation	Rising or Falling edge		
Trigger Delay	0		
Exposure Mode	Timed		
Exposure Time	Integration Time		
Exposure Auto	Off		

Registers—TRIGGER_MODE 830h			
Presence	[0]	1	
ON	[6]	1	
Polarity	[7]	Low/High	
Source	[8-10]	GPIO Pin	
Value	[11]	Low/High	
Mode	[12-15]	Trigger_Mode_4	
Parameter	[20-31]	N ≥ 1	

# 6.2.5 Trigger Mode 5 ("Multiple Exposure Pulse Width Mode")

Trigger Mode 5 allows the user to set the number of triggered images to be exposed before the image readout starts. In the case of Trigger Mode 5, the shutter time is controlled by the trigger pulse duration; the minimum resolution of the duration is generally 1 tick of the pixel clock (see PIXEL\_CLOCK\_FREQ: 1AFOh on page 132). The resolution also depends on the quality of the input trigger signal and the current trigger delay.

In the figure below, the camera starts integration of incoming light from the first external trigger input falling edge and exposes incoming light until the trigger is inactive. Repeat this sequence for N (parameter) external trigger inputs then finish integration. Parameter is required and shall be one or more  $(N \ge 1)$ .



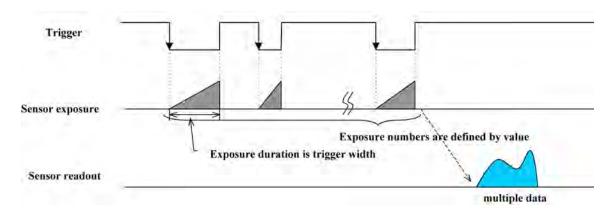


Figure 6.8: Trigger Mode 5 ("Multiple Exposure Pulse Width Mode")

GenICam—Acquisition Control		
Acquisition Mode	MultiFrame	
Acquisition Frame Count	N ≥ 1	
Trigger Selector	Exposure Active	
Trigger Mode	On	
Trigger Source	Line x (GPIO pin)	
Trigger Activation	Rising or Falling edge	
Trigger Delay	0	
Exposure Mode	Trigger Width	
Exposure Time	Integration Time	
Exposure Auto	Off	

Registers—TRIGGER_MODE 830h			
Presence	[0]	1	
ON	[6]	1	
Polarity	[7]	Low/High	
Source	[8-10]	GPIO Pin	
Value	[11]	Low/High	
Mode	[12-15]	Trigger_Mode_5	
Parameter	[20-31]	N ≥ 1 number of images exposed before image readout starts	

# 6.2.6 Trigger Mode 13 ("Low Smear Trigger Mode")

Trigger Mode 13 is a reduced smear imaging mode.

This mode is available for:

- FL3-GE-13S2
- FL3-GE-28S4

Smear reduction works by increasing the speed of the vertical clock near the end of the integration cycle. This step is also known as fast dump. Since the clock speed has been increased, this reduces the time each pixel data has to collect smear while it passes through the vertical shift register.

This trigger mode behaves similarly to standard external trigger mode (Trigger Mode 0) (page 71), except the trigger input first activates a fast dump off the CCD. The fast dump period is followed by exposure, which is controlled by the Shutter settings. The length of the fast dump period is determined by the trigger delay.

For other methods to minimize smear, see Smear Reduction on page 97.



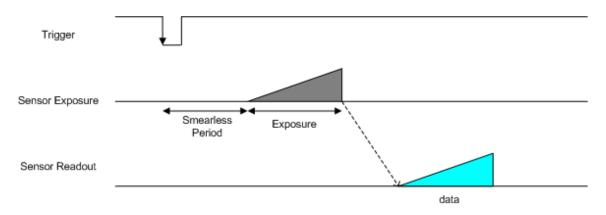


Figure 6.9: Trigger Mode 13 ("Low Smear Trigger Mode")

GenICam—Acquisition Control		
Acquisition Mode	Continuous	
Trigger Selector	Exposure Start	
Trigger Mode	On	
Trigger Source	Line x (GPIO pin)	
Trigger Activation	Rising or Falling edge	
Trigger Delay	Length of the fast dump period	
Exposure Mode	Timed	
Exposure Time	Integration Time	
Exposure Auto	Off	

Registers—TRIGGER_MODE 830h			
Presence	[0]	1	
ON	[6]	1	
Polarity	[7]	Low/High	
Source	[8-10]	GPIO Pin	
Value	[11]	Low/High	
Mode	[12-15]	Trigger_Mode_13	
Parameter	[20-31]	None	

# 6.2.7 Trigger Mode 14 ("Overlapped Exposure/Readout Mode")

Trigger Mode 14 is a vendor-unique trigger mode that is very similar to Trigger Mode 0, but allows for triggering at faster frame rates. This mode works well for users who want to drive exposure start with an external event. However, users who need a precise exposure start should use Trigger Mode 0.

In the figure below, the trigger may be overlapped with the readout of the image, similar to continuous shot (freerunning) mode. If the trigger arrives after readout is complete, it will start as quickly as the imaging area can be cleared. If the trigger arrives before the end of shutter integration (that is, before the trigger is *armed*), it is dropped. If the trigger arrives while the image is still being read out of the sensor, the start of exposure will be delayed until the next opportunity to clear the imaging area without injecting noise into the output image. The end of exposure cannot occur before the end of the previous image readout. Therefore, exposure start may be delayed to ensure this, which means priority is given to maintaining the proper exposure time instead of to the trigger start.



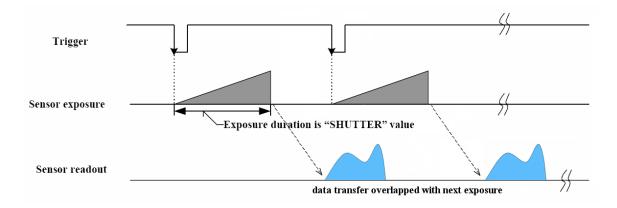


Figure 6.10: Trigger Mode 14 ("Overlapped Exposure/Readout Mode")

GenICam—Acquisition Control		
Acquisition Mode	Continuous	
Trigger Selector	Exposure Start	
Trigger Mode	On	
Trigger Source	Line x (GPIO pin)	
Trigger Activation	Rising or Falling edge	
Trigger Delay	0	
Exposure Mode	Timed	
Exposure Time	Integration Time	
Exposure Auto	Off	

Registers—TRIGGER_MODE 830h		
Presence	[0]	1
ON	[6]	1
Polarity	[7]	Low/High
Source	[8-10]	GPIO Pin
Value	[11]	Low/High
Mode	[12-15]	Trigger_Mode_14
Parameter	[20-31]	None

# 6.2.8 Trigger Mode 15 ("Multi-Shot Trigger Mode")

Trigger Mode 15 is a vendor-unique trigger mode that allows the user to fire a single hardware or software trigger and have the camera acquire and stream a predetermined number of images at the current frame rate.

The number of images to be acquired is determined by the Parameter field of the TRIGGER\_MODE register 0x830 (page 150), which allows up to 255 images to be acquired from a single trigger. Writing a value of 0 to the parameter field will result in an infinite number of images to be acquired, essentially allowing users to trigger the camera into a free-running mode. Once the trigger is fired, the camera will acquire N images with an exposure time equal to the value defined by the SHUTTER register, and stream the images to the host system at the current frame rate. Once this is complete, the camera can be triggered again to repeat the sequence.

Any write to the TRIGGER\_MODE register 0x830 will cause the current sequence to stop.



During the capture of N images, the camera is still in an asynchronous trigger mode (essentially Trigger Mode 14), rather than continuous (free-running) mode. The result of this is that the FRAME\_RATE register 0x83C will be turned OFF, and the camera put into extended shutter mode. Users should therefore ensure that the maximum shutter time is limited to 1/frame\_rate to get the N images captured at the current frame rate.



### **Related Knowledge Base Articles**

Title	Article
Extended shutter mode operation for DCAM-compliant PGR Imaging Products	Knowledge Base Article 166

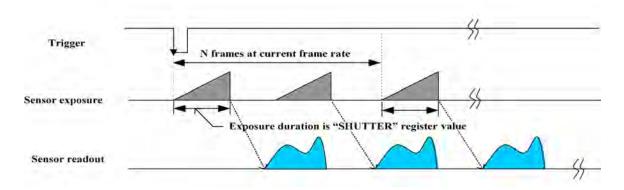


Figure 6.11: Trigger Mode 15 ("Multi-Shot Trigger Mode")

GenICam—Acquisition Control		
Acquisition Mode	MultiFrame	
Acquisition Frame Count	Number of images to be acquired	
Trigger Selector	Exposure Start	
Trigger Mode	On	
Trigger Source	Line x (GPIO pin)	
Trigger Activation	Rising or Falling edge	
Trigger Delay	0	
Exposure Mode	Timed	
Exposure Time	Integration Time	
Exposure Auto	Off	

Registers—TRIGGER_MODE 830h			
Presence	[0]	1	
ON	[6]	1	
Polarity	[7]	Low/High	
Source	[8-10]	GPIO Pin	
Value	[11]	Low/High	
Mode	[12-15]	Trigger_Mode_15	
Parameter	[20-31]	N number of images to be acquired	

# 6.3 GenlCam Acquisition Control

Name	Display Name	Description	Value
AcquisitionMode	Acquisition Mode	Sets the acquisition mode of the device	Continuous Single Frame Multi Frame
AcquisitionStart	Acquisition Start	Starts the acquisition of the device	Write Only
AcquisitionStop	Acquisition Stop	Stops the acquisition of the device at the end of the current frame	Write Only



Name	Display Name	Description	Value
AcquisitionFrameCount	Acquisition Frame Count	Number of frames to acquire in Multi Frame acquisition mode	
AcquisitionFrameRate	Acquisition Frame Rate (Hz)	Controls the acquisition rate (in Hertz) at which the frames are captured	
AcquisitionFrameRateControlEnabled	Acquisition Frame Rate Control Enabled	Enables manual control of the camera frame rate	True False
FrameRateAuto	Frame Rate Auto	Controls the mode for automatic frame rate adjustment	Off Continuous
TriggerSelector	Trigger Selector	Selects the type of trigger to configure	Exposure Start/ Exposure Active
TriggerMode	Trigger Mode	Controls whether or not the selected trigger is active	Off On
TriggerSource	Trigger Source	Specifies the internal signal or physical input line to use as the trigger source. The selected trigger must have its Trigger Mode set to On.	Software Line x where x is a GPIO trigger pin
TriggerActivation	Trigger Activation	Specifies the activation mode of the trigger	Falling Edge Rising Edge
TriggerDelay	TriggerDelay (us)	Specifies the delay (in microseconds) to apply after the trigger reception before activating it	
TriggerDelayEnabled	Trigger Delay Enabled	Specifies whether or not the Trigger Delay is enabled	True False
ExposureMode	Exposure Mode	Sets the operation mode of the exposure (shutter)	Timed Trigger Width
ExposureTime	ExposureTime (us)	Exposure time in microseconds when Exposure Mode is Timed	
ExposureAuto	Exposure Auto	Sets the automatic exposure mode when Exposure mode is Timed	Off Once Continuous

For information on triggering registers, see Asynchronous Trigger Settings on page 150.



# 7 Imaging Parameters and Control

# 7.1 Overview of Imaging Parameters

The camera supports control over the following imaging parameters:

Imaging Parameter	More Information	FlyCapture API Examples
Brightness	page 82	Example: Setting Brightness Using the FlyCapture API on page 82
Gain	page 82	Example: Setting Gain Using the FlyCapture API on page 82
Saturation (color models only)	page 83	Example: Setting Saturation Using the FlyCapture API on page 83
Hue (color models only)	page 84	
Sharpness	page 84	Example: Setting Sharpness Using the FlyCapture API on page 84
Gamma	page 85	Example: Setting Gamma Using the FlyCapture API on page 86
Lookup Table	page 85	
White Balance (color models only)	page 87	Example: Setting White Balance Using the FlyCapture API on page 88
Shutter	page 88	
Bayer Color Processing (color models only)	page 90	Example: Accessing Raw Bayer Data using FlyCapture2 on page 91
Image Mirror/Flip	page 91	
Auto Exposure	page 91	
Embedded Image Information	page 93	

Most of these imaging parameters are defined by **modes** and **values**.

There are three modes:

Mode	Description
Off	Feature is in manual mode and values can be set
Continuous	Feature is in automatice mode and values cannot be set
Once	Feature executes once automatically and then returns to manual mode



Users can define the values for manual operation of a feature.

# 7.2 GenlCam Analog Control

Name	Display Name	Description	Value
Gain	Gain (dB)	Gain applied to the image in dB	
GainAuto	Gain Auto	Controls the mode for automatic gain adjustment	Off Once Continuous
BlackLevel	Black Level (percent)	Analog black level (brightness) in percent	
BlackLevelEnabled	Black Level Enabled	Enables/disables black level adjustment	True False
	Black Level Auto	Controls the mode for automatic black level adjustment	Off Once Continuous
BalanceRatioSelector	Balance Ratio Selector	Selects which balance ratio to control (for White Balance)	Red Blue
BalanceRatio	Balance Ratio	Controls the ratio of the selected color component to a reference color component	
BalanceWhiteAuto	Balance White Auto	Controls the mode for automatic white balancing between color channels	Off Once Continuous
Gamma	Gamma	Controls the gamma correction of pixel intensity	
GammaEnabled	Gamma Enabled	Enables/disables gamma correction	True False
Sharpness	Sharpness	Sharpness of the image	
SharpnessEnabled	Sharpness Enabled	Enables/disables sharpness adjustment	True False
SharpnessAuto	Sharpness Auto	Controls the mode for automatic sharpness adjustment	Off Once Continuous
Hue	Hue (degrees)	Hue of the image in degrees	
HueEnabled	Hue Enabled	Enables/disables Hue	True False
	Hue Level Auto	Controls the mode for automatic hue adjustment	Off Once Continuous
Saturation	Saturation (percent)	Saturation of the image in percent	
	Saturation Enabled	Enables/disables saturation	True False
	Saturation Auto	Controls the mode for automatic saturation adjustment	Off Once Continuous



# 7.3 Brightness

Brightness, also known as offset or black level, controls the level of black in an image.

The camera supports brightness control.

# 7.3.1 Example: Setting Brightness Using the FlyCapture API

The following FlyCapture 2.0 code snippet adjusts brightness to 0.5% using the C++ interface. The snippet assumes a Camera object cam.

```
//Declare a Property struct.
Property prop;
//Define the property to adjust.
prop.type = BRIGHTNESS;
//Ensure the property is set up to use absolute value control.
prop.absControl = true;
//Set the absolute value of brightness to 0.5%.
prop.absValue = 0.5;
//Set the property.
error = cam.SetProperty( &prop );
```

# 7.4 Gain

Gain is the amount of amplification that is applied to a pixel by the A/D converter. An increase in gain can result in a brighter image but also an increase in noise.

The camera supports automatic and one-push gain modes. The A/D converter provides a PxGA gain stage (white balance/preamp) and VGA gain stage. The main VGA gain stage is available to the user, and is variable up to 24 dB in steps of 0.046 dB.



Increasing gain also increases image noise, which can affect image quality. To increase image intensity, try adjusting the lens aperture (iris) and shutter time (page 88) first.

# 7.4.1 Example: Setting Gain Using the FlyCapture API

The following FlyCapture 2.0 code snippet adjusts gain to 10.5 dB using the C++ interface, and assumes a Camera object cam.

```
//Declare a Property struct.
Property prop;
```



```
//Define the property to adjust.
prop.type = GAIN;

//Ensure auto-adjust mode is off.
prop.autoManualMode = false;

//Ensure the property is set up to use absolute value control.
prop.absControl = true;

//Set the absolute value of gain to 10.5 dB.
prop.absValue = 10.5;

//Set the property.
error = cam.SetProperty( &prop );
```

# 7.5 Saturation

This provides a mechanism to control the Saturation component of the images being produced by the camera, given a standard Hue, Saturation, Value (HSV) color space.

Saturation is applicable to color models only.



Saturation in this context does not refer to the saturation of a sensor charge.

# 7.5.1 Example: Setting Saturation Using the FlyCapture API

The following FlyCapture 2.0 code snippet adjusts saturation to 200% using the C++ interface. The snippet assumes a Camera object cam.

```
//Declare a property struct.
Property prop;
//Define the property to adjust.
prop.type = SATURATION;
//Ensure the property is on.
prop.onOff = true;
//Ensure auto-adjust mode is off.
prop.autoManualMode = false;
//Ensure the property is set up to use absolute value control.
prop.absControl = true;
//Set the absolute value of saturation to 200%.
prop.absValue = 200;
//Set the property.
```



```
error = cam.SetProperty( &prop );
```

# 7.6 Hue

This provides a mechanism to control the Hue component of the images being produced by the camera, given a standard Hue, Saturation, Value (HSV) color space.

Hue is applicable to color models only.

## 7.6.1 Example: Setting Hue Using the FlyCapture API

The following FlyCapture 2.0 code snippet adjusts hue to -30 deg. using the C++ interface. The snippet assumes a Camera object cam.

```
//Declare a Property struct.
Property prop;
//Define the property to adjust.
prop.type = HUE;
//Ensure the property is on.
prop.onOff = true;
//Ensure the property is set up to use absolute value control.
prop.absControl = true;
//Set the absolute value of hue to -30 deg.
prop.absValue = -30;
//Set the property.
error = cam.SetProperty( &prop );
```

# 7.7 Sharpness

The camera supports sharpness adjustment, which refers to the filtering of an image to reduce blurring at image edges. Sharpness is implemented as an average upon a 3x3 block of pixels, and is only applied to the green component of the Bayer tiled pattern. For sharpness values greater than 1000, the pixel is sharpened; for values less than 1000 it is blurred. When sharpness is in auto mode and gain is low, then a small amount of sharpening is applied, which increases as gain decreases. If gain is high, a small amount of blur is applied, increasing as gain increases.

When the camera is outputting raw Bayer data, Sharpness is Off by default. Otherwise, the default setting is On.

# 7.7.1 Example: Setting Sharpness Using the FlyCapture API

The following FlyCapture 2.0 code snippet adjusts sharpness to 1500 using the C++ interface. The snippet assumes a Camera object cam.

```
//Declare a Property struct.
Property prop;
```



```
//Define the property to adjust.
prop.type = SHARPNESS;
//Ensure the property is on.
prop.onOff = true;
//Ensure auto-adjust mode is off.
prop.autoManualMode = false;
//Set the value of sharpness to 1500.
prop.valueA = 1500;
//Set the property.
error = cam.SetProperty( &prop );
```

# 7.8 Gamma and Lookup Table

The camera supports gamma and lookup table (LUT) functionality.

Sensor manufacturers strive to make the transfer characteristics of sensors inherently linear, which means that as the number of photons hitting the imaging sensor increases, the resulting image intensity increases are linear. Gamma can be used to apply a non-linear mapping of the images produced by the camera. Gamma is applied after analog-to-digital conversion and is available in all pixel formats. Gamma values between 0.5 and 1 result in decreased brightness effect, while values between 1 and 4 produce an increased brightness effect. By default, Gamma is on and has a value of 1.25. To obtain a linear response, turn gamma off.

For 8-bit, gamma is applied as:

```
OUT = 255*(IN/255)^1/gamma
```



When Gamma is turned on, Lookup Table is turned off. When Lookup Table is turned on, Gamma is turned off.

Lookup Table allows the user to access and control a lookup table (LUT), with entries stored on-board the camera. The LUT is modified under the following circumstances:

- Camera reinitialization
- Changing the current video mode or current video format
- Changing gamma

The LUT can define up to 16 banks where each bank can contain up to 16 channels. Each channel shall define a table with a length of 2<sup>Input\_Depth</sup> entries where each entry is *Output\_Depth* bits wide. Channel table entries shall be padded to 32-bits.

Each bank may be read only, write only or both read and write capable as shown by the LUT\_Bank\_Rd\_Inq and LUT\_Bank\_Wr\_Inq fields. The active bank shall be set by writing to the Active\_Bank field of the LUT\_Ctrl register.

The Bank\_X\_Offset\_Inq register shall give the offset to start address of the array of channel tables in each bank. Multiple channels can be used to process color video pixel data.



#### **Lookup Table Data Structure**

Each bank of channels is composed of entries padded to a complete 32-bits. Each bank is organized as show in the table below.

Cn: Channel Number

En: Entry Number

C(0)E(0)
C(0)E(2 <sup>Input_Depth</sup> -1)
C(1)E(0)
C(1)E(2 <sup>Input_Depth</sup> -1)
C(Number_of_Channels-1)E(0)
C(Number_of_Channels-1) E(2 <sup>Input_Depth</sup> -1)

For information on the Lookup Table register, see LUT: 80000h - 80048h (IIDC 1.32) on page 154

### **Related Knowledge Base Articles**

Title	Article	
How is gamma calculated and applied?	Knowledge Base Article 391	

# 7.8.1 Example: Setting Gamma Using the FlyCapture API

The following FlyCapture 2.0 code snippet adjusts gamma to 1.5 using the C++ interface. The snippet assumes a Camera object cam.

```
//Declare a Property struct.
Property prop;
//Define the property to adjust.
prop.type = GAMMA;
//Ensure the property is on.
```



```
prop.onOff = true;
//Ensure the property is set up to use absolute value control.
prop.absControl = true;
//Set the absolute value of gamma to 1.5
prop.absValue = 1.5;
//Set the property.
error = cam.SetProperty( &prop );
```

## 7.9 White Balance

The camera supports white balance adjustment, which is a system of color correction to account for differing lighting conditions. Adjusting white balance by modifying the relative gain of R, G and B in an image enables white areas to look "whiter". Taking some subset of the target image and looking at the relative red to green and blue to green response, the objective is to scale the red and blue channels so that the response is 1:1:1.

The user can adjust the red and blue values. Both values specify relative gain, with a value that is half the maximum value being a relative gain of zero.

White Balance has two states:

State	Description
Off	The same gain is applied to all pixels in the Bayer tiling.
On/Manual	The Red value is applied to the red pixels of the Bayer tiling and the Blue value is applied to the blue pixels of the Bayer tiling.

The following table illustrates the default gain settings for most cameras.

	Red	Blue
Black and White	32	32
Color	1023	1023

The camera can also implement Auto and One Push white balance. One use of One Push/Auto white balance is to obtain a similar color balance between cameras that are slightly different from each other. In theory, if different cameras are pointed at the same scene, using One Push/Auto will result in a similar color balance between the cameras.

One Push only attempts to automatically adjust white balance for a set period of time before stopping. It uses a "white detection" algorithm that looks for "whitish" pixels in the raw Bayer image data. One Push adjusts the white balance for a specific number of iterations; if it cannot locate any whitish pixels, it will gradually look at the whitest objects in the scene and try to work off them. It will continue this until has completed its finite set of iterations.

Auto is continually adjusting white balance. It differs from One Push in that it works almost solely off the whitest objects in the scene.





The white balance of the camera before using One Push/Auto must already be relatively close; that is, if Red is set to 0 and Blue is at maximum (two extremes), One Push/Auto will not function as expected. However, if the camera is already close to being color balanced, then One Push/Auto will function properly.



For GenlCam features, One Push is the same as Once and Auto is the same as Continuous.

### 7.9.1 Example: Setting White Balance Using the FlyCapture API

The following FlyCapture 2.0 code snippet adjusts the white balance red channel to 500 and the blue channel to 850 using the C++ interface. The snippet assumes a Camera object cam.

```
//Declare a Property struct.
Property prop;
//Define the property to adjust.
prop.type = WHITE_BALANCE;
//Ensure the property is on.
prop.onOff = true;
//Ensure auto-adjust mode is off.
prop.autoManualMode = false;
//Set the white balance red channel to 500.
prop.valueA = 500;
//Set the white balance blue channel to 850.
prop.valueB = 850;
//Set the property.
error = cam.SetProperty( &prop );
```

# 7.10 Shutter

The camera supports automatic, manual and one-push control of the image sensor shutter time. Shutter times are scaled by the divider of the basic frame rate. For example, dividing the frame rate by two (e.g. 15 FPS to 7.5 FPS) causes the maximum shutter time to double (e.g. 66ms to 133ms).

The supported shutter time range is 0.03 ms to 32 seconds (extended shutter mode).



The terms "integration" and "exposure" are often used interchangeably with "shutter".



The time between the end of shutter for consecutive frames will always be constant. However, if the shutter time is continually changing (e.g. shutter is in Auto mode being controlled by Auto Exposure), the time between the beginning of consecutive integrations will change. If the shutter time is constant, the time between integrations will also be constant.

The camera continually exposes and reads image data off of the sensor under the following conditions:

- 1. The camera is powered up; and
- 2. The camera is in free running, not asynchronous trigger, mode. When in async trigger mode, the camera simply clears the sensor and does not read the data off the sensor.

The camera continues to expose images even when isochronous data transfer is disabled and images are not being streamed to the computer. The camera continues exposing images even when ISO is off in order to keep things such as the auto exposure algorithm (if enabled) running. This is done to ensure that when a user starts requesting images (ISO turned on), the first image received is properly exposed.

When operating in free-running mode, changes to the shutter value take effect with the next captured image, or the one after next. Changes to shutter in asynchronous trigger mode generally take effect on the next trigger.

#### 7.10.1 Extended Shutter Times

The maximum shutter time can be extended beyond the normal shutter range by turning off the frame rate setting. Once the frame rate is turned off, you should see the maximum value of the shutter time increase.

#### **Related Knowledge Base Articles**

Title	Article
Extended shutter mode operation for DCAM-compliant PGR Imaging Products.	Knowledge Base Article 166

#### **Related Resources**

Title	Link
FlyCapture SDK ExtendedShutterEx sample program	ExtendedShutterEx

# 7.10.2 Example: Setting Shutter Using the FlyCapture API

The following FlyCapture 2.0 code snippet adjusts the shutter speed to 20 ms using the C++ interface. The snippet assumes a Camera object cam.

```
//Declare a Property struct.
Property prop;
//Define the property to adjust.
prop.type = SHUTTER;
//Ensure the property is on.
prop.onOff = true;
//Ensure auto-adjust mode is off.
prop.autoManualMode = false;
```



```
//Ensure the property is set up to use absolute value control.
prop.absControl = true;

//Set the absolute value of shutter to 20 ms.
prop.absValue = 20;

//Set the property.
error = cam.SetProperty( &prop );
```

# 7.11 Bayer Color Processing

In color models, a Bayer tile pattern color filter array captures the intensity red, green or blue in each pixel on the sensor. The image below is an example of a Bayer tile pattern.

To determine the actual pattern on your camera, query the Pixel Color Filter GenlCam feature.

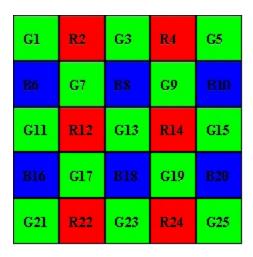


Figure 7.1: Example Bayer Tile Pattern

In order to produce color (e.g. RGB, YUV) and greyscale (e.g. Y8, Y16) images, color models perform on-board processing of the Bayer tile pattern output produced by the sensor.

Conversion from RGB to YUV uses the following formula:

$$\begin{bmatrix} Y_{601} \\ C_{_B} \\ C_{_R} \end{bmatrix} = \begin{bmatrix} 16 \\ 128 \\ 128 \end{bmatrix} + \frac{1}{256} \begin{bmatrix} 65.738 & 129.057 & 25.064 \\ -37.945 & -74.494 & 112.439 \\ 112.439 & -94.154 & -18.285 \end{bmatrix} \begin{bmatrix} R_{255} \\ G_{255} \\ B_{255} \end{bmatrix}$$

To convert the Bayer tile pattern to greyscale, the camera adds the value for each of the RGB components in the color processed pixel to produce a single greyscale (Y) value for that pixel, as follows:

$$Y = R/4 + G/2 + B/4$$



## 7.11.1 Accessing Raw Bayer Data

The actual physical arrangement of the red, green and blue "pixels" for a given camera is determined by the arrangement of the color filter array on the imaging sensor itself. The format, or order, in which this raw color data is streamed out, however, depends on the specific camera model and firmware version.

#### **Related Knowledge Base Articles**

Title	Article
Different color processing algorithms	Knowledge Base Article 33
Writing color processing software and color interpolation algorithms	Knowledge Base Article 37
How is color processing performed on my camera's images?	Knowledge Base Article 89

## 7.11.2 Example: Accessing Raw Bayer Data using FlyCapture2

Using the FlyCapture 2 SDK, raw image data can be accessed programmatically via the getData method of the Image class. In Raw8 modes, the first byte represents the pixel at [row 0, column 0], the second byte at [row 0, column 1], and so on.

Read the BAYER\_TILE\_MAPPING register 0x1040 to determine the current Bayer output format (RGGB, GRBG, and so on). Using a Bayer format of RGGB, for example, the getData method returns the following (assuming char\* data = rawImage.GetData(); and an Image object rawImage):

- data[0] = Row 0, Column 0 = red pixel (R)
- data[1] = Row 0, Column 1 = green pixel (G)
- data[640] = Row 1, Column 0 = green pixel (G)
- data[641] = Row 1, Column 1 = blue pixel (B)

# 7.12 Image Flip/Mirror

The camera supports horizontal image mirroring. The mirror image operation is performed on the camera using the on-board frame buffer (page 42).

# 7.13 Auto Exposure

Auto exposure allows the camera to automatically control shutter and/or gain in order to achieve a specific average image intensity. Additionally, users can specify the range of allowed values used by the auto-exposure algorithm by setting the auto exposure range, the auto shutter range, and the auto gain range.

Auto Exposure allows the user to control the camera system's automatic exposure algorithm. It has three useful states:



State	Description
Off	Control of the exposure is achieved via setting both shutter and gain. This mode is achieved by setting Auto Exposure to Off, or by setting Shutter and Gain to Manual.
ON  Manual Exposure Control	The camera automatically modifies Shutter and Gain to try to match the average image intensity to the Auto Exposure value. This mode is achieved by setting Auto Exposure to Manual and either/both of Shutter and Gain to Automatic.
ON Auto Exposure Control	The camera automatically modifies the value in order to produce an image that is visually pleasing. This mode is achieved by setting the all three of Auto Exposure, Shutter, and Gain to Automatic. In this mode, the value reflects the average image intensity.

Auto Exposure can only control the exposure when Shutter and/or Gain are set to automatic. If only one of the settings is in "auto" mode then the auto exposure controller attempts to control the image intensity using just that one setting. If both of these settings are in "auto" mode the auto exposure controller uses a shutter-before-gain heuristic to try and maximize the signal-to-noise ratio by favoring a longer shutter time over a larger gain value.

In absolute mode, an exposure value (EV) of 0 indicates the average intensity of the image is 18% of 1023 (18% gray).

The auto exposure algorithm is only applied to the active region of interest, and not the entire array of active pixels.

There are four parameters that affect Auto Exposure:

**Auto Exposure Range**—Allows the user to specify the range of allowed exposure values to be used by the automatic exposure controller when in auto mode.

**Auto Shutter Range**—Allows the user to specify the range of shutter values to be used by the automatic exposure controller which is generally some subset of the entire shutter range.

**Auto Gain Range**—Allows the user to specify the range of gain values to be used by the automatic exposure controller which is generally some subset of the entire gain range.

**Auto Exposure ROI** — Allows the user to specify a region of interest within the full image to be used for both auto exposure and white balance. The ROI position and size are relative to the transmitted image. If the request ROI is of zero width or height, the entire image is used.

# 7.13.1 Example: Setting Auto Exposure Using the FlyCapture API

The following FlyCapture 2.0 code snippet adjusts auto exposure to -3.5 EV using the C++ interface. The snippet assumes a Camera object cam.

```
//Declare a Property struct.
Property prop;
//Define the property to adjust.
prop.type = AUTO_EXPOSURE;
//Ensure the property is on.
prop.onOff = true;
//Ensure auto-adjust mode is off.
prop.autoManualMode = false;
```



```
//Ensure the property is set up to use absolute value control.
prop.absControl = true;

//Set the absolute value of auto exposure to -3.5 EV.
prop.absValue = -3.5;

//Set the property.
error = cam.SetProperty( &prop );
```

# 7.14 High Dynamic Range (HDR) Imaging

The camera can be set into a High Dynamic Range mode in which it cycles between 4 user-defined shutter and gain settings, applying one gain and shutter value pair per frame. This allows images representing a wide range of shutter and gain settings to be collected in a short time to be combined into a final HDR image later. The camera does not create the final HDR image; this must be done by the user.

The FlyCapture SDK includes the HighDynamicRange example program. This illustrates how to use the API to capture images in HDR mode.

For information on the HDR register, see HDR: 1800h – 1884h on page 161.

# 7.15 Embedded Image Information

This setting controls the frame-specific information that is embedded into the first several pixels of the image. The first byte of embedded image data starts at pixel 0,0 (column 0, row 0) and continues in the first row of the image data: (1, 0), (2,0), and so forth. Users using color cameras that perform Bayer color processing on the computer must extract the value from the non-color processed image in order for the data to be valid.



Embedded image values are those in effect at the end of shutter integration.

Each piece of information takes up 32-bits (4 bytes) of the image. When the camera is operating in Y8 (8bits/pixel) mode, this is therefore 4 pixels worth of data.

The following frame-specific information can be provided:

- Timestamp
- Gain
- Shutter
- Brightness
- Exposure
- White Balance
- Frame counter
- Strobe Pattern counter
- GPIO pin state
- ROI position



If you turned on all possible options the first 40 bytes of image data would contain camera information in the following format, when accessed using the FlyCapture 2 API:

(assuming unsigned char\* data = rawImage.GetData(); and an Image object rawImage):

- data[0] = first byte of Timestamp data
- data[4] = first byte of Gain data
- data[24] = first byte of Frame Counter data

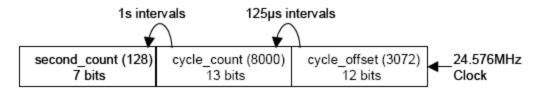
If only Shutter embedding were enabled, then the first 4 bytes of the image would contain Shutter information for that image. Similarly, if only Brightness embedding were enabled, the first 4 bytes would contain Brightness information.

For black and white cameras, white balance is still included, but no valid data is provided.

For information on the embedded information register, see FRAME\_INFO: 12F8h on page 162.

#### **Interpreting Timestamp information**

The Timestamp format is as follows (some cameras replace the bottom 4 bits of the cycle offset with a 4-bit version of the Frame Counter):



Cycle offset increments from 0 to 3071, which equals one cycle count.

Cycle count increments from 0 to 7999, which equals one second.

Second count increments from 0 to 127. All counters reset to 0 at the end of each cycle.

#### Interpreting ROI information

The first two bytes are the distance from the left frame border that the region of interest (ROI) is shifted. The next two bytes are the distance from the top frame border that the ROI is shifted.



# 8 Troubleshooting

# 8.1 Support

Point Grey Research endeavors to provide the highest level of technical support possible to our customers. Most support resources can be accessed through the Point Grey Product Support page.

#### **Creating a Customer Login Account**

The first step in accessing our technical support resources is to obtain a Customer Login Account. This requires a valid name and e-mail address. To apply for a Customer Login Account go to the Product Downloads page.

#### **Knowledge Base**

Our <u>Knowledge Base</u> contains answers to some of the most common support questions. It is constantly updated, expanded, and refined to ensure that our customers have access to the latest information.

#### **Product Downloads**

Customers with a Customer Login Account can access the latest software and firmware for their cameras from our <a href="Product\_Downloads">Product\_Downloads</a> page. We encourage our customers to keep their software and firmware up-to-date by downloading and installing the latest versions.

#### **Contacting Technical Support**

Before contacting Technical Support, have you:

- 1. Read the product documentation and user manual?
- 2. Searched the Knowledge Base?
- 3. Downloaded and installed the latest version of software and/or firmware?

If you have done all the above and still can't find an answer to your question, contact our Technical Support team.

# 8.2 Camera Diagnostics

There are a number of control and status registers that can be used for camera diagnostics. See Camera Diagnostics on page 163 for more information.

## 8.3 Status Indicator LED

The user can turn off the camera's status LED. LEDs are re-enabled the next time the camera is power cycled.

Table 8.1: LED During Camera Power-up and Operation

LED Status	Description
Off	Not receiving power
Steady green, high intensity (~5 seconds)	1. Camera powers up



LED Status	Description
Green/Red, flashing (~2 seconds)	2. Camera programs the FPGA
Green flashing quickly, low intensity	3. Establishing IP connection. The camera attempts to establish an IP connection in the following order:
One green blink (~1-2 seconds) Two green blinks (~1-2 seconds) Three green blinks (~1-2 seconds) Three red blinks (~1-2 seconds)	i) A persistent IP address, if enabled and available; ii) a DHCP address, if enabled and available; iii) a link-local address (LLA). iv) Failure to establish connection
Steady green, high intensity	4. Camera is streaming images
Red/Green flashing quickly	Firmware update in progress
Red flashing slowly	General error - contact technical support

For information on the LED register, see LED\_CTRL: 1A14h on page 165.

### 8.4 Test Pattern

The camera is capable of outputting continuous static images for testing and development purposes. The test pattern image is inserted into the imaging pipeline immediately prior to the transfer to the on-board FIFO, and is therefore not subject to changes in imaging parameters.

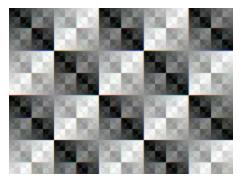


Figure 8.1: Test Pattern Sample Image

# 8.4.1 Image Format Control—Test Image

Image Format Control		
Test Image Selector	Off Test Image 1 Test Image 2	

# 8.5 Blemish Pixel Artifacts

Cosmic radiation may cause random pixels to generate a permanently high charge, resulting in a permanently lit, or 'glowing,' appearance. Point Grey tests for and programs white blemish pixel correction into the camera firmware.



In very rare cases, one or more pixels in the sensor array may stop responding and appear black (dead) or white (hot/stuck).

#### 8.5.1 Pixel Defect Correction

Point Grey tests for blemish pixels on each camera. The mechanism to correct blemish pixels is hard-coded into the camera firmware, and can be turned off and on by the user. Pixel correction is on by default. The correction algorithm involves applying the average color or grayscale values of neighboring pixels to the blemish pixel.



Pixel correction is not done in any of the binning modes (page 53).

#### **Related Knowledge Base Articles**

Title	Article	
How Point Grey tests for white blemish pixels	Knowledge Base Article 314	

For information on the Blemish Pixel Correction register, see PIXEL\_DEFECT\_CTRL: 1A60h on page 165.

#### 8.6 Vertical Smear Artifact

When a strong light source is shone on the camera, a faint bright line may be seen extending vertically through an image from a light-saturated spot. Vertical smear is a byproduct of the interline transfer system that extracts data from the CCD.

Smear is caused by scattered photons leaking into the shielded vertical shift register. When the pixel cells are full, some charges may spill out in to the vertical shift register. As the charge shifts in/out of the light sensitive sensor area and travels down the vertical shift register, it picks up the extra photons and causes a bright line in the image.

Smear above the bright spot is collected during read out while smear below the bright spot is collected during read in.

#### 8.6.1 Smear Reduction

Smear may be minimized using one or more of the following techniques:

- Reducing the bright light source.
- Increase the shutter time/lower the frame rate. This increases the amount of time light is collected in the photosensors relative to the time in the vertical transfer register.
- Turn the light source off before and after exposure by using a mechanical or LCD shutter.
- Use a pulsed or flashed light source. A pulsed light of 1/10,000 duration is sufficient in most cases to allow an extremely short 100ns exposure without smear.
- Increase light collimation by using a lens with variable aperture. Note that an effect of closing the iris is a



darker image.

• Some camera models have a low smear trigger mode (page 75) which may reduce the effect of smear.

## **Related Knowledge Base Articles**

Title	Article
Vertical bleeding or smearing from a saturated portion of an image	Knowledge Base Article 88



# **Appendix A: GenlCam Features**

The following features are included in the XML device description file on the camera to control, monitor, and query the camera operation. Not all operations can be controlled using the XML file; those not included are controlled via CSRs.



Except where noted, these features conform to the GenlCam Standard Features Naming Convention (SFNC) v1.5. The full SFNC can be found on the <u>EMVA.org website</u> and contains more details than provided below. Not all features are available on all cameras.

Non-SFNC features are noted with a grey background.

This file can be accessed via First URL bootstrap register 200h (page 108).

## A.1 Device Control

Name	Display Name	Description	Value
DeviceVendorName	Vendor Name	Name of the manufacturer	Point Grey Research
DeviceModelName	Model Name	Model name of the device	Flea3 GigE <model number=""></model>
DeviceVersion	Device Version	FPGA version	
DeviceFirmwareVersion	Device Firmware Version	Firmware version	
DeviceID	Device ID	Camera Serial Number	
DeviceScanType	Device Scan Type	Scan type of the sensor	Areascan (2D sensor)
DeviceTemperature	Device Temperature (C)	Device temperature in degrees Celsius	
DeviceReset	Device Reset	Resets the device to its initial state and default settings	Write Only
DeviceUserID	Device User ID	User defined name	
DeviceMaxThroughput	Device Max Throughput	Indicates maximum data in bytes from the camera each second	

# A.2 Analog Control

Name	Display Name	Description	Value
Gain	Gain (dB)	Gain applied to the image in dB	
GainAuto	Gain Auto	Controls the mode for automatic gain adjustment	Off Once Continuous
BlackLevel	Black Level (percent)	Analog black level (brightness) in percent	



Name	Display Name	Description	Value
BlackLevelEnabled	Black Level Enabled	Enables/disables black level adjustment	True False
	Black Level Auto	Controls the mode for automatic black level adjustment	Off Once Continuous
BalanceRatioSelector	Balance Ratio Selector	Selects which balance ratio to control (for White Balance)	Red Blue
BalanceRatio	Balance Ratio	Controls the ratio of the selected color component to a reference color component	
BalanceWhiteAuto	Balance White Auto	Controls the mode for automatic white balancing between color channels	Off Once Continuous
Gamma	Gamma	Controls the gamma correction of pixel intensity	
GammaEnabled	Gamma Enabled	Enables/disables gamma correction	True False
Sharpness	Sharpness	Sharpness of the image	
SharpnessEnabled	Sharpness Enabled	Enables/disables sharpness adjustment	True False
SharpnessAuto	Sharpness Auto	Controls the mode for automatic sharpness adjustment	Off Once Continuous
Hue	Hue (degrees)	Hue of the image in degrees	
HueEnabled	Hue Enabled	Enables/disables Hue	True False
	Hue Level Auto	Controls the mode for automatic hue adjustment	Off Once Continuous
Saturation	Saturation (percent)	Saturation of the image in percent	
	Saturation Enabled	Enables/disables saturation	True False
	Saturation Auto	Controls the mode for automatic saturation adjustment	Off Once Continuous

# A.3 Image Format Control

Name	Display Name	Description	Value
SensorWidth	Sensor Width	Effective width of the sensor in pixels	
SensorHeight	Sensor Height	Effective height of the sensor in pixels	
MaxWidth	Max Width	Maximum width of the image in pixels	
MaxHeight	Max Height	Maximum height of the image in pixels	



Name	Display Name	Description	Value
Width	Width	Width of the image provided by the device in pixels	
Height	Height	Height of the image provided by the device in pixels	
OffsetX	Offset X	Vertical offset from the origin to the AOI in pixels	
OffsetY	Offset Y	Horizontal offset from the origin to the AOI in pixels	
ReverseX	Reverse X	Flip horizontally the image sent by the device. The AOI is applied after the flip	True False
PixelFormat	Pixel Format	Format of the pixel data (not all cameras support all formats)	Mono8, Mono12, Mono16, Raw8, Raw12, Raw16, RGB, YUV411, YUV422
PixelCoding	Pixel Coding	Coding of the pixels in the image	Mono Raw YUV RGB
PixelSize	Pixel Size	Size of a pixel in bits	8/12/16/24
PixelColorFilter	Pixel Color Filter	Type of color filter that is applied to the image	
TestImageSelector	Test Image Selector	Selects the type of test image that is sent by the camera	Off Test Image 1 Test Image 2
VideoMode	Video Mode	Current video mode	0 8
PixelBigEndian	Pixel BigEndian	Set the pixel endianess for pixel format Mono16	True False
BinningHorizontal	Binning Horizontal	Number of horizontal pixels to combine together	
BinningVertical	Binning Vertical	Number of vertical pixels to combine together	
PixelDynamicRangeMin	Dynamic Range Min	Indicates the minimum pixel value transferred from the camera	
PixeIDynamicRangeMax	Dynamic Range Max	Indicates the maximum pixel value transferred from the camera	



# A.4 Acquisition Control

Name	Display Name	Description	Value
AcquisitionMode	Acquisition Mode	Sets the acquisition mode of the device	Continuous Single Frame Multi Frame
AcquisitionStart	Acquisition Start	Starts the acquisition of the device	Write Only
AcquisitionStop	Acquisition Stop	Stops the acquisition of the device at the end of the current frame	Write Only
AcquisitionFrameCount	Acquisition Frame Count	Number of frames to acquire in Multi Frame acquisition mode	
AcquisitionFrameRate	Acquisition Frame Rate (Hz)	Controls the acquisition rate (in Hertz) at which the frames are captured	
AcquisitionFrameRateControlEnabled	Acquisition Frame Rate Control Enabled	Enables manual control of the camera frame rate	True False
FrameRateAuto	Frame Rate Auto	Controls the mode for automatic frame rate adjustment	Off Continuous
TriggerSelector	Trigger Selector	Selects the type of trigger to configure	Exposure Start/ Exposure Active
TriggerMode	Trigger Mode	Controls whether or not the selected trigger is active	Off On
TriggerSource	iggerSource Trigger Source		Software Line x where x is a GPIO trigger pin
TriggerActivation	Trigger Activation	Specifies the activation mode of the trigger	Falling Edge Rising Edge
TriggerDelay	elay TriggerDelay (us)		
TriggerDelayEnabled	Trigger Delay Enabled	Specifies whether or not the Trigger Delay is enabled	True False
ExposureMode	Exposure Mode	Sets the operation mode of the exposure (shutter)	Timed Trigger Width
ExposureTime	ExposureTime (us)	Exposure time in microseconds when Exposure Mode is Timed	
ExposureAuto	Exposure Auto	Sets the automatic exposure mode when Exposure mode is Timed	Off Once Continuous



# A.5 Digital Input Output Control

Name	Display Name	Description	Value
LineSelector	+ Line Selector	Selects the physical line (or GPIO pin) of the external device connector to configure.	Line 0 Line 1 Line 2 Line 3
LineMode	Line Mode	Controls whether the physical line is used to Input or Output a signal. Choices are dependent on which line is selected.	Input Trigger Strobe Output
LineSource	Line Source	Selects which input or output signal to output on the selected line. Line Mode must be Output.	Exposure Active External Trigger Active
LineInverter	Line Inverter	Controls the invertion of the signal of the selected input or output line	True False
StrobeEnabled	Strobe Enabled	Enables/disables strobe	True False
UserOutputValue	User Output Value	Sets the value of the user output selector	True = High False = Low
LineStatus	Line Status	Returns the current status of the selected input or output line	True = High False = Low
LineStatusAll	Line Status All	Returns the current status of all available line signals at time of polling in a single bitfield	

# A.6 Transport Layer Control

All GigE Vision features start with GEV.

Name	Display Name	Description	Value
PayloadSize	Payload Size	Provides the number of bytes transferred for each image or chunk on the stream channel.  This is mainly used by the application software to determine size of image buffers to allocate.	
GevVersionMajor	GEV Version Major	Major version of the specification	
GevVersionMinor	GEV Version Minor	Minor version of the specification	
GevDeviceModeIsBigEndian  GEV Device Mode Is Endian		Endianess of device registers	True False
GevDeviceModeCharacterSet GEV Device Mode Character Set		Character set used by all the strings of the bootstrap registers	



Name	Display Name	Description	Value
GevInterfaceSelector	+ GEV Interface Selector	Selects which physical network interface to control	
GevMACAddress	GEV MAC Address	MAC address of the network interface	
GevCurrentIPConfigurationLLA	GEV Current IPConfiguration LLA	Indicates if Link Local Address (LLA) IP configuration scheme is activated on the given network interface	True False
GevCurrentIPConfigurationDHCP	GEV Current IPConfiguration DHCP	Indicates if DHCP IP configuration scheme is activated on the given network interface	True False
Gev- CurrentIPConfigurationPersistentIP	GEV Current IPConfiguration Persistent IP	Indicates if Persistent IP configuration scheme is activated on the given network interface	True False
GevCurrentIPAddress	GEV Current IPAddress	Current IP address for the given network interface	
GevCurrentSubnetMask	GEV Current Subnet Mask	Current subnet mask of the given interface	
GevCurrentDefaultGateway	GEV Current Default Gateway	Indicates the default gateway IP address to be used on the given network interface	
GevPersistentIPAddress	vPersistentIPAddress GEV Persistent IP Address		
GevPersistentSubnetMask	sistentSubnetMask  GEV Persistent Subnet Mask		
GevPersistentDefaulGateway	GEV Persistent Default Gateway	Indicates the persistent default gateway for this network interface. It is only used when the device boots with the persistent IP configuration scheme.	
GevLinkSpeed	GEV Link Speed	Indicates the speed of transmission negotiated by the given network interface in Mbps	



Name	Display Name	Description	Value
GevSupportedOptionSelector	+ GEV Supported Option Selector	Selects the GEV option to interrogate for existing support	User Defined Name Serial Number Heartbeat Disable Link Speed CCP Application Socket Manifest Table Test Data Discovery Ack Delay Discovery Ack Delay Writable Extended Status Codes Action Pending Ack Event Data Event Packet Resend Write Mem Commands Concatenation IPConfiguration DHCP IPConfiguration Persistent IP Stream Channel Source Socket
GEVSupportedOption	GEV Supported Option	Indicates whether or not the selected GEV option is supported	True False
GevFirstURL	GEV First URL	The first choice of URL for the SML device description file	
GevSecondURL	GEV Second URL	The second choice of URL for the SML device description file	
GevNumberOfInterfaces	GEV Number Of Interfaces	Indicates the number of physical network interfaces supported by this device	
GevMessageChannelCount	GEV Message Channel Count	Indicates the number of message channels supported by this device	
GevStreamChannelCount	GEV Stream Channel Count	Indicates the number of stream channels supported by this device	
GevHeartbeatTimeout	GEV Heartbeat Timeout	Indicates the current heartbeat timeout in milliseconds	
GevHeartbeatDisable	GEV Heartbeat Disable	Disables the GVCP heartbeat	True False
GevTimstampTickFrequency	GEV Timestamp Tick Frequency	Indicates the number of timestamps ticks in 1 second (frequency in Hertz)	



Name	Display Name	Description	Value
GevCCP	GEV CCP	Controls the device access privilege of an application	Open Access Exclusive Access Control Access
BevStreamChannelSelector	GEV Stream Channel Selector	Selects the stream channel to control	
GevSCPInterfaceIndex	GEV SCP Interface Index	Index of network interface to use	
GevSCPHostPort	GEV SCP Host Port	Host port of the channel	
GevSCPDirection	GEV SCP Direction	Transmit or receive of the channel	
GevSCPSFireTestPacket	GEV SCPS Fire Test Packet	Sends a test packet	True False
GevSCPSDoNotFragment	GEV SCPS Do Not Fragment	The state of this feature is copied into the "do not fragment" bit of the IP header of each stream packet	True False
GevSCPSBigEndian	GEV SCPS Big Endian	Endianess of multi-byte pixel data for this stream	True False
GevSCPSPacketSize	GEV SCPS Packet Size	Specifies the stream packet size in bytes to send on this channel	
GevSCPD	GEV SCPD	Indicates the delay (in timestamp counter units) to insert betweeen each packet for this stream channel. This can be used as a crude flow-control mechanism if the application or the network infrastructure cannot keep up with the packets coming from the device.	
GevSCDA	GEV SCDA	Indicates the destination IP address for this stream channel	
GevSCSP	GEV SCSP	Indicates the source UDP port address for this stream channel	
pgrDCTP	Device Current Throughput	Indicates the current data in bytes from the camera each second. This value is equivalent to either DeviceAssignedBandwidth or DeviceMaxThroughput, whichever is lower.	
pgrDABW	Device Assigned Bandwidth	Indicates assigned bandwidth (bytes/second) for the camera to transfer data except resend packets	



# A.7 User Set Control

Name	Display Name	Description	Value
CurrentUserSet	Current User Set	Indicates the user set that is currently in use. At initialization time, the camera loads the most recently saved user set	0 (default) 1 2
UserSetSelector	User Set Selector	Selects the user set to load or save	Default User Set 1 User Set 2
UserSetLoad	User Set Load	Loads the user set specified by the User Set Selector to the device and makes it active	Write Only
UserSetSave	User Set Save	Saves the user set specified by the User Set Selector to the non-volatile memory of the device	Write Only
DefaultUserSet	Default User Set	Selects the default user set as the default start up set	Default User Set 1 User Set 2



# **Appendix B: GigE Vision Bootstrap Registers**

The camera supports the following GigE Vision bootstrap registers. All registers are implemented according to the GigE Vision standard.

Register	Address (no offset)
Version	0000h
Device Mode	0004h
Device MAC	0008h
Supported IP Configuration	0010h
Current IP Configuration	0014h
Current IP Address	0024h
Current Subnet Mask	0034h
Current Default Gateway	0044h
Manufacturer Name	0048h
Model Name	0068h
Device Version	0088h
Manufacturer Info	00A8h
Serial Number	00D8h
First URL	0200h
Second URL	0400h
Number of Network Interfaces	0600h
Persistent IP Address	064Ch
Persistent Subnet Mask	065Ch
Persistent Default Gateway	066Ch
Link Speed	0670h
Number of Message Channels	0900h
Number of Stream Channels	0904h
Stream Channels Capability	092Ch
GVCP Capability	0934h
Heartbeat Timeout	0938h
Timestamp Tick Frequency	093Ch (high part) 0940h (low part)
Timestamp Control	0944h
Timestamp Value	0948h (high part) 094Ch (low part)
GVCP Configuration	0954h



Register	Address (no offset)
Control Channel Privelege	0A00h
Stream Channel Port	0D00h + 40h * x with 0 <= x < 512
Stream Channel Packet Size	0D04h + 40h * x with 0 <= x < 512
Stream Channel Packet Delay	0D08h + 40h * x with 0 <= x < 512
Stream Channel Destination Address	0D18h + 40h * x with 0 <= x < 512



# **Appendix C: Control and Status Registers**

# **C.1** Using Control and Status Registers

The user can monitor or control each feature of the camera through the control and status registers (CSRs) programmed into the camera firmware. These registers conform to the IIDC v1.32 standard (except where noted). *Format* tables for each 32-bit register are presented to describe the purpose of each bit that comprises the register. Bit 0 is always the most significant bit of the register value.

Register offsets and values are generally referred to in their hexadecimal forms, represented by either a '0x' before the number or 'h' after the number, e.g. the decimal number 255 can be represented as 0xFF or FFh.

The controllable fields of most registers are *Mode* and *Value*.

#### C.1.1 Modes

Each CSR has three bits for mode control, ON\_OFF, One\_Push and A\_M\_Mode (Auto/Manual mode). Each feature can have four states corresponding to the combination of mode control bits.



Not all features implement all modes.

**Table C.1: CSR Mode Control Descriptions** 

One_Push	ON_OFF	A_M_Mode	State
N/A	0	N/A	Off state. Feature will be fixed value state and uncontrollable.
N/A	1	1	Auto control state. Camera controls feature by itself continuously.
0	1	0	Manual control state. User can control feature by writing value to the value field.
1 (Self clear)	1	0	One-Push action. Camera controls feature by itself only once and returns to the Manual control state with adjusted value.

#### C.1.2 Values

If the *Presence\_Inq* bit of the register is one, the *value* field is valid and can be used for controlling the feature. The user can write control values to the *value* field only in the **Manual control state**. In the other states, the user can only read the *value*. The camera always has to show the real setting value at the *value* field if *Presence\_Inq* is one.



## C.1.3 Register Memory Map

The camera uses a 64-bit fixed addressing model. The upper 10 bits show the Bus ID, and the next six bits show the Node ID. The next 20 bits must be 1 (FFFF Fh).

Address	Register Name	Description	
FFFF F000 0000h	Base address		
FFFF F000 0400h	Config ROM		
FFFF F0F0 0000h	Base address for all camera control	command registers	
The following register addres	ses are offset from the base address,	FFFF F0F0 0000h.	
000h	INITIALIZE	Camera initialize register	
100h	V_FORMAT_INQ	Inquiry register for video format	
180h	V_MODE_INQ_X	Inquiry register for video mode	
200h	V_RATE_INQ_y_X	Inquiry register for video frame rate	
300h	Reserved		
	BASIC_FUNC_INQ		
400h	FEATURE_HI_INQ	Inquiry register for feature presence	
	FEATURE_LO_INQ		
500h	Feature_Name_INQ	Inquiry register for feature elements	
600h	CAM STA CTDI	Status and control register for camera	
640h	CAM_STA_CTRL	Feature control error status register	
700h	ABS_CSR_HI_INQ_x	Inquiry register for Absolute value CSR offset address	
800h	Feature_Name	Status and control register for feature	

The FlyCapture API library has function calls to get and set camera register values. These function calls automatically take into account the base address. For example, to get the 32-bit value of the SHUTTER register at 0xFFFF F0F0 081C:

#### FlyCapture v1.x:

```
flycaptureGetCameraRegister(context, 0x81C, &ulValue);
flycaptureSetCameraRegister(context, 0x81C, ulValue);
```

FlyCapture v2.x (assuming a camera object named cam):

```
cam.ReadRegister(0x81C, &regVal);
cam.WriteRegister(0x81C, regVal, broadcast=false);
```

Broadcast is only available for FlyCapture 2 and FireWire cameras. FireWire has the ability to write to multiple cameras at the same time.



# C.1.4 Config ROM

#### C.1.4.1 Root Directory

	Offset	Bit	Description
	400h	[0-7]	04h
		[8-15]	crc_length
		[16-31]	rom_crc_value
		[0-7]	31h
	40.41-	[8-15]	33h
	404h	[16-23]	39h
		[24-31]	34h
		[0-3]	0010 (binary)
Bus Info Block		[4-7]	Reserved
		[8-15]	FFh
	408h	[16-19]	max_rec
		[20]	Reserved
		[21-23]	mxrom
		[24-31]	chip_id_hi
	40Ch	[0-23]	node_vendor_id
	40CH	[24-31]	chip_id_hi
	410h	[0-31]	chip_id_lo
	414h	[0-15]	0004h
	41411	[16-31]	CRC
	418h	[0-7]	03h
	41011	[8-31]	module_vendor_id
		[0-7]	0Ch
Root Directory	41Ch	[8-15]	Reserved
		[16-31]	1000001111000000 (binary)
	420h	[0-7]	8Dh
	42011	[8-31]	indirect_offset
	424h	[0-7]	D1h
	42411	[8-31]	unit_directory_offset

## C.1.4.2 Unit Directory

Offset	Bit	Description
0000h	[0-15]	0003h
UUUUII	[16-31]	CRC



Offset	Bit	Description			
0004h	[0-7]	12h			
000411	[8-31]	unit_spec_ID (=0x00A02D)			
0008h	[0-7]	13h			
000811	[8-31] unit_sw_version (=0x000102)				
000Ch	[0-7] D4h				
000Ch	[8-31]	unit dependent directory offset			

## C.1.4.3 Unit Dependent Info

Offset	Bit	Description				
0000h	[0-15]	unit_dep_info_length				
UUUUN	[16-31]	CRC				
	[0-7]	40h				
0004h	[8-31]	command_regs_base 32-bit offset from the base address of initial register space of the base address of the command registers				
	[0-7]	81h				
0008h	[8-31]	vendor_name_leaf The number of 32-bits from the address of the vendor_name_leaf entry to the address of the vendor_ name leaf containing an ASCII representation of the vendor name of this node				
	[0-7]	82h				
000Ch	[8-31]	model_name_leaf The number of 32-bits from the address of the model_name_leaf entry to the address of the model_ name leaf containing an ASCII representation of the model name of this node				
	[0-7]	38h				
0010h	[8-31]	unit_sub_sw_version the sub version information of this unit unit_sub_sw_version = 0x000000h or unspecified for IIDC v1.30 unit_sub_sw_version = 0x000010h for IIDC v1.31 unit_sub_sw_version = 0x000020h for IIDC v1.32				
	[0-7]	39h				
0014h	[8-31]	Reserved				
_	[0-7]	3Ah				
0018h	[8-31]	Reserved				
	[0-7]	3Bh				
001Ch	[8-31] Reserved					
00201-	[0-7]	3Ch				
0020h	[8-31]	vendor_unique_info_0				
0024h	[0-7]	3Dh				
002411	[8-31]	vendor_unique_info_1				



Offset	Bit	Description				
0028h	[0-7]	3Eh				
002811	[8-31]	vendor_unique_info_2				
[0-7]		3Fh				
002Ch	[8-31]	vendor_unique_info_3				

#### C.1.5 Calculating Base Register Addresses using 32-bit Offsets

The addresses for many CSRs, such as those that provide control over absolute values, custom video modes, PIO, SIO and strobe output, can vary between cameras. In order to provide a common mechanism across camera models for determining the location of these CSRs relative to the base address, there are fixed locations for inquiry registers that contain offsets, or pointers, to the actual offsets.



To calculate the base address for an offset CSR:

- 1. Query the offset inquiry register.
- 2. Multiple the value by 4. (The value is a 32-bit offset.)
- 3. Remove the 0xF prefix from the result. (i.e., F70000h becomes 70000h)

For example, the Absolute Value CSRs provide minimum, maximum and current real-world values for camera properties such as gain, shutter, etc., as described in *Absolute Value Registers* (below). To determine the location of the shutter absolute value registers (code snippets use function calls included in the FlyCapture SDK, and assume a Camera object cam):

1. Read the ABS\_CSR\_HI\_INQ\_7 register 71Ch to obtain the 32-bit offset for the absolute value CSR for shutter. unsigned int ulValue;

```
cam.ReadRegister(0x71C, &ulValue);
```

- 2. The ulValue is a 32-bit offset, so multiply by 4 to get the actual offset.

  ulValue = ulValue \* 4; // ulValue == 0x3C0244, actual offset == 0xF00910
- 3. The actual offset 0xF00910 represents the offset from the base address 0xFFFF Fxxx xxxx. Since the PGR FlyCapture API automatically takes into account the base offset 0xFFFF F0F0 0000, the actual offset in this example would be 0x910.

```
ulValue = ulValue & 0xFFFF;
```

## C.1.6 Absolute Value Registers

Many Point Grey cameras implement "absolute" modes for various camera settings that report real-world values, such as shutter time in seconds (s) and gain value in decibels (dB). Using these absolute values is easier and more efficient than applying complex conversion formulas to the information in the *Value* field of the associated Control and Status Register. A relative value does not always translate to the same absolute value. Two properties that can affect this relationship are pixel clock frequency and horizontal line frequency. These properties are, in turn, affected by such properties as resolution, frame rate, region of interest (ROI) size and position, and packet size. Additionally, conversion formulas can change between firmware versions. Point Grey therefore recommends using absolute value registers, where possible, to determine camera values.



#### **C.1.6.1** Setting Absolute Value Register Values

For absolute values to be used, the associated feature CSR must be set to use absolute values.

Field	Bit	Description
Abs_Control	[1]	Absolute value control 0: Control with the value in the Value field 1: Control with the value in the Absolute value CSR. If this bit = 1, the value in the Value field is read-only.

In the FlyCapture API, this can also be done by setting the absControl member of the desired property structure to true.

#### C.1.6.2 Absolute Value Offset Addresses

The following set of registers indicates the locations of the absolute value registers. Not all cameras use all registers.



To calculate the base address for an offset CSR:

- 1. Query the offset inquiry register.
- 2. Multiple the value by 4. (The value is a 32-bit offset.)
- 3. Remove the 0xF prefix from the result. (i.e., F70000h becomes 70000h)

#### **32-bit Offsets for Absolute Value Registers**

Offset	Name	Bit	Description
700h	ABS_CSR_HI_INQ_0	[031]	Brightness
704h	ABS_CSR_HI_INQ_1	[031]	Auto Exposure
708h	ABS_CSR_HI_INQ_2	[031]	Sharpness
710h	ABS_CSR_HI_INQ_4	[031]	Hue
714h	ABS_CSR_HI_INQ_5	[031]	Saturation
718h	ABS_CSR_HI_INQ_6	[031]	Gamma
71Ch	ABS_CSR_HI_INQ_7	[031]	Shutter
720h	ABS_CSR_HI_INQ_8	[031]	Gain
724h	ABS_CSR_HI_INQ_9	[031]	Iris
734h	ABS_CSR_HI_INQ_13	[031]	Trigger Delay
73Ch	ABS_CSR_HI_INQ_15	[031]	Frame Rate
7C4h	ABS_CSR_LO_INQ_1	[031]	Pan
7C8h	ABS_CSR_LO_INQ_2	[031]	Tilt



Each set of absolute value CSRs consists of three registers as follows:

Offset	Name	Field	Bit	Description
Base + 000h		Min_Value	[0-31]	Minimum value for this feature. Read only.
Base + 004h	Absolute Value	Max_Value	[0-31]	Maximum value for this feature. Read only.
Base + 008h		Value	[0-31]	Current value of this feature.

#### For example:

Offset	Name	Field	Bit	Description
704h	ABS_CSR_HI_INQ_1		[031]	Auto Exposure.
Base + 0h		Min_Value	[0-31]	Min auto exposure value.
Base + 4h	ABS_VAL_AUTO_EXPOSURE	Max_Value	[0-31]	Max auto exposure value.
Base + 8h		Value	[0-31]	Current auto exposure value.

#### C.1.6.3 Units of Value for Absolute Value CSR Registers

The following tables describe the real-world units that are used for the absolute value registers. Each value is either Absolute (value is an absolute value) or Relative (value is an absolute value, but the reference is system dependent).

Feature	Function	Unit	Unit Description	Reference point	Value Type
Brightness	Black level offset	%			Absolute
Auto Exposure	Auto Exposure	EV	exposure value	0	Relative
Hue	Hue	deg	degree	0	Relative
Saturation	Saturation	%		100	Relative
Shutter	Integration time	S	seconds		Absolute
Gain	Circuit gain	dB	decibel	0	Relative
Iris	Iris	F	F number		Absolute
Trigger_Delay	Trigger Delay	S	seconds		Absolute
Frame_Rate	Frame rate	fps	frames per second		Absolute

#### C.1.6.4 Determining Absolute Value Register Values

The Absolute Value CSRs store 32-bit floating-point values with IEEE/REAL\*4 format. To programmatically determine the floating point equivalents of the minimum, maximum and current hexadecimal values for a property such as shutter, using the FlyCapture SDK:

- 1. Read the ABS\_CSR\_HI\_INQ\_7 register 71Ch to obtain the 32-bit offset for the absolute value CSR for shutter. cam.ReadRegister(context, 0x71C, &ulValue);
- 2. The ulValue is a 32-bit offset, so multiply by 4 to get the actual offset.

  ulValue = ulValue \* 4; // ulValue == 0x3C0244, actual offset == 0xF00910



This offset represents the offset from the base address 0xFFFF Fxxx xxxx. Since the PGR FlyCapture API automatically takes into account the base offset 0xFFFF F0F0 0000, the actual offset in this example would be 0x910.

3. Use the offset obtained to read the min, max and current absolute values and convert the 32-bit hexadecimal values to floating point.

```
// declare a union of a floating point and unsigned long
typedef union _AbsValueConversion
{
      unsigned long ulValue;
      float fValue;
} AbsValueConversion;
float fMinShutter, fMaxShutter, fCurShutter; AbsValueConversion minShutter,
maxShutter, curShutter;
// read the 32-bit hex value into the unsigned long member
cam.ReadRegister(context, 0x910, &minShutter.ulValue);
cam.ReadRegister(context, 0x914, &maxShutter.ulValue);
cam.ReadRegister(context, 0x918, &curShutter.ulValue);
fMinShutter = minShutter.fValue;
fMaxShutter = maxShutter.fValue;
fCurShutter = curShutter.fValue;
```



To get and set absolute values using the FlyCapture SDK, use the GetProperty and SetProperty functions to get or set the absValue member of the Property struct. Refer to the FlyCapture SDK Help for function definitions.

# **C.2** Inquiry Registers

# C.2.1 Basic Functions Inquiry Registers

The following registers show which basic functions are implemented on the camera.

(Bit values = 0: Not Available, 1: Available)



#### Format:

Offset	Name	Field	Bit	Description
		Advanced_Feature_Inq	[0]	Inquiry for advanced feature. (Vendor Unique Features)
		Vmode_Error_Status_Inq	[1]	Inquiry for existence of Vmode_Error_Status register
		Feature_Control_Error_Status_Inq	[2]	Inquiry for existence of Feature_Control_Error_ Status register
		Opt_Func_CSR_Inq	[3]	Inquiry for optional function CSR.
			[4-7]	Reserved
		1394.b_mode_Capability	[8]	Inquiry for 1394.b mode capability
			[9-15]	Reserved
		Cam_Power_Cntl	[16]	Camera process power ON/OFF capability
			[17-18]	Reserved
400h	BASIC_FUNC_INQ	One_Shot_Inq	[19]	One shot transmission capability
40011	BASIC_I ONC_INQ	Multi_Shot_Inq	[20]	Multi shot transmission capability
		Retransmit_Inq	[21]	Retransmit latest image capability (One_ shot/Retransmit)
		Image_Buffer_Inq	[22]	Image buffer capability (Multi_shot/Image_Buffer)
			[23-27]	Reserved
		Memory_Channel	[28-31]	Maximum memory channel number (N) Memory channel 0 = Factory setting memory 1 = Memory Ch 1 2 = Memory Ch 2 : N= Memory Ch N If 0000, user memory is not available.

## **C.2.2** Feature Presence Inquiry Registers

The following registers show the presence of the camera features or optional functions implemented on the camera.

(Bit values = 0: Not Available, 1: Available)



#### Format:

Offset	Name	Field	Bit	Description
		Brightness	[0]	Brightness Control
		Auto_Exposure	[1]	Auto Exposure Control
		Sharpness	[2]	Sharpness Control
		White_Balance	[3]	White Balance Control
		Hue	[4]	Hue Control
		Saturation	[5]	Saturation Control
		Gamma	[6]	Gamma Control
		Shutter	[7]	Shutter Speed Control
404h	Feature_Hi_Inq	Gain	[8]	Gain Control
		Iris	[9]	IRIS Control
		Focus	[10]	Focus Control
		Temperature	[11]	Temperature Control
		Trigger	[12]	Trigger Control
		Trigger_Delay	[13	Trigger Delay Control
		White_Shading	[14]	White Shading Compensation Control
		Frame_Rate	[15]	Frame rate prioritize control
			[16-31]	Reserved
		Zoom	[0]	Zoom Control
		Pan	[1]	Pan Control
		Tilt	[2]	Tilt Control
408h	Footure Le Ing	Optical Filter	[3]	Optical Filter Control
40811	Feature_Lo_Inq		[4-15]	Reserved
		Capture_Size	[16]	Capture image size for Format_6
		Capture_Quality	[17]	Capture image quality for Format_6
			[18-31]	Reserved
		-	[0]	Reserved
		PIO	[1]	Parallel input/output control
40.Ch	Out Function Inc.	SIO	[2]	Serial Input/output control
40Ch	Opt_Function_Inq	Strobe_Output	[3]	Strobe signal output
		Lookup_Table	[4]	Lookup table control
		-	[5-31]	Reserved
410h-47Fh	Reserved			
480h	Advanced_Feature_Inq	Advanced_ Feature_Quadlet_ Offset	[0-31]	32-bit offset of the advanced feature CSRs (see the Advanced Registers section) from the base address of initial register space. (Vendor unique)



Offset	Name	Field	Bit	Description
484h	PIO_Control_CSR_Inq	PIO_Control_ Quadlet_Offset	[0-31]	32-bit offset of the PIO control CSRs (see the Parallel Input/Output (PIO) section) from the base address of initial register space.
488h	SIO_Control_CSR_Inq	SIO_Control_ Quadlet_Offset	[0-31]	32-bit offset of the SIO control CSRs (see the Serial Port Input/Output (SIO) section) from the base address of initial register space.
48Ch	Strobe_Output_CSR_Inq	Strobe_Output_ Quadlet_Offset	[0-31]	32-bit offset of the strobe output signal CSRs (see the Strobe Signal Output section) from the base address of initial register space.
490h	Lookup_Table_CSR_Inq	Lookup_Table_ Quadlet_Offset	[0-31]	32-bit offset of the Lookup Table CSRs from the baes address of initial register space.

# **C.2.3** Feature Elements Inquiry Registers

The following registers show the presence of specific features, modes and minimum and maximum values for each of the camera features or optional functions implemented by the camera.

(Bit values = 0: Not Available, 1: Available)

Offset	Name	Field	Bit	Description	
		Presence_Inq	[0]	Presence of this feature	
		Abs_Control_Inq	[1]	Absolute value control	
			[2]	Reserved	
		One_Push_Inq	[3]	One push mode (controlled automatically only once)	
500h	BRIGHTNESS_INQ	ReadOut_Inq	[4]	Ability to read the value of this feature	
		On_Off_Inq	[5]	Ability to switch feature ON and OFF	
		Auto_Inq	[6]	Auto mode (controlled automatically)	
		Manual_Inq	[7]	Manual mode (controlled by user)	
		Min_Value	[8-19]	Minimum value for this feature control	
		Max_Value	[20-31]	Maximum value for this feature control	
504h	AUTO_EXPOSURE_INQ	Same format as the BRI	GHTNESS <sub>.</sub>	_INQ register	
508h	SHARPNESS_INQ	Same format as the BRI	GHTNESS <sub>.</sub>	_INQ register	
50Ch	WHITE_BALANCE_INQ	Same format as the BRI	GHTNESS <sub>.</sub>	_INQ register	
510h	HUE_INQ	Same format as the BRI	GHTNESS <sub>.</sub>	_INQ register	
514h	SATURATION_INQ	Same format as the BRI	GHTNESS <sub>.</sub>	_INQ register	
518h	GAMMA_INQ	Same format as the BRI	GHTNESS <sub>.</sub>	_INQ register	
51Ch	SHUTTER_INQ	Same format as the BRIGHTNESS_INQ register			
520h	GAIN_INQ	Same format as the BRIGHTNESS_INQ register			
524h	IRIS_INQ	Same format as the BRIGHTNESS_INQ register			
528h	FOCUS_INQ	Same format as the BRIGHTNESS_INQ register			



Offset	Name	Field	Bit	Description		
52Ch	TEMPERATURE_INQ	Same format as the BR	IGHTNESS <sub>.</sub>	_INQ register		
		Presence_Inq	[0]	Presence of this feature		
		Abs_Control_Inq	[1]	Absolute value control		
			[2-3]	Reserved		
		ReadOut_Inq	[4]	Ability to read the value of this feature		
		On_Off_Inq	[5]	Ability to switch feature ON and OFF		
		Polarity_Inq	[6]	Ability to change trigger input polarity		
		Value_Read_Inq	[7]	Ability to read raw trigger input		
		Trigger_Source0_Inq	[8]	Presence of Trigger Source 0 ID=0		
		Trigger_Source1_Inq	[9]	Presence of Trigger Source 1 ID=1		
		Trigger_Source2_Inq	[10]	Presence of Trigger Source 2 ID=2		
		Trigger_Source3_Inq	[11]	Presence of Trigger Source 3 ID=3		
530h	TRIGGER_INQ		[12-14]	Reserved		
	_	Software_Trigger_Inq	[15]	Presence of Software Trigger ID=7		
		Trigger_Mode0_Inq	[16]	Presence of Trigger Mode 0		
		Trigger_Mode1_Inq	[17]	Presence of Trigger Mode 1		
		Trigger_Mode2_Inq	[18]	Presence of Trigger Mode 2		
		Trigger_Mode3_Inq	[19]	Presence of Trigger Mode 3		
		Trigger_Mode4_Inq	[20]	Presence of Trigger Mode 4		
		Trigger_Mode5_Inq	[21]	Presence of Trigger Mode 5		
			[22-29]	Reserved		
		Trigger_Mode14_Inq	[30]	Presence of Trigger Mode 14 (Vendor unique trigger mode 0)		
		Trigger_Mode15_Inq	[31]	Presence of Trigger Mode 15 (Vendor unique trigger mode 1)		
		Presence_Inq	[0]	Presence of this feature		
		Abs_Control_Inq	[1]	Absolute value control		
			[2]	Reserved		
		One_Push_Inq	[3]	One push mode (controlled automatically only once)		
534h	TRIGGER_DLY_INQ	ReadOut_Inq	[4]	Ability to read the value of this feature		
		On_Off_Inq	[5]	Ability to switch feature ON and OFF		
			[6-7]	Reserved		
		Min_Value	[8-19]	Minimum value for this feature control		
		Max_Value	[20-31]	Maximum value for this feature control		
538h	WHITE_SHD_INQ	Same format as the BRIGHTNESS_INQ register				
53Ch	FRAME_RATE_INQ	Same format as the BR	Same format as the BRIGHTNESS_INQ register			



Offset	Name	Field	Bit	Description	
540h					
:	Reserved for other FEATL	JRE_HI_INQ			
57Ch					
580h	ZOOM_INQ	Same format as the BRIGHTNESS_INQ register			
584h	PAN_INQ	Same format as the BRIGHTNESS_INQ register			
588h	TILT_INQ	Same format as the BRIGHTNESS_INQ register			
58Ch	OPTICAL_FILTER_INQ	Same format as the BRIGHTNESS_INQ register			

## **C.2.4** Video Format Inquiry Registers

The following registers may be used to determine the video formats that are available with the camera.

(Bit values = 0: Not Available, 1: Available)

#### Format:

Offset	Name	Field	Bit	Description
		Format_0	[0]	VGA non-compressed format (160x120 through 640x480)
		Format_1 [1]		Super VGA non-compressed format (1) (800x600 through 1024x768)
100h	V_FORMAT_INQ	Format_2	[2]	Super VGA non-compressed format (2) (1280x960 through 1600x1200)
		Format_x	[3-5]	Reserved for other formats
		Format_6	[6]	Still Image Format
		Format_7	[7]	Partial Image Size Format
			[8-31]	Reserved

# C.2.5 Video Mode Inquiry Registers

The following registers may be used to determine the video modes that are available with the camera.

(Bit values = 0: Not Available, 1: Available)



#### Format:

Offset	Name	Field	Bit	Description
		Mode_0	[0]	160 x 120 YUV(4:4:4) Mode (24 bits/pixel)
		Mode_1	[1]	320 x 240 YUV(4:2:2) Mode (16 bits/pixel)
		Mode_2	[2]	640 x 480 YUV(4:1:1) Mode (12 bits/pixel)
100h	V_MODE_INQ_O	Mode_3	[3]	640 x 480 YUV(4:2:2) Mode (16 bits/pixel)
180h	(Format 0)	Mode_4	[4]	640 x 480 RGB Mode (24 bits/pixel)
		Mode_5	[5]	640 x 480 Y8 (Mono) Mode (8 bits/pixel)
		Mode_6	[6]	640 x 480 Y16 (Mono16) Mode (16 bits/pixel)
			[7-31]	Reserved
		Mode_0	[0]	800 x 600 YUV(4:2:2) Mode (16 bits/pixel)
		Mode_1	[1]	800 x 600 RGB Mode (24 bits/pixel)
		Mode_2	[2]	800 x 600 Y (Mono) Mode (8 bits/pixel)
	V_MODE_INQ_1 (Format 1)	Mode_3	[3]	1024 x 768 YUV(4:2:2) Mode (16 bits/pixel)
184h		Mode_4	[4]	1024 x 768 RGB Mode (24 bits/pixel)
		Mode_5	[5]	1024 x 768 Y (Mono) Mode (8 bits/pixel)
		Mode_6	[6]	800 x 600 Y (Mono16) Mode (16 bits/pixel)
		Mode_7	[7]	1024 x 768 Y (Mono16) Mode (16 bits/pixel)
			[8-31]	Reserved
		Mode_0	[0]	1280 x 960 YUV(4:2:2) Mode (16 bits/pixel)
		Mode_1	[1]	1280 x 960 RGB Mode (24 bits/pixel)
		Mode_2	[2]	1280 x 960 Y (Mono) Mode (8 bits/pixel)
	V_MODE_INQ_2	Mode_3	[3]	1600 x 1200 YUV(4:2:2) Mode (16 bits/pixel)
188h		Mode_4	[4]	1600 x 1200 RGB Mode (24 bits/pixel)
	(Format 2)	Mode_5	[5]	1600 x 1200 Y (Mono) Mode (8 bits/pixel)
		Mode_6	[6]	1280 x 960 Y (Mono16) Mode (16 bits/pixel)
		Mode_7	[7]	1600 x 1200 Y (Mono16) Mode (16 bits/pixel)
	_		[8-31]	Reserved
18Ch : 197h	Reserved			



Offset	Name	Field	Bit	Description
		Mode_0	[0]	Format 7 Mode 0
		Mode_1	[1]	Format 7 Mode 1
		Mode_2	[2]	Format 7 Mode 2
	V MODE INQ 7	Mode_3	[3]	Format 7 Mode 3
19Ch		Mode_4	[4]	Format 7 Mode 4
	(Format 7)	Mode_5	[5]	Format 7 Mode 5
		Mode_6	[6]	Format 7 Mode 6
		Mode_7	[7]	Format 7 Mode 7
			[8-31]	Reserved

# **C.2.6** Video Frame Rate Inquiry Registers

This set of registers allows the user to query the available frame rates for all Formats and Modes.

(Bit values = 0: Not Available, 1: Available)

Offset	Name	Field	Bit	Description
		FrameRate_0	[0]	Reserved
		FrameRate_1	[1]	Reserved
		FrameRate_2	[2]	7.5 fps
		FrameRate_3	[3]	15 fps
200h	V_RATE_INQ_0_0 (Format 0, Mode 0)	FrameRate_4	[4]	30 fps
	(i dimat d) made d)	FrameRate_5	[5]	60 fps
		FrameRate_6	[6]	120 fps
		FrameRate_7	[7]	240 fps
			[8-31]	Reserved
		FrameRate_0	[0]	1.875 fps
		FrameRate_1	[1]	3.75 fps
		FrameRate_2	[2]	7.5 fps
		FrameRate_3	[3]	15 fps
204h	V_RATE_INQ_0_1 (Format 0, Mode 1)	FrameRate_4	[4]	30 fps
	(Format o, Wode 1)	FrameRate_5	[5]	60 fps
		FrameRate_6	[6]	120 fps
		FrameRate_7	[7]	240 fps
			[8-31]	Reserved
208h	V_RATE_INQ_0_2 (Format 0, Mode 2)	Same format as V_RATE_INQ_0_1 Register (Format 0, Mode 1)		
20Ch	V_RATE_INQ_0_3 (Format 0, Mode 3)	Same format as V_RATE_INQ_0_1 Register (Format 0, Mode 1)		



Offset	Name	Field	Bit	Description	
210h	V_RATE_INQ_0_4 (Format 0, Mode 4)	Same format as V_RATE	Same format as V_RATE_INQ_0_1 Register (Format 0, Mode 1)		
214h	V_RATE_INQ_0_5 (Format 0, Mode 5)	Same format as V_RATE	:_INQ_0_1 R	legister (Format 0, Mode 1)	
218h	V_RATE_INQ_0_6 (Format 0, Mode 6)	Same format as V_RATE	:_INQ_0_1 R	legister (Format 0, Mode 1)	
21Ch : 21Fh	Reserved				
		FrameRate_0	[0]	Reserved	
		FrameRate_1	[1]	3.75 fps	
		FrameRate_2	[2]	7.5 fps	
		FrameRate_3	[3]	15 fps	
220h	V_RATE_INQ_1_0 (Format 1, Mode 0)	FrameRate_4	[4]	30 fps	
	(i office 1, wode of	FrameRate_5	[5]	60 fps	
		FrameRate_6	[6]	120 fps	
		FrameRate_7	[7]	240 fps	
			[8-31]	Reserved	
224h	V_RATE_INQ_1_1 (Format 1, Mode 1)	Same format as V_RATE_INQ_0_0 Register (Format 0, Mode 0)			
228h	V_RATE_INQ_1_2 (Format 1, Mode 2)	Same format as V_RATE_INQ_0_0 Register (Format 0, Mode 0)			
		FrameRate_0	[0]	1.875 fps	
		FrameRate_1	[1]	3.75 fps	
		FrameRate_2	[2]	7.5 fps	
		FrameRate_3	[3]	15 fps	
22Ch	V_RATE_INQ_1_3 (Format 1, Mode 3)	FrameRate_4	[4]	30 fps	
	(. Sac 2) Mode 3)	FrameRate_5	[5]	60 fps	
		FrameRate_6	[6]	120 fps	
		FrameRate_7	[7]	Reserved	
			[8-31]	Reserved	



Offset	Name	Field	Bit	Description	
		FrameRate_0	[0]	1.875 fps	
		FrameRate_1	[1]	3.75 fps	
		FrameRate_2	[2]	7.5 fps	
		FrameRate_3	[3]	15 fps	
230h	V_RATE_INQ_1_4 (Format 1, Mode 4)	FrameRate_4	[4]	30 fps	
	(Formac 1, Wode 1,	FrameRate_5	[5]	60 fps	
		FrameRate_6	[6]	Reserved	
		FrameRate_7	[7]	Reserved	
			[8-31]	Reserved	
234h	V_RATE_INQ_1_5 (Format 1, Mode 5)	Same format as V_RATE	_INQ_0_1 R	egister (Format 0, Mode 1)	
238h	V_RATE_INQ_1_6 (Format 1, Mode 6)	Same format as V_RATE	_INQ_1_0 re	egister (Format 1, Mode 0)	
23Ch	V_RATE_INQ_1_7 (Format 1, Mode 7)	Same format as V_RATE	_INQ_1_3 re	egister (Format 1, Mode 3)	
240h	V_RATE_INQ_2_0 (Format 2, Mode 0)	Same format as V_RATE_INQ_1_4 register (Format 1, Mode 4)			
244h	V_RATE_INQ_2_1 (Format 2, Mode 1)	Same format as V_RATE_INQ_1_4 register (Format 1, Mode 4)			
248h	V_RATE_INQ_2_2 (Format 2, Mode 2)	Same format as V_RATE_INQ_1_3 register (Format 1, Mode 3)		egister (Format 1, Mode 3)	
24Ch	V_RATE_INQ_2_3 (Format 2, Mode 3)	Same format as V_RATE_INQ_1_4 register (Format 1, Mode 4)			
		FrameRate_0	[0]	1.875 fps	
		FrameRate_1	[1]	3.75 fps	
		FrameRate_2	[2]	7.5 fps	
		FrameRate_3	[3]	15 fps	
250h	V_RATE_INQ_2_4 (Format 2, Mode 4)	FrameRate_4	[4]	30 fps	
	(Format 2, Wode 4)	FrameRate_5	[5]	Reserved	
		FrameRate_6	[6]	Reserved	
		FrameRate_7	[7]	Reserved	
			[8-31]	Reserved	
254h	V_RATE_INQ_2_5 (Format 2, Mode 5)	Same format as V_RATE_INQ_1_3 register (Format 1, Mode 3)			
258h	V_RATE_INQ_2_6 (Format 2, Mode 6)	Same format as V_RATE_INQ_1_4 register (Format 1, Mode 4)			
25Ch	V_RATE_INQ_2_7 (Format 2, Mode 7)	Same format as V_RATE		egister (Format 1, Mode 4)	



2600h         Reserved           287h         2E0h         V_CSR_INQ_7_0         Mode_0         [0-31]         CSR_32-bit offset for Format 7 Mode 0           2E4h         V_CSR_INQ_7_1         Mode_1         [0-31]         CSR_32-bit offset for Format 7 Mode 1           2E8h         V_CSR_INQ_7_2         Mode_2         [0-31]         CSR_32-bit offset for Format 7 Mode 2           2ECh         V_CSR_INQ_7_3         Mode_3         [0-31]         CSR_32-bit offset for Format 7 Mode 3           2F0h         V_CSR_INQ_7_5         Mode_5         [0-31]         CSR_32-bit offset for Format 7 Mode 4           2F4h         V_CSR_INQ_7_6         Mode_6         [0-31]         CSR_32-bit offset for Format 7 Mode 4           2F6h         V_CSR_INQ_7_6         Mode_6         [0-31]         CSR_32-bit offset for Format 7 Mode 6           2F0h         V_CSR_INQ_7_7         Mode_8         [0-31]         CSR_32-bit offset for Format 7 Mode 7           300h         V_CSR_INQ_7_9         Mode_9         [0-31]         CSR_32-bit offset for Format 7 Mode 19           308h         V_CSR_INQ_7_11         Mode_10         [0-31]         CSR_32-bit offset for Format 7 Mode 11           310h         V_CSR_INQ_7_13         Mode_11         [0-31]         CSR_32-bit offset for Format 7 Mode 11           3	Offset	Name	Field	Bit	Description
28Fh         V_CSR_INQ_7_0         Mode_0         [0-31]         CSR_32-bit offset for Format 7 Mode 0           2E4h         V_CSR_INQ_7_1         Mode_1         [0-31]         CSR_32-bit offset for Format 7 Mode 1           2E8h         V_CSR_INQ_7_2         Mode_2         [0-31]         CSR_32-bit offset for Format 7 Mode 2           2E6h         V_CSR_INQ_7_3         Mode_3         [0-31]         CSR_32-bit offset for Format 7 Mode 4           2F0h         V_CSR_INQ_7_4         Mode_4         [0-31]         CSR_32-bit offset for Format 7 Mode 4           2F4h         V_CSR_INQ_7_5         Mode_5         [0-31]         CSR_32-bit offset for Format 7 Mode 5           2F8h         V_CSR_INQ_7_6         Mode_6         [0-31]         CSR_32-bit offset for Format 7 Mode 5           2F0h         V_CSR_INQ_7_7         Mode_7         [0-31]         CSR_32-bit offset for Format 7 Mode 6           2F0h         V_CSR_INQ_7_8         Mode_8         [0-31]         CSR_32-bit offset for Format 7 Mode 9           300h         V_CSR_INQ_7_10         Mode_10         [0-31]         CSR_32-bit offset for Format 7 Mode 9           308h         V_CSR_INQ_7_11         Mode_11         [0-31]         CSR_32-bit offset for Format 7 Mode 10           300h         V_CSR_INQ_7_12         Mode_11         [0-31]	260h		•	•	
2E0h         V_CSR_INQ_7_0         Mode_0         [0-31]         CSR 32-bit offset for Format 7 Mode 0           2E4h         V_CSR_INQ_7_1         Mode_1         [0-31]         CSR 32-bit offset for Format 7 Mode 1           2E8h         V_CSR_INQ_7_2         Mode_2         [0-31]         CSR 32-bit offset for Format 7 Mode 2           2E6h         V_CSR_INQ_7_3         Mode_3         [0-31]         CSR 32-bit offset for Format 7 Mode 3           2F0h         V_CSR_INQ_7_4         Mode_6         [0-31]         CSR 32-bit offset for Format 7 Mode 4           2F4h         V_CSR_INQ_7_5         Mode_6         [0-31]         CSR 32-bit offset for Format 7 Mode 4           2F4h         V_CSR_INQ_7_6         Mode_6         [0-31]         CSR 32-bit offset for Format 7 Mode 6           2F6h         V_CSR_INQ_7_7         Mode_7         [0-31]         CSR 32-bit offset for Format 7 Mode 6           2F6h         V_CSR_INQ_7_8         Mode_8         [0-31]         CSR 32-bit offset for Format 7 Mode 7           300h         V_CSR_INQ_7_10         Mode_10         [0-31]         CSR 32-bit offset for Format 7 Mode 9           308h         V_CSR_INQ_7_11         Mode_11         [0-31]         CSR 32-bit offset for Format 7 Mode 10           300h         V_CSR_INQ_7_11         Mode_11         [0-31]	:	Reserved			
2E4h         V_CSR_INQ_T1         Mode_1         [0-31]         CSR 32-bit offset for Format 7 Mode 1           2E8h         V_CSR_INQ_72         Mode_2         [0-31]         CSR 32-bit offset for Format 7 Mode 2           2ECh         V_CSR_INQ_73         Mode_3         [0-31]         CSR 32-bit offset for Format 7 Mode 3           2F0h         V_CSR_INQ_74         Mode_4         [0-31]         CSR 32-bit offset for Format 7 Mode 4           2F4h         V_CSR_INQ_75         Mode_5         [0-31]         CSR 32-bit offset for Format 7 Mode 5           2F8h         V_CSR_INQ_76         Mode_6         [0-31]         CSR 32-bit offset for Format 7 Mode 7           300h         V_CSR_INQ_77         Mode_8         [0-31]         CSR 32-bit offset for Format 7 Mode 8           304h         V_CSR_INQ_7.9         Mode_9         [0-31]         CSR 32-bit offset for Format 7 Mode 9           308h         V_CSR_INQ_7.10         Mode_10         [0-31]         CSR 32-bit offset for Format 7 Mode 10           30Ch         V_CSR_INQ_7.11         Mode_11         [0-31]         CSR 32-bit offset for Format 7 Mode 11           310h         V_CSR_INQ_7.13         Mode_13         [0-31]         CSR 32-bit offset for Format 7 Mode 12           314h         V_CSR_INQ_7.13         Mode_13         [0-31]		V CCD INO 7 O	Made O	[0.24]	CCD 22 hit offset for Formet 7 Made 0
2E8h         V_CSR_INQ_7_2         Mode_2         [0-31]         CSR 32-bit offset for Format 7 Mode 2           2ECh         V_CSR_INQ_7_3         Mode_3         [0-31]         CSR 32-bit offset for Format 7 Mode 3           2F0h         V_CSR_INQ_7_4         Mode_4         [0-31]         CSR 32-bit offset for Format 7 Mode 4           2F4h         V_CSR_INQ_7_5         Mode_5         [0-31]         CSR 32-bit offset for Format 7 Mode 5           2F8h         V_CSR_INQ_7_6         Mode_6         [0-31]         CSR 32-bit offset for Format 7 Mode 6           2FCh         V_CSR_INQ_7_8         Mode_8         [0-31]         CSR 32-bit offset for Format 7 Mode 7           300h         V_CSR_INQ_7_9         Mode_9         [0-31]         CSR 32-bit offset for Format 7 Mode 8           304h         V_CSR_INQ_7_10         Mode_10         [0-31]         CSR 32-bit offset for Format 7 Mode 10           306h         V_CSR_INQ_7_11         Mode_10         [0-31]         CSR 32-bit offset for Format 7 Mode 10           307h         V_CSR_INQ_7_12         Mode_10         [0-31]         CSR 32-bit offset for Format 7 Mode 11           310h         V_CSR_INQ_7_13         Mode_12         [0-31]         CSR 32-bit offset for Format 7 Mode 12           314h         V_CSR_INQ_7_13         Mode_13         [0-31]<			_		
2ECh         V_CSR_INQ_7_3         Mode_3         [0-31]         CSR 32-bit offset for Format 7 Mode 3           2F0h         V_CSR_INQ_7_4         Mode_4         [0-31]         CSR 32-bit offset for Format 7 Mode 4           2F4h         V_CSR_INQ_7_5         Mode_5         [0-31]         CSR 32-bit offset for Format 7 Mode 5           2F8h         V_CSR_INQ_7_6         Mode_6         [0-31]         CSR 32-bit offset for Format 7 Mode 6           2FCh         V_CSR_INQ_7_7         Mode_7         [0-31]         CSR 32-bit offset for Format 7 Mode 7           300h         V_CSR_INQ_7_9         Mode_8         [0-31]         CSR 32-bit offset for Format 7 Mode 8           304h         V_CSR_INQ_7_10         Mode_9         [0-31]         CSR 32-bit offset for Format 7 Mode 9           308h         V_CSR_INQ_7_11         Mode_10         [0-31]         CSR 32-bit offset for Format 7 Mode 10           300h         V_CSR_INQ_7_11         Mode_11         [0-31]         CSR 32-bit offset for Format 7 Mode 10           300h         V_CSR_INQ_7_12         Mode_12         [0-31]         CSR 32-bit offset for Format 7 Mode 10           300h         V_CSR_INQ_7_13         Mode_13         [0-31]         CSR 32-bit offset for Format 7 Mode 12           314h         V_CSR_INQ_7_13         Mode_13         [0-31]			_		
2FOh         V_CSR_INQ.7.4         Mode_4         [0-31]         CSR 32-bit offset for Format 7 Mode 4           2F4h         V_CSR_INQ.7_5         Mode_5         [0-31]         CSR 32-bit offset for Format 7 Mode 5           2F8h         V_CSR_INQ.7_6         Mode_6         [0-31]         CSR 32-bit offset for Format 7 Mode 6           2FCh         V_CSR_INQ.7_7         Mode_7         [0-31]         CSR 32-bit offset for Format 7 Mode 7           300h         V_CSR_INQ.7_8         Mode_8         [0-31]         CSR 32-bit offset for Format 7 Mode 8           304h         V_CSR_INQ.7_9         Mode_9         [0-31]         CSR 32-bit offset for Format 7 Mode 9           308h         V_CSR_INQ.7_11         Mode_11         [0-31]         CSR 32-bit offset for Format 7 Mode 10           300h         V_CSR_INQ.7_12         Mode_12         [0-31]         CSR 32-bit offset for Format 7 Mode 11           310h         V_CSR_INQ.7_13         Mode_12         [0-31]         CSR 32-bit offset for Format 7 Mode 12           314h         V_CSR_INQ.7_14         Mode_13         [0-31]         CSR 32-bit offset for Format 7 Mode 13           316h         V_CSR_INQ.7_15         Mode_14         [0-31]         CSR 32-bit offset for Format 7 Mode 15           320h         V_CSR_INQ.7_16         Mode_15         [0-3			_		
2F4h         V_CSR_INQ_7_5         Mode_5         [0-31]         CSR 32-bit offset for Format 7 Mode 5           2F8h         V_CSR_INQ_7_6         Mode_6         [0-31]         CSR 32-bit offset for Format 7 Mode 6           2FCh         V_CSR_INQ_7_7         Mode_7         [0-31]         CSR 32-bit offset for Format 7 Mode 7           300h         V_CSR_INQ_7_8         Mode_8         [0-31]         CSR 32-bit offset for Format 7 Mode 8           304h         V_CSR_INQ_7_9         Mode_9         [0-31]         CSR 32-bit offset for Format 7 Mode 9           308h         V_CSR_INQ_7_10         Mode_10         [0-31]         CSR 32-bit offset for Format 7 Mode 10           30Ch         V_CSR_INQ_7_11         Mode_11         [0-31]         CSR 32-bit offset for Format 7 Mode 10           310h         V_CSR_INQ_7_12         Mode_12         [0-31]         CSR 32-bit offset for Format 7 Mode 11           314h         V_CSR_INQ_7_13         Mode_13         [0-31]         CSR 32-bit offset for Format 7 Mode 13           318h         V_CSR_INQ_7_14         Mode_14         [0-31]         CSR 32-bit offset for Format 7 Mode 14           310h         V_CSR_INQ_7_15         Mode_15         [0-31]         CSR 32-bit offset for Format 7 Mode 15           320h         V_CSR_INQ_7_16         Mode_16         [				-	
2F8h         V_CSR_INQ_7_6         Mode_6         [0-31]         CSR 32-bit offset for Format 7 Mode 6           2FCh         V_CSR_INQ_7_7         Mode_7         [0-31]         CSR 32-bit offset for Format 7 Mode 7           300h         V_CSR_INQ_7_8         Mode_8         [0-31]         CSR 32-bit offset for Format 7 Mode 8           304h         V_CSR_INQ_7_9         Mode_9         [0-31]         CSR 32-bit offset for Format 7 Mode 9           308h         V_CSR_INQ_7_10         Mode_10         [0-31]         CSR 32-bit offset for Format 7 Mode 10           30Ch         V_CSR_INQ_7_11         Mode_11         [0-31]         CSR 32-bit offset for Format 7 Mode 11           310h         V_CSR_INQ_7_12         Mode_12         [0-31]         CSR 32-bit offset for Format 7 Mode 11           314h         V_CSR_INQ_7_13         Mode_13         [0-31]         CSR 32-bit offset for Format 7 Mode 13           318h         V_CSR_INQ_7_14         Mode_14         [0-31]         CSR 32-bit offset for Format 7 Mode 14           310h         V_CSR_INQ_7_15         Mode_15         [0-31]         CSR 32-bit offset for Format 7 Mode 15           320h         V_CSR_INQ_7_16         Mode_16         [0-31]         CSR 32-bit offset for Format 7 Mode 15           324h         V_CSR_INQ_7_18         Mode_17 <t< td=""><td></td><td></td><td>_</td><td></td><td></td></t<>			_		
2FCh         V_CSR_INQ_7_7         Mode_7         [0-31]         CSR 32-bit offset for Format 7 Mode 7           300h         V_CSR_INQ_7_8         Mode_8         [0-31]         CSR 32-bit offset for Format 7 Mode 8           304h         V_CSR_INQ_7_9         Mode_9         [0-31]         CSR 32-bit offset for Format 7 Mode 9           308h         V_CSR_INQ_7_10         Mode_10         [0-31]         CSR 32-bit offset for Format 7 Mode 10           30Ch         V_CSR_INQ_7_11         Mode_11         [0-31]         CSR 32-bit offset for Format 7 Mode 11           310h         V_CSR_INQ_7_12         Mode_12         [0-31]         CSR 32-bit offset for Format 7 Mode 12           314h         V_CSR_INQ_7_13         Mode_13         [0-31]         CSR 32-bit offset for Format 7 Mode 13           318h         V_CSR_INQ_7_14         Mode_14         [0-31]         CSR 32-bit offset for Format 7 Mode 14           31Ch         V_CSR_INQ_7_15         Mode_15         [0-31]         CSR 32-bit offset for Format 7 Mode 15           320h         V_CSR_INQ_7_16         Mode_16         [0-31]         CSR 32-bit offset for Format 7 Mode 16           324h         V_CSR_INQ_7_18         Mode_17         [0-31]         CSR 32-bit offset for Format 7 Mode 17           328h         V_CSR_INQ_7_19         Mode_19					
300h         V_CSR_INQ_7_8         Mode_8         [0-31]         CSR 32-bit offset for Format 7 Mode 8           304h         V_CSR_INQ_7_9         Mode_9         [0-31]         CSR 32-bit offset for Format 7 Mode 9           308h         V_CSR_INQ_7_10         Mode_10         [0-31]         CSR 32-bit offset for Format 7 Mode 10           30Ch         V_CSR_INQ_7_11         Mode_11         [0-31]         CSR 32-bit offset for Format 7 Mode 11           310h         V_CSR_INQ_7_12         Mode_12         [0-31]         CSR 32-bit offset for Format 7 Mode 12           314h         V_CSR_INQ_7_13         Mode_13         [0-31]         CSR 32-bit offset for Format 7 Mode 13           318h         V_CSR_INQ_7_14         Mode_14         [0-31]         CSR 32-bit offset for Format 7 Mode 13           310h         V_CSR_INQ_7_15         Mode_15         [0-31]         CSR 32-bit offset for Format 7 Mode 14           310h         V_CSR_INQ_7_16         Mode_16         [0-31]         CSR 32-bit offset for Format 7 Mode 15           320h         V_CSR_INQ_7_17         Mode_16         [0-31]         CSR 32-bit offset for Format 7 Mode 16           324h         V_CSR_INQ_7_18         Mode_17         [0-31]         CSR 32-bit offset for Format 7 Mode 17           328h         V_CSR_INQ_7_19         Mode_18	2F8h		_	[0-31]	CSR 32-bit offset for Format 7 Mode 6
304h V_CSR_INQ_7_10 Mode_19 [0-31] CSR 32-bit offset for Format 7 Mode 9 308h V_CSR_INQ_7_10 Mode_10 [0-31] CSR 32-bit offset for Format 7 Mode 10 30Ch V_CSR_INQ_7_11 Mode_11 [0-31] CSR 32-bit offset for Format 7 Mode 11 310h V_CSR_INQ_7_12 Mode_12 [0-31] CSR 32-bit offset for Format 7 Mode 12 314h V_CSR_INQ_7_13 Mode_13 [0-31] CSR 32-bit offset for Format 7 Mode 13 318h V_CSR_INQ_7_14 Mode_14 [0-31] CSR 32-bit offset for Format 7 Mode 14 31Ch V_CSR_INQ_7_15 Mode_15 [0-31] CSR 32-bit offset for Format 7 Mode 14 31Ch V_CSR_INQ_7_16 Mode_16 [0-31] CSR 32-bit offset for Format 7 Mode 15 320h V_CSR_INQ_7_16 Mode_16 [0-31] CSR 32-bit offset for Format 7 Mode 16 324h V_CSR_INQ_7_17 Mode_17 [0-31] CSR 32-bit offset for Format 7 Mode 17 328h V_CSR_INQ_7_18 Mode_18 [0-31] CSR 32-bit offset for Format 7 Mode 18 32Ch V_CSR_INQ_7_19 Mode_19 [0-31] CSR 32-bit offset for Format 7 Mode 19 330h V_CSR_INQ_7_20 Mode_20 [0-31] CSR 32-bit offset for Format 7 Mode 20 334h V_CSR_INQ_7_21 Mode_21 [0-31] CSR 32-bit offset for Format 7 Mode 20 334h V_CSR_INQ_7_21 Mode_21 [0-31] CSR 32-bit offset for Format 7 Mode 21 338h V_CSR_INQ_7_21 Mode_21 [0-31] CSR 32-bit offset for Format 7 Mode 22 33Ch V_CSR_INQ_7_23 Mode_22 [0-31] CSR 32-bit offset for Format 7 Mode 23 340h V_CSR_INQ_7_24 Mode_24 [0-31] CSR 32-bit offset for Format 7 Mode 24 344h V_CSR_INQ_7_25 Mode_25 [0-31] CSR 32-bit offset for Format 7 Mode 25 348h V_CSR_INQ_7_26 Mode_26 [0-31] CSR 32-bit offset for Format 7 Mode 26 34Ch V_CSR_INQ_7_26 Mode_26 [0-31] CSR 32-bit offset for Format 7 Mode 27 350h V_CSR_INQ_7_28 Mode_28 [0-31] CSR 32-bit offset for Format 7 Mode 27 350h V_CSR_INQ_7_28 Mode_29 [0-31] CSR 32-bit offset for Format 7 Mode 29 358h V_CSR_INQ_7_29 Mode_29 [0-31] CSR 32-bit offset for Format 7 Mode 29 358h V_CSR_INQ_7_29 Mode_29 [0-31] CSR 32-bit offset for Format 7 Mode 29	2FCh	V_CSR_INQ_7_7	Mode_7	[0-31]	CSR 32-bit offset for Format 7 Mode 7
308h         V_CSR_INQ_7_10         Mode_10         [0-31]         CSR 32-bit offset for Format 7 Mode 10           30Ch         V_CSR_INQ_7_11         Mode_11         [0-31]         CSR 32-bit offset for Format 7 Mode 11           310h         V_CSR_INQ_7_12         Mode_12         [0-31]         CSR 32-bit offset for Format 7 Mode 12           314h         V_CSR_INQ_7_13         Mode_13         [0-31]         CSR 32-bit offset for Format 7 Mode 13           318h         V_CSR_INQ_7_14         Mode_14         [0-31]         CSR 32-bit offset for Format 7 Mode 14           31Ch         V_CSR_INQ_7_15         Mode_15         [0-31]         CSR 32-bit offset for Format 7 Mode 15           320h         V_CSR_INQ_7_16         Mode_16         [0-31]         CSR 32-bit offset for Format 7 Mode 16           324h         V_CSR_INQ_7_17         Mode_17         [0-31]         CSR 32-bit offset for Format 7 Mode 17           328h         V_CSR_INQ_7_18         Mode_18         [0-31]         CSR 32-bit offset for Format 7 Mode 18           32Ch         V_CSR_INQ_7_21         Mode_19         [0-31]         CSR 32-bit offset for Format 7 Mode 19           330h         V_CSR_INQ_7_20         Mode_20         [0-31]         CSR 32-bit offset for Format 7 Mode 20           334h         V_CSR_INQ_7_21         Mode_21 <td>300h</td> <td>V_CSR_INQ_7_8</td> <td>Mode_8</td> <td>[0-31]</td> <td>CSR 32-bit offset for Format 7 Mode 8</td>	300h	V_CSR_INQ_7_8	Mode_8	[0-31]	CSR 32-bit offset for Format 7 Mode 8
30Ch         V_CSR_INQ_7_11         Mode_11         [0-31]         CSR 32-bit offset for Format 7 Mode 11           310h         V_CSR_INQ_7_12         Mode_12         [0-31]         CSR 32-bit offset for Format 7 Mode 12           314h         V_CSR_INQ_7_13         Mode_13         [0-31]         CSR 32-bit offset for Format 7 Mode 13           318h         V_CSR_INQ_7_14         Mode_14         [0-31]         CSR 32-bit offset for Format 7 Mode 14           31Ch         V_CSR_INQ_7_15         Mode_15         [0-31]         CSR 32-bit offset for Format 7 Mode 15           320h         V_CSR_INQ_7_16         Mode_16         [0-31]         CSR 32-bit offset for Format 7 Mode 16           324h         V_CSR_INQ_7_17         Mode_17         [0-31]         CSR 32-bit offset for Format 7 Mode 17           328h         V_CSR_INQ_7_18         Mode_18         [0-31]         CSR 32-bit offset for Format 7 Mode 18           32Ch         V_CSR_INQ_7_19         Mode_19         [0-31]         CSR 32-bit offset for Format 7 Mode 19           330h         V_CSR_INQ_7_20         Mode_20         [0-31]         CSR 32-bit offset for Format 7 Mode 20           334h         V_CSR_INQ_7_21         Mode_21         [0-31]         CSR 32-bit offset for Format 7 Mode 21           336h         V_CSR_INQ_7_22         Mode_22 <td>304h</td> <td>V_CSR_INQ_7_9</td> <td>Mode_9</td> <td>[0-31]</td> <td>CSR 32-bit offset for Format 7 Mode 9</td>	304h	V_CSR_INQ_7_9	Mode_9	[0-31]	CSR 32-bit offset for Format 7 Mode 9
310h         V_CSR_INQ_7_12         Mode_12         [0-31]         CSR 32-bit offset for Format 7 Mode 12           314h         V_CSR_INQ_7_13         Mode_13         [0-31]         CSR 32-bit offset for Format 7 Mode 13           318h         V_CSR_INQ_7_14         Mode_14         [0-31]         CSR 32-bit offset for Format 7 Mode 14           31ch         V_CSR_INQ_7_15         Mode_15         [0-31]         CSR 32-bit offset for Format 7 Mode 15           320h         V_CSR_INQ_7_16         Mode_16         [0-31]         CSR 32-bit offset for Format 7 Mode 16           324h         V_CSR_INQ_7_17         Mode_17         [0-31]         CSR 32-bit offset for Format 7 Mode 17           328h         V_CSR_INQ_7_18         Mode_18         [0-31]         CSR 32-bit offset for Format 7 Mode 18           32ch         V_CSR_INQ_7_19         Mode_19         [0-31]         CSR 32-bit offset for Format 7 Mode 19           330h         V_CSR_INQ_7_20         Mode_20         [0-31]         CSR 32-bit offset for Format 7 Mode 20           334h         V_CSR_INQ_7_21         Mode_21         [0-31]         CSR 32-bit offset for Format 7 Mode 21           336h         V_CSR_INQ_7_22         Mode_22         [0-31]         CSR 32-bit offset for Format 7 Mode 22           340h         V_CSR_INQ_7_23         Mode_23 <td>308h</td> <td>V_CSR_INQ_7_10</td> <td>Mode_10</td> <td>[0-31]</td> <td>CSR 32-bit offset for Format 7 Mode 10</td>	308h	V_CSR_INQ_7_10	Mode_10	[0-31]	CSR 32-bit offset for Format 7 Mode 10
314h   V_CSR_INQ_7_13   Mode_13   [0-31]   CSR 32-bit offset for Format 7 Mode 13   318h   V_CSR_INQ_7_14   Mode_14   [0-31]   CSR 32-bit offset for Format 7 Mode 14   31Ch   V_CSR_INQ_7_15   Mode_15   [0-31]   CSR 32-bit offset for Format 7 Mode 15   320h   V_CSR_INQ_7_16   Mode_16   [0-31]   CSR 32-bit offset for Format 7 Mode 16   324h   V_CSR_INQ_7_17   Mode_17   [0-31]   CSR 32-bit offset for Format 7 Mode 17   328h   V_CSR_INQ_7_18   Mode_18   [0-31]   CSR 32-bit offset for Format 7 Mode 18   32Ch   V_CSR_INQ_7_19   Mode_19   [0-31]   CSR 32-bit offset for Format 7 Mode 19   330h   V_CSR_INQ_7_20   Mode_20   [0-31]   CSR 32-bit offset for Format 7 Mode 20   334h   V_CSR_INQ_7_21   Mode_21   [0-31]   CSR 32-bit offset for Format 7 Mode 21   338h   V_CSR_INQ_7_22   Mode_22   [0-31]   CSR 32-bit offset for Format 7 Mode 22   33Ch   V_CSR_INQ_7_23   Mode_23   [0-31]   CSR 32-bit offset for Format 7 Mode 23   340h   V_CSR_INQ_7_24   Mode_24   [0-31]   CSR 32-bit offset for Format 7 Mode 24   344h   V_CSR_INQ_7_25   Mode_25   [0-31]   CSR 32-bit offset for Format 7 Mode 25   348h   V_CSR_INQ_7_26   Mode_26   [0-31]   CSR 32-bit offset for Format 7 Mode 26   34Ch   V_CSR_INQ_7_27   Mode_27   [0-31]   CSR 32-bit offset for Format 7 Mode 26   34Ch   V_CSR_INQ_7_28   Mode_28   [0-31]   CSR 32-bit offset for Format 7 Mode 27   350h   V_CSR_INQ_7_29   Mode_29   [0-31]   CSR 32-bit offset for Format 7 Mode 29   358h   V_CSR_INQ_7_29   Mode_29   [0-31]   CSR 32-bit offset for Format 7 Mode 29   358h   V_CSR_INQ_7_29   Mode_29   [0-31]   CSR 32-bit offset for Format 7 Mode 29   358h   V_CSR_INQ_7_30   Mode_30   [0-31]   CSR 32-bit offset for Format 7 Mode 29   358h   V_CSR_INQ_7_30   Mode_30   [0-31]   CSR 32-bit offset for Format 7 Mode 29   358h   V_CSR_INQ_7_30   Mode_30   [0-31]   CSR 32-bit offset for Format 7 Mode 29   358h   V_CSR_INQ_7_30   Mode_30   [0-31]   CSR 32-bit offset for Format 7 Mode 29   358h   V_CSR_INQ_7_30   Mode_30   [0-31]   CSR 32-bit offset for Format 7 Mode 29   358h   V_CSR_INQ_7_30   Mode	30Ch	V_CSR_INQ_7_11	Mode_11	[0-31]	CSR 32-bit offset for Format 7 Mode 11
318h         V_CSR_INQ_7_14         Mode_14         [0-31]         CSR 32-bit offset for Format 7 Mode 14           31Ch         V_CSR_INQ_7_15         Mode_15         [0-31]         CSR 32-bit offset for Format 7 Mode 15           320h         V_CSR_INQ_7_16         Mode_16         [0-31]         CSR 32-bit offset for Format 7 Mode 16           324h         V_CSR_INQ_7_17         Mode_17         [0-31]         CSR 32-bit offset for Format 7 Mode 17           328h         V_CSR_INQ_7_18         Mode_18         [0-31]         CSR 32-bit offset for Format 7 Mode 18           32Ch         V_CSR_INQ_7_19         Mode_19         [0-31]         CSR 32-bit offset for Format 7 Mode 19           330h         V_CSR_INQ_7_20         Mode_20         [0-31]         CSR 32-bit offset for Format 7 Mode 20           334h         V_CSR_INQ_7_21         Mode_21         [0-31]         CSR 32-bit offset for Format 7 Mode 21           338h         V_CSR_INQ_7_22         Mode_22         [0-31]         CSR 32-bit offset for Format 7 Mode 22           340h         V_CSR_INQ_7_23         Mode_23         [0-31]         CSR 32-bit offset for Format 7 Mode 23           340h         V_CSR_INQ_7_24         Mode_24         [0-31]         CSR 32-bit offset for Format 7 Mode 23           340h         V_CSR_INQ_7_25         Mode_25 <td>310h</td> <td>V_CSR_INQ_7_12</td> <td>Mode_12</td> <td>[0-31]</td> <td>CSR 32-bit offset for Format 7 Mode 12</td>	310h	V_CSR_INQ_7_12	Mode_12	[0-31]	CSR 32-bit offset for Format 7 Mode 12
31Ch         V_CSR_INQ_7_15         Mode_15         [0-31]         CSR 32-bit offset for Format 7 Mode 15           320h         V_CSR_INQ_7_16         Mode_16         [0-31]         CSR 32-bit offset for Format 7 Mode 16           324h         V_CSR_INQ_7_17         Mode_17         [0-31]         CSR 32-bit offset for Format 7 Mode 17           328h         V_CSR_INQ_7_18         Mode_18         [0-31]         CSR 32-bit offset for Format 7 Mode 18           32Ch         V_CSR_INQ_7_19         Mode_19         [0-31]         CSR 32-bit offset for Format 7 Mode 19           330h         V_CSR_INQ_7_20         Mode_20         [0-31]         CSR 32-bit offset for Format 7 Mode 20           334h         V_CSR_INQ_7_21         Mode_21         [0-31]         CSR 32-bit offset for Format 7 Mode 21           338h         V_CSR_INQ_7_22         Mode_22         [0-31]         CSR 32-bit offset for Format 7 Mode 22           33Ch         V_CSR_INQ_7_23         Mode_23         [0-31]         CSR 32-bit offset for Format 7 Mode 23           340h         V_CSR_INQ_7_24         Mode_24         [0-31]         CSR 32-bit offset for Format 7 Mode 24           344h         V_CSR_INQ_7_25         Mode_25         [0-31]         CSR 32-bit offset for Format 7 Mode 25           348h         V_CSR_INQ_7_26         Mode_26 <td>314h</td> <td>V_CSR_INQ_7_13</td> <td>Mode_13</td> <td>[0-31]</td> <td>CSR 32-bit offset for Format 7 Mode 13</td>	314h	V_CSR_INQ_7_13	Mode_13	[0-31]	CSR 32-bit offset for Format 7 Mode 13
320h         V_CSR_INQ_7_16         Mode_16         [0-31]         CSR 32-bit offset for Format 7 Mode 16           324h         V_CSR_INQ_7_17         Mode_17         [0-31]         CSR 32-bit offset for Format 7 Mode 17           328h         V_CSR_INQ_7_18         Mode_18         [0-31]         CSR 32-bit offset for Format 7 Mode 18           32Ch         V_CSR_INQ_7_19         Mode_19         [0-31]         CSR 32-bit offset for Format 7 Mode 19           330h         V_CSR_INQ_7_20         Mode_20         [0-31]         CSR 32-bit offset for Format 7 Mode 20           334h         V_CSR_INQ_7_21         Mode_21         [0-31]         CSR 32-bit offset for Format 7 Mode 21           338h         V_CSR_INQ_7_22         Mode_22         [0-31]         CSR 32-bit offset for Format 7 Mode 22           33Ch         V_CSR_INQ_7_23         Mode_23         [0-31]         CSR 32-bit offset for Format 7 Mode 23           340h         V_CSR_INQ_7_24         Mode_24         [0-31]         CSR 32-bit offset for Format 7 Mode 24           344h         V_CSR_INQ_7_25         Mode_25         [0-31]         CSR 32-bit offset for Format 7 Mode 25           348h         V_CSR_INQ_7_26         Mode_26         [0-31]         CSR 32-bit offset for Format 7 Mode 26           34Ch         V_CSR_INQ_7_27         Mode_27 <td>318h</td> <td>V_CSR_INQ_7_14</td> <td>Mode_14</td> <td>[0-31]</td> <td>CSR 32-bit offset for Format 7 Mode 14</td>	318h	V_CSR_INQ_7_14	Mode_14	[0-31]	CSR 32-bit offset for Format 7 Mode 14
324h         V_CSR_INQ_7_17         Mode_17         [0-31]         CSR 32-bit offset for Format 7 Mode 17           328h         V_CSR_INQ_7_18         Mode_18         [0-31]         CSR 32-bit offset for Format 7 Mode 18           32Ch         V_CSR_INQ_7_19         Mode_19         [0-31]         CSR 32-bit offset for Format 7 Mode 19           330h         V_CSR_INQ_7_20         Mode_20         [0-31]         CSR 32-bit offset for Format 7 Mode 20           334h         V_CSR_INQ_7_21         Mode_21         [0-31]         CSR 32-bit offset for Format 7 Mode 21           338h         V_CSR_INQ_7_22         Mode_22         [0-31]         CSR 32-bit offset for Format 7 Mode 22           33Ch         V_CSR_INQ_7_23         Mode_23         [0-31]         CSR 32-bit offset for Format 7 Mode 23           340h         V_CSR_INQ_7_24         Mode_24         [0-31]         CSR 32-bit offset for Format 7 Mode 24           344h         V_CSR_INQ_7_25         Mode_25         [0-31]         CSR 32-bit offset for Format 7 Mode 25           348h         V_CSR_INQ_7_26         Mode_26         [0-31]         CSR 32-bit offset for Format 7 Mode 26           34Ch         V_CSR_INQ_7_27         Mode_27         [0-31]         CSR 32-bit offset for Format 7 Mode 27           350h         V_CSR_INQ_7_28         Mode_29 <td>31Ch</td> <td>V_CSR_INQ_7_15</td> <td>Mode_15</td> <td>[0-31]</td> <td>CSR 32-bit offset for Format 7 Mode 15</td>	31Ch	V_CSR_INQ_7_15	Mode_15	[0-31]	CSR 32-bit offset for Format 7 Mode 15
328h         V_CSR_INQ_7_18         Mode_18         [0-31]         CSR 32-bit offset for Format 7 Mode 18           32Ch         V_CSR_INQ_7_19         Mode_19         [0-31]         CSR 32-bit offset for Format 7 Mode 19           330h         V_CSR_INQ_7_20         Mode_20         [0-31]         CSR 32-bit offset for Format 7 Mode 20           334h         V_CSR_INQ_7_21         Mode_21         [0-31]         CSR 32-bit offset for Format 7 Mode 21           338h         V_CSR_INQ_7_22         Mode_22         [0-31]         CSR 32-bit offset for Format 7 Mode 22           33Ch         V_CSR_INQ_7_23         Mode_23         [0-31]         CSR 32-bit offset for Format 7 Mode 23           340h         V_CSR_INQ_7_24         Mode_24         [0-31]         CSR 32-bit offset for Format 7 Mode 24           344h         V_CSR_INQ_7_25         Mode_25         [0-31]         CSR 32-bit offset for Format 7 Mode 25           348h         V_CSR_INQ_7_26         Mode_26         [0-31]         CSR 32-bit offset for Format 7 Mode 26           340h         V_CSR_INQ_7_27         Mode_27         [0-31]         CSR 32-bit offset for Format 7 Mode 27           350h         V_CSR_INQ_7_28         Mode_28         [0-31]         CSR 32-bit offset for Format 7 Mode 28           354h         V_CSR_INQ_7_29         Mode_29 <td>320h</td> <td>V_CSR_INQ_7_16</td> <td>Mode_16</td> <td>[0-31]</td> <td>CSR 32-bit offset for Format 7 Mode 16</td>	320h	V_CSR_INQ_7_16	Mode_16	[0-31]	CSR 32-bit offset for Format 7 Mode 16
32Ch         V_CSR_INQ_7_19         Mode_19         [0-31]         CSR 32-bit offset for Format 7 Mode 19           330h         V_CSR_INQ_7_20         Mode_20         [0-31]         CSR 32-bit offset for Format 7 Mode 20           334h         V_CSR_INQ_7_21         Mode_21         [0-31]         CSR 32-bit offset for Format 7 Mode 21           338h         V_CSR_INQ_7_22         Mode_22         [0-31]         CSR 32-bit offset for Format 7 Mode 22           33Ch         V_CSR_INQ_7_23         Mode_23         [0-31]         CSR 32-bit offset for Format 7 Mode 23           340h         V_CSR_INQ_7_24         Mode_24         [0-31]         CSR 32-bit offset for Format 7 Mode 24           344h         V_CSR_INQ_7_25         Mode_25         [0-31]         CSR 32-bit offset for Format 7 Mode 25           348h         V_CSR_INQ_7_26         Mode_26         [0-31]         CSR 32-bit offset for Format 7 Mode 26           34Ch         V_CSR_INQ_7_27         Mode_27         [0-31]         CSR 32-bit offset for Format 7 Mode 27           350h         V_CSR_INQ_7_28         Mode_28         [0-31]         CSR 32-bit offset for Format 7 Mode 28           354h         V_CSR_INQ_7_29         Mode_29         [0-31]         CSR 32-bit offset for Format 7 Mode 29           358h         V_CSR_INQ_7_30         Mode_29 <td>324h</td> <td>V_CSR_INQ_7_17</td> <td>Mode_17</td> <td>[0-31]</td> <td>CSR 32-bit offset for Format 7 Mode 17</td>	324h	V_CSR_INQ_7_17	Mode_17	[0-31]	CSR 32-bit offset for Format 7 Mode 17
330h V_CSR_INQ_7_20 Mode_20 [0-31] CSR 32-bit offset for Format 7 Mode 20  334h V_CSR_INQ_7_21 Mode_21 [0-31] CSR 32-bit offset for Format 7 Mode 21  338h V_CSR_INQ_7_22 Mode_22 [0-31] CSR 32-bit offset for Format 7 Mode 22  33Ch V_CSR_INQ_7_23 Mode_23 [0-31] CSR 32-bit offset for Format 7 Mode 23  340h V_CSR_INQ_7_24 Mode_24 [0-31] CSR 32-bit offset for Format 7 Mode 24  344h V_CSR_INQ_7_25 Mode_25 [0-31] CSR 32-bit offset for Format 7 Mode 25  348h V_CSR_INQ_7_26 Mode_26 [0-31] CSR 32-bit offset for Format 7 Mode 26  34Ch V_CSR_INQ_7_27 Mode_27 [0-31] CSR 32-bit offset for Format 7 Mode 26  350h V_CSR_INQ_7_28 Mode_28 [0-31] CSR 32-bit offset for Format 7 Mode 28  354h V_CSR_INQ_7_29 Mode_29 [0-31] CSR 32-bit offset for Format 7 Mode 29  358h V_CSR_INQ_7_30 Mode_30 [0-31] CSR 32-bit offset for Format 7 Mode 30	328h	V_CSR_INQ_7_18	Mode_18	[0-31]	CSR 32-bit offset for Format 7 Mode 18
334h         V_CSR_INQ_7_21         Mode_21         [0-31]         CSR 32-bit offset for Format 7 Mode 21           338h         V_CSR_INQ_7_22         Mode_22         [0-31]         CSR 32-bit offset for Format 7 Mode 22           33Ch         V_CSR_INQ_7_23         Mode_23         [0-31]         CSR 32-bit offset for Format 7 Mode 23           340h         V_CSR_INQ_7_24         Mode_24         [0-31]         CSR 32-bit offset for Format 7 Mode 24           344h         V_CSR_INQ_7_25         Mode_25         [0-31]         CSR 32-bit offset for Format 7 Mode 25           348h         V_CSR_INQ_7_26         Mode_26         [0-31]         CSR 32-bit offset for Format 7 Mode 26           34Ch         V_CSR_INQ_7_27         Mode_27         [0-31]         CSR 32-bit offset for Format 7 Mode 27           350h         V_CSR_INQ_7_28         Mode_28         [0-31]         CSR 32-bit offset for Format 7 Mode 28           354h         V_CSR_INQ_7_29         Mode_29         [0-31]         CSR 32-bit offset for Format 7 Mode 29           358h         V_CSR_INQ_7_30         Mode_30         [0-31]         CSR 32-bit offset for Format 7 Mode 30	32Ch	V_CSR_INQ_7_19	Mode_19	[0-31]	CSR 32-bit offset for Format 7 Mode 19
338h       V_CSR_INQ_7_22       Mode_22       [0-31]       CSR 32-bit offset for Format 7 Mode 22         33Ch       V_CSR_INQ_7_23       Mode_23       [0-31]       CSR 32-bit offset for Format 7 Mode 23         340h       V_CSR_INQ_7_24       Mode_24       [0-31]       CSR 32-bit offset for Format 7 Mode 24         344h       V_CSR_INQ_7_25       Mode_25       [0-31]       CSR 32-bit offset for Format 7 Mode 25         348h       V_CSR_INQ_7_26       Mode_26       [0-31]       CSR 32-bit offset for Format 7 Mode 26         34Ch       V_CSR_INQ_7_27       Mode_27       [0-31]       CSR 32-bit offset for Format 7 Mode 27         350h       V_CSR_INQ_7_28       Mode_28       [0-31]       CSR 32-bit offset for Format 7 Mode 28         354h       V_CSR_INQ_7_29       Mode_29       [0-31]       CSR 32-bit offset for Format 7 Mode 29         358h       V_CSR_INQ_7_30       Mode_30       [0-31]       CSR 32-bit offset for Format 7 Mode 30	330h	V_CSR_INQ_7_20	Mode_20	[0-31]	CSR 32-bit offset for Format 7 Mode 20
33Ch V_CSR_INQ_7_23 Mode_23 [0-31] CSR 32-bit offset for Format 7 Mode 23  340h V_CSR_INQ_7_24 Mode_24 [0-31] CSR 32-bit offset for Format 7 Mode 24  344h V_CSR_INQ_7_25 Mode_25 [0-31] CSR 32-bit offset for Format 7 Mode 25  348h V_CSR_INQ_7_26 Mode_26 [0-31] CSR 32-bit offset for Format 7 Mode 26  34Ch V_CSR_INQ_7_27 Mode_27 [0-31] CSR 32-bit offset for Format 7 Mode 27  350h V_CSR_INQ_7_28 Mode_28 [0-31] CSR 32-bit offset for Format 7 Mode 28  354h V_CSR_INQ_7_29 Mode_29 [0-31] CSR 32-bit offset for Format 7 Mode 29  358h V_CSR_INQ_7_30 Mode_30 [0-31] CSR 32-bit offset for Format 7 Mode 30	334h	V_CSR_INQ_7_21	Mode_21	[0-31]	CSR 32-bit offset for Format 7 Mode 21
340h       V_CSR_INQ_7_24       Mode_24       [0-31]       CSR 32-bit offset for Format 7 Mode 24         344h       V_CSR_INQ_7_25       Mode_25       [0-31]       CSR 32-bit offset for Format 7 Mode 25         348h       V_CSR_INQ_7_26       Mode_26       [0-31]       CSR 32-bit offset for Format 7 Mode 26         34Ch       V_CSR_INQ_7_27       Mode_27       [0-31]       CSR 32-bit offset for Format 7 Mode 27         350h       V_CSR_INQ_7_28       Mode_28       [0-31]       CSR 32-bit offset for Format 7 Mode 28         354h       V_CSR_INQ_7_29       Mode_29       [0-31]       CSR 32-bit offset for Format 7 Mode 29         358h       V_CSR_INQ_7_30       Mode_30       [0-31]       CSR 32-bit offset for Format 7 Mode 30	338h	V_CSR_INQ_7_22	Mode_22	[0-31]	CSR 32-bit offset for Format 7 Mode 22
344h       V_CSR_INQ_7_25       Mode_25       [0-31]       CSR 32-bit offset for Format 7 Mode 25         348h       V_CSR_INQ_7_26       Mode_26       [0-31]       CSR 32-bit offset for Format 7 Mode 26         34Ch       V_CSR_INQ_7_27       Mode_27       [0-31]       CSR 32-bit offset for Format 7 Mode 27         350h       V_CSR_INQ_7_28       Mode_28       [0-31]       CSR 32-bit offset for Format 7 Mode 28         354h       V_CSR_INQ_7_29       Mode_29       [0-31]       CSR 32-bit offset for Format 7 Mode 29         358h       V_CSR_INQ_7_30       Mode_30       [0-31]       CSR 32-bit offset for Format 7 Mode 30	33Ch	V_CSR_INQ_7_23	Mode_23	[0-31]	CSR 32-bit offset for Format 7 Mode 23
348h         V_CSR_INQ_7_26         Mode_26         [0-31]         CSR 32-bit offset for Format 7 Mode 26           34Ch         V_CSR_INQ_7_27         Mode_27         [0-31]         CSR 32-bit offset for Format 7 Mode 27           350h         V_CSR_INQ_7_28         Mode_28         [0-31]         CSR 32-bit offset for Format 7 Mode 28           354h         V_CSR_INQ_7_29         Mode_29         [0-31]         CSR 32-bit offset for Format 7 Mode 29           358h         V_CSR_INQ_7_30         Mode_30         [0-31]         CSR 32-bit offset for Format 7 Mode 30	340h	V_CSR_INQ_7_24	Mode_24	[0-31]	CSR 32-bit offset for Format 7 Mode 24
34Ch       V_CSR_INQ_7_27       Mode_27       [0-31]       CSR 32-bit offset for Format 7 Mode 27         350h       V_CSR_INQ_7_28       Mode_28       [0-31]       CSR 32-bit offset for Format 7 Mode 28         354h       V_CSR_INQ_7_29       Mode_29       [0-31]       CSR 32-bit offset for Format 7 Mode 29         358h       V_CSR_INQ_7_30       Mode_30       [0-31]       CSR 32-bit offset for Format 7 Mode 30	344h	V_CSR_INQ_7_25	Mode_25	[0-31]	CSR 32-bit offset for Format 7 Mode 25
350h       V_CSR_INQ_7_28       Mode_28       [0-31]       CSR 32-bit offset for Format 7 Mode 28         354h       V_CSR_INQ_7_29       Mode_29       [0-31]       CSR 32-bit offset for Format 7 Mode 29         358h       V_CSR_INQ_7_30       Mode_30       [0-31]       CSR 32-bit offset for Format 7 Mode 30	348h	V_CSR_INQ_7_26	Mode_26	[0-31]	CSR 32-bit offset for Format 7 Mode 26
350h         V_CSR_INQ_7_28         Mode_28         [0-31]         CSR 32-bit offset for Format 7 Mode 28           354h         V_CSR_INQ_7_29         Mode_29         [0-31]         CSR 32-bit offset for Format 7 Mode 29           358h         V_CSR_INQ_7_30         Mode_30         [0-31]         CSR 32-bit offset for Format 7 Mode 30	34Ch		Mode_27	[0-31]	CSR 32-bit offset for Format 7 Mode 27
354h       V_CSR_INQ_7_29       Mode_29       [0-31]       CSR 32-bit offset for Format 7 Mode 29         358h       V_CSR_INQ_7_30       Mode_30       [0-31]       CSR 32-bit offset for Format 7 Mode 30	350h	V_CSR_INQ_7_28	Mode_28	[0-31]	CSR 32-bit offset for Format 7 Mode 28
358h V_CSR_INQ_7_30 Mode_30 [0-31] CSR 32-bit offset for Format 7 Mode 30	354h	V_CSR_INQ_7_29	Mode_29	[0-31]	CSR 32-bit offset for Format 7 Mode 29
	358h		_		CSR 32-bit offset for Format 7 Mode 30
	35Ch	V_CSR_INQ_7_31	Mode_31	[0-31]	CSR 32-bit offset for Format 7 Mode 31



# **C.3** General Camera Operation

The following settings control general status and monitoring of the camera:

- Memory Channel Registers (below)
- Device Information (on page 130)
- Camera Memory (on page 132)
- Firmware Information (on page 134)

# **C.3.1** Memory Channel Registers

The values of the following registers are saved in memory channels.

Register Name	Offset
CURRENT_FRAME_RATE	600h
CURRENT_VIDEO_MODE	604h
CURRENT_VIDEO_FORMAT	608h
CAMERA_POWER	610h
CUR_SAVE_CH	620h
BRIGHTNESS	800h
AUTO_EXPOSURE	804h
SHARPNESS	808h
WHITE_BALANCE	80Ch
HUE	810h
SATURATION	814h
GAMMA	818h
SHUTTER	81Ch
GAIN	820h
IRIS	824h
FOCUS	828h
TRIGGER_MODE	830h
TRIGGER_DELAY	834h
FRAME_RATE	83Ch
PAN	884h
TILT	888h
ABS_VAL_AUTO_EXPOSURE	908h
ABS_VAL_SHUTTER	918h
ABS_VAL_GAIN	928h
ABS_VAL_BRIGHTNESS	938h
ABS_VAL_GAMMA	948h



Register Name	Offset
ABS_VAL_TRIGGER_DELAY	958h
ABS_VAL_FRAME_RATE	968h
IMAGE_DATA_FORMAT	1048h
AUTO_EXPOSURE_RANGE	1088h
AUTO_SHUTTER_RANGE	1098h
AUTO_GAIN_RANGE	10A0h
GPIO_XTRA	1104h
SHUTTER_DELAY	1108h
GPIO_STRPAT_CTRL	110Ch
GPIO_CTRL_PIN_x	1110h, 1120h, 1130h, 1140h
GPIO_XTRA_PIN_x	1114h, 1124h, 1134h, 1144h
GPIO_STRPAT_MASK_PIN_x	1118h, 1128h, 1138h, 1148h
FRAME_INFO	12F8h
IMAGE_POSITION	008h
IMAGE_SIZE	00Ch
COLOR_CODING_ID	010h
UDP_PORT	1F1Ch
DESTINATION_IP	1F34h
GVCP Configuration (includes Heartbeat Disable) (GigE Vision Bootstrap Register)	0954h (no offset)
Stream Channel Packet Size (GigE Vision Bootstrap Register)	0D04h (no offset)
Stream Channel Packet Delay (GigE Vision Bootstrap Register)	0D08h (no offset)
Heartbeat Timeout (GigE Vision Bootstrap Register)	0938h (no offset)

## C.3.1.1 MEMORY\_SAVE: 618h

#### Format:

Field	Bit	Description
Memory_Save	[0]	1 = Current status modes are saved to MEM_SAVE_CH (Self cleared)
	[1-31]	Reserved

#### C.3.1.2 MEM\_SAVE\_CH: 620h

#### Format:

Field	Bit	Description
Mem_Save_Ch	[0-3]	Write channel for Memory_Save command.  Shall be >=0001 (0 is for factory default settings)  See BASIC_FUNC_INQ register.
	[4-31]	Reserved



### C.3.1.3 CUR\_MEM\_CH: 624h

#### Format:

Field	Bit	Description				
Cur_Mem_Ch	[0-3]	Read: The current memory channel number Write: Loads the camera status, modes and values from the specified memory channel.				
	[4-31]	Reserved				

### C.3.2 Device Information CSRs

In addition to the GenICam Device Control features in the camera's XML file, the following registers are available for device and status monitoring:

**Voltage**—This allows the user to access and monitor the input as well as several of the internal voltages of the cameras.

Current — This allows the user to access and monitor the current consumption of the camera.

**Camera Power**—Allows the user to power up or power down the camera.

**Pixel Clock Frequency**—This specifies the current pixel clock frequency (in Hz) in IEEE-754 32-bit floating point format. The camera pixel clock defines an upper limit to the rate at which pixels can be read off the image sensor.

**Horizontal Line Frequency**—This specifies the current horizontal line frequency in Hz in IEEE-754 32-bit floating point format.

### C.3.2.1 SERIAL\_NUMBER: 1F20h

Field	Bit	Description
Serial_Number	[0-31]	Unique serial number of camera (read-only)



### C.3.2.2 MAIN\_BOARD\_INFO: 1F24h

### Format:

Field	Bit		Description
Major_Board_Design	[0-11]	0x6: Ladybug Head 0x7: Ladybug Base Unit 0x10: Flea 0x18: Dragonfly2 0x19: Flea2 0x1A: Firefly MV 0x1C: Bumblebee2 0x1F: Grasshopper 0x22: Grasshopper2 0x21: Flea2G-13S2 0x24: Flea2G-50S5 0x26: Chameleon	0x27: Grasshopper Express 0x29: Flea3 FireWire 14S3/20S4 0x2A: Flea3 FireWire 03S3 0x2B: Flea3 FireWire 03S1 0x2F: Flea3 GigE 14S3/20S4 0x32: Flea3 GigE 13S2 0x34: Flea3 USB 3.0 0x36: Zebra2 0x39: Flea3 GigE 03S2/08S2 0x3E: Flea3 GigE 50S5 0x3F: Flea3 GigE 28S4 0x40: Flea3 GigE 03S1
Minor_Board_Rev	[12-15]	Internal use	
Reserved	[16-31]	Reserved	

### C.3.2.3 VOLTAGE: 1A50h - 1A54h

### Format:

Offset	Name	Field	Bit	Description
	Presence_Inq	[0]	Presence of this feature 0: Not available, 1: Available	
1A50h	1A50h VOLTAGE_LO_INQ	-	[1-7]	Reserved
			[8-19]	Number of voltage registers supported
		-	[20-31]	Reserved
1A54h	VOLTAGE_HI_INQ		[0-31]	32-bit offset of the voltage CSRs, which report the current voltage in Volts using the 32-bit floating-point IEEE/REAL*4 format.

### C.3.2.4 CURRENT: 1A58h - 1A5Ch

Offset	Name	Field	Bit	Description
	Presence_ Inq	[0]	Presence of this feature 0: Not available, 1: Available	
1A58h	A58h CURRENT_ LO_INQ		[1-7]	Reserved
			[8-19]	Number of current registers supported
			[20-31]	Reserved
1A5Ch	CURRENT_ HI_INQ		[0-31]	32-bit offset of the current registers, which report the current in amps using the 32-bit floating-point IEEE/REAL*4 format.



### C.3.2.5 TEMPERATURE: 82Ch

#### Format:

Field	Bit	Description
Presence_Inq	[0]	Presence of this feature 0: Not Available, 1: Available
	[1-19]	Reserved
Value	[20-31]	Value. In Kelvin (0°C = 273.15K) in increments of one-tenth (0.1) of a Kelvin

### C.3.2.6 CAMERA\_POWER: 610h

#### Format:

Field	Bit	Description
Cam_Pwr_Ctrl	[0]	Read: 0: Camera is powered down, or in the process of powering up (i.e., bit will be zero until camera completely powered up ), 1: Camera is powered up  Write: 0: Begin power-down process, 1: Begin power-up process
	[1-30]	Reserved
Camera_Power_Status	ower_Status [31] Read only Read: the pending value of Cam_Pwr_Ctrl	

### C.3.2.7 PIXEL\_CLOCK\_FREQ: 1AF0h

#### Format:

Field	Bit	Description
Pixel_Clock_Freq	[0-31]	Pixel clock frequency in Hz (read-only).

### C.3.2.8 HORIZONTAL\_LINE\_FREQ: 1AF4h

#### Format:

Field	Bit	Description
Horizontal_Line_Freq	[0-31]	Horizontal line frequency in Hz (read-only).

### C.3.3 Camera Memory

### C.3.3.1 DATA\_FLASH\_CTRL: 1240h

This register controls access to the camera's on-board flash memory. Each bit in the data flash is initially set to 1.

The user can transfer as much data as necessary to the offset address (1244h), then perform a single write to the control register to commit the data to flash. Any modified data is committed by writing to this register, or by accessing any other control register.



Field	Bit	Description
Presence_Inq	[0]	Presence of this feature 0: Not Available, 1: Available
	[1-5]	Reserved
Clean_Page	[6]	Read: 0: Page is dirty, 1: Page is clean  Write: 0: No-op, 1: Write page to data flash
	[7]	Reserved
Page_Size	[8-19]	8 == 256 byte page 9 == 512 byte page
Num_Pages	[20-31]	11 == 2048 pages 13 == 8192 pages

### C.3.3.2 DATA\_FLASH\_DATA: 1244h

This register provides the 32-bit offset to the start of where the data is stored in the flash memory.

#### Format:

Offset	Field	Bit	Description
1244h	DF_Data	[0-31]	32-bit offset to the start of data

### C.3.3.3 IMAGE\_RETRANSMIT: 634h

This register provides an interface to the camera's frame buffer functionality.

Transmitting buffered data is available when continuous shot is disabled. Either One shot or Multi shot can be used to transmit buffered data when *Transfer\_Data\_Select* = 1. Multi shot is used for transmitting one or more (as specified by *Count\_Number*) buffered images. One shot is used for retransmission of the last image from the retransmit buffer.



For GenICam features, One shot is the same as Single Frame and Multi shot is the same as Multi Frame.

Image data is stored in a circular image buffer when *Image\_Buffer\_Ctrl* = 1. If the circular buffer overflows, the oldest image in the buffer is overwritten.

Transmitted data is always stored in the retransmit buffer. If a last or previous image does not exist, (for example, an image has not been acquired since a video format or mode change), the camera still transmits an image from the retransmit buffer, but its contents are undefined.

The image buffer is initialized when *Image\_Buffer\_Ctr* is written to '1'. Changing the video format, video mode, image\_size, or color\_coding causes the image buffer to be initialized and *Max\_Num\_Images* to be updated.



Field	Bit	Description
Image_Buffer_Ctrl	[0]	Image Buffer On/Off Control 0: OFF, 1: ON
Transfer_Data_Select	[1]	Transfer data path 0: Live data, 1: Buffered image data Ignored if ISO_EN=1
	[2-7]	Reserved
Max_Num_Images	[8-19]	Maximum number of images that can be stored in the current video format. Must be greater than zero. This field is read only.
Number_of_Images	[20-31]	The number of images currently in buffer. This field is read only.

### C.3.4 Firmware Information

### C.3.4.1 FIRMWARE\_VERSION: 1F60h

This register contains the version information for the currently loaded camera firmware.

#### Format:

Field	Bit	Description	
Major	[0-7]	Major revision number	
Minor	[8-15]	Minor revision number	
Туре	[16-19]	Type of release: 0: Alpha 1: Beta 2: Release Candidate 3: Release	
Revision	[20-31]	Revision number	

### C.3.4.2 FIRMWARE\_BUILD\_DATE: 1F64h

### Format:

Field	Bit	Description
Build_Date	[0-31]	Date the current firmware was built in Unix time format (read-only)

### C.3.4.3 FIRMWARE\_DESCRIPTION: 1F68-1F7Ch

Null padded, big-endian string describing the currently loaded version of firmware.

## C.4 Input/Output Control

The following settings are used for input/output control:



- GPIO Pin Control (below)
- GPIO Xtra Control (for Pulse Width Modulation) (on next page)
- GPIO Strobe Control Registers (on next page)
- Strobe Output Registers (on page 138)
- Serial Communication Registers (on page 139)
- Debouncer Control (on page 143)

### C.4.1 GPIO\_CTRL\_PIN: 1110h-1140h

These registers provide control over the GPIO pins.

Pin	Register		
0	GPIO_CTRL_PIN_0	1110h	
1	GPIO_CTRL_PIN_1	1120h	
2	GPIO_CTRL_PIN_2	1130h	
3	GPIO_CTRL_PIN_3	1140h	

Field	Bit	Description		
Presence_Inq	[0]	Presence of this feature 0: Not Available, 1: Available		
	[1-11]	Reserved		
Pin_Mode  [12-15]  Current GPIO Mode:  0: Input 1: Output 2: Asynchronous Trigger 3: Strobe 4: Pulse width modulation (PWM)		0: Input 1: Output 2: Asynchronous Trigger		
	[16-30]	For Modes 0, 1, and 2: Reserved For Mode 4 (PWM:) see below		
Data	[31]	For Modes 0, 1, and 2: Data field  0 = 0 V (falling edge), 1 = +3.3 V (rising edge)  For Mode 4 (PWM): see below		
Pwm_Count [16-23] Read: The c does not au Write: Writi		Number of PWM pulses  Read: The current count; counts down the remaining pulses. After reaching zero, the count does not automatically reset to the previously-written value.  Write: Writing the number of pulses starts the PWM. Write 0xFF for infinite pulses. (Requires write of 0x00 before writing a different value.)		
	[24]	Reserved		
En_Pin	The GPIO pin to be used as a PWM enable i.e. the PWM continues as long a held in a certain state (high or low).			
	[28]	Reserved		



Field	Bit	Description	
Disable_Pol	[29]	Polarity of the PWM enable pin (En_Pin) that will disable the PWM. If this bit is 0, the PWM is disabled when the PWM enable pin goes low.	
En_En	[30]	0: Disable enable pin (En_Pin) functionality 1: Enable En_Pin functionality	
Pwm_Pol	[31]	Polarity of the PWM signal 0: Low, 1: High	

### C.4.2 GPIO\_XTRA\_PIN: 1114h-1144h

These registers contain mode specific data for the GPIO pins. Units are ticks of a 1.024MHz clock.

Pin	Register		
0	GPIO_XTRA_PIN_0	1114h	
1	GPIO_XTRA_PIN_1	1124h	
2	GPIO_XTRA_PIN_2	1134h	
3	GPIO_XTRA_PIN_3	1144h	

#### Format:

Field	Bit	Description	
Mode_Specific_1	[0-15]	GPIO_MODE_4: Low period of PWM pulse (if Pwm_Pol = 0)	
Mode_Specific_2	[16-31]	GPIO_MODE_4: High period of PWM pulse (if Pwm_Pol = 0)	

### C.4.3 GPIO\_STRPAT\_CTRL: 110Ch

This register provides control over a shared 4-bit counter with programmable period. When the *Current\_Count* equals N a GPIO pin will only output a strobe pulse if bit[N] of the GPIO\_STRPAT\_MASK\_PIN\_x register's *Enable\_Pin* field is set to '1'.

Field	Bit	Description	
Presence_Inq	[0]	Presence of this feature 0: Not Available, 1: Available	
	[1-18]	Reserved	
Count_Period	[19-23]	Controls the period of the strobe pattern Valid values: 116	
	[24-27]	Reserved	
Current_Count	[28-31]	Read-only  The value of the bit index defined in GPIO_x_STRPAT_MASK that will be used during the next image's strobe. <i>Current_Count</i> increments at the same time at the strobe start signal occurs.	



### C.4.4 GPIO\_STRPAT\_MASK\_PIN: 1118h-1148h

These registers define the actual strobe pattern to be implemented by GPIO pins in conjunction with the *Count\_Period* defined in GPIO STRPAT CTRL register 110Ch.

For example, if *Count\_Period* is set to '3', bits 16-18 of the *Enable\_Mask* can be used to define a strobe pattern. An example strobe pattern might be bit 16=0, bit 17=0, and bit 18=1, which will cause a strobe to occur every three frames (when the *Current\_Count* is equal to 2).

Pin	Register	
0	GPIO_STRPAT_MASK_PIN_0	1118h
1	GPIO_STRPAT_MASK_PIN_1	1128h
2	GPIO_STRPAT_MASK_PIN_2	1138h
3	GPIO_STRPAT_MASK_PIN_3	1148h

#### Format:

Field	Bit	Description	
Presence_Inq	[0]	Presence of this feature 0: Not Available, 1: Available	
	[1-15]	Reserved	
Enable_Mask	[16-31]	Bit field representing the strobe pattern used in conjunction with <i>Count_Period</i> in GPIO_STRPAT_CTRL	
		0: Do not output a strobe, 1: Output a strobe	

### C.4.5 GPIO\_XTRA: 1104h

The GPIO\_XTRA register controls when a strobe starts: relative to the start of integration (default) or relative to the time of an asynchronous trigger.

Field	Bit	Description	
Strobe_Start	[0]	O: Strobe start is relative to start of integration (default)  1: Strobe start is relative to external trigger	
	[1-31]	Reserved Reserved	



### **C.4.6** Strobe Output Registers



To calculate the base address for an offset CSR:

- 1. Query the offset inquiry register.
- 2. Multiple the value by 4. (The value is a 32-bit offset.)
- 3. Remove the 0xF prefix from the result. (i.e., F70000h becomes 70000h)

Offset	Name	Field	Bit	Description
48Ch	STROBE_ OUTPUT_CSR_ INQ	Strobe_Output_ Quadlet_Offset	[0-31]	32-bit offset of the Strobe output signal CSRs from the base address of initial register space
		Strobe_0_Inq	[0]	Presence of strobe 0 signal
		Strobe_1_Inq	[1]	Presence of strobe 1 signal
Base + Oh	STROBE_CTRL_ INQ	Strobe_2_Inq	[2]	Presence of strobe 2 signal
		Strobe_3_Inq	[3]	Presence of strobe 3 signal
		-	[4-31]	Reserved
		Presence_Inq	[0]	Presence of this feature
			[1-3]	Reserved
		ReadOut_Inq	[4]	Ability to read the value of this feature
Base +	CTRODE O INO	On_Off_Inq	[5]	Ability to switch feature ON and OFF
100h	STROBE_0_INQ	Polarity_Inq	[6]	Ability to change signal polarity
			[7]	Reserved
		Min_Value	[8-19]	Minimum value for this feature control
		Max_Value	[20-31]	Maximum value for this feature control
Base + 104h	STROBE_1_INQ	Same definition as Strobe_0_Inq		
Base + 108h	STROBE_2_INQ	Same definition as Strobe_0_Inq		
Base + 10Ch	STROBE_3_INQ	Same definition as Strobe_0_Inq		



Offset	Name	Field	Bit	Description	
		Presence_Inq	[0]	Presence of this feature 0: Not Available, 1: Available	
			[1-5]	Reserved	
		On_Off	[6]	Read: read a status Write: ON or OFF this function  0: OFF, 1: ON If this bit = 0, other fields will be read only.  When ON, strobe signals continue to output after the camera stops streaming images. To stop strobe output, this bit must be explicitly turned OFF.	
Base + 200h	STROBE_0_CNT	Signal_Polarity	[7]	Select signal polarity  If Polarity_Inq = 1:  Read to get strobe output polarity  Write to change strobe output polarity  If Polarity_Inq = 0, then Read only  0: Low active output, 1: High active output	
		Delay_Value	[8-19]	Delay after start of exposure until the strobe signal asserts	
		Duration_Value	[20-31]	Duration of the strobe signal  A value of 0 means de-assert at the end of exposure, if required.	
Base + 204h	STROBE_1_CNT	Same definition as Strobe_0_ Cnt			
Base + 208h	STROBE_2_CNT	Same definition as St	robe_0_Cn	t	
Base + 20Ch	STROBE_3_CNT	Same definition as Strobe_0_Cnt			

### C.4.7 Serial Input/Output Registers

This section describes the control and inquiry registers for the serial input/output (SIO) control functionality.



To calculate the base address for an offset CSR:

- 1. Query the offset inquiry register.
- 2. Multiple the value by 4. (The value is a 32-bit offset.)
- 3. Remove the 0xF prefix from the result. (i.e., F70000h becomes 70000h)



Offset	Name	Field	Bit	Description
488h	SIO_CONTROL_ CSR_INQ	SIO_ Control_ Quadlet_ Offset	[0-31]	32-bit offset of the SIO CSRs from the base address of initial register space
Base + Oh	SERIAL_MODE_ REG	Baud_Rate	[0-7]	Read: Get current baud rate Write: Set baud rate  0: 300 bps 1: 600 bps 2: 1200 bps 3: 2400 bps 4: 4800 bps 5: 9600 bps 6: 19200 bps 7: 38400 bps 8: 57600 bps 9: 115200 bps 10: 230400 bps Other values reserved
		Char_ Length	[8-15]	Character length setting  Read: Get data length  Write: Set data length (must not be 0)  7: 7 bits, 8: 8 bits  Other values reserved
		Parity	[16-17]	Parity setting  Read: Get current parity  Write: Set parity  0: None, 1: Odd, 2: Even
		Stop_Bit	[18-19]	Stop bits  Read: Get current stop bit  Write: Set stop bit  0: 1, 1: 1.5, 2: 2
			[20-23]	Reserved
		Buffer_ Size_Inq	[24-31]	Buffer Size (Read-Only)  This field indicates the maximum size of the receive/transmit data buffer. See also SIO Buffers on page 47  If this value=1, Buffer_Status_Control and SIO_Data_Register characters 1-3 should be ignored.



Offset	Name	Field	Bit	Description
				Receive enable
Base + 4h	SERIAL_ CONTROL_REG	RE	[0]	Indicates if the camera's ability to receive data has been enabled. Enabling this register causes the receive capability to be immediately started. Disabling this register causes the data in the buffer to be flushed.
				Read: Current status Write: 0 Disable, 1: Enable
				Transmit enable
		TE	[1]	Indicates if the camera's ability to transmit data has been enabled. Enabling this register causes the transmit capability to be immediately started. Disabling this register causes data transmission to stop immediately, and any pending data is discarded.  Read: Current status
				Write: 0: Disable, 1: Enable
		-	[2-7]	Reserved
	SERIAL_ STATUS_REG	TDRD	[8]	Transmit data buffer ready (read only)  Indicates if the transmit buffer is ready to receive data from the user. It will be in the Ready state as long as TBUF_ST != 0 and TE is enabled.  Read only  0: Not ready, 1: Ready
		-	[9]	Reserved
		RDRD	[10]	Receive data buffer ready (read only)  Indicates if the receive buffer is ready to be read by the user. It will be in the Ready state as long as RBUF_ST != 0 and RE is enabled.  Read only  0: Not ready, 1: Ready
			[11]	Reserved
		-	[11]	Receive buffer over run error
		ORER	[12]	Read: Current status Write: 0: Clear flag, 1: Ignored
		FER	[13]	Receive data framing error  Read: Current status  Write: 0: Clear flag, 1: Ignored
		PER	[14]	Receive data parity error  Read: Current status  Write: 0: Clear flag, 1: Ignored
		-	[15-31]	Reserved



Offset	Name	Field	Bit	Description
				SIO receive buffer status
Base + 8h	RECEIVE_ BUFFER_ STATUS_ CONTROL	RBUF_ST	[0-8]	Indicates the number of bytes that have arrived at the camera but have yet to be queued to be read.  Read: Valid data size of current receive buffer Write: Ignored
				SIO receive buffer control
		RBUF_CNT	[8-15]	Indicates the number of bytes that are ready to be read.
				Read: Remaining data size for read Write: Set input data size
		-	[16-31]	Reserved
				SIO output buffer status
Base + Ch	TRANSMIT_ BUFFER_ STATUS_ CONTROL	TBUF_ST	[0-8]	Indicates the minimum number of free bytes available to be filled in the transmit buffer. It will count down as bytes are written to any of the SIO_DATA_REGISTERs starting at 2100h. It will count up as bytes are actually transmitted after a write to <i>TBUF_CNT</i> . Although its maximum value is 255, the actual amount of available buffer space may be larger.
				Read: Available data space of transmit buffer Write: Ignored
		TBUF_CNT	[8-15]	Indicates the number of bytes that have been stored since it was last written to. Writing any value to TBUF_CNT will cause it to go to 0. Writing a number less than its value will cause that many bytes to be transmitted and the rest thrown away. Writing a number greater than its value will cause that many bytes to be written - its value being valid and the remainder being padding.
				Read: Written data size to buffer Write: Set output data size for transmit.
		-	[16-31]	Reserved
Base + 100h	SIO_DATA_ REGISTER	Char_0	[0-7]	Character_0  Read: Read character from receive buffer. Padding data if data is not available.  Write: Write character to transmit buffer. Padding data if data is invalid.
		Char_1	[8-16]	Character_1  Read: Read character from receive buffer+1. Padding data if data is not available.  Write: Write character to transmit buffer+1. Padding data if data is
				invalid.



Offset	Name	Field	Bit	Description
		Char_2	[17-23]	Character_2  Read: Read character from receive buffer+2. Padding data if data is not available.  Write: Write character to transmit buffer+2. Padding data if data is invalid.
		Char_3	[24-31]	Character_3  Read: Read character from receive buffer+3. Padding data if data is not available.  Write: Write character to transmit buffer+3. Padding data if data is invalid.
Base + 104h : Base + 1FFh	SIO_DATA_ REGISTER_ALIAS		[0-31]	Alias SIO_Data_Register area for block transfer.

## C.4.8 DEBOUNCER\_CTRL

These registers provide control over the debouncer.



The DEBOUNCER\_INQ registers allows for the presence of the debouncer on all eight GPIO pins. However, the debouncer feature only works on GPIO input pins: GPIO0, GPIO2, and GPIO3.

### C.4.8.1 DEBOUNCER\_INQ: 0x11fch

Field	Bit	Description
Presence_Inq	[0]	Presence of this feature 0: Not Available, 1: Available
Debouncer_0_Inq	[1]	Presence of the debouncer on GPIO_0
Debouncer_1_Inq	[2]	Presence of the debouncer on GPIO_1
Debouncer_2_Inq	[3]	Presence of the debouncer on GPIO_2
Debouncer_3_Inq	[4]	Presence of the debouncer on GPIO_3
Debouncer_4_Inq	[5]	Presence of the debouncer on GPIO_4
Debouncer_5_Inq	[6]	Presence of the debouncer on GPIO_5
Debouncer_6_Inq	[7]	Presence of the debouncer on GPIO_6
Debouncer_7_Inq	[8]	Presence of the debouncer on GPIO_7
	[9-10]	Reserved
Min_Value	[11]	Minimum value for debouncer control in microseconds. Must be greater than or equal to 1 microsecond.



Field	Bit	Description
Max_Value	[12-31]	Maximum value for debouncer control in microseconds. Must be less than or equal to 1 second.

### C.4.8.2 DEBOUNCER\_X\_CTRL: 0x111c - 0x118c

Register	
DEBOUNCER_O_CTRL	0x111c
DEBOUNCER_1_CTRL	0x112c
DEBOUNCER_2_CTRL	0x113c
DEBOUNCER_3_CTRL	0x114c
DEBOUNCER_4_CTRL	0x115c
DEBOUNCER_5_CTRL	0x116c
DEBOUNCER_6_CTRL	0x117c
DEBOUNCER_7_CTRL	0x118c

#### Format:

Field	Bit	Description
Presence_Inq	[0]	Presence of this feature 0: Not Available, 1: Available
	[1-5]	Reserved
On_Off [6]		Read: read a status Write: ON or OFF this function  0 = OFF; 1 = ON  If this bit = 0, other fields will be read only.
	[7-11]	Reserved
Debouncer_Value	[12-31]	Debouncer value in microseconds.  When Debounce_Value = 0 or On_Off is set to OFF, the camera defaults to using a value of 16 ticks of the current pixel clock.

## C.5 Video Format, Mode, and Frame Rate Settings

The following settings control the video format and mode of the camera.

Frame Rate — This provides control over the frame rate of the camera. When this feature is in auto mode, exposure time is limited by the frame rate value dynamically, which is determined by the Current Frame Rate. When this feature is in manual mode, the actual frame interval (time between individual image acquisitions) is fixed by the frame rate value. The available frame rate range depends on the current video format and/or video mode.

This is set to OFF when the camera is operating in asynchronous trigger mode. For more information, see Asynchronous Triggering on page 68.

Current Frame Rate—Allows the user to query and modify the current frame rate of the camera.



Current Video Mode—Allows the user to query and modify the current video mode of the camera.

**Current Video Format** — Allows the user to query and modify the current video format of the camera. Note: GigE Vision cameras only operate in Format 7.

### C.5.1 FRAME\_RATE: 83Ch



Formulas for converting the fixed point (relative) values to floating point (absolute) values are not provided. Users wishing to work with real-world values should refer to Absolute Value CSRs (page 114).

#### Format:

Field	Bit	Description	
Presence_Inq	[0]	Presence of this feature  0: Not Available, 1: Available	
		Absolute value control	
Abs_Control	[1]	0: Control in the Value field, 1: Control in the Absolute value CSR.	
		If this bit = 1, the value in the Value field is read-only.	
	[2-4]	Reserved	
		One push auto mode (controlled automatically only once)	
One_Push	[5]	Read: 0: Not in operation, 1: In operation Write: 1: Begin to work (self-cleared after operation)	
		If A_M_Mode = 1, this bit is ignored	
ON OFF	[6]	Read: read a status Write: ON or OFF for this feature	
ON_OFF	[6]	0: OFF, 1: ON If this bit = 0, other fields will be read only	
A_M_Mode	[7]	Read: read a current mode Write: set the mode	
		0: Manual, 1: Automatic	
	[8-19] Reserved		
Value	[20-31]	Value. A write to this value in 'Auto' mode will be ignored.	

#### **Related Resources**

Title	Link
FlyCapture SDK ExtendedShutterEx sample program	ExtendedShutterEx



### C.5.2 CURRENT\_FRAME\_RATE: 600h

### Format:

Field	Bit	Description
Cur_V_Frm_Rate	[0-2]	Current frame rate FrameRate_0 FrameRate_7
	[3-31]	Reserved.

### C.5.3 CURRENT\_VIDEO\_MODE: 604h

#### Format:

Field	Bit	Description
Cur_V_Mode	[0-3]	Current video mode Mode_0 Mode_8
	[4-31]	Reserved.

### C.5.4 CURRENT\_VIDEO\_FORMAT: 608h

#### Format:

Field	Bit	Description
Cur_V_Format	[0-2]	Current video format Format_0 Format_7  Note: GigE Vision cameras operate only in Format 7 mode.
	[3-31]	Reserved.

### C.5.5 FORMAT\_7\_RESIZE\_INQ: 1AC8h

This register reports all internal camera processes being used to generate images in the current video mode. For example, users can read this register to determine if pixel binning and/or subsampling is being used to achieve a non-standard custom image size.

This register is read-only.

Field	Bit	Description
Presence_Inq	[0]	Presence of this feature 0: Not Available, 1: Available
	[1-7]	Reserved
Num_Cols	[8-11]	Number of columns being binned/subsampled, minus 1 (e.g., if combining 4 columns together, this register will report a value of 3)



Field	Bit	Description
Num_Rows	[12-15]	Number of rows binned/subsampled, minus 1 (e.g., if combining 4 columns together, this register will report a value of 3)
	[16-23]	Reserved
V_Pre_Color	[24]	Vertical subsampling/downsampling performed before color processing 0: Off, 1: On
H_Pre_Color	[25]	Horizontal subsampling/downsampling performed before color processing 0: Off, 1: On
V_Post_Color	[26]	Vertical subsampling/downsampling performed after color processing 0: Off, 1: On
H_Post_Color	[27]	Horizontal subsampling/downsampling performed after color processing 0: Off, 1: On
V_Bin	[28]	Standard vertical binning (addition of adjacent lines within horizontal shift register) 0: Off, 1: On
H_Bin	[29]	Standard horizontal binning (addition of adjacent lines within horizontal shift register) 0: Off, 1: On
V_Bayer_Bin	[30]	Vertical bayer binning (addition of adjacent even/odd lines within the interline transfer buffer) 0: Off, 1: On
H_Bayer_Bin	[31]	Horizontal bayer binning (addition of adjacent even/odd columns within the horizontal shift register)  0: Off, 1: On

## C.5.6 Inquiry Registers for Custom Video Mode Offset Addresses

The following set of registers indicates the locations of the custom video mode base registers. These offsets are relative to the base offset 0xFFFF F0F0 0000.

Table C.2: Custom Video Mode Inquiry Register Offset Addresses

Offset	Name	Field	Bit	Description
2E0h	V_CSR_INQ_7_0	Mode_0	[0-31]	32-bit offset for Mode 0
2E4h	V_CSR_INQ_7_1	Mode_1	[0-31]	32-bit offset for Mode 1
2E8h	V_CSR_INQ_7_2	Mode_2	[0-31]	32-bit offset for Mode 2
2ECh	V_CSR_INQ_7_3	Mode_3	[0-31]	32-bit offset for Mode 3
2F0h	V_CSR_INQ_7_4	Mode_4	[0-31]	32-bit offset for Mode 4
2F4h	V_CSR_INQ_7_5	Mode_5	[0-31]	32-bit offset for Mode 5
2F8h	V_CSR_INQ_7_6	Mode_6	[0-31]	32-bit offset for Mode 6
2FCh	V_CSR_INQ_7_7	Mode_7	[0-31]	32-bit offset for Mode 7
300h	V_CSR_INQ_7_8	Mode_8	[0-31]	32-bit offset for Mode 8





To calculate the base address for an offset CSR:

- 1. Query the offset inquiry register.
- 2. Multiple the value by 4. (The value is a 32-bit offset.)
- 3. Remove the 0xF prefix from the result. (i.e., F70000h becomes 70000h)

### C.5.6.1 Image Size and Position

These registers are inquiry registers for maximum image size and unit size, and to determine an area of required data.

#### Format:

Address	Name	Field	Bit	Description
Base +	144 V 1844 OF SIZE 1840	Hmax	[0-15]	Maximum horizontal pixel number Hmax = Hunit * n = Hposunit*n3 (n, n3 are integers)
000h	MAX_IMAGE_SIZE_INQ	Vmax	[16-31]	Maximum vertical pixel number Vmax = Vunit * m = Vposunit*m3 (m, m3 are integers)
Base +	LINIT CIZE INO	Hunit	[0-15]	Horizontal unit pixel number
004h	UNIT_SIZE_INQ	Vunit	[16-31]	Vertical unit pixel number
Base +	UNIT_POSITION_INQ	Hposunit	[0-15]	Horizontal unit pixel number for position If read value of Hposunit is 0, Hposunit = Hunit for IIDC 1.20 compatibility.
04Ch		Vposunit	[16-31]	Vertical unit number for position If read value of Vposunit is 0, Vposunit = Vunit for IIDC 1.20 compatibility.
Base +	IMAGE POSITION	Left	[0-15]	Left position of requested image region (pixels) Left = Hposunit * n1 Left + Width <= Hmax
008h	IMAGE_POSITION	Тор	[16-31]	Top position of requested image region (pixels)  Top = Vposunit * m1  Top + Height <= Vmax
Base +		Width	[0-15]	Width of requested image region (pixels) Width = Hunit * n2
00Ch	IMAGE_SIZE	Height	[16-31]	Height of requested image region (pixels) Height = Vunit * m2 (n1, n2, m1, m2 are integers)

### C.5.6.2 COLOR\_CODING\_ID and COLOR\_CODING\_INQ

The COLOR\_CODING\_INQ register describes the color-coding capability of the system. Each coding scheme has its own ID number. The required color-coding scheme must be set to COLOR\_CODING\_ID register as the ID number.

Address	Name	Field	Bit	Description	ID
Base +	COLOR_CODING_	Coding_ID	[0-7]	Color coding ID from COLOR_CODING_INQ register	N/A
010h	ID		[8-31]	Reserved	N/A



Address	Name	Field	Bit	Description	ID
		Mono8	[0]	Y only. Y=8bits, non compressed	0
		4:1:1 YUV8	[1]	4:1:1, Y=U=V= 8bits, non compressed	1
		4:2:2 YUV8	[2]	4:2:2, Y=U=V=8bits, non compressed	2
		4:4:4 YUV8	[3]	4:4:4, Y=U=V=8bits, non compressed	3
		RGB8	[4]	R=G=B=8bits, non compressed	4
		Mono16	[5]	Y only, Y=16bits, non compressed	5
Base +	COLOR_CODING_	RGB16	[6]	R=G=B=16bits, non compressed	6
014h	INQ	Signed Mono16	[7]	Y only, Y=16 bits, non compressed (signed integer)	7
		Signed RGB16	[8]	R=G=B=16 bits, non compressed (signed integer)	8
		Raw8	[9]	Raw data output of color filter sensor, 8 bits	9
		Raw16	[10]	Raw data output of color filter sensor, 16 bits	10
		Mono12	[11]	Y only. Y=12 bits, non compressed	
		Raw12	[12]	Raw data output of color filter sensor, 12 bits	
			[13-31]	Reserved	11-31

### C.5.6.3 FRAME\_INTERVAL\_INQ

### Format:

Address	Name	Field	Bit	Description
Base + 050h	FRAME_INTERVAL_ INQ	FrameInterval	[0-31]	Current frame interval (seconds) based on the current camera conditions, including exposure time. The reciprocal value of this (1 / FrameInterval) is the frame rate of the camera.  IEEE/REAL*4 floating-point value (see Determining Absolute Value Register Values(page 114)  If 0, the camera can't report the value and it should be ignored.

### **C.5.7** Pixel Formats

### C.5.7.1 DATA\_DEPTH: 630h

This register allows the user to control the endianness of Y16 images.



Field	Bit	Description
Data_Depth	[0-7]	Effective data depth of current image data.  If read value of Data_Depth is zero, shall ignore this field.  Read: Effective data depth  Write: Ignored
Little_Endian	[8]	Little endian mode for 16-bit pixel formats only  Write/Read:  0: Big endian mode (default on initialization)  1: Little endian mode
	[9-31	Reserved

### C.5.7.2 BAYER\_MONO\_CTRL: 1050h

This register enables raw Bayer output in non-Format 7 Y8/Y16 modes, or Format 7 Mono8/Mono16 modes.

#### Format:

Field	Bit	Description
Presence_Inq	[0]	Presence of this feature.  0: Not Available, 1: Available
	[1-30]	Reserved.
Bayer_Mono_Ctrl	[31]	Value  0: Disable raw Bayer output in mono modes, 1: Enable raw Bayer output in mono modes

## **C.6** Asynchronous Trigger Settings

For information about working with the trigger registers in your FlyCapture application, refer to the AsyncTriggerEx sample program, available with the FlyCapture SDK.

**Trigger Mode**—This controls the trigger mode. When trigger mode is enabled, frame rate is changed from Auto to Off state. This change affects the maximum shutter time (page 88). If trigger mode is disabled, frame rate remains in the Off state.

**Trigger Delay**—This provides control over the time delay, depending on the current mode:

• In Asynchronous trigger mode: controls the delay between the trigger event and the start of integration (shutter open).

Software Trigger - This allows the user to generate a software asynchronous trigger.

### C.6.1 TRIGGER\_MODE: 830h

Control of the register is via the ON\_OFF bit and the Trigger\_Mode and Parameter fields.



Field	Bit	Description
Presence_Inq	[0]	Presence of this feature 0: Not Available, 1: Available
Abs_Control	[1]	Absolute value control  0: Control with the Value field, 1: Control with the Absolute value CSR.  If this bit = 1, the value in the Value field is read-only.
	[2-5]	Reserved
ON_OFF	[6]	Read: read a status Write: ON or OFF for this feature  0: OFF, 1: ON If this bit = 0, other fields will be read only
Trigger_Polarity	[7]	Select trigger polarity (except for Software_Trigger)  0: Trigger active low, 1: Trigger active high
Trigger_Source	[8-10]	Select trigger source: used to select which GPIO pin will be used for external trigger purposes.  Sets trigger source ID from <i>Trigger_Source_Inq</i> field of TRIGGER_INQ register.
Trigger_Value	[11]	Trigger input raw signal value: used to determine the current raw signal value on the pin.  Read only  0: Low, 1: High
	[8-11]	Reserved
Trigger_Mode	[12-15]	Trigger mode (Trigger_Mode_015): used to set the trigger mode to be used. For more information, see Trigger Modes on page 71.  Query the Trigger_Mode_Inq fields of the TRIGGER_INQ register for available trigger modes.
	[16-19]	Reserved
Parameter	[20-31]	Parameter for trigger function, if required (optional)

## C.6.2 TRIGGER\_DELAY: 834h

Field	Bit	Description	
Presence_Inq	[0]	Presence of this feature 0: Not Available, 1: Available	
		Absolute value control	
Abs_Control	[1]	0: Control with the Value field, 1: Control with the Absolute value CSR.	
		If this bit = 1, the value in the Value field is read-only.	
	[2-5]	Reserved	



Field	Bit	Description		
ON_OFF	[6]	Read: read a status Write: ON or OFF for this feature  0: OFF, 1: ON If this bit = 0, other fields will be read only		
	[7-19] Reserved			
Value	[20-31]	Value.		

### C.6.3 SOFTWARE\_TRIGGER: 62Ch



Bit 0 of this register indicates if the camera is ready to be triggered again for both software and hardware triggering.

#### Format:

Field	Bit	Description	
		This bit automatically resets to zero in all trigger modes except Trigger Mode 3.	
Software_Trigger	[0]	Read: 0: Ready, 1: Busy Write: 0: Reset software trigger, 1: Set software trigger	

## **C.7** Controlling Imaging Parameters

The registers in this section are used to control imaging parameters for the camera.

### C.7.1 Imaging Parameters: 800h-888h

The following imaging parameters share the same register format.

Parameter	Register
Brightness	800h
Sharpness	808h
Hue	810h
Saturation	814h
Gamma	818h
Gain	820h
Iris	824h
Focus	828h
Pan	884h
Tilt	888h

These imaging parameters are defined by **modes** and **values**.



### There are three modes:

Mode	Description
On/Off	Determines if the feature is on. If off, values are fixed and not controllable.
Auto/Manual	If the feature is on, determines if the feature is in automatic or manual mode. If manual, values can be set.
One Push	If the feature is in manual mode, the camera executes once automatically and then returns to manual mode.

The value field in this register can be set in three ways:

Method	Description		
Absolute	The user sets the value is set via the absolute register. The <i>Value</i> field becomes read only and reflects the converted absolute value.		
Manual	The user sets the value in the <i>Value</i> field. The absolute register becomes read only and contains the current value.		
Automatic	The value is set automatically by another register and both the <i>Value</i> field and the absolute register become read only.		



Formulas for converting the fixed point (relative) values to floating point (absolute) values are not provided. Users wishing to work with real-world values should refer to Absolute Value CSRs (page 114).

Field	Bit	Description	
Presence_Inq	[0]	Presence of this feature 0: Not Available, 1: Available	
Abs_Control	[1]	Absolute value control  0: Control in the Value field, 1: Control in the Absolute value CSR.	
	[2-4]	If this bit = 1, the value in the Value field is read-only.  Reserved	
One_Push	[5]	One push auto mode (controlled automatically only once)  Read: 0: Not in operation, 1: In operation  Write: 1: Begin to work (self-cleared after operation)  If A_M_Mode = 1, this bit is ignored	
Read: read a status Write: ON or OFF for this feature  ON_OFF  0: OFF, 1: ON If this bit = 0, other fields will be read only		Write: ON or OFF for this feature  0: OFF, 1: ON	



Field	Bit	Description	
A_M_Mode	[7]	Read: read a current mode Write: set the mode	
		0: Manual, 1: Automatic	
	[8-19]	Reserved	
Value	[20-31]	Value. A write to this value in 'Auto' mode will be ignored.	

### C.7.2 LUT: 80000h - 80048h (IIDC 1.32)

Offset	Name	Field	Bit	Description
		Presence_Inq	[0]	Presence of this feature 0: Not Available, 1: Available
			[1-4]	Reserved
		ON_OFF_Inq	[5]	Capability of turning this feature ON or OFF.
			[6-7]	Reserved
80000h	LUT_Ctrl_Inq	Input_Depth	[8-12]	Input data bit depth
	(Read Only)	Output_Depth	[13-17]	Output data bit depth
			[18]	Reserved
		Number_of_Channels	[19-23]	Number of channels
			[24-26]	Reserved
		Number_of_Banks	[27-31]	Number of banks



Offset	Name	Field	Bit	Description
		Read_Bank_0_Inq	[0]	Capability of reading data from Bank 0
		Read_Bank_1_Inq	[1]	Capability of reading data from Bank 1
		Read_Bank_2_Inq	[2]	Capability of reading data from Bank 2
		Read_Bank_3_Inq	[3]	Capability of reading data from Bank 3
		Read_Bank_4_Inq	[4]	Capability of reading data from Bank 4
		Read_Bank_5_Inq	[5]	Capability of reading data from Bank 5
		Read_Bank_6_Inq	[6]	Capability of reading data from Bank 6
000046	LUT_Bank_Rd_	Read_Bank_7_Inq	[7]	Capability of reading data from Bank 7
80004h	Inq	Read_Bank_8_Inq	[8]	Capability of reading data from Bank 8
		Read_Bank_9_Inq	[9]	Capability of reading data from Bank 9
		Read_Bank_10_Inq	[10]	Capability of reading data from Bank 10
		Read_Bank_11_Inq	[11]	Capability of reading data from Bank 11
		Read_Bank_12_Inq	[12]	Capability of reading data from Bank 12
		Read_Bank_13_Inq	[13]	Capability of reading data from Bank 13
		Read_Bank_14_Inq	[14]	Capability of reading data from Bank 14
		Read_Bank_15_Inq	[15]	Capability of reading data from Bank 15
		Write_Bank_0_Inq	[16]	Capability of writing data to Bank 0
		Write_Bank_1_Inq	[17]	Capability of writing data to Bank 1
		Write_Bank_2_Inq	[18]	Capability of writing data to Bank 2
		Write_Bank_3_Inq	[19]	Capability of writing data to Bank 3
		Write_Bank_4_Inq	[20]	Capability of writing data to Bank 4
		Write_Bank_5_Inq	[21]	Capability of writing data to Bank 5
		Write_Bank_6_Inq	[22]	Capability of writing data to Bank 6
	LUT_Bank_Wr_	Write_Bank_7_Inq	[23]	Capability of writing data to Bank 7
	Inq	Write_Bank_8_Inq	[24]	Capability of writing data to Bank 8
		Write_Bank_9_Inq	[25]	Capability of writing data to Bank 9
		Write_Bank_10_Inq	[26]	Capability of writing data to Bank 10
		Write_Bank_11_Inq	[27]	Capability of writing data to Bank 11
		Write_Bank_12_Inq	[28]	Capability of writing data to Bank 12
		Write_Bank_13_Inq	[29]	Capability of writing data to Bank 13
		Write_Bank_14_Inq	[30]	Capability of writing data to Bank 14
		Write_Bank_15_Inq	[31]	Capability of writing data to Bank 15



Offset	Name	Field	Bit	Description
		Presence_Inq	[0]	Presence of this Feature 0: Not Available, 1: Available
			[1-4]	Reserved
				Read: read a status Write: ON or OFF this feature
80008h	LUT_Ctrl	ON_OFF	[5]	0: OFF 1: ON
				When ON is written, the ON_OFF field of the GAMMA register is turned to OFF.
			[6-27]	Reserved
		Active_Bank	[28-31]	Active bank
8000Ch	Bank_0_ Offset_Inq	Bank_0_Quadlet_Offset	[0-31]	32-bit offset of Bank 0 table data
80010h	Bank_1_ Offset_Inq	Bank_1_Quadlet_Offset	[0-31]	32-bit offset of Bank 1 table data
80014h	Bank_2_ Offset_Inq	Bank_2_Quadlet_Offset	[0-31]	32-bit offset of Bank 2 table data
80018h	Bank_3_ Offset_Inq	Bank_3_Quadlet_Offset	[0-31]	32-bit offset of Bank 3 table data
8001Ch	Bank_4_ Offset_Inq	Bank_4_Quadlet_Offset	[0-31]	32-bit offset of Bank 4 table data
80020h	Bank_5_ Offset_Inq	Bank_5_Quadlet_Offset	[0-31]	32-bit offset of Bank 5 table data
80024h	Bank_6_ Offset_Inq	Bank_6_Quadlet_Offset	[0-31]	32-bit offset of Bank 6 table data
80028h	Bank_7_ Offset_Inq	Bank_7_Quadlet_Offset	[0-31]	32-bit offset of Bank 7 table data
8002Ch	Bank_8_ Offset_Inq	Bank_8_Quadlet_Offset	[0-31]	32-bit offset of Bank 8 table data
80030h	Bank_9_ Offset_Inq	Bank_9_Quadlet_Offset	[0-31]	32-bit offset of Bank 9 table data
80034h	Bank_10_ Offset_Inq	Bank_10_Quadlet_Offset	[0-31]	32-bit offset of Bank 10 table data
80038h	Bank_11_ Offset_Inq	Bank_11_Quadlet_Offset	[0-31]	32-bit offset of Bank 11 table data
8003Ch	Bank_12_ Offset_Inq	Bank_12_Quadlet_Offset	[0-31]	32-bit offset of Bank 12 table data
80040h	Bank_13_ Offset_Inq	Bank_13_Quadlet_Offset	[0-31]	32-bit offset of Bank 13 table data
80044h	Bank_14_ Offset_Inq	Bank_14_Quadlet_Offset	[0-31]	32-bit offset of Bank 14 table data
80048h	Bank_15_ Offset_Inq	Bank_15_Quadlet_Offset	[0-31]	32-bit offset of Bank 15 table data



### C.7.3 WHITE\_BALANCE: 80Ch

### Format:

Field	Bit	Description	
Presence_Inq	[0]	Presence of this feature 0: Not Available, 1: Available	
		Absolute value control	
Abs_Control	[1]	0: Control with the Value field, 1: Control with the Absolute Value CSR	
		If this bit is 1, then Value is ignored	
	[2-4]	Reserved	
		One push auto mode (controlled automatically by camera only once)	
One_Push	[5]	Read: 0: Not in operation, 1: In operation Write: 1: Begin to work (self-cleared after operation)	
		If A_M_Mode = 1, this bit is ignored	
ON_OFF	[6]	Read: read a status Write: ON or OFF for this feature	
ON_OTT		0: OFF, 1: ON If this bit = 0, other fields will be read only	
A_M_Mode	[7]	Read: read the current mode. Write: Set the mode.	
		0: Manual, 1: Auto	
U_Value/B_Value	[8-19]	Blue Value. A write to this value in 'Auto' mode will be ignored.	
V_Value/R_Value	[20-31]	Red Value. A write to this value in 'Auto' mode will be ignored.	

## C.7.4 BAYER\_TILE\_MAPPING: 1040h

This 32-bit read only register specifies the sense of the cameras' Bayer tiling. Various colors are indicated by the ASCII representation of the first letter of their name.

Color	ASCII
Red (R)	52h
Green (G)	47h
Blue (B)	42h
Monochrome (Y)	59h

For example, 0x52474742 is RGGB and 0x59595959 is YYYY.





Because color models support on-board color processing, the camera reports YYYY tiling when operating in any non-raw Bayer data format. For more information, see <u>Bayer Color Processing on page 90</u>.

### **Format**

Field	Bit	Description	
Bayer_Sense_A	[0-7]	ASCII representation of the first letter of the color of pixel (0,0) in the Bayer tile.	
Bayer_Sense_B	[8-15]	ASCII representation of the first letter of the color of pixel (0,1) in the Bayer tile.	
Bayer_Sense _C	[16-24]	ASCII representation of the first letter of the color of pixel (1,0) in the Bayer tile.	
Bayer_Sense _D	[25-31]	ASCII representation of the first letter of the color of pixel (1,1) in the Bayer tile.	

### C.7.5 MIRROR\_IMAGE\_CTRL: 1054h

#### Format:

Field	Bit	Description	
Presence_Inq	[0]	Presence of this feature.  0: Not Available, 1: Available	
	[1-30]	Reserved.	
Mirror_Image_Ctrl	[31]	Value 0: Disable horizontal (mirror) image flip 1: Enable horizontal (mirror) image flip	

### **C.7.6 SHUTTER: 81Ch**

This register has three states:

State	Description
Manual/Abs	The shutter value is set by the user via the ABS_VAL_SHUTTER register (page 114). The Value field becomes read only and reflects the converted value of the ABS_VAL_SHUTTER register.
Manual	The user sets the shutter value via the <i>Value</i> field. The ABS_VAL_SHUTTER register becomes read only and contains the current shutter time.
Auto	The shutter value is set by the auto exposure controller (if enabled) (page 91). Both the <i>Value</i> field and the ABSVAL_SHUTTER register become read only.

The fixed-point (relative) values reported by this register can be converted to absolute values based on the following chart:

Fixed-point Value Range	Equivalent Absolute Value Unit	Equivalent Absolute Value Range
1 to 1024	10 us	0.01 ms to 10.24 ms
1025 to 1536	20 us	10.26 ms to 20.48 ms
1537 to 2048	40 us	20.52 to 40.96 ms



Fixed-point Value Range		
2049 to 2560	80 us	41.04 ms to 81.92 ms

Field	Bit	Description	
Presence_Inq	[0]	Presence of this feature 0: Not Available, 1: Available	
Abs_Control	[1]	Absolute value control  0: Control with the <i>Value</i> field, 1: Control with the Absolute value CSR.  If this bit = 1, the value in the <i>Value</i> field is ignored.	
	[2-4]	Reserved	
One_Push	[5]	One push auto mode (controlled automatically by camera only once)  Read: 0: Not in operation, 1: In operation  Write: 1: Begin to work (self-cleared after operation)  If A_M_Mode = 1, this bit is ignored	
ON_OFF	[6]	Read: read a status Write: ON or OFF for this feature  0: OFF, 1: ON If this bit = 0, other fields will be read only	
A_M_Mode	[7]	Read: read a current mode Write: set the mode  0: Manual, 1: Automatic	
High_Value	[8-19]	Upper 4 bits of the shutter value available only in extended shutter mode (outside of specification).	
Value	[20-31]	Value. A write to this value in 'Auto' mode will be ignored.	

## C.7.7 AUTO\_EXPOSURE: 804h



Formulas for converting the fixed point (relative) values to floating point (absolute) values are not provided. Users wishing to work with real-world values should refer to Absolute Value CSRs (page 114).



Field	Bit	Description	
Presence Inq	[0]	Presence of this feature	
	[-1	0: Not Available, 1: Available	
		Absolute value control	
Abs_Control	[1]	0: Control with the Value field, 1: Control with the Absolute value CSR.	
		If this bit = 1, the value in the <i>Value</i> field is ignored.	
	[2-4]	Reserved	
		One push auto mode (controlled automatically by camera only once)	
Our Buch	(e)	Read: 0: Not in operation, 1: In operation	
One_Push	[5]	Write: 1: Begin to work (self-cleared after operation)	
		If A_M_Mode = 1, this bit is ignored	
		Read: read a status	
ON_OFF	[6]	Write: ON or OFF for this feature	
014_011	[0]	0: OFF, 1: ON	
		If this bit = 0, other fields will be read only	
		Read: read a current mode	
A_M_Mode	[7]	Write: set the mode	
		0: Manual, 1: Automatic	
High_Value	[8-19]	Upper 4 bits of the shutter value available only in extended shutter mode (outside of specification).	
Value	[20-31]	Value.	
Turuc	[20 31]	A write to this value in 'Auto' mode will be ignored.	

### C.7.7.1 AUTO\_EXPOSURE\_RANGE: 1088h

Fixed point (relative) values must be specified. Do not specify absolute values.

### Format:

Field	Bit	Description	
Presence_Inq	[0]	Presence of this feature 0: Not Available, 1: Available	
	[1-7]	Reserved	
Min_Value	[8-19]	Lower bound	
Max_Value	[20-31]	Upper bound	

### C.7.7.2 AUTO\_SHUTTER\_RANGE: 1098h

Fixed point (relative) values must be specified. Do not specify absolute values.



Field	Bit	Description	
Presence_Inq	[0]	Presence of this feature  0: Not Available, 1: Available	
	[1-5]	Reserved	
Min_Dark_Noise	[6]	Minimizes dark current noise with extended shutter times. This feature is currently experimental.  0: Disable dark noise minimization, 1: Enable dark noise minimization	
	[7]	Reserved	
Min_Value	[8-19]	Lower bound	
Max_Value	[20-31]	Upper bound	



The actual range used is further restricted to match the current grab mode (see SHUTTER register 81Ch (page 158) for the list of ranges).

### C.7.7.3 AUTO\_GAIN\_RANGE: 10A0h

#### Format:

Field	Bit	Description	
Presence_Inq	[0]	Presence of this feature 0: Not Available, 1: Available	
	[1-5]	Reserved	
ON_OFF	[6]	Read: read a status Write: ON or OFF for this feature  0: OFF, 1: ON If this bit = 0, other fields will be read only	
	[7]	Reserved	
Min_Value	[8-19]	Lower bound	
Max_Value	[20-31]	Upper bound	

### C.7.8 HDR: 1800h - 1884h

This register allows the user to access and control a multiple exposure quick cycle mode, which is useful for high dynamic range (HDR) imaging.

Note that if bit [31] of the FRAME\_INFO register 12F8h (page 162) is set to 1, the camera will embed the current shutter/gain value in the image when bit [6] of HDR\_CTRL is set to 1. The image timestamp will be embedded in the first 32-bits of image data, the shutter value in the second 32-bits, and gain in the third, all in big-endian format.

Note that the on/off bit for the HDR shutter and gain registers is hard-coded to on.



Offset	Name	Field	Bit	Description
	Presence_Inq	[0]	Presence of this feature 0: Not available, 1: Available	
		-	[1-5]	Reserved
1800h	1800h HDR_CTRL	ON_OFF	[6]	Read: read a status Write: ON or OFF for this feature  0: OFF, 1: ON If this bit = 0, other fields will be read only
		-	[7-31]	Reserved
		Presence_Inq	[0]	Presence of this feature 0: Not available, 1: Available
1820h	HDR_SHUTTER_0	-	[1-19]	Reserved
		Value	[20-31]	Query SHUTTER_INQ register 51Ch for range of possible shutter values
	824h HDR_GAIN_0	Presence_Inq	[0]	Presence of this feature 0: Not available, 1: Available
1824h		-	[1-19]	Reserved
		Value	[20-31]	Query GAIN_INQ register 520h for range of possible gain values
1840h	HDR_SHUTTER_1	Same format as HDR_SHUTTER_0		
1844h	HDR_GAIN_1	Same format as HDR_GAIN_0		
1860h	HDR_SHUTTER_2	Same format as HDR_SHUTTER_0		
1864h	HDR_GAIN_2	Same format as HDR_GAIN_0		
1880h	HDR_SHUTTER_3	Same format as HDR_SHUTTER_0		
1884h	HDR_GAIN_3	Same format as HDR_GAIN_0		

## C.7.9 FRAME\_INFO: 12F8h

Field	Bit	Description	Frame-Specific Information	
Presence_Inq	[0]	Presence of this feature 0: Not Available, 1: Available		
	[1-5]	Reserved		



Field	Bit	Description	Frame-Specific Information		
ROI_Pos_Inq	[6]				
GPIO_State_Inq	[7]				
Strobe_Pat_Inq	[8]				
Frame_Count_Inq	[9]				
WB_CSR_Inq	[10]	Presence of image-specific information display			
Exp_CSR_Inq	[11]	0: Not Available, 1: Available			
Bright_CSR_Inq	[12]				
Shutter_CSR_Inq	[13]				
Gain_CSR_Inq	[14]				
Time_Inq	[15]				
CSR_Abs_Value	[16]	Toggles between displaying 32-bit relative or absolute CSR values. If absolute value not supported, relative value is displayed.  O: Relative, 1: Absolute  This field is currently read-only			
	[17-21]	Reserved			
	[22]		Region of Interest (ROI) position (See page 94)		
	[23]		GPIO Pin State		
	[24]		Strobe Pattern Counter		
	[25]		Frame Counter		
Insert_Info	[26]	Display image-specific information	White Balance CSR		
ilisert_illio	[27]	0: Off 1: On	Exposure CSR		
	[28]		Brightness CSR		
	[29]		Shutter Value		
	[30]		Gain CSR		
	[31]		Timestamp (See page 94)		

## C.8 Troubleshooting

The following registers help with troubleshooting issues with the camera:

- Camera Diagnostics (below)
- Pixel Defect Correction (on page 165)

### C.8.1 Camera Diagnostics

Use the following parameters to monitor the error status of the camera and troubleshoot problems:

**Time from Initialize**—This reports the time, in seconds, since the camera was initialized during a hard power-up. This is different from powering up the camera, which will not reset this time.



**Link Up Time**—This reports the time, in seconds, since the last Ethernet reconnection occurred. This will be equal to the Time from Initialize if no reconnection has occurred since the last time the camera was initialized.

**Transmit Failure**—This contains a count of the number of failed frame transmissions that have occurred since the last reset.

**Camera Log**—This provides access to the camera's 256 byte internal message log, which is often useful for debugging camera problems. Contact <u>technical support</u> for interpretation of message logs.

#### **C.8.1.1** INITIALIZE: 000h

#### Format:

Offset	Name	Field	Bit	Description
000h	INITIALIZE	Initialize	[0]	If this bit is set to 1, the camera will reset to its initial state and default settings. This bit is self-cleared.
		[1-31]	Reserved	

### C.8.1.2 TIME\_FROM\_INITIALIZE: 12E0h

#### Format:

Field	Bit	Description	
Presence_Inq	[0]	Presence of this feature 0: Not Available, 1: Available	
Time_From_Init	[1-31]	Time in seconds since the camera was initialized.	

### C.8.1.3 LINK\_UP\_TIME: 12E4h

### Format:

Field	Bit	Description	
Presence_Inq	[0]	Presence of this feature 0: Not Available, 1: Available	
Time_From_Reset	[1-31]	Time in seconds since the camera detected a re-connection.	

### C.8.1.4 XMIT\_FAILURE: 12FCh

Field	Bit	Description	
Presence_Inq	[0]	Presence of this feature 0: Not Available, 1: Available	
Frame_Count	[1-31]	Read: Count of failed frame transmissions. Write: Reset.	



### C.8.1.5 VMODE\_ERROR\_STATUS: 628h

#### Format:

Field	Bit	Description
Vmode_Error_Status	[0]	Error status of combination of video format, mode, frame rate and ISO_SPEED setting.  0: no error, 1: error
		This flag will be updated every time one of the above settings is changed by writing a new value.
		variet.
	[1-31]	Reserved.

### C.8.1.6 LED\_CTRL: 1A14h



On GigE Vision cameras, this register enables or disables both the main camera status LED and the GigE connector indicator LEDs, if equipped.

#### Format:

Field	Bit	Description
Presence_Inq	[0]	Presence of this feature 0: Not Available, 1: Available
	[1-22]	Reserved
LED_Ctrl	[23-31]	Enable or disable the LED 0x00: Off, 0x74: On

### C.8.1.7 TEST\_PATTERN: 104Ch

### Format:

Field	Bit	Description
Presence_Inq	[0]	Presence of this feature 0: Not Available, 1: Available
	[1-30]	Reserved
Test_Pattern_1	[31]	Value 0: Disable test pattern, 1: Enable test pattern

## C.8.2 PIXEL\_DEFECT\_CTRL: 1A60h

Field	Bit	Description
Presence_Inq	[0]	Presence of this feature 0: Not Available, 1: Available
	[1-5]	Reserved
ON_OFF	[6]	Enable or disable FPGA pixel correction 0: Off, 1: On



Field	Bit	Description	
[7]		Reserved	
Max_Pixels	[8-19] Maximum number of pixels that can be corrected by the FPGA		
Cur_Pixels	[20-31]	Current number of pixels that are being corrected by the FPGA	



# **Contacting Point Grey Research**

For any questions, concerns or comments please contact us via the following methods:

Email	General questions about Point Grey Research  Technical support (existing customers only)			
Knowledge Base	Find answers to commonly asked questions i	n our <u>Knowledge Base</u>		
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# **Revision History**

Revision	Date	Notes
1.0	May 12, 2011	Initial version: support for model FL3-GE-13S2
1.1	August 29, 2011	Change in LED behavior during IP addressing
2.0	November 25, 2011	Added models FL3-GE-03S2 and FL3-GE-08S2 Added Trigger Mode 13 (Low Smear) to model FL3-GE-13S2 Added Multicasting support
3.0	February 28, 2012	Added models FL3-GE-50S5 and FL3-GE-14S3 Added installation instructions (Chapter 2) Added video mode and frame rate tables for monochrome models (Chapter 4) Added more information on smear reduction (Chapter 7)
4.0	February 29, 2012	Added model FL3-GE-20S4
5.0	July 9, 2012	Added model FL3-GE-03S1 Added revised dimensional diagram Added debouncer section Added GenlCam features Added Input/Output control chapter Moved Control and Status Registers into Appendix
5.1	July 17, 2012	Added model FL3-GE-13S2 available with CS-mount Added imaging performance tables and new Quantum Efficiency graphs
5.2	July 24, 2012	Corrected Full Well Depth for FL3-GE-03S1 Added Dynamic Range graph
6.0	September 24, 2012	Added model FL3-GE-28S4

