# Schematics For RK3568 Photonicat

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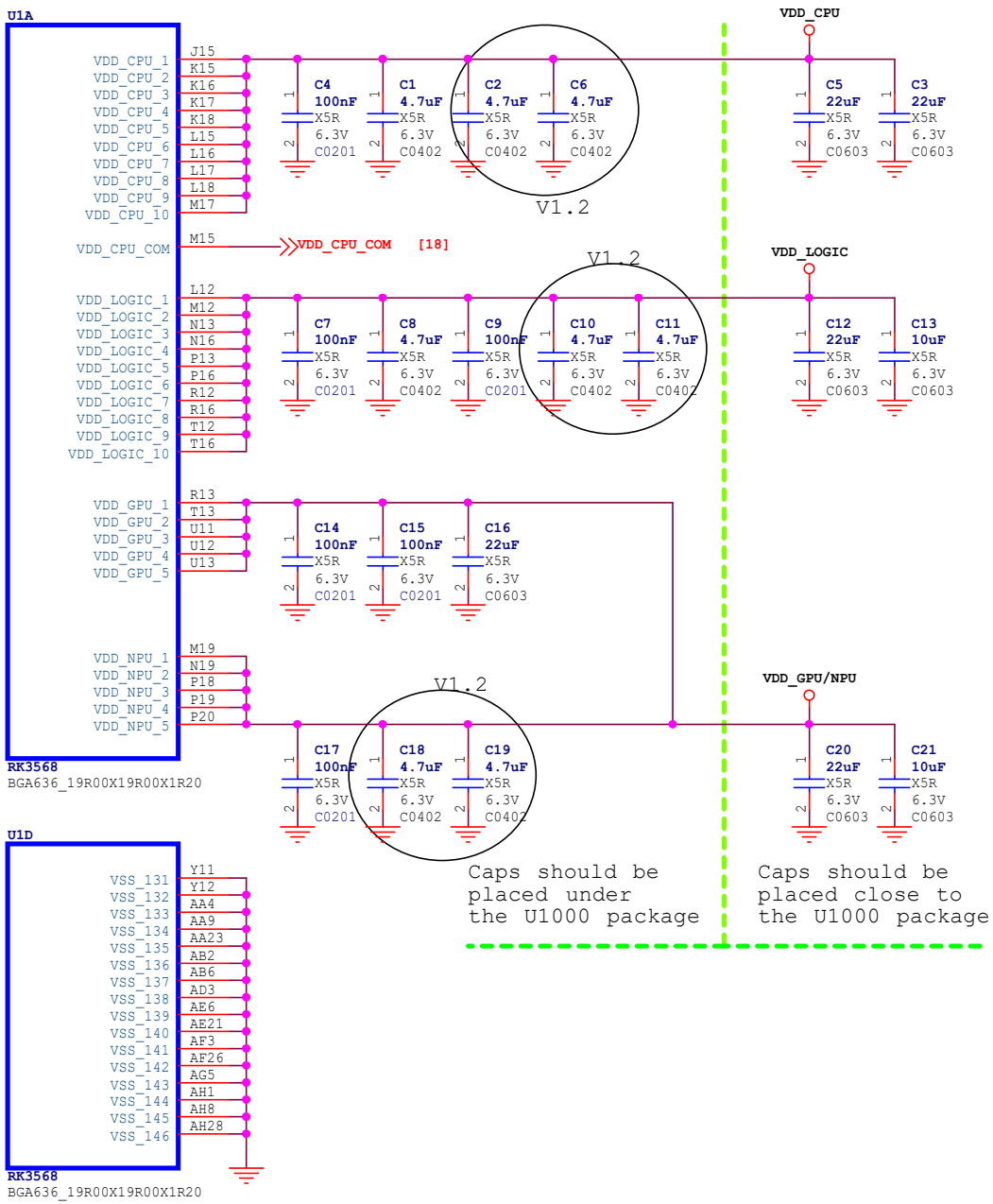
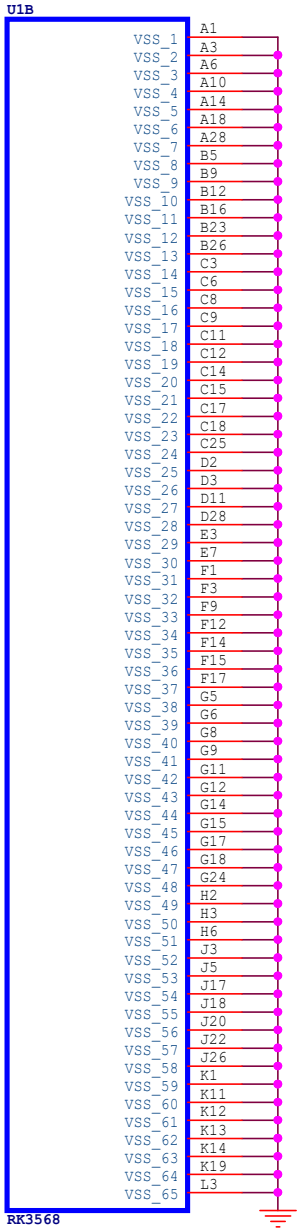
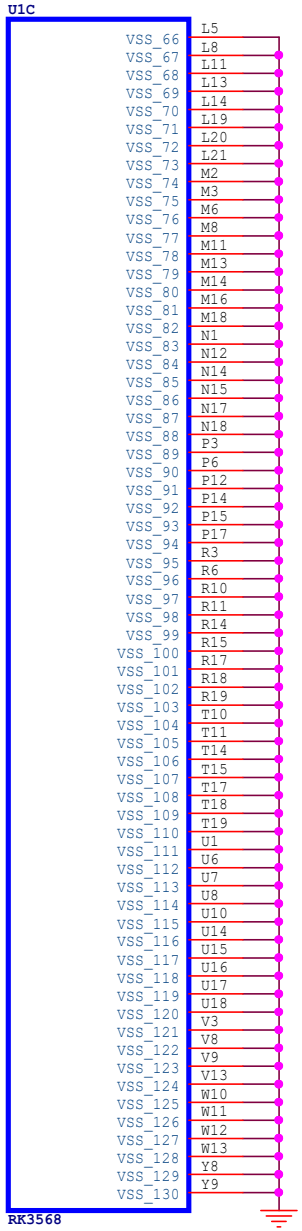
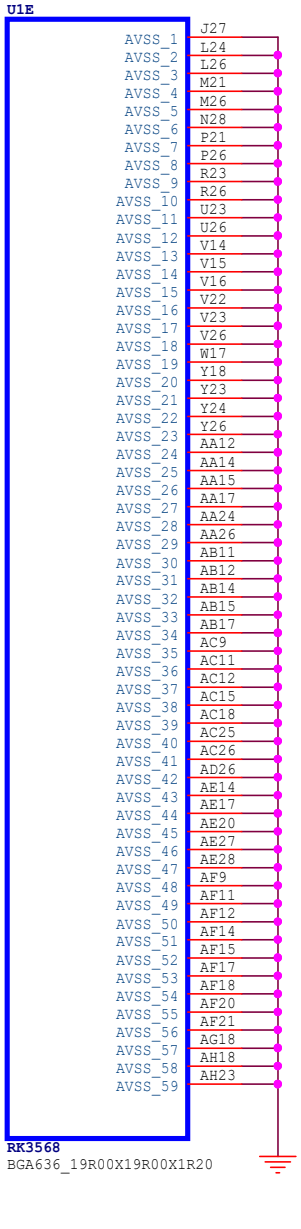
# RK3568_ABCDE (Power&Gnd)

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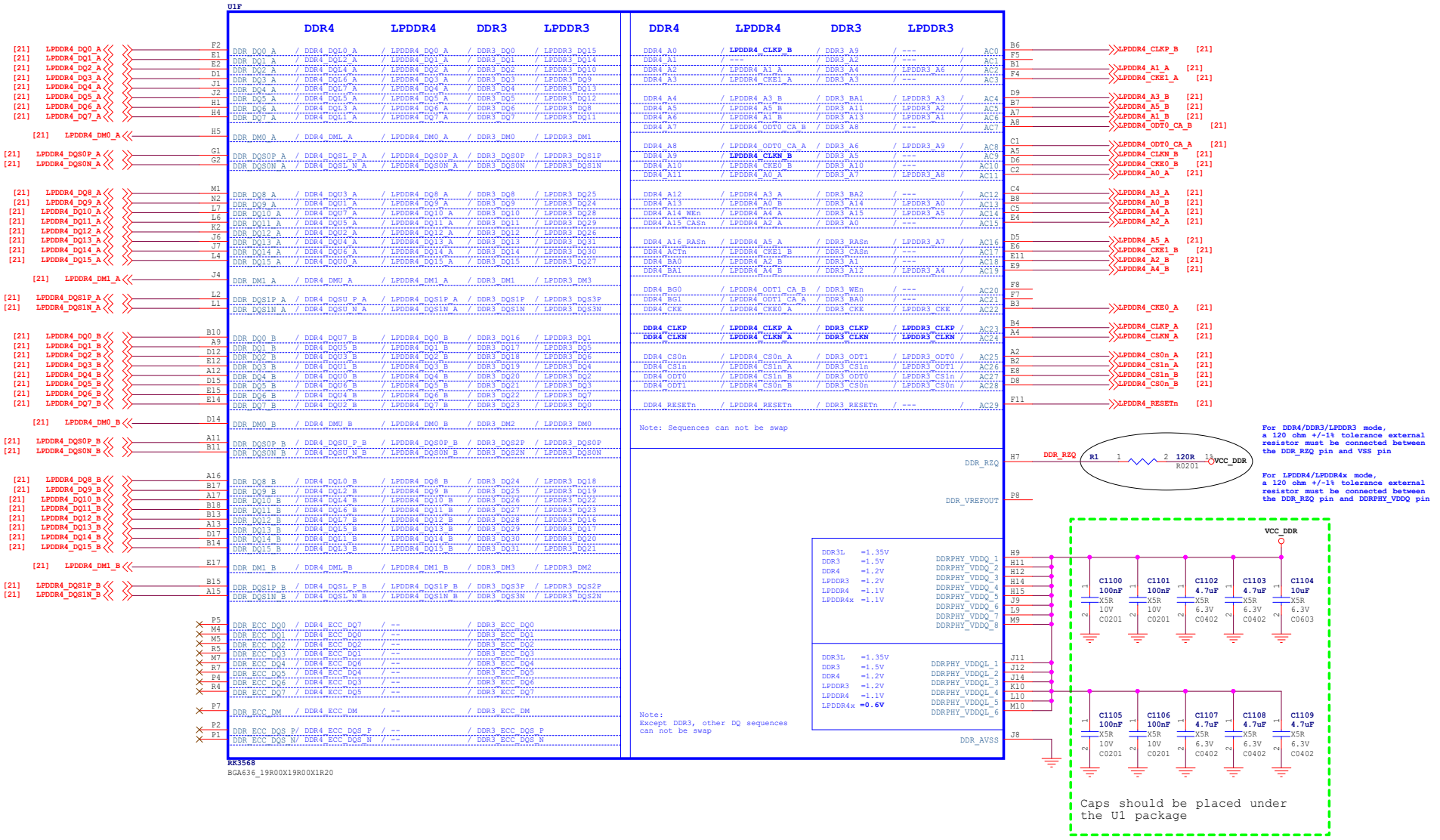
# RK3568_F (DDR PHY)

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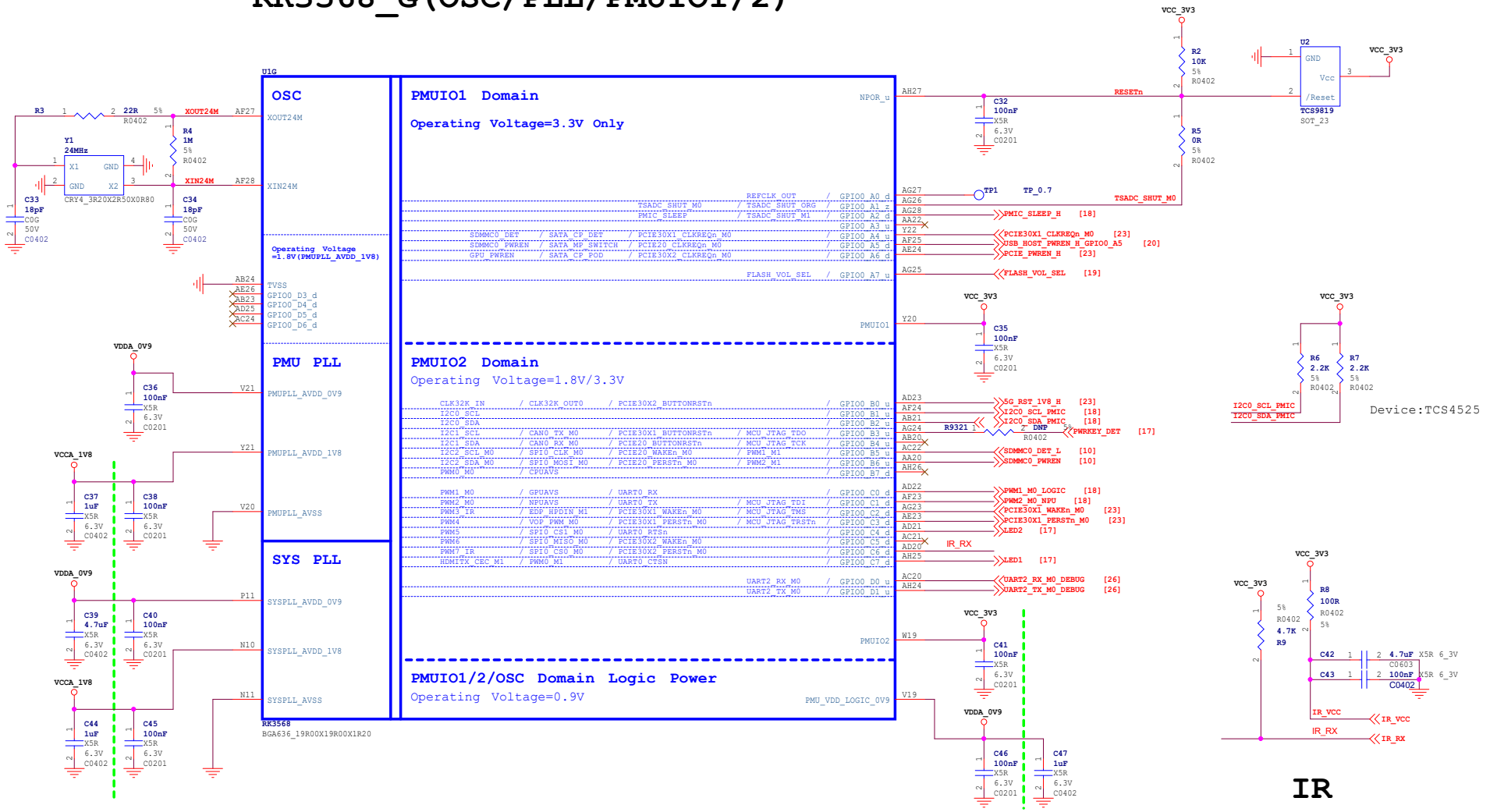
# RK3568_G(OSC/PLL/PMUIO1/2)




**Note:**
Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

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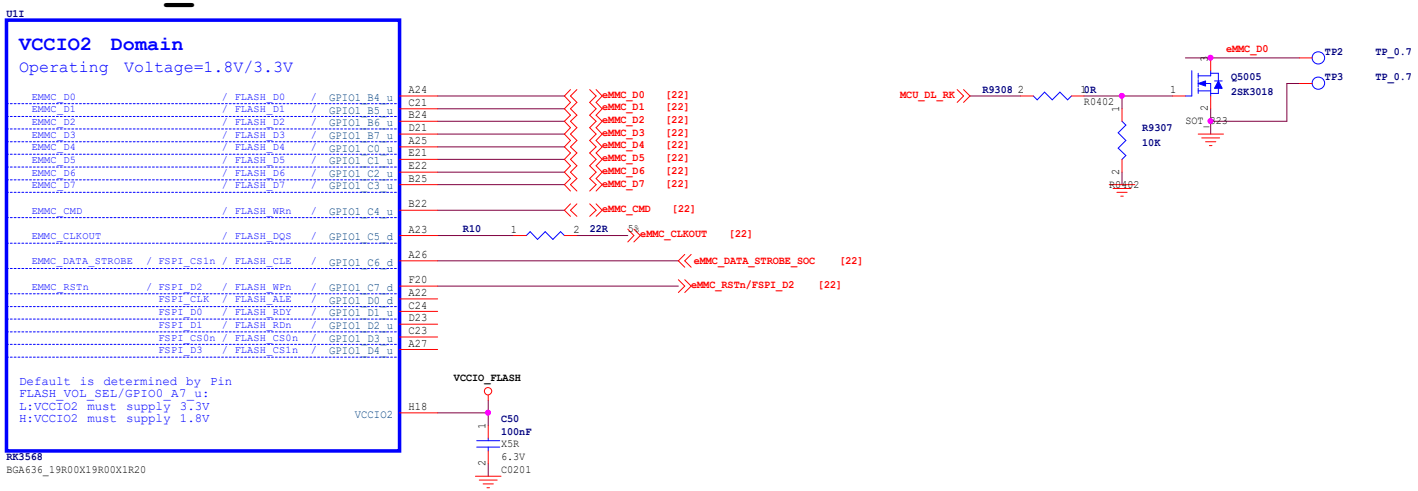
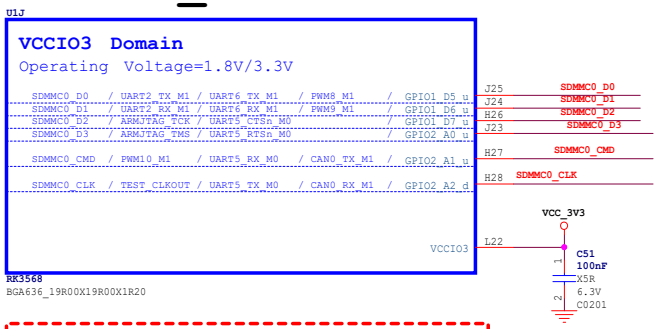
# RK3568_I(VCCIO2 Domain)

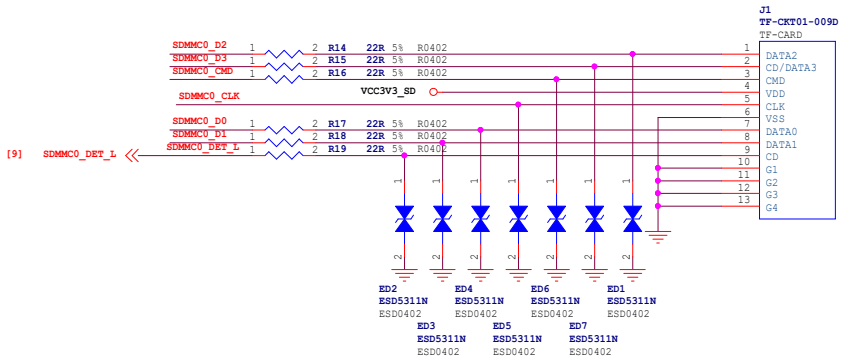


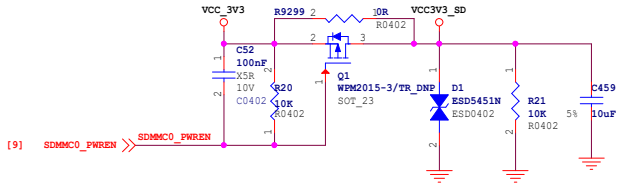

# RK3568_J(VCCIO3 Domain)




**Note:**
Caps of between dashed green lines and U1000 should be placed under the U1000 package

## MicroSD Card

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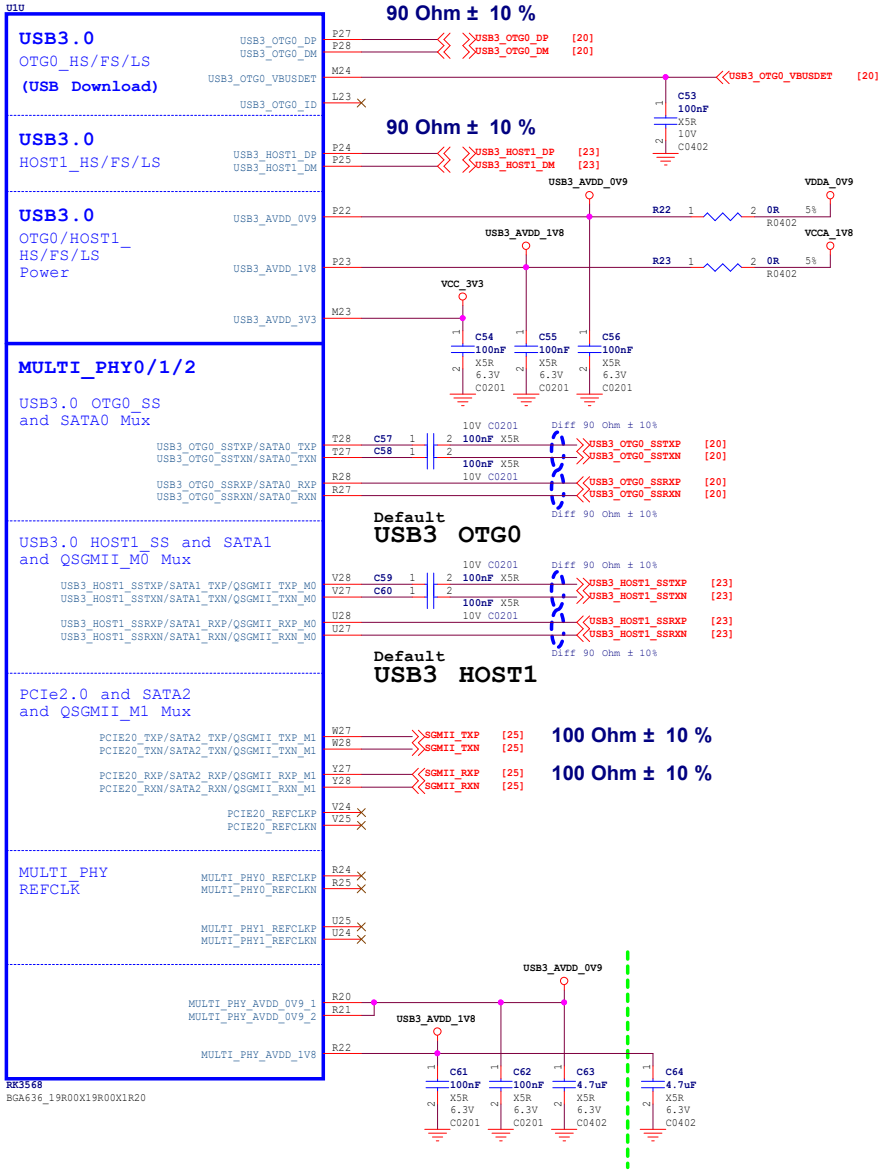
# RK3568_U(USB3.0/SATA/QSGMII/PCIe2.0 x1)







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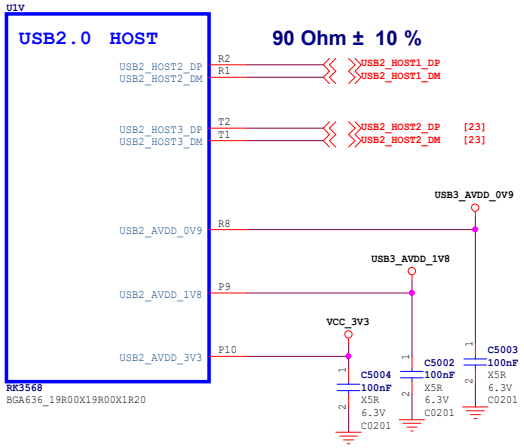
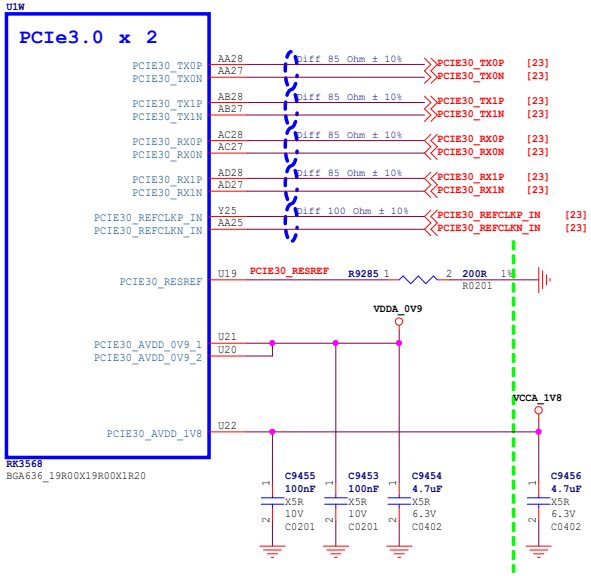
# RK3568_V(USB2.0 HOST)




# RK3568_W(PCIe3.0 x2)

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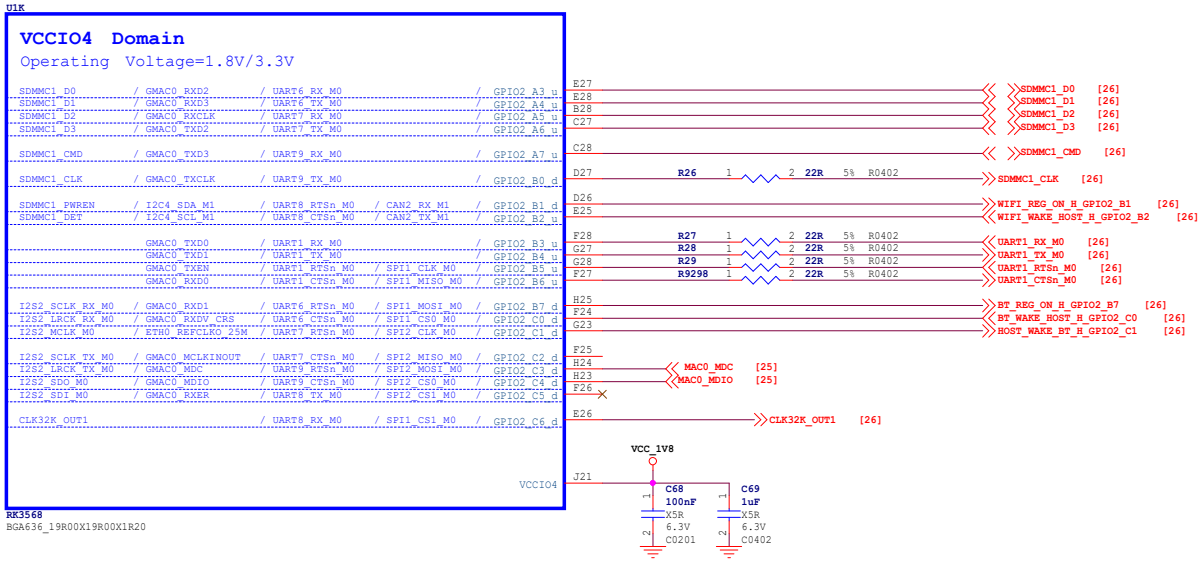
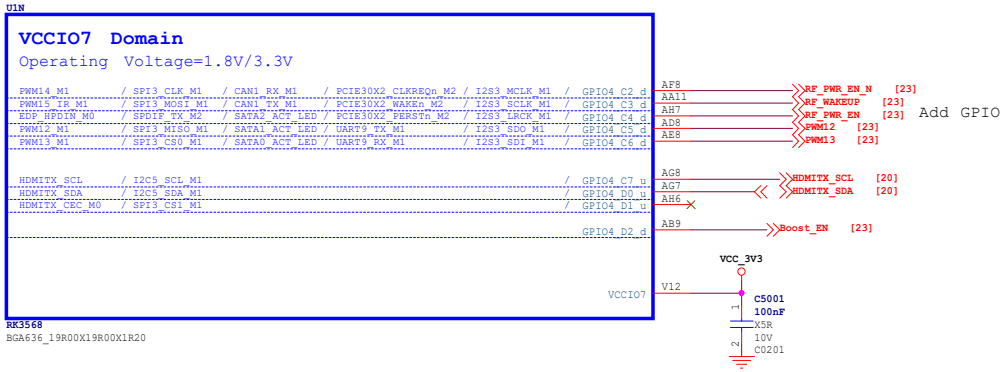
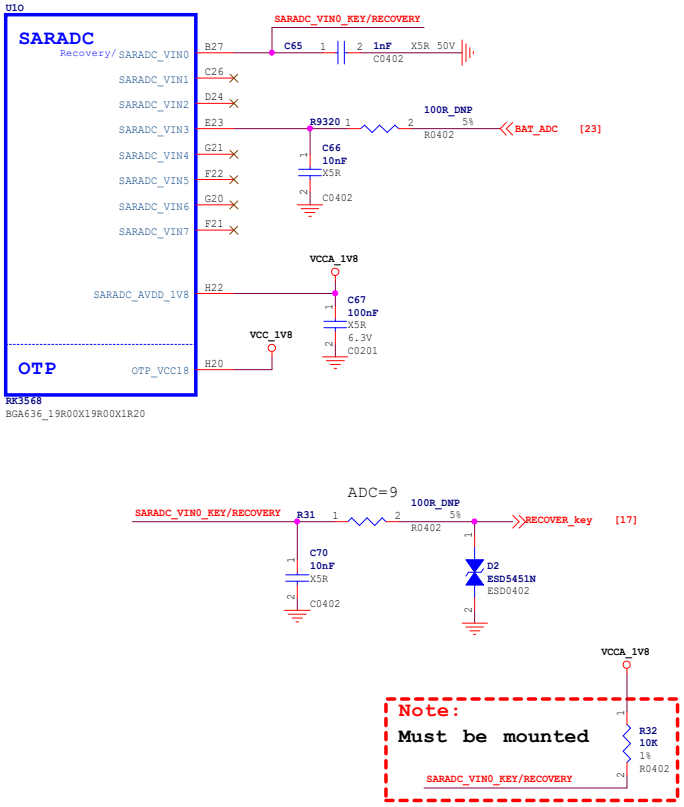
# RK3568_K(VCCIO4 Domain)




# RK3568_N(VCCIO7 Domain)




# RK3568_O(SARADC/OTP)




**Note:**
Caps of between dashed green lines and U1000 should be placed under the U1000 package

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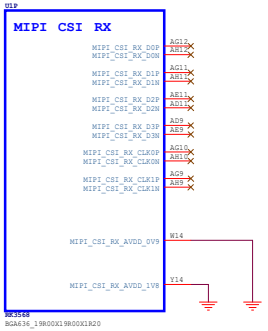
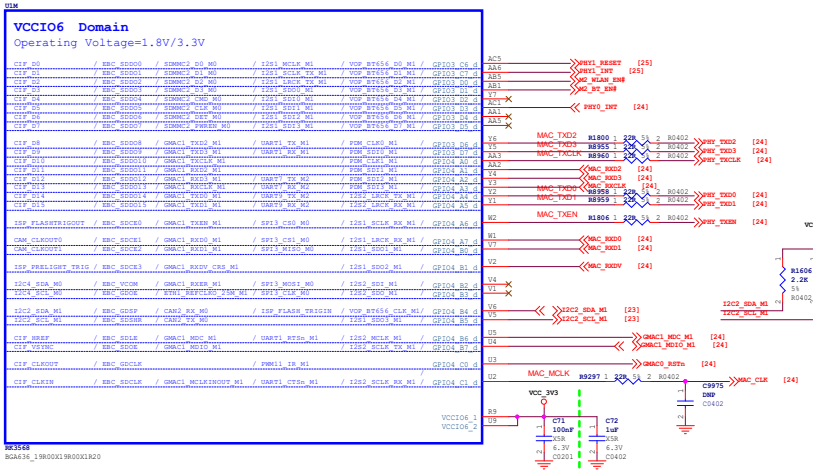
# RK3568_P(MIPI_CSI_RX)




| | | |
|---|---|---|
| Option1 | Sensor1 x4Lane | MIPI_CSI_RX_D0-3<br>MIPI_CSI_RX_CLK0 |
| Option2 | Sensor1 x2Lane<br>+<br>Sensor2 x2Lane | MIPI_CSI_RX_D0-1<br>MIPI_CSI_RX_CLK0 |
| | | MIPI_CSI_RX_D2-3<br>MIPI_CSI_RX_CLK1 |

# RK3568_M(VCCIO6 Domain)




| Mode | 16bit | 12bit | 10bit | 8bit |
|---|---|---|---|---|
| CIF_D0 | D0 | -- | -- | -- |
| CIF_D1 | D1 | -- | -- | -- |
| CIF_D2 | D2 | -- | -- | -- |
| CIF_D3 | D3 | -- | -- | -- |
| CIF_D4 | D4 | D0 | -- | -- |
| CIF_D5 | D5 | D1 | -- | -- |
| CIF_D6 | D6 | D2 | D0 | -- |
| CIF_D7 | D7 | D3 | D1 | -- |
| CIF_D8 | D8 | D4 | D2 | D0 |
| CIF_D9 | D9 | D5 | D3 | D1 |
| CIF_D10 | D10 | D6 | D4 | D2 |
| CIF_D11 | D11 | D7 | D5 | D3 |
| CIF_D12 | D12 | D8 | D6 | D4 |
| CIF_D13 | D13 | D9 | D7 | D5 |
| CIF_D14 | D14 | D10 | D8 | D6 |
| CIF_D15 | D15 | D11 | D9 | D7 |

Support BT601 YCbCr 422 8bit input
Support BT656 YCbCr 422 8bit input
Support RAW 8/10/12bit input
Support BT1120 YCbCr 422 8/10/12/16bit input, single/dual-edge sampling
Support 2/4 mixed BT656/BT1120 YCbCr 422 8bit input

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package



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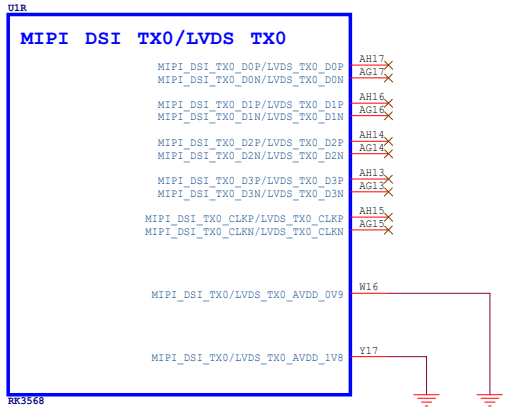
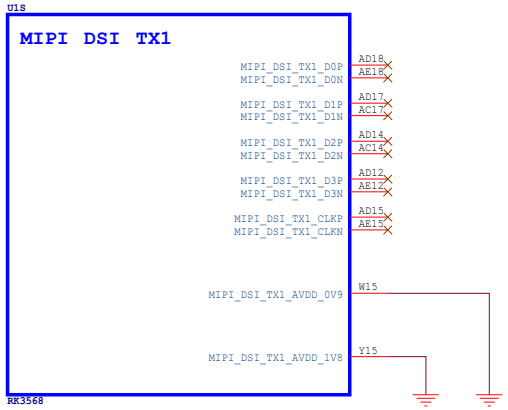
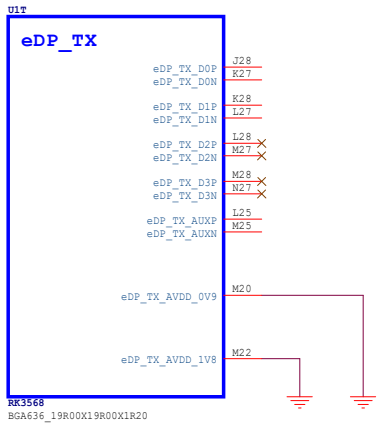
# RK3568_R(MIPI_DSI_TX0/LVDS_TX0)




# RK3568_S(MIPI_DSI_TX1)




# RK3568_T(eDP TX)




**Note:**
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
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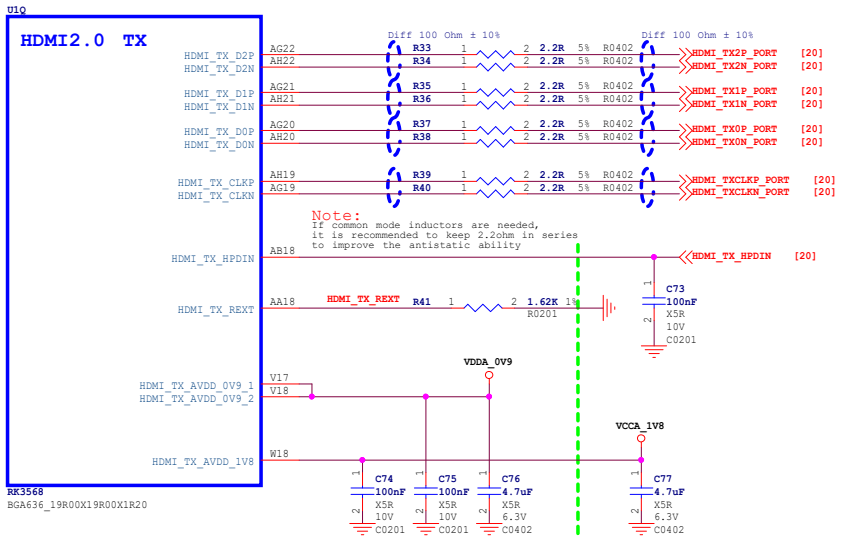
# RK3568_Q(HDMI2.0 TX)

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# RK3568_L(VCCIO5 Domain)

U1L

## VCCIO5 Domain

Operating Voltage=1.8V/3.3V

| | | | | | |
|---|---|---|---|---|---|
| LCDC_D0 | VOP_BT656_D0_M0 | SPI0_MISO_M1 | PCIE20_CLKREQn_M1 | I2S1_MCLK_M2 | GPIO2_D0_d | AG6 |
| LCDC_D1 | VOP_BT656_D1_M0 | SPI0_MOSI_M1 | PCIE20_WAKEn_M1 | I2S1_SCLK_TX_M2 | GPIO2_D1_d | AD7 |
| LCDC_D2 | VOP_BT656_D2_M0 | SPI0_CS0_M1 | PCIE30X1_CLKREQn_M1 | I2S1_LRCK_TX_M2 | GPIO2_D2_d | AC8 |
| LCDC_D3 | VOP_BT656_D3_M0 | SPI0_CLK_M1 | PCIE30X1_WAKEn_M1 | I2S1_SDI0_M2 | GPIO2_D3_d | AC7 |
| LCDC_D4 | VOP_BT656_D4_M0 | SPI2_CS1_M1 | PCIE30X2_CLKREQn_M1 | I2S1_SDI1_M2 | GPIO2_D4_d | AF5 |
| LCDC_D5 | VOP_BT656_D5_M0 | SPI2_CS0_M1 | PCIE30X2_WAKEn_M1 | I2S1_SDI2_M2 | GPIO2_D5_d | AF6 |
| LCDC_D6 | VOP_BT656_D6_M0 | SPI2_MOSI_M1 | PCIE30X2_PERSTn_M1 | I2S1_SDI3_M2 | GPIO2_D6_d | AD6 |
| LCDC_D7 | VOP_BT656_D7_M0 | SPI2_MISO_M1 | UART8_TX_M1 | I2S1_SDO0_M2 | GPIO2_D7_d | AH5 |
| LCDC_CLK | VOP_BT656_CLK_M0 | SPI2_CLK_M1 | UART8_RX_M1 | I2S1_SDO1_M2 | GPIO3_A0_d | AH4 |
| LCDC_D8 | VOP_BT1120_D0 | SPI1_CS0_M1 | PCIE30X1_PERSTn_M1 | SDMMC2_D0_M1 | GPIO3_A1_d | AB8 |
| LCDC_D9 | VOP_BT1120_D1 | GMAC1_TXD2_M0 | I2S3_MCLK_M0 | SDMMC2_D1_M1 | GPIO3_A2_d | AE5 |
| LCDC_D10 | VOP_BT1120_D2 | GMAC1_TXD3_M0 | I2S3_SCLK_M0 | SDMMC2_D2_M1 | GPIO3_A3_d | AG4 |
| LCDC_D11 | VOP_BT1120_D3 | GMAC1_RXD2_M0 | I2S3_LRCK_M0 | SDMMC2_D3_M1 | GPIO3_A4_d | AF4 |
| LCDC_D12 | VOP_BT1120_D4 | GMAC1_RXD3_M0 | I2S3_SDO_M0 | SDMMC2_CMD_M1 | GPIO3_A5_d | AH3 |
| LCDC_D13 | VOP_BT1120_CLK | GMAC1_TXCLK_M0 | I2S3_SDI_M0 | SDMMC2_CLK_M1 | GPIO3_A6_d | AG3 |
| LCDC_D14 | VOP_BT1120_D5 | GMAC1_RXCLK_M0 | | SDMMC2_DET_M1 | GPIO3_A7_d | AH2 |
| LCDC_D15 | VOP_BT1120_D6 | ETH1_REFCLKO_25M_M0 | | SDMMC2_PWREN_M1 | GPIO3_B0_d | AG2 |
| LCDC_D16 | VOP_BT1120_D7 | GMAC1_RXD0_M0 | UART4_RX_M1 | PWM8_M0 | GPIO3_B1_d | AG1 |
| LCDC_D17 | VOP_BT1120_D8 | GMAC1_RXD1_M0 | UART4_TX_M1 | PWM9_M0 | GPIO3_B2_d | AF2 |
| LCDC_D18 | VOP_BT1120_D9 | GMAC1_RXDV_CRS_M0 | I2C5_SCL_M0 | PDM_SDI0_M2 | GPIO3_B3_d | AF1 |
| LCDC_D19 | VOP_BT1120_D10 | GMAC1_RXER_M0 | I2C5_SDA_M0 | PDM_SDI1_M2 | GPIO3_B4_d | AE1 |
| LCDC_D20 | VOP_BT1120_D11 | GMAC1_TXD0_M0 | I2C3_SCL_M1 | PWM10_M0 | GPIO3_B5_d | AE2 |
| LCDC_D21 | VOP_BT1120_D12 | GMAC1_TXD1_M0 | I2C3_SDA_M1 | PWM11_IR_M0 | GPIO3_B6_d | AE3 |
| LCDC_D22 | PWM12_M0 | GMAC1_TXEN_M0 | UART3_TX_M1 | PDM_SDI2_M2 | GPIO3_B7_d | AD4 |
| LCDC_D23 | PWM13_M0 | GMAC1_MCLKINOUT_M0 | UART3_RX_M1 | PDM_SDI3_M2 | GPIO3_C0_d | AD2 |
| LCDC_HSYNC | VOP_BT1120_D13 | SPI1_MOSI_M1 | PCIE20_PERSTn_M1 | I2S1_SDO2_M2 | GPIO3_C1_d | AD1 |
| LCDC_VSYNC | VOP_BT1120_D14 | SPI1_MISO_M1 | UART5_TX_M1 | I2S1_SDO3_M2 | GPIO3_C2_d | AA7 |
| LCDC_DEN | VOP_BT1120_D15 | SPI1_CLK_M1 | UART5_RX_M1 | I2S1_SCLK_RX_M2 | GPIO3_C3_d | AC4 |
| PWM14_M0 | VOP_PWM_M1 | GMAC1_MDC_M0 | UART7_TX_M1 | PDM_CLK1_M2 | GPIO3_C4_d | AC3 |
| PWM15_IR_M0 | SPDIF_TX_M1 | GMAC1_MDIO_M0 | UART7_RX_M1 | I2S1_LRCK_RX_M2 | GPIO3_C5_d | AC2 |
| | | | | | VCCIO5_1 | V10 |
| | | | | | VCCIO5_2 | V11 |

RK3568

BGA636_19R00X19R00X1R20

**Note:**

Caps of between dashed green lines and U1000 should be placed under the U1000 package



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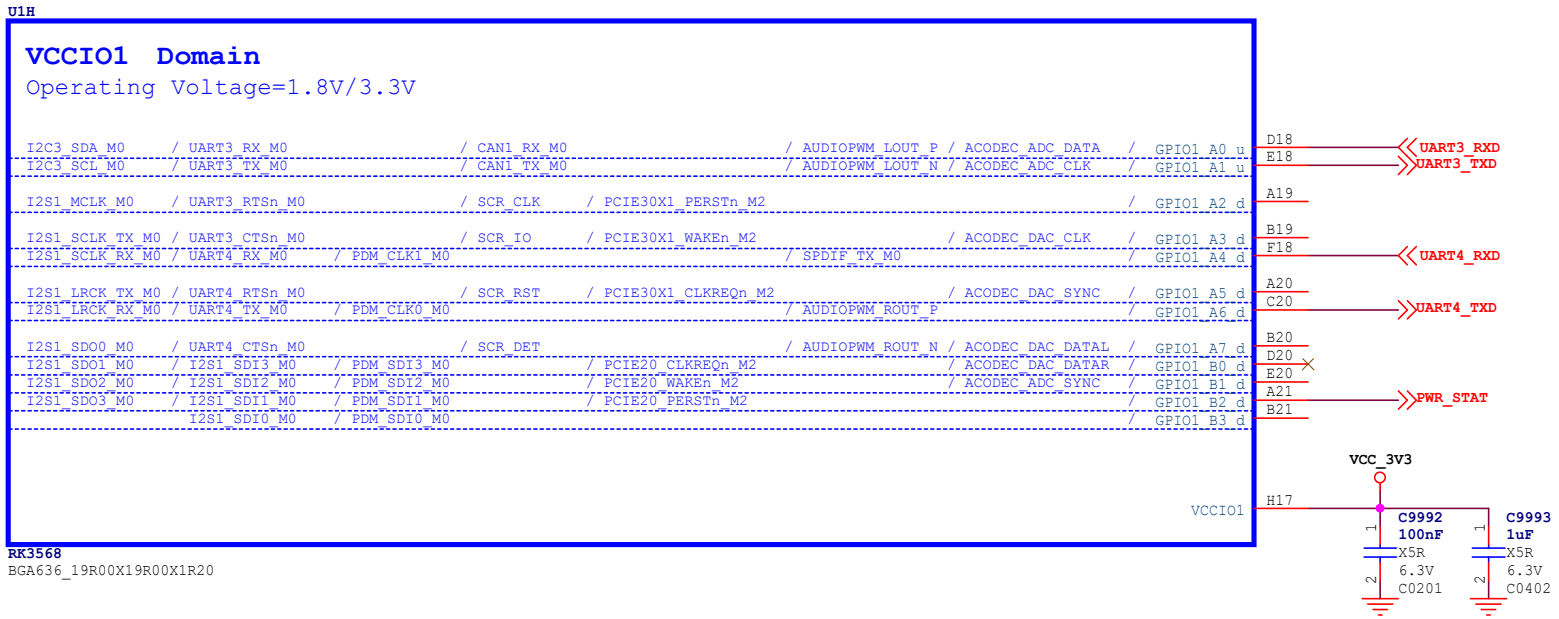
# RK3568_H(VCCIO1 Domain)

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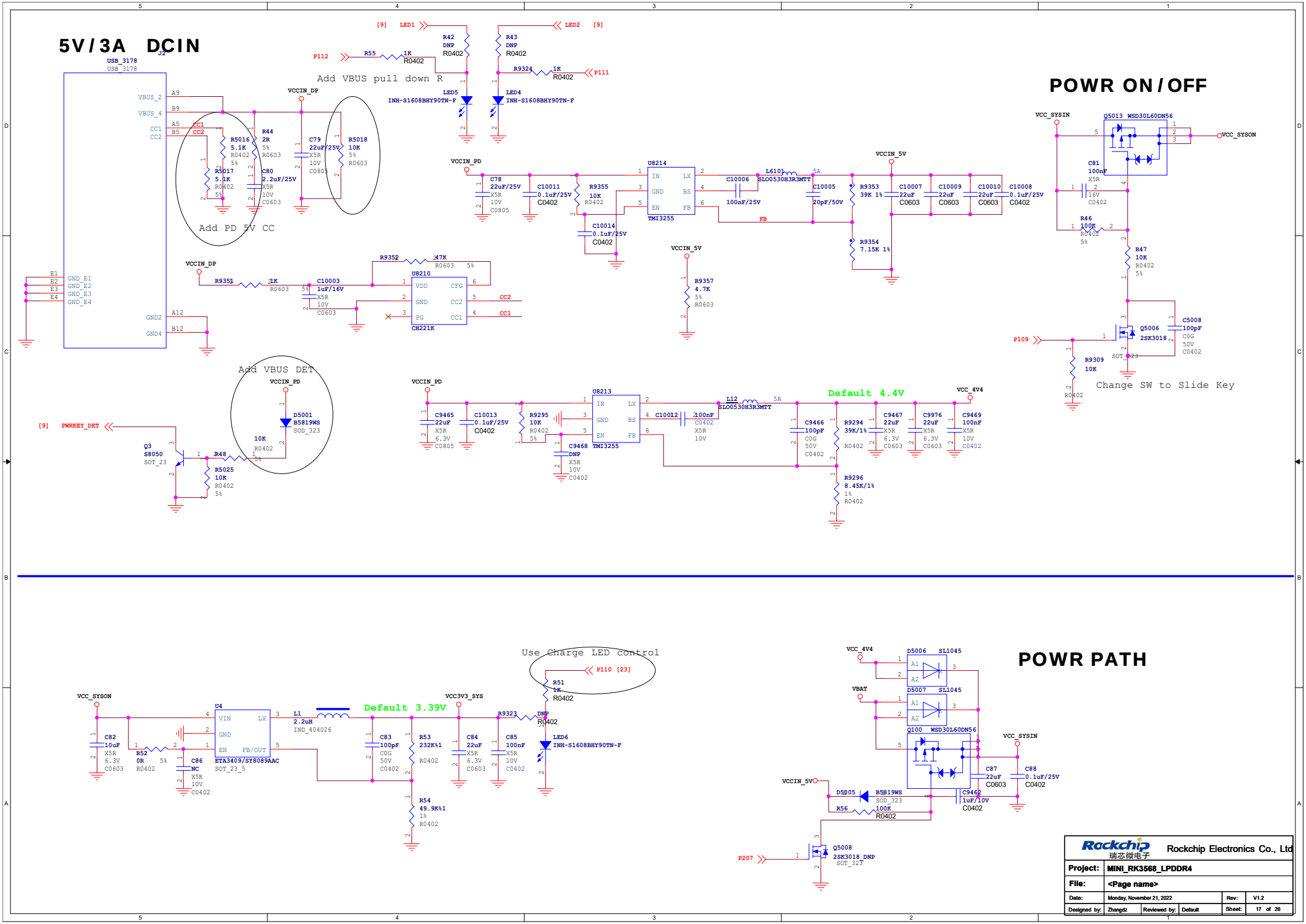


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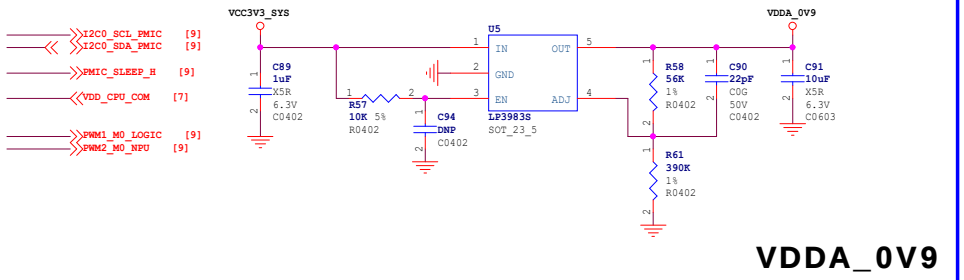
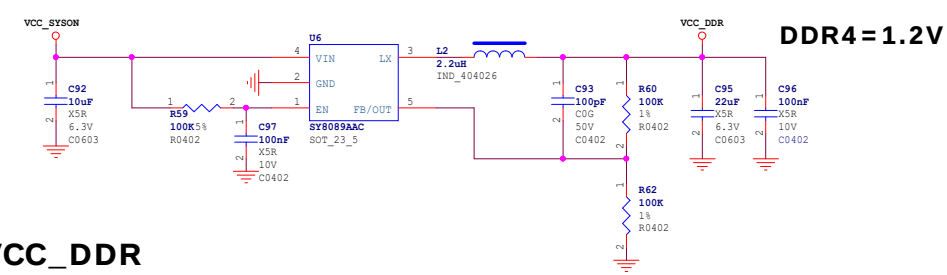



## VDDA_0V9

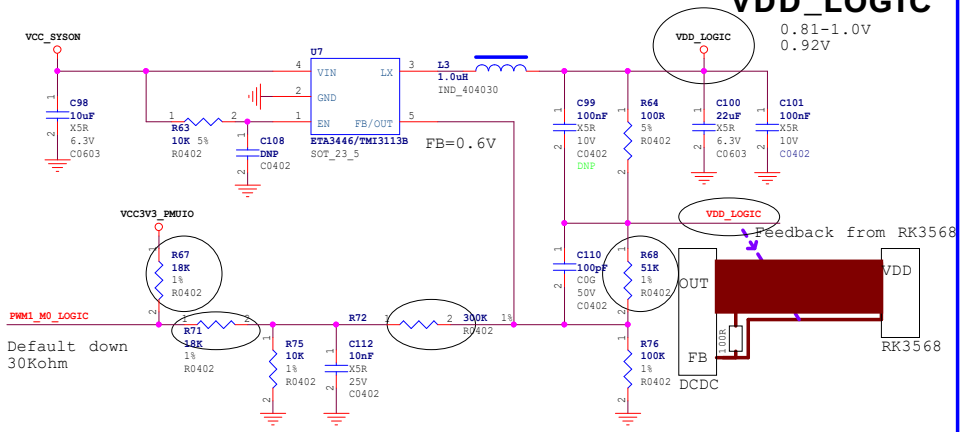



DDR4=1.2V

## VCC_DDR

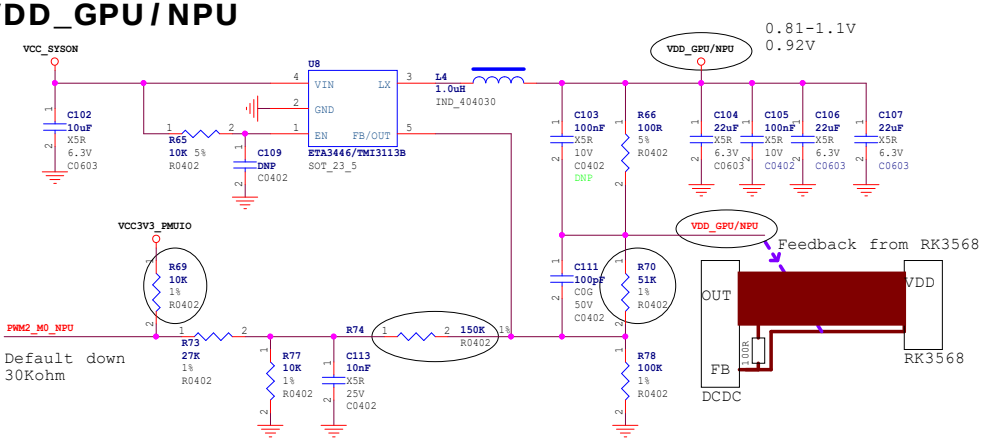
## VDD_LOGIC

0.81-1.0V
0.92V

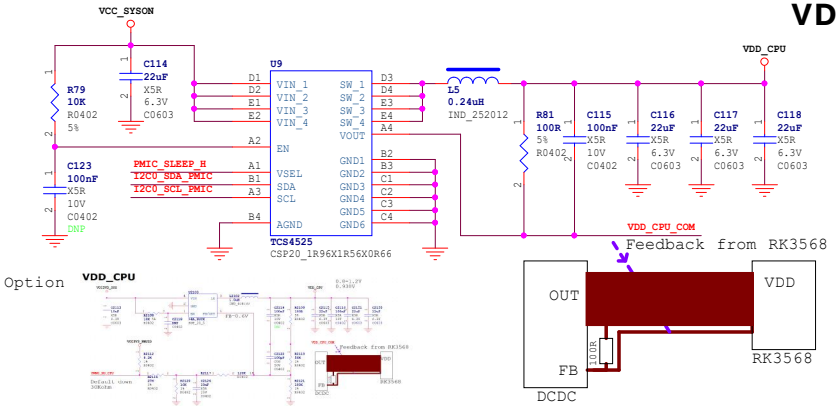



## VDD_GPU/NPU

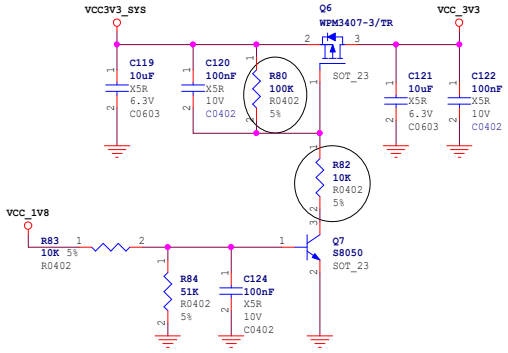
0.81-1.1V
0.92V



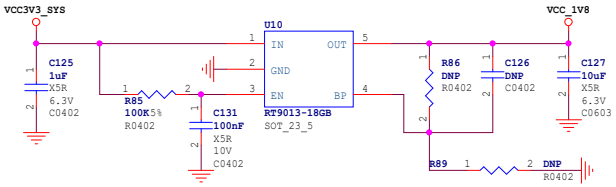

## VDD_CPU



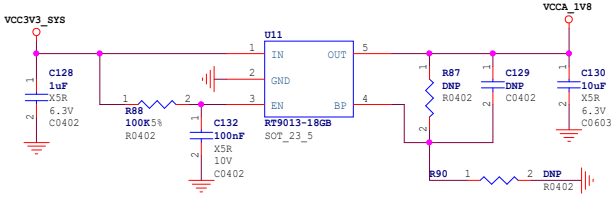

## VCC_3V3




## VCC_1V8




## VCCA_1V8

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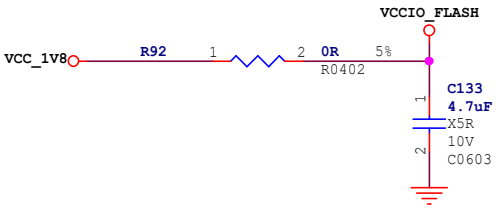
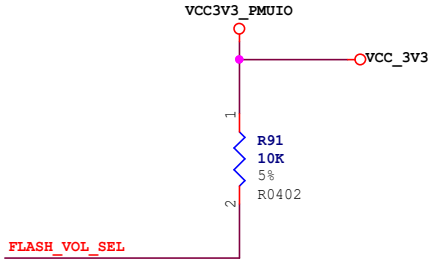
FLASH_VOL_SEL [9]

# Flash Power Manage

| | VCCIO2 domain voltage: Recommend voltage value (VCCIO_FLASH) | FLASH_VOL_SEL state decided to VCCIO2 domain IO driven by default |
|---|---|---|
| eMMC | 1.8V | FLASH_VOL_SEL --> Logic=H |
| Nand flash | Default 3.3V, Adjust according to demand 1.8V | FLASH_VOL_SEL --> Logic=L(Default) |
| SPI flash | Default 3.3V, Adjust according to demand 1.8V | FLASH_VOL_SEL --> Logic=L(Default) |




Note:
FLASH_VOL_SEL state decided
to VCCIO2 domain IO driven by default
Logic=L:3.3V IO driven
Logic=H:1.8V IO driven



| | | | | | |
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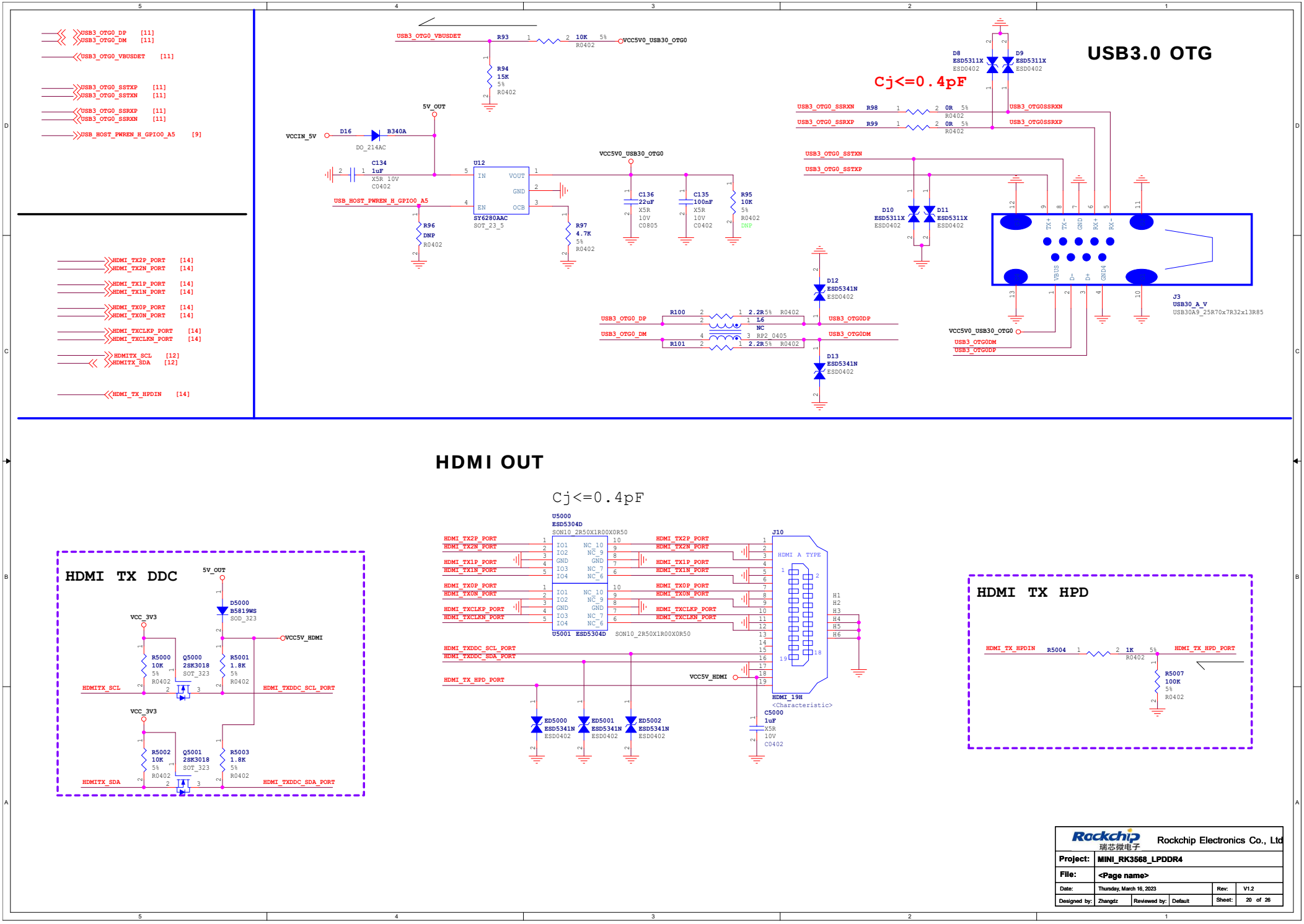
USB3.0 OTG
Cj<=0.4pF
HDMI OUT
Cj<=0.4pF
HDMI TX DDC
HDMI TX HPD
USB3_OTG0_DP [11]
USB3_OTG0_DM [11]
USB3_OTG0_VBUSDET [11]
USB3_OTG0_SSTXP [11]
USB3_OTG0_SSTXN [11]
USB3_OTG0_SSRXP [11]
USB3_OTG0_SSRXN [11]
USB_HOST_PWREN_H_GPIO0_A5 [9]
HDMI_TX2P_PORT [14]
HDMI_TX2N_PORT [14]
HDMI_TX1P_PORT [14]
HDMI_TX1N_PORT [14]
HDMI_TX0P_PORT [14]
HDMI_TX0N_PORT [14]
HDMI_TXCLKP_PORT [14]
HDMI_TXCLKN_PORT [14]
HDMITX_SCL [12]
HDMITX_SDA [12]
HDMI_TX_HPDIN [14]
VCC5V0_USB30_OTG0
VCC5V_HDMI
VCC_3V3
5V_OUT
VCCIN_5V
SY6280AAC
ESD5311X
ESD5341N
HDMI_19H
USB30_A_V
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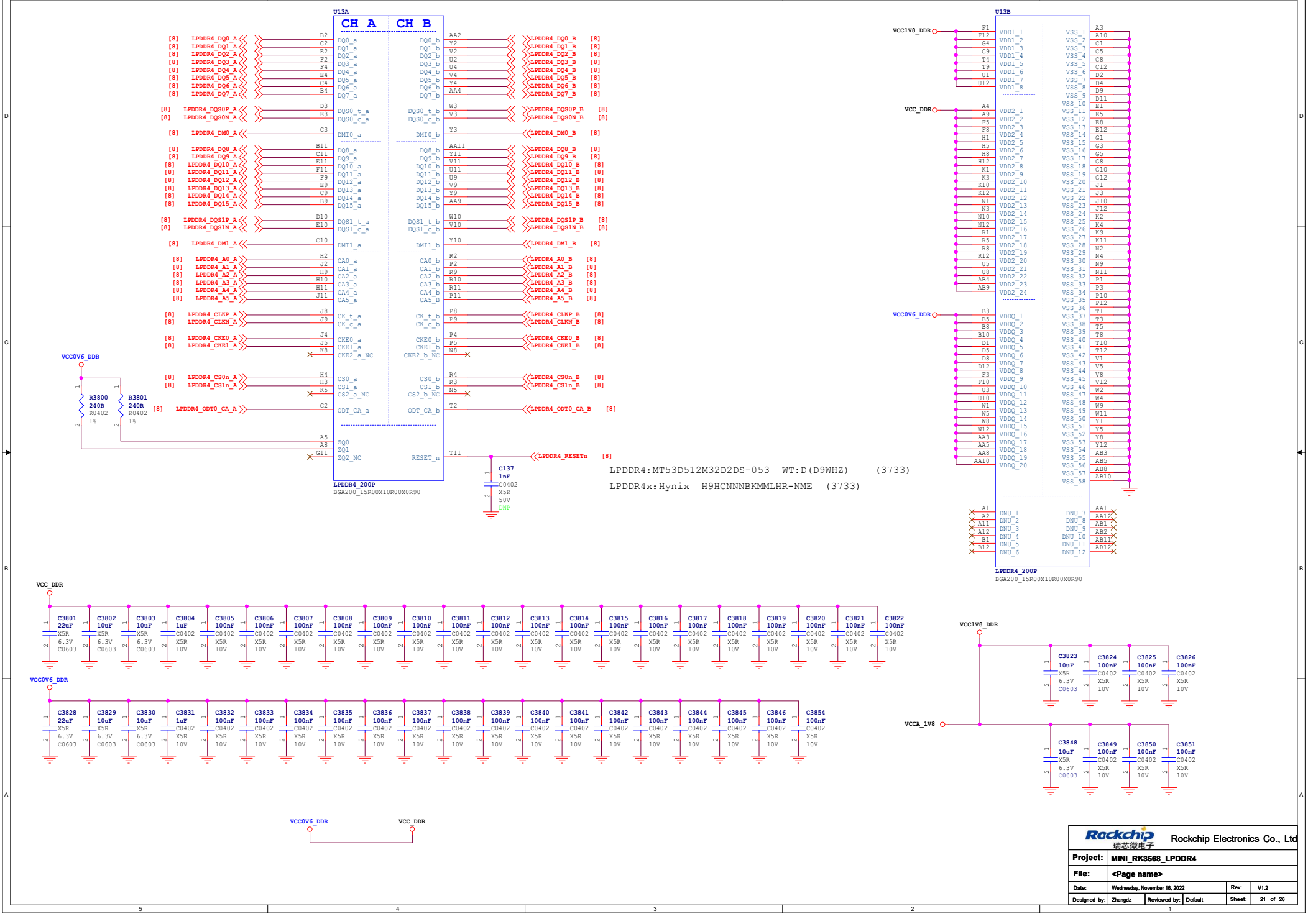
U13A
CH A
CH B
LPDDR4_200P
BGA200_15R00X10R00X0R90
U13B
VCC1V8_DDR
VCC_DDR
VCC0V6_DDR
LPDDR4:MT53D512M32D2DS-053 WT:D(D9WHZ) (3733)
LPDDR4x:Hynix H9HCNNNBKMMLHR-NME (3733)
R3800 240R R0402 1%
R3801 240R R0402 1%
C137 1nF C0402 X5R 50V DNP
VCCA_1V8
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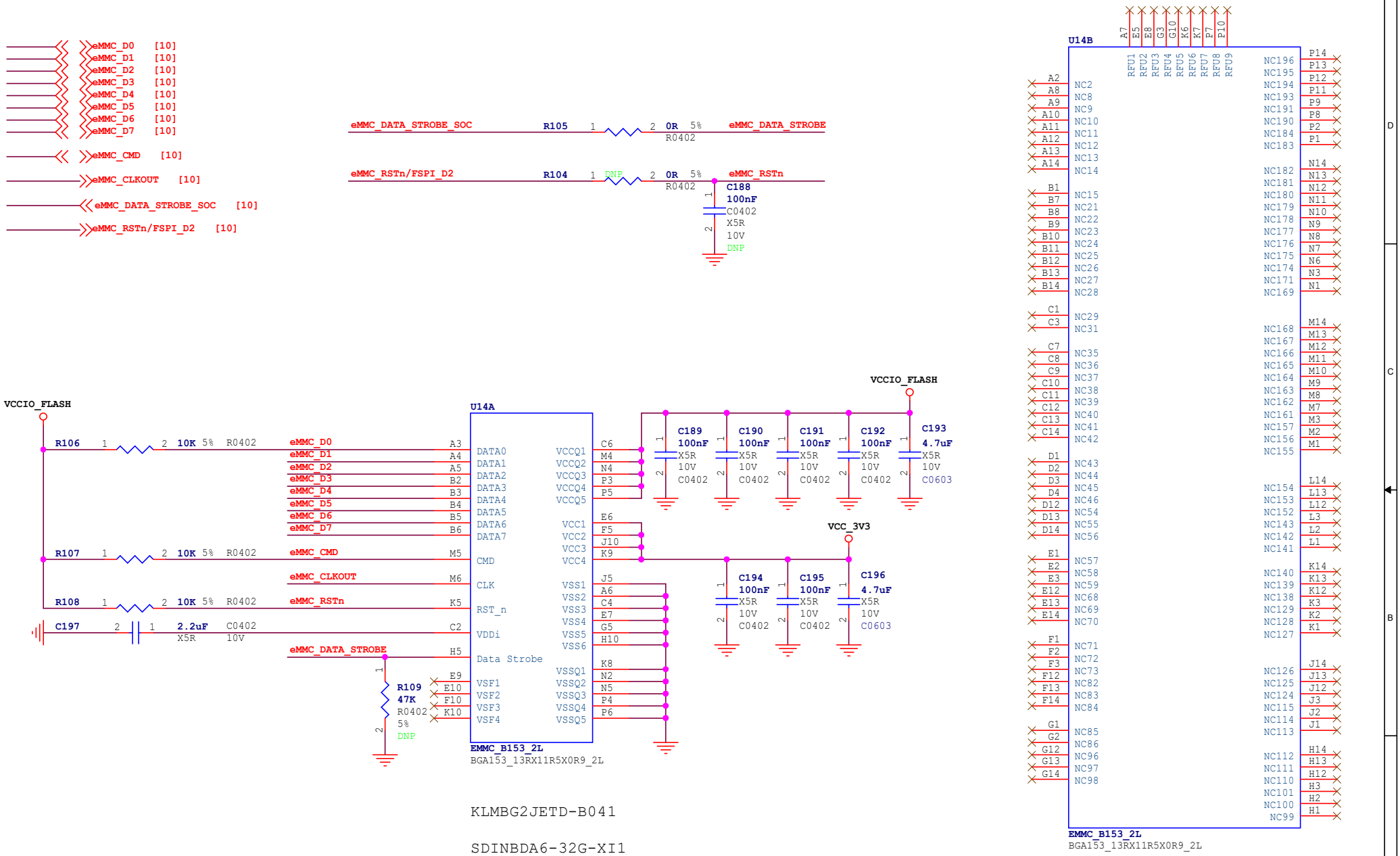


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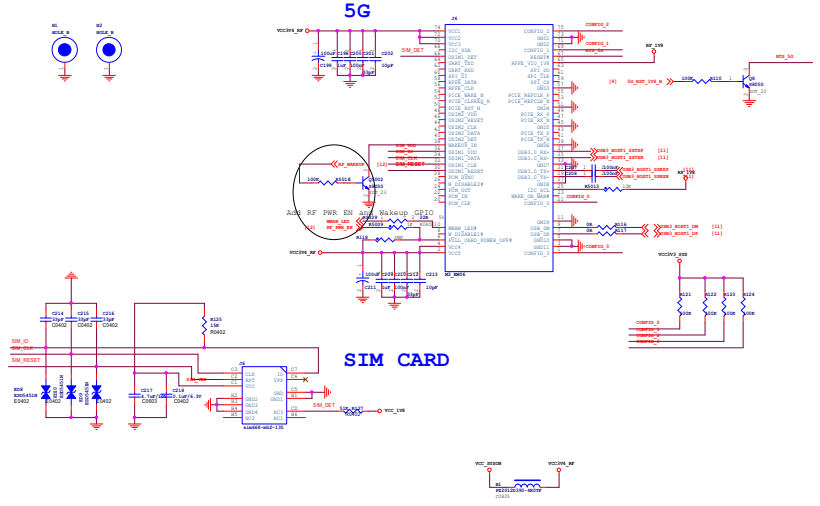


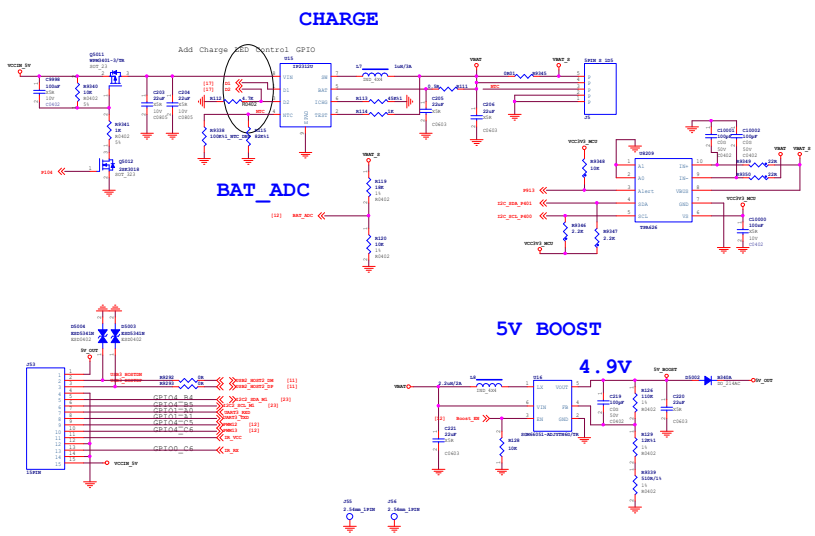


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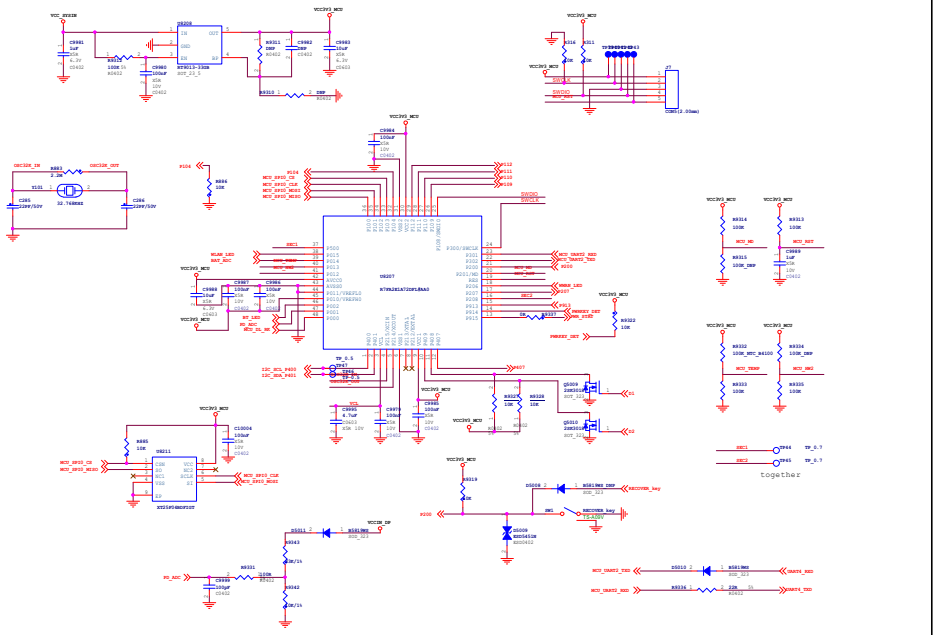


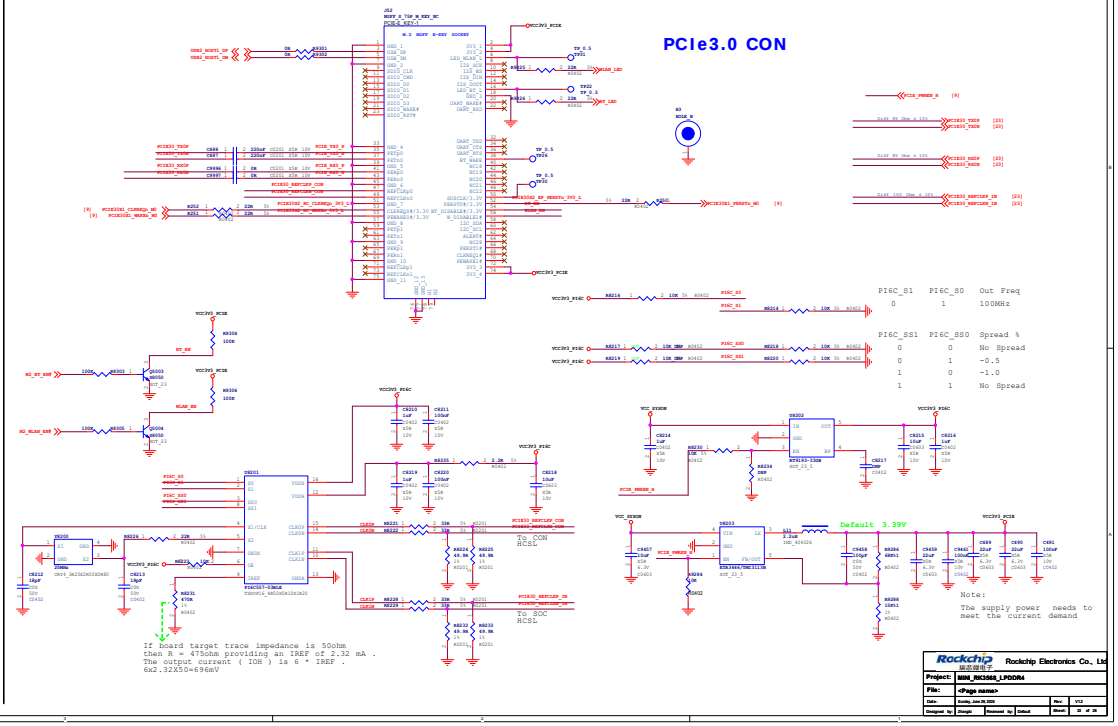


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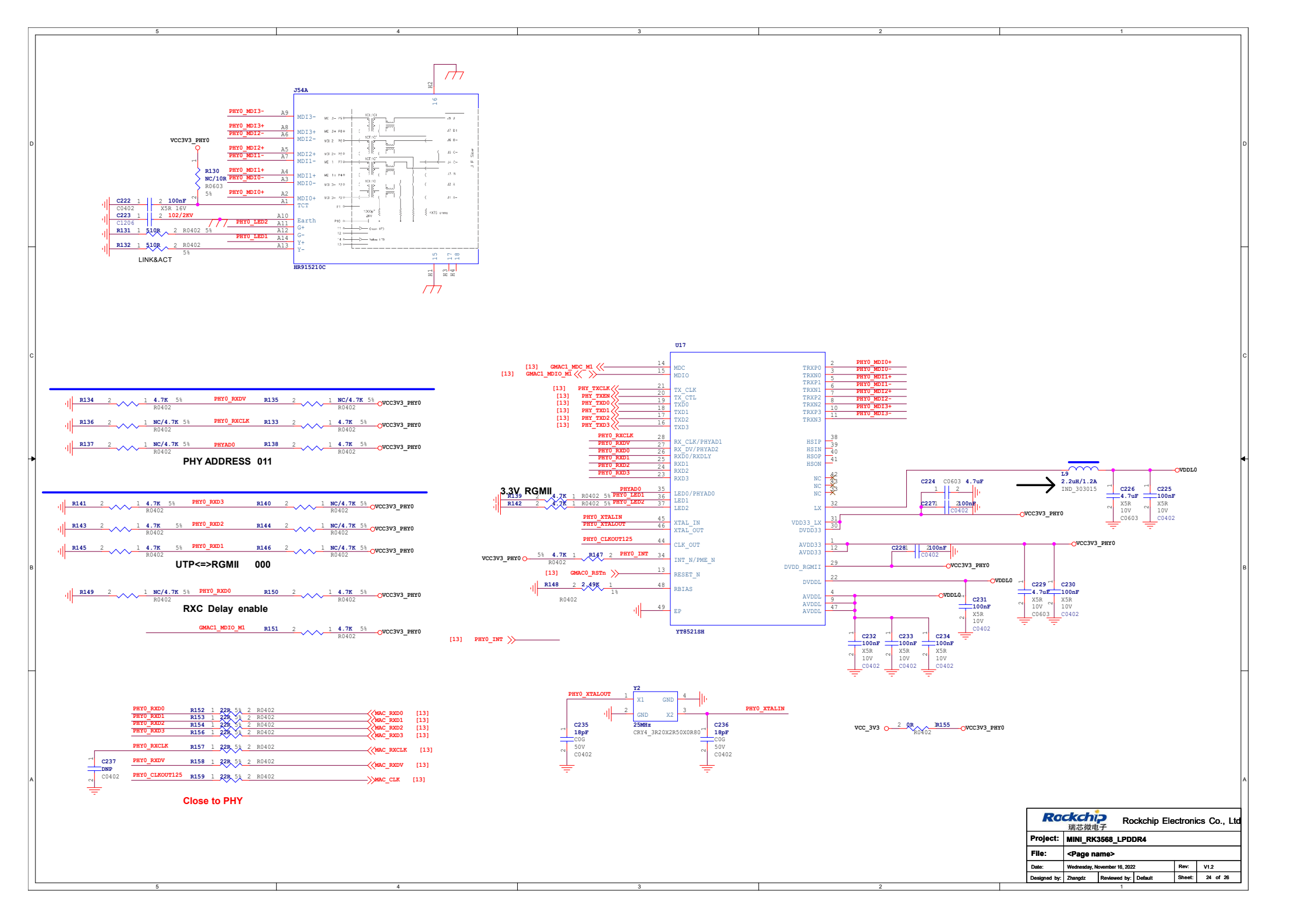


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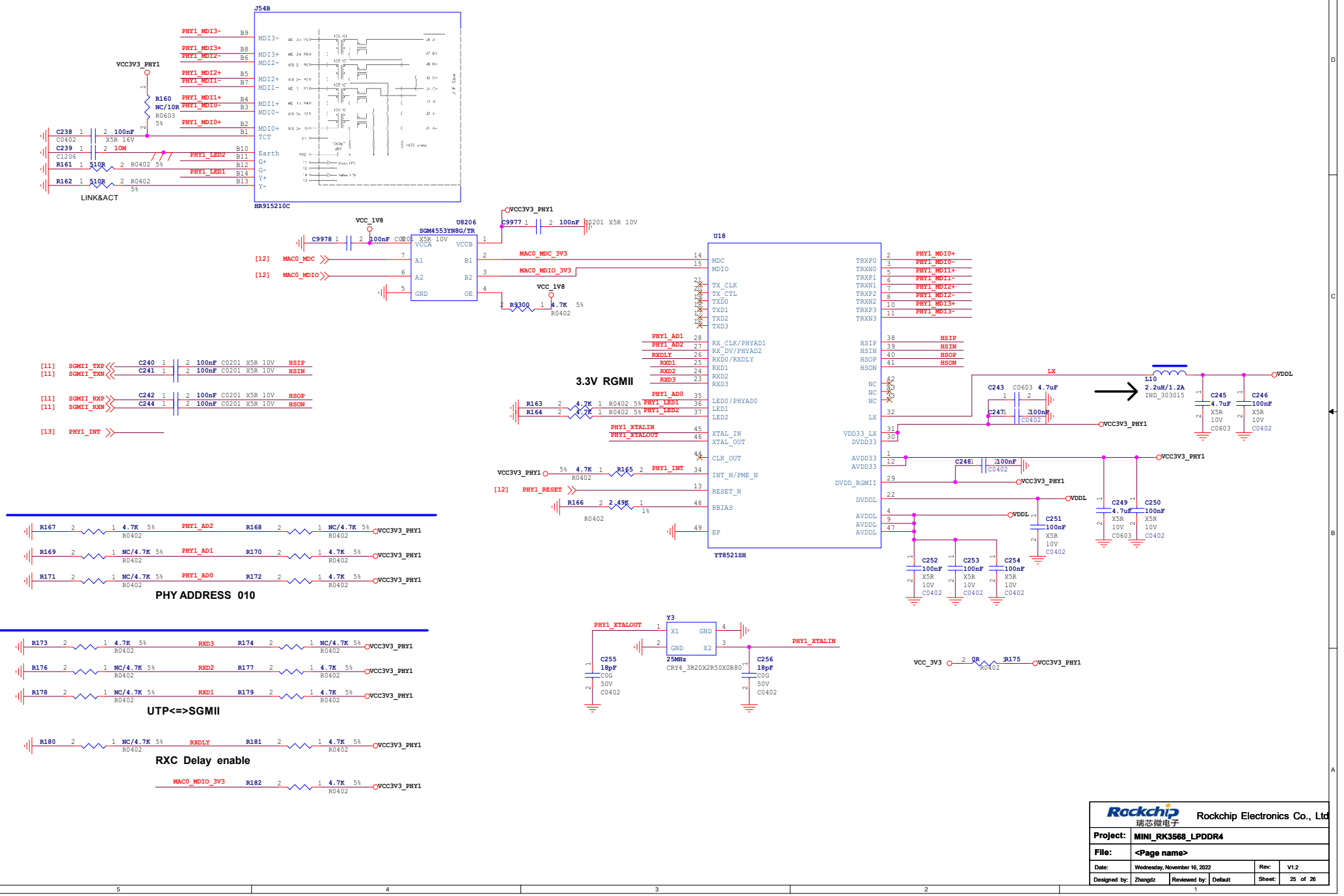
J54B
HR915210C
LINK&ACT
U8206
SGM4553YN8G/TR
U18
YT8521SH
3.3V RGMII
PHY ADDRESS 010
UTP<=>SGMII
RXC Delay enable
Y3
25MHz
L10
2.2uH/1.2A
IND_303015
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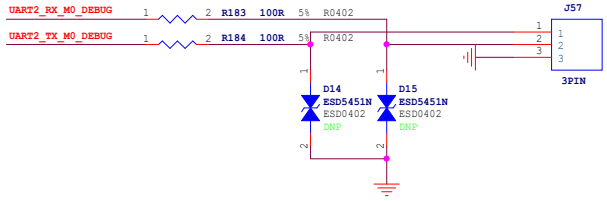
# Debug UART2

UART2_RX_M0_DEBUG [9]
UART2_TX_M0_DEBUG [9]



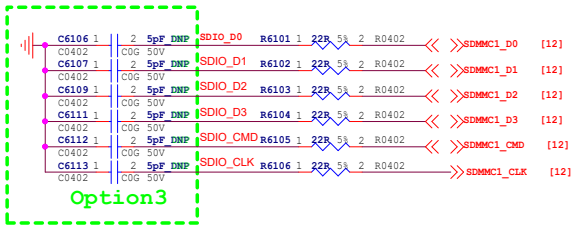

Option0

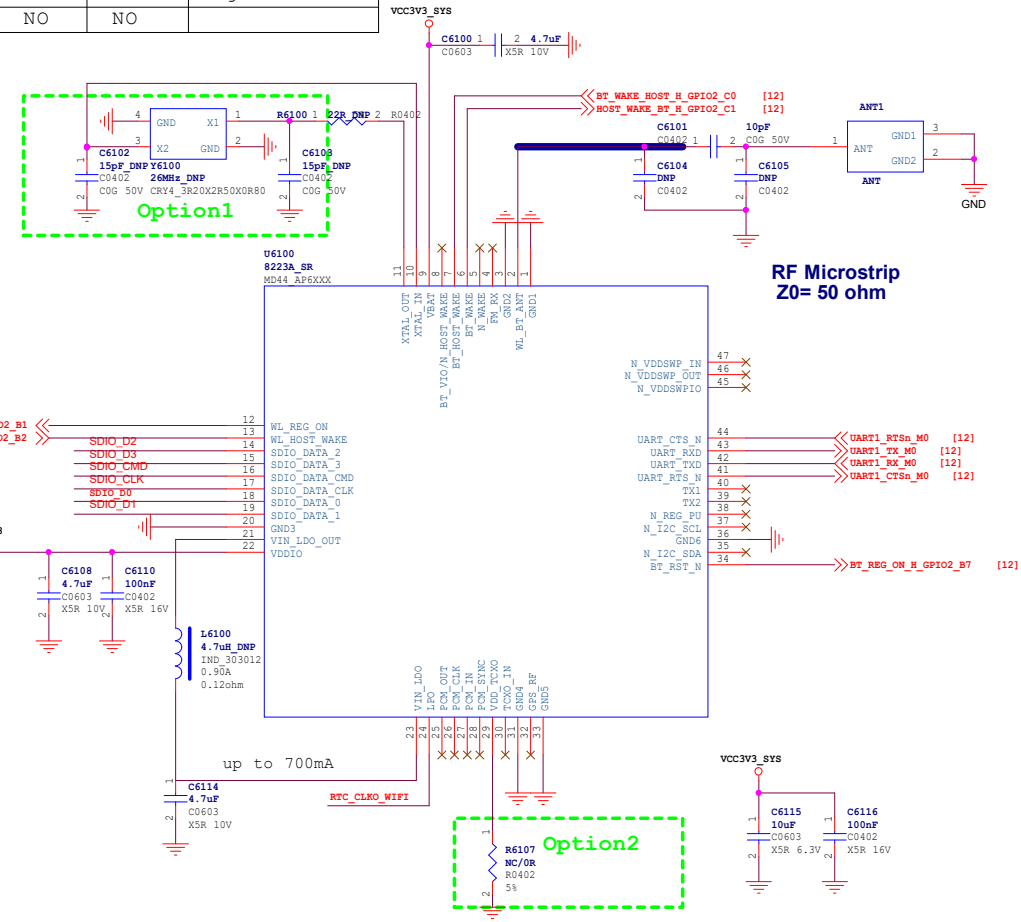
# SDIO WIFI/BT MODULE

Note:VBAT电压范围3.0V~4.8V，
能够至少0.2A

YES：根据要 贴 ;NO:根据 不贴

| | Option1 | Option2 | Option3 | |
|---|---|---|---|---|
| AP6212 | 26MHz | NO | NO | |
| AP6330 | 26MHz | NO | NO | |
| AP6335 | 37.4MHz | YES | YES | b/g/n/ac |
| XZ3660 | 26MHz | NO | NO | |

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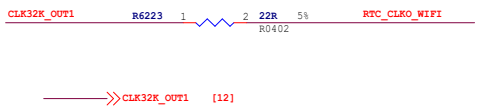


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