Programmable 14+1 Channel Voltage Buffers with NVM for TFT LCD

Features

- **Supply Operation Range : 6.5V to 18V**
- **14+1 Channels :**
  - **---14 Channel Rail-to-Rail Programmable Gamma Buffers**
    - **10 bits Resolution for each Channel**
    - **25mA Output Current for each Channel**
    - **2 Banks Registers Using Bank_Sel to Select which Bank Data Output**
  - **---1 Channel Rail-to-Rail Vcom Buffer:**
    - **7 Bits Adjustable Output**
    - **±100mA Output Current**
    - **±260mA Output Short-Circuit Current**
    - **20V/μs Slew Rate**
- **2-Wire I²C Slave Mode Interface**
- **Using One Control Pin Enable to Store Data into Non-Volatile Memory (NVM)**
- **Non-Volatile Memory (NVM) Store Setting (at Least 100 Re-Write Times)**
- **QFN5X5-32 Package**

Applications

- **TFT-LCD Monitors**
- **LCD Televisions**

General Description

The G1632 consists of 14+1 channel buffers target toward the needs of thin film transistor liquid crystal display (TFT LCD). This device incorporates one Vcom buffer and 14 gamma buffers, and are programmed through I²C interface. It contains two register banks which can store two different sets of gamma reference values. Each buffer is capable of driving heavy capacitive loads and offering large current loading (Vcom: 100mA, Gammas: 25mA).

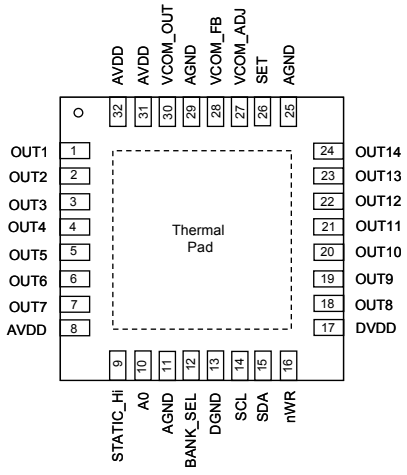
The G1632 is available in the QFN5X5-32 package.

Ordering Information

ORDER NUMBER	MARKING	TEMP. RANGE	PACKAGE (Green)
G1632QA1U	1632	-40°C to 85°C	QFN5X5-32
G1632QA1R	1632	-40°C to 85°C	QFN5X5-32

Note: QA:QFN5X5-32
1: Bonding Code
U: Tape & reel R: Tray
Green : Lead Free / Halogen Free

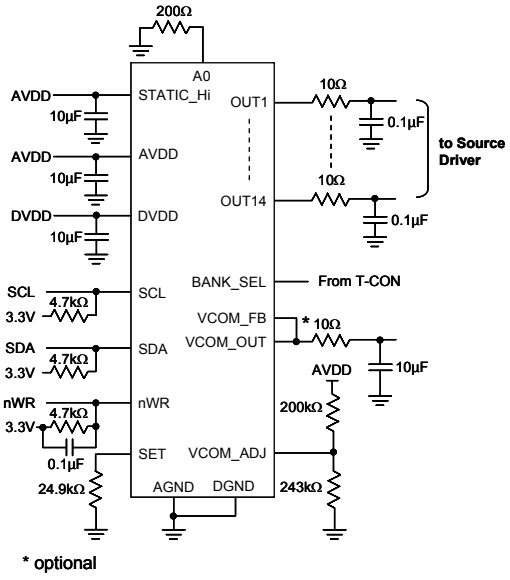
Pin Configuration



G1632 QFN5X5-32

Note: Recommend connecting the Thermal Pad to the Ground for excellent power dissipation.

Typical Application Circuit



* optional

Absolute Maximum Ratings

AVDD, STATIC_Hi to AGND. . . . . -0.3V to +20V
DVDD to DGND . . . . . .-0.3V to +4V
DGND to AGND . . . . . -0.3V to +0.3V
VCOM_FB, VCOM_ADJ to AGND . . . . . .-0.3V to +20V
BANK_SEL, A0, SCL, SDA, nWR, SET to AGND . . . . . -0.3V to +4V
VCOM_OUT, OUT_(*1) to AGND . . -0.3V to (AVDD+0.3V)
VCOM Maximum Continuous Output Current . . . . . -260mA to +260mA
OUT1~OUT14 Maximum Continuous Output Current . . . . . -100mA to +100mA
Thermal Resistance Junction to Ambient, (θ_{JA})
QFN5X5-32. . . . . 52.18C/W(*2)
Continuous Power Dissipation (T_A=25°C)
QFN5X5-32 . . . . . .2.396W(*2)
Thermal Resistance Junction to Case, (θ_{JC})
QFN5X5-32 . . . . . 5.2074°C/W
Storage Temperature Range . . . . . -65°C to 150°C
Junction Temperature . . . . . .150°C
Reflow Temperature (soldering, 10sec) . . . . . 260°C
ESD (HBM) 2000V
Machine Mode (MM) 200V

Recommend Operating Range

Operating Supply Voltage Range . . 6.5V ≤ V_{DD} ≤ 18V
Operating Temperature Range . . . . . .-40°C to 85°C

* Note 1: The _ is number define, ex OUT1, OUT2, we define OUT_.
* Note 2: Please refer to 1in^2 of 1oz PCB Layout Section.

Electrical Characteristics

The following specifications apply for the typical application circuit unless otherwise specified.

DVDD = 3V; AVDD=16.5V, AGND=DGND= 0V; T_{amb} = 25°C; R_L=10kΩ; C_L=10pF

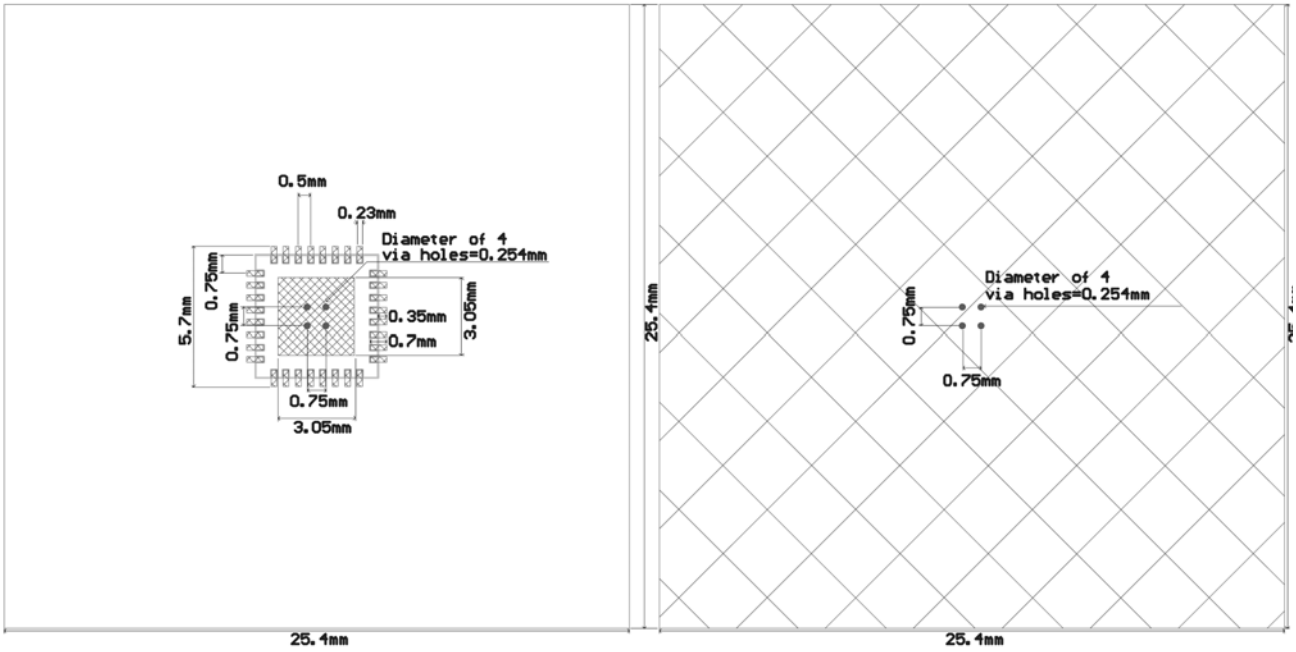
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNIT
General							
Power Supply	AVDD			6.5	---	18	V
	DVDD			2.3	---	3.6	V
$UVLO_{DVDD}$	$UVLO_{DVDD}$			---	---	2.2	V (*)
Supply Current	Iq	Gamma code=512,	AVDD	---	16	24	mA
		V_{COM} code=64, No loading	DVDD	---	400	600	µA
Thermal Shutdown	T_{SD}			---	150	---	°C
Gamma Buffers							
Quiescent Current	$I_{S(OUT\_)}$	Per-Channel, no loading		---	500	---	µA
Output Swing High	V_{OH}	No loading, AVDD=16.5V,	OUT1 to OUT7	---	---	STATIC_Hi	V
		DAC =1023	OUT8 to OUT14	---	---	STATIC_Hi-1.5	
Output Swing Low	V_{OL}	No loading, AVDD=16.5V,	OUT1 to OUT7	1.5	---	---	V
		DAC=0	OUT8 to OUT14	0	---	---	
Power Supply Rejection Ratio	PSRR	AVDD=6.5V to 18V		45	70	---	dB
Load Regulation		OUT=AVDD/2; I_{SINK}=I_{SOURCE}=20mA			0.3	1.5	mV/mA
Slew Rate	SR			8	16	---	V/µs
Band width	BW			4	10	---	MHz
Output Current	I_{OUT}			---	±25	---	mA
Short-Circuit Current	I_{SC}			---	±100	---	mA
STATIC Hi Voltage	V_{STATIC_Hi}	Ref. High Voltage Range		AVDD-4	---	AVDD	V
Program to Out Delay	T_D	No loading		---	4	8	µs
DROP Voltage period	T_{DROP}			---	---	10	µs
Full-Scale Error		AVDD=16.5V		-4	---	+4	LSB
Integral Nonlinearity	INL	V_{STATIC_Hi} =16V, No loading, AVDD=16.5V		-4	---	+4	LSB
Differential Nonlinearity	DNL	V_{STATIC_Hi} =16V, No loading, AVDD=16.5V		-1	---	+1	LSB

Electrical Characteristics (continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
VCOM Buffers						
Quiescent Current	I_{COM}	Buffer configuration, V_{COM_FB}=VAVDD/2, no load	---	3	---	mA
Output Voltage Swing, High	V_{OH}	I_{COM_OUT} = 100µA	AVDD-20	AVDD-5	---	mV
		I_{COM_OUT} = 100mA	AVDD-1.5	AVDD-1.3	---	V
Output Voltage Swing, Low	V_{OL}	I_{COM_OUT} = -100µA	---	2	20	mV
		I_{COM_OUT} = -100mA	---	1.5	1.8	V
Output Current	I_{OUT}	to AVDD/2	---	±100	---	mA
Short-Circuit Current	I_{SC}	to AVDD/2	---	±180	---	mA
Slew Rate	SR		20	70	---	V/µs
-3dB Bandwidth	F_{3dB}	R_L=10kP, C_L=10pF, buffer configuration	13	19	---	MHz
I^2C Control						
Logic-Input Low Input	V_{IL}	SCL, SDA	---	---	0.3*DVDD	V
Logic-Input High Input	V_{IH}	SCL, SDA	0.7*DVDD	---	---	V
SCL Clock Frequency	F_{SCL}		0	---	400	kHz
I^2C Clock High Level	T_{SCHi}		0.6	---	---	µs
I^2C Clock Low Level	T_{SCLo}		1.2	---	---	µs
I^2C Data Set-up Time	T_{SDS}		100	---	---	ns
I^2C Data Hold Time	T_{SDH}		0	---	900	ns
SDA and SCL Rise Time	T_R		---	---	1000	ns
SDA and SCL Fall Time	T_F		---	---	300	ns
SDA and SCL Input Capacitance			---	5	---	pF
Start Condition of Setup Time	T_{STS}		0.6	---	---	µs
Start Condition of Hold Time	T_{STH}	10% of SDA to 90% of SCL	0.6	---	---	µs
I^2C Input Filter Spike Suppression	T_{SP}		---	---	50	ns
Bus Free Time Between Stop to Start	T_{BUF}		4.7	---	---	µs
A0 Pull-Up Resistance	R_{A0}		80	110	140	kΩ
nWR Pull-Up Resistance	R_{nWR}		7	10	14	kΩ
Sink Current Adjustment						
SET Voltage Resolution			7	---	---	Bits
SET Differential Nonlinearity		Monotonic over-temperature	-1	---	+1	LSB
SET Zero-Scale Error			-1	+1	+2	LSB
SET Full-Scale Error			-4	---	+4	LSB
SET Current	I_{SET}		---	---	120	µA
V_{SET}/V_{AVDD} Voltage Ratio		DAC full Scale	0.045	0.050	0.055	V/V

* : 2.4V @ RT = 85 degree, 2.2V @RT = 70 degree

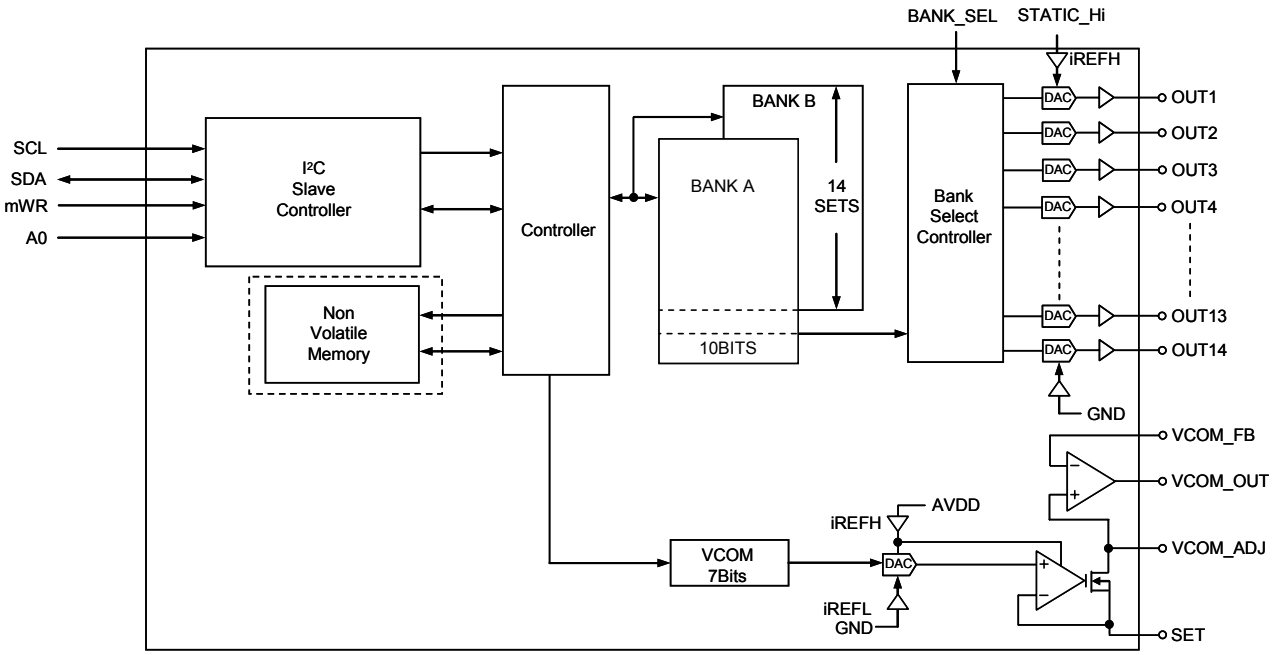
1in^2 of 1oz PCB Layout Section



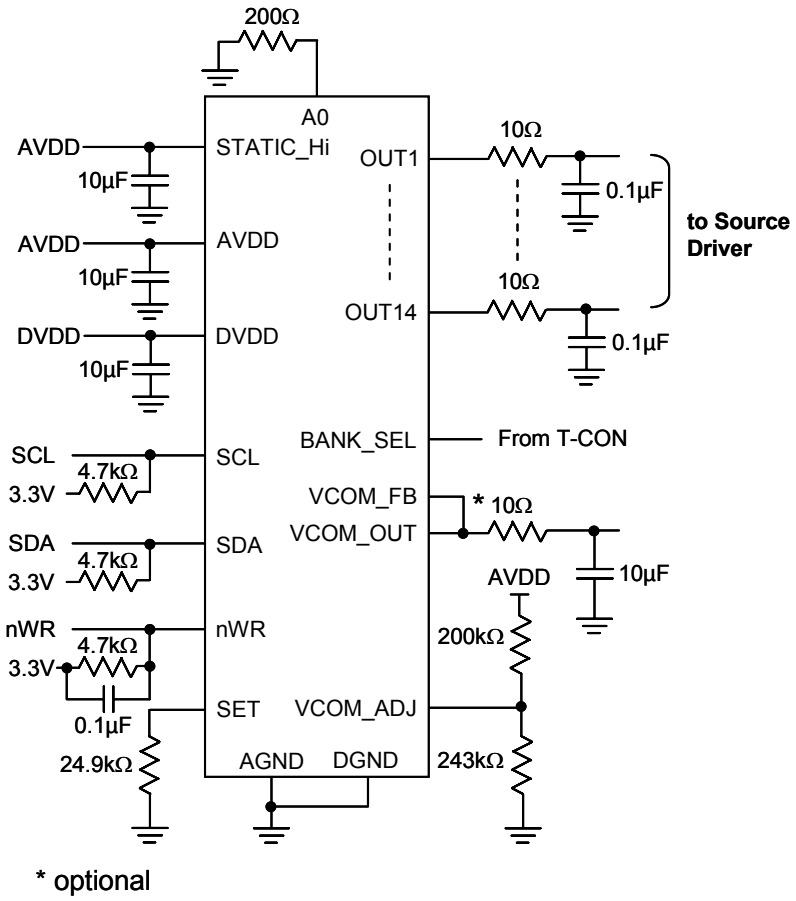
Pin Descriptions

PIN	NAME	I/O	FUNCTION
1	OUT1	O	Analog Output 1
2	OUT2	O	Analog Output 2
3	OUT3	O	Analog Output 3
4	OUT4	O	Analog Output 4
5	OUT5	O	Analog Output 5
6	OUT6	O	Analog Output 6
7	OUT7	O	Analog Output 7
8,31,32	AVDD	P	Analog Power Supply
9	STATIC_Hi	I	High Reference for OUTPUT Voltage
10	A0	I	Device Address Select (A0 : Low => Address (0x74), A0: High => Address (0x75))
11,25,29	AGND	-	Analog Ground
12	BANK_SEL	I	Internal A/B Bank Select(Lo : Bank A; Hi : Bank B)
13	DGND	-	Digital GND
14	SCL	I	I^2C-Compatible Clock Input
15	SDA	B	I^2C-Compatible Serial Bidirectional Data Line
16	nWR	I	Enable/Disable write data into Non-Volatile Memory. If nWR equal Low, it can write data into Non-Volatile Memory(Normal-High, Active-Low)
17	DVDD	P	Digital Power Supply
18	OUT8	O	Analog Output 8
19	OUT9	O	Analog Output 9
20	OUT10	O	Analog Output 10
21	OUT11	O	Analog Output 11
22	OUT12	O	Analog Output 12
23	OUT13	O	Analog Output 13
24	OUT14	O	Analog Output 14
26	SET	I	Full-Scale Sink-Current Adjustment Input
27	VCOM_ADJ	O	Adjust Sink-Current Output. This Pin connects to the resistive voltage-divider between AVDD and GND that sets the VCOM voltage
28	VCOM_FB	I	Internal Vcom OP FB signal
30	VCOM_OUT	O	Voltage OUT for VCOM use
Thermal Pad			Thermal Pad connect to AGND

Block Diagram

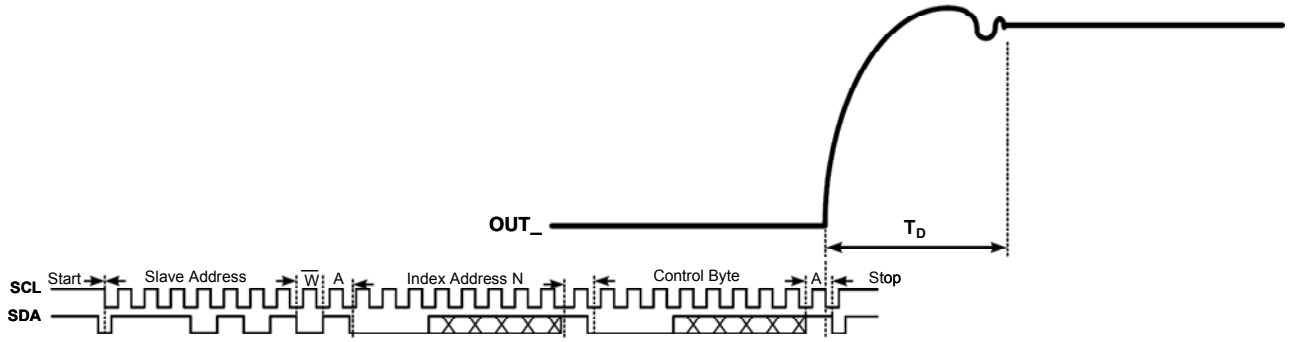


Typical Application Circuit



Application Information

The G1632 provide 14 channels of programmable voltage reference and 1 channel of static voltage references and GND for gamma correction in TFT-LCD display. It contains two register banks can store two different sets of gamma reference values. Gamma values are programmed into the banks through the I^2C interface and the outputs can switch within T_D.



Output Buffers

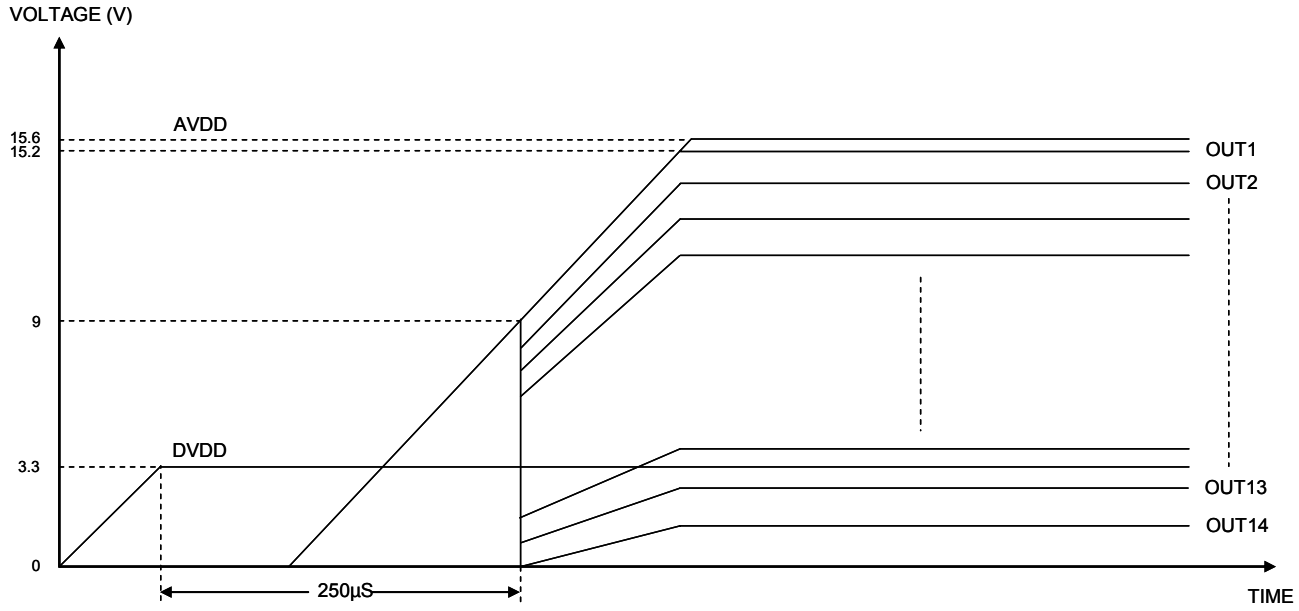
Gamma Buffer Output Value determined by the Ref. Voltage (STATIC_Hi, GND) and the decimal value of the binary code. The Value is calculated using below Equation.

V_{OUT} = [(STATIC_Hi) / 1024*Decimal Value].

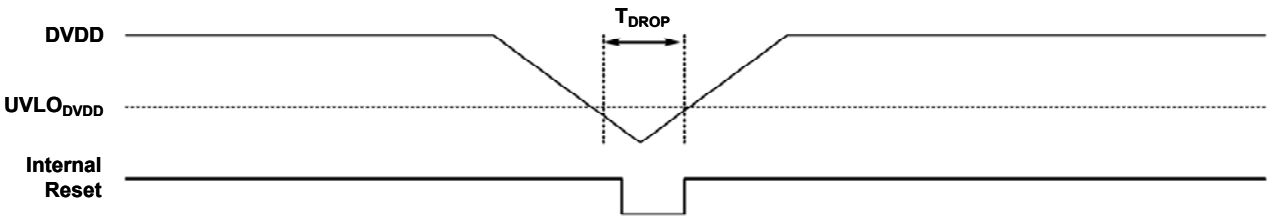
Decimal value is transfer from input binary code.

Power on Sequence

The Buffer can be powered using an analog voltage and digital voltage. The digital supply must be applied prior to the analog supply to avoid excessive current and power consumption.



Once digital supply excess UVLO, all register will be released from zero state to normal state. After power on State, the outputs are in high-impedance mode until data have been written to registers from NVM. If the DVDD power drop to UVLO than recover to DVDD excess than TDROP, the internal logic will reset. The same as reset process, the NVM data will re-download to registers, and the outputs are in high-impedance mode until data have been written to registers from NVM.



Thermal-Overload Protection

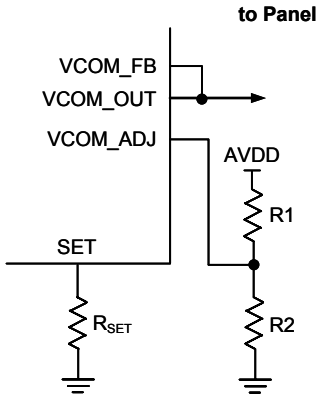
Thermal-overload protection prevents excessive power dissipation from overheating the G1632. When the junction temperature exceeds T_J = 150°C, a thermal sensor active the fault protection, which shuts down all outputs except the reference, allowing the device to cool down. It will reactivate the device when power turn on again. The protection will base on the control byte (B6). The default setting is enable (B6 = Low). If the Bit6 = high, the thermal sensor will disable. The setting value will keep until control byte setting change.

Register Banks

The IC features two register banks: Bank A and Bank B. The user can program one set of gamma values into Bank A and the other set of gamma values into Bank B. The P-Gamma can output Bank A or Bank B by H/W BANK_SEL pin. (Lo : Bank A; Hi : Bank B)

VCOM Application

The Device also provides the ability to reduce the flicker of an LCD Panel by adjustment of the VCOM voltage during production test and alignment. A 128-Step resolution is provide under digital control. The output is connected to an external voltage divider, so that the device will have the capability to reduce the voltage on the output by increasing the output sink current. The adjustment of the output is provided by the I^2C interface.



I_{OUT} = (Setting/128)*(AVDD/(20*RSET)).

V_{OUT} = (R2/(R1+R2))*AVDD*(1-(Setting/128)*(R1/(20*R_{SET}))

RSET Resistor

The External resistor sets the full-scale sink current that determines the lowest voltage of the external voltage divide R1 and R2. The maximum I_{SET} current has to be less than 120μA. The minimum RSET resistor with AVDD equal to 10V is 4.17kΩ. Table 1 gives the calculated value of V_{OUT} for resistors values of: R_{SET}=24.9kΩ, R1=200 kΩ, R2=243kΩ and AVDD=10V.

Table 1. Calculated VCOM Output Voltages

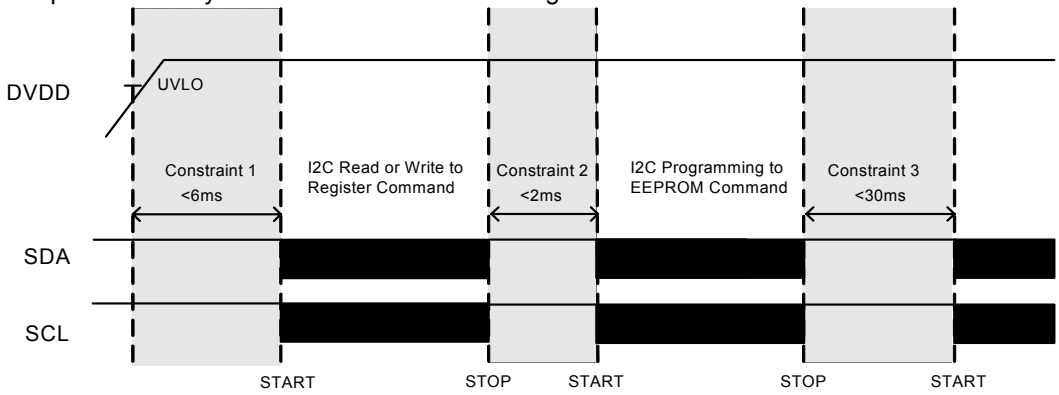
SETTING VALUE	VOUT
0	5.485
10	5.313
20	5.141
30	4.969
40	4.797
50	4.625
60	4.453
70	4.281
80	4.109
90	3.936
100	3.764
110	3.592
120	3.420
127	3.300

nWR Setting

The nWR pin control the non-volatile memory can write by I^2C interface. The nWR change to Low level define can write data into non-volatile memory by I^2C interface. If nWR is High level and I^2C command is write mode. The data will prohibit to write data into non-volatile memory.

I^2C Communication Timing

G1632 guarantees the maximum delay of I^2C blanking time. It can be referred when ACK pooling method is not adopted. The period of delay time is shown as the below figure.



Constraint 1: EEPROM start up blanking time.
It is the time from DVDD power up cross UVLO level to the end of loading EEPROM data to DAC.
Any attempt from the I^2C master talking to G1632 is not acknowledged.

Constraint 2: Read EEPROM blanking time.
It is the time from a valid stop condition of a read or writing to register sequence to the end of the internal operating cycle.
Any attempt from the I^2C master talking to G1632 is not acknowledged.

Constraint 3: Program EEPROM blanking time.
It is the time from a valid stop condition of a programming command to internal EEPROM of G1632 programming finish.
Any attempt from the I^2C master talking to G1632 is not acknowledged.

I^2C Communication Timing

I²C Operation

The Data transfers follow the below timing diagram. After start condition, the first byte contains the device address and write/read bit. This address is a 7-bit device address (hex 74h, 75h using A0 to select) is allowed for this G1632.

1.Write Mode

If the read/write bit =low @ I²C protocol , the device enter the write mode, and the Host can write data into register part, including CONTROL BYTE, VCOM register, DAC_Reg. if the RESET, WR to NVM bit of Control Byte is “1”, G1632 returns "ACK" at "slave address" and "index address",and returns "NACK" at "data byte".

■ Burst Mode

For the burst mode in the write transfer, a master device sends data to program all the output buffers. The input data bytes (DATA 1 (MSB) and (DATA 1 (LSB)) to the first channel (OUT1) is the third byte following the control byte. The second channel (OUT2) is programmed by the fifth and sixth byte (DATA 2 (MSB) and (DATA 2 (LSB)), and so on. Each byte is followed by an acknowledge bit.

■ Single Mode

The device also support single mode transfer, a master device send data to program define output buffer. Each of the input data bytes (DATA N (MSB) and (DATA N (LSB)) to the N channel (OUT N) is followed by an acknowledge bit.

Write Protocol Define:

OUT_EN=0x02
WR2NVM=0x08
RESET=0x10

1. Load NVM to DAC_Reg (Reset)

0x10 (RESET)

S	Slave Address	W	A	Index Address 0	A	Control Byte	A	P

2. Write DAC_Reg to NVM

If (Control Byte & RESET)
Return (ErrMsg):
else

Control Byte | 0x08

S	Slave Address	W	A	Index Address 0	A	Control Byte	A	P	(the output may not be interrupted)

3. set OUT_EN bit "1"

0x2 (OUT_EN)

S	Slave Address	W	A	Index Address 0	A	Control Byte	A	P

4. Single Write to DVCOM

S	Slave Address	W	A	Index Address 1	A	DVCOM	A	P

5. Single Write to DAC_Reg (Single Mode)

If ((Control Byte & WR2NVM) || (Control Byte & RESET))
return (ErrMsg);
else

0x00

S	Slave Address	W	A	Index Address 0	A	Control Byte	A	P

S	Slave Address	W	A	Index Address X	A	GX (MSB)	A	GX (LSB)	A	P	(X>=2)

0x02(OUT_EN)

S	Slave Address	W	A	Index Address 0	A	Control Byte	A	P

6. Burst Write to DAC_Reg (Burst Mode)

If ((Control Byte & WR2NVM) || (Control Byte & RESET))
return (ErrMsg);
else

0x00

S	Slave Address	W	A	Index Address 0	A	Control Byte	A	P

S	Slave Address	W	A	Index Address X	A	G1 (MSB)	A	G1 (LSB)	A	GN (MSB)	A	GN (LSB)	A	P	(X>=2)

0x02(OUT_EN)

S	Slave Address	W	A	Index Address 0	A	Control Byte	A	P

2. Read Mode

If the read/write bit = high, the device enter the read mode, and the Host can read data from registers. When "read" from G1632 at "POWER-ON RESET" or "WR to NVM", G1632 returns "ACK" at "slave address" and "index address" and puts current data to "data byte". The acknowledge bit of "data byte" is determined by the Host.

Read/Write mode

- Can't read/write DAC_Reg from Host until RESET, WR to NVM bit=0
- clear OUT_EN bit before write
- enable OUT_EN bit after finish writing action

OUT_EN=0x02
WR2NVM=0x08
RESET=0x10

1. Single Read Control Byte or DVCOM Register

S	Slave Address	W	A	Index Address 0/1	A	S	Slave Address	R	A	DATA	NA	P

2. Single Read DAC_Reg

If (Control Byte & RESET)
Return (ErrMsg):
else

S	Slave Address	W	A	Index Address i	A	S	Slave Address	R	A	Index i DATA	NA	P

3. Burst Read DAC_Reg

If (Control Byte & RESET)
Return (ErrMsg):
else

S	Slave Address	W	A	Index Address N	A	S	Slave Address	R	A	Index i DATA	A	Index i+1 DATA	A	Index i+n-1 DATA	A	Index i+n DATA	NA	P

4. Force Stop DAC Output

If ((Control Byte & WR2NVM) || (Control Byte & RESET))
return (ErrMsg);
else

0x00

S	Slave Address	W	A	Index Address 0	A	Control Byte	A

3. Control Byte define

Control Byte:

B7	B6	B5	B4	B3	B2	B1	B0
Reserved	HOT_EN	Reserved	RESET	WR to NVM	Reserved	OUT_EN	Reserved

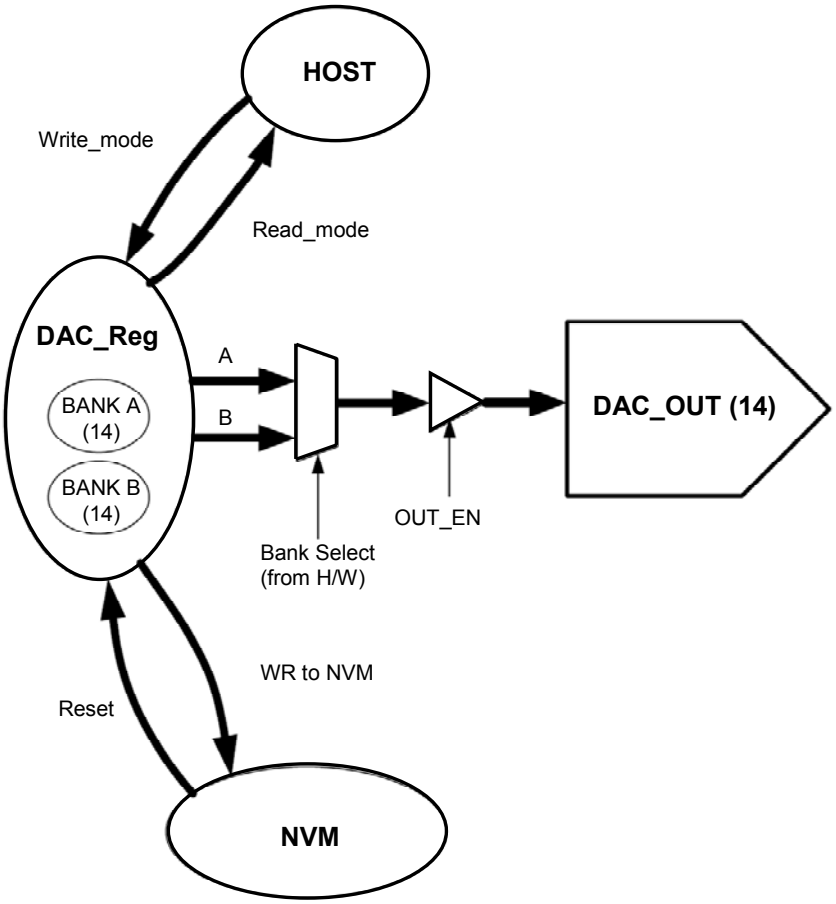
B0: Reserved, always set to 0
B1: OUT_EN:
1: DAC_OUT output enable (from DAC_Reg, Bank_A or Bank_B by Bank_Select(H/W))
0:Disable DAC_OUT output (change DAC_OUT I/O status to HI-Z)
B2: Reserved, always set to 0
B3: WR to NVM:
1: Write DAC_Reg (both Bank_A & Bank_B) and VCOM_Reg data into NVM
B4: RESET:
1: Download data from NVM to DAC_Reg
B5: Reserved, always set to 0
B6: HOT_EN:
1: Thermal Sensor disable
0: Thermal Sensor enable
B7: Reserved, always set to 0

■ Reset Bit
The device also support Reset mode. When the control bit (Reset bit) is set to “1”, the device will set the OUT_EN bit to “0” and then the DAC output is at Hi-Z status. At the same time, NVM data will be loaded to DAC_Reg and VCOM register. OUT_EN will stay “0” in the loading process. When data loading finished, G1632 internal H/W will make OUT_EN to “1” so that the analog DAC output is valid from Hi-Z state. Then the DAC will output the correct value from NVM. This bit will remain “1” until the download and dump process finish, and then be set to “0”.

■ WR to NVM Bit
If the control bit enable, the device will store the DAC Value to NVM. This bit will remain “1” until the writing to NVM process finish, and then be set to “0”. This bit can’t be enabled to “1” until RESET bit = “0”.

■ OUT_EN Bit
If the control bit is set to “1”, the analog DAC output will be valid from Hi-Z state, and the output data is from DAC_Reg, the output bank is selected by H/W pin BANK_SEL. This bit is always high during DAC output period. The Bit only controls Gamma Part, and it can’t be enabled until RESET, WR to NVM bit = “0”.

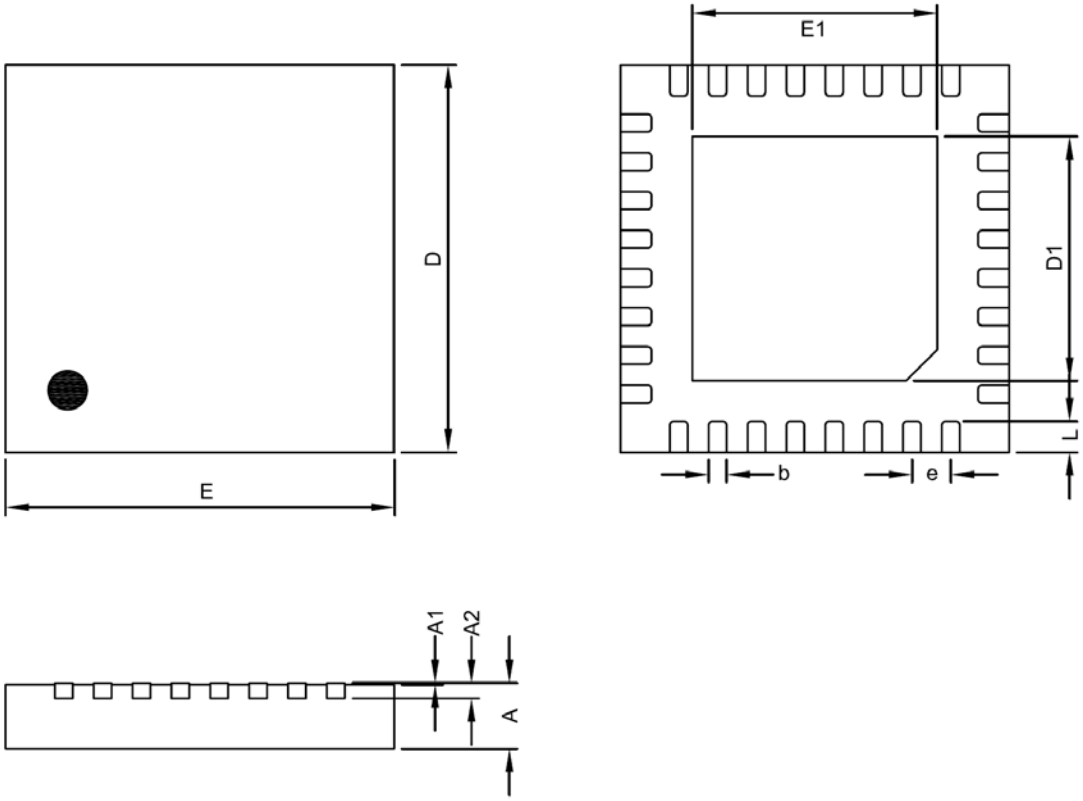
4. Action Flow State Machine Chart



5. Register Index Mapping Table

Device Address	0x74h,0x75h									
Index Addr (1 byte)	Data								Default	Note
Hex	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0		
00		HOT_EN		RESET	WR to NUM		OUT_EN			CTRL Byte
01	DVR[6]	DVR[5]	DVR[4]	DVR[3]	DVR[2]	DVR[1]	DVR[0]			Digital VCOM
02	-	-	DATA1[9:4]						Bank A	Gamma 1/Gamma 2
03	DATA1[3:0]				-	-	DATA2[9:8]			
04	DATA2[7:0]									
05	-	-	DATA3[9:4]						Bank A	Gamma 3/Gamma 4
06	DATA3[3:0]				-	-	DATA4[9:8]			
07	DATA4[7:0]									
08	-	-	DATA5[9:4]						Bank A	Gamma 5/Gamma 6
09	DATA5[3:0]				-	-	DATA6[9:8]			
0A	DATA6[7:0]									
0B	-	-	DATA7[9:4]						Bank A	Gamma 7/Gamma 8
0C	DATA7[3:0]				-	-	DATA8[9:8]			
0D	DATA8[7:0]									
0E	-	-	DATA9[9:4]						Bank A	Gamma 9/Gamma 10
0F	DATA9[3:0]				-	-	DATA10[9:8]			
10	DATA10[7:0]									
11	-	-	DATA11[9:4]						Bank A	Gamma 11/Gamma 12
12	DATA11[3:0]				-	-	DATA12[9:8]			
13	DATA12[7:0]									
14	-	-	DATA13[9:4]						Bank A	Gamma 13/Gamma 14
15	DATA13[3:0]				-	-	DATA14[9:8]			
16	DATA14[7:0]									
17	-	-	DATA15[9:4]						Bank A	Reserved
18	DATA15[3:0]				-	-	DATA16[9:8]			
19	DATA16[7:0]									
1A	-	-	DATA17[9:4]						Bank A	Reserved
1B	DATA17[3:0]				-	-	DATA18[9:8]			
1C	DATA18[7:0]									
1D	-	-	DATA19[9:4]						Bank A	Reserved
1E	DATA19[3:0]				-	-	DATA20[9:8]			
1F	DATA20[7:0]									
20	-	-	DATA21[9:4]						Bank A	Reserved
21	DATA21[3:0]				-	-	DATA22[9:8]			
22	DATA22[7:0]									
23										Reserved
24	DVR[7:0]									Reserved
25	-	-	DATA1[9:4]						Bank B	Gamma 1/Gamma 2
26	DATA1[3:0]				-	-	DATA2[9:8]			
27	DATA2[7:0]									
28	-	-	DATA3[9:4]						Bank B	Gamma 3/Gamma 4
29	DATA3[3:0]				-	-	DATA4[9:8]			
2A	DATA4[7:0]									
2B	-	-	DATA5[9:4]						Bank B	Gamma 5/Gamma 6
2C	DATA5[3:0]				-	-	DATA6[9:8]			
2D	DATA6[7:0]									
2E	-	-	DATA7[9:4]						Bank B	Gamma 7/Gamma 8
2F	DATA7[3:0]				-	-	DATA8[9:8]			
30	DATA8[7:0]									
31	-	-	DATA9[9:4]						Bank B	Gamma 9/Gamma 10
32	DATA9[3:0]				-	-	DATA10[9:8]			
33	DATA10[7:0]									
34	-	-	DATA11[9:4]						Bank B	Gamma 11/Gamma 12
35	DATA11[3:0]				-	-	DATA12[9:8]			
36	DATA12[7:0]									
37	-	-	DATA13[9:4]						Bank B	Gamma 13/Gamma 14
38	DATA13[3:0]				-	-	DATA14[9:8]			
39	DATA14[7:0]									
3A	-	-	DATA15[9:4]						Bank B	Reserved
3B	DATA15[3:0]				-	-	DATA16[9:8]			
3C	DATA16[7:0]									
3D	-	-	DATA17[9:4]						Bank B	Reserved
3E	DATA17[3:0]				-	-	DATA18[9:8]			
3F	DATA18[7:0]									
40	-	-	DATA19[9:4]						Bank B	Reserved
41	DATA19[3:0]				-	-	DATA20[9:8]			
42	DATA20[7:0]									
43	-	-	DATA21[9:4]						Bank B	Reserved
44	DATA21[3:0]				-	-	DATA22[9:8]			
45	DATA22[7:0]									

Package Information

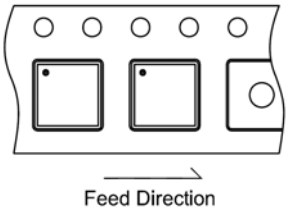


QFN5X5-32 Package

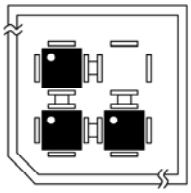
Symbol	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.90	1.00	0.0315	0.0354	0.0394
A1	0.00	- - -	0.05	0.0000	- - -	0.0020
A2	0.20 REF			0.0079 REF		
D	4.95	5.00	5.05	0.1949	0.1969	0.1988
E	4.95	5.00	5.05	0.1949	0.1969	0.1988
D1	3.05	3.20	3.30	0.1201	0.1260	0.1300
E1	3.05	3.20	3.30	0.1201	0.1260	0.1300
b	0.18	0.25	0.30	0.0071	0.0098	0.0118
e	0.50 BSC			0.0197 BSC		
L	0.30	0.40	0.45	0.0118	0.0157	0.0177

Taping Specification

G1632QA1U



G1632QA1R



G1632QA1U

PACKAGE	Q'TY/REEL
QFN5X5-32	3,000 ea

G1632QA1R

PACKAGE	Q'TY/TRAY
QFN5X5-32	490 ea