4 kb Microwire Serial CMOS EEPROM

Description

The CAT93C66 is a 4 kb CMOS Serial EEPROM device which is organized as either 256 registers of 16 bits (ORG pin at $V_{\rm CC}$) or 512 registers of 8 bits (ORG pin at GND). The CAT93W66 features x16 memory organization only. Each register can be written (or read) serially by using the DI (or DO) pin. The device features sequential read and self-timed internal write with auto-clear. On-chip Power-On Reset circuitry protects the internal logic against powering up in the wrong state.

Features

- High Speed Operation: 4 MHz (5 V), 2 MHz (1.8 V)
- 1.8 V to 5.5 V Supply Voltage Range
- Selectable x8 or x16 Memory Organization: CAT93C66
- Self-timed Write Cycle with Auto-clear
- Sequential Read
- Software Write Protection
- Power-up Inadvertent Write Protection
- Low Power CMOS Technology
- 1,000,000 Program/Erase Cycles
- 100 Year Data Retention
- Industrial and Extended Temperature Ranges
- 8-lead PDIP, SOIC, TSSOP, 6-lead SOT-23, 8-pad TDFN and UDFN Packages
- These Devices are Pb–Free, Halogen Free/BFR Free, and RoHS Compliant

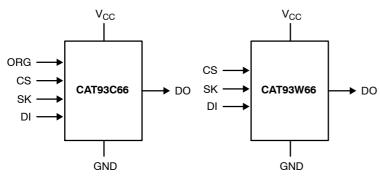


Figure 1. Functional Symbols

CAT93C66 Selectable Organization:

When the ORG pin is connected to $V_{\rm CC}$, the x16 organization is selected. When it is connected to ground, the x8 organization is selected. If the ORG pin is left unconnected, then an internal pull-up device will select the x16 organization.

CAT93W66:

The device works in x16 mode only.



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SOIC-8 V, W* SUFFIX CASE 751BD UDFN-8 HU4 SUFFIX CASE 517AZ TDFN-8* VP2 SUFFIX CASE 511AK



PDIP-8 L SUFFIX CASE 646AA



TSSOP-8 Y SUFFIX CASE 948AL

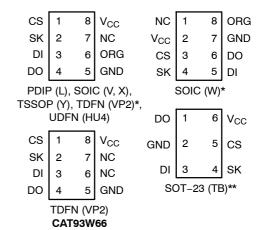


SOIC-8 X SUFFIX CASE 751BE



SOT23-6 TB SUFFIX CASE 527AJ

PIN CONFIGURATION



- * Not recommended for new designs
- ** CAT93C66 available in SOT-23 6-pin for x8 Organization. Contact factory for availability.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 16 of this data sheet.

Table 1. PIN FUNCTION

Pin Name	Function	Pin Name	Function
CS	Chip Select	V _{CC}	Power Supply
SK	Clock Input	GND	Ground
DI	Serial Data Input	ORG (Note 1)	Memory Organization
DO	Serial Data Output	NC	No Connection

^{1.} ORG Pin available for the CAT93C66 only.

Table 2. ABSOLUTE MAXIMUM RATINGS

Parameters	Ratings	Units
Storage Temperature	-65 to +150	°C
Voltage on Any Pin with Respect to Ground (Note 2)	-0.5 to +6.5	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 3. RELIABILITY CHARACTERISTICS (Note 3)

S	Symbol	Parameter	Min	Units
N _{ENI}	ID (Note 4)	Endurance	1,000,000	Program / Erase Cycles
	T_{DR}	Data Retention	100	Years

^{3.} These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC-Q100 and JEDEC test methods.

Table 4. D.C. OPERATING CHARACTERISTICS - MATURE PRODUCT

(V_{CC} = +1.8 V to +5.5 V, T_A = -40°C to +125°C unless otherwise specified.)

Symbol	Parameter	Test Condi	tions	Min	Max	Units
I _{CC1}	Power Supply Current (Write)	f _{SK} = 1 MHz, V _{CC} = 5.0 V		1	mA	
I _{CC2}	Power Supply Current (Read)	f _{SK} = 1 MHz, V _{CC} = 5.0 V			500	μΑ
I _{SB1}	Power Supply Current	V _{IN} = GND or V _{CC} ,	$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$		2	μΑ
	(Standby) (x8 Mode)	CS = GND ORG = GND	$T_A = -40^{\circ}\text{C to } +125^{\circ}\text{C}$		4	
I _{SB2}	Power Supply Current	V _{IN} = GND or V _{CC} , CS = GND	$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$		1	μΑ
	(Standby) (x16 Mode)	ORG = Float or V _{CC}	$T_A = -40^{\circ}\text{C to } +125^{\circ}\text{C}$		2	
ILI	Input Leakage Current	V _{IN} = GND to V _{CC}	$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$		1	μΑ
			$T_A = -40^{\circ}\text{C to } +125^{\circ}\text{C}$		2	
I _{LO}	I _{LO} Output Leakage Current	$V_{OUT} = GND \text{ to } V_{CC},$	$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$		1	μΑ
		CS = GND	$T_A = -40^{\circ}\text{C to } +125^{\circ}\text{C}$		2	
V _{IL1}	Input Low Voltage	4.5 V ≤ V _{CC} < 5.5 V		-0.1	0.8	V
V _{IH1}	Input High Voltage	4.5 V ≤ V _{CC} < 5.5 V		2	V _{CC} + 1	V
V _{IL2}	Input Low Voltage	1.8 V ≤ V _{CC} < 4.5 V		0	V _{CC} x 0.2	V
V _{IH2}	Input High Voltage	1.8 V ≤ V _{CC} < 4.5 V		V _{CC} x 0.7	V _{CC} + 1	V
V _{OL1}	Output Low Voltage	4.5 V ≤ V _{CC} < 5.5 V, I _{OL} = 2.1 mA			0.4	V
V _{OH1}	Output High Voltage	$4.5 \text{ V} \le \text{V}_{CC} < 5.5 \text{ V}, \text{ I}_{OH} = -400 \mu\text{A}$		2.4		V
V _{OL2}	Output Low Voltage	1.8 V ≤ V _{CC} < 4.5 V, I _{OL} = 1 mA			0.2	V
V _{OH2}	Output High Voltage	$1.8 \text{ V} \le \text{V}_{CC} < 4.5 \text{ V}, \text{I}_{OH} = -100$	μΑ	V _{CC} - 0.2		V

^{2.} The DC input voltage on any pin should not be lower than -0.5 V or higher than $V_{CC} + 0.5$ V. During transitions, the voltage on any pin may undershoot to no less than -1.5 V or overshoot to no more than $V_{CC} + 1.5$ V, for periods of less than 20 ns.

^{4.} Block Mode, $V_{CC} = 5 \text{ V}$, 25°C .

Table 5. D.C. OPERATING CHARACTERISTICS - NEW PRODUCT (REV H)

(V_{CC} = +1.8 V to +5.5 V, T_A =-40°C to +125°C unless otherwise specified.)

Symbol	Parameter	Test Cor	nditions	Min	Max	Units
I _{CC1}	Supply Current (Write)	Write, V _{CC} = 5.0 V			1	mA
I _{CC2}	Supply Current (Read)	Read, DO open, f _{SK} = 2 MH	z, V _{CC} = 5.0 V		500	μΑ
I _{SB1}	Standby Current	V _{IN} = GND or V _{CC}	$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$		2	μΑ
	(x8 Mode)	CS = GND, ORG = GND	$T_A = -40^{\circ}\text{C to } +125^{\circ}\text{C}$		5	
I _{SB2}	Standby Current	V _{IN} = GND or V _{CC}	$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$		1	μΑ
	(x16 Mode)	CS = GND, ORG = Float or V _{CC}	$T_A = -40^{\circ}\text{C to } +125^{\circ}\text{C}$		3	
I _{LI}	Input Leakage Current	V _{IN} = GND to V _{CC}	$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$		1	μΑ
			$T_A = -40^{\circ}\text{C to } +125^{\circ}\text{C}$		2	
I _{LO}	Output Leakage	V _{OUT} = GND to V _{CC}	$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$		1	μΑ
	Current	CS = GND	$T_A = -40^{\circ}\text{C to } +125^{\circ}\text{C}$		2	
V _{IL1}	Input Low Voltage	4.5 V ≤ V _{CC} < 5.5 V		-0.1	0.8	V
V _{IH1}	Input High Voltage	4.5 V ≤ V _{CC} < 5.5 V		2	V _{CC} + 1	V
V _{IL2}	Input Low Voltage	1.8 V ≤ V _{CC} < 4.5 V		0	V _{CC} x 0.2	V
V _{IH2}	Input High Voltage	1.8 V ≤ V _{CC} < 4.5 V		V _{CC} x 0.7	V _{CC} + 1	V
V _{OL1}	Output Low Voltage	4.5 V ≤ V _{CC} < 5.5 V, I _{OL} = 3 mA			0.4	V
V _{OH1}	Output High Voltage	$4.5 \text{ V} \le \text{V}_{CC} < 5.5 \text{ V}, \text{ I}_{OH} = -400 \mu\text{A}$		2.4		V
V _{OL2}	Output Low Voltage	$1.8 \text{ V} \le \text{V}_{CC} < 4.5 \text{ V}, \text{I}_{OL} = 1 \text{ mA}$			0.2	V
V _{OH2}	Output High Voltage	$1.8 \text{ V} \le \text{V}_{\text{CC}} < 4.5 \text{ V}, \text{I}_{\text{OH}} = -$	100 μΑ	V _{CC} - 0.2		V

Table 6. PIN CAPACITANCE ($T_A = 25$ °C, f = 1.0 MHz, $V_{CC} = +5.0$ V)

Symbol	Test	Conditions	Min	Тур	Max	Units
C _{OUT} (Note 5)	Output Capacitance (DO)	V _{OUT} = 0 V			5	pF
C _{IN} (Note 5)	Input Capacitance (CS, SK, DI, ORG)	V _{IN} = 0 V			5	pF

^{5.} These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC-Q100 and JEDEC test methods.

Table 7. POWER-UP TIMING (Notes 6, 7)

Symbol	Parameter	Max	Units
t _{PUR}	Power-up to Read Operation	1	ms
t _{PUW}	Power-up to Write Operation	1	ms

^{6.} These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC-Q100 and JEDEC test methods.

Table 8. A.C. TEST CONDITIONS

Input Rise and Fall Times	≤ 50 ns		
Input Pulse Voltages	0.4 V to 2.4 V	$4.5 \text{ V} \le \text{V}_{CC} \le 5.5 \text{ V}$	
Timing Reference Voltages	0.8 V, 2.0 V	$4.5 \text{ V} \le \text{V}_{CC} \le 5.5 \text{ V}$	
Input Pulse Voltages	0.2 V _{CC} to 0.7 V _{CC}	$1.8 \text{ V} \le \text{V}_{\text{CC}} \le 4.5 \text{ V}$	
Timing Reference Voltages	0.5 V _{CC}	1.8 V ≤ V _{CC} ≤ 4.5 V	
Output Load	Current Source I _{OLmax} /I _{OHmax} ; CL = 100 pF		

^{7.} t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated.

Table 9. A.C. CHARACTERISTICS - MATURE PRODUCT

(V_{CC} = +1.8 V to +5.5 V, T_A = -40°C to +125°C, unless otherwise specified.) (Note 8)

		Limits		
Symbol	Parameter	Min	Max	Units
t _{CSS}	CS Setup Time	50		ns
t _{CSH}	CS Hold Time	0		ns
t _{DIS}	DI Setup Time	100		ns
t _{DIH}	DI Hold Time	100		ns
t _{PD1}	Output Delay to 1		0.25	μs
t _{PD0}	Output Delay to 0		0.25	μs
t _{HZ} (Note 9)	Output Delay to High-Z		100	ns
t _{EW}	Program/Erase Pulse Width		5	ms
t _{CSMIN}	Minimum CS Low Time	0.25		μs
tskHI	Minimum SK High Time	0.25		μs
t _{SKLOW}	Minimum SK Low Time	0.25		μs
t _{SV}	Output Delay to Status Valid		0.25	μs
SK _{MAX}	Maximum Clock Frequency	DC	2000	kHz

^{8.} Test conditions according to "A.C. Test Conditions" table.

Table 10. A.C. CHARACTERISTICS - NEW PRODUCT (Rev H)

 $(V_{CC} = +1.8 \text{ V to } +5.5 \text{ V}, \text{ TA} = -40^{\circ}\text{C to } +125^{\circ}\text{C}, \text{ unless otherwise specified.})$

		V _{CC} = 1.8 V - 5.5 V		V _{CC} = 4.5 V - 5.5 V		
Symbol	Parameter	Min	Max	Min	Max	Units
t _{CSS}	CS Setup Time	50		50		ns
t _{CSH}	CS Hold Time	0		0		ns
t _{DIS}	DI Setup Time	100		50		ns
t _{DIH}	DI Hold Time	100		50		ns
t _{PD1}	Output Delay to 1		0.25		0.1	μs
t _{PD0}	Output Delay to 0		0.25		0.1	μs
t _{HZ} (Note 10)	Output Delay to High-Z		100		100	ns
t _{EW}	Program/Erase Pulse Width		5		5	ms
t _{CSMIN}	Minimum CS Low Time	0.25		0.1		μs
tskhi	Minimum SK High Time	0.25		0.1		μs
t _{SKLOW}	Minimum SK Low Time	0.25		0.1		μs
t _{SV}	Output Delay to Status Valid		0.25		0.1	μs
SK _{MAX}	Maximum Clock Frequency	DC	2000	DC	4000	kHz

^{10.} This parameter is tested initially and after a design or process change that affects the parameter.

These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC-Q100 and JEDEC test methods.

Device Operation

The CAT93C66 is a 4096-bit nonvolatile memory intended for use with industry standard microprocessors. The CAT93C66 can be organized as either registers of 16 bits or 8 bits. When organized as X16, seven 11-bit instructions control the reading, writing and erase operations of the device. When organized as X8, seven 12-bit instructions control the reading, writing and erase operations of the device. The CAT93W66 works in x16 mode only. The device operates on a single power supply and will generate on chip, the high voltage required during any write operation.

Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (SK). The DO pin is normally in a high impedance state except when reading data from the device, or when checking the ready/busy status after a write operation. The serial communication protocol follows the timing shown in Figure 2.

The ready/busy status can be determined after the start of internal write cycle by selecting the device (CS high) and polling the DO pin; DO low indicates that the write operation is not completed, while DO high indicates that the device is ready for the next instruction. If necessary, the DO pin may be placed back into a high impedance state during chip select by shifting a dummy "1" into the DI pin. The DO pin will enter the high impedance state on the rising edge of the clock (SK). Placing the DO pin into the high impedance state is recommended in applications where the DI pin and the DO pin are to be tied together to form a common DI/O pin.

The format for all instructions sent to the device is a logical "1" start bit, a 2-bit (or 4-bit) opcode, 8-bit address (an additional bit when organized X8) and for write operations a 16-bit data field (8-bit for X8 organizations). The instruction format is shown in Instruction Set table.

Table 11. INSTRUCTION SET

			Address		Data		
Instruction	Start Bit	Opcode	x8 (Note 11)	x16	x8 (Note 11)	x16	Comments
READ	1	10	A8-A0	A7-A0			Read Address AN – A0
ERASE	1	11	A8-A0	A7-A0			Clear Address AN – A0
WRITE	1	01	A8-A0	A7-A0	D7-D0	D15-D0	Write Address AN – A0
EWEN	1	00	11XXXXXXX	11XXXXXX			Write Enable
EWDS	1	00	00XXXXXXX	00XXXXXX			Write Disable
ERAL	1	00	10XXXXXXX	10XXXXXX			Clear All Addresses
WRAL	1	00	01XXXXXXX	01XXXXXX	D7-D0	D15-D0	Write All Addresses

^{11.} The x8 memory organization is available for the CAT93C66 only.

Read

Upon receiving a READ command and an address (clocked into the DI pin), the DO pin of the CAT93C66, CAT93W66 will come out of the high impedance state and, after sending an initial dummy zero bit, will begin shifting out the data addressed (MSB first). The output data bits will toggle on the rising edge of the SK clock and are stable after the specified time delay (tpD0 or tpD1).

For the CAT93C66, CAT93W66 after the initial data word has been shifted out and CS remains asserted with the SK clock continuing to toggle, the device will automatically increment to the next address and shift out the next data word in a sequential READ mode. As long as CS is continuously asserted and SK continues to toggle, the device will keep incrementing to the next address automatically until it reaches to the end of the address space, then loops back to address 0. In the sequential READ mode, only the initial data word is preceeded by a dummy zero bit. All subsequent data

words will follow without a dummy zero bit. The READ instruction timing is illustrated in Figure 3.

Erase/Write Enable and Disable

The device powers up in the write disable state. Any writing after power-up or after an EWDS (erase/write disable) instruction must first be preceded by the EWEN (erase/write enable) instruction. Once the write instruction is enabled, it will remain enabled until power to the device is removed, or the EWDS instruction is sent. The EWDS instruction can be used to disable all CAT93C66, CAT93W66 write and erase instructions, and will prevent any accidental writing or clearing of the device. Data can be read normally from the device regardless of the write enable/disable status. The EWEN and EWDS instructions timing is shown in Figure 4.

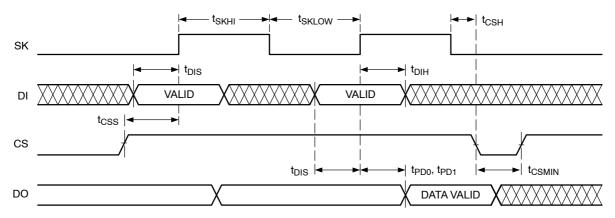


Figure 2. Synchronous Data Timing

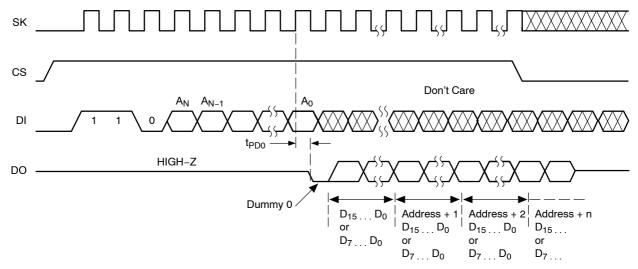


Figure 3. READ Instruction Timing

Write

After receiving a WRITE command (Figure 5), address and the data, the CS (Chip Select) pin must be deselected for a minimum of t_{CSMIN}. The falling edge of CS will start the self clocking clear and data store cycle of the memory location specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C66, CAT93W66 can be determined by selecting the device and polling the DO pin. Since this device features Auto-Clear before write, it is NOT necessary to erase a memory location before it is written into.

Erase

Upon receiving an ERASE command and address, the CS (Chip Select) pin must be deasserted for a minimum of t_{CSMIN} (Figure 6). The falling edge of CS will start the self clocking clear cycle of the selected memory location. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C66, CAT93W66 can be determined by selecting the device and polling the DO pin. Once cleared, the content of a cleared location returns to a logical "1" state.

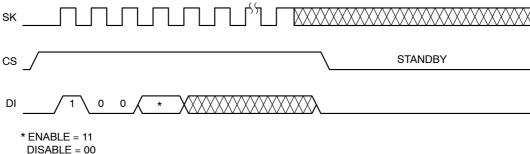


Figure 4. EWEN/EWDS Instruction Timing

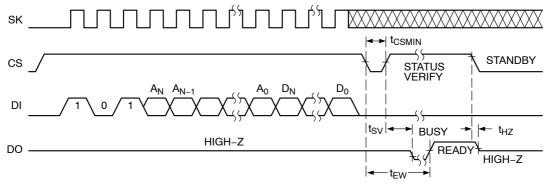


Figure 5. Write Instruction Timing

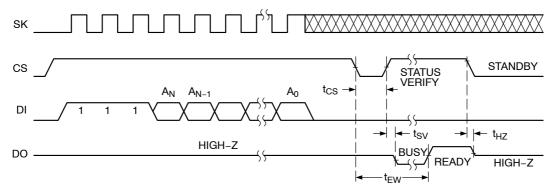


Figure 6. Erase Instruction Timing

Erase All

Upon receiving an ERAL command (Figure 7), the CS (Chip Select) pin must be deselected for a minimum of $t_{\rm CSMIN}$. The falling edge of CS will start the self clocking clear cycle of all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the device can be determined by selecting the device and polling the DO pin. Once cleared, the contents of all memory bits return to a logical "1" state.

Write All

Upon receiving a WRAL command and data, the CS (Chip Select) pin must be deselected for a minimum of t_{CSMIN} (Figure 8). The falling edge of CS will start the self clocking data write to all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the device can be determined by selecting the device and polling the DO pin. It is not necessary for all memory locations to be cleared before the WRAL command is executed.

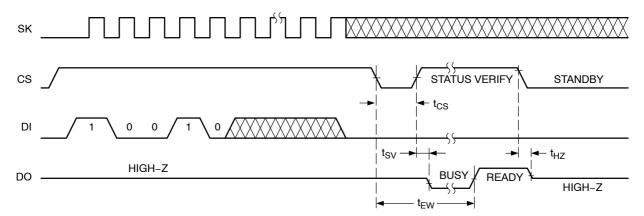


Figure 7. ERAL Instruction Timing

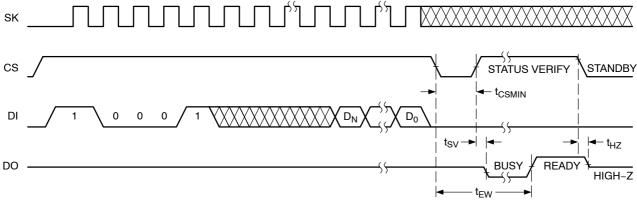
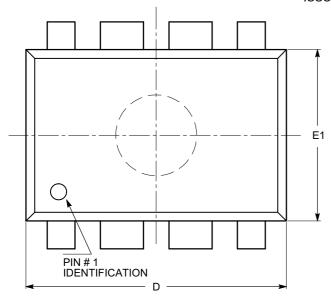


Figure 8. WRAL Instruction Timing

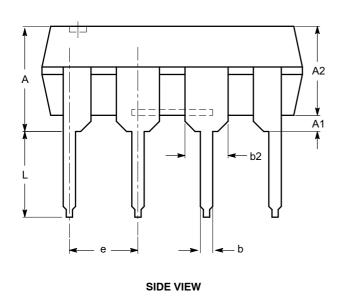
PACKAGE DIMENSIONS

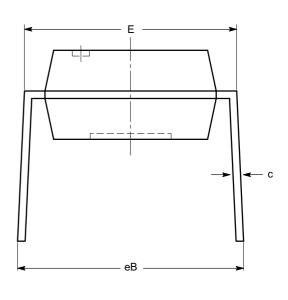
PDIP-8, 300 mils CASE 646AA-01 ISSUE A



SYMBOL	MIN	NOM	MAX		
Α			5.33		
A1	0.38				
A2	2.92	3.30	4.95		
b	0.36	0.46	0.56		
b2	1.14	1.52	1.78		
С	0.20	0.25	0.36		
D	9.02	9.27	10.16		
Е	7.62	7.87	8.25		
E1	6.10	6.35	7.11		
е	2.54 BSC				
eB	7.87		10.92		
L	2.92	3.30	3.80		

TOP VIEW



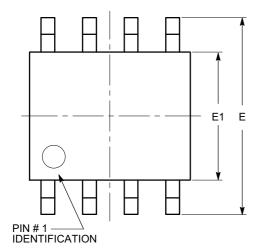


END VIEW

- (1) All dimensions are in millimeters.
- (2) Complies with JEDEC MS-001.

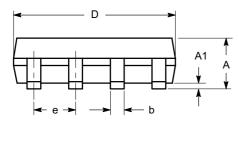
PACKAGE DIMENSIONS

SOIC 8, 150 mils CASE 751BD-01 ISSUE O

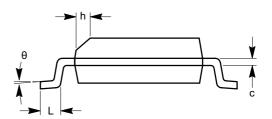


SYMBOL	MIN	NOM	MAX
Α	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
С	0.19		0.25
D	4.80		5.00
Е	5.80		6.20
E1	3.80		4.00
е		1.27 BSC	
h	0.25		0.50
L	0.40		1.27
θ	0°		8°

TOP VIEW



SIDE VIEW

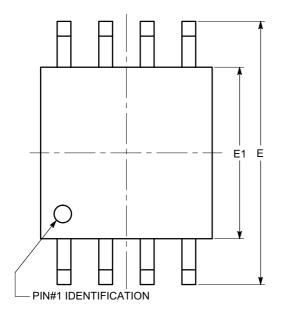


END VIEW

- (1) All dimensions are in millimeters. Angles in degrees.(2) Complies with JEDEC MS-012.

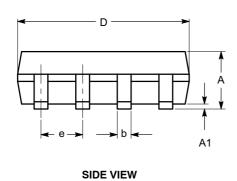
PACKAGE DIMENSIONS

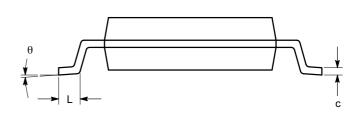
SOIC-8, 208 mils CASE 751BE-01 ISSUE O



SYMBOL	MIN	NOM	MAX
Α			2.03
A1	0.05		0.25
b	0.36		0.48
С	0.19		0.25
D	5.13		5.33
Е	7.75		8.26
E1	5.13		5.38
е		1.27 BSC	
L	0.51		0.76
θ	0°		8°

TOP VIEW



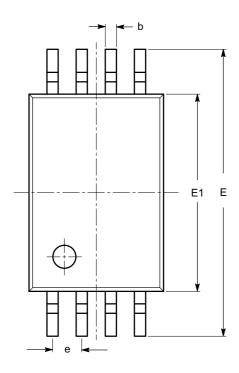


END VIEW

- (1) All dimensions are in millimeters. Angles in degrees.(2) Complies with EIAJ EDR-7320.

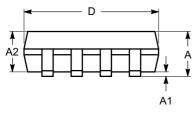
PACKAGE DIMENSIONS

TSSOP8, 4.4x3 CASE 948AL-01 ISSUE O

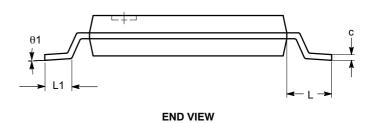


SYMBOL	MIN	NOM	MAX
Α			1.20
A1	0.05		0.15
A2	0.80	0.90	1.05
b	0.19		0.30
С	0.09		0.20
D	2.90	3.00	3.10
Е	6.30	6.40	6.50
E1	4.30	4.40	4.50
е	0.65 BSC		
L	1.00 REF		
L1	0.50	0.60	0.75
θ	0°		8°

TOP VIEW



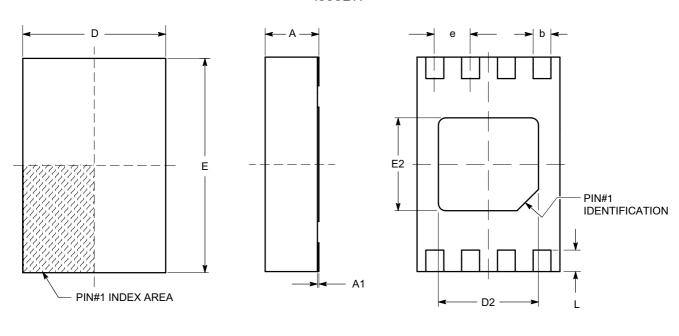
SIDE VIEW



- (1) All dimensions are in millimeters. Angles in degrees.(2) Complies with JEDEC MO-153.

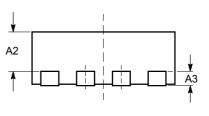
PACKAGE DIMENSIONS

TDFN8, 2x3 CASE 511AK-01 ISSUE A



SIDE VIEW

SYMBOL	MIN	NOM MAX			
Α	0.70	0.75	0.80		
A1	0.00	0.02	0.05		
A2	0.45	0.55 0.65			
АЗ	0.20 REF				
b	0.20	0.25	0.30		
D	1.90	2.00 2.10			
D2	1.30	1.40 1.50			
Е	2.90	2.90 3.00 3.10			
E2	1.20	1.30 1.40			
е	0.50 TYP				
L	0.20	0.30	0.40		



BOTTOM VIEW

FRONT VIEW

Notes:

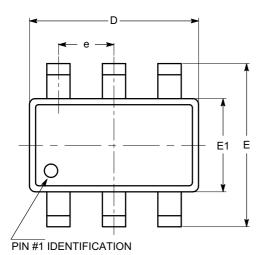
(1) All dimensions are in millimeters.

TOP VIEW

(2) Complies with JEDEC MO-229.

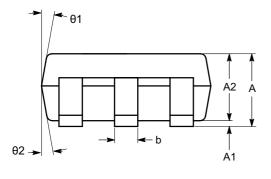
PACKAGE DIMENSIONS

SOT-23, 6 Lead CASE 527AJ-01 ISSUE O



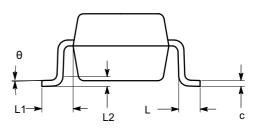
TOP VIEW

SYMBOL	MIN	NOM	MAX	
А	0.90		1.45	
A1	0.00		0.15	
A2	0.90	1.15	1.30	
b	0.30		0.50	
С	0.08	0.08		
D	2.90 BSC			
Е	2.80 BSC			
E1	1.60 BSC			
е	0.95 BSC			
L	0.30 0.45		0.60	
L1	0.60 REF			
L2	0.25 REF			
θ	0° 4° 8°			
θ1	5° 10°		15°	
θ2	5° 10°		15°	



SIDE VIEW

- (1) All dimensions in millimeters. Angles in degrees.(2) Complies with JEDEC standard MO-178.

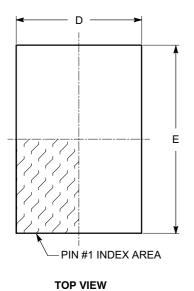


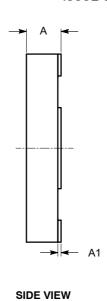
END VIEW

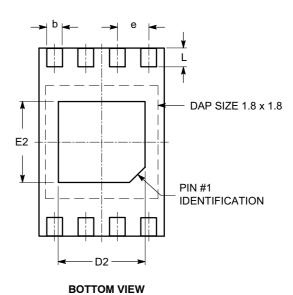
PACKAGE DIMENSIONS

UDFN8, 2x3 EXTENDED PAD

CASE 517AZ-01 ISSUE O

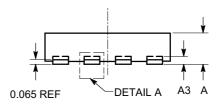




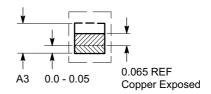


SYMBOL	MIN	NOM	MAX
Α	0.45	0.50	0.55
A1	0.00	0.02	0.05
А3	0.127 REF		
b	0.20	0.25	0.30
D	1.95	2.00	2.05
D2	1.35	1.40	1.45
Е	2.95	3.00	3.05
E2	1.25	1.30	1.35
е	0.50 REF		
L	0.25	0.30	0.35

- (1) All dimensions are in millimeters.
- (2) Refer JEDEC MO-236/MO-252.



FRONT VIEW



DETAIL A

Table 12. ORDERING INFORMATION

Device Order Number	Specific Device Marking*	Package Type	Temperature Range	Lead Finish	Shipping
CAT93C66LI-G	93C66H	PDIP-8	I = Industrial (-40°C to +85°C)	NiPdAu	Tube, 50 Units / Tube
CAT93C66VE-G	93C66H	SOIC-8, JEDEC	E = Extended (-40°C to +125°C)	NiPdAu	Tube, 100 Units / Tube
CAT93C66VE-GT3	93C66H	SOIC-8, JEDEC	E = Extended (-40°C to +125°C)	NiPdAu	Tape & Reel, 3,000 Units / Reel
CAT93C66VI-G	93C66H	SOIC-8, JEDEC	I = Industrial (-40°C to +85°C)	NiPdAu	Tube, 100 Units / Tube
CAT93C66VI-GT3	93C66H	SOIC-8, JEDEC	I = Industrial (-40°C to +85°C)	NiPdAu	Tape & Reel, 3,000 Units / Reel
CAT93C66VP2E-GT3	M2T	TDFN-8	E = Extended (-40°C to +125°C)	NiPdAu	Tape & Reel, 3,000 Units / Reel
CAT93C66VP2I-GT3	M2T	TDFN-8	I = Industrial (-40°C to +85°C)	NiPdAu	Tape & Reel, 3,000 Units / Reel
CAT93C66YI-G	M66	TSSOP-8	I = Industrial (-40°C to +85°C)	NiPdAu	Tube, 100 Units / Tube
CAT93C66YI-GT3	M66	TSSOP-8	I = Industrial (-40°C to +85°C)	NiPdAu	Tape & Reel, 3,000 Units / Reel
CAT93C66YE-GT3	M66	TSSOP-8	E = Extended (-40°C to +125°C)	NiPdAu	Tape & Reel, 3,000 Units / Reel
CAT93W66VP2I-GT3	M2C	TDFN-8	I = Industrial (-40°C to +85°C)	NiPdAu	Tape & Reel, 3,000 Units / Reel
CAT93C66XI-T2	93C66H	SOIC-8, EIAJ	E = Extended (-40°C to +125°C)	Matte-Tin	Tape & Reel, 2,000 Units / Reel
CAT93C66HU4I-GT3	M2U	UDFN-8	I = Industrial (-40°C to +85°C)	NiPdAu	Tape & Reel, 3,000 Units / Reel
CAT93C66HU4E-GT3	M2U	UDFN-8	E = Extended (-40°C to +125°C)	NiPdAu	Tape & Reel, 3,000 Units / Reel

^{*} Marking for New Product (Rev H)

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^{12.} All packages are RoHS-compliant (Lead-free, Halogen-free).

^{13.} The standard lead finish is NiPdAu.

^{14.} For additional package and temperature options, please contact your nearest ON Semiconductor Sales office.

^{15.} For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

^{16.} For detailed information and a breakdown of device nomenclature and numbering systems, please see the ON Semiconductor Device Nomenclature document, TND310/D, available at www.onsemi.com