Autotuning Methods

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Contents

The Need for Autotuning in High Performance Computing

High Performance Computing has been a cornerstone of scientific and industrial progress for at least five decades. By paying the cost of increased complexity, software and hardware engineering advances continue to overcome several challenges on the way of the sustained performance improvements observed during the last fifty years. A consequence of this mounting complexity is that reaching the theoretical peak hardware performance for a given program requires not only expert knowledge of specific hardware architectures, but also mastery of programming models and languages for parallel and distributed computing.

If we state performance optimization problems as *search* or *learning* problems, by converting implementation and configuration choices to *parameters* which might affect performance, we can draw and adapt proven methods from search, mathematical optimization, and *statistical learning*. The effectiveness of these adapted methods on performance optimization problems varies greatly, and hinges on practical and mathematical properties of the problem and the corresponding *search space*. The application of such methods to the automation of program optimization for specific hardware, under a set of *constraints*, is named *autotuning*.

Improving performance also relies on gathering application-specific knowledge, which entails extensive experimental costs since, with the exception of linear algebra routines, theoretical peak performance is not always a reachable comparison baseline. When adapting methods for autotuning we must face challenges emerging from practical properties, such as restricted time and cost budgets, constraints on feasible parameter values, and the need to mix *categorical*, *continuous*, and *discrete* parameters. To achieve

useful results we must also choose methods that make hypotheses compatible with problem search spaces, such as the existence of *discoverable*, or at least *exploitable*, relationships between parameters and performance. Choosing an autotuning method requires determining a balance between the exploration of a problem, when we would seek to discover and explain relationships between parameters and performance, and the exploitation of the best optimizations we can find, when we would seek only to minimize performance.

The contributions of this thesis are strategies to apply to program autotuning the statistical learning methods of *Design of Experiments* [1], or *Experimental Design*, and *Gaussian Process Regression* [2]. This thesis presents background and a high-level view of the theoretical foundations of each method, and detailed discussions of the challenges involved in specializing the general definitions of search heuristics and statistical learning methods to different autotuning problems, as well as what can be *learned* about specific autotuning search spaces, and how that acquired knowledge can be leveraged for further optimization.

This chapter aims to substantiate the claim that autotuning methods have a fundamental role to play on the future of program performance optimization, arguing that the value and the difficulty of the efforts to carefully tune software became more apparent ever since advances in hardware stopped leading to effortless performance improvements, at least from the programmer's perspective. The following sections discuss the historical context for the changes in trends on computer architecture, and characterize the search spaces found when optimizing performance on different domains.

1.1 Historical Trends in Hardware Design

The physical constraints imposed by technological advances on circuit design were evident since the first vacuum tube computers that already spanned entire floors, such as the ENIAC in 1945 [3]. The practical and economical need to fit more computing power into real estate is one force for innovation in hardware design that spans its history, and is echoed in modern supercomputers, such as the *Summit* from *Oak Ridge National Laboratory* [4], which spans an entire room.

Figure 1.1 highlights the unrelenting and so far successful pursuit of smaller transistor fabrication processes, and the resulting capability to fit more computing power on a fixed chip area. This trend was already observed in integrated circuits by Gor-

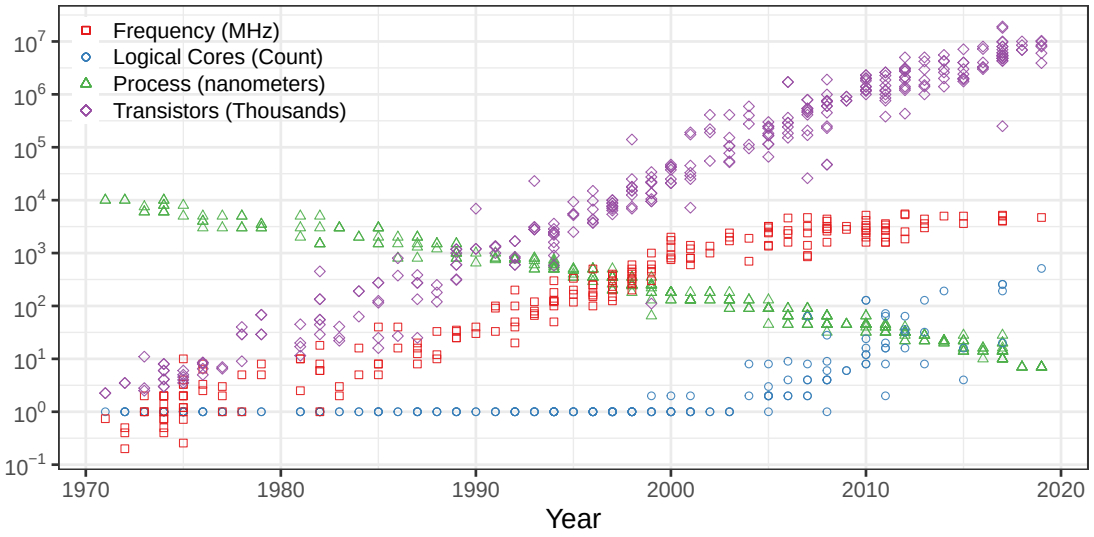

Figure 1.1: 49 years of microprocessor data, highlighting the sustained exponential increases and reductions on transistor counts and fabrication processes, the stagnation of frequency scaling around 2005, and one solution found for it, the simultaneous exponential increase on logical core count. Data from Wikipedia [6, 7]

don Moore *et al.* in 1965 [5], who also postulated its continuity. The performance improvements produced by the design efforts to make Moore's forecast a self-fulfilling prophecy were boosted until around 2005 by the performance gained from increases in circuit frequency.

Robert Dennard *et al.* remarked in 1974 [8] that smaller transistors, in part because they generate shorter circuit delays, decrease the energy required to power a circuit and enable an increase in operation frequency without breaking power usage constraints. This scaling effect, named *Dennard's scaling*, is hindered primarily by leakage current, caused by quantum tunneling effects in small transistors. Figure 1.1 shows a marked stagnation on frequency increase after around 2005, as transistors crossed the 10^2nm fabrication process. It was expected that leakage due to tunneling would limit frequency scaling strongly, even before the transistor fabrication process reached 10nm [9].

Current hardware is now past the effects of Dennard's scaling. The increase in logical cores, still around 2015, can be interpreted as preparation for and mitigation of the end of frequency scaling, and ushered in an age of multicore scaling. Still, in order to meet power consumption constraints, up to half of a multicore processor could have to be powered down at all times. This phenomenon is named *Dark Silicon* [10], and still

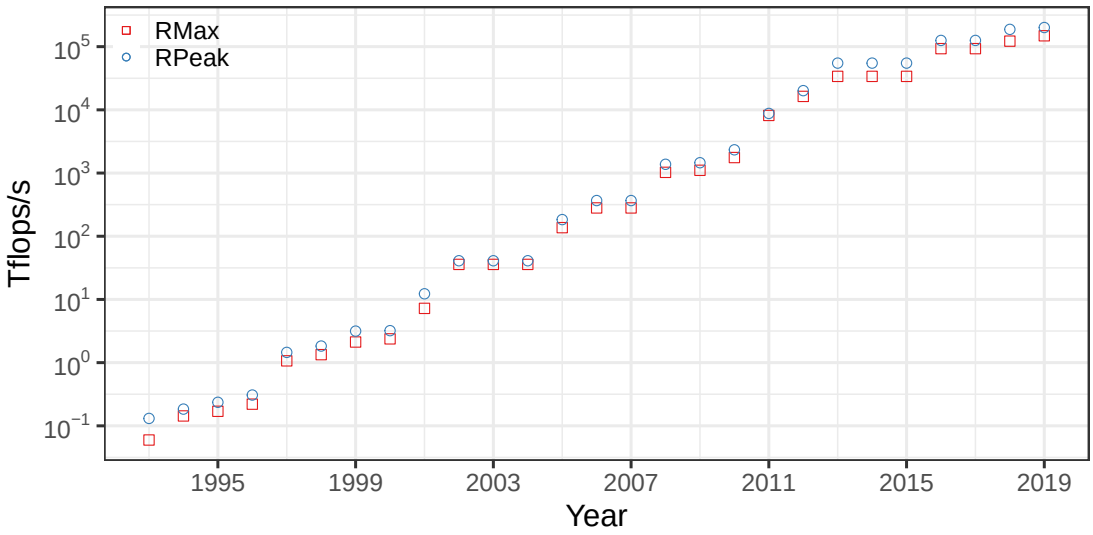

Figure 1.2: Sustained exponential increase of theoretical *RPeak* and achieved *RMax* performance for the supercomputer ranked 1st on TOP500 [14]

presents significant challenges to hardware designers and programmers [11, 12, 13].

The *Top500* [14] list gathers information about commercially available supercomputers, and ranks them by their performance on the *LINPACK* benchmark [15]. Figure 1.2 shows the peak theoretical performance $RPeak$, and the maximum performance achieved on the LINPACK benchmark $RMax$, in $Tflops/s$, for the top-ranked supercomputers on TOP500. Despite the smaller performance gains from hardware design that are to be expected for post-Dennard's scaling processors, the increase in computer performance has continued its exponential climb, sustained mostly by software improvements.

Although hardware accelerators, such as GPUs and FPGAs, have also helped to sustain exponential performance increase, their use is not an escape from the fundamental scaling constraints imposed by current semiconductor design. Figure 1.3 shows the increase in processor and accelerator core count on the top-ranked supercomputers on Top500. Half of the top-ranked supercomputers in the last decade had accelerator cores, and of those, all had around ten times more accelerator than processor cores. The apparent stagnation of core count in top-ranked supercomputers, even considering accelerators, highlights the crucial impact of software on performance.

Advances in hardware design are currently not capable of providing performance

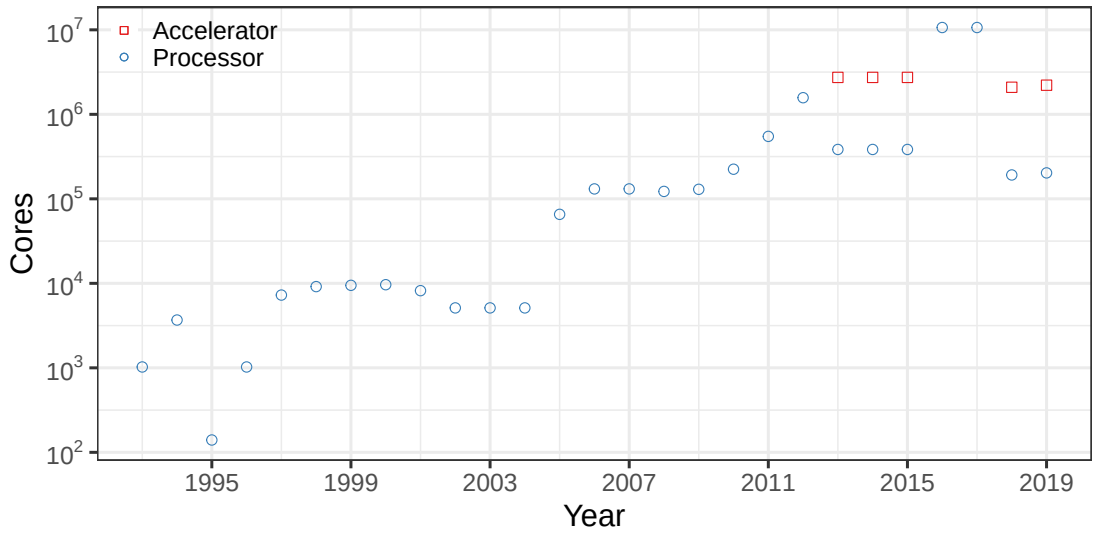

Figure 1.3: Processor and accelerator core count in supercomputers ranked 1st on TOP500 [14]. Core count trends for supercomputers are not necessarily bound to processor trends observed on Figure 1.1.

improvements via frequency scaling without dissipating more power than the processor was designed to support, which violates power constraints and risks damaging the circuit. From the programmer's perspective, effortless performance improvements from hardware have not been expected for quite some time, and the key to sustaining historical trends in performance scaling has lied in accelerators, parallel and distributed programming libraries, and fine tuning of several stages of the software stack, from instruction selection to the layout of neural networks.

The problem of optimizing software for performance presents its own challenges. The search spaces that emerge from autotuning problems grow quickly to a size for which it would take a prohibitive amount of time to determine the best configuration by exhaustively evaluating all possibilities. Although this means we must seek to decrease the amount of possibilities, by restricting allowed parameter values, or dropping parameters completely, it is often unclear how to decide which parameters should be restricted or dropped. The next section introduces a simple autotuning problem, and presents an overview of autotuning search spaces from the size perspective. The section also briefly introduces methods used to explore autotuning search spaces, which are discussed in Chapter 3.

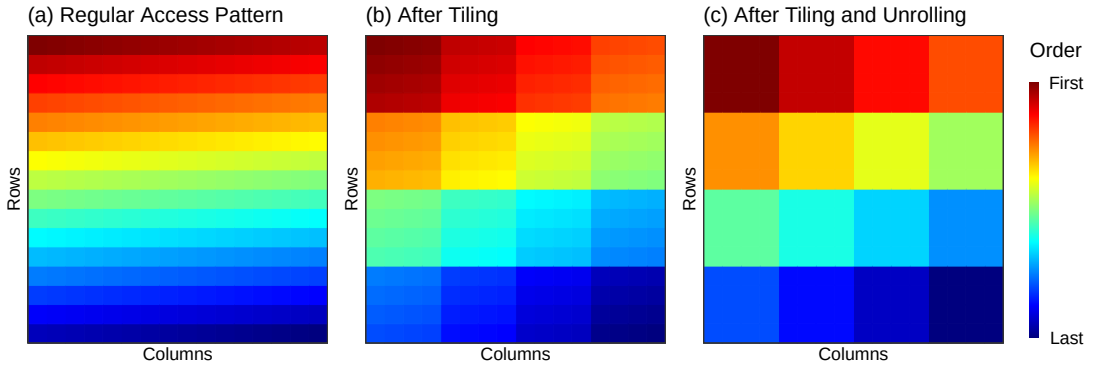

Figure 1.4: Access patterns on GEMM, for the *destination* matrix, using loop nest optimizations. Panel *(a)* shows the access order of a naive implementation, panel *(b)* shows the effect of loop *tiling*, or *blocking*, and panel *(c)* shows the compounded effect of loop *unrolling*

1.2 Characterizing Search Spaces from Autotuning Problems

A classical autotuning example is the problem of decreasing the execution time of basic components for linear algebra, such as the ones from the original BLAS [16], or for general matrix multiplication (GEMM) [17]. One way to optimize such programs is to exploit cache locality by reordering and organizing loop iterations, using source code transformation methods such as loop *tiling*, or *blocking*, and *unrolling*. We now briefly describe loop tiling and unrolling in the context of GEMM, and how these methods generate a relatively large and complex search space.

Figure 1.5 shows three GEMM implementations in C. Figure 1.5a shows a naive implementation, with three nested loops span the size of the square matrices, accessing elements of the *destination* matrix C in the order shown on the leftmost panel of Figure 1.4. If loop indices are split in blocks, as shown in Figure 1.5b, memory accesses will be performed in *tiles*, as shown on the center panel of Figure 1.4, which can improve performance by using only elements that fit on the processor's cache. Loop unrolling, shown in Figure 1.5c, is an additional source transformation that can be performed on top of tiling, and can improve performance by grouping iterations of a loop, as is represented on the rightmost panel of Figure 1.4, ensuring that processor registers are used.

```
int N = 256;

float A[N][N], B[N][N], C[N][N];
int i, j, k;

// [...] Initialize A, B, C

for(i = 0; i < N; i++){
  for(j = 0; j < N; j++){
    for(k = 0; k < N; k++){
      C[i][j] += A[i][k] * B[k][j];
    }
  }
}
```

(a) Naive implementation

```
int N = 256;
int B_size = 4;

int A[N][N], B[N][N], C[N][N];
int i, j, k, x, y;

// [...] Initialize A, B, C

for(i = 0; i < N; i += B_size){
  for(j = 0; j < N; j += B_size){
    for(k = 0; k < N; k++){
      for(x = i; x < min(i + B_size, N); x++){
        for(y = j; y < min(j + B_size, N); y++){
          C[x][y] += A[x][k] * B[k][y];
        }
      }
    }
  }
}
```

(b) Blocked, or tiled

```
int N = 256;
int B_size = 4;

int A[N][N], B[N][N], C[N][N];
int i, j, k;

// [...] Initialize A, B, C

for(i = 0; i < N; i += B_size){
  for(j = 0; j < N; j += B_size){
    for(k = 0; k < N; k++){
      C[i + 0][j + 0] += A[i + 0][k] * B[k][j + 0];
      C[i + 0][j + 1] += A[i + 0][k] * B[k][j + 1];

      // [...] Unroll the remaining 12 iterations

      C[i + Bsize - 1][j + B_size - 2] += A[i + Bsize - 1][k] * B[k][j + B_size - 2];
      C[i + Bsize - 1][j + B_size - 1] += A[i + Bsize - 1][k] * B[k][j + B_size - 1];
    }
  }
}
```

(c) Tiled and unrolled

Figure 1.5: Loop nest optimizations for GEMM, in C

1.3 Thesis Contributions

1.4 Text Structure

Chapter 3 presents background for the application of methods derived from search heuristics, mathematical optimization, and statistical learning to autotuning.

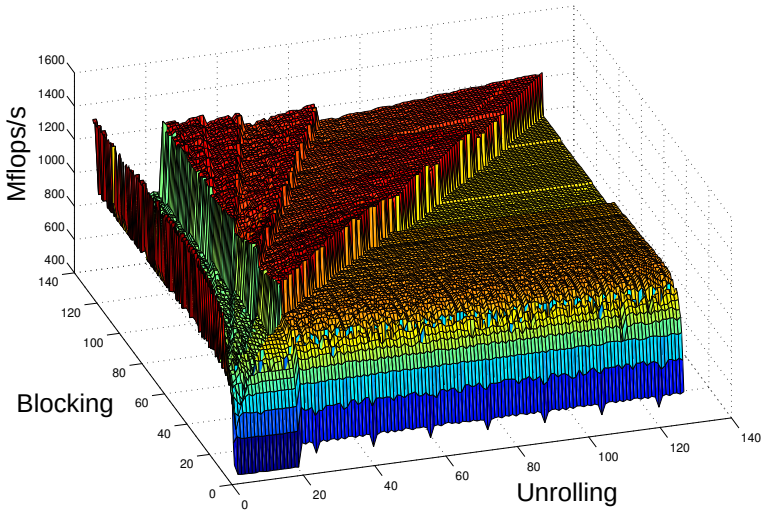

Figure 1.6: A search space defined for loop blocking and unrolling parameters, in a matrix multiplication kernel [18]

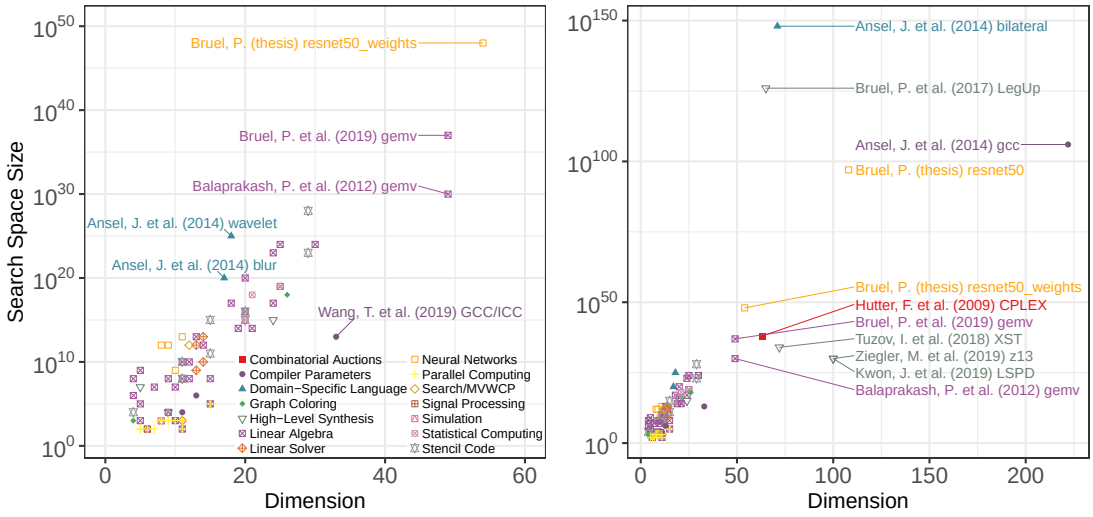

Figure 1.7: Dimension and search space size for autotuning problems from different domains [19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 18]. The left panel shows a zoomed view of the right panel

Reproducible Science

Search and Statistical Learning for Autotuning

Design of Experiments

Gaussian Process Regression

5.1 References

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