	Compilation Hierarchy Node	Combinational ALUTs	Dedicated Logic Registers	Block Memory Bits	DSP Blocks	Pins	Virtual Pins	Full Hierarchy Name	Entity Name	Library Name
1	|DE1_SoC	1221 (139)	1592 (9)	16128	0	107	0	|DE1_SoC	DE1_SoC	work
1	|audio_and_video_config:cfg|	95 (2)	56 (9)	0	0	0	0	|DE1_SoC|audio_and_video_config:cfg	audio_and_video_config	work
1	|Altera_UP_I2C:I2C_Controller|	22 (22)	14 (14)	0	0	0	0	|DE1_SoC|audio_and_video_config:cfg|Altera_UP_I2C:I2C_Controller	Altera_UP_I2C	work
2	|Altera_UP_I2C_AV_Auto_Initialize:Auto_Initialize|	57 (57)	20 (20)	0	0	0	0	|DE1_SoC|audio_and_video_config:cfg|Altera_UP_I2C_AV_Auto_Initialize:Auto_Initialize	Altera_UP_I2C_AV_Auto_Initialize	work
3	|Altera_UP_Slow_Clock_Generator:Clock_Generator_400KHz|	14 (14)	13 (13)	0	0	0	0	|DE1_SoC|audio_and_video_config:cfg|Altera_UP_Slow_Clock_Generator:Clock_Generator_400KHz	Altera_UP_Slow_Clock_Generator	work
2	|audio_codec:codec|	268 (11)	228 (2)	12288	0	0	0	|DE1_SoC|audio_codec:codec	audio_codec	work
1	|Altera_UP_Audio_In_Deserializer:Audio_In_Deserializer|	109 (5)	112 (40)	6144	0	0	0	|DE1_SoC|audio_codec:codec|Altera_UP_Audio_In_Deserializer:Audio_In_Deserializer	Altera_UP_Audio_In_Deserializer	work
1	|Altera_UP_Audio_Bit_Counter:Audio_Out_Bit_Counter|	10 (10)	6 (6)	0	0	0	0	|DE1_SoC|audio_codec:codec|Altera_UP_Audio_In_Deserializer:Audio_In_Deseri	Altera_UP_Audio_Bit_Counter	work

	Compilation Hierarchy Node	Combinational ALUTs	Dedicated Logic Registers	Block Memory Bits	DSP Blocks	Pins	Virtual Pins	Full Hierarchy Name	Entity Name	Library Name
								alizer|Altera_UP_Audio_Bit_Counter:Audio_Out_Bit_Counter		
2	|Altera_UP_SYNC_FIFO:Audio_In_Left_Channel_FIFO|	47 (0)	33 (0)	3072	0	0	0	|DE1_SoC|audio_codec:codec|Altera_UP_Audio_In_Deserializer:Audio_In_Deserializer|Altera_UP_SYNC_FIFO:Audio_In_Left_Channel_FIFO	Altera_UP_SYNC_FIFO	work
1	|scfifo:Sync_FIFO|	47 (0)	33 (0)	3072	0	0	0	|DE1_SoC|audio_codec:codec|Altera_UP_Audio_In_Deserializer:Audio_In_Deserializer|Altera_UP_SYNC_FIFO:Audio_In_Left_Channel_FIFO|scfifo:Sync_FIFO	scfifo	work
1	|scfifo_8ba1:auto_generated|	47 (0)	33 (0)	3072	0	0	0	|DE1_SoC|audio_codec:codec|Altera_UP_Audio_In_Deserializer:Audio_In_Deserializer|Altera_UP_SYNC_FIFO:Audio_In_Left_Channel_FIFO|	scfifo_8ba1	work

	Compilation Hierarchy Node	Combinational ALUTs	Dedicated Logic Registers	Block Memory Bits	DSP Blocks	Pins	Virtual Pins	Full Hierarchy Name	Entity Name	Library Name
								scfifo:Sync_FIFO|scfifo_8ba1:auto_generated		
1	|a_dpfifo_r2a1:dpfifo|	47 (24)	33 (13)	3072	0	0	0	|DE1_SoC|audio_codec:codec|Altera_UP_Audio_In_Deserializer:Audio_In_Deserializer|Altera_UP_SYNC_FIFO:Audio_In_Left_Channel_FIFO|scfifo:Sync_FIFO|scfifo_8ba1:auto_generated|a_dpfifo_r2a1:dpfifo	a_dpfifo_r2a1	work
1	|altsyncram_p3i1:FIFOram|	0 (0)	0 (0)	3072	0	0	0	|DE1_SoC|audio_codec:codec|Altera_UP_Audio_In_Deserializer:Audio_In_Deserializer|Altera_UP_SYNC_FIFO:Audio_In_Left_Channel_FIFO|scfifo:Sync_FIFO|scfifo_8ba1:auto_generated|a_dpfifo_r2a1:dpfifo|altsyncram_p3i1:FIFOra	altsyncram_p3i1	work

	Compilation Hierarchy Node	Combinational ALUTs	Dedicated Logic Registers	Block Memory Bits	DSP Blocks	Pins	Virtual Pins	Full Hierarchy Name	Entity Name	Library Name
								m		
2	| cntr_h2b:rd_ptr_msb|	7 (7)	6 (6)	0	0	0	0	|DE1_SoC| audio_codec:codec| Altera_UP_Audio_In_Deserializer:Audio_In_Deserializer| Altera_UP_SYNC_FIFO:Audio_In_Left_Channel_FIFO| scfifo:Sync_FIFO| scfifo_8ba1:auto_generated| a_dpfifo_r2a1:dpfifo| cntr_h2b:rd_ptr_msb	cntr_h2b	work
3	| cntr_i2b:wr_ptr|	8 (8)	7 (7)	0	0	0	0	|DE1_SoC| audio_codec:codec| Altera_UP_Audio_In_Deserializer:Audio_In_Deserializer| Altera_UP_SYNC_FIFO:Audio_In_Left_Channel_FIFO| scfifo:Sync_FIFO| scfifo_8ba1:auto_generated| a_dpfifo_r2a1:dpfifo| cntr_i2b:wr_ptr	cntr_i2b	work
4	| cntr_u27:u	8 (8)	7 (7)	0	0	0	0	|DE1_SoC| audio_code	cntr_u27	work

	Compilation Hierarchy Node	Combinational ALUTs	Dedicated Logic Registers	Block Memory Bits	DSP Blocks	Pins	Virtual Pins	Full Hierarchy Name	Entity Name	Library Name
	sedw_counter|							c:codec|Altera_UP_Audio_In_Deserializer:Audio_In_Deserializer|Altera_UP_SYNC_FIFO:Audio_In_Left_Channel_FIFO|scfifo:Sync_FIFO|scfifo_8ba1:auto_generated|a_dpfifo_r2a1:dpfifo|cntr_u27:usedw_counter		
3	|Altera_UP_SYNC_FIFO:Audio_In_Right_Channel_FIFO|	47 (0)	33 (0)	3072	0	0	0	|DE1_SoC|audio_codec:codec|Altera_UP_Audio_In_Deserializer:Audio_In_Deserializer|Altera_UP_SYNC_FIFO:Audio_In_Right_Channel_FIFO	Altera_UP_SYNC_FIFO	work
1	|scfifo:Sync_FIFO|	47 (0)	33 (0)	3072	0	0	0	|DE1_SoC|audio_codec:codec|Altera_UP_Audio_In_Deserializer:Audio_In_Deserializer|Altera_UP_SYNC_FIFO:Audio_In_Right_Channel_FIFO|	scfifo	work

	Compilation Hierarchy Node	Combinational ALUTs	Dedicated Logic Registers	Block Memory Bits	DSP Blocks	Pins	Virtual Pins	Full Hierarchy Name	Entity Name	Library Name
								scfifo:Sync_FIFO		
1	| scfifo_8ba1:auto_generated|	47 (0)	33 (0)	3072	0	0	0	|DE1_SoC|audio_codec:codec|Altera_UP_Audio_In_Deserializer:Audio_In_Deserializer|Altera_UP_SYNC_FIFO:Audio_In_Right_Channel_FIFO|scfifo:Sync_FIFO|scfifo_8ba1:auto_generated	scfifo_8ba1	work
1	| a_dpfifo_r2a1:dpfifo|	47 (24)	33 (13)	3072	0	0	0	|DE1_SoC|audio_codec:codec|Altera_UP_Audio_In_Deserializer:Audio_In_Deserializer|Altera_UP_SYNC_FIFO:Audio_In_Right_Channel_FIFO|scfifo:Sync_FIFO|scfifo_8ba1:auto_generated|a_dpfifo_r2a1:dpfifo	a_dpfifo_r2a1	work
1	| altsyncram_p3i1:FIFOram|	0 (0)	0 (0)	3072	0	0	0	|DE1_SoC|audio_codec:codec|Altera_UP_Audio_In_Deserializer:Audio_In_Deseri	altsyncram_p3i1	work

	Compilation Hierarchy Node	Combinational ALUTs	Dedicated Logic Registers	Block Memory Bits	DSP Blocks	Pins	Virtual Pins	Full Hierarchy Name	Entity Name	Library Name
								alizer|Altera_UP_SYNC_FIFO:Audio_In_Right_Channel_FIFO|scfifo:Sync_FIFO|scfifo_8ba1:auto_generated|a_dpfifo_r2a1:dpfifo|altsyncram_p3i1:FIFOram		
2	|cntr_h2b:rd_ptr_msb|	7 (7)	6 (6)	0	0	0	0	|DE1_SoC|audio_codec:codec|Altera_UP_Audio_In_Deserializer:Audio_In_Deserializer|Altera_UP_SYNC_FIFO:Audio_In_Right_Channel_FIFO|scfifo:Sync_FIFO|scfifo_8ba1:auto_generated|a_dpfifo_r2a1:dpfifo|cntr_h2b:rd_ptr_msb	cntr_h2b	work
3	|cntr_i2b:wr_ptr|	8 (8)	7 (7)	0	0	0	0	|DE1_SoC|audio_codec:codec|Altera_UP_Audio_In_Deserializer:Audio_In_Deserializer|Altera_UP_S	cntr_i2b	work

	Compilation Hierarchy Node	Combinational ALUTs	Dedicated Logic Registers	Block Memory Bits	DSP Blocks	Pins	Virtual Pins	Full Hierarchy Name	Entity Name	Library Name
								YNC_FIFO:Audio_In_Right_Channel_FIFO|scfifo:Sync_FIFO|scfifo_8ba1:auto_generated|a_dpfifo_r2a1:dpfifo|cntr_i2b:wr_ptr		
4	|cntr_u27:usedw_counter|	8 (8)	7 (7)	0	0	0	0	|DE1_SoC|audio_codec:codec|Altera_UP_Audio_In_Deserializer:Audio_In_Deserializer|Altera_UP_SYNC_FIFO:Audio_In_Right_Channel_FIFO|scfifo:Sync_FIFO|scfifo_8ba1:auto_generated|a_dpfifo_r2a1:dpfifo|cntr_u27:usedw_counter	cntr_u27	work
2	|Altera_UP_Audio_Out_Serializer:Audio_Out_Serializer|	145 (49)	108 (42)	6144	0	0	0	|DE1_SoC|audio_codec:codec|Altera_UP_Audio_Out_Serializer:Audio_Out_Serializer	Altera_UP_Audio_Out_Serializer	work
1	|Altera_UP_SYNC_FIF	48 (0)	33 (0)	3072	0	0	0	|DE1_SoC|audio_codec:codec|	Altera_UP_SYNC_FIFO	work

	Compilation Hierarchy Node	Combinational ALUTs	Dedicated Logic Registers	Block Memory Bits	DSP Blocks	Pins	Virtual Pins	Full Hierarchy Name	Entity Name	Library Name
	O:Audio_Out_Left_Channel_FIFO|							Altera_UP_Audio_Out_Serializer:Audio_Out_Serializer| Altera_UP_SYNC_FIFO:Audio_Out_Left_Channel_FIFO		
1	| scfifo:Sync_FIFO|	48 (0)	33 (0)	3072	0	0	0	|DE1_SoC| audio_codec:codec| Altera_UP_Audio_Out_Serializer:Audio_Out_Serializer| Altera_UP_SYNC_FIFO:Audio_Out_Left_Channel_FIFO| scfifo:Sync_FIFO	scfifo	work
1	| scfifo_8ba1:auto_generated|	48 (0)	33 (0)	3072	0	0	0	|DE1_SoC| audio_codec:codec| Altera_UP_Audio_Out_Serializer:Audio_Out_Serializer| Altera_UP_SYNC_FIFO:Audio_Out_Left_Channel_FIFO| scfifo:Sync_FIFO| scfifo_8ba1:auto_generated	scfifo_8ba1	work
1	| a_dpfifo_r2a1:dpfifo|	48 (25)	33 (13)	3072	0	0	0	|DE1_SoC| audio_codec:codec| Altera_UP_A	a_dpfifo_r2a1	work

	Compilation Hierarchy Node	Combinational ALUTs	Dedicated Logic Registers	Block Memory Bits	DSP Blocks	Pins	Virtual Pins	Full Hierarchy Name	Entity Name	Library Name
								udio_Out_Serializer:Audio_Out_Serializer|Altera_UP_SYNC_FIFO:Audio_Out_Left_Channel_FIFO|scfifo:Sync_FIFO|scfifo_8ba1:auto_generated|a_dpfifo_r2a1:dpfifo		
1	|altsyncram_p3i1:FIFOram|	0 (0)	0 (0)	3072	0	0	0	|DE1_SoC|audio_codec:codec|Altera_UP_Audio_Out_Serializer:Audio_Out_Serializer|Altera_UP_SYNC_FIFO:Audio_Out_Left_Channel_FIFO|scfifo:Sync_FIFO|scfifo_8ba1:auto_generated|a_dpfifo_r2a1:dpfifo|altsyncram_p3i1:FIFOram	altsyncram_p3i1	work
2	|cntr_h2b:rd_ptr_msb|	7 (7)	6 (6)	0	0	0	0	|DE1_SoC|audio_codec:codec|Altera_UP_Audio_Out_Serializer:Audio_Out_Serializer|	cntr_h2b	work

	Compilation Hierarchy Node	Combinational ALUTs	Dedicated Logic Registers	Block Memory Bits	DSP Blocks	Pins	Virtual Pins	Full Hierarchy Name	Entity Name	Library Name
								Altera_UP_SYNC_FIFO:Audio_Out_Left_Channel_FIFO|scfifo:Sync_FIFO|scfifo_8ba1:auto_generated|a_dpfifo_r2a1:dpfifo|cntr_h2b:rd_ptr_msb		
3	|cntr_i2b:wr_ptr|	8 (8)	7 (7)	0	0	0	0	|DE1_SoC|audio_codec:codec|Altera_UP_Audio_Out_Serializer:Audio_Out_Serializer|Altera_UP_SYNC_FIFO:Audio_Out_Left_Channel_FIFO|scfifo:Sync_FIFO|scfifo_8ba1:auto_generated|a_dpfifo_r2a1:dpfifo|cntr_i2b:wr_ptr	cntr_i2b	work
4	|cntr_u27:usedw_counter|	8 (8)	7 (7)	0	0	0	0	|DE1_SoC|audio_codec:codec|Altera_UP_Audio_Out_Serializer:Audio_Out_Serializer|Altera_UP_SYNC_FIFO:Audio_Out_L	cntr_u27	work

	Compilation Hierarchy Node	Combinational ALUTs	Dedicated Logic Registers	Block Memory Bits	DSP Blocks	Pins	Virtual Pins	Full Hierarchy Name	Entity Name	Library Name
								eft_Channel_FIFO|scfifo:Sync_FIFO|scfifo_8ba1:auto_generated|a_dpfifo_r2a1:dpfifo|cntr_u27:usedw_counter		
2	|Altera_UP_SYNC_FIFO:Audio_Out_Right_Channel_FIFO|	48 (0)	33 (0)	3072	0	0	0	|DE1_SoC|audio_codec:codec|Altera_UP_Audio_Out_Serializer:Audio_Out_Serializer|Altera_UP_SYNC_FIFO:Audio_Out_Right_Channel_FIFO	Altera_UP_SYNC_FIFO	work
1	|scfifo:Sync_FIFO|	48 (0)	33 (0)	3072	0	0	0	|DE1_SoC|audio_codec:codec|Altera_UP_Audio_Out_Serializer:Audio_Out_Serializer|Altera_UP_SYNC_FIFO:Audio_Out_Right_Channel_FIFO|scfifo:Sync_FIFO	scfifo	work
1	|scfifo_8ba1:auto_generated|	48 (0)	33 (0)	3072	0	0	0	|DE1_SoC|audio_codec:codec|Altera_UP_Audio_Out_Serializer:Audio_Out_Seri	scfifo_8ba1	work

	Compilation Hierarchy Node	Combinational ALUTs	Dedicated Logic Registers	Block Memory Bits	DSP Blocks	Pins	Virtual Pins	Full Hierarchy Name	Entity Name	Library Name
								alizer|Altera_UP_SYNC_FIFO:Audio_Out_Right_Channel_FIFO|scfifo:Sync_FIFO|scfifo_8ba1:auto_generated		
1	|a_dpfifo_r2a1:dpfifo|	48 (25)	33 (13)	3072	0	0	0	|DE1_SoC|audio_codec:codec|Altera_UP_Audio_Out_Serializer:Audio_Out_Serializer|Altera_UP_SYNC_FIFO:Audio_Out_Right_Channel_FIFO|scfifo:Sync_FIFO|scfifo_8ba1:auto_generated|a_dpfifo_r2a1:dpfifo	a_dpfifo_r2a1	work
1	|altsyncram_p3i1:FIFOram|	0 (0)	0 (0)	3072	0	0	0	|DE1_SoC|audio_codec:codec|Altera_UP_Audio_Out_Serializer:Audio_Out_Serializer|Altera_UP_SYNC_FIFO:Audio_Out_Right_Channel_FIFO|scfifo:Sync_FIFO|scfifo_8ba1:	altsyncram_p3i1	work

	Compilation Hierarchy Node	Combinational ALUTs	Dedicated Logic Registers	Block Memory Bits	DSP Blocks	Pins	Virtual Pins	Full Hierarchy Name	Entity Name	Library Name
								auto_generated|a_dpfifo_r2a1:dpfifo|altsyncram_p3i1:FIFOram		
2	|cntr_h2b:rd_ptr_msb|	7 (7)	6 (6)	0	0	0	0	|DE1_SoC|audio_codec:codec|Altera_UP_Audio_Out_Serializer:Audio_Out_Serializer|Altera_UP_SYNC_FIFO:Audio_Out_Right_Channel_FIFO|scfifo:Sync_FIFO|scfifo_8ba1:auto_generated|a_dpfifo_r2a1:dpfifo|cntr_h2b:rd_ptr_msb	cntr_h2b	work
3	|cntr_i2b:wr_ptr|	8 (8)	7 (7)	0	0	0	0	|DE1_SoC|audio_codec:codec|Altera_UP_Audio_Out_Serializer:Audio_Out_Serializer|Altera_UP_SYNC_FIFO:Audio_Out_Right_Channel_FIFO|scfifo:Sync_FIFO|scfifo_8ba1:auto_generated|	cntr_i2b	work

	Compilation Hierarchy Node	Combinational ALUTs	Dedicated Logic Registers	Block Memory Bits	DSP Blocks	Pins	Virtual Pins	Full Hierarchy Name	Entity Name	Library Name
								a_dpfifo_r2a1:dpfifo|cntr_i2b:wr_ptr		
4	|cntr_u27:usedw_counter|	8 (8)	7 (7)	0	0	0	0	|DE1_SoC|audio_codec:codec|Altera_UP_Audio_Out_Serializer:Audio_Out_Serializer|Altera_UP_SYNC_FIFO:Audio_Out_Right_Channel_FIFO|scfifo:Sync_FIFO|scfifo_8ba1:auto_generated|a_dpfifo_r2a1:dpfifo|cntr_u27:usedw_counter	cntr_u27	work
3	|Altera_UP_Clock_Edge:ADC_Left_Right_Clock_Edges|	1 (1)	2 (2)	0	0	0	0	|DE1_SoC|audio_codec:codec|Altera_UP_Clock_Edge:ADC_Left_Right_Clock_Edges	Altera_UP_Clock_Edge	work
4	|Altera_UP_Clock_Edge:Bit_Clock_Edges|	1 (1)	2 (2)	0	0	0	0	|DE1_SoC|audio_codec:codec|Altera_UP_Clock_Edge:Bit_Clock_Edges	Altera_UP_Clock_Edge	work
5	|Altera_UP_Clock_Edge:DAC_Left_Right_Clo	1 (1)	2 (2)	0	0	0	0	|DE1_SoC|audio_codec:codec|Altera_UP_Clock_Edge:D	Altera_UP_Clock_Edge	work

	Compilation Hierarchy Node	Combinational ALUTs	Dedicated Logic Registers	Block Memory Bits	DSP Blocks	Pins	Virtual Pins	Full Hierarchy Name	Entity Name	Library Name
	ck_Edges|							AC_Left_Right_Clock_Edges		
3	|board_logic:board|	21 (21)	34 (34)	0	0	0	0	|DE1_SoC|board_logic:board	board_logic	work
4	|clock_divider:cdiv|	23 (23)	23 (23)	0	0	0	0	|DE1_SoC|clock_divider:cdiv	clock_divider	work
5	|clock_generator:my_clock_gen|	0 (0)	0 (0)	0	0	0	0	|DE1_SoC|clock_generator:my_clock_gen	clock_generator	work
1	|altpll:DE_Clock_Generator_Audio|	0 (0)	0 (0)	0	0	0	0	|DE1_SoC|clock_generator:my_clock_gen|altpll:DE_Clock_Generator_Audio	altpll	work
1	|altpll_1uu1:auto_generated|	0 (0)	0 (0)	0	0	0	0	|DE1_SoC|clock_generator:my_clock_gen|altpll:DE_Clock_Generator_Audio|altpll_1uu1:auto_generated	altpll_1uu1	work
6	|collision_detection:comb_193|	5 (5)	1 (1)	0	0	0	0	|DE1_SoC|collision_detection:comb_193	collision_detection	work
7	|counter:scoring|	52 (52)	40 (40)	0	0	0	0	|DE1_SoC|counter:scoring	counter	work
8	|generate_row:row|	20 (16)	15 (12)	0	0	0	0	|DE1_SoC|generate_row:row	generate_row	work
1	|LFSR:lfsr|	4 (4)	3 (3)	0	0	0	0	|DE1_SoC|generate_row:row|LFSR:lfsr	LFSR	work
9	|keyboard_press_driv	26 (12)	55 (21)	0	0	0	0	|DE1_SoC|keyboard_press_driver:	keyboard_press_driver	work

	Compilation Hierarchy Node	Combinational ALUTs	Dedicated Logic Registers	Block Memory Bits	DSP Blocks	Pins	Virtual Pins	Full Hierarchy Name	Entity Name	Library Name
	er:keyboard|							keyboard		
1	| keyboard_inner_driver:kbd|	14 (14)	34 (34)	0	0	0	0	|DE1_SoC| keyboard_press_driver:keyboard| keyboard_inner_driver:kbd	keyboard_inner_driver	work
10	| obstacle_logic:obs|	0 (0)	134 (134)	0	0	0	0	|DE1_SoC| obstacle_logic:obs	obstacle_logic	work
11	|player:pl|	15 (15)	5 (5)	0	0	0	0	|DE1_SoC| player:pl	player	work
12	| sld_hub:auto_hub|	92 (1)	91 (0)	0	0	0	0	|DE1_SoC| sld_hub:auto_hub	sld_hub	altera_sld
1	| alt_sld_fab_with_jtag_input:\instrumentation_fabric_with_node_gen:fabric_gen_new_way:with_jtag_input_gen:instrumentation_fabric|	91 (0)	91 (0)	0	0	0	0	|DE1_SoC| sld_hub:auto_hub| alt_sld_fab_with_jtag_input:\instrumentation_fabric_with_node_gen:fabric_gen_new_way:with_jtag_input_gen:instrumentation_fabric	alt_sld_fab_with_jtag_input	altera_sld
1	| alt_sld_fab:instrumentation_fabric|	91 (0)	91 (0)	0	0	0	0	|DE1_SoC| sld_hub:auto_hub| alt_sld_fab_with_jtag_input:\instrumentation_fabric_with_node_gen:fabric_gen_new_way:with_jtag_input_gen:instrumentation_fabric|	alt_sld_fab	alt_sld_fab

	Compilation Hierarchy Node	Combinational ALUTs	Dedicated Logic Registers	Block Memory Bits	DSP Blocks	Pins	Virtual Pins	Full Hierarchy Name	Entity Name	Library Name
								alt_sld_fab:instrumentation_fabric		
1	| alt_sld_fab_alt_sld_fab:alt_sld_fab|	91 (1)	91 (5)	0	0	0	0	|DE1_SoC|sld_hub:auto_hub|alt_sld_fab_with_jtag_input:\instrumentation_fabric_with_node_gen:fabric_gen_new_way:with_jtag_input_gen:instrumentation_fabric|alt_sld_fab:instrumentation_fabric|alt_sld_fab_alt_sld_fab:alt_sld_fab	alt_sld_fab_alt_sld_fab	alt_sld_fab
1	| alt_sld_fab_alt_sld_fab_sldfabric:sldfabric|	90 (0)	86 (0)	0	0	0	0	|DE1_SoC|sld_hub:auto_hub|alt_sld_fab_with_jtag_input:\instrumentation_fabric_with_node_gen:fabric_gen_new_way:with_jtag_input_gen:instrumentation_fabric|alt_sld_fab:instrumentation_fabric|alt_sld_fab_alt_sld_fab:alt_sld_fab|alt_sld_fab_alt_sld_fab_	alt_sld_fab_alt_sld_fab_sldfabric	alt_sld_fab

	Compilation Hierarchy Node	Combinational ALUTs	Dedicated Logic Registers	Block Memory Bits	DSP Blocks	Pins	Virtual Pins	Full Hierarchy Name	Entity Name	Library Name
								sldfabric:sldfabric		
1	| sld_jtag_hub:\jtag_hub_gen:real_sld_jtag_hub|	90 (57)	86 (58)	0	0	0	0	|DE1_SoC|sld_hub:auto_hub|alt_sld_fab_with_jtag_input:\instrumentation_fabric_with_node_gen:fabric_gen_new_way:with_jtag_input_gen:instrumentation_fabric|alt_sld_fab:instrumentation_fabric|alt_sld_fab_alt_sld_fab:alt_sld_fab|alt_sld_fab_alt_sld_fab_sldfabric:sldfabric|sld_jtag_hub:\jtag_hub_gen:real_sld_jtag_hub	sld_jtag_hub	work
1	| sld_rom_sr:hub_info_reg|	15 (15)	9 (9)	0	0	0	0	|DE1_SoC|sld_hub:auto_hub|alt_sld_fab_with_jtag_input:\instrumentation_fabric_with_node_gen:fabric_gen_new_way:with_jtag_input_gen:instrumentation_fabric|	sld_rom_sr	work

	Compilation Hierarchy Node	Combinational ALUTs	Dedicated Logic Registers	Block Memory Bits	DSP Blocks	Pins	Virtual Pins	Full Hierarchy Name	Entity Name	Library Name
								alt_sld_fab:instrumentation_fabric|alt_sld_fab_alt_sld_fab:alt_sld_fab|alt_sld_fab_alt_sld_fab_sldfabric:sldfabric|sld_jtag_hub:\jtag_hub_gen:real_sld_jtag_hub|sld_rom_sr:hub_info_reg		
2	|sld_shadow_jsm:shadow_jsm|	18 (18)	19 (19)	0	0	0	0	|DE1_SoC|sld_hub:auto_hub|alt_sld_fab_with_jtag_input:\instrumentation_fabric_with_node_gen:fabric_gen_new_way:with_jtag_input_gen:instrumentation_fabric|alt_sld_fab:instrumentation_fabric|alt_sld_fab_alt_sld_fab:alt_sld_fab|alt_sld_fab_alt_sld_fab_sldfabric:sldfabric|sld_jtag_hub:\jtag_hub_gen:real_sld_j	sld_shadow_jsm	altera_sld

	Compilation Hierarchy Node	Combinational ALUTs	Dedicated Logic Registers	Block Memory Bits	DSP Blocks	Pins	Virtual Pins	Full Hierarchy Name	Entity Name	Library Name
								tag_hub|sld_shadow_jsm:shadow_jsm		
13	|sld_signaltap:auto_signaltap_0|	244 (2)	632 (60)	3840	0	0	0	|DE1_SoC|sld_signaltap:auto_signaltap_0	sld_signaltap	work
1	|sld_signaltap_impl:sld_signaltap_body|	242 (0)	572 (0)	3840	0	0	0	|DE1_SoC|sld_signaltap:auto_signaltap_0|sld_signaltap_impl:sld_signaltap_body	sld_signaltap_impl	work
1	|sld_signaltap_implb:sld_signaltap_body|	242 (67)	572 (194)	3840	0	0	0	|DE1_SoC|sld_signaltap:auto_signaltap_0|sld_signaltap_impl:sld_signaltap_body|sld_signaltap_implb:sld_signaltap_body	sld_signaltap_implb	work
1	altdpram:\stp_non_zero_ram_gen:attribute_mem_gen:attribute_mem|	2 (0)	46 (46)	0	0	0	0	|DE1_SoC|sld_signaltap:auto_signaltap_0|sld_signaltap_impl:sld_signaltap_body|sld_signaltap_implb:sld_signaltap_body|altdpram:\stp_non_zero_ram_gen:attribute_mem_gen:attribute_mem	altdpram	work
1	|	2 (0)	0 (0)	0	0	0	0	|DE1_SoC|	lpm_decode	work

	Compilation Hierarchy Node	Combinational ALUTs	Dedicated Logic Registers	Block Memory Bits	DSP Blocks	Pins	Virtual Pins	Full Hierarchy Name	Entity Name	Library Name
	lpm_decode:wdecoder|							sld_signaltap:auto_signaltap_0|sld_signaltap_impl:sld_signaltap_body|sld_signaltap_implb:sld_signaltap_body|altdpram:\stp_non_zero_ram_gen:attribute_mem_gen:attribute_mem|lpm_decode:wdecoder		
1	| decode_vnf:auto_generated|	2 (2)	0 (0)	0	0	0	0	|DE1_SoC|sld_signaltap:auto_signaltap_0|sld_signaltap_impl:sld_signaltap_body|sld_signaltap_implb:sld_signaltap_body|altdpram:\stp_non_zero_ram_gen:attribute_mem_gen:attribute_mem|lpm_decode:wdecoder|decode_vnf:auto_generated	decode_vnf	work
2	| altsyncram:\stp_non_zero_ram_g	0 (0)	0 (0)	3840	0	0	0	|DE1_SoC|sld_signaltap:auto_signaltap_0|sld_signalta	altsyncram	work

	Compilation Hierarchy Node	Combinational ALUTs	Dedicated Logic Registers	Block Memory Bits	DSP Blocks	Pins	Virtual Pins	Full Hierarchy Name	Entity Name	Library Name
	en:stp_buffer_ram|							p_impl:sld_signaltap_body|sld_signaltap_implb:sld_signaltap_body|altsyncram:\stp_non_zero_ram_gen:stp_buffer_ram		
1	| altsyncram_cb84:auto_generated|	0 (0)	0 (0)	3840	0	0	0	|DE1_SoC|sld_signaltap:auto_signaltap_0|sld_signaltap_impl:sld_signaltap_body|sld_signaltap_implb:sld_signaltap_body|altsyncram:\stp_non_zero_ram_gen:stp_buffer_ram|altsyncram_cb84:auto_generated	altsyncram_cb84	work
3	| lpm_shiftreg:segment_offset_config_deserialize|	0 (0)	7 (7)	0	0	0	0	|DE1_SoC|sld_signaltap:auto_signaltap_0|sld_signaltap_impl:sld_signaltap_body|sld_signaltap_implb:sld_signaltap_body|lpm_shiftreg:segment_offset_config_	lpm_shiftreg	work

	Compilation Hierarchy Node	Combinational ALUTs	Dedicated Logic Registers	Block Memory Bits	DSP Blocks	Pins	Virtual Pins	Full Hierarchy Name	Entity Name	Library Name
								deserialize		
4	|lpm_shiftreg:status_register|	17 (17)	17 (17)	0	0	0	0	|DE1_SoC|sld_signaltap:auto_signaltap_0|sld_signaltap_impl:sld_signaltap_body|sld_signaltap_implb:sld_signaltap_body|lpm_shiftreg:status_register	lpm_shiftreg	work
5	|serial_crc_16:\tdo_crc_gen:tdo_crc_calc|	4 (4)	13 (13)	0	0	0	0	|DE1_SoC|sld_signaltap:auto_signaltap_0|sld_signaltap_impl:sld_signaltap_body|sld_signaltap_implb:sld_signaltap_body|serial_crc_16:\tdo_crc_gen:tdo_crc_calc	serial_crc_16	work
6	|sld_buffer_manager:sld_buffer_manager_inst|	58 (58)	44 (44)	0	0	0	0	|DE1_SoC|sld_signaltap:auto_signaltap_0|sld_signaltap_impl:sld_signaltap_body|sld_signaltap_implb:sld_signaltap_body|sld_buffer_manager:sld	sld_buffer_manager	work

	Compilation Hierarchy Node	Combinational ALUTs	Dedicated Logic Registers	Block Memory Bits	DSP Blocks	Pins	Virtual Pins	Full Hierarchy Name	Entity Name	Library Name
								_buffer_manager_inst		
7	| sld_ela_control:ela_control|	38 (1)	166 (1)	0	0	0	0	|DE1_SoC| sld_signaltap:auto_signaltap_0| sld_signaltap_impl:sld_signaltap_body| sld_signaltap_implb:sld_signaltap_body| sld_ela_control:ela_control	sld_ela_control	work
1	| lpm_shiftreg:trigger_config_deserialize|	0 (0)	4 (4)	0	0	0	0	|DE1_SoC| sld_signaltap:auto_signaltap_0| sld_signaltap_impl:sld_signaltap_body| sld_signaltap_implb:sld_signaltap_body| sld_ela_control:ela_control| lpm_shiftreg:trigger_config_deserialize	lpm_shiftreg	work
2	| sld_ela_basic_multi_level_trigger:\basic_multi_level_mbpm_trigger_gen:multi_level_mbpm|	30 (0)	150 (0)	0	0	0	0	|DE1_SoC| sld_signaltap:auto_signaltap_0| sld_signaltap_impl:sld_signaltap_body| sld_signaltap_implb:sld_signaltap_b	sld_ela_basic_multi_level_trigger	work

	Compilation Hierarchy Node	Combinational ALUTs	Dedicated Logic Registers	Block Memory Bits	DSP Blocks	Pins	Virtual Pins	Full Hierarchy Name	Entity Name	Library Name
								ody| sld_ela_control:ela_control| sld_ela_basic_multi_level_trigger: \basic_multi_level_mbpm_trigger_gen:multi_level_mbpm		
1	| lpm_shiftreg:trigger_condition_deserialize|	0 (0)	90 (90)	0	0	0	0	|DE1_SoC| sld_signaltap:auto_signaltap_0| sld_signaltap_impl:sld_signaltap_body| sld_signaltap_implb:sld_signaltap_body| sld_ela_control:ela_control| sld_ela_basic_multi_level_trigger: \basic_multi_level_mbpm_trigger_gen:multi_level_mbpm| lpm_shiftreg:trigger_condition_deserialize	lpm_shiftreg	work
2	| sld_mbpmg: \trigger_modules_gen:0:trigger_match|	30 (0)	60 (0)	0	0	0	0	|DE1_SoC| sld_signaltap:auto_signaltap_0| sld_signaltap_impl:sld_signaltap_body|	sld_mbpmg	work

	Compilation Hierarchy Node	Combinational ALUTs	Dedicated Logic Registers	Block Memory Bits	DSP Blocks	Pins	Virtual Pins	Full Hierarchy Name	Entity Name	Library Name
								sld_signaltap_implb:sld_signaltap_body|sld_ela_control:ela_control|sld_ela_basic_multi_level_trigger:\basic_multi_level_mbpm_trigger_gen:multi_level_mbpm|sld_mbpmg:\trigger_modules_gen:0:trigger_match		
1	|sld_sbpmg:\gen_sbpmg_pipeline_less_than_two:sm0:0:sm1|	1 (1)	2 (2)	0	0	0	0	|DE1_SoC|sld_signaltap:auto_signaltap_0|sld_signaltap_impl:sld_signaltap_body|sld_signaltap_implb:sld_signaltap_body|sld_ela_control:ela_control|sld_ela_basic_multi_level_trigger:\basic_multi_level_mbpm_trigger_gen:multi_level_mbpm|sld_mbpmg:\trigger_modules_gen:0:trigger_matc	sld_sbpmg	work

	Compilation Hierarchy Node	Combinational ALUTs	Dedicated Logic Registers	Block Memory Bits	DSP Blocks	Pins	Virtual Pins	Full Hierarchy Name	Entity Name	Library Name
								h| sld_sbpmg: \gen_sbpmg_pipeline_less_than_two:sm0:0:sm1		
2	| sld_sbpmg: \gen_sbpmg_pipeline_less_than_two:sm0:10:sm1|	1 (1)	2 (2)	0	0	0	0	|DE1_SoC| sld_signaltap:auto_signaltap_0| sld_signaltap_impl:sld_signaltap_body| sld_signaltap_implb:sld_signaltap_body| sld_ela_control:ela_control| sld_ela_basic_multi_level_trigger: \basic_multi_level_mbpm_trigger_gen:multi_level_mbpm| sld_mbpmg: \trigger_modules_gen:0:trigger_match| sld_sbpmg: \gen_sbpmg_pipeline_less_than_two:sm0:10:sm1	sld_sbpmg	work
3	| sld_sbpmg: \gen_sbpmg_pipeline_less_than_two:sm0:11:sm1|	1 (1)	2 (2)	0	0	0	0	|DE1_SoC| sld_signaltap:auto_signaltap_0| sld_signaltap_impl:sld_signaltap_body|	sld_sbpmg	work

	Compilation Hierarchy Node	Combinational ALUTs	Dedicated Logic Registers	Block Memory Bits	DSP Blocks	Pins	Virtual Pins	Full Hierarchy Name	Entity Name	Library Name
								sld_signaltap_implb:sld_signaltap_body|sld_ela_control:ela_control|sld_ela_basic_multi_level_trigger:\basic_multi_level_mbpm_trigger_gen:multi_level_mbpm|sld_mbpmg:\trigger_modules_gen:0:trigger_match|sld_sbpmg:\gen_sbpmg_pipeline_less_than_two:sm0:11:sm1		
4	|sld_sbpmg:\gen_sbpmg_pipeline_less_than_two:sm0:12:sm1|	1 (1)	2 (2)	0	0	0	0	|DE1_SoC|sld_signaltap:auto_signaltap_0|sld_signaltap_impl:sld_signaltap_body|sld_signaltap_implb:sld_signaltap_body|sld_ela_control:ela_control|sld_ela_basic_multi_level_trigger:\basic_multi_level_mbpm_trigger_gen:multi_lev	sld_sbpmg	work

	Compilation Hierarchy Node	Combinational ALUTs	Dedicated Logic Registers	Block Memory Bits	DSP Blocks	Pins	Virtual Pins	Full Hierarchy Name	Entity Name	Library Name
								el_mbpm| sld_mbpmg: \trigger_modules_gen:0: trigger_match| sld_sbpmg: \gen_sbpmg_pipeline_less_than_two :sm0:12:sm1		
5	| sld_sbpmg: \gen_sbpmg_pipeline_less_than_two:sm0:13:sm1|	1 (1)	2 (2)	0	0	0	0	|DE1_SoC| sld_signaltap:auto_signaltap_0| sld_signaltap_impl:sld_signaltap_body| sld_signaltap_implb:sld_signaltap_body| sld_ela_control:ela_control| sld_ela_basic_multi_level_trigger: \basic_multi_level_mbpm_trigger_gen:multi_level_mbpm| sld_mbpmg: \trigger_modules_gen:0: trigger_match| sld_sbpmg: \gen_sbpmg_pipeline_less_than_two :sm0:13:sm1	sld_sbpmg	work
6	| sld_sbpmg:	1 (1)	2 (2)	0	0	0	0	|DE1_SoC| sld_signaltap:auto_signa	sld_sbpmg	work

	Compilation Hierarchy Node	Combinational ALUTs	Dedicated Logic Registers	Block Memory Bits	DSP Blocks	Pins	Virtual Pins	Full Hierarchy Name	Entity Name	Library Name
	\gen_sbpmg_pipeline_less_than_two:sm0:14:sm1|							ltap_0|sld_signaltap_impl:sld_signaltap_body|sld_signaltap_implb:sld_signaltap_body|sld_ela_control:ela_control|sld_ela_basic_multi_level_trigger:\basic_multi_level_mbpm_trigger_gen:multi_level_mbpm|sld_mbpmg:\trigger_modules_gen:0:trigger_match|sld_sbpmg:\gen_sbpmg_pipeline_less_than_two:sm0:14:sm1		
7	|sld_sbpmg:\gen_sbpmg_pipeline_less_than_two:sm0:15:sm1|	1 (1)	2 (2)	0	0	0	0	|DE1_SoC|sld_signaltap:auto_signaltap_0|sld_signaltap_impl:sld_signaltap_body|sld_signaltap_implb:sld_signaltap_body|sld_ela_control:ela_control|sld_ela_basic_multi_leve	sld_sbpmg	work

	Compilation Hierarchy Node	Combinational ALUTs	Dedicated Logic Registers	Block Memory Bits	DSP Blocks	Pins	Virtual Pins	Full Hierarchy Name	Entity Name	Library Name
								l_trigger:\basic_multi_level_mbpm_trigger_gen:multi_level_mbpm|sld_mbpmg:\trigger_modules_gen:0:trigger_match|sld_sbpmg:\gen_sbpmg_pipeline_less_than_two:sm0:15:sm1		
8	|sld_sbpmg:\gen_sbpmg_pipeline_less_than_two:sm0:16:sm1|	1 (1)	2 (2)	0	0	0	0	|DE1_SoC|sld_signaltap:auto_signaltap_0|sld_signaltap_impl:sld_signaltap_body|sld_signaltap_implb:sld_signaltap_body|sld_ela_control:ela_control|sld_ela_basic_multi_level_trigger:\basic_multi_level_mbpm_trigger_gen:multi_level_mbpm|sld_mbpmg:\trigger_modules_gen:0:trigger_match|sld_sbpmg:\gen_sbpmg_pipeline_le	sld_sbpmg	work

	Compilation Hierarchy Node	Combinational ALUTs	Dedicated Logic Registers	Block Memory Bits	DSP Blocks	Pins	Virtual Pins	Full Hierarchy Name	Entity Name	Library Name
								ss_than_two:sm0:16:sm1		
9	| sld_sbpmg:\gen_sbpmg_pipeline_less_than_two:sm0:17:sm1|	1 (1)	2 (2)	0	0	0	0	|DE1_SoC|sld_signaltap:auto_signaltap_0|sld_signaltap_impl:sld_signaltap_body|sld_signaltap_implb:sld_signaltap_body|sld_ela_control:ela_control|sld_ela_basic_multi_level_trigger:\basic_multi_level_mbpm_trigger_gen:multi_level_mbpm|sld_mbpmg:\trigger_modules_gen:0:trigger_match|sld_sbpmg:\gen_sbpmg_pipeline_less_than_two:sm0:17:sm1	sld_sbpmg	work
10	| sld_sbpmg:\gen_sbpmg_pipeline_less_than_two:sm0:18:sm1|	1 (1)	2 (2)	0	0	0	0	|DE1_SoC|sld_signaltap:auto_signaltap_0|sld_signaltap_impl:sld_signaltap_body|sld_signaltap_implb:sld_signaltap_body|	sld_sbpmg	work

	Compilation Hierarchy Node	Combinational ALUTs	Dedicated Logic Registers	Block Memory Bits	DSP Blocks	Pins	Virtual Pins	Full Hierarchy Name	Entity Name	Library Name
								sld_ela_control:ela_control|sld_ela_basic_multi_level_trigger:\basic_multi_level_mbpm_trigger_gen:multi_level_mbpm|sld_mbpmg:\trigger_modules_gen:0:trigger_match|sld_sbpmg:\gen_sbpmg_pipeline_less_than_two:sm0:18:sm1		
11	|sld_sbpmg:\gen_sbpmg_pipeline_less_than_two:sm0:19:sm1|	1 (1)	2 (2)	0	0	0	0	|DE1_SoC|sld_signaltap:auto_signaltap_0|sld_signaltap_impl:sld_signaltap_body|sld_signaltap_implb:sld_signaltap_body|sld_ela_control:ela_control|sld_ela_basic_multi_level_trigger:\basic_multi_level_mbpm_trigger_gen:multi_level_mbpm|sld_mbpmg:\trigger_modules_gen:0:	sld_sbpmg	work

	Compilation Hierarchy Node	Combinational ALUTs	Dedicated Logic Registers	Block Memory Bits	DSP Blocks	Pins	Virtual Pins	Full Hierarchy Name	Entity Name	Library Name
								trigger_match|sld_sbpmg:\gen_sbpmg_pipeline_less_than_two:sm0:19:sm1		
12	|sld_sbpmg:\gen_sbpmg_pipeline_less_than_two:sm0:1:sm1|	1 (1)	2 (2)	0	0	0	0	|DE1_SoC|sld_signaltap:auto_signaltap_0|sld_signaltap_impl:sld_signaltap_body|sld_signaltap_implb:sld_signaltap_body|sld_ela_control:ela_control|sld_ela_basic_multi_level_trigger:\basic_multi_level_mbpm_trigger_gen:multi_level_mbpm|sld_mbpmg:\trigger_modules_gen:0:trigger_match|sld_sbpmg:\gen_sbpmg_pipeline_less_than_two:sm0:1:sm1	sld_sbpmg	work
13	|sld_sbpmg:\gen_sbpmg_pipeline_less_than_two:sm	1 (1)	2 (2)	0	0	0	0	|DE1_SoC|sld_signaltap:auto_signaltap_0|sld_signaltap_impl:sld_signaltap_bo	sld_sbpmg	work

	Compilation Hierarchy Node	Combinational ALUTs	Dedicated Logic Registers	Block Memory Bits	DSP Blocks	Pins	Virtual Pins	Full Hierarchy Name	Entity Name	Library Name
	0:20:sm1|							dy| sld_signaltap_implb:sld_signaltap_body| sld_ela_control:ela_control| sld_ela_basic_multi_level_trigger:\basic_multi_level_mbpm_trigger_gen:multi_level_mbpm| sld_mbpmg:\trigger_modules_gen:0:trigger_match| sld_sbpmg:\gen_sbpmg_pipeline_less_than_two:sm0:20:sm1		
14	| sld_sbpmg:\gen_sbpmg_pipeline_less_than_two:sm0:21:sm1|	1 (1)	2 (2)	0	0	0	0	|DE1_SoC| sld_signaltap:auto_signaltap_0| sld_signaltap_impl:sld_signaltap_body| sld_signaltap_implb:sld_signaltap_body| sld_ela_control:ela_control| sld_ela_basic_multi_level_trigger:\basic_multi_level_mbpm_trigger_g	sld_sbpmg	work

	Compilation Hierarchy Node	Combinational ALUTs	Dedicated Logic Registers	Block Memory Bits	DSP Blocks	Pins	Virtual Pins	Full Hierarchy Name	Entity Name	Library Name
								en:multi_level_mbpm|sld_mbpmg:\trigger_modules_gen:0:trigger_match|sld_sbpmg:\gen_sbpmg_pipeline_less_than_two:sm0:21:sm1		
15	|sld_sbpmg:\gen_sbpmg_pipeline_less_than_two:sm0:22:sm1|	1 (1)	2 (2)	0	0	0	0	|DE1_SoC|sld_signaltap:auto_signaltap_0|sld_signaltap_impl:sld_signaltap_body|sld_signaltap_implb:sld_signaltap_body|sld_ela_control:ela_control|sld_ela_basic_multi_level_trigger:\basic_multi_level_mbpm_trigger_gen:multi_level_mbpm|sld_mbpmg:\trigger_modules_gen:0:trigger_match|sld_sbpmg:\gen_sbpmg_pipeline_less_than_two:sm0:22:sm1	sld_sbpmg	work
16	|sld_sbpmg	1 (1)	2 (2)	0	0	0	0	|DE1_SoC|sld_signalta	sld_sbpmg	work

	Compilation Hierarchy Node	Combinational ALUTs	Dedicated Logic Registers	Block Memory Bits	DSP Blocks	Pins	Virtual Pins	Full Hierarchy Name	Entity Name	Library Name
	:\gen_sbpmg_pipeline_less_than_two:sm0:23:sm1|							p:auto_signaltap_0|sld_signaltap_impl:sld_signaltap_body|sld_signaltap_implb:sld_signaltap_body|sld_ela_control:ela_control|sld_ela_basic_multi_level_trigger:\basic_multi_level_mbpm_trigger_gen:multi_level_mbpm|sld_mbpmg:\trigger_modules_gen:0:trigger_match|sld_sbpmg:\gen_sbpmg_pipeline_less_than_two:sm0:23:sm1		
17	|sld_sbpmg:\gen_sbpmg_pipeline_less_than_two:sm0:24:sm1|	1 (1)	2 (2)	0	0	0	0	|DE1_SoC|sld_signaltap:auto_signaltap_0|sld_signaltap_impl:sld_signaltap_body|sld_signaltap_implb:sld_signaltap_body|sld_ela_control:ela_control|sld_ela_basi	sld_sbpmg	work

	Compilation Hierarchy Node	Combinational ALUTs	Dedicated Logic Registers	Block Memory Bits	DSP Blocks	Pins	Virtual Pins	Full Hierarchy Name	Entity Name	Library Name
								c_multi_level_trigger:\basic_multi_level_mbpm_trigger_gen:multi_level_mbpm|sld_mbpmg:\trigger_modules_gen:0:trigger_match|sld_sbpmg:\gen_sbpmg_pipeline_less_than_two:sm0:24:sm1		
18	|sld_sbpmg:\gen_sbpmg_pipeline_less_than_two:sm0:25:sm1|	1 (1)	2 (2)	0	0	0	0	|DE1_SoC|sld_signaltap:auto_signaltap_0|sld_signaltap_impl:sld_signaltap_body|sld_signaltap_implb:sld_signaltap_body|sld_ela_control:ela_control|sld_ela_basic_multi_level_trigger:\basic_multi_level_mbpm_trigger_gen:multi_level_mbpm|sld_mbpmg:\trigger_modules_gen:0:trigger_match|sld_sbpmg:\gen_sbpmg	sld_sbpmg	work

	Compilation Hierarchy Node	Combinational ALUTs	Dedicated Logic Registers	Block Memory Bits	DSP Blocks	Pins	Virtual Pins	Full Hierarchy Name	Entity Name	Library Name
								_pipeline_less_than_two:sm0:25:sm1		
19	| sld_sbpmg:\gen_sbpmg_pipeline_less_than_two:sm0:26:sm1|	1 (1)	2 (2)	0	0	0	0	|DE1_SoC|sld_signaltap:auto_signaltap_0|sld_signaltap_impl:sld_signaltap_body|sld_signaltap_implb:sld_signaltap_body|sld_ela_control:ela_control|sld_ela_basic_multi_level_trigger:\basic_multi_level_mbpm_trigger_gen:multi_level_mbpm|sld_mbpmg:\trigger_modules_gen:0:trigger_match|sld_sbpmg:\gen_sbpmg_pipeline_less_than_two:sm0:26:sm1	sld_sbpmg	work
20	| sld_sbpmg:\gen_sbpmg_pipeline_less_than_two:sm0:27:sm1|	1 (1)	2 (2)	0	0	0	0	|DE1_SoC|sld_signaltap:auto_signaltap_0|sld_signaltap_impl:sld_signaltap_body|sld_signaltap_implb:sld_signaltap_b	sld_sbpmg	work

	Compilation Hierarchy Node	Combinational ALUTs	Dedicated Logic Registers	Block Memory Bits	DSP Blocks	Pins	Virtual Pins	Full Hierarchy Name	Entity Name	Library Name
								ody| sld_ela_control:ela_control| sld_ela_basic_multi_level_trigger: \basic_multi_level_mbpm_trigger_gen:multi_level_mbpm| sld_mbpmg: \trigger_modules_gen:0: trigger_match| sld_sbpmg: \gen_sbpmg_pipeline_less_than_two:sm0:27:sm1		
21	| sld_sbpmg: \gen_sbpmg_pipeline_less_than_two:sm0:28:sm1|	1 (1)	2 (2)	0	0	0	0	|DE1_SoC| sld_signaltap:auto_signaltap_0| sld_signaltap_impl:sld_signaltap_body| sld_signaltap_implb:sld_signaltap_body| sld_ela_control:ela_control| sld_ela_basic_multi_level_trigger: \basic_multi_level_mbpm_trigger_gen:multi_level_mbpm| sld_mbpmg: \trigger_mo	sld_sbpmg	work

	Compilation Hierarchy Node	Combinational ALUTs	Dedicated Logic Registers	Block Memory Bits	DSP Blocks	Pins	Virtual Pins	Full Hierarchy Name	Entity Name	Library Name
								dules_gen:0:trigger_match|sld_sbpmg:\gen_sbpmg_pipeline_less_than_two:sm0:28:sm1		
22	|sld_sbpmg:\gen_sbpmg_pipeline_less_than_two:sm0:29:sm1|	1 (1)	2 (2)	0	0	0	0	|DE1_SoC|sld_signaltap:auto_signaltap_0|sld_signaltap_impl:sld_signaltap_body|sld_signaltap_implb:sld_signaltap_body|sld_ela_control:ela_control|sld_ela_basic_multi_level_trigger:\basic_multi_level_mbpm_trigger_gen:multi_level_mbpm|sld_mbpmg:\trigger_modules_gen:0:trigger_match|sld_sbpmg:\gen_sbpmg_pipeline_less_than_two:sm0:29:sm1	sld_sbpmg	work
23	|sld_sbpmg:\gen_sbpmg_pipeline_less_th	1 (1)	2 (2)	0	0	0	0	|DE1_SoC|sld_signaltap:auto_signaltap_0|sld_signaltap_impl:sld_s	sld_sbpmg	work

	Compilation Hierarchy Node	Combinational ALUTs	Dedicated Logic Registers	Block Memory Bits	DSP Blocks	Pins	Virtual Pins	Full Hierarchy Name	Entity Name	Library Name
	an_two:sm0:2:sm1|							ignaltap_body|sld_signaltap_implb:sld_signaltap_body|sld_ela_control:ela_control|sld_ela_basic_multi_level_trigger:\basic_multi_level_mbpm_trigger_gen:multi_level_mbpm|sld_mbpmg:\trigger_modules_gen:0:trigger_match|sld_sbpmg:\gen_sbpmg_pipeline_less_than_two:sm0:2:sm1		
24	|sld_sbpmg:\gen_sbpmg_pipeline_less_than_two:sm0:3:sm1|	1 (1)	2 (2)	0	0	0	0	|DE1_SoC|sld_signaltap:auto_signaltap_0|sld_signaltap_impl:sld_signaltap_body|sld_signaltap_implb:sld_signaltap_body|sld_ela_control:ela_control|sld_ela_basic_multi_level_trigger:\basic_multi_level_mbp	sld_sbpmg	work

	Compilation Hierarchy Node	Combinational ALUTs	Dedicated Logic Registers	Block Memory Bits	DSP Blocks	Pins	Virtual Pins	Full Hierarchy Name	Entity Name	Library Name
								m_trigger_gen:multi_level_mbpm|sld_mbpmg:\trigger_modules_gen:0:trigger_match|sld_sbpmg:\gen_sbpmg_pipeline_less_than_two:sm0:3:sm1		
25	|sld_sbpmg:\gen_sbpmg_pipeline_less_than_two:sm0:4:sm1|	1 (1)	2 (2)	0	0	0	0	|DE1_SoC|sld_signaltap:auto_signaltap_0|sld_signaltap_impl:sld_signaltap_body|sld_signaltap_implb:sld_signaltap_body|sld_ela_control:ela_control|sld_ela_basic_multi_level_trigger:\basic_multi_level_mbpm_trigger_gen:multi_level_mbpm|sld_mbpmg:\trigger_modules_gen:0:trigger_match|sld_sbpmg:\gen_sbpmg_pipeline_less_than_two:sm0:4:sm1	sld_sbpmg	work
26	|	1 (1)	2 (2)	0	0	0	0	|DE1_SoC|	sld_sbpmg	work

	Compilation Hierarchy Node	Combinational ALUTs	Dedicated Logic Registers	Block Memory Bits	DSP Blocks	Pins	Virtual Pins	Full Hierarchy Name	Entity Name	Library Name
	sld_sbpmg:\gen_sbpmg_pipeline_less_than_two:sm0:5:sm1|							sld_signaltap:auto_signaltap_0|sld_signaltap_impl:sld_signaltap_body|sld_signaltap_implb:sld_signaltap_body|sld_ela_control:ela_control|sld_ela_basic_multi_level_trigger:\basic_multi_level_mbpm_trigger_gen:multi_level_mbpm|sld_mbpmg:\trigger_modules_gen:0:trigger_match|sld_sbpmg:\gen_sbpmg_pipeline_less_than_two:sm0:5:sm1		
27	| sld_sbpmg:\gen_sbpmg_pipeline_less_than_two:sm0:6:sm1|	1 (1)	2 (2)	0	0	0	0	|DE1_SoC|sld_signaltap:auto_signaltap_0|sld_signaltap_impl:sld_signaltap_body|sld_signaltap_implb:sld_signaltap_body|sld_ela_control:ela_control|	sld_sbpmg	work

	Compilation Hierarchy Node	Combinational ALUTs	Dedicated Logic Registers	Block Memory Bits	DSP Blocks	Pins	Virtual Pins	Full Hierarchy Name	Entity Name	Library Name
								sld_ela_basic_multi_level_trigger:\basic_multi_level_mbpm_trigger_gen:multi_level_mbpm|sld_mbpmg:\trigger_modules_gen:0:trigger_match|sld_sbpmg:\gen_sbpmg_pipeline_less_than_two:sm0:6:sm1		
28	|sld_sbpmg:\gen_sbpmg_pipeline_less_than_two:sm0:7:sm1|	1 (1)	2 (2)	0	0	0	0	|DE1_SoC|sld_signaltap:auto_signaltap_0|sld_signaltap_impl:sld_signaltap_body|sld_signaltap_implb:sld_signaltap_body|sld_ela_control:ela_control|sld_ela_basic_multi_level_trigger:\basic_multi_level_mbpm_trigger_gen:multi_level_mbpm|sld_mbpmg:\trigger_modules_gen:0:trigger_match|sld_sbpmg:	sld_sbpmg	work

	Compilation Hierarchy Node	Combinational ALUTs	Dedicated Logic Registers	Block Memory Bits	DSP Blocks	Pins	Virtual Pins	Full Hierarchy Name	Entity Name	Library Name
								\gen_sbpmg_pipeline_less_than_two:sm0:7:sm1		
29	| sld_sbpmg:\gen_sbpmg_pipeline_less_than_two:sm0:8:sm1|	1 (1)	2 (2)	0	0	0	0	|DE1_SoC|sld_signaltap:auto_signaltap_0|sld_signaltap_impl:sld_signaltap_body|sld_signaltap_implb:sld_signaltap_body|sld_ela_control:ela_control|sld_ela_basic_multi_level_trigger:\basic_multi_level_mbpm_trigger_gen:multi_level_mbpm|sld_mbpmg:\trigger_modules_gen:0:trigger_match|sld_sbpmg:\gen_sbpmg_pipeline_less_than_two:sm0:8:sm1	sld_sbpmg	work
30	| sld_sbpmg:\gen_sbpmg_pipeline_less_than_two:sm0:9:sm1|	1 (1)	2 (2)	0	0	0	0	|DE1_SoC|sld_signaltap:auto_signaltap_0|sld_signaltap_impl:sld_signaltap_body|sld_signaltap_implb:sld	sld_sbpmg	work

	Compilation Hierarchy Node	Combinational ALUTs	Dedicated Logic Registers	Block Memory Bits	DSP Blocks	Pins	Virtual Pins	Full Hierarchy Name	Entity Name	Library Name
								_signaltap_body|sld_ela_control:ela_control|sld_ela_basic_multi_level_trigger:\basic_multi_level_mbpm_trigger_gen:multi_level_mbpm|sld_mbpmg:\trigger_modules_gen:0:trigger_match|sld_sbpmg:\gen_sbpmg_pipeline_less_than_two:sm0:9:sm1		
3	|sld_ela_trigger_flow_mgr:\builtin:ela_trigger_flow_mgr_entity|	7 (7)	11 (1)	0	0	0	0	|DE1_SoC|sld_signaltap:auto_signaltap_0|sld_signaltap_impl:sld_signaltap_body|sld_signaltap_implb:sld_signaltap_body|sld_ela_control:ela_control|sld_ela_trigger_flow_mgr:\builtin:ela_trigger_flow_mgr_entity	sld_ela_trigger_flow_mgr	work
1	|lpm_shiftreg:trigger_	0 (0)	10 (10)	0	0	0	0	|DE1_SoC|sld_signaltap:auto_signa	lpm_shiftreg	work

	Compilation Hierarchy Node	Combinational ALUTs	Dedicated Logic Registers	Block Memory Bits	DSP Blocks	Pins	Virtual Pins	Full Hierarchy Name	Entity Name	Library Name
	config_deserialize|							ltap_0|sld_signaltap_impl:sld_signaltap_body|sld_signaltap_implb:sld_signaltap_body|sld_ela_control:ela_control|sld_ela_trigger_flow_mgr:\builtin:ela_trigger_flow_mgr_entity|lpm_shiftreg:trigger_config_deserialize		
8	| sld_offload_buffer_mgr:\stp_non_zero_depth_offload_gen:stp_offload_buff_mgr_inst|	36 (11)	77 (0)	0	0	0	0	|DE1_SoC|sld_signaltap:auto_signaltap_0|sld_signaltap_impl:sld_signaltap_body|sld_signaltap_implb:sld_signaltap_body|sld_offload_buffer_mgr:\stp_non_zero_depth_offload_gen:stp_offload_buff_mgr_inst	sld_offload_buffer_mgr	work
1	| lpm_counter:\adv_point_3_and_more:advanc	7 (0)	5 (0)	0	0	0	0	|DE1_SoC|sld_signaltap:auto_signaltap_0|sld_signaltap_impl:sld_s	lpm_counter	work

	Compilation Hierarchy Node	Combinational ALUTs	Dedicated Logic Registers	Block Memory Bits	DSP Blocks	Pins	Virtual Pins	Full Hierarchy Name	Entity Name	Library Name
	e_pointer_counter|							ignaltap_body| sld_signaltap_implb:sld_signaltap_body| sld_offload_buffer_mgr:\stp_non_zero_depth_offload_gen:stp_offload_buff_mgr_inst| lpm_counter:\adv_point_3_and_more:advance_pointer_counter		
1	| cntr_u8i:auto_generated|	7 (7)	5 (5)	0	0	0	0	|DE1_SoC| sld_signaltap:auto_signaltap_0| sld_signaltap_impl:sld_signaltap_body| sld_signaltap_implb:sld_signaltap_body| sld_offload_buffer_mgr:\stp_non_zero_depth_offload_gen:stp_offload_buff_mgr_inst| lpm_counter:\adv_point_3_and_more:advance_pointer_counte	cntr_u8i	work

	Compilation Hierarchy Node	Combinational ALUTs	Dedicated Logic Registers	Block Memory Bits	DSP Blocks	Pins	Virtual Pins	Full Hierarchy Name	Entity Name	Library Name
								r| cntr_u8i:auto_generated		
2	| lpm_counter:read_pointer_counter|	7 (0)	7 (0)	0	0	0	0	|DE1_SoC| sld_signaltap:auto_signaltap_0| sld_signaltap_impl:sld_signaltap_body| sld_signaltap_implb:sld_signaltap_body| sld_offload_buffer_mgr: \stp_non_zero_depth_offload_gen:stp_offload_buff_mgr_inst | lpm_counter:read_pointer_counter	lpm_counter	work
1	| cntr_4vi:auto_generated|	7 (7)	7 (7)	0	0	0	0	|DE1_SoC| sld_signaltap:auto_signaltap_0| sld_signaltap_impl:sld_signaltap_body| sld_signaltap_implb:sld_signaltap_body| sld_offload_buffer_mgr: \stp_non_zero_depth_offload_gen:stp_offload_buff_mgr_inst | lpm_counte	cntr_4vi	work

	Compilation Hierarchy Node	Combinational ALUTs	Dedicated Logic Registers	Block Memory Bits	DSP Blocks	Pins	Virtual Pins	Full Hierarchy Name	Entity Name	Library Name
								r:read_pointer_counter|cntr_4vi:auto_generated		
3	| lpm_counter:status_advance_pointer_counter|	6 (0)	4 (0)	0	0	0	0	|DE1_SoC|sld_signaltap:auto_signaltap_0|sld_signaltap_impl:sld_signaltap_body|sld_signaltap_implb:sld_signaltap_body|sld_offload_buffer_mgr:\stp_non_zero_depth_offload_gen:stp_offload_buff_mgr_inst|lpm_counter:status_advance_pointer_counter	lpm_counter	work
1	| cntr_09i:auto_generated|	6 (6)	4 (4)	0	0	0	0	|DE1_SoC|sld_signaltap:auto_signaltap_0|sld_signaltap_impl:sld_signaltap_body|sld_signaltap_implb:sld_signaltap_body|sld_offload_buffer_mgr:\stp_non_zero_depth_offload_gen:stp_offload_buff_mgr_inst	cntr_09i	work

	Compilation Hierarchy Node	Combinational ALUTs	Dedicated Logic Registers	Block Memory Bits	DSP Blocks	Pins	Virtual Pins	Full Hierarchy Name	Entity Name	Library Name
								| lpm_counter:status_advance_pointer_counter| cntr_09i:auto_generated		
4	| lpm_counter:status_read_pointer_counter|	3 (0)	1 (0)	0	0	0	0	|DE1_SoC| sld_signaltap:auto_signaltap_0| sld_signaltap_impl:sld_signaltap_body| sld_signaltap_implb:sld_signaltap_body| sld_offload_buffer_mgr:\stp_non_zero_depth_offload_gen:stp_offload_buff_mgr_inst| lpm_counter:status_read_pointer_counter	lpm_counter	work
1	| cntr_kri:auto_generated|	3 (3)	1 (1)	0	0	0	0	|DE1_SoC| sld_signaltap:auto_signaltap_0| sld_signaltap_impl:sld_signaltap_body| sld_signaltap_implb:sld_signaltap_body| sld_offload_buffer_mgr:\stp_non_zero_depth_of	cntr_kri	work

	Compilation Hierarchy Node	Combinational ALUTs	Dedicated Logic Registers	Block Memory Bits	DSP Blocks	Pins	Virtual Pins	Full Hierarchy Name	Entity Name	Library Name
								fload_gen:stp_offload_buff_mgr_inst|lpm_counter:status_read_pointer_counter|cntr_kri:auto_generated		
5	|lpm_shiftreg:info_data_shift_out|	0 (0)	15 (15)	0	0	0	0	|DE1_SoC|sld_signaltap:auto_signaltap_0|sld_signaltap_impl:sld_signaltap_body|sld_signaltap_implb:sld_signaltap_body|sld_offload_buffer_mgr:\stp_non_zero_depth_offload_gen:stp_offload_buff_mgr_inst|lpm_shiftreg:info_data_shift_out	lpm_shiftreg	work
6	|lpm_shiftreg:ram_data_shift_out|	1 (1)	30 (30)	0	0	0	0	|DE1_SoC|sld_signaltap:auto_signaltap_0|sld_signaltap_impl:sld_signaltap_body|sld_signaltap_implb:sld_signaltap_body|sld_offload_buffer_mgr:	lpm_shiftreg	work

	Compilation Hierarchy Node	Combinational ALUTs	Dedicated Logic Registers	Block Memory Bits	DSP Blocks	Pins	Virtual Pins	Full Hierarchy Name	Entity Name	Library Name
								\stp_non_zero_depth_offload_gen:stp_offload_buff_mgr_inst|lpm_shiftreg:ram_data_shift_out		
7	|lpm_shiftreg:status_data_shift_out|	1 (1)	15 (15)	0	0	0	0	|DE1_SoC|sld_signaltap:auto_signaltap_0|sld_signaltap_impl:sld_signaltap_body|sld_signaltap_implb:sld_signaltap_body|sld_offload_buffer_mgr:\stp_non_zero_depth_offload_gen:stp_offload_buff_mgr_inst|lpm_shiftreg:status_data_shift_out	lpm_shiftreg	work
9	|sld_rom_sr:crc_rom_sr|	20 (20)	8 (8)	0	0	0	0	|DE1_SoC|sld_signaltap:auto_signaltap_0|sld_signaltap_impl:sld_signaltap_body|sld_signaltap_implb:sld_signaltap_body|sld_rom_sr:crc_rom_sr	sld_rom_sr	work
14	|	103 (103)	171 (171)	0	0	0	0	|DE1_SoC|	update_scre	work

	Compilation Hierarchy Node	Combinational ALUTs	Dedicated Logic Registers	Block Memory Bits	DSP Blocks	Pins	Virtual Pins	Full Hierarchy Name	Entity Name	Library Name
	update_screen:su|							update_screen:su	en	
15	|video_driver:v1|	118 (74)	98 (49)	0	0	0	0	|DE1_SoC|video_driver:v1	video_driver	work
1	|CLOCK25_PLL:c25_gen|	0 (0)	0 (0)	0	0	0	0	|DE1_SoC|video_driver:v1|CLOCK25_PLL:c25_gen	CLOCK25_PLL	CLOCK25_PLL
1	|CLOCK25_PLL_0002:clock25_pll_inst|	0 (0)	0 (0)	0	0	0	0	|DE1_SoC|video_driver:v1|CLOCK25_PLL:c25_gen|CLOCK25_PLL_0002:clock25_pll_inst	CLOCK25_PLL_0002	CLOCK25_PLL
1	|altera_pll:altera_pll_i|	0 (0)	0 (0)	0	0	0	0	|DE1_SoC|video_driver:v1|CLOCK25_PLL:c25_gen|CLOCK25_PLL_0002:clock25_pll_inst|altera_pll:altera_pll_i	altera_pll	work
2	|altera_up_avalon_video_vga_timing:video|	44 (44)	49 (49)	0	0	0	0	|DE1_SoC|video_driver:v1|altera_up_avalon_video_vga_timing:video	altera_up_avalon_video_vga_timing	work