
Notes:

- The main purpose of this week is to analyse the operations of a MIPS processor.
- Students are NOT requested to submit anything.

Given the following single cycle MIPS processor architecture.

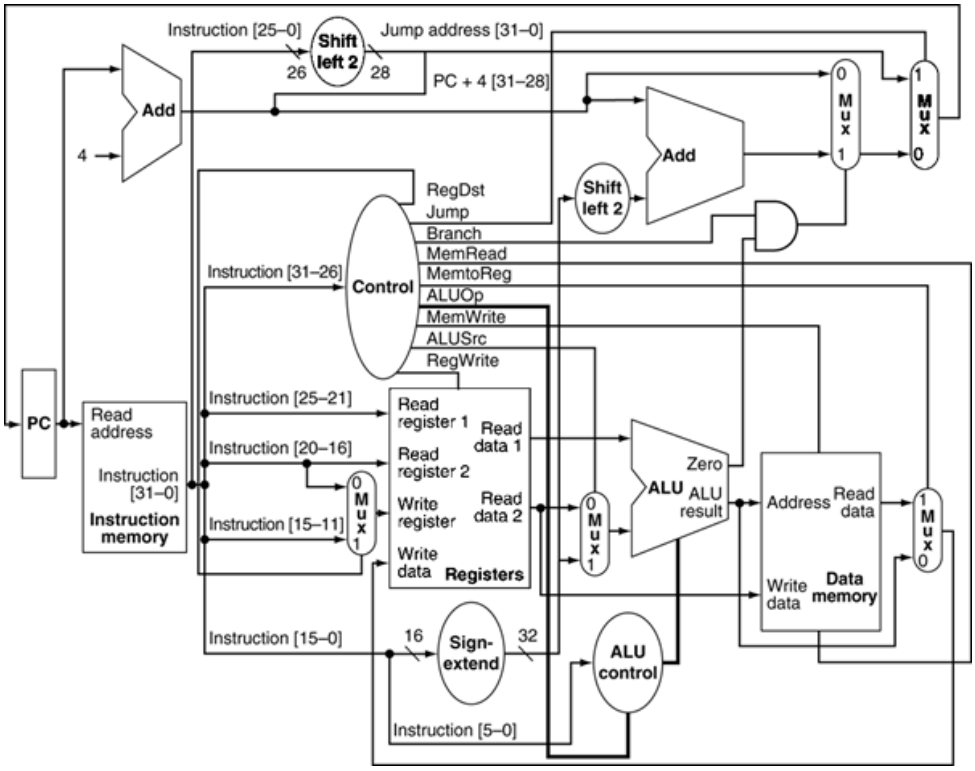

Figure 1: Full datapath of a single cycle MIPS processor

Assume that `$s0` and `$s1` registers store two integer numbers 100 and 200, respectively. The memory word at address 300 keeps an integer number 2019.

Question 1. With each instruction below, please identify which functional units will participate into the processing of the instruction. What are values of the inputs and outputs of those functional units? Identify values of control signals for each instruction.

1. `add $s0, $s0, $s1`
2. `addi $s1, $s0, 5`
3. `lw $s0, 100($s1)`
4. `sw $s0, 100($s1)`
5. `beq $s0, $s1, L1`

Functional unit	Execution time
Mux	10ns
Add	10ns
Shift left	10ns
Instruction memory	150ns
Registers	150ns
Sign extend	10ns
ALU	150ns
Data memory	200ns

Table 1: Execution time for functional units

Question 2. Table 1 shows execution time of each functional unit in the MIPS single cycle processor. Calculate execution time of following instructions:

1. `add $s0, $s0, $s1`
2. `addi $s1, $s0, 5`
3. `lw $s0, 100($s1)`
4. `sw $s0, 100($s1)`
5. `beq $s0, $s1, L1`

Then, calculate the cycle time for this processor.

——————the end——————