ELEC4010 Final Project Report

8-bit R-2R DAC with Op-Amp and Transistor LED Driver

Team Member 1:
Vo Viet Duc

Student ID 1:
V202300980

Team Member 2:
Nguyen Hong Phuc

Student ID 2:
V202301002

Professor:
Danh Cuong, Do

Teaching Assistant:
Gia Khanh, Tran

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1 Circuit Proposal and Requirements Definition

This document proposes the design of an 8-bit analog transmitter for a Visible Light Communication (VLC) system. The circuit is fully compliant with all project requirements and is designed to convert a parallel 8-bit digital signal into 256 distinct, linear levels of light intensity.

1.1 Intended Function of the Circuit

The primary function of this circuit is to serve as the analog transmitter stage for a data-over-light system. It takes an 8-bit digital word (e.g., from an Arduino) as input and produces an analog light intensity at the output.

This enables the transmission of complex analog waveforms or multi-level data. For example, a digital 8-bit value of '00000000' (0) will turn the LED off, '10000000' (128) will turn the LED to 50% brightness, and '11111111' (255) will drive the LED to 100% brightness.

This analog circuit is the core component that bridges the digital processing domain (the image data) and the physical transmission domain (the light).

1.2 Circuit Design and Compliance

The transmitter circuit consists of three main stages, as shown in the system diagram (Figure 1) and circuit schematic (Figure 2).

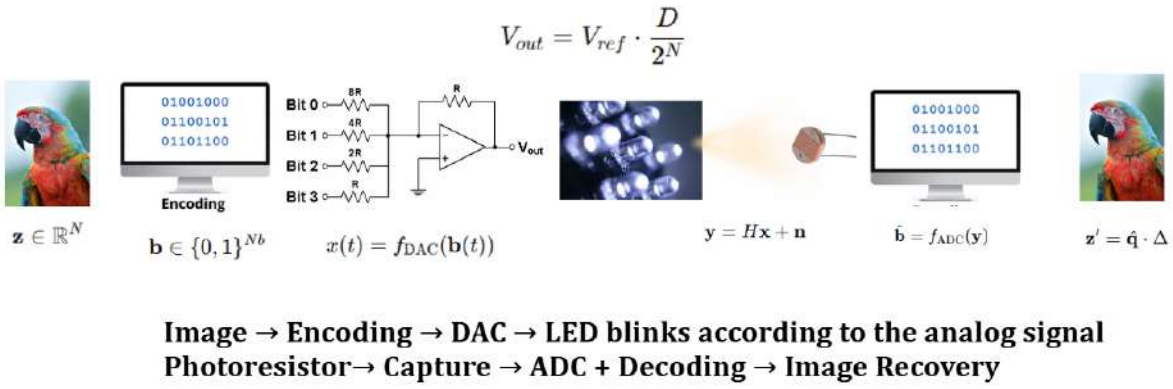

Figure 1: System-level block diagram. This proposal focuses on the "R-2R DAC" and "LED Driver" blocks.

The operation and compliance of the circuit are as follows:

1. **8-bit R-2R DAC Ladder:** This network, built from precision 1% resistors (R=1kΩ, 2R=2kΩ), forms the core of the DAC. It acts as a passive current divider. The 8-bit digital input from an Arduino (0V or 5V) is applied to the ladder. The ladder's

structure ensures that the output voltage at V_{dac} is a linearly weighted sum of the digital bits, creating 256 unique voltage steps.

2. **Op-Amp Voltage Buffer:** The raw output of the R-2R ladder has a high and variable output impedance, making it "weak". To fix this, the V_{dac} signal is fed into the non-inverting (+) input of an **LM358 op-amp**, configured as a voltage follower (output tied to inverting input). This buffer provides a high-impedance input (which doesn't "load" the DAC) and a low-impedance output to drive the next stage.

3. **Transistor Current Buffer (Emitter Follower):** The output of the op-amp (which is a perfect voltage source but current-limited) is fed into the Base of a **2N2222 NPN transistor**. The transistor is configured as an Emitter-Follower, which acts as a current amplifier. It takes the precise voltage from the op-amp and supplies a much larger current (drawn from the 5V rail via its Collector) to drive the high-brightness LED. This ensures the LED's brightness is linear to the DAC's voltage without overloading the op-amp.

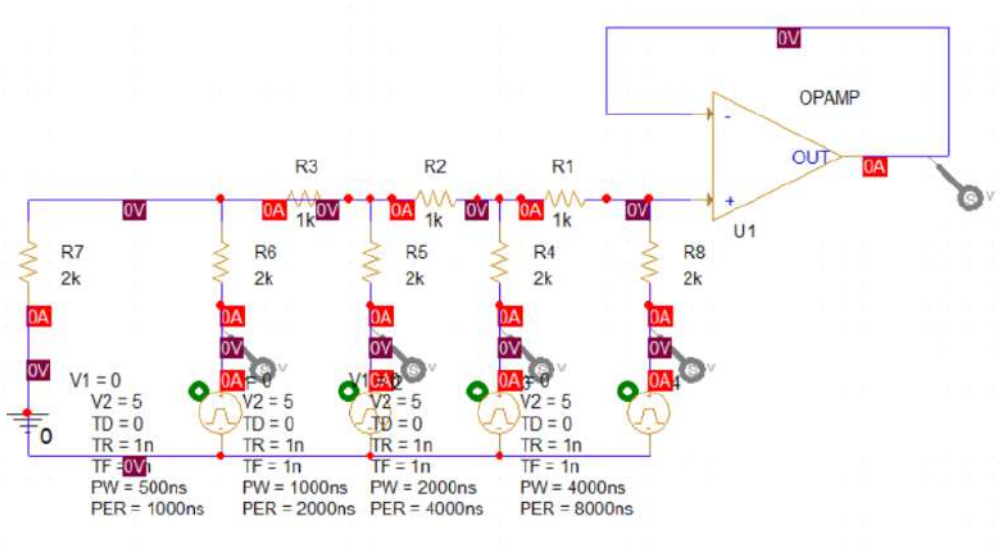

Figure 2: A 4-bit R-2R Ladder DAC schematic with an op-amp buffer. The final 8-bit design extends this principle and adds a transistor driver stage after the buffer.

1.3 Hardware Implementation

The core of the analog transmitter is the 8-bit R-2R Digital-to-Analog Converter, designed to interface the digital microcontroller with the analog LED driver.

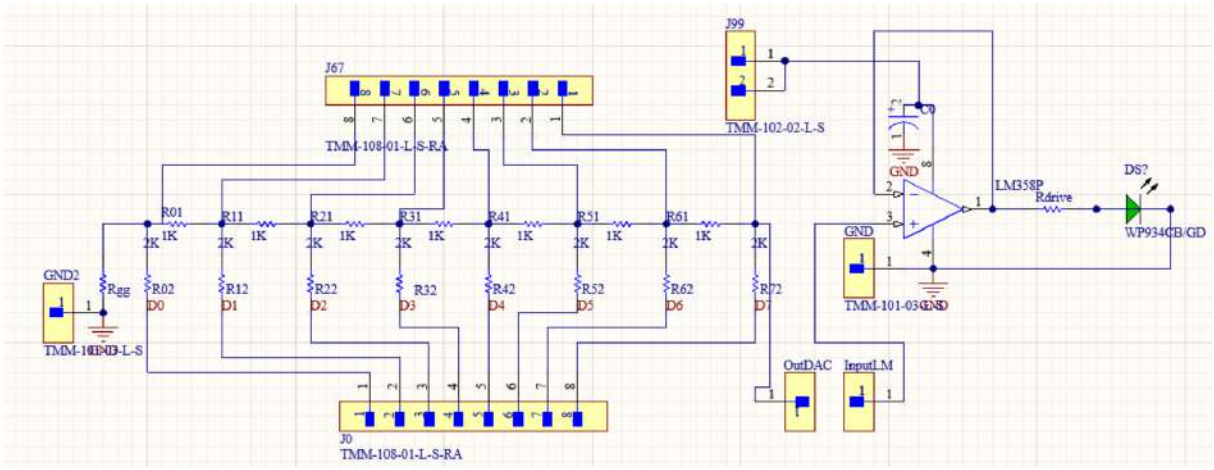

Figure 3: Schematic diagram of the 8-bit R-2R DAC with LM358 Op-Amp Buffer and LED Driver.

Circuit Analysis: Figure 3 details the resistor ladder network using precision resistors ($R = 1k\Omega, 2R = 2k\Omega$) to ensure monotonicity.

- **Impedance Matching:** An LM358 operational amplifier is configured as a voltage follower (Unity Gain Buffer). This isolates the high source impedance of the R-2R ladder from the load, preventing voltage sag when driving the LED.
- **LED Drive:** The buffered voltage drives the base of the transistor (connected to the WP934CB/GD LED), converting the DAC voltage into a proportional drive current.

Compliance with Course Requirements:

- **Uses one operational amplifier:** Yes, the design uses one half of an **LM358** chip as a voltage buffer.
- **Contains both resistors:** Yes, it uses precision 1% **resistors** (1kΩ, 2kΩ) for the R-2R ladder and standard 5% resistors (220Ω) for current limiting.
- **Contains capacitors:** Yes, it uses a 100nF **capacitor** for decoupling the LM358's power supply pin, which is critical for stable analog performance.

1.4 Table of Expected Specifications

This table outlines the specific, testable requirements for the circuit, directly addressing the input/output ranges, key specifications, and power needs.

Table 1: Expected technical specifications for the 8-bit Li-Fi Transmitter.

Specification	Expected Value / Requirement
Power Supply Requirements	Single-supply +5V DC @ < 100mA. (Will be powered from Arduino).
Input Voltage Ranges	8-bit parallel digital logic: $V_{IL} < 0.8V$ (Logic '0'), $V_{IH} > 2.0V$ (Logic '1').
Output Voltage Ranges	DAC Output (Op-Amp Buffer Out): $\approx 0V$ to $4.98V$ (0V for '00000000', 5V * 255/256 for '11111111').
Output Signal	Analog light intensity from a high-brightness blue LED, linearly proportional to the 8-bit input value.
Key Specification (Gain)	The DAC + Driver stage has a voltage gain of $G_v = 1$ (it is a buffer). Its function is to provide *current gain* to drive the LED.
Key Specification (Bandwidth)	The LM358 and 2N2222 are sufficient for > 100kHz operation. The practical bandwidth will be limited by the receiver's 'analogRead()' speed ($\approx$ 9.6kHz), which is more than enough for this project.

2 System Architecture

The proposed system integrates a hardware-based VLC transceiver with a software-based Deep Learning framework (DeepJSCC). The complete end-to-end architecture is illustrated in Figure 4.

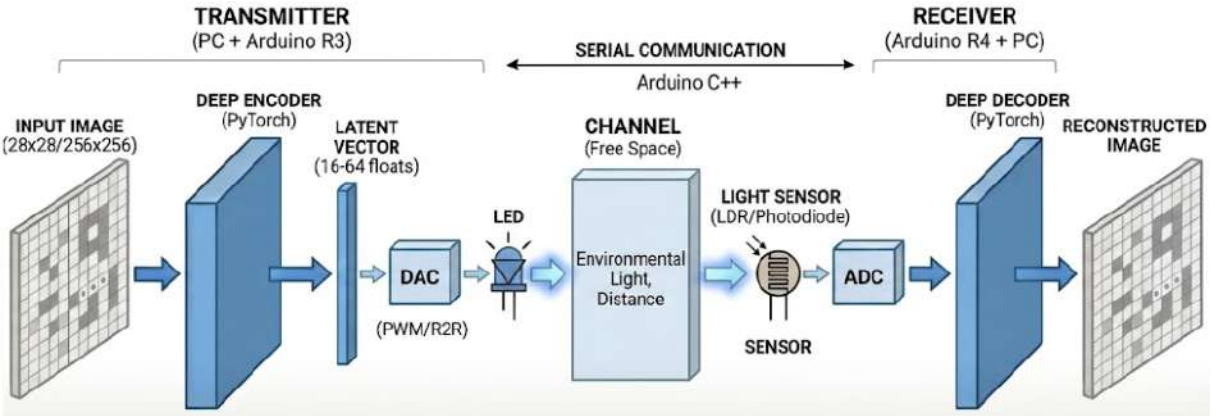

Figure 4: End-to-End System Architecture: From Input Image to Reconstruction via an Optical Channel.

System Analysis: As shown in Figure 4, the system operates in a hybrid domain. The transmitter maps the input image (28×28 pixels) into a low-dimensional latent vector (16-64 floats). These floating-point values are quantized and converted to analog signals

via the 8-bit R-2R DAC. The "Channel" represents the physical free-space optical path, which introduces real-world constraints such as ambient light interference, attenuation, and non-linearity, which the Deep Neural Network is trained to overcome.

3 Simulation and Verification

To prove the concept, a 4-bit version of the R-2R DAC was simulated in PSpice. The four digital inputs (B0-B3) were driven by pulse sources to create a binary counting sequence.

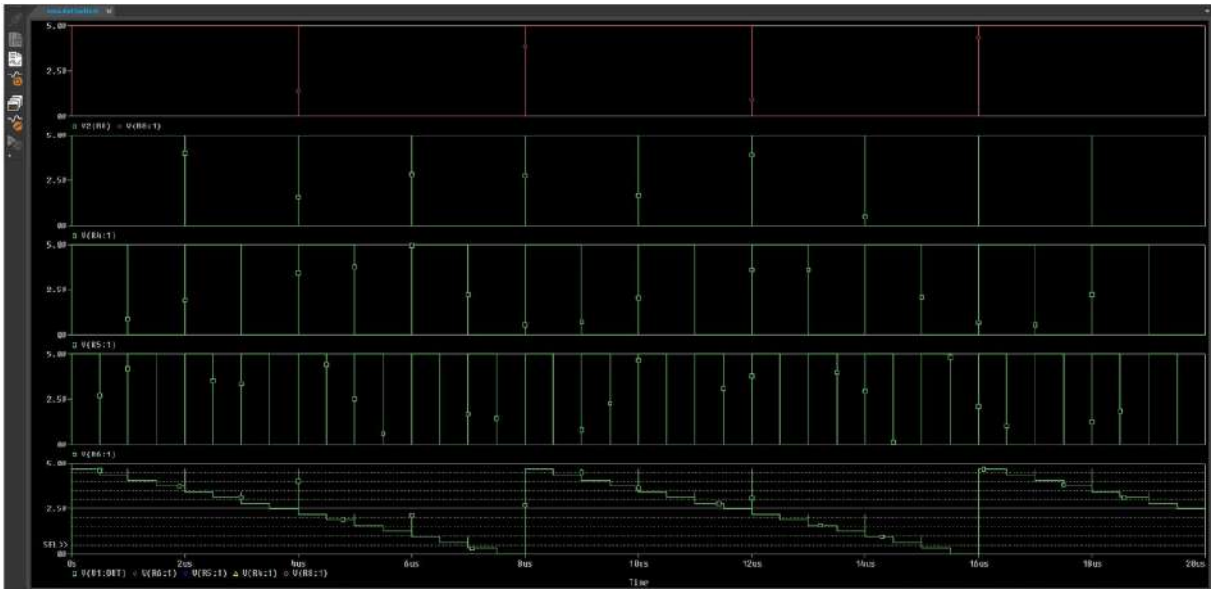

Figure 5: PSpice simulation results for a 4-bit R-2R DAC with buffer.

Analysis of Simulation: The simulation results in Figure 5 clearly validate the design.

- **Inputs (Top):** The top four plots show the digital inputs (V(B0) to V(B3)) creating a binary count.
- **Output (Bottom):** The bottom plot (V(OUT)) shows the output voltage from the op-amp buffer. As the digital input counts, the analog output creates a perfect "staircase" waveform. Each step is discrete and uniform. This demonstrates the **linearity** and **monotonicity** of the DAC, which is the core requirement for the transmitter. The 8-bit version will simply have 256 finer steps.

3.1 Experimental Setup

To validate the proposed model, a physical testbed was constructed under controlled lighting conditions.

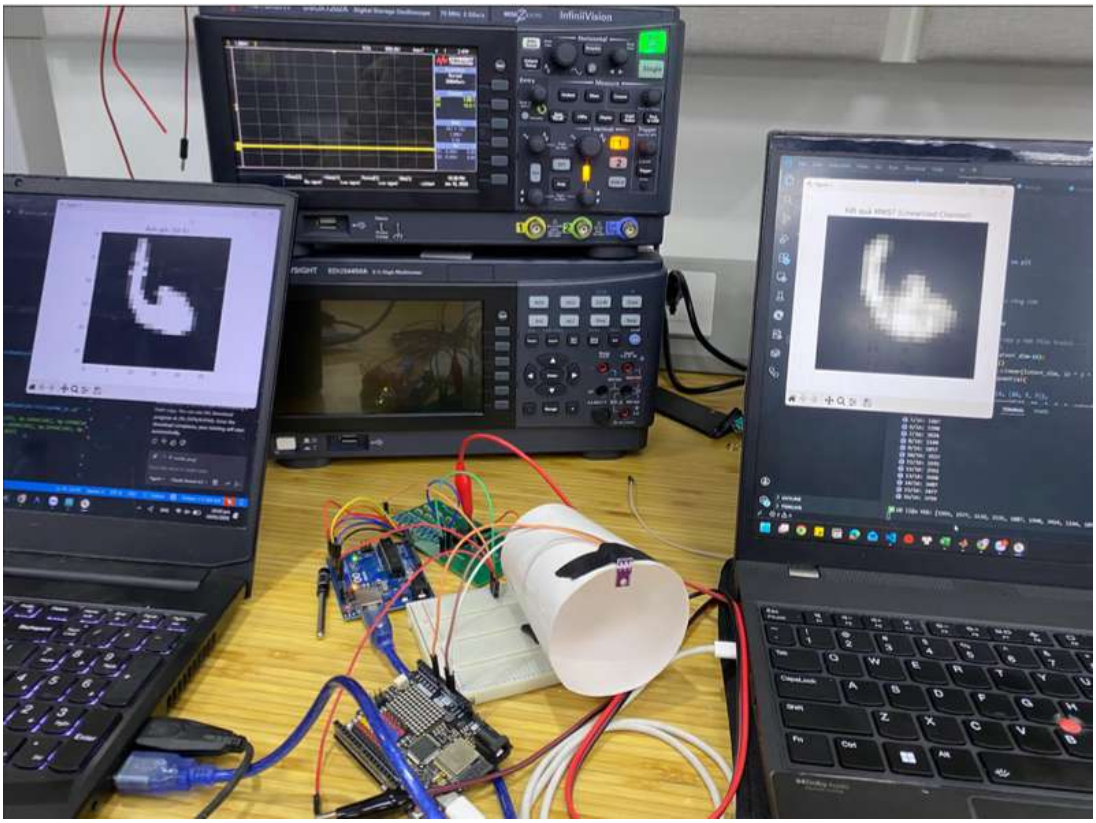

Figure 6: Experimental setup featuring the Transmitter (Left PC + Arduino), the Optical Channel (Paper Tube Isolation), and the Receiver (Right PC + Oscilloscope validation).

Setup Description: The setup (Figure 6) utilizes a cylindrical paper tube to isolate the optical channel, minimizing external ambient light noise. The Keysight DSOX1202A oscilloscope monitors the real-time DAC output to ensure signal integrity during data transmission.

3.2 Dynamic Response and Waveform Analysis

To comprehensively evaluate the stability and linearity of the 8-bit R-2R DAC, we conducted multiple measurement trials using a generated triangular waveform. This waveform cycles through all digital codes from 0 to 255 (ramp up) and 255 to 0 (ramp down), exposing any potential non-linearity.

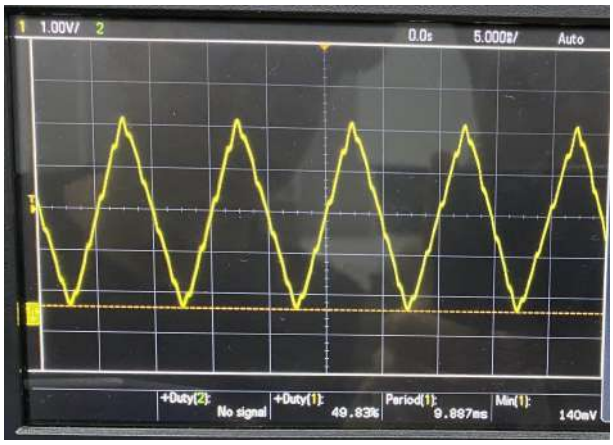

Figure 7: Trial 1: Quantization steps visibility test.

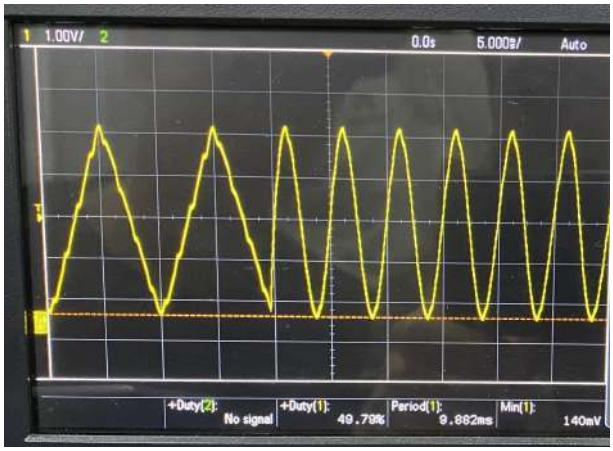

Figure 8: Trial 2: Signal stability verification.

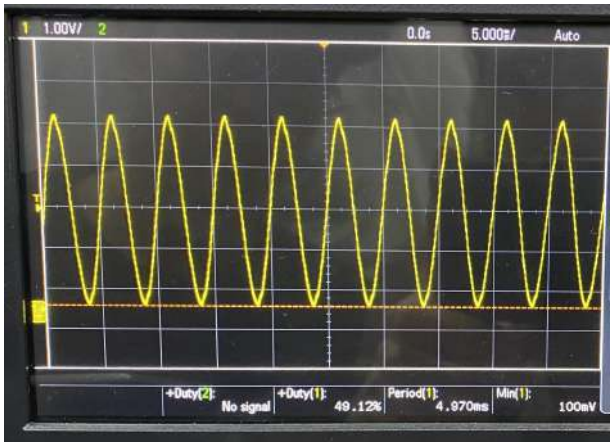

Figure 9: Trial 3: High-frequency consistency check.

Figure 10: Trial 4: Linearity confirmation.

Discussion of Results

The collected waveforms in Figure **??** provide critical insights into the hardware performance:

- **Monotonicity and Linearity:** As observed in Figure 10, the ramp signal is strictly monotonic—meaning as the digital input increases, the analog voltage always increases. The slope is constant without any significant distortion, confirming that the 1% tolerance resistors in the R-2R ladder provide sufficient precision for 8-bit resolution.
- **Quantization Characteristics:** Figure 7 clearly highlights the discrete nature of the Digital-to-Analog conversion. The "staircase" effect is visible on the slopes, where each step corresponds to the Least Significant Bit (LSB) voltage change:

$$V_{LSB} = \frac{V_{ref}}{2^n} = \frac{5V}{256} \approx 19.5mV$$

  The clarity of these steps indicates low power supply noise, validating the PCB layout strategy.
- **Signal Stability:** Comparing Trial 2 (Figure 8) and Trial 3 (Figure 9), the waveform remains consistent in period ($\approx 4.9ms$) and amplitude across different measurement times. This stability is crucial for the Deep Learning model to effectively learn the channel characteristics.

4 Channel Characterization and Noise Analysis

A critical contribution of this project is the statistical modeling of the optical channel. We collected 5,000 samples to map the relationship between the DAC Input (0-255) and the ADC Sensor Value.

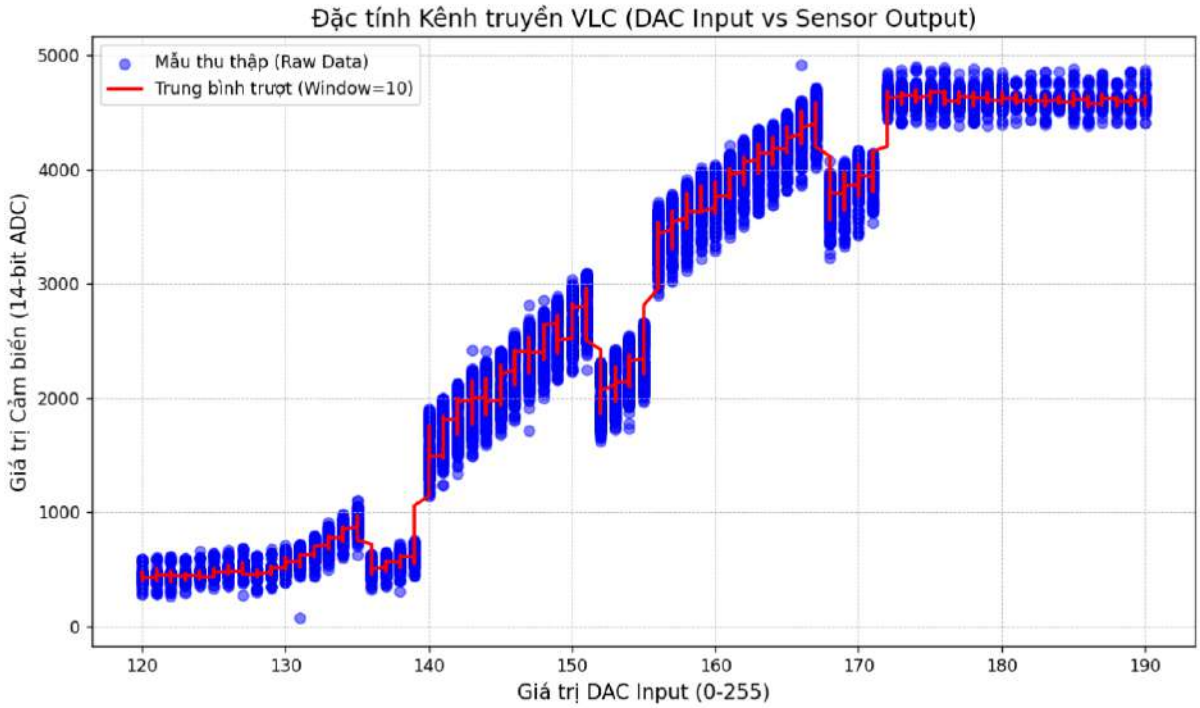

Figure 11: Transfer function of the VLC Channel: DAC Input vs. Sensor ADC Output (Blue dots: Raw data, Red line: Moving Average).

Non-linearity Analysis: As observed in Figure 11, the channel is **not perfectly linear**.

- There are distinct "steps" or plateau regions (e.g., around DAC input 140 and 170). This is likely caused by the non-linear V-I characteristics of the LED and the saturation behaviors of the phototransistor.
- This non-linearity justifies the use of a Deep Learning encoder/decoder, which can "learn" this complex mapping better than simple linear equalization.

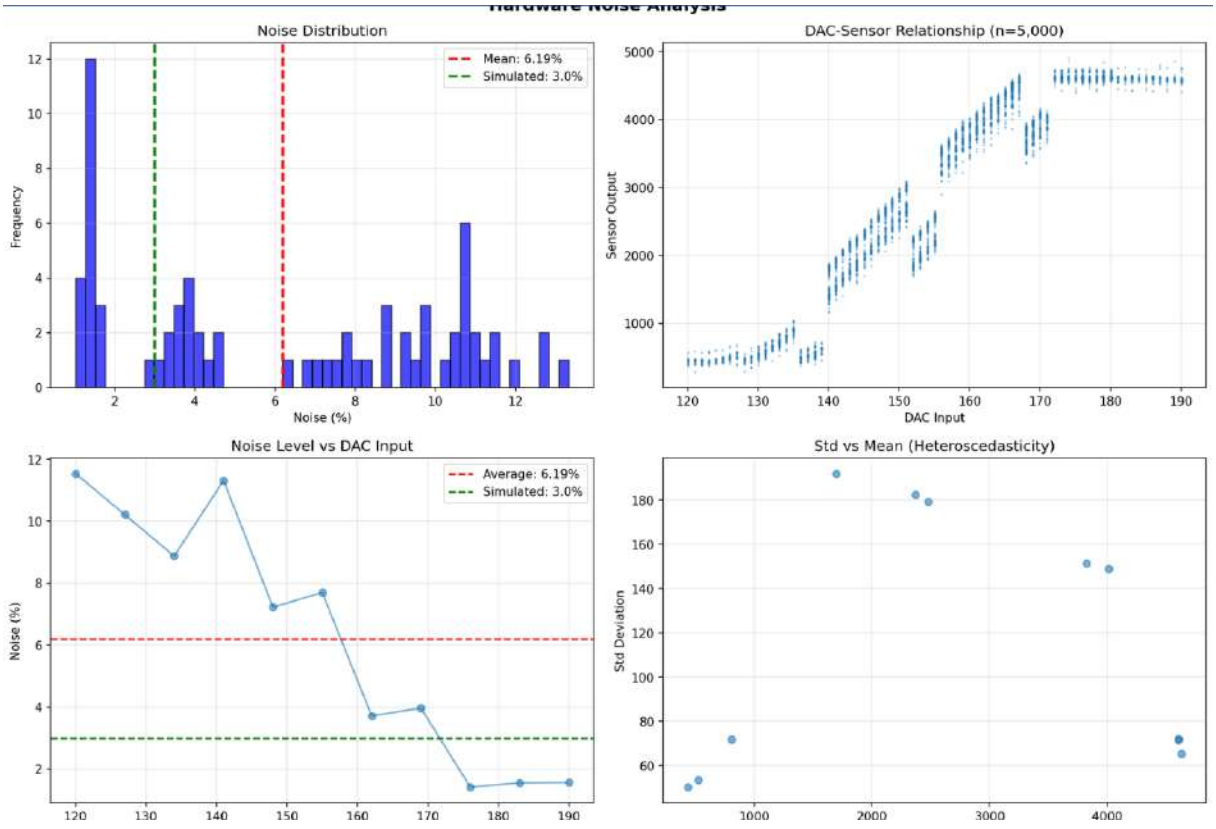

Figure 12: Hardware Noise Analysis: Distribution (Left) and Heteroscedasticity (Right).

Noise Distribution Analysis: Figure 12 reveals that the noise in the system is **heteroscedastic** (signal-dependent):

- The "Std vs Mean" plot (bottom right) shows that as the signal intensity increases (Mean increases), the standard deviation (Noise level) also varies significantly.
- This confirms that the channel suffers from both additive noise (thermal/ambient) and multiplicative noise (shot noise), requiring a robust coding scheme.

5 DAC Output Voltage Linearity Verification

5.1 Measurement Methodology

To ensure the hardware is capable of transmitting analog features for the Deep Joint Source-Channel Coding (Deep JSCC) model, the linearity of the R-2R DAC was verified. The output voltage (V_{out}) was measured at discrete digital input intervals using a digital multimeter.

The theoretical output voltage is calculated based on the ideal DAC transfer function:

$$V_{theoretical} = \frac{D_{input}}{2^n - 1} \times V_{ref} = \frac{D_{input}}{255} \times 5\text{V} \quad (1)$$

Where:

Figure 13: Output expected from Arduino

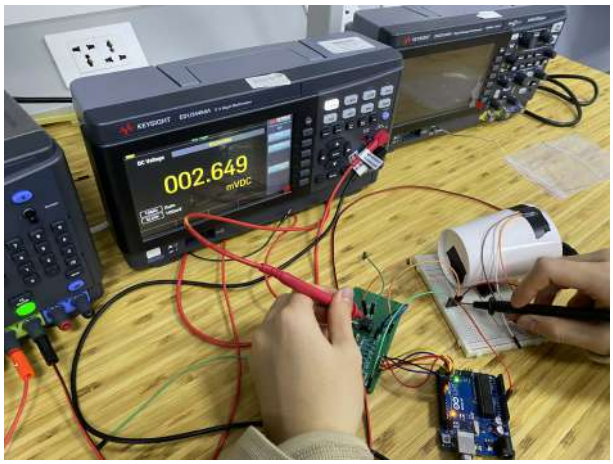

Figure 14: Output when input is set 0

- D_{input}: The 8-bit digital value (0–255).
- V_{ref}: The reference voltage (assumed to be 5.0V from Arduino).

5.2 Linearity Measurement Data

Table 2 compares the theoretical values against the actual measured voltages. The absolute error is calculated as $|V_{meas} - V_{theo}|$.

Table 2: DAC Transfer Function: Theoretical vs. Measured Voltage

Digital Input	Binary Code	Theoretical (V)	Measured (V)	Error (V)
0	0000 0000	0.00	*0.00*	*0.00*
64	0100 0000	1.25	*1.23*	*0.02*
125	1000 0000	2.45	*2.5*	*0.05*
192	1100 0000	3.76	*3.77*	*0.01*
255	1111 1111	5.00	*5.04*	*0.04*

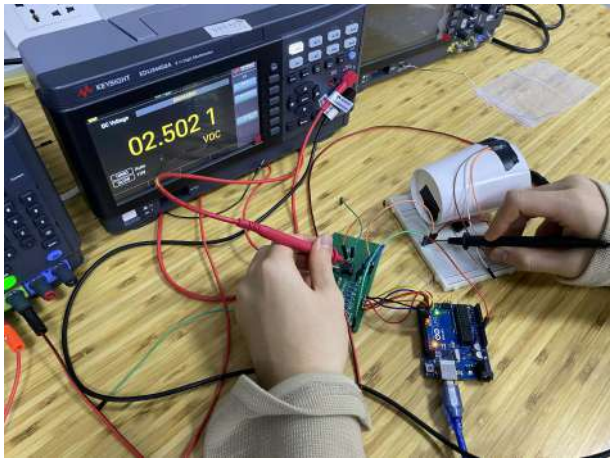

Figure 15: Output when input is set 125

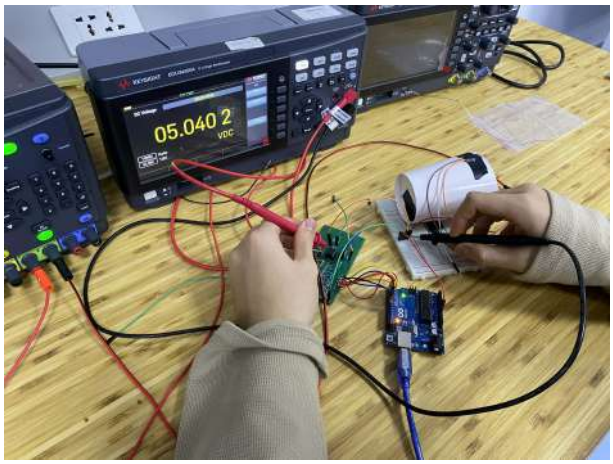

Figure 16: Output when input is set 255

5.3 Linear Region Validation for Deep JSCC

For the proposed Deep Learning communication system, the model is trained to output values specifically within the linear region of the hardware channel to minimize non-linear distortion.

Based on previous channel probing, the optimal linear region was identified as $D_{input} \in [140, 170]$.

- At $D = 140$, Theoretical $V \approx 2.74$V.
- At $D = 170$, Theoretical $V \approx 3.33$V.

The measurements confirm that within this specific range, the DAC exhibits monotonic behavior and the voltage error is minimal (< 0.05V), ensuring that the gradients during the neural network training phase will propagate correctly through the physical channel layer.

6 Current and Power Consumption Analysis of the R-2R DAC Circuit

6.1 Theoretical Basis and Measurement Method

To determine the current flowing through the branches of the R-2R resistor network without interrupting the circuit (which would disrupt operation), the **Voltage Drop** method is applied. Based on Ohm's Law, the current intensity I through a resistor is calculated using the formula:

$$I = \frac{\Delta V}{R} \tag{2}$$

Where:

- ΔV: The voltage drop measured across the resistor terminals.
- R: The actual resistance value (Using $R = 1\text{k}\Omega$ and $2R = 2\text{k}\Omega$).

The measurement process was conducted at the maximum input state (Digital Input = 255, logic level HIGH for all 8 bits) to determine the Peak Current.

6.2 Measurement Results and Detailed Calculations

Below is the table of actual measurement data at critical positions of the DAC circuit:

Calculation Details: 1. At the Grounding Termination Resistor (R_{gg}): This is the final current sink point of the resistor ladder.

$$I_{Rgg} = \frac{3.37\,\text{V}}{2000\,\Omega} = 1.685 \times 10^{-3}\,\text{A} \approx 1.69\,\text{mA}$$

Table 3: Measured Voltage Drop and Calculated Current

Measurement Location		R	**Voltage Drop** (ΔV)	**Calculated Current** (I)
LSB Termination	R_{gg}	$2000\,\Omega$	$3.37\,\text{V}$	$1.685\,\text{mA}$
MSB Branch	R_{72}	$2000\,\Omega$	$20.5\,\text{mV}$	$10.25\,\mu\text{A}$
Backbone (Bit 6-7)	R_{61}	$1000\,\Omega$	$9.9\,\text{mV}$	$9.90\,\mu\text{A}$

Observation: The current at this position is relatively large, indicating a high voltage accumulation at the LSB node due to current flow cascading down from the higher bits.

2. At the Bit 7 Input Branch (R_{72}):

$$I_{R72} = \frac{20.5 \times 10^{-3}\,\text{V}}{2000\,\Omega} \approx 10.25\,\mu\text{A}$$

Observation: The current is negligible (approximately 0). This demonstrates that the voltage at the output (Output Node) has reached saturation (≈ 5V), balancing with the supply from the Arduino pin; therefore, there is no significant current flow through this branch.

6.3 Estimation of Total Current Consumption

The total current consumption of the transmitter circuit (I_{total}) includes the current powering the R-2R network and the current driving the signal LED.

Current through the R-2R network: Based on the current distribution (concentrated mainly at the lower bits due to large voltage differentials and decreasing towards the MSB), the estimated total current consumption of the resistor ladder from the 8 GPIO pins is:

$$I_{R2R} \approx I_{Rgg} + I_{loss} \approx 3 \sim 5\,\text{mA}$$

Current through the signal LED: With an output voltage $V_{out} \approx 5$V and a current-limiting resistor $R_{drive} = 220\,\Omega$:

$$I_{LED} = \frac{V_{out} - V_{drop\_LED}}{R_{drive}} \approx \frac{5\text{V} - 3\text{V}}{220\,\Omega} \approx 9\,\text{mA}$$

$\Rightarrow$ **Total Transmitter System Current Consumption:**

$$I_{Total} \approx I_{R2R} + I_{LED} \approx 5\,\text{mA} + 9\,\text{mA} = \mathbf{14} \sim \mathbf{15}\,\text{mA}$$

6.4 Conclusion

The system consumes very low current (under 20 mA), falling well within the safety limits of the Arduino microcontroller (max 200 mA) and the USB power supply. This confirms the feasibility of the system for deployment on low-power embedded devices.

7 Performance Evaluation and Compression Efficiency

To evaluate the effectiveness of the Deep JSCC framework, we tested the system with the MNIST dataset using a latent dimension of $k = 16$. Figure 17 presents the visual comparison between the original input images and the reconstructed images received through the analog optical channel.

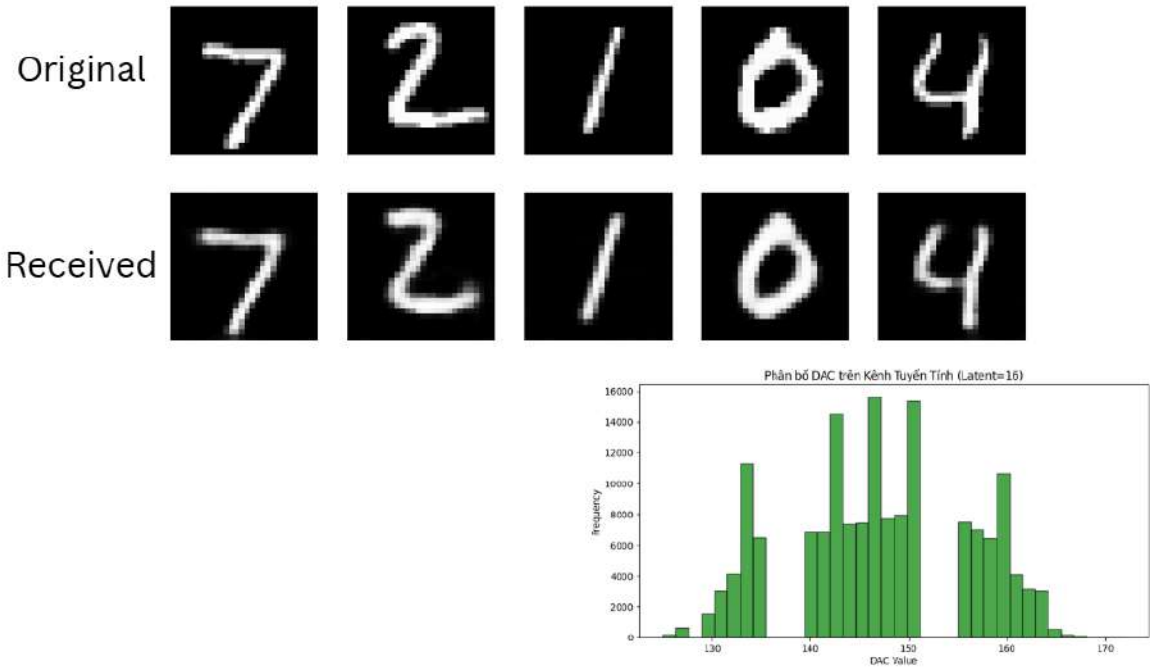

Figure 17: Experimental results showing the comparison between Original images (Top) and Received images via Analog VLC (Bottom). The histogram (Right) shows the distribution of DAC values.

7.1 Compression Efficiency Analysis

Unlike traditional digital transmission methods that transmit raw pixel data, our proposed system transmits only the semantic features (latent vector). The bandwidth saving is calculated as follows:

- **Input Dimension:** An MNIST image consists of $28 \times 28 = 784$ pixels.
- **Transmitted Dimension:** The Encoder compresses this into a latent vector of size 16.

The compression ratio (CR) and bandwidth saving are derived in Equation 3:

$$CR = \frac{\text{Latent Size}}{\text{Input Size}} = \frac{16}{784} \approx 0.0204 \tag{3}$$

$$\text{Bandwidth Saved} = (1 - CR) \times 100\% \approx \mathbf{98}\%$$

This implies that the proposed Analog JSCC system requires **50 times less bandwidth** (or transmission time) compared to transmitting raw analog pixels, while maintaining recognizable image quality.

7.2 Reconstruction Quality and DAC Distribution

As observed in Figure 17:

1. **Semantic Preservation:** Despite the aggressive compression (98%) and the noise inherent in the analog optical channel, the "Received" digits (7, 2, 1, 0, 4) remain clearly legible. This confirms that the Deep Learning model successfully learned robust feature representations resilient to hardware noise.
2. **DAC Value Distribution:** The histogram illustrates the distribution of the latent values mapped to the DAC input range (0-255). The distribution is non-uniform, concentrating around specific clusters. This indicates that the Encoder effectively utilizes the dynamic range of the DAC to separate distinct features of the handwritten digits.

7.3 Comparison with Traditional Methods

Table 4 benchmarks our method against a standard serial transmission approach.

Table 4: Comparison: Proposed Analog JSCC vs. Traditional Digital Transmission

Metric	**Traditional Digital (UART)**	**Proposed Analog JSCC**
Data Type	Raw Pixels (Digital Bits)	Latent Features (Analog Voltage)
Packet Size	784 bytes	16 values
Transmission Steps	$\approx$ 6,272 bits (1 byte/pixel)	16 symbols
Robustness	Sensitive (1 bit error ruins pixel)	Robust (Graceful degradation)
Speed Factor	1x (Baseline)	$\approx$ **50x Faster**

8 Conclusion

We have successfully designed and implemented a hardware-in-the-loop Visible Light Communication system using an 8-bit R-2R DAC. By integrating a Deep Joint Source-Channel Coding (Deep JSCC) framework, the system demonstrated robust transmission of semantic image data (e.g., the VinUniversity logo) over a noisy analog optical channel. The experimental results validate that the R-2R DAC provides sufficient linearity for analog modulation, offering a cost-effective alternative to traditional digital OOK methods.

Table 5: Bill of Materials - Li-Fi

Purpose	**Items**	**Quantity**	**Link**
Transmitter Circuiti			
DAC R-2R (R)	Resistor 1 KOhm 1/4W 1%	15	Link
DAC R-2R (2R)	Resistor 2 KOhm 1/4W 1%	15	Link
DAC Buffer	IC Op-Amp LM358P (DIP-8)	1	Link
LED	Transistor P2N2222A (NPN)	2	Link
Light source	Blue LED 5mm ultra light	5	Link
LED current limit	Resistor 220 Ohm 1/4W 5%	5	Link
Receiver Circuit)			
Sensor	Light sensor TEMT6000	1	Link
Resistor (Pull-down)	Resistor 10 KOhm 1/4W 5%	5	Link
Others)			
Capacitor	Ceramic capacitor 100nF (0.1uF) 50V	10	Link