Assignment II – Cache Design

Please design an experiment (using the cache simulator) for studying the factors that affects the performance of cache accesses. We will address traces from gcc_ld_trace.txt or go_ld_trace.txt as benchmarks. Please fill your results and plot graph of each table. In particular, what does the results suggest about the design of cache.

a. Block Size Tradeoff on direct mapped cache

	Direct mapped			
Block Size (Bytes)	Cache Size (KB)			
	4	8	16	32
4				
8				
16				
32				

b. N-way associative cache with replacement algorithms: Least recently used (LRU), and Round Robin (RR).

	Associativity			
Cache Size (KB)	Two-way		Four-way	
	LRU	RR	LRU	RR
1				
4				
8				
32				
512				
1024				

Note that simulation code and traces can be downloaded from
https://www.cp.eng.chula.ac.th/~krerk/books/Computer%20Architecture/CacheSim