

# 5.4-GHz Low Noise Amplifier: Design and Simulation

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**Abstract**—Nowadays, due to the noticeable development of IoT, wireless sensors have been increasingly improved to achieve both of low power consumption and wide broadcast range. This leads to challenges in power amplifier design. In this article, we propose a method to design a 5.4-GHz Low Noise Amplifier using S-parameters. Concretely, we use a cascade configuration of two transistors to enhance the internal gain. Besides, we also design an input matching alongside with an output matching circuit in order to minimize the amplifier's noise figure as well as maximize the power delivered on the load. The simulation results show that our Low Noise Amplifier is able to reach a spectacular results with 30 dB of transducer gain and 1.99 dB of noise figure. As a result, this model is theoretically reasonable to a Low Noise Amplifier.

**Keyword**— Microwave engineering, Low noise amplifier, S-parameter

## I. INTRODUCTION

Nowadays, thanks to the growth of technology, life is likely to become easier and more convenient. Indeed, under the 4th Industrial Revolution, a huge amount of sensors have been designed and improved so that they can consume low power as well as communicate with the others without a wire (i.e., wireless devices). The such sensors will collect a great deal of data in order to help robots learn the artificial intelligence. Thus, intelligent robots can assist man in heavy and harmful works, which has increasingly enhanced life quality of human.

To reach the above picture, there are still several challenges that we must design low power wireless sensors, while these sensors can still broad signal in a wide area. Besides, 5th-Generation Wireless Systems (5G), which is now in the development progress, also requires high frequency bands. With 5G, user can access large information because of a wide bandwidth. However, design chips in high frequency emerges more problems than in middle or low frequency. This leads to a fact that microwave engineering is still completely unsolved, and it demands resources of well-knowledge researchers and engineers to tackle existing challenges.

Consider to the field of Microwave Engineering, there is a number of technical problems need to be addressed due to problematic phenomena of the high frequency. Among these ones, power amplifier design is one of the most largely tough cases. Actually, in the low and middle frequency, it seems to be uncomplicated to design an amplifier with a high gain. However, in the high frequency, it is really a challenge because of the non-ideality of components. Concretely, a resistor may become an inductor in the high frequency. This uncertainty

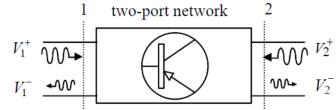


Fig. 1: A two-port network

is difficult to predict function of the component and bring more problems that requires the designers need to consider comprehensively.

Be inspired of the power amplifier design's challenges, in this article, we propose a method to design and simulate a 5.4-GHz Low Noise Amplifier, using S-parameters of a transistor. In the following, we will explain the design approach using S-parameters in section II, and implement these theories in section III to solve the problem of the 5.4-GHz Low Noise Amplifier. Then, a simulation in section IV will be conducted to verify these above designs before concluding what we achieved in the last section.

## II. PROPOSED METHOD

In the high frequency, a circuit is typically represented by S-matrix, while Z-matrix and Y-matrix are not preferred. It can be explained that to measure Z-matrix or Y-matrix, we need to short or open a terminal of the network. Unfortunately, a short- or open- circuit is incredibly a reactor (e.g., inductor or capacitor) in the high frequency, which cannot reveal a right measure as in the low and middle frequency. To handle with this situation, people use ratios between incident and reflect waves to build up a S-matrix for representing a circuit network in high frequency.

A transistor can be considered as a 2-port network (figure 1) and its S-matrix is a 2x2 matrix.

$$S = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \quad (1)$$

where

$$S_{ij} = \left. \frac{V_i^-}{V_j^+} \right|_{V_k^+=0, k \neq j} \quad (2)$$

In physical meaning, while  $S_{21}$  and  $S_{12}$  depict forward and backward gain of the transistor,  $S_{11}$  and  $S_{22}$  illustrate the maximum delivered power ability to the network at the terminal 1 and 2. Therefore, by examining such S-matrix, we can understand features of a transistor.

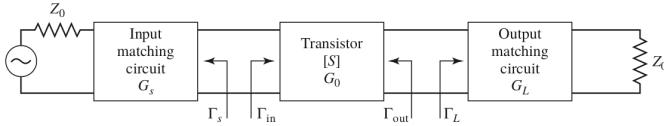


Fig. 2: Model of a power amplifier

Figure 2 depicts a model of a power amplifier. In which, there are generally 3 parts, namely Input matching, Transistor, and Output matching. To design a low noise amplifier, the most important parameter is Noise Figure. Noise figure of a transistor can be computed based on its S-matrix.

$$NF = NF_{min} + \frac{4R_N}{Z_0} \frac{|\Gamma_S - \Gamma_{opt}|^2}{(1 - |\Gamma_S|^2)|1 + \Gamma_{opt}|^2} \quad (3)$$

where  $NF_{min}$ ,  $R_N$ ,  $\Gamma_{opt}$  are parameters of the transistor, and they depend on DC-bias condition.  $Z_0$  is the characteristic impedance of transmission line and its value is typically  $50\Omega$ . Besides, transducer gain of this amplifier is also an essential evaluating parameter. It can be calculated using S-matrix of the transistor.

$$G_T = \frac{P_L}{P_{av}} = \frac{1 - |\Gamma_S|^2}{|1 - \Gamma_S \Gamma_{in}|^2} |S_{21}|^2 \frac{1 - |\Gamma_L|^2}{|1 - \Gamma_L S_{22}|^2} \quad (4)$$

It is clear in equation 3 that if  $\Gamma_S = \Gamma_{opt}$ , noise figure will get the minimum value of  $NF_{min}$ . Hence, we can force the input matching circuit to obtain this extreme condition, so the noise figure will be as low as the expectation. Moreover, to maximize the transducer gain,  $\Gamma_L = \Gamma_{out}^*$  is taken into account in the output matching circuit. Finally, we have all of parameters for input and output matching circuit.

$$\Gamma_S = \Gamma_{opt} \quad (5)$$

$$\Gamma_L = \Gamma_{out}^* = (S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - \Gamma_S S_{11}})^* \quad (6)$$

To design a matching circuit, a  $50\Omega$  transmission line is used, accompanying with a quarter-wavelength transmission line. Assume that we need to convert a resistor of  $50\Omega$  to a value  $Z_B$ , corresponding to  $\Gamma_B/\phi$  ( $-180^\circ \leq \phi \leq 180^\circ$ ). The characteristic impedance of the quarter-wavelength transmission line is computed so that the  $50\Omega$  is converted to have a reflection coefficient of  $\Gamma_A = -\Gamma_B$ .

$$Z_1 = \sqrt{Z_0 Z_c} = \sqrt{Z_0 (Z_0 \frac{1 - \Gamma_B}{1 + \Gamma_B})} = Z_0 \sqrt{\frac{1 - \Gamma_B}{1 + \Gamma_B}} \quad (7)$$

Then, length of the  $50\Omega$  transmission line is also computed to transform  $-\Gamma_B$  to  $\Gamma_B/\phi$ .

$$l_0 = \frac{180^\circ - \phi}{720^\circ} \lambda \quad (8)$$

Figure 3 and figure 4 show the impedance matching circuit and the Smith-chart representation of the design.

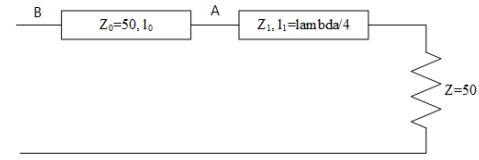


Fig. 3: Matching circuit model

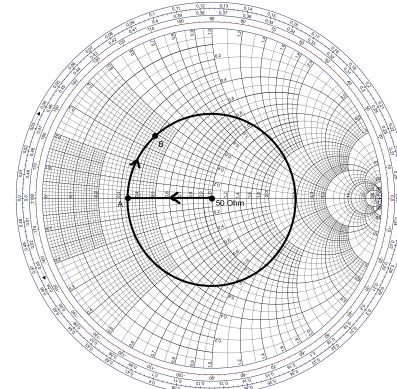


Fig. 4: Smith-chart representation of the impedance patching design

### III. IMPLEMENTATION

Firstly, we use a cascade configuration of two HBTs in figure 5 in order to boost the internal gain. Then, these transistors are biased at  $I_{CQ} = 6.458mA$  (table I). From here, several characteristic parameters of the cascade model is measured in table II.

As the above analysis, when choosing  $\Gamma_S = \Gamma_{opt} = 0.269/116.248$ , the noise figure of LNA will be minimized.

$$NF = NF_{min} = 1.99 \text{ dB} \quad (9)$$

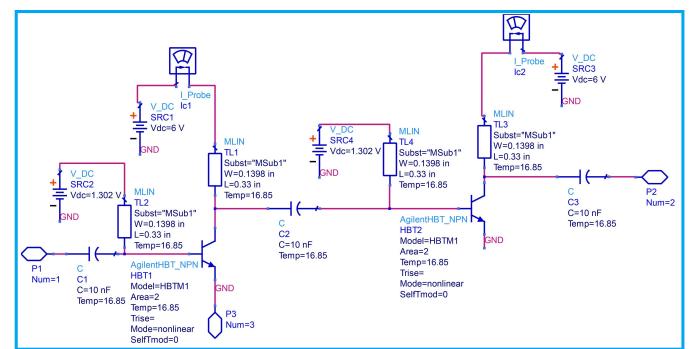


Fig. 5: Bias of BJT

TABLE I: Bias collector current of two transistors

Parameter	Value
$I_{CQ1}$	6.458 mA
$I_{CQ2}$	6.458 mA

TABLE II: Characteristic parameters of the cascade model

Parameter	Value
$S_{11}$	$0.687/-126.708$
$S_{12}$	$0.004/43.855$
$S_{21}$	$25.041/-156.196$
$S_{22}$	$0.315/-34.447$
$\Gamma_{opt}$	$0.269/116.248$
$NF$	$2.44 \text{ dB}$
$NF_{min}$	$1.99 \text{ dB}$
$R_N$	$414 \Omega$

Then, output-, load-, and input- reflection coefficients is calculated based on equation 6.

$$\Gamma_{out} = S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - \Gamma_SS_{11}} = 0.339/-31.924 \quad (10)$$

$$\Gamma_L = \Gamma_{out}^* = 0.339/31.924 \quad (11)$$

Consequently, we can design matching circuits corresponding to these reflection coefficients. Figure 6 and 7 are the input and output matching circuit, respectively.

$$Input - matching : \begin{cases} Z_1 = 37.96\Omega, \lambda/4 \text{ TL} \\ l_0 = 0.085\lambda, 50\Omega \text{ TL} \end{cases}$$

$$Output - matching : \begin{cases} Z_1 = 35.13\Omega, \lambda/4 \text{ TL} \\ l_0 = 0.206\lambda, 50\Omega \text{ TL} \end{cases}$$

Also, from equation 4, the transducer gain of the LNA can be computed.

$$G_T = 982.3 = 29.922 \text{ dB} \quad (12)$$

Finally, by combining the cascade model and 2 matching circuits, we achieved the LNA in figure 8.

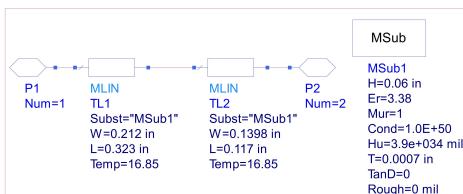


Fig. 6: Input matching circuit

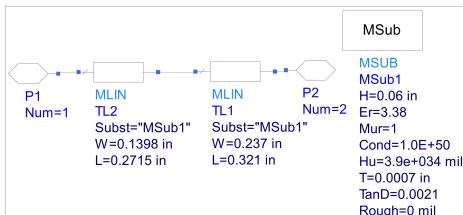


Fig. 7: Output matching circuit

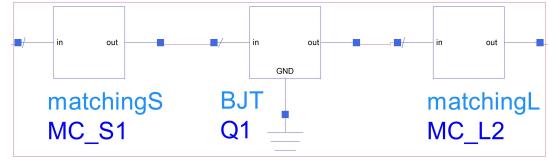


Fig. 8: LNA model

TABLE III: Parameters of the LNA at the frequency of 5.4 GHz

Parameter	Value
$NF$	$1.99 \text{ dB}$
$G_T$	$30.00 \text{ dB}$
$RL_1$	$-10.31 \text{ dB}$
$RL_2$	$-98.28 \text{ dB}$
$I$	$93.35 \text{ dB}$
$P_{1dB,in}$	$-8.20 \text{ dBm}$
$IIP3$	$-9.83 \text{ dBm}$
$OIP3$	$19.61 \text{ dBm}$

#### IV. SIMULATION RESULTS

After completing the design, we conduct a simulation to verify some important parameters of the LNA. Figure 9 depicts results in a wide range of frequency, while table III shows results at the frequency of 5.4 GHz. In figure 9a, noise figure of the LNA approximates to the minimum noise figure (1.99 dB) at 5.4 GHz as expected. Also, in figure 9b, the transducer gain drops as increasing the frequency, and stand at 30.00 dB at the examined frequency. Consider to return loss (figure 9c and 9d), while the matched load results in a deep valley of the load return loss (-98.28 dB) at 5.4 GHz, the source return loss stands at -10.31 dB because of the non-matched source. Meanwhile, the LNA is quite isolated with 93.35 dB at the operation frequency. In figure 9f, m2 is the normal operation point and m1 is the 1dB compression point. From that, we can point out value of input power at the 1dB compression point. To examine the Inception Point 3, we carry out a Two-tone test, which is illustrated in figure 9g and 9h.

Table IV reveals a comparison between theoretical and simulation results. It is clear that noise figure and transducer gain in both cases are equivalent, which demonstrates that our design is theoretically valid. Furthermore, in table V, noise figure and transducer gain values are also compared to figure out how good the design improves such parameters before and after matching. As we can see that due to choosing  $\Gamma_S = \Gamma_{opt}$ , we can reduce the noise figure of the system for about 20%, whilst the transducer gain is added more 7% residue. This leads to a fact that our design works well.

TABLE IV: Comparison between theoretical and simulation results

Parameter	Theoretical	Simulation
$NF$	$1.99 \text{ dB}$	$1.99 \text{ dB}$
$G_T$	$29.92 \text{ dB}$	$30.00 \text{ dB}$

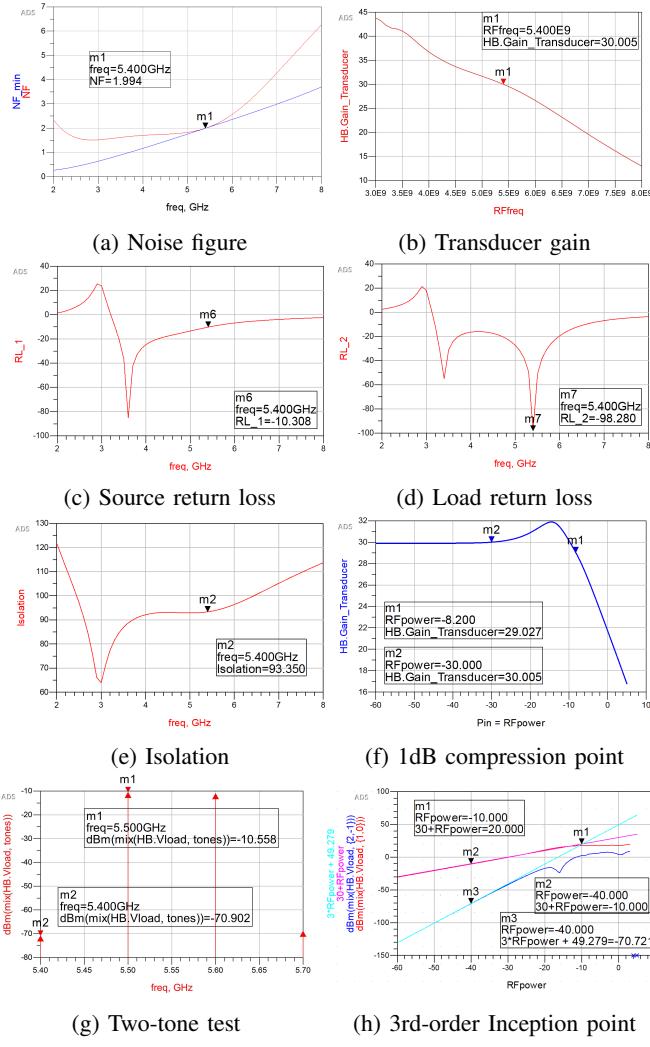


Fig. 9: Parameters of the LNA in a wide range of frequency

TABLE V: Comparison between before and after matching

Parameter	Before	After
NF	2.44 dB	1.99 dB
G <sub>T</sub>	28.08 dB	30.00 dB

## VI. ACKNOWLEDGE

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## V. CONCLUSION

In this article, we designed a Low Noise Amplifier at a high frequency of 5.4 GHz. This design is based on S-parameters of a transistor. Here, we use a cascade configuration of two HBTs in order to boost the internal gain. In addition, we also design an input matching circuit to minimize the noise figure of the amplifier. Moreover, an output matching circuit is placed before the load so as to maximize the power delivered on the load. Finally, the simulation results show that our design is efficient with 30 dB of transducer gain as well as 1.99 dB of noise figure. Therefore, our model is theoretically good enough for a Low Noise Amplifier.