MCG

Friday, December 19, 2014
9:02 AM

1) INTRODUCTION

The multipurpose clock generator (MCG) module provides several clock source choices for the MCU. The module contains a frequency-locked loop (FLL) and a phase-locked loop (PLL). The FLL is controllable by either an internal or an external reference clock. The PLL is controllable by the external reference clock. The module can select either of the FLL or PLL output clocks, or either of the internal or external reference clocks as a source for the MCU system clock. The MCG operates in conjuction with a crystal oscillator, which allows an external crystal, ceramic resonator, or another external clock source to produce the external reference clock.

2) MODE OPERATION

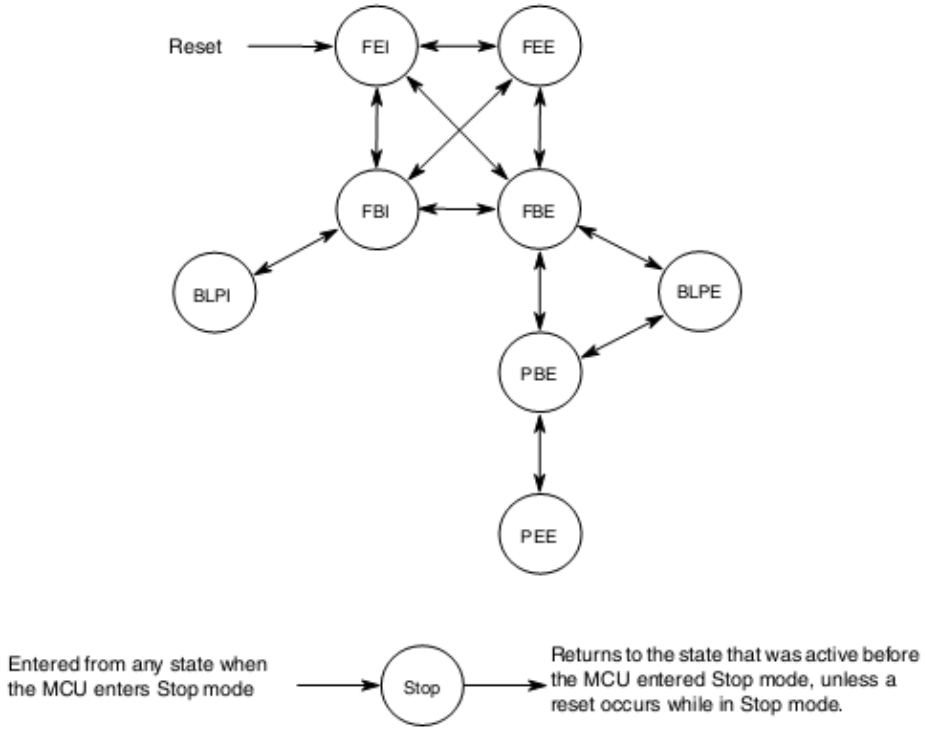

Figure 24-16. MCG mode state diagram

3) KEIL DEFINITION

```
/** MCG - Register Layout Typedef */
```

```
typedef struct {
  __IO uint8_t C1;                  /**< MCG Control 1 Register, offset: 0x0 */
  __IO uint8_t C2;                  /**< MCG Control 2 Register, offset: 0x1 */
  __IO uint8_t C3;                  /**< MCG Control 3 Register, offset: 0x2 */
  __IO uint8_t C4;                  /**< MCG Control 4 Register, offset: 0x3 */
  __IO uint8_t C5;                  /**< MCG Control 5 Register, offset: 0x4 */
  __IO uint8_t C6;                  /**< MCG Control 6 Register, offset: 0x5 */
  __I  uint8_t S;                   /**< MCG Status Register, offset: 0x6 */
       uint8_t RESERVED_0[1];
  __IO uint8_t SC;                  /**< MCG Status and Control Register, offset: 0x8 */
       uint8_t RESERVED_1[1];
  __IO uint8_t ATCVH;               /**< MCG Auto Trim Compare Value High Register, offset: 0xA */
  __IO uint8_t ATCVL;               /**< MCG Auto Trim Compare Value Low Register, offset: 0xB */
  __I  uint8_t C7;                  /**< MCG Control 7 Register, offset: 0xC */
  __IO uint8_t C8;                  /**< MCG Control 8 Register, offset: 0xD */
  __I  uint8_t C9;                  /**< MCG Control 9 Register, offset: 0xE */
  __I  uint8_t C10;                 /**<  MCG Control 10 Register, offset: 0xF */
} MCG_Type;
```