SIM

Wednesday, December 17, 2014
4:23 PM

1) INTRODUCTION

The system integration module (SIM) provides system control and chip configuration registers.

2) FEATURES

System clocking configuration
- System clock divide values
  - Architectural clock gating control
  - ERCLK32K clock selection
  - USB clock selection
  - UART0 and TPM clock selection
- Flash and System RAM size configuration
- USB regulator configuration
- TPM external clock and input capture selection
- UART receive/transmit source selection/configuration

3) REGISTER DEFINITION

See reference manual for more details.

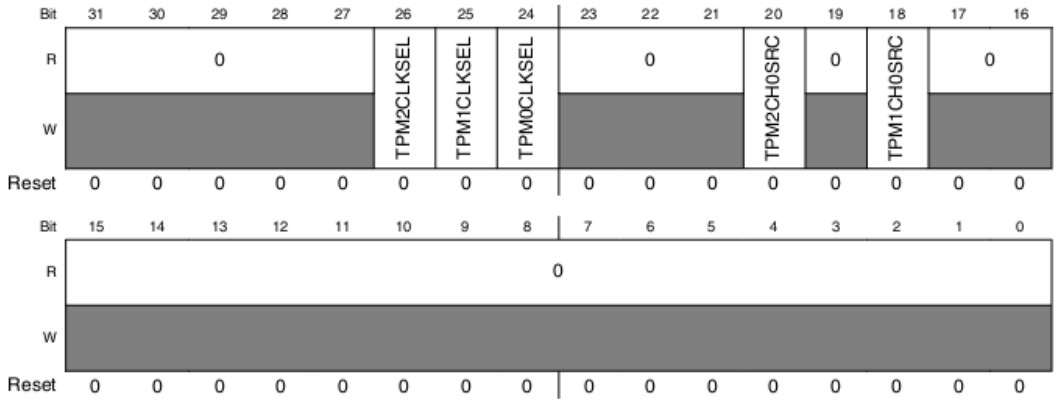
```
/** SIM - Register Layout Typedef */
typedef struct {
  __IO uint32_t SOPT1;                  /**< System Options Register 1, offset: 0x0 */
  __IO uint32_t SOPT1CFG;               /**< SOPT1 Configuration Register, offset: 0x4 */
     uint8_t RESERVED_0[4092];
  __IO uint32_t SOPT2;                  /**< System Options Register 2, offset: 0x1004 */
     uint8_t RESERVED_1[4];
  __IO uint32_t SOPT4;                  /**< System Options Register 4, offset: 0x100C */
  __IO uint32_t SOPT5;                  /**< System Options Register 5, offset: 0x1010 */
     uint8_t RESERVED_2[4];
  __IO uint32_t SOPT7;                  /**< System Options Register 7, offset: 0x1018 */
     uint8_t RESERVED_3[8];
  __I  uint32_t SDID;                   /**< System Device Identification Register, offset: 0x1024 */
     uint8_t RESERVED_4[12];
  __IO uint32_t SCGC4;                  /**< System Clock Gating Control Register 4, offset: 0x1034 */
  __IO uint32_t SCGC5;                  /**< System Clock Gating Control Register 5, offset: 0x1038 */
  __IO uint32_t SCGC6;                  /**< System Clock Gating Control Register 6, offset: 0x103C */
  __IO uint32_t SCGC7;                  /**< System Clock Gating Control Register 7, offset: 0x1040 */
  __IO uint32_t CLKDIV1;                /**< System Clock Divider Register 1, offset: 0x1044 */
     uint8_t RESERVED_5[4];
  __IO uint32_t FCFG1;                  /**< Flash Configuration Register 1, offset: 0x104C */
  __I  uint32_t FCFG2;                  /**< Flash Configuration Register 2, offset: 0x1050 */
     uint8_t RESERVED_6[4];
  __I  uint32_t UIDMH;                  /**< Unique Identification Register Mid-High, offset: 0x1058 */
  __I  uint32_t UIDML;                  /**< Unique Identification Register Mid Low, offset: 0x105C */
  __I  uint32_t UIDL;                   /**< Unique Identification Register Low, offset: 0x1060 */
     uint8_t RESERVED_7[156];
  __IO uint32_t COPC;                   /**< COP Control Register, offset: 0x1100 */
  __O  uint32_t SRVCOP;                 /**< Service COP Register, offset: 0x1104 */
} SIM_Type;
```

4 RTCCLKOUTSEL	RTC clock out select

Field	Description
	Selects either the RTC 1 Hz clock or the OSC clock to be output on the RTC_CLKOUT pin. 0 RTC 1 Hz clock is output on the RTC_CLKOUT pin. 1 OSCERCLK clock is output on the RTC_CLKOUT pin.
3–0 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

3.4) System Options Register 4 (SIM_SOPT4)

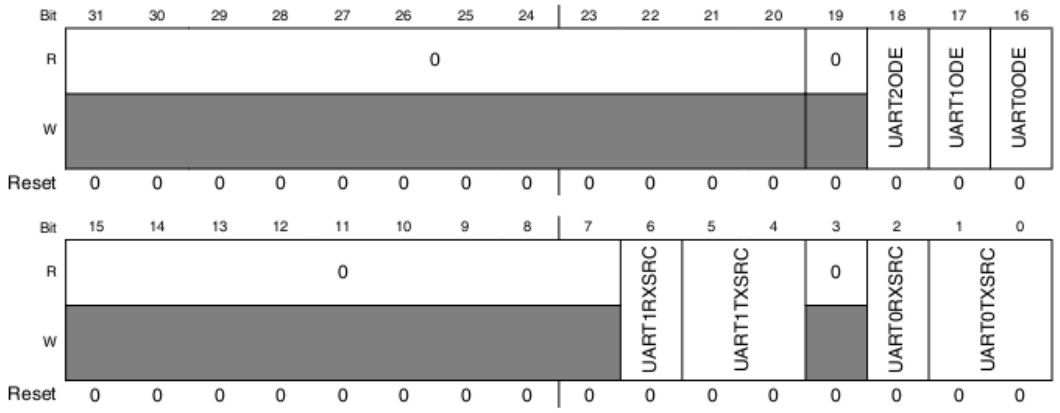
Address: 4004_7000h base + 100Ch offset = 4004_800Ch



Field	Description
31–27 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
26 TPM2CLKSEL	TPM2 External Clock Pin Select Selects the external pin used to drive the clock to the TPM2 module. **NOTE:** The selected pin must also be configured for the TPM external clock function through the appropriate pin control register in the port control module. 0 TPM2 external clock driven by TPM_CLKIN0 pin. 1 TPM2 external clock driven by TPM_CLKIN1 pin.
25 TPM1CLKSEL	TPM1 External Clock Pin Select Selects the external pin used to drive the clock to the TPM1 module. **NOTE:** The selected pin must also be configured for the TPM external clock function through the appropriate pin control register in the port control module.

Field	Description
	0 TPM1 external clock driven by TPM_CLKIN0 pin. 1 TPM1 external clock driven by TPM_CLKIN1 pin.
24 TPM0CLKSEL	TPM0 External Clock Pin Select Selects the external pin used to drive the clock to the TPM0 module. **NOTE:** The selected pin must also be configured for the TPM external clock function through the appropriate pin control register in the port control module. 0 TPM0 external clock driven by TPM_CLKIN0 pin. 1 TPM0 external clock driven by TPM_CLKIN1 pin.
23–21 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
20 TPM2CH0SRC	TPM2 channel 0 input capture source select Selects the source for TPM2 channel 0 input capture. **NOTE:** When TPM2 is not in input capture mode, clear this field. 0 TPM2_CH0 signal 1 CMP0 output
19 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
18 TPM1CH0SRC	TPM1 channel 0 input capture source select Selects the source for TPM1 channel 0 input capture. **NOTE:** When TPM1 is not in input capture mode, clear this field. 0 TPM1_CH0 signal 1 CMP0 output
17–0 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

3.5) System Options Register 5 (SIM_SOPT5)



Field	Description
31–20 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
19 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
18 UART2ODE	UART2 Open Drain Enable 0 Open drain is disabled on UART2 1 Open drain is enabled on UART2
17 UART1ODE	UART1 Open Drain Enable 0 Open drain is disabled on UART1 1 Open drain is enabled on UART1
16 UART0ODE	UART0 Open Drain Enable 0 Open drain is disabled on UART0 1 Open drain is enabled on UART0
15–7 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
6 UART1RXSRC	UART1 receive data source select Selects the source for the UART1 receive data. 0 UART1_RX pin 1 CMP0 output
5–4 UART1TXSRC	UART1 transmit data source select Selects the source for the UART1 transmit data.

Field	Description
	00 UART1_TX pin 01 UART1_TX pin modulated with TPM1 channel 0 output 10 UART1_TX pin modulated with TPM2 channel 0 output 11 Reserved
3 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
2 UART0RXSRC	UART0 receive data source select Selects the source for the UART0 receive data. 0 UART0_RX pin 1 CMP0 output
1–0 UART0TXSRC	UART0 transmit data source select Selects the source for the UART0 transmit data. 00 UART0_TX pin 01 UART0_TX pin modulated with TPM1 channel 0 output 10 UART0_TX pin modulated with TPM2 channel 0 output 11 Reserved

3.6) System Options Register 7 (SIM_SOPT7)

Field	Description
31–8 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
7 ADC0ALTTRGEN	ADC0 alternate trigger enable Enable alternative conversion triggers for ADC0. 0 TPM1 channel 0 (A) and channel 1 (B) triggers selected for ADC0. 1 Alternate trigger selected for ADC0.
6–5 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
4 ADC0PRETRGSEL	ADC0 pretrigger select Selects the ADC0 pre-trigger source when alternative triggers are enabled through ADC0ALTTRGEN. 0 Pre-trigger A 1 Pre-trigger B
3–0 ADC0TRGSEL	ADC0 trigger select Selects the ADC0 trigger source when alternative triggers are functional in stop and VLPS modes. . 0000 External trigger pin input (EXTRG_IN) 0001 CMP0 output 0010 Reserved 0011 Reserved 0100 PIT trigger 0 0101 PIT trigger 1 0110 Reserved 0111 Reserved 1000 TPM0 overflow 1001 TPM1 overflow 1010 TPM2 overflow 1011 Reserved 1100 RTC alarm 1101 RTC seconds 1110 LPTMR0 trigger 1111 Reserved

3.7) System Device Identification Register (SIM_SDID)

Address: 4004_7000h base + 1024h offset = 4004_8024h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	FAMID				SUBFAMID				SERIESID				SRAMSIZE				REVID				DIEID							0			PINID			
W																																
Reset	*	*	*	*	*	*	*	*	0	0	0	1	*	*	*	*	*	*	*	*	0	1	0	0	1	0	0	0	*	*	*	*

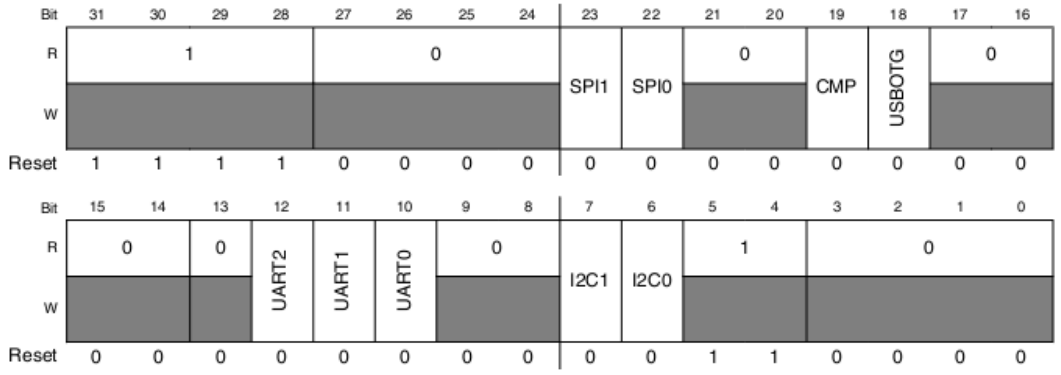
* Notes:
- FAMID field: Device specific value.
- SUBFAMID field: Device specific value.
- SRAMSIZE field: Device specific value.
- REVID field: Device specific value.
- PINID field: Device specific value.

Field	Description
31–28 FAMID	Kinetis family ID Specifies the Kinetis family of the device. 0000 KL0x Family (low end) 0001 KL1x Family (basic) 0010 KL2x Family (USB) 0011 KL3x Family (Segment LCD) 0100 KL4x Family (USB and Segment LCD)
27–24 SUBFAMID	Kinetis Sub-Family ID Specifies the Kinetis sub-family of the device. 0010 KLx2 Subfamily (low end) 0100 KLx4 Subfamily (basic analog) 0101 KLx5 Subfamily (advanced analog) 0110 KLx6 Subfamily (advanced analog with I2S)
23–20 SERIESID	Kinetis Series ID Specifies the Kinetis family of the device. 0001 KL family
19–16 SRAMSIZE	System SRAM Size Specifies the size of the System SRAM 0000 0.5 KB 0001 1 KB 0010 2 KB 0011 4 KB 0100 8 KB 0101 16 KB

Field	Description
	0110 32 KB 0111 64 KB
15–12 REVID	Device revision number Specifies the silicon implementation number for the device.
11–7 DIEID	Device die number Specifies the silicon implementation number for the device.
6–4 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
3–0 PINID	Pincount identification Specifies the pincount of the device. 0000 16-pin 0001 24-pin 0010 32-pin 0011 Reserved 0100 48-pin 0101 64-pin 0110 80-pin 0111 Reserved 1000 100-pin 1001 Reserved 1010 Reserved 1011 Reserved 1100 Reserved 1101 Reserved 1110 Reserved 1111 Reserved

3.8) System Clock Gating Control Register 4 (SIM_SCGC4)

Address: 4004_7000h base + 1034h offset = 4004_8034h



Field	Description
31–28 Reserved	This field is reserved. This read-only field is reserved and always has the value 1.
27–24 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
23 SPI1	SPI1 Clock Gate Control This bit controls the clock gate to the SPI1 module. 0 Clock disabled 1 Clock enabled
22 SPI0	SPI0 Clock Gate Control This bit controls the clock gate to the SPI0 module. 0 Clock disabled 1 Clock enabled
21–20 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
19 CMP	Comparator Clock Gate Control This bit controls the clock gate to the comparator module. 0 Clock disabled 1 Clock enabled
18 USBOTG	USB Clock Gate Control This bit controls the clock gate to the USB module.

Field	Description
	0 Clock disabled 1 Clock enabled
17–14 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
13 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
12 UART2	UART2 Clock Gate Control This bit controls the clock gate to the UART2 module. 0 Clock disabled 1 Clock enabled
11 UART1	UART1 Clock Gate Control This bit controls the clock gate to the UART1 module. 0 Clock disabled 1 Clock enabled
10 UART0	UART0 Clock Gate Control This bit controls the clock gate to the UART0 module. 0 Clock disabled 1 Clock enabled
9–8 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
7 I2C1	I2C1 Clock Gate Control This bit controls the clock gate to the I^2C1 module. 0 Clock disabled 1 Clock enabled
6 I2C0	I2C0 Clock Gate Control This bit controls the clock gate to the I^2C0 module. 0 Clock disabled 1 Clock enabled
5–4 Reserved	This field is reserved. This read-only field is reserved and always has the value 1.
3–0 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.