Tutorial 3 - Discrete Walsh Transform Solution

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1 LABORATORY QUESTIONS

1. Discrete Walsh transform processor (30%). Make a combinatorial, parallel implementation of an $N = 64$ DWT processor for the Altera Cyclone V 5CSEMA5 FPGA used in the DE1-SoC board. Your inputs should be 16-bit integers in two's complement form, and your output represented as a two's complement fraction with sufficiently large wordlength that overflow cannot occur.

   Create a set of random test vectors and verify that your design is correct via simulation. The FPGA design tools report the maximum clock rate, f_{max} which can be achieved by your design. What is this value? The maximum throughput is thus $2Nf_{max}$ bytes/sec. Calculate the throughput of your design.

2. Pipelined DWT processor (30%). Modify your DWT processor so that it is pipelined and verify via simulation. What is the new design's maximum throughput? What is the speedup compared with the non-pipelined design?

3. Multicycle execution (40%). It may not be feasible to supply the DWT processor with 64 high-speed, parallel inputs. Develop a modified version of the DWT processor which takes 2 inputs samples per cycle, i.e. it takes $N/2$ cycles to obtain a complete input vector. Redesign your processor so that it minimises the area-delay product (area being measured in LUTs) and can process streaming input data without stalling. What is the maximum performance in bytes/sec?

4. Comparison (bonus 20%). Integrate the DWT processor with an linear feedback shift register based random number generator which is used as the source of the input data. Implement the design in hardware and verify its correct operation. Identify the sources of bottlenecks in your design.

2 SOLUTIONS

1. Discrete Walsh transform processor.

   Combinatorial, parallel implementation of an $N = 64$ DWT processor for the Altera Cyclone I 2C70F672 FPGA used in the DE2-70 board.

   Inputs are 16-bit integers in two's complement form, and output represented as a two's complement fraction with wordlength of 22.

   The set of random test vectors are in 'xin.txt' and verify that your design is correct via simulation.

   The FPGA design tools report the maximum clock rate f_{max} as ... MHz. The maximum throughput is thus $2Nf_{max}$ = ...*2*64 bytes/sec.

2. Pipelined DWT processor. Pipelined processor and simulation.

   The new design's maximum throughput is thus $2Nf_{max}$ = ... bytes/sec.

   The speedup compared with the non-pipelined design is ....

3. Multicycle execution.

   A modified version of the DWT processor which takes 2 inputs samples per cycle, 32 cycles to obtain a complete input vector.

   Redesign a DWT processor which can process streaming input data without stalling.

   The maximum performance in bytes/sec is ... bytes/sec.

4. Comparison.

   The sources of bottlenecks in the design is ...

REFERENCES