Reconfigurable Computing

Tutorial 2 - LSTM Network (Parallelism)

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1 Introduction

Compiler directives are used in Vivado HLS to generate solutions with different architectures and degrees of parallelism. This tutorial has the following goals:

- Gain experience in optimising a design with compiler directives.

2 Laboratory Questions

Your answers to this laboratory should be in the form of a simple report. For each question below, provide a listing of the changes to the original code as well as the speedup compared with the baseline design generated in the previous tutorial in your report.

2.1 (30%) Loop Pipelining

We will first explore how loop pipelining can be used to increase parallelism in the design. Use the Analysis Perspective to understand the timing implications of your changes. Find the configuration which gives the best overall result in terms of: execution time T; area A (defined as the percentage of the most used resource out of LUTs, memories and DSPs); and AT product.

2.2 (30%) Array Partitioning

Keeping the best Loop Pipelining directives, explore how array partitioning can improve the execution time of your design. Find the configuration that provides the best execution time and best AT product.

2.3 (40%) Other Directives

Using other directives such as Dataflow, optimise the design as much as possible. Report on the speedup of your final solution vs only applying Loop Pipelining and Array Partitioning.