Electronic Photonic Integrated Circuits and Control Systems

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For my family and Indonesia

Declaration

I hereby declare that this submission is my own work and to the best of my knowledge contains no materials previously published or written by another person, or substantial proportions of material which have been accepted for the award of any other degree or diploma at the University of Sydney or any other educational institution, except where due acknowledgement is made in the thesis. Any contribution made to the research by others, with whom I have worked at the University of Sydney or elsewhere, is explicitly acknowledged in the thesis.

- The research direction and subject were suggested by Professor Philip H. W. Leong, Professor Benjamin J. Eggleton and Dr. Chunle Xiong.

- The idea of heater controller design and the use of phase locked loop for photonic switch control with FPGA, were originally proposed by Professor Philip H.W. Leong.

- The experiments from Chapter 3 to Chapter 6 were conducted at the Centre of Ultra-high Bandwidth Devices for Optical System (CUDOS) and Australian Institute for Nanoscale Science and Technology (AINST) at The University of Sydney.

- Advice and editing assistance for the preparation of this thesis have been provided by Professor Philip H. W. Leong, Professor Benjamin J. Eggleton and Dr. Chunle Xiong.

- The idea of monolithic segmented transmitter design with smart partitioning was originally proposed by Dr. Douglas M. Gill and team at IBM T. J. Watson.

- The device under test and equipments as presented in Chapter 7 were developed by IBM T. J. Watson team and the experiments were conducted at IBM T. J. Watson Research Centre in Yorktown Heights - New York, USA.

- Part of thesis are copied with permission from papers co-authored with Dr. Chunle Xiong.

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Acknowledgements

Abstract

Photonics and electronics have complementary strengths. Photonic systems can operate at frequencies several orders of magnitude higher than electronics, whereas electronics offers extremely high density and easily built memories. Integrated photonic-electronic systems promise to combine advantage of both, leading to advantages in accuracy, reconfigurability and energy efficiency.

This work concerns of hybrid and monolithic electronic-photonic system design. Focusing on applications in photonic-chip-based optical signal processing, the contributions of this thesis are five-fold. First, a high resolution voltage supply to control the thermooptic photonic chip for time-bin entanglement is described, in which the electronics system controller can be scaled with more number of power channels and the ability to daisy-chain the devices. This controller is integrated with a silicon nitride photonic circuit, which combines low loss and tight integration, paving the way for scalable real-world quantum information processors. Second, a system identification technique embedded with feedback control for wavelength stabilization and control model in silicon nitride photonic integrated circuits is proposed. Using the system, the wavelength in thermooptic device can be stabilized in dynamic environment. Third, the generation of more deterministic photon sources with temporal multiplexing established using field programmable gate arrays (FPGAs) as controller photonic device is demonstrated for the first time. The FPGAs configuration employed phase locked loop with simple logic and synchronized delay. The result shows an enhancement to the single photon output probability without introducing additional multi-photon noise. Fourth, multiple-input and multiple-output (MIMO) control of a silicon nitride thermooptic photonic circuits incorporating Mach Zehnder interferometers (MZIs) is demonstrated for the first time using a dual proportional integral reference tracking technique. The system exhibits improved performance in term of control accuracy by reducing wavelength peak drift due to internal and external disturbances. Finally, a monolithically integrated complementary metal oxide semiconductor (CMOS) nanophotonic segmented transmitter is characterized. With segmented design, the monolithic Mach Zehnder modulator (MZM) shows a low link sensitivity and low insertion loss with driver flexibility. This transmitter holds promise for high energy efficiency applications.

Publications

The work presented in this thesis has been published in a number of journals and conferences.
Journal publications:

1. **A. Mahendra**, C. Xiong, X. Zhang, B. J. Eggleton, P. H. W. Leong. "Multi wavelength stabilization control of thermooptic system with adaptive reconfiguration". *Journal of Applied Optics*, Vol. 56, Issue 4, pp. 1113-1118, 2017.

2. C. Xiong, X. Zhang, Z. Liu, M. J. Collins, **A. Mahendra**, L. G. Helt, M. J. Steel, D. Choi, C. J. Chae, P. H. W. Leong, B. J. Eggleton. "Active temporal multiplexing of indistinguishable single photons". *Nature Communications*, 7 (10853), 2016. (doi:10.1038/ncomms10853)

3. C. Xiong, X. Zhang, **A. Mahendra**, J. He, D. Choi, C. J. Chae, D. Marpaung, A. Leinse, R. G. Heideman, M. Hoekman, C. G. H. Roeloffzen, R. M. Oldenbeuving, P. W. L. Van Dijk, C. Taddei, P. H. W. Leong, B. J. Eggleton, "A compact and reconfigurable silicon nitride time-bin entanglement circuit". *Optica*, 2(8):724-727, August 2015.

Conference presentations:

1. **A. Mahendra**, D. M. Gill, C. Xiong, J. S. Orcutt, B. G. Lee, T. N. Huynh, J. E. Proesel, N. Dupuis, P. H. W. Leong, B. J. Eggleton, and W. M. J. Green, "Monolithically integrated CMOS nanophotonic segmented mach zehnder transmitter". *CLEO Conference* US, San Jose, California USA, May 2017.

2. **A. Mahendra**, C. Xiong, X. Zhang, B. J. Eggleton, P. H. W. Leong. "Dynamic thermal control scheme of silicon nitride photonic integrated circuits". *In 40th Australian Conference on Optical Fibre Technology*, 38-40, Adelaide, November 2015.

3. X. Zhang, **A. Mahendra**, P. H. W. Leong, B. J. Eggleton, C. Xiong, "Time-bin entanglement in compact and reconfigurable silicon nitride photonic circuits". *In the Australian Conference on Optics, Lasers and Spectroscopy*, Adelaide, November 2015.

4. C. Xiong, X. Zhang, Z. Liu, **A. Mahendra**, D. Choi, C. J. Chae, P. H. W. Leong, M. Collins, B. J. Eggleton, "Active temporal multiplexing of a silicon heralded single-photon source". *CLEO Europe Postdeadline*, Munich, Germany, June 2015.

Patent submission:

1. **A. Mahendra**, P. H. W. Leong, C. Xiong, B. J. Eggleton. Patent No. US 62/416,695, *US Provisional Patent*, 2016.

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Nomenclature

List of Symbols

(i) Idler

(s) Single

$\varphi_{p,s,i}$ Relative phase difference

$T\omega$ Natural frequency

T_1 First time constant

x Mode

δ_t Relative delay

η Plant output

η_I Idler efficiencies

η_S Net signal

$|k\rangle_x$ State in which there is a photon

λ Wavelength

Ω Impedance in ohm

θ Phase

υ Frequency

φ_p Phase difference

ζ Damping coefficient

C Controller

c Speed of light

d External disturbance

d_I Dark count rates per pulse

d_S Signal detectors

dn/dT Thermooptic coeffient

F Sensor

$H(s)$ Transfer function

K Gain

kth   k time slot

k_d Derivative gain

k_i Integral gain

k_p Proportional gain

n Sensor noise

P Plant

P_{in} Power in

P_{out} Power out

r Reference or command input

T Room temperature

T_d Derivative time

T_i Integral time

u Actuating signal

v Sum of actuating signal and disturbance

y Sum of plant output and noise

List of Abbreviations

ADC   Analog to digital converter

ADF   Add-drop filter

APD   Avalanche photo diode

ASE   Amplified spontaneous emission

ASICs   Application specific integrated circuits

ATT   Attenuator

AWG   Arrayed waveguide grating

BER   Bit error rate

BPF   Band pass filter

CAR   Coincidence-to-accidental ratio

CML   Current mode logic

CMOS   Complemententary metal oxide semiconductor

DAC   Digital to analog converter

DFB   Distributed feedback laser

DG   Delay generator

DIP   Dual in-line package

FC   Fiber couplers

FPGAs   Field programmable gate arrays

GaAs   Galium Arsenide

Ge   Germanium

HOM   Hong Ou Mandel quantum interference

HSPS   Heralded single photon source

InP   Indium Phosphide

IP	Inline polarizer
LAN	Local area network
LUT	Look up table
MIMO	Multiple-input multiple-output
MLL	Mode locked laser
MUX	Multiplexing
MZI	Mach Zehnder interferometer
MZM	Mach Zehnder modulator
NRZ	Non return zero
OA	Optical amplifier
OADMs	Optical add-drop multiplexer
ODL	Optical delay line
OLUT	Optical look up table
OMA	Optical modulation amplitude
OSA	Optical spectrum analyzer
OTDL	Optical tunable delay line
PC	Polarization controller
PCB	Printed circuit board
PIC	Photonic integrated circuits
PID	Proportional integral derivative
PLC	Planar lightwave circuits
PM	Power meter
PMF	Polarization maintaining optical fiber
PRBS	Pseudorandom binary sequence

PWM	Pulse width modulation
PZT	Lead zirconate titanate
QIP	Quantum information processing
QIS	Quantum information science
QKD	Quantum key distribution
R-OMA	Relative optical modulation amplitude
RC	Resistance-capacitance
SFWM	Spontaneous four wave mixing
Si_3N_4	Silicon Nitride
SiO_2	Silicon oxide
SISO	Single input single output
SOI	Silicon on insulator
SPD	Single photon detectors
SPDC	Spontaneous parametric down conversion
SPI	Serial Peripheral Interface
SSPD	Superconducting single photon detector
SW	Switch
SWW	Silicon wire waveguide
TFT	Thin film transistor
TIA	Time interval analyzer
TPI	Two-photon interference
UMZIs	Unbalanced Mach-Zehnder interferometer
USB	Universal Serial Bus
VOA	Variable optical attenuator
WDM	Wavelength divison multiplexing

Chapter 1

Introduction

1.1   Motivations and Aims

Electronics and photonics are at the heart of the internet technologies which have become an integral part of our society. The term electronics refers to use of electrons to manipulate, or process analog and digital information. Photonics is the study of light or photon manipulation, involving generation and detection through emission, switching, amplification, detection, transmission and information processing. At the heart of all of these devices are numerous control circuits which manipulate, or process, the information. Data centres, cloud computing, social media and high speed internet access are all examples of applications which heavily rely on both electronics and photonics. Other less ubiquitous, but no less important, technologies include quantum information processing for secure communication, computation and quantum teleportation.

Electronic-photonic integration, an emerging technology combining mature electronics engineering and integrated photonics, has great potential to be applied in a diverse range of applications from communications to quantum technologies. However, it has been challenging to develop reliable and accurate electronic photonic integrated circuits, such as in systems using thermooptic and electrooptic effect. Fast electrooptic switches have many applications, mostly used in Lithium Niobate but can also be realized in Complementary Metal-Oxide Semiconductor (CMOS) compatible silicon. Thermooptic effect is slower but useful for reconfigurable circuits. In thermooptic systems, silicon based material is used to realize photonic integrated circuits because of its compatibility with low cost CMOS process. However, this material has a high thermooptic coefficient making it is prone to thermal crosstalk [3]. In electrooptic systems, electrooptic switches are used for controlling photon generation in order to create more deterministic single photon sources have been proposed [4]. The challenges for such systems are to realize efficient and accurate switch

timing between electronic and photonic devices. Another challenge is due to manufacturing incompatibilities between electronics and photonics. Thus, electronic-photonic chips typically contain only few optical devices adjacent to simple circuits and constrained to niche manufacturing processes [5]. All these challenges require robust, low power, compact and high performance integrated systems.

The main objectives of this thesis are to address above the above mentioned challenges to achieve reliable, low power, high performance and compact integrated electronic photonic systems in a number of particular applications.

1.2   Contributions

In order to achieve these goals, techniques for improving integrated systems have been investigated and the contributions of the work include the following:

- A novel integrated time bin entanglement system [6].

- A unique integrated controller circuit for wavelength stabilization [7].

- The first demonstration of more deterministic photon sources with active temporal multiplexing [8].

- A novel algorithm for multiple-input and multiple-output control for photonic integrated circuits [9].

- A novel monolithic segmented Mach Zehnder transmitter design [10].

1.3   Organization of the Thesis

Chapter 2 provides background for understanding the origin of electronic and photonic circuits. Electronic and photonic integration is considered in detail in the context of hybrid integration and monolithic integration.

Chapter 3 deals with a time-bin entanglement experiment silicon nitride chip. The principles, circuits and implementation with two photon interference measurement are described in detail. Different voltage resolutions are tested to confirm the calibration of a Mach Zehnder Interferometer and quantum interference.

Chapter 4 presents the use of unique integrated system controller with hardware for dynamic thermal control. The technique uses an infrared sensor as feedback input from photonic chip and is embedded with the control system. The implementation of robust control

is determined from a measured transfer response and is modeled to achieve tunable control parameters.

Chapter 5 presents the use of FPGAs for controlling an electrooptic switch in active temporal multiplexing experiments. The interface and accurate timing control for electronic and photonic devices are designed and measured to achieve high coincidence to accidental ratio of generated photon pairs. Single photon outputs with temporal multiplexing are compared to output without multiplexing and spatial multiplexing technique.

Chapter 6 provides multi control photonic integrated system for MZI structure that applied in silicon nitride photonic integrated circuits. The multi control algorithm is described in detail with dual proportional integral reference tracking technique for wavelength stabilization experiments.

Chapter 7 presents monolithic CMOS nanophotonic device characterization in terms of performance and energy efficiency. Two segmented Mach Zehnder transmitter designs and the drivers are explained in detail.

Chapter 8 provides a summary of the work, and discusses future directions for research.

Chapter 2

Background

2.1 Introduction

This chapter begins by describing the foundation on which the research in this thesis is based. In particular a description of how electronics, photonics, hybrid integration, monolithic integration and applications in quantum and telecommunications relate is presented. The work in this thesis involves all of these research fields.

2.2 Historical Background

Electronic-photonic integration deals with the application of electronic integrated circuits and photonic integrated circuits. Electronic devices are concerned with applying the properties of electrons and optical devices are used to process, transport and generate photons. In electronic-photonic integrated systems, electronic devices offer extremely high density and memories are easily constructed, photonics enables high bandwidth, and can operate at frequencies several orders of magnitude higher than electronics. This has enabled the demonstrations of circuits with record functionalities. High speed internet access, wireless communication system with ultra high data rates and high performance computing are some of the breakthroughs achieved through the unique combination of photonics and electronics.

2.2.1 Electronic Integrated Circuits

Electronics, perhaps more than any other field of technology, is one of the great success stories of the 20th century. This technology has changed modern living and became an integral part of our society. One of the revolutionary device of electronics is the integrated circuit or IC. IC is a device which integrate many sets of functionalities and electronic circuits

on one chip of silicon. It is small size and low cost [11], thus shows an unlimited number of opportunities to be applied in variety of applications such as military [12], consumer electronics [13], telecommunication [14], astronomy [15], biology [16] and quantum [17].

The enabling technology behind the IC was the invention of transfer resistor, or transistor, in 1947 by William Shockley and his colleagues at Bell Laboratories, Murray Hill, New Jersey pave the way in the solid-state era of electronics [18]. This invention proved that electronic circuits could be made incredibly smaller, required much less power and more reliable than vacuum tube technology. Based on this invention, Shockley and two Bell Labs colleagues, John Barden and Walter Brattain were awarded the Nobel Prize decade later. This breakthrough was quickly followed by the invention of IC using planar transistor [19] by Jack Kilby, research engineer at Texas Instruments in the late 1950s. He introduced the concept of integrating device and circuit elements onto a single silicon chip. This planar transistor was the origin of density doubling law known as Moore's Law. Integrated circuit with planar transistors reveal the potential for extending operating and cost benefits of transistors to mass-produced electronic circuits, laying the foundations for the field of microelectronics. As the requirement of electronic applications increasing, Gordon Moore recognized that products developments was needed for larger transistor integration. Metal-oxide semiconductor (MOS) technology [20] appeared as the most effective technique to achieving larger scales of integration [21]. During this time, the most significant product to be introduced was microprocessors [22]. This started the tremendous coupling of IC and software technology. However, power dissipation was becoming important issue in IC by the mid-1980. The solution, was to apply complementary metal-oxide semiconductor (CMOS) technology. This technology reduces the standby power dissipation in logic circuits to almost zero [21]. The CMOS technology rapidly became the standard of very large scale integration (VLSI) design. Following Moore's Law, over the years, the sizes of transistor have reduced from 10s of microns in the early 1970s to up 10 nanometers in 2017 [23].

After the successful of IC for electronic devices, there have been many attempts of integration to other technologies to obtain the same benefits of compact and low cost IC. The other technologies include integrated sensor [24], microelectromechanical systems [25] and integrated optics [26]. These integrated systems can be found now in our daily life such as inkjet printer, smartphone, smartwatch, etc.

In most applications, feedback control can be found in integrated system to enable stable, accurate and high performance system. One of the most commonly industrial used feedback control techniques is Proportional-Integral-Derivative (PID). The term feedback denotes a situation in which two or more dynamical systems are connected together with each affecting the other with coupled dynamics. A dynamic system is a system which changes over

time, in many cases in response to an external force or stimulation [1]. The PID controller input/output relation with error feedback is described in equation 2.1.

$$u = k_p e + k_i \int_0^t e(\tau)d\tau + k_d \frac{de}{dt} = k_p(e + \frac{1}{T_i} \int_0^t e(\tau)d\tau + T_d \frac{de}{dt}). \tag{2.1}$$

Fig. 2.1. shows u as the control signal, e as error and r is the reference signal. τ is the variable of integration which takes on values from time 0 to the present t. The control action is the sum of three terms: proportional feedback, integral term and derivative action. The parameters for this control action are k_p as proportional gain, k_i as integral gain and k_d as derivative gain. S is the complex frequency of the transfer function in the Laplace domain. The two time constants T_i (integral time) and T_d (derivative time) are sometimes used as alternative of integral and derivative gains.
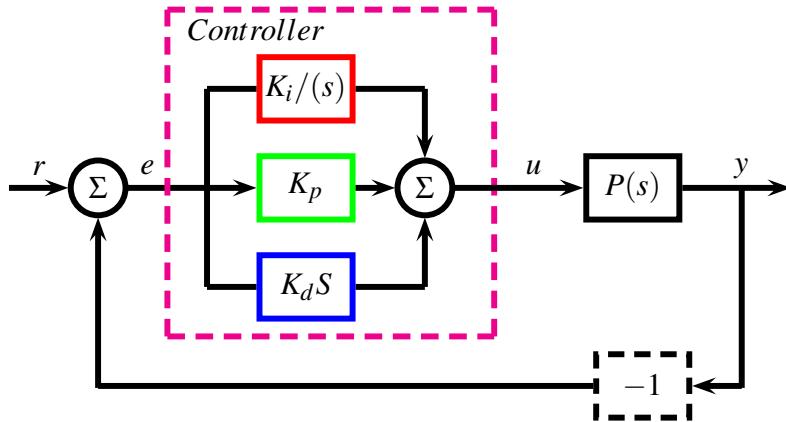
Fig. 2.1 General PID closed loop system diagram adopted from [1]

The race to innovate has led to unprecedented progress since the inception of the electronics industry. Today, many applications require different electronics platform for specific system and need to be optimized in term of cost, performance and flexibility. Implementation in software using basic electronic platform for computing such as general purpose processors or GPP (Intel core, ARM, AMD), application specific processors (digital signal processor, network processor) and micro controller (AVR, 8051) give more flexibility. However the performance of this system is usually low. Another option is to use massive paralllel processing electronics device such as Graphical Processing Unit (GPU) which offer better performance. Implementation in hardware with custom circuits or ASICs (Application Specific Integrated Circuits) provide even higher speed of operation, lower power dissipation and lower cost but with it comes less flexibility and no programmability. On the other hand, programmable electronics devices such as Field Programmable Gate Arrays (FPGAs) [27] offer high flexi-

bility by allowing flexible logic inside the device to be interconnected to implement arbitrary digital circuits. This type of device provides realization of relatively large logic circuits up to million equivalent gates in size. FPGAs are used today in many various applications, such as test equipment, consumer products like DVD players and high-end television sets, controller circuits for automobile factories, computer equipment like large tape and disk storage systems, internet routers and high-speed network switches. FPGAs contains three main types of resources: I/O blocks for connecting to the pins of the package, logic blocks, and interconnection between switches and wires. Programmable connections exist in all of the resources.The interconnection wires are structured as horizontal and vertical routing channels between rows and columns of logic blocks and organised in a two-dimensional array. The routing channels consist of wires and programmable switches that enable the logic blocks to be interconnected in many ways. These make this device very competitive in aspect of balance between flexibility, speed, power efficiency and development cost.

One of keys to the long-term success of the electronic computing community, and in particular of the hardware and software, has been open source licensing. Open source platforms such as Raspberry Pi [28] and Arduino [29] enable research and development at modest cost, allowing anyone to do cutting edge, creative work in a process that can instantly go into large-scale production. These open source platforms nowadays also contained FPGAs and powerful mobile processor such as ARM core processor. Countless successful companies have been formed by leveraging these platforms. What has emerged is a vibrant community of companies and academics using the open source hardware and software library that have been developed over the past 25 years in the electronic computing industry, and repurposing them to build electronic system prototypes. The promise of open source hardware and software not only lies in open libraries but also on integrating multiple functions into a single system enabling rapid prototyping, and verifying all the functionalities before integrating these into system on chip or chip stack. Doing so has radically driven down the cost of research and development, and will create the opportunity for a variety of fundamentally new applications of electronics and photonics, where high complexity systems can be built at very modest cost.

2.2.2 Photonic Integrated Circuits

Optics is the science of light which include physical optics, nonlinear optics, quantum optics and nano-optics while photonics is the technology of detecting, generating or controlling light and other forms of radiant energy which quantum unit is the photon [30]. Photonics usually involves the interplay between electronics and optics. This technology has been applied in diverse applications such as defense (laser weapon), energy (solar cells), medicine

(laser surgery), sensing (fiber sensor), data storage (CD/Blu-ray), entertainment (laser shows), bio (optical tweezers), nano (integrated photonics), space science (adaptive science), human-machine interface (CMOS camera) and communication (fiber optic communication).

The Nobel Prize award 2009 in Physics to Prof. Charles Kao regarded as the "father of fiber optic communications" emphasizes the great changes in modern society. Fiber optics have played a main role in initiating the Information Age and has changed the way we receive information and communicate. Fiber optic communications systems use lightwaves in the near-infrared region of electromagnetic spectrum (from about 800 nm to 2500 nm). Theoretically, in free space (i.e air or vacuum) c or speed of light = 3 x 10^8 m/s which derived from frequency (υ) x wavelength (λ) as shown in equation 2.2.

$$c = \upsilon \; x \; \lambda \qquad (2.2)$$

One of the important parameter used in telecommunication is power in decibel (dB). This is the ratio between two values expression in logarithmic unit of a physical quantity, often power or intensity. In optical fiber communication the relationship between power and decibel unit is 0 dBm = 1 mW. Therefore, positive values of dBm are greater than 1 mW and negative values are less than 1 mW. The decibel (dB) unit is defined by equation 2.3.

$$dB = 10 \log \frac{P_{out}}{P_{in}} \qquad (2.3)$$

In computing, photonics is used for chip-to-chip optical interconnects and on-chip optical interconnect communications. In order to enable photonic interconnect communications, it uses several components such as laser diodes, modulator, optical fibers, optical amplifiers, Wavelength-Division Multiplexing (WDM) components and photodetectors. In electronics, electrical interconnect (copper) provides resistance-capacitance (RC) delay, bandwidth limitation($\sim$5GHz) and higher power consumption compare to optics. Optical interconnects can give high bandwidth (> 40 Gb/s) with relatively low power consumption using Wavelength-Division Multiplexing (WDM) [31]. WDM means many independent data channels in the same fibre or waveguide, using different wavelength. In high performance interconnects applications, Dense Wavelength-Division Multiplexing (DWDM) is used with dozens of wavelength per waveguide. Simulation and experimental results suggest that it can provide bandwidth density on the order of 320 Gb/s/μm at only 250 fJ/bit resulting improvement of energy efficiency over optimized electrical interconnect [32]. Optical interconnect is motivating new field in research and development of "silicon photonics".

While research into integrated photonic has been active for the past two decades, its application to real-world systems has gathered serious attention only in the past couple of
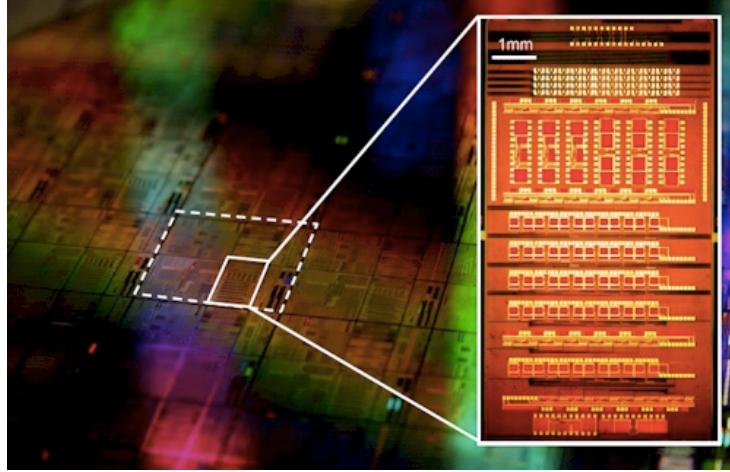
Fig. 2.2 Photonic integrated circuit IBM chip. With permission.

years. The main obstacle in this regards was the fact that the past majority of integrated photonic systems demonstrated to date relied on discrete components, occupying large volume, suffering from reduced reliability due to various interconnection; and requiring cost for packaging. This situation is somewhat reminiscent of photonic in the early twentieth century. In the last few years, many more essential components have been integrated onto chips, leading to more complex architectures and functionalities.

Most photonic integrated systems, whether they are performing some signal processing function, or simply transferring information as in an optical link, make use of the same basic components. One definition of photonic integrated circuits is the use of optical component and technique with integration for processing optical signals. The most common component to perform optical signal processing in photonic integrated circuits are waveguides, splitters and fibre couplers. From these basic components, photonic integrated circuits designers can build Mach Zehnder Interferometer (MZI) and ring resonators which, in turn, can be used to build photonic switches, filters, modulators, etc [33].

In the same way, integration of photonic circuits is the key to bringing these technologies into large scale applications. First, the possibility of integrating all circuit elements onto a single chip would reduce inter-component coupling losses, which is of utmost importance for increasing the system link gain as well as achieving a more energy efficient circuit. Second, photonic integrated circuits need significantly less packaging together with the possiblity for large scale production would significantly drive down manufacturing costs. In addition, the inherently low size and weight benefits of photonic integrated circuits would make them attractive in a vast range of applications, such as in telecommunication and quantum. All of these would be additional benefits to CMOS compatible processing capability of producing photonic integrated circuits.

2.3   Integration

The 21st century saw two major advances which changed the way human communicated, the first was brought about by the use of internet for communication. The second progress was resurge in electronic and photonic circuit integration, brought about by scientific breakthrough which have had a major impact on the world as we know it today.

One of the dominant choice material for electronic photonic integration is silicon, mainly because the potential attraction of integration with electronics in a cost-effective manner. Such research began in the mid 1980s. Government through Defence Advanced Research Project Agency (DARPA) believed that highly developed electronics photonic integrated circuits will meet both military and commercial need. In 2004, DARPA microelectronics office made a major investment which also known as electronic photonic integrated circuits project (EPIC) to develop electronic photonic integrated circuits which consist of several teams. The teams were the BAE systems team (electronic warfare application-specific EPIC), the Lincoln Laboratory team (high resolution optical sampling technology), the Luxtera team (CMOS photonic technology), UCLA (nonlinear silicon photonics), California Institute of Technology (optical signal amplification in silicon), University of Michigan (CMOS-compatible quantum dot lasers grown directly on Si/SiGe), Translucent (low-cost buried photonic layer beneath CMOS), Brown University (all-silicon periodic nanometric superlattices toward a silicon layer) and Stanford University (germanium quantum wells on silicon substrate for optical modulation) [34].
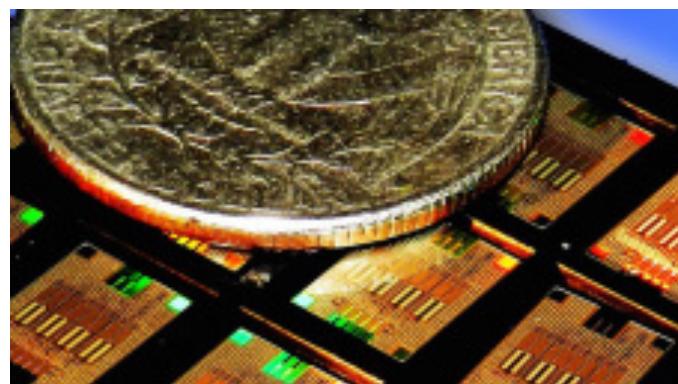
Fig. 2.3 Monolithic chip of IBM silicon photonic transceiver. With permission.

Industries are now motivating electronic photonic integration field forward at an acceler-ated rate. Intel, IBM, Cisco and many big companies, foresees a cost-driven transition to optical interconnect that could revolutionize enterprise networks and servers. These compa-nies chose to invest in electronic photonic integrated circuits because it could enabling cost

effective ultrafast processing and alleviate electronic bottleneck in a new generation of chips and computers. This will link up computing and communication.

Integration approaches adopted different technique as summarised in Table 2.1. Monolithic refer to all-silicon fabrication or all-in group-IV heterostructures [35]. III-V and II-IV device bonded to Si illustrate hybrid (also known as heterogeneous integration). Both monolithic and hybrid integration are useful. We can select the type of integration depends on what is the requirement or need with the applications. Some of these options provide trade off in term of cost and performance. For both integration types, some of useful options are: electrical silicon laser on chip, an off-chip laser that optically pumps several silicon Raman laser on-chip, hybrid integration of electrical III-V laser on-chip, and off-chip lasers of various kinds that communicate via fiber optics with electronic photonic integrated circuits without laser. Another technique that has been developed recently by IBM team is using smart partitioning [36]. This technique maintaining enough electrical content on the photonics chip as is necessary for fully functional wafer level testing and chip disposition prior to assembly. Not only for optimize yield and minimize cost, smart partitioning can open up for use in a broader range of applications.

Table 2.1 Electronic photonic integration approach adopted from [2]

Integration type	Monolithic Front-end	Monolithic Back-end	Hybrid Flip-chip bonding
Operation speed	Higher	Lower	Lower
Assembly cost	Lower	Lower	Higher
Development cost	Higher	Intermediate	Lower
Challenge for integration	Harder	Harder	Easier
Available waveguide	SOI, bulk-Si	SiN, a-Si	SOI

2.4   Recent Trends

Recent works to resolve manufacturing challenge for electronics and photonics has been demonstrated. In 2012, Orcutt et al. [37] presented device design methodology requiring zero process infrastructure changes. This enabled high performance photonic-electronic integrated circuits platform widely available. The challenges however still remain due material sensitivity to temperature and environmental change of the optical components.

Optical components must be stable under diverse circumstances in chip scale integrated system. Such systems required stable and accurate control to get high performance optical systems. In order to predict the heater effect, several model and simulation were proposed

to different photonic integrated system applications. In 2004, Xiao et al. [38] described a simple model to estimate the effect of environment temperature induced heater resistance change on the performance of MZI type variable optical attenuators. It is suggested that the effect of environment quite significant confirmed with experiment results. To minimize the effect, heater material with low temperature resistance coefficient can be selected, however it creates challenges on the heater fabrication and control. Automatic loop controller has been used as an alternative solution to this problem [39] and has been applied in diverse applications such as optical switch [40] [41], polarizer [42], resonator [43] [44], optical locking [45] and quantum state based optics generation [46]. Furthermore, in 2004, Harjanne et al. [41] demonstrated differential control method for fast switching in a SOI thermo-optic MZI. The switching speed can be directly determined by using properly heating voltage. This switch was driven with a digital signal processor equipped with simple electronic circuits. However, the speed is limited by the heater breakdown point, heat build-up and also the speed of controller circuit. Furthermore, in 2013, Palupi et al. [47] simulated the temperature effect of Wavelength Division Multiplexing (WDM) interleaver by using single and cascaded MZI.

Moreover, at higher bandwidth, optical ring modulators are sensitive to temperature or wavelength fluctuations causing wavelength misalignment, fabrication imperfections, laser wavelength drift and environmental temperature variation, thermo-optic tuning using active control is required for each modulator. In 2011, Qiu et al. [44] showed active feedback control of the resonant wavelength of a silicon dual-ring resonator. The control mechanism is based on thermo-optic tuning with micro-heaters. The feedback control design enables mirroring based electro-optic to be applied in a dynamic environment.

One of the common techniques for feedback control is proportional integral derivative (PID) controller as described in 2.2.1. This control algorithm has been used in photonics applications such as temperature controller of Fiber Bragg Grating sensors [48], distributed Brillouin sensor system [49], optical-fiber microwave delay [50], mirroring resonators [51], enhanced ADC applications [52], electro-optic modulator [53], phase shifter of optical beam [54] [55], and stable single photon interference [56]. Stability and precision are the key important parameters in these applications. Furthermore, many efforts have been attempted to find best performance of integrated photonic circuits of MZI based on thermooptic effect with various materials. There are AlGaAs/GaAs [57], Silicon on Insulator (SOI) [58–67], InGaAsP-InP [68], SiNi [43], Ge_xSi_{1-x} [69], crosslinkable fluorinated poly(arylene ethers) [70].

Several works utilize FPGAs as control devices for photonics applications. In 2012, Lentine etal [71] presented simulation and control loop implementation using FPGAs to

stabilize the resonant wavelength of an optical resonant modulator using bit error rate measurements. This scheme is used to control the optical wavelength that varies as a function of temperature and fabrication tolerances (dimension and thicknesses).

Moreover, one of the critical component in modern optical communication system is the optical add-drop filter (ADF). Basically, this is a building block for optical add-drop multiplexer (OADMs), wavelength division multiplexing (WDM) and reconfigurable (OADMs) in communication systems. In 2013, Zhu et al. [72] demonstrated integration of silicon photonics mirroring ADF with FPGAs as control interface. Result shows that the mirroring can be controlled with simple arrangement and with low driving voltage. This indicates the feasibility of the mirroring ADF as parts of power efficient photonic integrated circuits in the future.

Progress in optical interconnect technology is a positive indication to break the current trade-off between bandwidth and the capacity of electrical memory system interconnection, and to decrease the I/O power consumption. In 2013, Byun et al. [73] presented an optical interconnect transceiver chip for DRAM optical interface. The chip was fabricated on bulk-Si wafer using DRAM-compatible processes. The chip verification was performed by interfacing between a DDR3 DRAM and FPGA-based memory controller. Moreover, Beux [74] et al. proposed an implementation of reconfigurable photonics switching. Since high performance FPGAs computation capacity is related directly to proportional to the size and expressive to power of LUT (Look Up Table), Optical Look Up Table (OLUT) shows promise in the future design of FPGAs. This work adopted silicon photonics technology to replace a traditional LUT with an optical core implementation. The demonstration exhibits the potential of silicon photonics CMOS technology suited for optically assisted on-chip computation.

Many efforts in photonics integrated circuits implementation are advancing [75–80]. Furthermore, reference [81] reported an electronic-photonic system on a single chip integrating over 850 photonic components and 70 million transistors that work together to equipped with memory, logic and interconnect functions, using a standard microelectronics foundry process. This represents the new era of chip-scale electronic-photonic systems. Recent investment also has been started in 2016 that combine industries, government and universities efforts to build advanced electronic photonic manufacturing capability which also known as American Institute for Manufacturing Integrated Photonics (AIM) program. With this potential, broad range of applications could benefits from this technology and program in order to create small, low power and lightweight device. In addition of high bandwidth and energy efficiency advantages, photonics also proposed as one physical representation of quantum computing.

2.4.1 Quantum Applications

In physics, a quanta is the smallest unit of physical matter involved in an interaction while Quantum Information Processing (QIP) employs quantum mechanics for information storage, computation and communication. It enables improvement in communication and computational efficiency by utilizing non-classical correlations of quantum mechanics and superposition principle. For instance, a quantum computer utilizes quantum effects such as entanglement or superposition to perform operations on data. In classical bit, data represented by 0 or 1. On contrary, quantum computer uses quantum bits (qubits) which can represent a superposition of possible states 0 or 1 or quantum superposition of 0 and 1. For instance, 3 bits in classical computation indicates exactly one state, one number between 1 until 8. However, with 3 qubits, it denotes up to 8 states simultaneously. By encoding a qubits, the state of the qubits could be presented in either quantum states $|0\rangle$ or $|1\rangle$. Generally quantum mechanics permit the qubits pure state to be in some complex linear combinations. Both of the states are given by the equation 2.4. A geometrical representation for qubit states denoted by a Euclidean 3-D sphere know as Bloch sphere [82].

$$|\psi\rangle = cos\theta\,|0\rangle + e^{i\phi}sin\theta\,|1\rangle \qquad (2.4)$$

For quantum digital logic design, qubits are manipulated by quantum gates similar as AND, OR and NOT gates manipulate bits. Quantum gates represented by Hadamard, Phase Rotation and Controlled Not [83]. In quantum computer, qubits stored in quantum register (qregister). This storage is illustrated by a wave function where the coefficients are complex numbers whose amplitudes squared are the probabilities to quantify the qubits in each state. The complex numbers shows the phases that can constructively and destructively interfere.

To start with quantum computation, first n-qubit register initialized with starting values. For each step, n qubits go into and out of quantum gates. Quantum measurement is applied in order to read quantum information in qregister which will produce random n-bit string. The probability distribution of string is switched in favour of the right answer. Because quantum computers are probabilistic, multiple runs with majority polling of the outputs are required to produce the right answer with high probability. However, the results are not deterministic. Despite this problem, by rerunning until probability of error is less than an acceptable value, correct answers can be obtained.

Theoretically, quantum computing can be applied to database search problem such as searching for an entry in an unsorted array, guessing password and attacking symmetric ciphers for example AES. Furthermore, compared to classical run time which is O(N), linear search with Grover's Algorithm takes O($\sqrt{N}$) using O($log_2 N$) qubits of storage with

probability of measuring wrong answer $O(\frac{1}{N})$ [84] . Another example in quantum computer is Shor's Algorithm [85]. This algorithm takes $O((logN)^3)$ time to factor the integer N, faster than the best classical time $O(2^{logN})$. In 2001 [86], a team at IBM implemented Shor's algorithm and factored 15 using 7 qubits. The experimental of this algorithm was employed nuclear magnetic resonance. It used seven spin-$\frac{1}{2}$ nuclei in a molecule as quantum bits and manipulated in room temperature liquid-state nuclear magnetic resonance techniques.

In quantum photonic based systems, single photon sources are essential to many experiments in quantum information science as well as efficient quantum computation [87] [88]. Several of experimental effort are in progress to make productive sources of indistinguishable single photons such as complex setup in high vacuum and cryogenic temperatures. However, these setups not directly fit for scalability. Recently, Silicon-On-Insulator (SOI) integrated photonic circuits are able to implement high fidelity multiqubit operations [62] [89]. This platform also has a number of benefits including scalability, on-chip integration of state-of-the-art electronics, electro-optic switching and optical interconnect system [62, 90–92].

Quantum effects are specifically not difficult to observe in optical systems. One of the approach for QIP uses photons to implement quantum logic [93]. In quantum state generation, the Mach Zehnder Interferometer (MZI) can be used for generating qubits. In typical MZI, configuration uses two beamsplitters. The first beamsplitter splits an optical signal into two coherent waves that go along paths with different effective length. Second, it remerge and superposes two waves, directing to quantum interference fringes in the evaluated output signal.

2.4.1.1   Time Bin Entanglement

One of the main sources for quantum information such as communication system over optical fiber and quantum computer is entanglement [94] [95] . This main source describing nonlocal behaviour of correlated systems which quantum state unable to fully represent individually. Time-bin entangled photon pairs is a coherent superposition of two pair photon states located at different temporal position by using a coherent double pump pulse through Spontaneous Four Wave Mixing (SFWM) [96].

One of a metric to characterize the signal-to-noise ratio of a photon source is Coincidence-to-Accidental Ratio (CAR). The CAR can be expressed as the coincidence rate per pulse of function of C in equation 2.5. The η_I and η_S are the idler efficiencies and the net signal for each channel, and d_I, d_S the dark count rates per pulse in the dark and signal detectors [97]. In SFWM, the idler and signal photons were inserted into an optical band pass filter (BPF) to further reduce the pump photons. After this process, photons launched into 1-bit delay

Mach-Zehnder interferometers [98]. By controlling the temperature of the interferometer, the phase different between the two path can be adjusted.

$$CAR = \frac{C}{(\frac{C}{\eta_S} + d_I)(\frac{C}{\eta_I} + d_S)}$$

(2.5)

In 2008, Harada et.al [91] observed high-purity correlated and entangled photon pairs created through Spontaneous Four-Wave Mixing (SFWM) in a silicon wire waveguide. They reported CAR around 200 and time-bin entangled photon with $> 95\%$ visibility without substracting the accidental coincidences. Promising alternative device to process this is silicon nitride waveguide. The advantage of this device is 100 times more compact than silica waveguide.

2.4.1.2 Temporal Multiplexing

One of the most commonly used methods to generate photon in Quantum Information Science (QIS) applications is Spontaneous Parametric Down Conversion (SPDC) [96]. Heralded Single Photon Source (HSPS) based on SPDC is an alternative approach for generating on-demand single-photon sources [97]. In this scheme, a pair of photons is produced from a nonlinear crystal pumped by a laser. However, because of significant order emissions probability drastically reduce the quality of HSPS [99], single SPDC source is basically limited. This limitation can be overcome by using temporal or spatial multiplexing of several sources [100–102].

There are two advantages of spatial multiplexing technique in generating single photon. It can improve one-pair generation probability and signal-to-noise ratio of an m-SPDC array similar to a 1-SPDC source. Simple temporal multiplexing scheme with theoretical simulation shows reducing the number of higher order photon events from heralded single-photon sources based on SPDC [103]. Furthermore, Ma et al. [99] presented simulation indicates that photon based on multiplexing of four SPDC sources can perform better than the heralding based on highly advanced photon-number-resolving detectors. Moreover, in 2011, Mower and Englund presented scheme for generating on-demand, indistinguishable single photon using active temporal multiplexing [4]. The simulation exhibits single photon generation efficiency over time-multiplexing protocol by assuming existing fabrication capabilities. However, the result has limited to simulation, not with real system implementation.
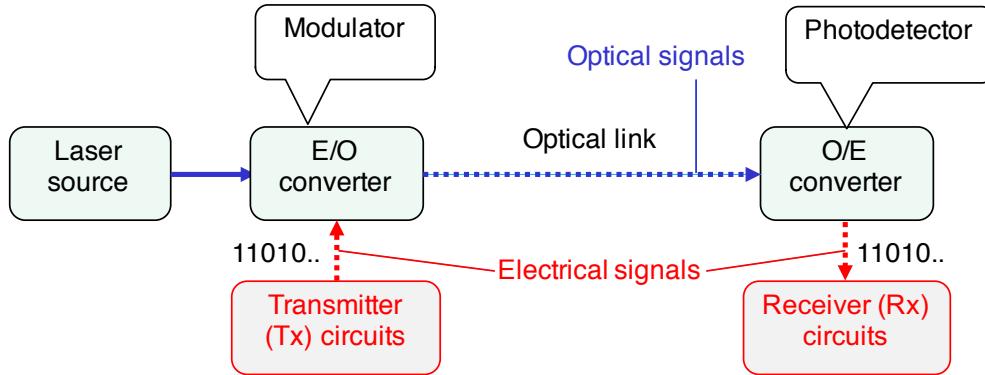
Fig. 2.4 General communication block diagram

2.4.2   Optical Transceiver Applications

In telecommunication, general transmission link in optical communication consist of several components including laser that provide modulation source and the external modulator device as shown in Fig. 2.4. From this figure, external modulator transmitter is connected with optical link and receiver with optical to electrical converter.
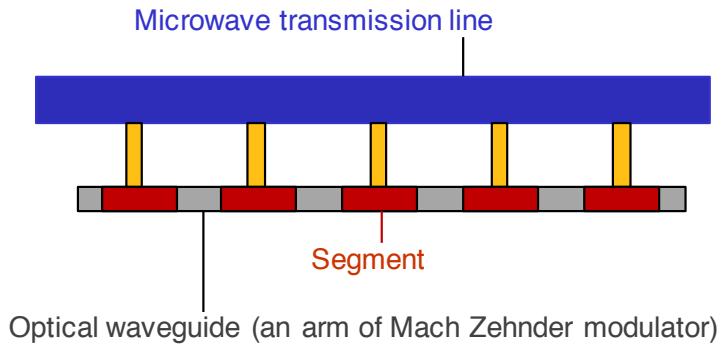
Fig. 2.5 Segmented modulator design concept

One of the key consideration for designing transmitter in optical communication link is using segmented technique where the optical waveguide in an arm or both arm in Mach Zehnder modulator is segmented to the connection of microwave transmission line as shown in Fig. 2.5. This method enables velocity matching which is important in high speed system, minimizes parasitic capacitance therefore reduces the overall energy consumption, and also enables extended modulation bandwidth [104]. Because of this advantages, recently many researchers applied this technique to their design consideration. For instance, Temporiti et al. demonstrate a hybrid (different material combination) 55 nm BiCMOS transmitter based on segmented Mach Zehnder design [105]. Furthermore, Lopez et al. from IHP also

recently present hybrid (different material combination) silicon germanium electronic driver with indium phosphide photonic circuits [106]. In addition, hybrid (separate silicon chip die) integrated circuits also has been demonstrated recently by IBM team using segmented design [107]. Hybrid technique enable designer to focus on the optical and electrical functionally independently. This approach also permits optimizing the best chip technology for each purpose. However, due to separate electrical and optical circuit design environments, hybrid integration poses another challenge in co-optimization of the component. Recently monolithic integration with segmented design has been demonstrated in silicon germanium platform by Rito et al. from IHP [108]. In monolithic design, the co-optimization of component is very natural due to a single design environment enabled for both electrical and photonic components [109].

2.5 Summary

This chapter reviewed recent advances in electronics, photonics and their integration. It collected the prior art related to this thesis.

Chapter 3

An Integrated Time Bin Entanglement System

3.1 Introduction

Entanglement is at the heart of photonic quantum technologies such as secure communication [110], super-resolution metrology [111], and powerful computation [112]. Photons are usually entangled in one of three degrees of freedom: polarization, optical path, or time bin. On-chip polarization entangled photon sources have been reported [113] [114], but only the components for photon generation were on-chip due to the difficulty of the integrating polarization analysis devices. Chip-scale optical path entangled photon generation and analysis [115] and teleportation [116] have seen rapid development, aiming for on-chip quantum computation. Time-bin entanglement is of particular interest because it (*i*) can be extended to higher dimensions for computation [117], (*ii*) is insensitive to polarization fluctuation and polarization dispersion, and therefore very promising for long-distance quantum key distribution (QKD) [110], and (*iii*) is naturally compatible with integrated optics: photons can be generated in nonlinear waveguides, and entangled and analyzed using on-chip unbalanced Mach-Zehnder interferometers (UMZIs) [91] [118].

For time-bin entanglement to be useful in the real world, the on-chip integration of the entire entanglement system is essential. High performance of the entanglement system not only relies on photon generation but also hinges on the compactness, scalability, and reconfigurability of the photonic circuit that prepares pump time bins, demultiplexes the photons, and analyzes the entanglement. References [91] and [118] reported photon generation from compact silicon devices, but the wavelength demultiplexing was off chip, and entanglement

analysis was based on silica waveguides, which have large bending radii due to their low index contrast. These features are incompatible with high-density integration.

In this chapter, we report a time-bin entanglement photonic chip that integrates pump time-bin preparation, wavelength demultiplexing, and entanglement analysis. Our demonstration was based on a high-index-contrast silicon nitride (Si_3N_4) circuit. The waveguide bending radii were reduced from millimeter (for silica) to micrometer scale while maintaining low loss, making high-density integration possible. Beyond compactness, the circuit offered tunability and stability, resulting in high performance: a two-photon interference (TPI) fringe with 88.4% visibility (without subtracting any noise) was measured.
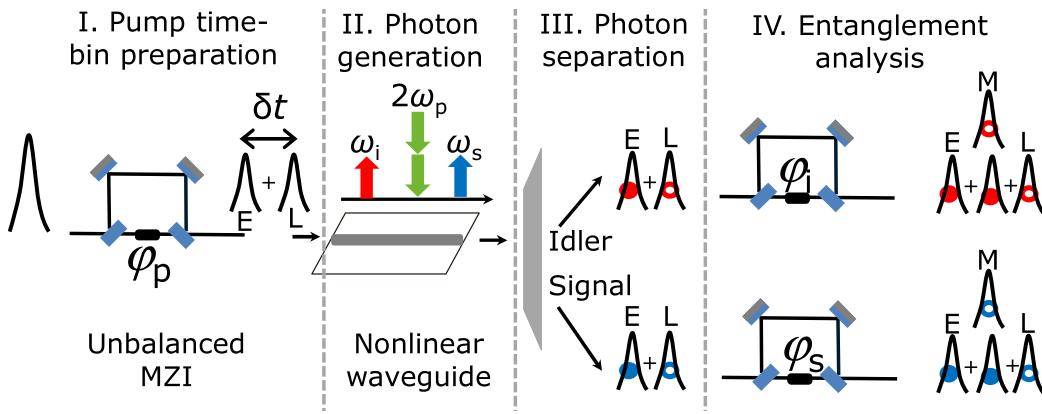
Fig. 3.1 Principle of time-bin entanglement generation

3.2 Time Bin Entanglement Working Principle

Fig. 3.1 shows the principle of time-bin entanglement generation involving four steps: (*I*) using an UMZI to generate pump "early" (E) and "late" (L) time bins with a relative delay of δ_t and phase difference of φ_p, (*II*) using a nonlinear waveguide to generate correlated photon pairs, called signal and idler, via a nonlinear process such as spontaneous four-wave mixing, (*III*) using wavelength demultiplexers to remove pump and separate photon pairs, and (*IV*) using another two UMZIs identical to the first one for entanglement analysis. In step (*II*) the pump power is controlled so that photon pairs can only be generated either in the "early" or "late" time bin, both with a probability of 50%. This forms a superposition state $1/\sqrt{2}(|E\rangle_2|E\rangle_i + e^{j2\varphi_p}|L\rangle_s|L\rangle_i)$, namely, time-bin entanglement. In step (*IV*), when the "early" photons pass through the longer path and the "late" photons pass through the shorter, nonclassical TPI will occur in the "middle" (M) time bin because the "early" and "late" photons are indistinguishable [91] [117] [118].

To generate high-quality time-bin entangled photons and achieve high-visibility interference, three requirements must be met. First, the relative delay between the two time bins must be longer than the minimum of the pump pulse width, photon coherent time, and resolution of the detection system. This arrangement can avoid single-photon interference and ensures that the detection system can distinguish different time bins. On the other hand, a long delay will reduce the bit rate for quantum information processing and can also introduce additional propagation loss. The second requirement is that the relative phase difference $\varphi_{p,s,i}$ between the longer and shorter paths must be stable, and the path length difference of the three UMZIs must be almost equal (errors within the coherent time of laser pulses); otherwise, interference will not occur. The third requirement is that the probability of photons appearing in each time bin must be equal to 50% to maximize the interference fringe's visibility. Photonic integration can meet all of these requirements.
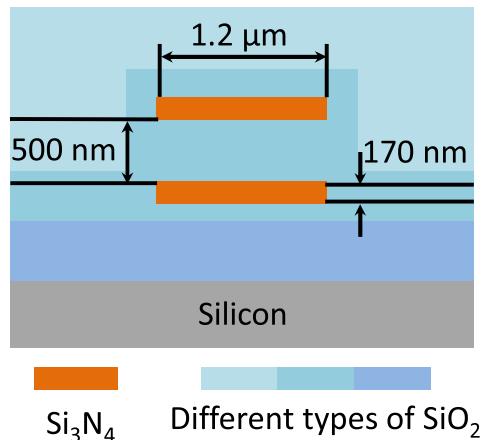
Fig. 3.2 The cross section of the Si_3N_4 waveguides

3.3 Photonic and Electronic Control Circuits

3.3.1 Silicon Nitride Photonic Integrated Circuits

In our demonstration, we focused on integrating the components for steps (*I*), (*III*), and (*IV*) on a single chip (28 mm x 8 mm) to achieve the above mentioned phase stability, path length accuracy, and exact 50% probability of generating photons in each time bin. The circuit was made using the double-stripe Si_3N_4 TriPleX waveguide technology with LioniX BV [119] [120]. The waveguides consisted of two stripes of Si_3N_4 layers stacked on top of each other with SiO_2 as an intermediate layer and cladding. The stripes were designed to be 1.2 μm wide, and the Si_3N_4 layers and the SiO_2 intermediate layer were designed

to be 170 and 500 nm thick, respectively [Fig. 3.2]. This was optimized for single-mode operation at 1550 nm with a high index contrast, allowing a 125 μm bending radius with a propagation loss of < 0.2 dB/cm for TE polarization. At 1550 nm, the waveguide exhibits a group index of 1.715 and an effective mode area of 2.72 μm^2 (1.6 and 1.7 μm along the x and y directions, respectively). Spot-size converters were used at both ends of the waveguides to reduce the waveguide to SMF28 fiber coupling loss to around 1 dB per facet. A photograph and the schematic layout of the chip are shown in Fig. 3.3 and Fig. 3.4. The longer arm of the UMZIs was approximately 14 cm long and made in a spiral fashion, benefiting from the small bending radius offered by Si$_3$N$_4$. This gave a 795 ps delay relative to the shorter arm. The demultiplexers consisted of two slightly unbalanced MZIs (length differences are 73.1 and 146.2 μm) the first rejected the pump by varying phase φ_{f1}, and the second separated f1 signal and idler photons by adjusting phase φ_{f2}.
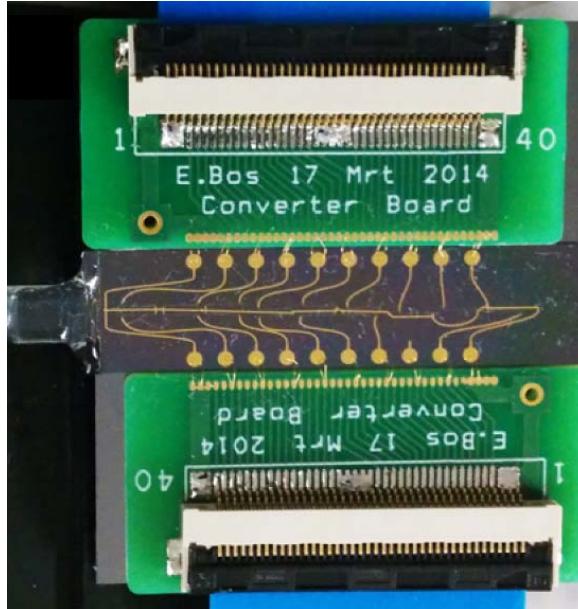
Fig. 3.3 A photograph of the Si$_3$N$_4$-based time-bin entanglement chip

All MZIs and UMZIs incorporated tunable couplers for input and output. Each tunable coupler was a balanced MZI having two directional couplers with a fixed ratio close to 50:50 and a phase shifter in one arm to achieve an arbitrarily tunable splitting ratio. Tunability was critical for generating and analyzing photons in two time bins with equal probabilities, and for achieving lossless demultiplexing. All phases were controlled through resistive heaters that were wire bonded [yellow lines in Fig. 3.3] to standard electronic printed circuit boards. Independent 16-bit digital-to-analog converters provided high-resolution control of 15 heaters on the chip. When a voltage (U) is applied, the temperature of the waveguide
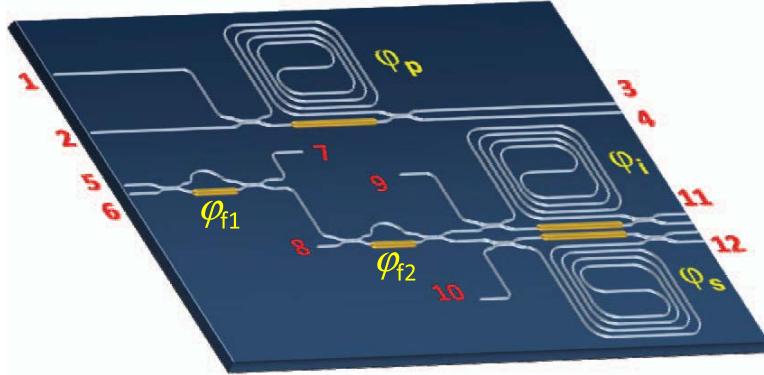
Fig. 3.4 The schematic structure of the photonic circuit on the chip

under the heater will exponentially increase to a maximum value determined by the power dissipated in the heater. Accordingly, the refractive index of the waveguide will increase, and this will introduce phase shift. This thermo-optic phase shift changes quadratically with U [116]. All waveguides, except the longer arm of the UMZIs, were a few millimeters long so that the heaters could be constructed on top to achieve any phase shift up to 2π while maintaining low loss and keeping within the dissipation limits of the heaters. All optical input and output ports of the chip were arranged to align with a waveguide array with a spacing of 127 μm and pigtailed to a polarization-maintaining fiber array [not shown in Fig. 3.4]. The white lines in Fig. 3.4 represent the Si_3N_4 waveguides, and the yellow lines are the resistive heaters. Only heaters for pump, signal and idler phase shift, and wavelength demultiplexing are shown. Each tunable coupler consists of a balanced MZI with a heater in one arm (not shown). In total there are 15 heaters on the chip. The numbers label the ports. A straight reference waveguide was included for alignment and coupling loss measurement during the pigtailing process. The total insertion loss of the 6.65 cm long reference waveguide was measured to be 4.5 dB.

3.4 Time Bin Entanglement Demonstration

3.4.1 Chip Implementation and Characterization

Prior to the quantum entanglement experiment, we characterized the circuit in the classical regime to ensure that the couplers and demultiplexers were set correctly. For the UMZI that was used to generate two pump time bins [Fig. 3.4, labeled by φ_p], we injected a pulse train with a pulse width of 10 ps at 1555.7 nm into input port 2 and monitored it from the two output ports 3 and 4 using a fast oscilloscope. Because of the delay in the longer arm,

we observed double pulses separated by 795 ps at each output. The early pulses from both outputs were from the shorter arm, and the late ones were from the longer arm. By adjusting the voltage applied to the heater for the output coupler, the amplitudes of the early pulses became equal, as did the late pulses when the output splitting ratio was exactly 50:50. This was independent of the input splitting ratio. As the pulses from the longer arm experienced higher loss, the input splitting ratio deviated from 50:50. By adjusting the voltage applied to the heater for the input coupler, the early pulses became equal to the late pulses in amplitude when the effective input splitting ratio was 50:50 after taking into account the longer arm loss.
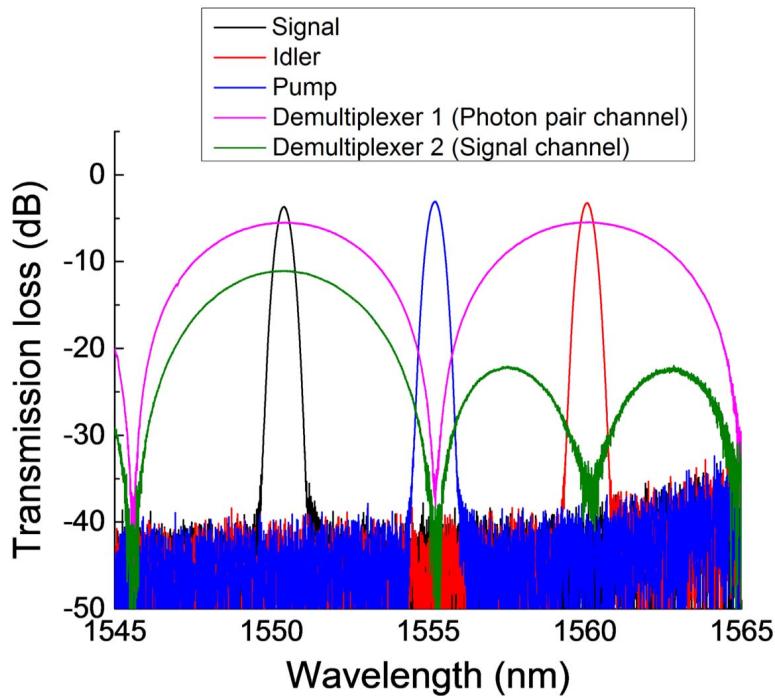
Fig. 3.5 Characterization of the wavelength demultiplexer

For demultiplexer 1 (labeled by φ_{f1}), which was used to reject the pump, we could not measure the two outputs because one output was connected to demultiplexer 2 (labeled by φ_{f2}) on the chip. To characterize it, we injected a broadband amplified spontaneous emission (ASE) source into port 7 and monitored the spectra at ports 5 and 6 using an optical spectral analyzer. By adjusting the voltages applied to the three heaters for the MZI, the spectra measured from ports 5 and 6 were complementary to each other, and the loss between ports 7 and 5 was 5 dB at the transmission bands (pink trace, Fig. 3.5) when the heaters were optimized. The loss was mainly due to waveguide-coupling and fan-out waveguide propagation losses, indicating nearly zero loss of the demultiplexer. The black, blue, and

red traces in Fig. 3.5 are the transmission spectra of three 0.5 nm bandpass filter (BPFs), indicating the signal, pump, and idler wavelengths used in our experiments. The pink trace shows the rejection of pump at the photon pair channel from demultiplexer 1, and the green trace shows the signal channel from demultiplexer 2. The isolation to the pump was at least 25 dB. Due to symmetry of a MZI, when we injected pump, signal, and idler to port 6 in the quantum experiment, the input from demultiplexer 1 to 2 kept the signal and idler photons and rejected the pump.

Because both outputs of demultiplexer 2 were connected to UMZIs on-chip, we characterized them (labeled φ_i and φ_s) using the approach for setting up the pump UMZI before we could optimize demultiplexer 2. For characterizing demultiplexer 2, we injected an ASE source to port 6 and monitored the spectra from ports 11 and 12. When all heaters for demultiplexer 2 were set correctly, the spectra from ports 11 and 12 showed a dip at the pump wavelength and were complementary at the signal and idler wavelengths. The green trace in Fig. 3.5 shows the spectrum taken from port 12, indicating very good separation of signal and idler channels. This loss spectrum shows that the total loss at the transmission windows of the whole circuit was approximately 11 dB, which comprised fiber-waveguide coupling loss, propagation loss in the longer arm, and a 3 dB loss in the UMZI output coupler. It should be noted from Fig. 3.5 that the MZI-based demultiplexers cannot do narrowband filtering, but can separate pump, signal, and idler very well. This is sufficient for performing quantum operations on signal and idler photons on-chip with off-chip narrowband filters placed before single-photon detectors (SPDs). Once the SPDs are on-chip, narrowband filtering on-chip is required, and this is possible with the TriPlex technology [120].

3.4.2 Two-photon Interference Measurement

After all the heaters were set in place, we performed the time-bin entanglement experiments. The setup is illustrated in Fig. 3.6 with blue solid lines are optical fibers, and black dashed lines are electric cables (BPF, bandpass filter; TIA, time-interval analyzer; SPD, single-photon detector). The pump was a mode-locked fiber laser emitting 10 ps pulses at 1555.7 nm with a repetition rate of 50 MHz. The pulses were injected into the first UMZI from port 2 for pump time-bin preparation. The output from port 3 of the UMZI was coupled to a 3 mm long, 220 nm high, and 460 nm wide silicon nanowire on another chip for photon pair generation. The output of the nanowire was sent back to port 6 of the on-chip demultiplexers, which rejected the pump and separated the signal (1550.9 nm) and idler (1560.6 nm) photons. Both outputs of demultiplexer 2 were connected to the UMZIs on-chip for entanglement analysis.
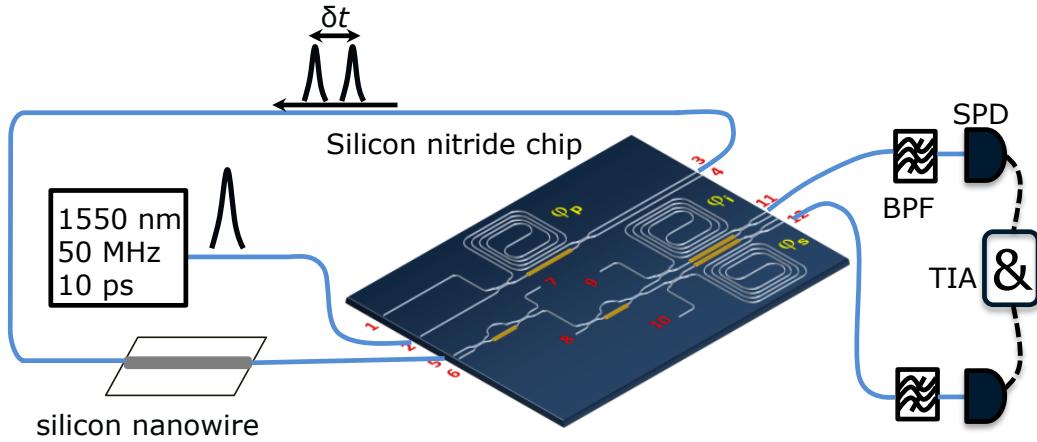
Fig. 3.6 Entanglement experimental setup

The signal and idler photons were coupled to off-chip bandpass filters through ports 12 and 11 to further remove the pump and be postselected in the 0.5 nm bandwidth shown in Fig. 3.5, before being detected by two InGaAs avalanche SPDs (ID210 from ID Quantique). The SPDs were gated by the 50 MHz laser clock, and the gates were aligned with the "middle" which shows interference time bin. The effective gate width was 1 ns. We used this SPD configuration to avoid the detection of photons from other time bins [91]. To minimize the dark counts and after-pulsing probability, the detection efficiency was set at 10% and dead time was set at 20 μs. The coincidences were analyzed by a time interval analyzer.

The coincidences were a function of $\cos(\varphi_s+\varphi_i+2\varphi_p)$ [91] and [118]. At the coupled peak power (into the silicon nanowire), when we fixed and φ_i (no voltage applied) and varied adjusting the voltage (U) applied to the heater, we observed an 86.8% visibility fringe, without subtracting any noise (Fig. 3.7, black squares). Black squares and red dots represent two nonorthogonal measurements when the voltage applied to the heater of the UMZI in the idler channel was set at 0 and 4 V, respectively. Fig. 3.7 shows coincidences as a function of the square of the applied voltage to the heater of the UMZI in the signal photon channel. The dashed lines are cosine fits. Poisson error bars are used. To confirm the entanglement, high visibility fringes must be observed in two nonorthogonal measurement bases [91] [118]. We thus slightly changed φ_i by applying 4 V to its heater and again varied φ_s, which resulted in an 88.4% visibility fringe (red dots) being observed. Both fringes exhibited high visibilities beyond the classical limit of 70.7% [121], clearly indicating that high-quality time-bin entanglement had been achieved.

While recording the coincidence measurements, we monitored the single count at each detector and observed that they were insensitive to $\varphi_{s,i}$ (Fig. 3.8), further evidence that the interference fringe was due to two-photon entanglement. Measured singles for the signal
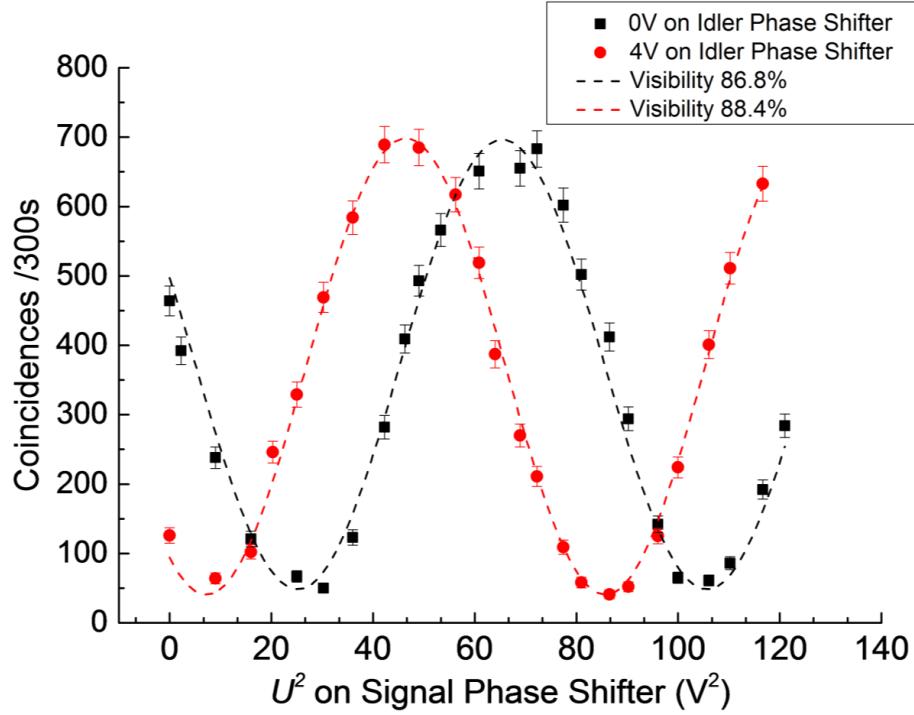
Fig. 3.7 Coincidences measurement result

(blue diamonds) and idler (red dots) channels at different applied voltages to the signal channel heater. Poisson error bars are used.

The visibility of an ideal TPI fringe should be 100%. Our demonstration shows a maximum 88.4% visibility because of accidental coincidences from a few noise sources. The first is the dark count of the detectors. The second is due to the small probability of producing multiple pairs. Finally, the third is due to the so-called charge persistence effect of the SPDs [122] [123]. This effect means when SPDs work at the gated mode, the photons that arrive at the SPDs will interact with the detector even though the gate is OFF. The interaction will trap electrons and produce a detection pulse once the gate is back ON in a few nanoseconds. In our measurements, we observed an extra small coincidence peak in addition to the main peak in the histogram, indicating the capture of photons from the early time bin even though the detectors were expected to only detect the photons from the middle time bin.

Although our demonstration did not integrate the nonlinear waveguide for photon pair generation on the same chip, recent progress has shown that it is possible to use Si_3N_4 nonlinear devices for photon pair generation [124], and such nonlinear devices can be made using the TriPlex technology [125]. In addition, a Si_3N_4 platform compatible with our circuit exhibits a fast stress-optic effect at > 1 MHz [126], indicating the potential of our circuit
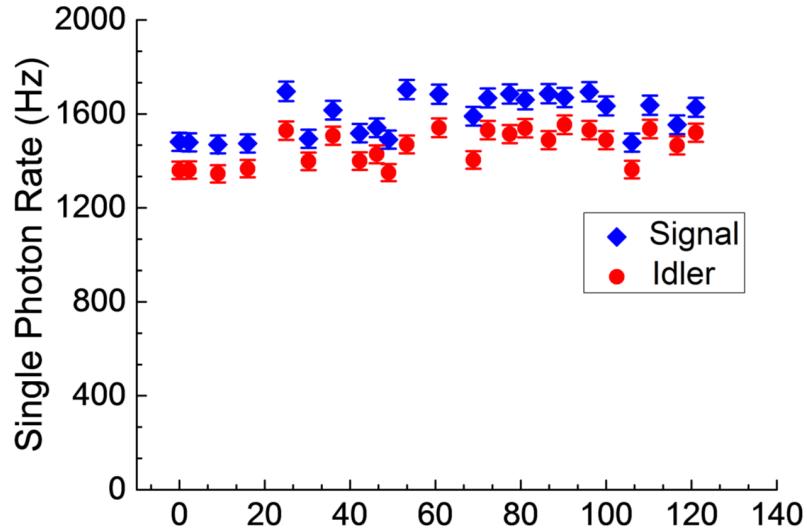
Fig. 3.8 Measured singles for the signal and idler

for operating at a much higher speed in the future for quantum information processing. Our demonstration clearly establishes that Si_3N_4 photonic circuits incorporating all four steps illustrated in Fig. 3.1 for time-bin entanglement are feasible. Once this technology is available, taking advantage of the reconfigurability of the circuit, on-chip time-bin entangled photons can be tested as demonstrated in this Letter, and then switched to port 7 for long-distance entanglement distribution by simply controlling the phase φ_{f1}. On the other hand, taking advantage of the compactness of the circuit, multiple time-bin entanglement sources and Bell measurement devices can be made on a single chip for on-chip time-bin qubit teleportation.

3.5   Summary

We have demonstrated a high-performance time-bin entanglement photonic chip based on Si_3N_4. This is a significant step toward the ultimate goal of completely integrating all components to realize chip-scale time-bin qubit transmitters and receivers for QKD, and integrating many entanglement sources and analysis circuits on a chip for large-scale quantum computation.

Chapter 4

Dynamic Thermal Photonic Controller

4.1 Introduction

Photonic Integrated Circuits (PIC) are a key technology for the practical realization of optical processing in applications as diverse as microwave photonics to quantum applications [80] [123] [6]. PIC using silicon based materials in a thermooptic system can be fabricated with relatively low cost in Complementary Metal-Oxide Semiconductor (CMOS) technology. However, the use of multiple heaters on a chip is prone to thermal crosstalk and environmental change because of the relatively high thermooptic coefficient of these materials [127] [3]. This creates undesirable wavelength shifts and affecting system performance. Multiple heaters in photonic integrated circuits must be controlled dynamically to achieve reliable performance of the thermooptic system.

Prior efforts to resolve thermal sensitivity of a thermooptic system have focused on differential control techniques [41], Wheatstone bridge with Proportional-Integral Derivative (PID) feedback [51], active feedback [44], mean power monitoring [128], dithering [129], and balance homodyne locking [130]. These all require external or on-chip photodetectors to monitor the traveling light in the resonators. The robustness, loop interaction and control are also hard to analyze and may not yield the best overall control.

In this chapter, we demonstrate wavelength stabilization in compact and low loss silicon nitride multi-heaters PIC based on Mach Zehnder Interferometer (MZI) structure. We demonstrate that a single-board low-cost microcontroller-based design can be used to implement a wavelength stabilization with external disturbance on silicon nitride PIC.

4.2 Thermooptic System Controller

4.2.1 Photonic Chip and System Controller

The silicon nitride circuits were fabricated using double stripe waveguide technology with LioniX BV [44]. The waveguides comprised of cladding and two strips of Si_3N_4 layers stacked on top of each other with SiO_2 as an intermediate layer. The strips were constructed to be 1.5 μm wide, and the Si_3N_4 layers and the SiO_2 intermediate layer were formed to be 170 and 500 nm thick, respectively. This allowed < 100 μm bending radius with a propagation loss of < 0.2 dB/cm for TE polarization and single mode operation at 1550 nm with high index contrast.
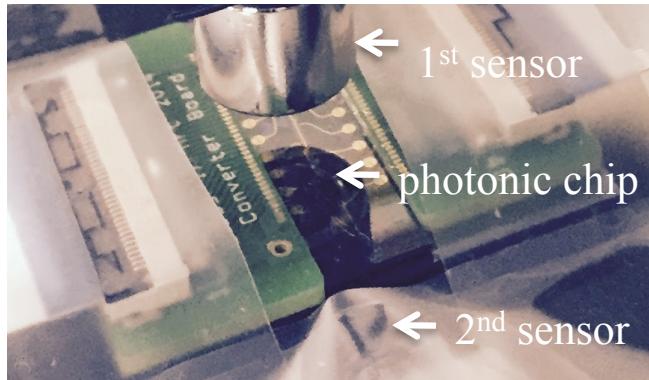
Fig. 4.1 Chip setup

There are 15 heaters inside the chip, each with a nominal resistance of 600 Ω. In this experiment, heaters were connected via electrical wire bonded directly to the heater controller as illustrated in Fig. 4.1. The chip temperature is monitored via an infrared sensor (first sensor), which collects the target chip and ambient temperature. The gap between chip and sensor is around 5 mm. The second sensor is attached on the heatsink plate to monitor overall temperature of the chip. This sensor is using TSIC™306 with T092 package. The photonic chip and sensor setup are shown in Fig. 4.1.

The heater controller, as shown in Fig. 4.2, consists of 16 channels outputs, and 15 of them can be used to provide power to the 15 heaters on the photonic chip. The hardware is designed specifically based on open source Arduino using ATmega32u4 with two 16-bit Octal Digital to Analog Converter (DACs), eight dual amplifiers and 16 voltage follower circuits integrated onto one board. These electronic circuits as shown in Fig. 4.3 can be scaled for more channel output. The hardware are controlled via SPI (Serial Peripheral Interface Bus). Since the circuit using dual Octal DAC, digital multiplexer is used for selection between two DACs. The voltage output of this controller can provide up to 30 V depending on the
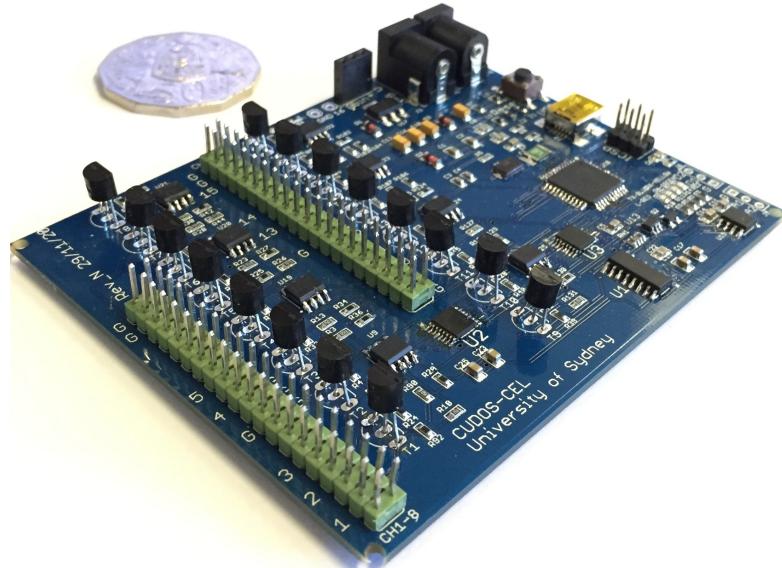
Fig. 4.2 Heater controller circuit board

amplifier circuits gain setup and voltage follower input. To prevent the damage of the Silicon Nitride photonic chip, the input was limited to maximum 20 V. The graphical user interface (GUI) for reconfigurable power supply or heater controller is created using Processing open source software with serial command.
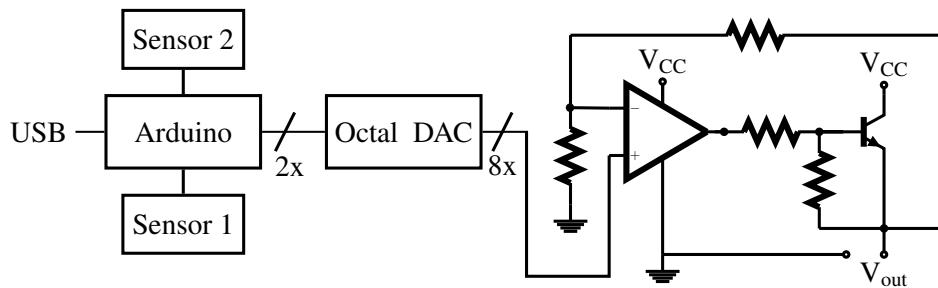
Fig. 4.3 Electronic control circuits

4.2.2 System Identification and Control Model

The step response model of the plant for Proportional-Integral-Derivative (PID) feedback controller is generated using plant identification system in Matlab and followed by parameterized $H(s)$ with underdamped pair and real pole as shown in Fig. 4.4 which is described by Eq (4.1). In this model, the configurable parameters include the damping coefficient ζ and the gain K. The other parameters are the first time constant T_1 and the time constant
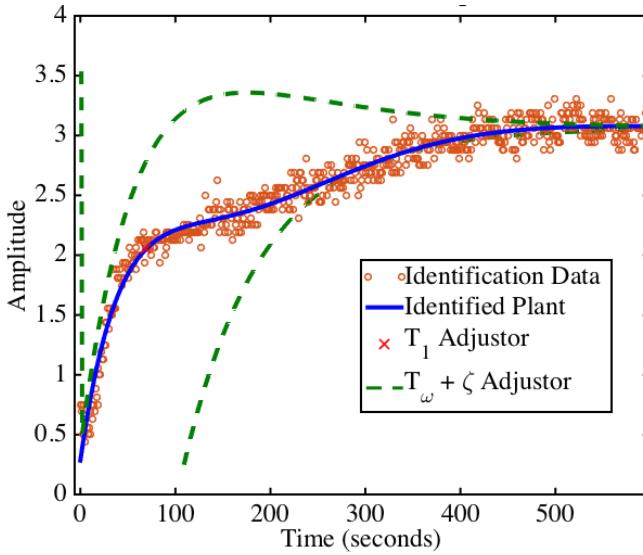
Fig. 4.4 Underdamped pair and real pole plot

associated with the natural frequency $T\omega$. The estimated parameters for identified plant structure are $K = 5.3132$, $T_1 = 67.285$, $T\omega = 76.3$ and $\zeta = 0.714$.

$$H(s) = \frac{K}{(T_1 s + 1)(T\omega^2 s^2 + 2\zeta T\omega s + 1)} \tag{4.1}$$

Using PID tuner with balance setting, the rise time and settling time are 108 seconds and 502 seconds respectively. The overshoot is about 3.87 %, peak 1.04 and phase margin 69 deg@0.014 rad/s with stable closed loop.

4.3   Experimental Setup

In order to evaluate full system performace, initial experiments were conducted to understand the characteristic of Si_3N_4 photonic chip. Fig. 4.5 shows the control program flow of heater controller. First, selected wavelength target is set on computer using graphical user interface (GUI). The library is created based on experiment result based on temperature and wavelength data. The data are collected on computer by supplying power from 15 mW to 326.6 mW. This library is used for temperature reference on wavelength target and used as lookup table in the program. The blue figure in Fig. 4.5 illustrates the heaters of MZI based structure of the Si_3N_4 photonic chip.

To characterize the chip, first we measured the output responses from two active heaters (Ch 1 and Ch 2) and sensors as shown in Fig. 4.6. The detail chip configuration can be seen in Fig. 6.4 (chip test setup in Chapter 6) and appendix. We increased the power on channel
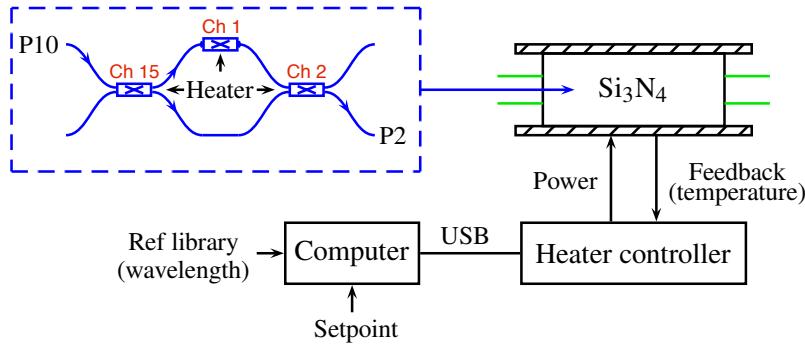
Fig. 4.5 Chip setup illustration with controller

2 at around 277 mW (supplied with 12.89 V). After few seconds, the chip temperature increases from around 19°C to about 20.5°C. Start from about 200 second, channel 1 voltage is increased gradually from 0 to 14 V. We can see that the chip temperature rises from about 21°C to around 22.5°C. The heatsink temperature also increases from 21.4°C to 21.9°C. It is clear, from Fig. 4.6, that the thermal distribution from two active heaters affect the overall chip temperature.
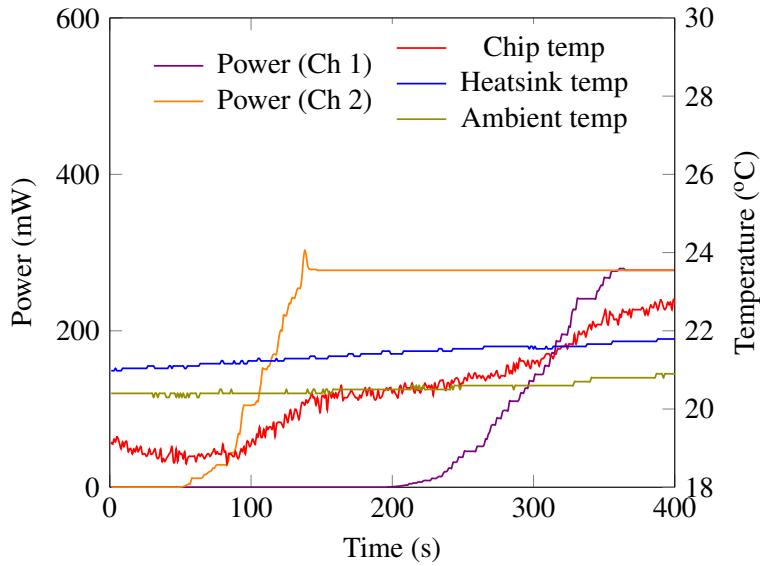
Fig. 4.6 Initial system characterization

In order to identify the crosstalk, several heaters on the chip are activated on channels 3, 4, 5 and 6. All heaters are supplied with 9 V. Fig. 4.7 shows the wavelength shift with temperature. We can see that the temperature gap between initial and after four heaters active is about 3.4°C. The wavelength also shifted from about 1553 nm (red plot) to around 1548 nm (blue plot).
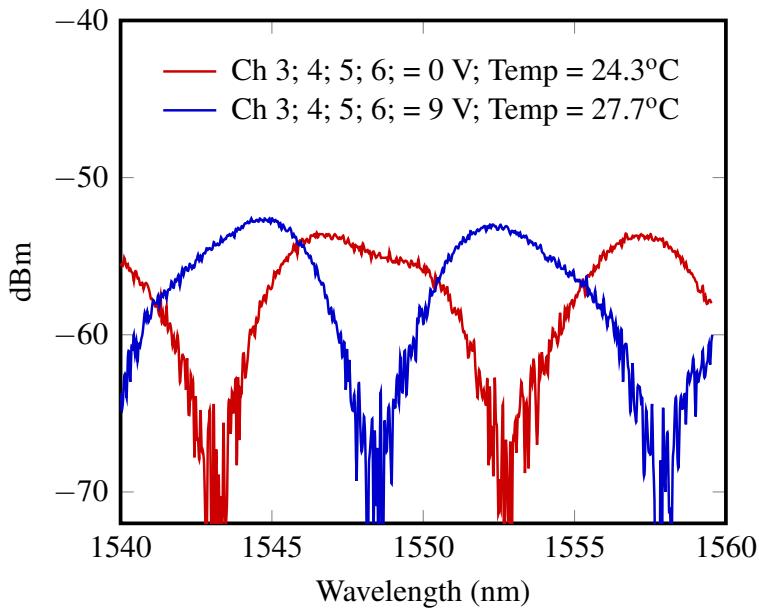
Fig. 4.7 Wavelength shift with temperature

The full measurement setup for the feedback control system is shown in Fig. 4.8. Ampli-fied Spontaneous Emission (ASE) generates a broadband light source in the telecom C-band. The output is controlled with an attenuator, a fiber Inline Polarizer (IP) and a Polarization Controller (PC). The input power was monitored using a Power Meter (PM) and a 50:50 fiber coupler. The fiber connection (red lines) from the coupler to the chip is via Polarization Maintaining optical Fiber (PMF) pigtailed to the chip. The output was connected to Optical Spectrum Analyzer (OSA) and PM using 99% and 1% coupler for analysis.
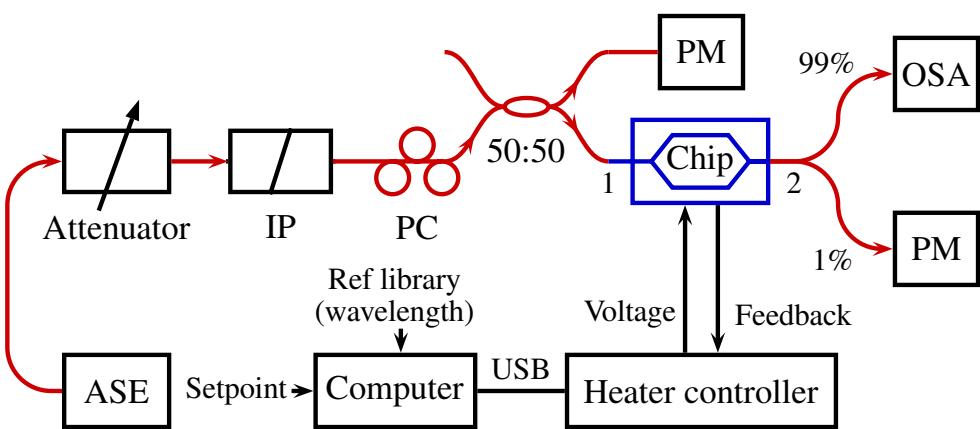
Fig. 4.8 Measurement setup
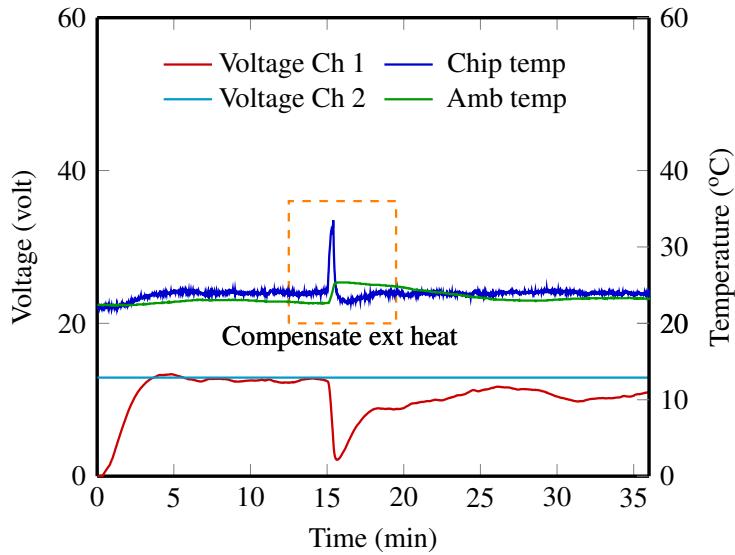
Fig. 4.9 Close feedback with heater blower

4.4   Experimental Results

For feedback control system, temperature and wavelength data are collected on computer by supplying voltage from 1 to 14 V as described in experimental setup (4.3). The correlation between temperature and wavelength is used as reference for the program. The tuned PID parameters are obtained from the control model as described in (4.2.2) system identification and control model. The parameters ($Kp = 0.3877$, $Ki = 198.1$, $Kd = 49.52$) are then applied to the feedback control systems. To evaluate the performance of the system, we measure the system stability of closed loop systems.

In the closed loop experiment test, channel 2 as the arm of the same MZI on the chip is supplied with 12.9 V. The second step is to set the temperature to 24.2^oC, this setting is used for creating initial wavelength spectrum. External disturbance is created by using a hot air blower to heat the silicon nitride chip from about 80 cm for about 15 s. From the experiments, the temperature sensor shows an increase in temperature to about 34^oC from 24^oC as shown in Fig. 4.9. This setup is used to simulate extreme environment condition or volatile external environment.

Fig. 4.9 and Fig. 4.10 represent a full system test with external disturbance with wavelength shift. The heating started at 15th min. During this time, the closed loop systems respond to or compensate for the disturbance by adjusting the voltage of feedback control input to the target wavelength peak. As shown in Fig. 4.9 and Fig. 4.10, the feedback responds to the drift by lowering the voltage which recovers the wavelength shift to the condition before the disturbance.
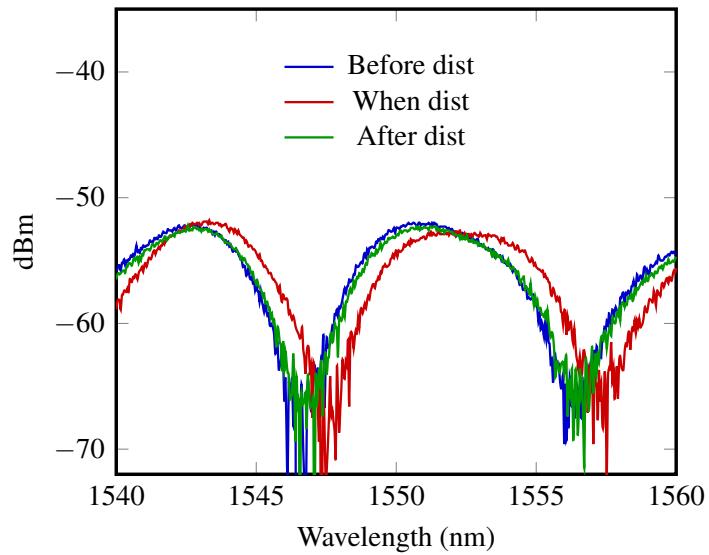
Fig. 4.10 Wavelength stabilization with external disturbance

4.5   Summary

In conclusion, a system identification technique and a feedback controller for on-chip heaters have been demonstrated for wavelength stabilization. The model can be used as a basic control scheme for a more complex system.

Chapter 5

FPGA as a Photonic Controller

5.1   Introduction

Single particles of light photons are a vital resource for the implementation of quantum-enhanced technologies such as optical quantum computing [131] and simulation [132]. To make such technologies practical requires single-photon sources, which can emit single photons on-demand and indistinguishable in all relevant degrees of freedom: central frequency, bandwidth, spatial mode, and polarization [87] [133]. Despite recent progress on relaxing these requirements [134] [135], sources that meet the required thresholds do not yet exist. Two strategies have been proposed to develop the desired photon sources [136]. One is to use 'single-emitter' quantum systems [137–140] such as quantum dots or colour centres in diamond. These systems typically emit single photons nearly on-demand, with a recent demonstration showing that the emitted photons from a single quantum dot can be highly indistinguishable [141]. However, producing highly indistinguishable photons from distinct emitters remains challenging because of the difficulty of fabricating identical emitters at the nanoscale [142] [143]. The alternative approach is to generate correlated photon pairs via spontaneous nonlinear optical processes, such as parametric down conversion or four-wave mixing in suitable crystals or waveguides, where the detection of one photon in a pair 'heralds' the existence of its partner [144–146]. However the photon pair generation events are unpredictable (being associated with vacuum fluctuations) and contain contributions from multi-pair events. Indeed the probabilities of single- (P_1) and multi-pair ($P_{>1}$) events are both related to the mean number of pairs created per pump pulse μ. They both increase with μ, and ($P_{>1}$) increases more rapidly (to leading order it grows quadratically rather than linearly). Therefore, these sources are usually operated in the $\mu \ll 1$ (and thus $P_1 \ll 1$) regime to minimize the multi-photon noise. Unfortunately, most useful quantum protocols require many simultaneous single-photon inputs in different modes, and as the success rate falls as

$(P_1)^n$ for n input modes, operation quickly becomes impractical [133] [134]. This has limited the world record quantum photonic demonstration to less than 11-photon level [95] [147].

A promising solution is to actively multiplex non-deterministic photons in different spatial or temporal modes to enhance the probability of single-photon output [148] [101] [149] [100]. Spatial multiplexing has been implemented in a few architectures [99] [97], but scaling quickly becomes infeasible as the number of photon sources and heralding detectors increases rapidly with the number of modes to be multiplexed [97] [150]. Temporal multiplexing, proposed in refs [149] [100] [4], reuses the same detectors and photon-generation components, and thus is significantly more resource efficient and scalable. The scheme in ref. [4] requires an electronic circuit to extract timing information from the heralding photons, which is subsequently used to control a switching network that actively routes the heralded photons into a pre-defined temporal mode. Recently two groups have demonstrated initial experimental implementations of active temporal multiplexing [151] [152], but the remaining challenges are: managing the photons' arrival time to the accuracy of several picoseconds, and controlling their polarization to maintain the photons' indistinguishability; and developing ultra-low-loss integrated optical components so that the desired enhancement can be achieved in a scalable manner.

In this chapter, we demonstrate the multiplexing of photons from four temporal modes solely using fibre-integrated optics and off-the-shelf electronic components. We show a 100% enhancement to the single-photon output probability without introducing additional multi-photon noise. Photon indistinguishability is confirmed by a fourfold Hong-Ou-Mandel quantum interference with a $91\pm16\%$ visibility after subtracting multi-photon noise due to high pump power. Our demonstration paves the way for scalable multiplexing of many non-deterministic photon sources to a single near-deterministic source, which will be of benefit to future quantum photonic technologies.
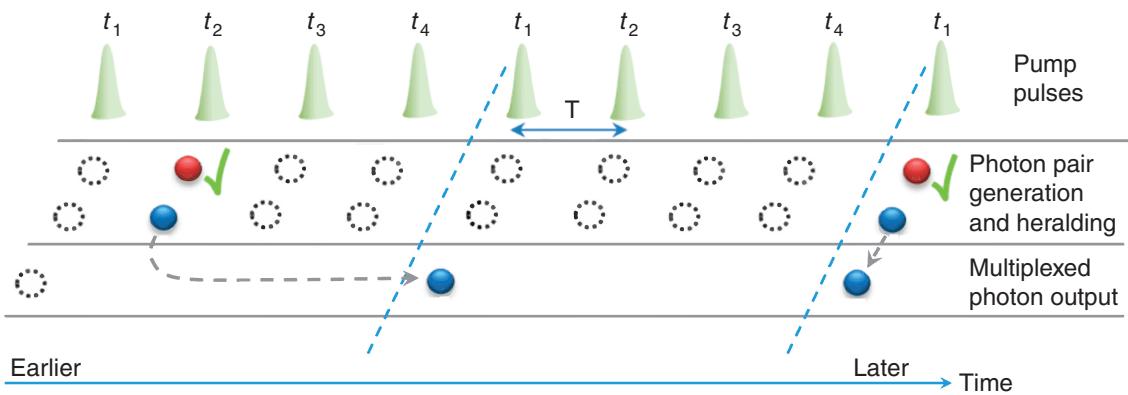
Fig. 5.1 Active temporal multiplexing principle

5.2 Active Temporal Multiplexing Scheme

5.2.1 FPGA as Photonic Device Controller

The principle of our demonstration is illustrated in Fig. 5.1. Compared with one pump pulse at period $4T$, a group of pump pulses at period T are approximately four times as likely to generate a pair in the given time frame of $4T$ if the individual pulse energy is the same. However, the random nature of the generation process within each time bin remains the same. The situation changes after the heralded photons are actively delayed to time bin t_1: if the switching network has sufficiently low losses, the heralded single-photon output probability at the $4T$ clock period will be increased. A nonlinear device is pumped by pulses separated in time by period T, each generating correlated photon pairs randomly. The two photons from each pair are spatially separated by frequency (colour) and the heralding photons (red) are detected, indicating the existence of the heralded photons (blue). Depending on the time bin in which a pair is generated, an appropriate delay is applied to the heralded photon so that it always appears in time bin t_1 with a nominal period NT ($N{=}4$ in this work).

5.2.2 Optic and FPGA Integration

To implement the scheme shown in Fig. 5.1, we design an experiment as shown in Fig. 5.2 (see Supplementary Fig. 5.7 and Supplementary Note 1 for the full setup). A mode-locked fibre laser with a repetition rate of 10 MHz (100 ns period) produces 10 ps pulses at 1,550 nm. Each pulse is split into four pulses spaced by 25 ns using two one-to-four fibre couplers and three tunable optical fibre delay lines. The four pulses then propagate along a 3-mm long nonlinear silicon nanowire, probabilistically generating correlated photon pairs via spontaneous four-wave mixing in the four time-bins [153]. As a result of energy conservation and phase matching, photon pairs are generated at frequencies symmetrically around the pump over a 6 THz bandwidth [153]. An arrayed waveguide grating (AWG, 100 GHz channel spacing and 50 GHz channel bandwidth) is used to select the photon pairs generated at 1,545 and 1,555 nm, block the pump, and spatially separate the two photons of each pair. The 1,555 nm photons are detected by a fast and low-noise niobium nitride superconducting single-photon detector as heralding signals. These signals contain the timing information of the 1,545 nm photons and are sent to a field-programmable gate array (FPGA) for analysis.

A phase-locked loop in the FPGA is used to lock to and multiply the laser's original 10 MHz clock to a 40 MHz clock. A finite state machine operating on the 40 MHz clock generates four non-overlapping clocks at four phases relative to the 10 MHz clock. A heralding photon detection signal from the superconducting single-photon detector is ANDed

with each clock phase and an appropriate three binary-digit output latches. The output
is connected to the switching network, so that the 1,545nm photons are routed into the
appropriate sequence of delay lines. All of these operations require the careful alignment
of the clock with the optical pulses that contain the generated photons. This is done by
optimizing the counts in a series of coincidence measurements, adjusting the tunable optical
delay lines and tunable digital delays (see Supplementary Note 2).
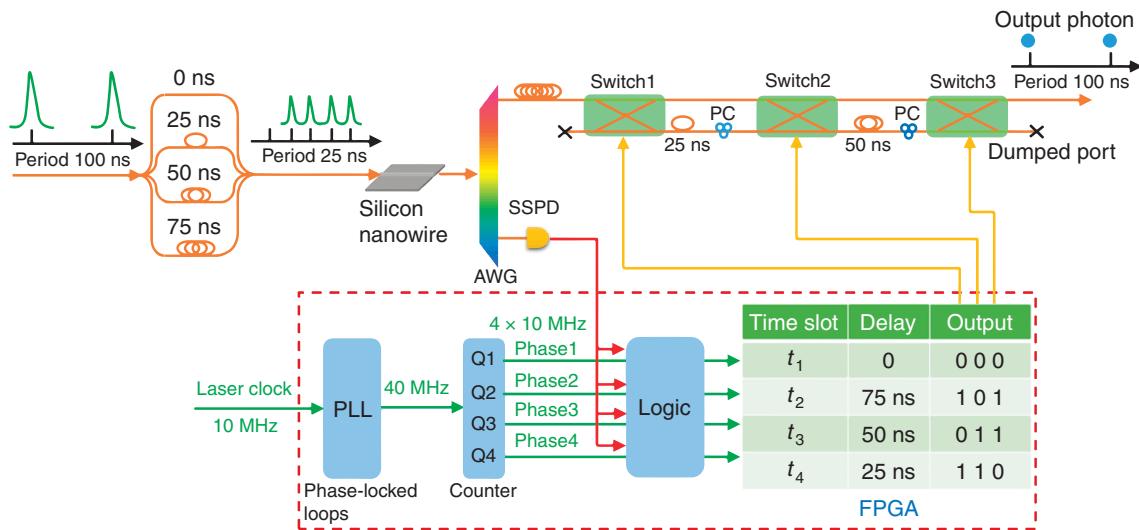
Fig. 5.2 Active temporal multiplexing experiment setup

5.3   Experimental Setup

Fig. 5.2 shows experimental setup of four temporal mode multiplexing. Pulses from a mode-
locked picosecond fibre laser are split to four copies using fibre couplers and tunable delay
lines, and pump a silicon nanowire for spontaneous four-wave mixing. The 0, 25, 50 and
75 ns delays are all relative to the uppermost optical path. After pump blocking, frequency
selection and spatial separation of the two photons of each pair, the heralding signals are
analysed by a FPGA and the heralded photons are buffered using a long fibre delay to wait
for the electronic decisions. The loss of the 200 m long buffer fibre is < 0.1 dB. The FPGA
configures the switching network to route the heralded photons into a single spatial-temporal
mode. Logic '0' means the photon remains in the input ('bar') channel; a '1' means the
photon is routed to the cross channel.

5.4   Experimental Results

To receive any benefit from a four temporal mode multiplexing setup, the switching network must have a total loss below the four times (that is, 6 dB) maximum expected enhancement. We use optical ceramic switches, made from ultra-low-loss lead lanthanum zirconium titanate [154]. These switches are fibre pigtailed and spliced with the fibre delay lines to minimize the loss of each path to around 2.8 dB, with ± 0.3 dB difference between different routes (see Supplementary Fig. 5.7). Since this loss difference is much less than the overall loss in the experiment, its effect on output photon statistics is negligible. The setup described so far ensures indistinguishability in the spectral and temporal degrees of freedom, but we also require indistinguishability in polarization. In Fig. 5.2, the heralded photons from different time bins have the same polarization before they enter the switching network. However, they experience different optical paths to obtain the correct delays, and to minimize losses these components are not polarization maintaining. This is addressed using two polarization controllers applied to the two optical delay lines (see Supplementary Note 3). The additional loss introduced by each polarization controller is ~ 0.1 dB.
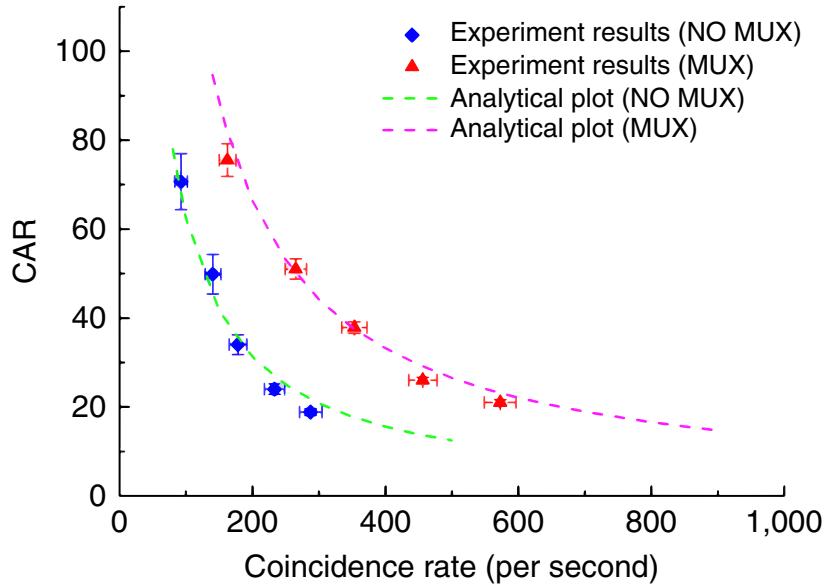
Fig. 5.3 Coincidence result

The key to verifying our design is to compare the heralded single-photon output probability per 100 ns clock period (that is, the original 10 MHz clock) at the same multi-photon noise level for sources with and without the multiplexing switching network. These two quantities are characterized by coincidence-to-accidental ratio (CAR) measurements [155].

When a pair of photons generated in the same pump pulse are detected and the detection signals sent to a time interval analyser, a coincidence is recorded. When photons generated from different pulses are detected, the coincidence represents an accidental coincidence. All of these coincidences (C) and accidentals (A) are recorded as a histogram by the time interval analyser (see Supplementary Fig. 5.7 and Supplementary Note 1), and CAR=C/A. The measured CAR as a function of the coincidence rate without multiplexing (NO MUX, that is, pumping at 10 MHz) is plotted in Fig. 5.3, indicated by diamonds. Poisson error bars are used for the plots. Dashed lines are analytic plots using the model in ref. [97]. The CAR decreases with the increased coincidence rate due to multi-pair noise and this is a typical feature of such measurements [97] [153] [155].

For comparison, we perform measurements at the same pump peak powers for the multiplexed source (MUX, that is, pumping at 40 MHz and adding the switching network to the setup). The results are plotted as triangles in Fig. 5.3. The CAR still decreases with the increased coincidence rate because the original NO MUX sources have this feature. However, when compared with the NO MUX source, at the same CAR, that is, the same multi-pair noise level, the coincidence rates are nearly doubled. At the highest power level in our experiment, the detected coincidence rate has been increased from $\sim 300 \ s^{-1}$ for the source without multiplexing to nearly $600 \ s^{-1}$ after performing multiplexing. As simply doubling the number of pump pulses per period (that is, keeping the same peak power and without an active switching circuit) can lead to similar results in Fig. 5.3 (ref. [153]), we express the improvement as an enhancement factor of MUX/NO MUX heralded single-photon output probability per 100 ns at the same CAR level. The enhancement is due to the fact that in the NO MUX case, there is a single pump pulse per 100 ns, while in the MUX case, there are four pump pulses per 100 ns; and the ratio between single- and multi-pair probabilities remains the same when the pulses have the same peak power. Taking into account the losses of waveguide-fibre coupling, spectral filters and the efficiency of detectors, we estimate the mean number of pairs per 100 ns clock period from the measured coincidence rate at each CAR level, and then infer the heralded single-photon output probabilities using a thermal distribution function for both NOMUX and MUX sources (see Supplementary Note 4). The enhancement factor at each CAR level is plotted in Fig. 5.4 as circles, showing that our four temporal mode multiplexing nearly enhances the heralded single-photon output probability by 100% (that is, 3 dB). The enhancement is less than the ideal factor of 4 (that is, 6 dB) because of the 3 dB loss of the switching network.

For the multiplexed source to be useful, the multiplexed heralded photons must be indistinguishable. This is tested by Hong-Ou-Mandel (HOM) quantum interference [156]. We build another heralded single-photon source based on a second 3-mm long silicon
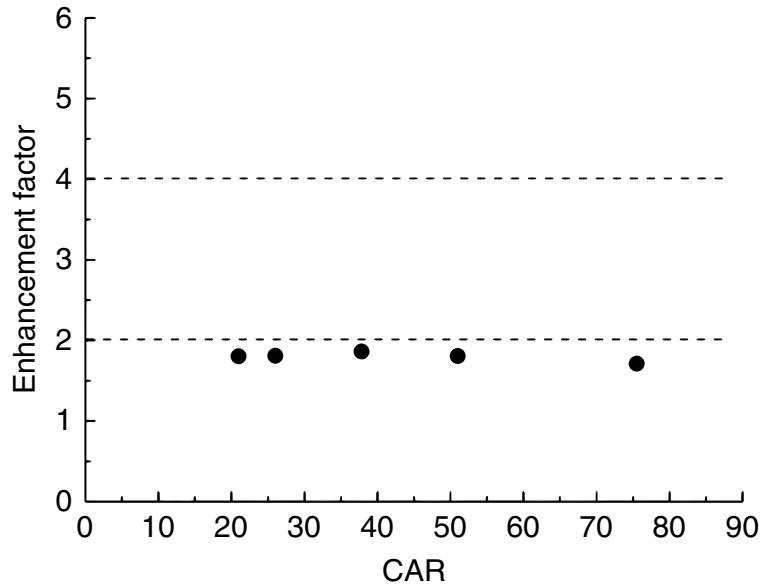
Fig. 5.4 CAR result

nanowire pumped by the same 10 MHz laser, but without multiplexing (see Supplementary Note 5). The photons from this second source are in a certain spatial-temporal state, that is, in an identical polarization state and at the accurate 100 ns clock cycle of the laser, and so they provide a reference to check if the multiplexed photons are indistinguishable. Note that as the AWG channels used to filter the generated photons have a slightly larger bandwidth (50 GHz) than the pump (10 ps transform limited pulses corresponding to 44 GHz), the photons to be interfered have some chance to be in different spectral modes. This may slightly reduce the HOM interference visibility [157].

As the photons to be interfered at a 50:50 beam splitter must be heralded by their corresponding partner photons, the HOM interference here actually involves fourfold (or four photon) coincidence measurements [158] [159] (Supplementary Fig. 5.7). Because the fourfold coincidence rate from two separate sources is very low due to the low photon collection efficiency, we first perform a standard twofold interference measurement (that is, without heralding) to find the appropriate delay between photons from the two sources [158]. Fig. 5.5 presents indistinguishability measurement of the multiplexed photons. Raw visibility of twofold (diamonds, left axis) and fourfold (squares, right axis) measurements. In this measurement, the pump powers are set at a level of CAR=18 for both. The twofold dip shows a raw visibility of 24±1.9% (diamonds in Fig. 5.5). Then we take the fourfold HOM interference measurement, but at higher pump powers for both sources in order to have sufficient coincidence counts to make the statistics meaningful in a reasonable amount of
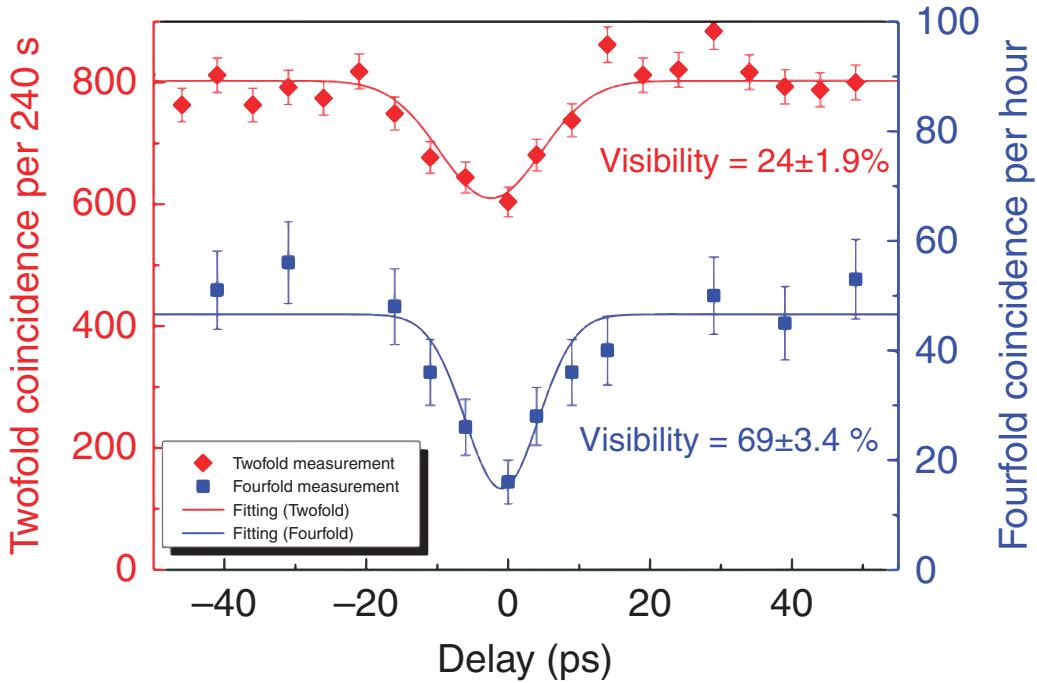
Fig. 5.5 Two-fold result

measurement time (for example, 50 coincidences in 1 h) with our low-efficiency detectors. The cost is that the CAR drops to 7, and more multi-photon noise is generated and reduces the visibility of the HOM dip. We observe a fourfold HOM dip with raw visibility of $69\pm3.4\%$ (squares in Fig. 5.5), indicating that non-classical interference occurred between the multiplexed photons and the photons from the second source. To check that the residual photon distinguishability is not because of multiplexing but due to multi-photon noise at high pump powers, we measure the detector dark count and multi-photon contribution from each source (see Supplementary Note 5) [159]. Using these data we correct the raw data, which yields a visibility of $91\pm16\%$ (Fig. 5.6), clearly showing that the multiplexed photons are highly indistinguishable. This non-100% visibility is partly because of the large error bars resulting from the low count rates, and partly due to the photons' spectral distinguishability introduced by the slightly broader band filtering of the photons mentioned earlier. Fig. 5.6 shows fourfold HOM dip visibility after subtracting multi-photon noise. Poisson error bars are used for the plots. Solid lines are Gaussian fits according to the spectral filtering shape in the experiment.

Varnava et al. [134] have shown that if the product of the detector efficiency with the source efficiency is greater than 2/3, then efficient linear optical quantum computation is possible. The detector efficiency has been brought to nearly unity by advanced supercon-
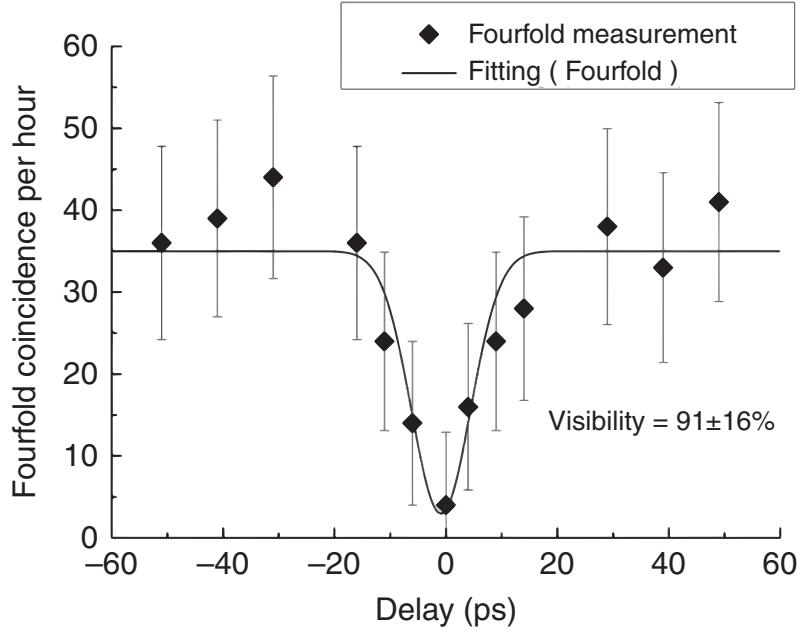
Fig. 5.6 Four-fold result

ducting technology [160]. Thus, recalling caveats concerning indistinguishability between distinct near deterministic sources as discussed in the Introduction, we need to bring non-deterministic nonlinear photon sources into the nearly deterministic regime, that is, increase the source efficiency to at least 0.67 to make optical quantum information processing a reality. The source efficiency is the product of photon-generation efficiency and spectral filtering transmission efficiency. Assuming 90% filter transmission, the photon-generation efficiency has to be greater than 0.75. If we start with a generation efficiency of 0.015 (arbitrarily chosen to be $<<$1 to suppress multi-pair generation), using the first-order approximation (more rigorous and detailed analysis can be found in refs [100] [4]), we need to multiplex at least N=0.75/0.015=50 time-bins if the switch circuit has negligible losses. The required number of switches is an integer no less than $log_2 N$+1 (ref. [4]), which is 7. Using seven switches, the number of multiplexed time-bins is $2^{(7-1)} = 64$. As this number is larger than the required N = 50, and the probability of generating more than one pair in 64 time-bins is low since 0.015$<$1/64, it is possible to achieve the required enhancement. The major challenge is to reduce the losses of switches. Recent development of stress-optic effect-based switches has the potential to bring the switching losses down to the desired level [126]. This type of switch has a 2 mm thick lead zirconate titanate (PZT) film on the top of a very low loss (as low as 0.0005 dB cm^{-1}) SiN waveguide [126]. The applied stress has nearly no

impact on the loss and thus the switch can be practically lossless if we make the switches and delay lines on the same chip to avoid waveguide-fibre coupling.

The other challenge involved in developing high performance heralded single-photon sources is to have pure heralded photon sources before multiplexing so that the photons after multiplexing are highly indistinguishable. In our current demonstration, the interplay between pump bandwidth and phase matching dictates that purity is maximized with sufficiently narrow filter bandwidths. In the future, we can increase heralded photon purity by either using narrower bandpass filters to appropriately reduce the generated photon bandwidth or employing micro-ring resonators as the nonlinear device [161].

5.5   Summary

In conclusion, this demonstration provides a road map for creating near-deterministic heralded single-photon sources using a resource efficient and thus scalable multiplexing scheme. With nearly unity efficiency detectors, 90% transmission filters and low-loss switches, this scheme will ultimately provide a solution for single photon sources.

5.6   Supplementary Note

5.6.1   Note 1: Full setup and explanation of coincidence measurements
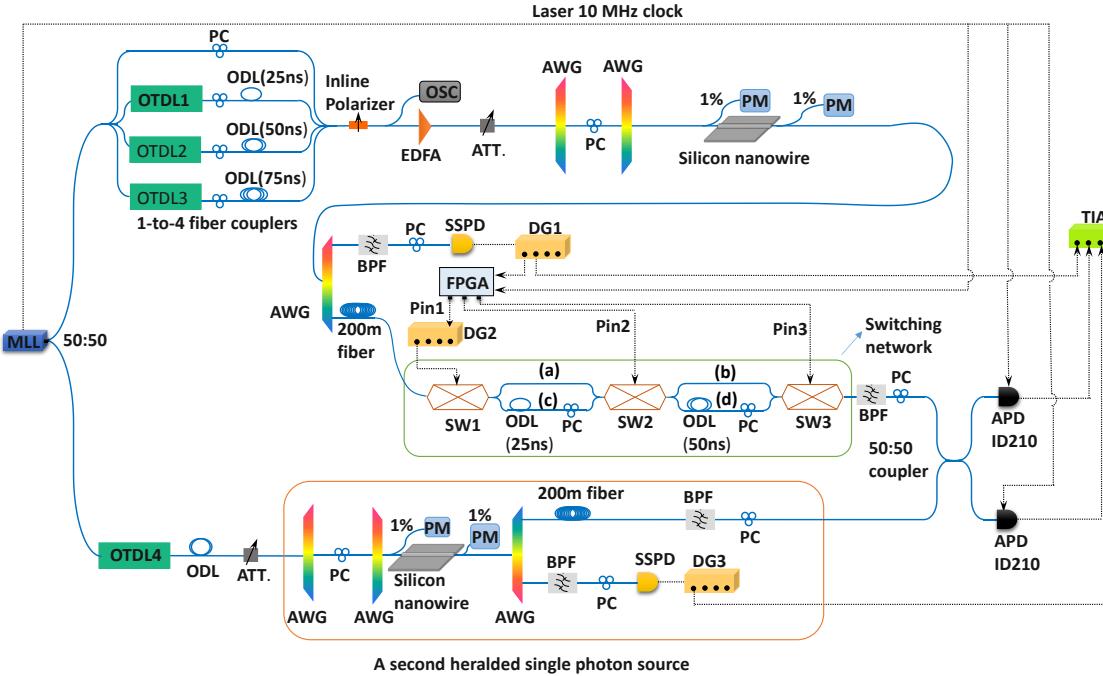
Fig. 5.7 Full setup of the experiments

The full setup of our experiments is illustrated in Supplementary Fig. 5.7. Solid and dashed lines represent optical fibers and electronic cables, respectively. MLL: mode-locked laser, OTDL: optical tunable delay line, ODL: optical delay line, PC: polarization controller, ATT: attenuator, OSC: oscilloscope, AWG: arrayed waveguide grating, PM: power meter, SSPD: superconducting single photon detector, DG: delay generator, FPGA: field- programmable gate array, SW: switch, BPF: bandpass filter, APD: avalanche photo diode, TIA: time interval analyzer. The top half of the diagram, excluding the 50:50 coupler before the two avalanche photo diode single photon detectors (ID210, Id-Quantique), is for the CAR measurements of the source with four temporal-mode multiplexing (MUX). When doing the measurements for the source without MUX, we connected only one of the four channels of the 1-to-4 fiber couplers (FCs), and removed the switching network. This arrangement allowed the least change to the experimental conditions for the MUX and NO MUX measurements, and thus guaranteed a fair comparison between them. Because the losses of the four channels of the FCs were slightly different, we used one polarization controller (PC) in each channel and an inline polarizer immediately after the FCs to ensure the pulses in the

four temporal modes after the inline polarizer had the same intensity. A fast optical sampling oscilloscope was used to monitor the pulse intensities. The CAR measurements for pumping at the 10 MHz clock of only t_1, t_2, t_3 or t_4 (Fig. 5.7) indicate that all four NO MUX sources have the same performance, as shown by diamonds in Fig. 5.3.

The bottom half of Supplementary Fig. 5.7 is a second heralded single photon source based on a silicon nanowire [153] with the same specification to that used in the MUX experiments. This source was pumped at the laser's 10 MHz clock, and provided a reference for the indistinguishability test of the multiplexed photons via the four-fold HOM quantum interference [158].
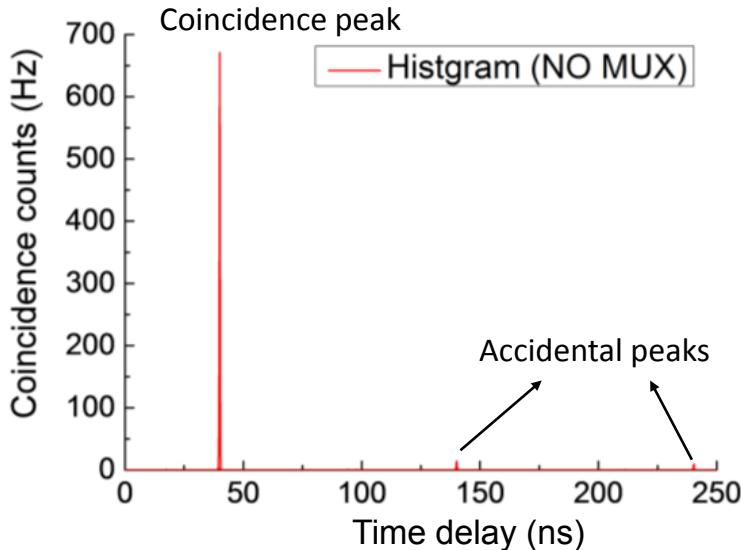
Fig. 5.8 Histogram for CAR measurements result with NO MUX

When we performed the CAR measurements for the NO MUX and MUX photon sources, we took the 50:50 coupler out of the setup and connected the heralded photon output directly to one ID210 detector. In both cases, the heralded photon events detected by an ID210 triggered by the 10 MHz laser clock were used as the 'start', and the heralding photon events detected by a SSPD were used as the 'stop' for the TIA to construct the histograms: coincidences vs time delay between 'start' and 'stop'. This 'start' and 'stop' arrangement is different from the standard way of using heralding signals as the 'start' and heralded as the 'stop' just for our experimental convenience to adjust the delays, and it does not change the physics. A suitable electronic delay was applied to the heralding detection signals so that the delay in the histogram was always within the 0-250 ns time window. Supplementary Fig. 5.8 and Fig. 5.9 show typical histograms for the NO MUX and MUX sources in the
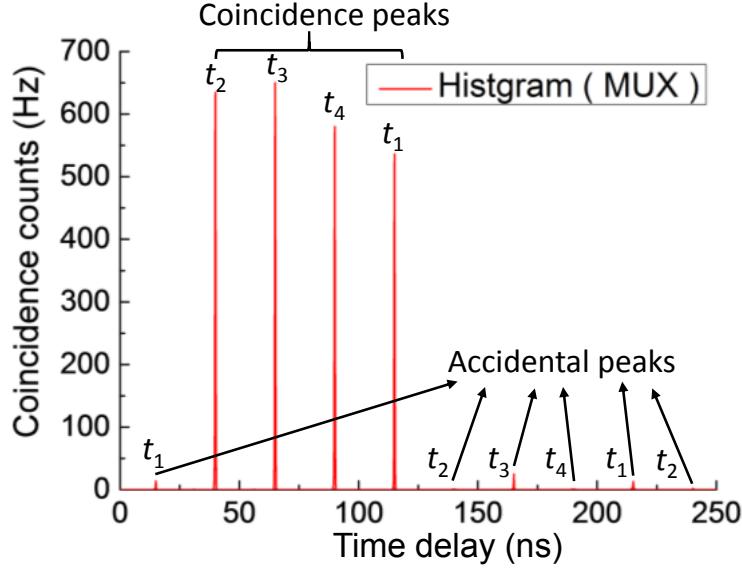
Fig. 5.9 Histogram for CAR measurements result with MUX

CAR measurements [155]. For the NO MUX source (Supplementary Fig. 5.8), we sum up all counts in the coincidence peak and the accidental peak closest to the coincidence peak as the coincidences and accidentals, respectively. The time interval between the peaks is the pump laser period. The ratio between them gives the CAR. For the MUX source (Supplementary Fig. 5.9), depending on in which time bin the heralded photons are generated, they experience different optical delays to be multiplexed to the 10 MHz clock; however the heralding photons are still on the 40 MHz clock, so there are four coincidence peaks (the signature of successful multiplexing). These peaks look slightly different from one another because photons generated in different time bins experience slightly different losses when propagating through different optical paths. Each coincidence peak should have their corresponding accidental peak. Two accidental peaks nearly disappear because the photons that are generated in time bins t_2 and t_4 require logic '1' be applied to switch1 (Fig. 5.2). This switching operation on switch1 only allows heralded photons to arrive at the detector when there are heralding events, and therefore switches away all other events that may give rise to coincidences in the accidental peak. To calculate the CAR for the MUX source, we sum up the counts in all four coincidence peaks as the coincidences; and multiply the overall counts in the two visible accidental peaks by two as the accidentals. This process is considered to be fair because: first, the sources pumped by each individual temporal mode have been tested to have the same performance; second, corresponding to the loss differences between the different paths, the accidentals for t_3 should be higher than those for t_2, while

the accidentals for t_1 should be lower than those for t_4, and the total accidentals for t_3 and t_1 can approximately represent those for t_2 and t_4.

5.6.2   Note 2: Clock, optical delay, and switching network management

To make this temporal multiplexing experiment successful, we had to synchronize: (I) the 40 MHz clock of the FPGA and the heralding event so that the FPGA could find out which time bin the heralding photons were generated; (II) the switching electronic signals from the FPGA and the heralded photons arriving at the switches so that proper delays could be applied to the photons; and (III) the relative optical delays in the four channels of the FCs and in the switching network.

For synchronization (I), we used a digital delay generator (DG1 in Supplementary Fig. 5.7) between the SSPD heralding detection signal output and the FPGA. By doing an AND operation between the heralding detection signals and the FPGA clock, and comparing the FPGA output count rate with that on the SSPD software, we could find the correct delay using DG1. Once this was done, we could proceed to synchronization (II).

To simplify synchronization (II), we configured the FPGA such that according to a heralding event, the three binary-digit output was latched until the next heralding event occurred. For example, if a photon pair was generated in time bin t_1, '000' was applied to the switches until the next pair was generated. If the next pair was generated in time bin t_4, the output of the FPGA would change to '110' (Fig. 5.2). In this way we only need to synchronize the switching signals that control switch1 with the incoming photons, because once photons pass through switch1, they are routed directly through switch2 and switch3 that are always under the correct logic control.

Because the relative delay between heralding and heralded events was the same no matter in which time bin the photon pairs were generated, we only need to do synchronization for one pump temporal mode. As the initial input status to the switches was '0', we had to choose the pump on the clock of either t_2 or t_4 for synchronization because only these two pump modes required a logic '1' input to switch1 and were possible for delay alignment. In the setup shown in Supplementary Fig. 5.7, we only connected the channel of FCs with 25 ns optical delays (i.e. t_2) and applied a constant output '101' from the FPGA to the switches to take a coincidence measurement as the reference. Then we added a digital delay generator (DG2 in Supplementary Fig. 5.7) between the logic output pin1 of the FPGA and switch1. We could continuously tune the delay of the switching signals to switch1 via DG2 and measure the coincidences. By trial and error, the correct delay was found when the measured coincidences matched with the reference measurement. This delay was then double confirmed by coincidence measurements for the other three temporal pump modes.

Note that DG2 only responds when the output logic from pin1 changes from '0' to '1' and keeps switch1 at the "switching" status for 100 ns, so the use of DG2 here is optional as long as we ensure the signals from the FPGA are sent to all three switches before the incoming photons. The advantages of having DG2 for synchronization are that we have a more accurate control to the switching circuit and thus can route some unheralded photons (i.e., pairs are generated but the heralding photons have been lost) to the dumped port. For synchronization (*III*), we manually cut optical fibers with the lengths providing delays of approximately 25 ns and 50 ns and spliced the fibers in paths (c) and (d) of the switching network (Supplementary Fig. 5.7); and then used off-the-shelf fiber-integrated optical tunable delay lines (OTDL) with a tuning step of 1 ps in three channels of the FCs for multiplexing the pump to match the delays in the switching network. Compared with directly using OTDL in the switching network, this arrangement minimized the losses of the multiplexed heralded photons.

5.6.3   Note 3: Polarization management

Due to the use of non-polarization maintaining components in the switching network, photons with the same polarization at the input generally will have different polarization at the output if they go through different optical paths. Depending on in which time bin the heralded photons are generated, they go through the combination of optical paths shown in Supplementary Fig. 5.7, t_1: (a)+(b), t_2: (c)+(b), t_3: (a)+(d), and t_4: (c)+(d). We found that adding one PC in each of (c) and (d) was sufficient to maintain the polarization of the photons. For example, the photons from t_1 and t_2 share the path (b), the PC in (c) can always adjust the polarization of photons to be the same to those in (a). Then (c) becomes equal to (a) in terms of polarization. The same rule applies to (d) and (b) and thus photons from all time bins will have the same polarization at the output of the switching network.

5.6.4   Note 4: Inferring heralded single photon output probability

Because we did not use photon number resolving detectors, we cannot measure the heralded single photon output probability directly, but we can infer it from the coincidences measured by threshold detectors.

As shown in Supplementary Fig. 5.7, both the generated photons and the pump were filtered using AWGs with the same channel bandwidth of 50 GHz. This arrangement makes it appropriate to use the thermal distribution to describe the photon generation statistics [155]. Using the measured coincidences, we calculate the mean number of generated pairs per 100 ns clock period μ, by taking into account the total losses in the heralding and heralded photon

arms. Using $P_1 = \mu/(1+\mu)^2$ we infer the heralded single photon generation probability per 100 ns clock period. Using $P_1\eta$ with η being the overall photon pair collection efficiency, we calculate the heralded single photon output probability for the plots in Fig. 5.4.

5.6.5 Note 5: Four-fold HOM interference

The delay management procedure described in Supplementary Note 2 aligns the photon arrival time to an accuracy of 1 ns, which is determined by the time resolution of the coincidence measurement system. The four-fold HOM interference requires the delay alignment at the accuracy of photons' coherence time which is of the order of the pump pulse width 10 ps. The measurements were taken in the following steps. First, we connected only the channel of the 1-to-4 FCs without optical delay lines as the pump of the MUX source so that photons were always generated in time bin t_1. By varying the delay of OTDL4 in the second source (see Supplementary Fig. 5.7), we adjusted the fine delay via two-fold HOM interference and fixed the delay on OTDL4. Second, we connected in turn only the channel of the 1-to-4 FCs with OTDL1, OTDL2, or OTDL3, to determine and fix the fine delays for them via two-fold measurements. Third, we connected all four channels of the 1-to-4 FCs to obtain the fully multiplexed source and took the two-fold and four-fold HOM interference measurements by varying the fine delay on OTDL4.

As the pump powers for the four-fold HOM interference measurement were relatively high, we attribute the 69% visibility predominantly to multi-pair noise. To obtain this noise information, we performed four-fold coincidence measurements at the same fine delays set in the raw measurements by disconnecting input to the 50:50 coupler from the MUX and second photon sources, respectively [159]. Because subtracting these four-fold counts from the raw four-fold counts would subtract the noise due to detector dark count twice, we also measured the four-fold coincidences by disconnecting both sources from the 50:50 coupler, and added these dark count induced four-fold counts back to get the net four-fold coincidences. To understand this process, we give an example: we obtained a raw four-fold coincidence count C_{raw} at a particular delay δt. We measured the multi-pair noise contribution to C_{raw} from two sources at delay δt to be C_{n1} and C_{n2}, and the detector dark count contribution to C_{raw} at delay δt to be C_d. The corrected net four-fold coincidence is then $C_{raw} - C_{n1} - C_{n2} + C_d$. We did this correction for all delays shown in Fig. 5.5 and obtained the data for Fig. 5.6. This multi-pair noise subtraction yields a $91\pm16\%$ visibility.

Chapter 6

Adaptive Reconfiguration for Photonic Stabilization

6.1 Introduction

Photonic integrated circuits (PICs) have been proposed for many applications, including sensing [162], communication [129], and quantum computing [6]. PICs are often implemented in complementary metal-oxide semiconductor (CMOS) compatible technologies, and the materials involved have high thermo-optic coefficients [3], making their operation very sensitive to temperature changes.
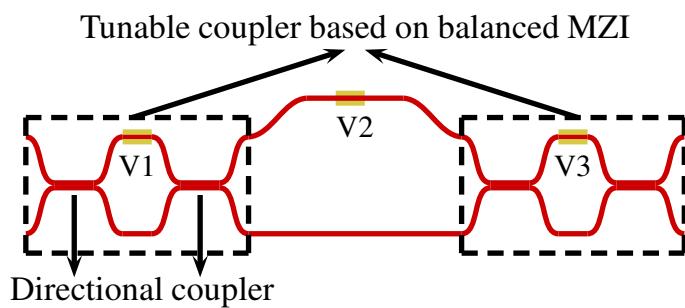
Fig. 6.1 Schematic of an on-chip MZIs-based WDM.

Temperature sensitivity can be used advantageously. For example, a quantum time-bin entanglement experiment used temperature-dependent tunable couplers and phase shifters to control the amplitude, phase, and wavelength of certain photon states [6]. Fig. 6.1 shows the schematic of an on-chip wavelength division multiplexer (WDM) based on Mach-Zehnder interferometers (MZIs). The yellow parts are heaters for thermooptic based phase shifters. V1, V2, V3 are voltage inputs to adjust refractive index of the waveguide, which enables a

controllable phase shift. Overall, it is a MZI with two arms slightly unbalanced in length. The slight difference in arm lengths determines the free spectral range, and the phase shifter can vary the peak wavelengths [Fig. 6.2]. The red sinusoid line is the light signal which has intensity, wavelength, free spectral range (FSR), peak wavelength and extinction ratio. When both input and output couplers are exactly at the 50:50 splitting ratio, the best extinction ratio is achieved. In reality, it is difficult to make on-chip directional couplers with exactly 50:50 splitting ratio due to fabrication imperfections. The solution is to make an arbitrarily tunable coupler based on a MZI with two arms balanced in length, as shown in the dashed rectangles in Fig. 6.1. In such a balanced MZI, even if the input and output directional couplers deviate from the 50:50 splitting ratio, we can use the phase shifter to control the ultimate splitting ratio. The phase shifters use thermo-optic effects through applying a certain voltage to the resistive heaters. Three resistive heaters, controlled by voltages V1, V2, and V3, are used to adjust the refractive index of the waveguide, allowing a controllable phase shift. When this MZI-based configuration scales up and is integrated into more complicated circuits with multiple inputs, outputs, and several functionalities, care must be taken to avoid changes in the output, i.e., signal drift. Thus accurate and robust control of multiple inputs and multiple outputs (MIMOs) are required in practical systems.
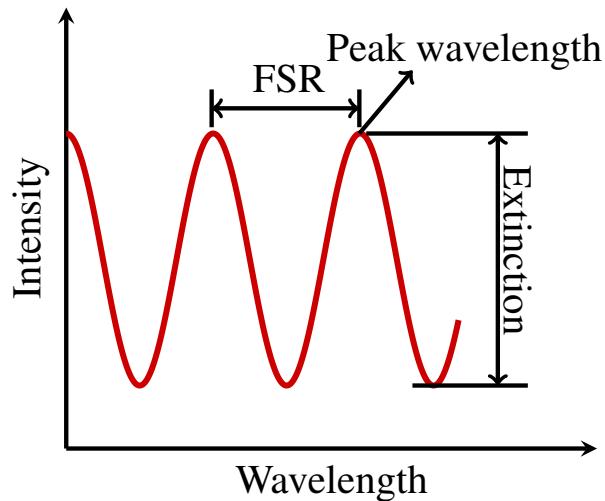
Fig. 6.2 A typical spectral response of the WDM with a light source.

Control schemes on photonic-based electro-optic and thermo-optic systems have been proposed for many applications. For instance, ring resonator MIMO-based electrooptic systems have been proposed using cascaded micro resonator based matrix switches in a silicon photonic interconnection network for many core computing applications [163]. The system used resonator-based electro-optic switches to achieve nonblocking interconnections

among multiple inputs and multiple outputs. MZI thermo-optic systems with MIMO control is an alternative approach that has versatile functionality and reconfigurability.

Efforts to address the issue of thermal sensitivity are reviewed in Refs. [41] [51] [44] [130] [164], and approaches include athermal waveguides, thermally self-compensating passive circuits, and active feedback control. Wavelength locking and thermally stabilized operation were demonstrated using a silicon microring resonator and dithering in a thermally volatile environment [165]. In addition, a contactless integrated photonic probe as input for feedback control for compact system integration was also demonstrated [166]. In 2015, Fisher et al. [167] proposed a control-scheme-based calibration technique and extremum-seeking algorithm on a large PIC incorporating ring resonators and MZI structures; however, there has been no experimental demonstration on MZI-based systems. In addition, the robustness, loop interaction, and control are not analyzed and may not yield the best overall control.

In Chapter 4 of this thesis and Ref. [7], we presented a unique design of single input and single output system controller with a proportional integral derivative algorithm for wavelength stabilization with external disturbance. This chapter demonstrates, for the first time, to the best of our knowledge, MIMO control of a silicon nitride thermo-optic PIC incorporating MZIs. This work differs in several aspects, including control algorithm, experimental setup, feedback input, circuit under test complexity, and disturbance compared to Ref. [7]. Using a dual proportional integral reference tracking algorithm [168] [169] combined with system identification [170], we demonstrate reliable performance with enhanced reconfigurability. For system identification, the underdamped pair and real pole method is applied for robust analysis [171]. The control system adaptively tunes and maintains the operation wavelength of the target outputs. The system performance was improved in terms of control accuracy by reducing wavelength peak drift due to internal and external disturbances from 0.5 to 0.1 nm.

6.1.1 Multiple-Input Multiple-Output Controller

To provide system summary for analysis and design of the input/output response, the basic control system transfer function for the experiments needs to be defined [1]. Fig. 6.3 shows basic feedback loop with the assumption that the three components (P: plant; C: controller; F: sensor) are linear functions of the sums of their inputs. Another parameters to be considered are r: reference or command input; u: actuating signal; d: external disturbance; v: sum (represented by Σ) of actuating signal and disturbance; η: plant output; y: sum of plant output and noise n; n: sensor noise.

Consider the system in Fig. 6.3 has three blocks representing a plant or process P (blue), a feedback controller C (green), and a sensor or feedforward controller F (red). There are three external signals: the reference r, the measurement noise n, and the load disturbance d.
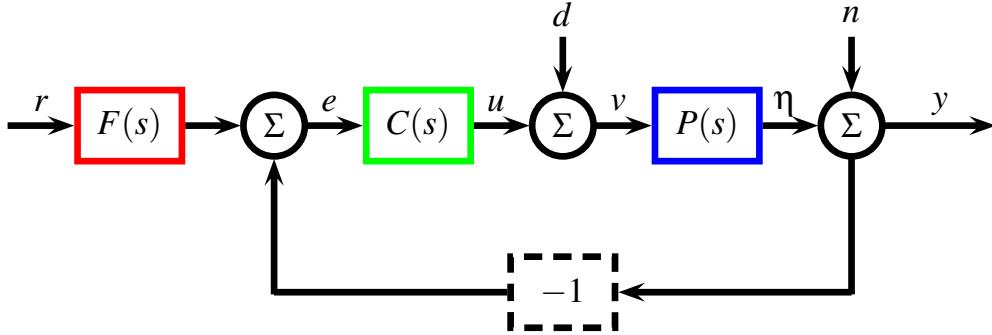
Fig. 6.3 Basic feedback loop with the assumption adopted from [1]

A typical problem is to obtain how the error e is correlating to the signals r, d, and n, as follows:

$$e = Fr - y. \tag{6.1}$$

To attain the relevant transfer function, it starts with the control error e, given by Eq (6.1). From the block diagram as shown in Fig. 6.3, signal y is the sum of n and η, where η is the output of the plant; thus, we can specify Eq (6.2) as follows:

$$y = n + \eta, \quad \eta = P(d+u), \quad u = Ce. \tag{6.2}$$

$$
\begin{aligned}
e = Fr - y = Fr - (n + \eta) &= Fr - (n + P(d+u)) \\
&= Fr - (n + P(d + Ce)),
\end{aligned} \tag{6.3}
$$

$$e = Fr - n - Pd - PCe. \tag{6.4}$$

$$
\begin{aligned}
e &= \frac{F}{1+PC}r - \frac{1}{1+PC}n - \frac{P}{1+PC}d \\
&= G_{\mathrm{er}}r + G_{\mathrm{en}}n + G_{\mathrm{ed}}d,
\end{aligned} \tag{6.5}
$$

We get Eq (6.3) by combining Eq (6.1) and Eq (6.2). Therefore, Eq (6.4) is the result of this combination. Finally, solving Eq (6.4) for e result in Eq (6.5). G is described as the transfer function.

$$G_{er}r = \frac{F}{1+PC}, \quad G_{en}n = \frac{-1}{1+PC}, \quad G_{ed}d = \frac{-P}{1+PC} \tag{6.6}$$

The error e is the sum of three terms, hinge on the reference r, the load disturbance d and the measurement noise n. The functions in Eq (6.6) are transfer functions from reference r, noise n and disturbance d to the error e.
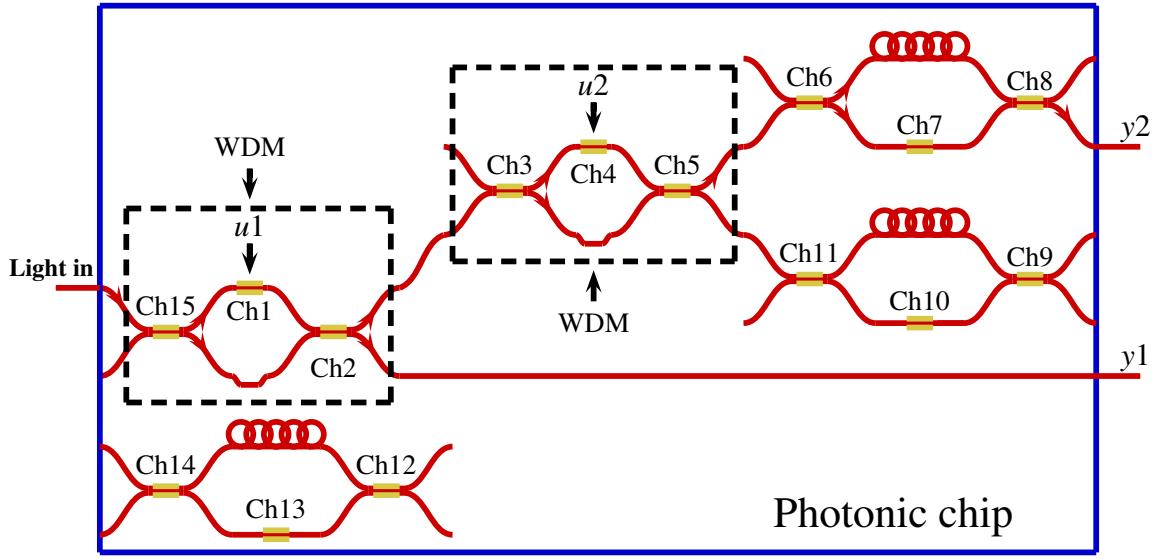
Fig. 6.4 Chip test setup with two feedback inputs and two outputs

The control feedback system in this chapter provides several parameters for the experiment setup shown in Fig. 6.6. Plant P is represented by the silicon nitride photonic chip, and controller C, is the heater controller that supplies the voltage to the chip. The objective of the control system is to set the output $y(y1, y2)$ by manipulating input $u(u1, u2)$, the voltage input to the heater. The output y is detected using the OSAs. This output is compared by F to the reference value r. The control objective is to keep $e = y - r$ small.

$$y(s) = P(s)u(s), \quad u(s) = C(s)e(s) \tag{6.7}$$

$$e(s) = r(s) - F(s)y(s) \tag{6.8}$$

Assume the plant P, controller C and sensor F are linear and time-invariant. The system can be analyzed using the Laplace transform on the variables. This gives the relations as described in Eq (6.7) and Eq (6.8). These equations give the $y(s)$ as described in Eq (6.9) by solving $y(s)$ in term of $r(s)$.

$$y(s) = \frac{P(s)C(s)}{1 + F(s)P(s)C(s)} r(s) \tag{6.9}$$

Fig. 6.4 depicts chip test setup with two feedback inputs $u1$ and $u2$ and two outputs $y1$ and $y2$; Feedback points are Ch1 and Ch4 (WDM parts); Ch1-Ch15 are heater points inside the chip. The red lines represent the Si_3N_4 waveguides, and the yellow lines are the resistive heaters.

6.1.2 Control Transfer Function

Feedback control aims to manipulate an output subject to an unknown disturbance, with the goal of minimizing an error function. MIMO systems use different error functions to single input single output (SISO) and can present a sensitivity to uncertainty that is fundamentally different [172]. MIMO transfer functions use vector values for inputs and outputs, and can be specified by concatenation of SISO transfer function models, as follows:

$$H(s) = \frac{K}{(T_1 s + 1)(T \omega^2 s^2 + 2\zeta T \omega s + 1)} \tag{6.10}$$
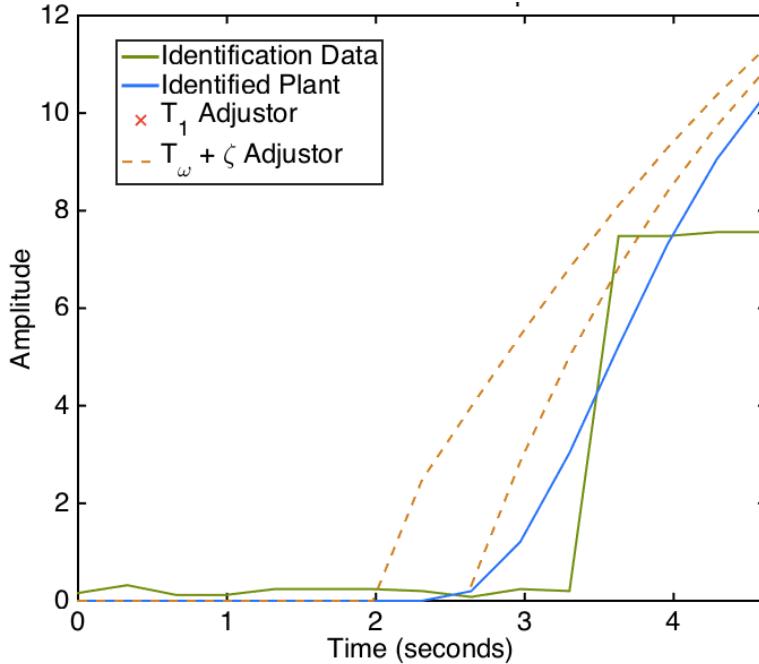
Fig. 6.5 Control model analysis.

Fig. 6.5 shows control model using underdamped pair and real pole analysis. The green solid line depicts the identified signal from the experiment. The blue solid line shows the

identified generated plant model with underdamped pair and real pole analysis. Red cross mark is the the first time constant (T_1) parameter. The dashed orange lines are the natural frequency ($T\omega$) and (the damping coefficient (ζ) parameters used to tune the model.

Eq (6.10) is based on underdamped pair and real pole, which described in Ref. [171]. The transfer function is deduced from the experimental setup via system identification [170]. Once inputs and outputs are obtained from the experimental data, the transfer function is analyzed and the coefficients needed for real control algorithm are obtained. The MIMO model generated by this transfer function is described in detail in Ref. [173]. The transfer function model of the plant for proportional integral reference tracking in this experiment is generated using a plant identification system in Matlab$^\circledR$ [174], assuming a transfer function $H(s)$ with underdamped pair and real pole as shown in Fig. 6.5, which is described by Eq (6.10).

The configurable parameters include the damping coefficient ζ and the gain K. The other parameters are the first time constant T_1 and the time constant associated with the natural frequency $T\omega$. The estimated parameters for identified plant structure are $K = 38.151$, $T_1 = 2.62$, $T\omega = 0.41912$ and $\zeta = 0.447$. Using proportional integral control with standard tuner and balance settings, the rise time and settling time are 1.21 and 6.72 s, respectively. The overshoot is about 9.94%, peak 1.1, and phase margin 60 deg at 0.817 rad/s, ensuring closed loop stability.

6.2 Experimental Setup
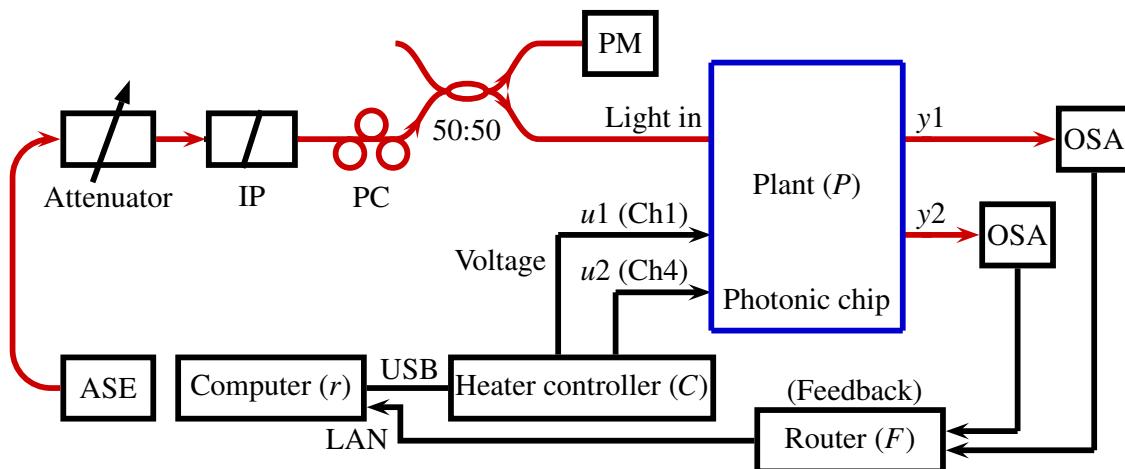
Fig. 6.6 Experiment setup of MIMO feedback control.

Fig. 6.6 presents experiment setup of MIMO feedback control. Red solid lines are optical fibers, and black solid lines are electric cables (ASE: amplified spontaneous emission; IP: inline polarizer; PC: polarization controller; PM: power meter; OSA: optical spectrum analyzer; LAN: local area network; USB: universal serial bus).

Our experiment studies a silicon nitride photonic chip. The chip shown in Fig. 6.7 is fabricated using the double-stripe waveguide technology with LioniX BV [119]. The waveguides comprise SiO_2 cladding and two strips of Si_3N_4 layers stacked on top of each other with SiO_2 as an intermediate layer. The strips are constructed to be 1.5 μm wide, and the Si_3N_4 layers and SiO_2 intermediate layers are formed to be 170 and 500 nm thick, respectively. This allows < 100 μm bending radius with a propagation loss of < 0.2 dB/cm for TE polarization and single-mode operation at 1550 nm with a high index contrast. All waveguide inputs and outputs are pigtailed with a polarization maintaining fiber (PMF) array. The layout of the chip is sketched in Fig. 6.4. Our research focuses on stabilizing the operation wavelengths of the two MZI-based WDMs when internal and external heat disturbances occur, as explained in Fig. 6.1 and Fig. 6.2. All heaters that are used to control the phase shift have a nominal resistance of 600 Ω.

To have a reference point at a specific wavelength, calibration on applied voltage inputs and correlated wavelength output are conducted. Open loop calibration experiments are carried out by collecting data of applied voltage and wavelength output response. A Yenista® OSA20 optical spectrum analyzer is used to confirm the wavelength outputs. These applied voltages and wavelength outputs data are then used as a lookup table on programing the feedback control. The feedback control points are at channel 1 and channel 4 on heater controller. The range of the output of OSA 1 or trace window is set to 1558 to 1565 nm to avoid double peak detection. The second output at OSA 2 is also fixed to 1543 to 1549 nm for the same reason.

Fig. 6.7 shows a photograph of the Si_3N_4-based MZI thermooptic chip. The yellow parts are wire bonds for heaters, and the green parts are custom printed circuit boards connected via ribbon cable for providing voltage to the heaters. On the top side is the pigtailed fiber array and two green connector lines for ribbon cable connection to the heaters on the chip and integrated system controller (Fig. 6.8).

To verify our proposed dual proportional integral reference tracking algorithm, the measurement is arranged as shown in Fig. 6.6. Amplified spontaneous emission generates a broadband light source in the telecom C-band. The output is controlled with a tunable attenuator, a fiber inline polarizer and a polarization controller. The input power is monitored using a power meter and a 50:50 fiber coupler. In this experiment, 15 heaters are connected via electrical wires (black lines) bonded directly to the heater controller shown in Fig. 6.8.
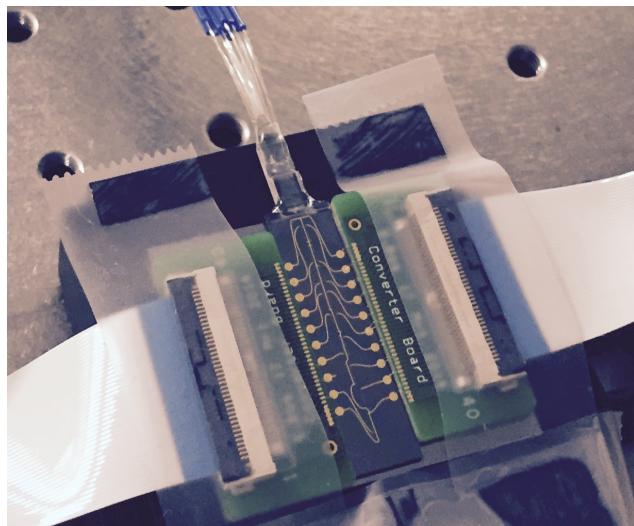
Fig. 6.7 A photograph of the Si_3N_4-based MZI thermooptic chip.
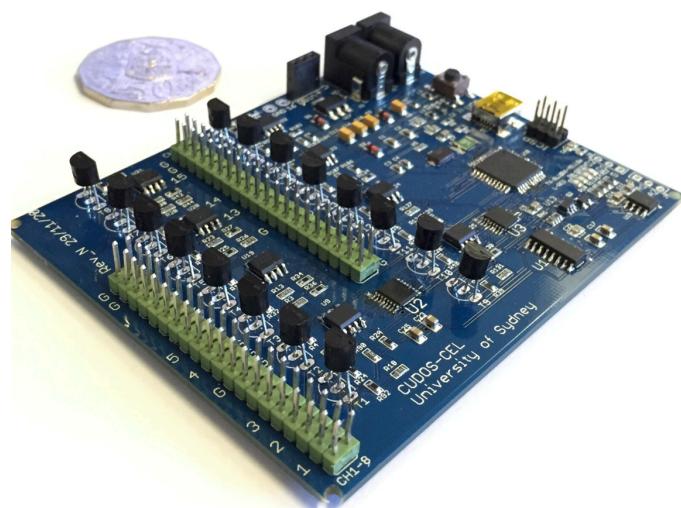
Fig. 6.8 A photograph of integrated system controller.

The heater controller as shown in Fig. 6.8 consists of 16 channel outputs, 15 of them used to provide voltages to the heaters on the photonic chip. The hardware is designed specifically based on open source Arduino using ATmega32u4 with two 16-bit octal digital analog converters, eight dual amplifiers, and 16 V follower circuits integrated onto one board. These electronic circuits as shown in Fig. 6.8 could be scaled for more channel outputs. Two outputs of the chips are connected to two Anritsu® MS9740A optical spectrum analyzers (OSAs). The OSA is used to obtain the operation wavelength of the WDMs. These signals are then used as the inputs in our control algorithm.

6.3   Experimental Results

Experiments are carried out to test the performance of the MIMO feedback control system. Three different conditions are used to evaluate the performance. The first test is SISO with internal disturbance. The second test is MIMO closed loop with internal disturbance. Finally, the MIMO system test with external disturbance is conducted.
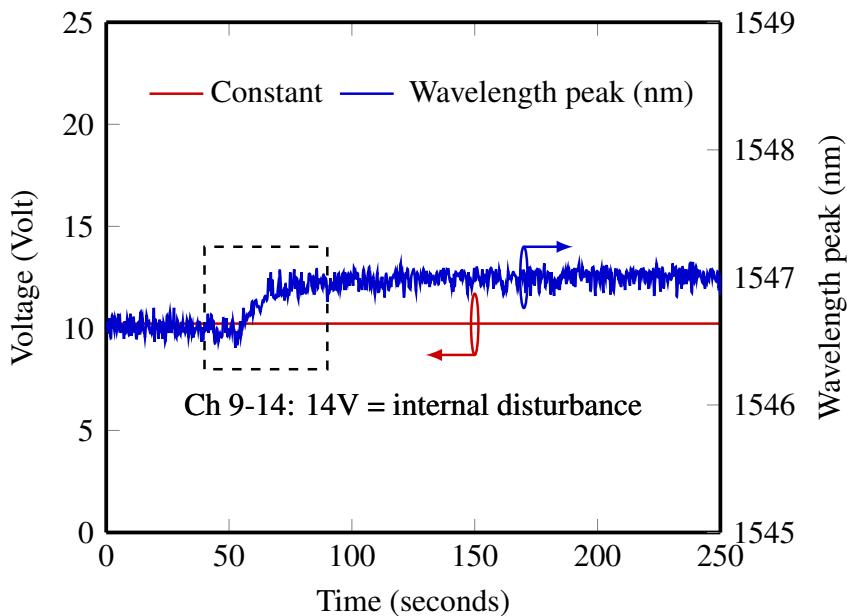
Fig. 6.9 Internal disturbance quantification

The closed loop systems are prepared with several procedures. The identification step response was collected from input and output experiment data as described in the transfer function model before the control parameters applied into a real system. This data is then analyzed and tuned using system identification system in MATLAB® [170]. The tuned parameters of the proportional integral term were then applied to the system. To make

feedback control test 1, wavelength output and voltage input were calibrated to acquire a set of targets. By applying voltages at channel 1 from 0 to 14 V, the peak wavelength output was varied from 1548.2 to 1543.2 nm. For feedback control test 2 at channel 4, changing the heater voltage from 0 to 14 V resulted in a wavelength peak from 1561.2 to 1552.88 nm. As the proportional and integral terms depend on coefficient Kp and Ti [1], the optimal values for the proportional and integral terms where 100 and 0.010 for Kp and Ti values.

Fig. 6.9 shows internal disturbance quantification from channel 9 to 14. The red line illustrates the voltage constant setting at Ch1. The blue line represents wavelength peak measurements when the voltage applied to the heaters. The wavelength drift starts at around 55 seconds when Ch9-14 are applied with 14 V inputs (internal disturbance).
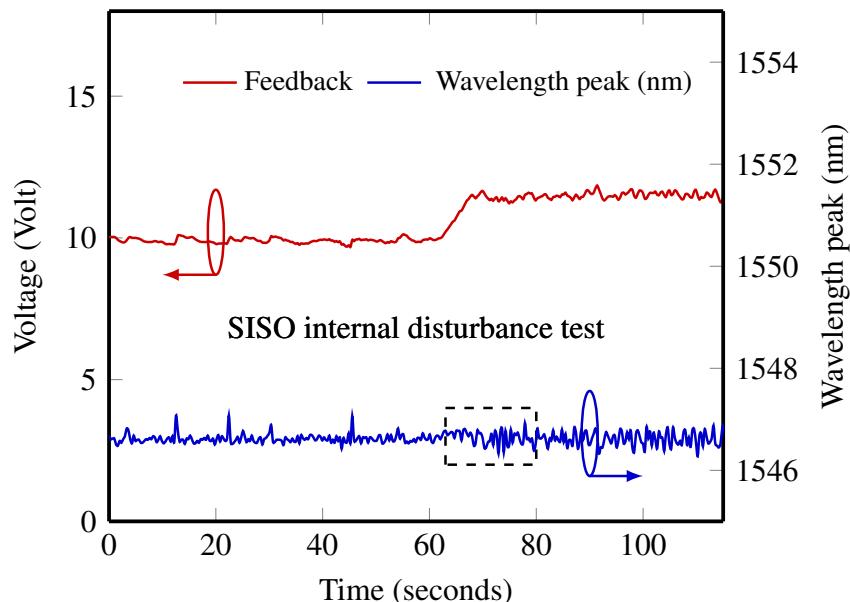
Fig. 6.10 Single closed loop with internal disturbance test.

Several channels are used to create internal disturbance of the photonic chip. Channels 9, 10, 11, 12, 13, and 14 are used to create an internal disturbance source by supplying 14 V for each channel. By activating these channels, the temperature increases because of the heat accumulation created by the channel heaters. This accumulation causes the wavelength drift. The internal disturbance quantification result is shown in Fig. 6.9. From this figure, the wavelength peak drifts from 1546.5 to 1547 nm or about 0.5 nm when the internal disturbance is active. The total of applied power for internal disturbance in this silicon nitride is calculated by $((Vin^2)/Resistance) * Channel\ active)$. The total was 0.32 W per 1 nm drift.

Fig. 6.10 presents single closed loop with internal disturbance test. The red solid line represents feedback voltage input of feedback point at Ch1 of the heater ($u1$). The blue solid line illustrates controlled wavelength peak signal ($y1$). The controller responses the change

of wavelength peak when internal disturbance occur at around 65 seconds by adjusting the feedback voltage input.

A single closed loop test result is shown in Fig. 6.10. Without internal disturbance, the peak wavelength output is around 1546.6 nm at 10.2 V. For this test, internal disturbance is started at about 65 s. Fig. 6.10 shows the feedback control system responded to the output change and stabilized the output. The response speed of the system was about 0.3 ms; this comes from the sample rate from the OSA through the local area network connection.
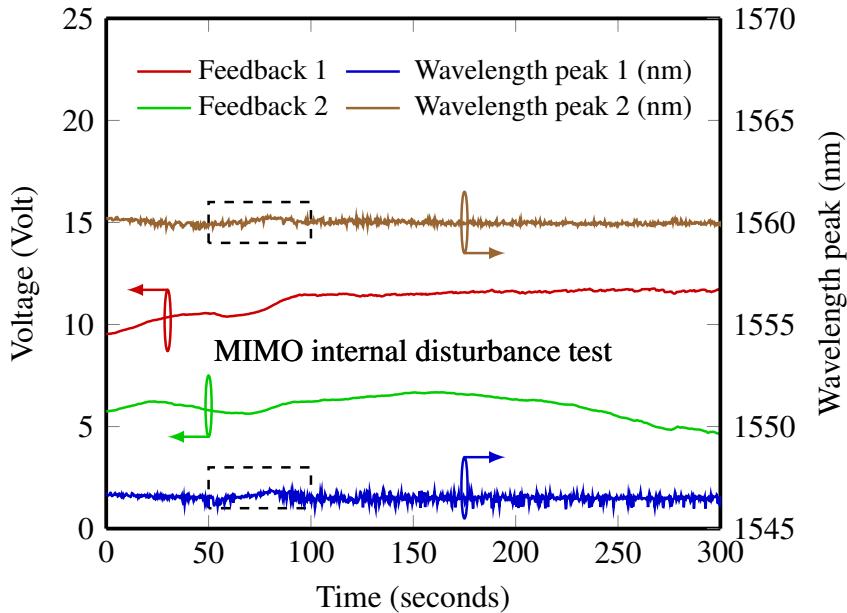
Fig. 6.11 MIMO closed loop with internal disturbance test.

Fig. 6.11 shows MIMO closed loop with internal disturbance test. The red line represents feedback voltage input of feedback point at Ch1 of the heater ($u1$). The brown line illustrates controlled wavelength peak signal ($y1$). The green solid line presents as feedback voltage input at feedback point at Ch4 of the heater ($u2$). The blue solid line depicts controlled wavelength peak signal ($y2$). The internal disturbance applies at around 50 seconds.

For the MIMO test with internal disturbance, the feedback control system is set at channel 1 and channel 4. Channels 2, 3, 5, 6, 7, 8, and 15 voltage inputs are situated as the calibration. Fig. 6.11 shows the test result with two inputs and two outputs. The two feedback control points at channels 1 and 4 applied a tuned robust dual proportional integral reference tracking technique with optimal parameters as described in the previous section. The internal disturbance started at around 70 s. Two target outputs are fixed at 1546.6 nm at output 1 and 1560.1 nm at output 2. This setup is based on the lookup table from the calibration result of each point to applied voltage correlation. Fig. 6.11 depicts the stabilization of two targets;

the feedback system adjust the inputs automatically depending on the drift. The two inputs change correspondingly and interact with each other to balance the two outputs.
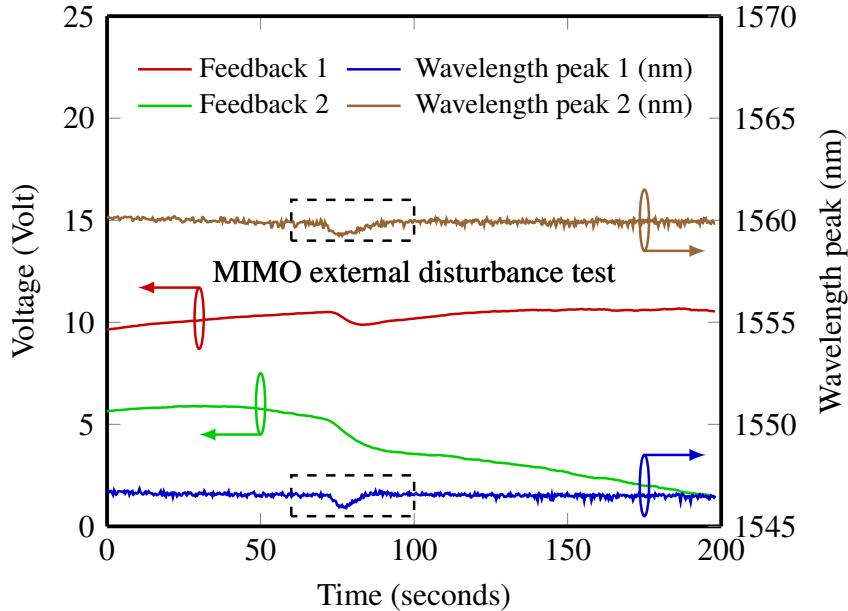
Fig. 6.12 MIMO closed loop with external disturbance test.

External disturbance is created by using a hot air blower to heat the silicon nitride chip from about 80 cm for about 15 s. The external heat from the blower also creates wavelength drift similar to internal disturbance. From the experiments, the temperature sensor shows an increase in temperature to about 34^oC from 24^oC. This setup is used to simulate extreme environment condition or volatile external environment.

Fig. 6.12 depicts a full system test with external disturbance. The red line represents feedback voltage input of feedback point at Ch1 of the heater ($u1$). The brown line illustrates controlled wavelength peak signal ($y1$). The green solid line presents as feedback voltage input at feedback point at Ch4 of the heater ($u2$). The blue solid line depicts controlled wavelength peak signal ($y2$). The heating started at 70 s. During this time, the MIMO closed loop systems also respond to or compensate for the disturbance by adjusting the voltages of both feedback control inputs to the target wavelength peak. In contrast with internal disturbance drift, this disturbance changes the wavelength peak to shift from higher to lower wavelength peak value. This condition is possibly due to the random heat effect during hot air blower heating to one of the phase shifters. As shown in Fig. 6.12, the feedback responds to the drift by lowering the voltage to adjust the wavelength direction to the target.

The present demonstration shows the utility of the approach for dual outputs. The same technique can be extended to larger numbers of inputs and outputs, and is an alternative to

other approaches such as dithering [129] and extremum seeking [167]. It allows solid control theory to be applied to the problem, leading to a more robust solution with improved transient response. Future work will involve larger degrees of integration, using schemes such as those of Ref. [166].

6.4   Summary

In conclusion, we proposed a MIMO control with a multi-proportional integral reference tracking technique combined with system identification scheme to maintain peak wavelength of PIC outputs. The control scheme can then be adaptively tuned by the integrated electronics circuit controller. We envision that such an adaptively tuned complex MZI structure should constitute a practical building block for reconfigurable and robust photonic systems, with the key advantages of enabling reliable and adaptive reconfiguration of complex PICs.

Chapter 7

Monolithic Segmented Transmitter

7.1   Introduction

The compatibility of CMOS electronics with photonic applications, can be harnessed to process, transmit and encode information with high power efficiency, low cost and high speed [2]. Silicon photonics and electronic integration promises to revolutionize new applications including telecommunications, sensor and quantum computing [175].

Electronic photonic integration has unlocked new levels of performance in optical transceivers for modern data centers and high performance computing. There are several schemes to bring about dramatic energy efficiency, cost reduction and performance for electronic and photonic integration, including hybrid to full monolithic solutions. Such integration can be either with silicon or other supported materials. Hybrid integration has been demonstrated recently for transceiver application using silicon for electronic driver and photonic circuits [176–182], InP-double heterojunction bipolar transistor electronic and electrooptic polymer for photonic device [183–186], III/V on silicon integration [107] [187–189], silicon hybrid plasmonic [190] [191], silica and lithium niobate hybrid [192] [193], silicon organic hybrid [194], silica with integrated distributed feedback laser arrays [195] and BiCMOS technology with InP [106] [196]. Hybrid techniques enable designers to focus on the optical and electrical functionality independently. This approach also permits optimizing the best chip technology for each purpose. However, due to separate electrical and optical circuit design environments, hybrid integration poses another challenge in co-optimization of the components. Monolithic integration has been demonstrated recently on silicon for electronic and photonic components [36] [197–201], GaAs [202], BiCMOS [108] [203–208], silicon with distributed feedback laser [209] and GeSi [210]. They allow component co-optimization within a single electronic/photonic design environment, and permits for disposition prior to assembly and functional wafer level testing to optimize yield and minimize cost.

The main challenges in transceiver design include how to maximize the optical modulation, improve receiver sensitivity, optimize energy efficiency and reach the optical link budget. Multi segments design of optical Mach Zehnder modulators (MZM) has attracted many research groups to tackle these challenges in the past few years. This design choice offer some advantages. First, segmented design reduces the lumped device capacitance seen by each driver segment, thus enabling extended modulation bandwidth. Furthermore, segmented MZMs can eliminate a significant direct current (DC) power draw because it does not require termination resistor. This permits a larger peak-to-peak RF drive to be realized from a given technology. Previous segmented designs have been reported on hybrid silicon [107], [106], [203] [208] and monolithic BiCMOS technology [108].

Monolithic CMOS segmented MZM should be more straightforward to design due to its unified electronic/photonic environment. This design choice also gives an ability to reduce parasitic capacitance, which would have a larger impact on MZM designs with a high degree of segmentation, since the driver power consumption scales with the total capacitance of the modulator. Therefore, minimizing parasitic capacitance can reduce power consumption.

In this chapter, we present a monolithically integrated CMOS nanophotonic multi segments Mach-Zehnder transmitter design. The transmitter and electronic driver are fully integrated in a 90 nm CMOS process. We report on three segments transmitter with low insertion loss at 1.5 dB and low transmitter link sensitivity at -14.1 dBm at BER = 10^{-12} at 12.5 Gbps. In addition, we demonstrate a novel monolithic six segments transmitter design with 1.3 pJ/bit at 12.5 Gbps and 1.4 pJ/bit at 16 Gbps power efficiency.
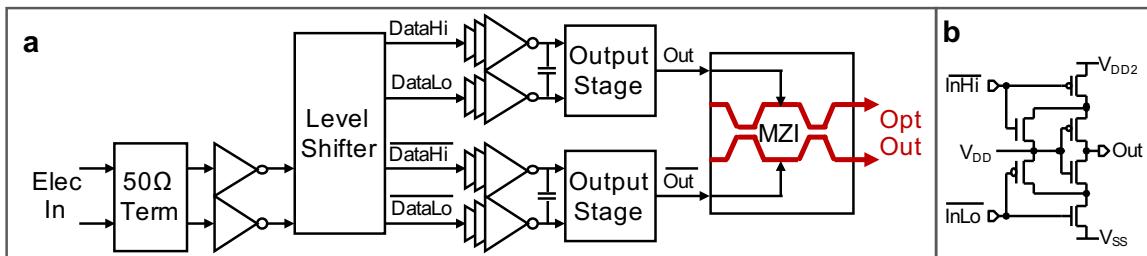
Fig. 7.1 TX block diagram with three segments MZM driver

7.2 Segmented Mach Zehnder Design

7.2.1 Three Segmented Design and CMOS Design

Fig. 7.1 shows a three segments transmitter block diagram and CMOS driver. This driver has 50 Ω on-chip termination to ground with differential inputs. The output stage employs

cascoding to limit the static voltage across any device to VDD (positive supply voltage) while providing VSS (negative supply voltage) to VDD2 output switch. This CMOS driver circuits is the modified version of the driver in [211], eliminating the CML block.
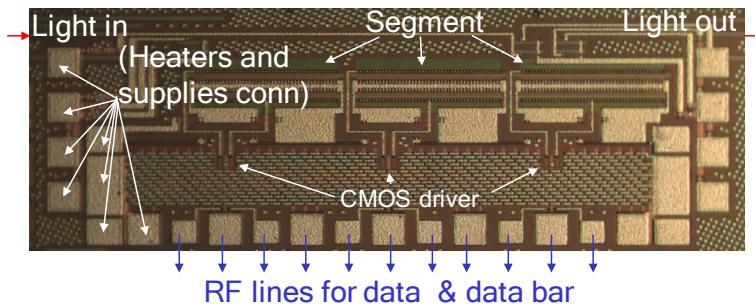
Fig. 7.2 Photomicrograph of the three segments MZM chip

Fig. 7.2 presents a photomicrograph of monolithic three segments MZM. The CMOS driver and photonic device were designed for a low loss optical transmitter targeting short-reach optical interconnect applications at 1.3 μm. This monolithic MZM has three segments on each arm with 440 μm long electro-optic phase shifter within each segment. Furthermore, the three segments transmitter has two passive waveguides with length of 40 μm and 980 μm. There are two thermal heaters available within each of the input and output coupler for tuning the best extinction ratio. This ratio is achieved with a 50/50 splitting. Moreover, thermal phase shifter is included on each MZM arm. In order to measure insertion loss, a reference straight waveguide is also designed and aligned with the segmented MZM.
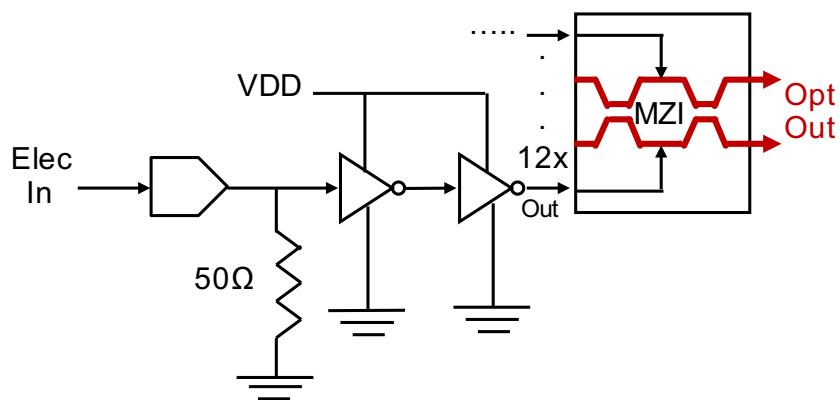
Fig. 7.3 TX block diagram with six segments MZM driver
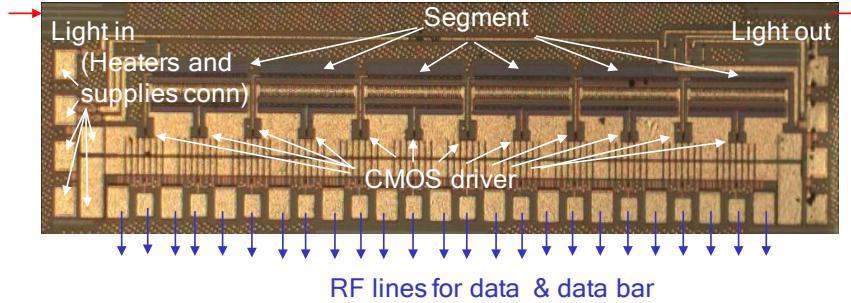
Fig. 7.4 Photomicrograph of the six segments MZM chip

7.2.2   Six Segmented Design and CMOS Driver

Fig. 7.3 shows a six segments MZM CMOS driver with transmitter block diagram. The CMOS driver has 50 Ω on chip termination to ground with single ended input and VDD voltage source, and can drive 12 single ended inputs. Fig. 7.4 presents a photomicrograph of a monolithic six segments MZM. Similar to the three segments design, it is designed for short reach optical interconnect applications. This segmented MZM has six segments on each arm and electrooptic phase shifter within each arm. In addition, the six segments design has five passive waveguides. Thermal heaters are also available on six segments modulator for coupler and phase shifter tuning.

7.3   Experimental Setup

Both three and six segmented have been realized using IBM's CMOS9WG and operate at 1310 nm wavelength. Fig. 7.5 shows the schematic of the three segments MZM experimental setup (PC: Polarization Controller, PM: Power Meter, OA: Optical Amplifier, VOA: Variable Optical Attenuator). A distributed feedback (DFB) laser (ILX lightwave LDCC-3916) is used to supply light input. A polarization controller is positioned before the MZM input. Single mode tapered-lensed fibers placed with 3-axis precision stages are employed to edge coupled the light to the MZM. A power monitor is used to measure both segments MZM output with thermal tuning on the couplers to achieve 50/50 % splitting ratio. A pattern generator is employed to generate an NRZ PRBS 2^7-1 sequence. The differential inputs of each segment of this three segments MZM ($D1$-$D3$/data and $\overline{D1}$-$\overline{D3}$/data bar) are arranged in a push pull configuration. Electrical radio frequency phase shifter are used to finely control the delay of the driving signals.
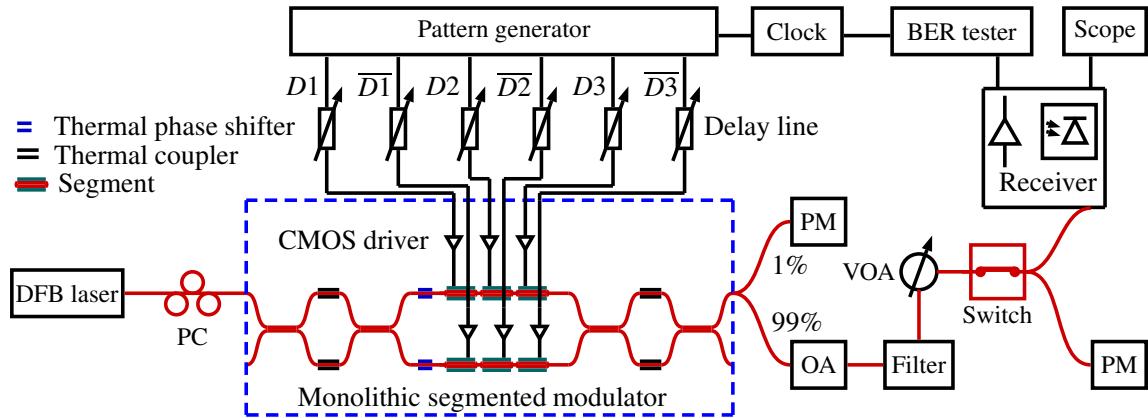
Fig. 7.5 Schematic of three segments MZM experimental setup.
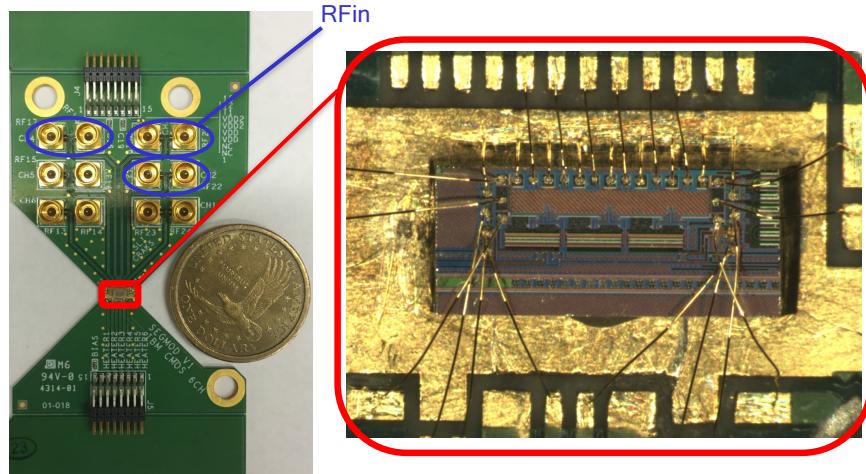
Fig. 7.6 Custom PCB and photomicrograph of three segments MZM

Ribbon cables are employed for supplying DC biases to the thermal phase shifter and driver circuits, via a custom printed circuit board (PCB) as shown in Fig. 7.6. The monolithic segmented MZM transmitter is wire bonded to the custom PCB which has matched impedance high speed cable connectors. The bias voltage of the cathode modulator is 2.4 V. VDD is supplied at 1.2 V while VDD2 is supplied at 2.4 V. Both VDD and VDD2 voltage are set at these conditions to achieve transmitter functionality while minimizing power consumption.

Output light from monolithic MZM transmitter is tapped 1% for power monitoring while 99% passes through an optical amplifier. This amplified optical signal goes through filter, followed by a variable optical attenuator (VOA) and optical switch to select between power meter and a sampling scope with a 30 GHz photo-detector plugin with reference receiver (RX). The RX uses a commercial 43 Gbps (MPRV133XU U^{2}t) with an integrated trans-
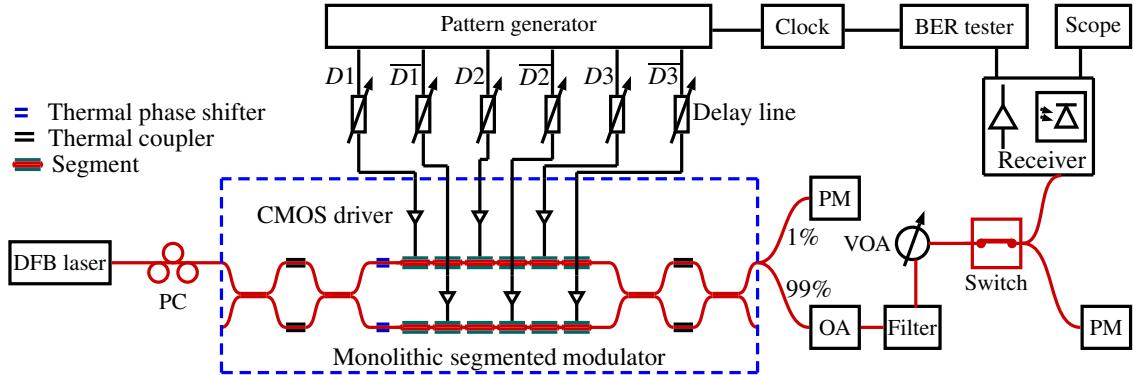
Fig. 7.7 Schematic of six segments MZM experimental setup.

impedance amplifier (TIA). The output from reference receiver is fed into a scope (Textronix DSA8300) and BER tester (SHF1001B). A pattern generator (SHF10001-SHF121044), BER tester and scope are triggered by an external clock from the signal generator.
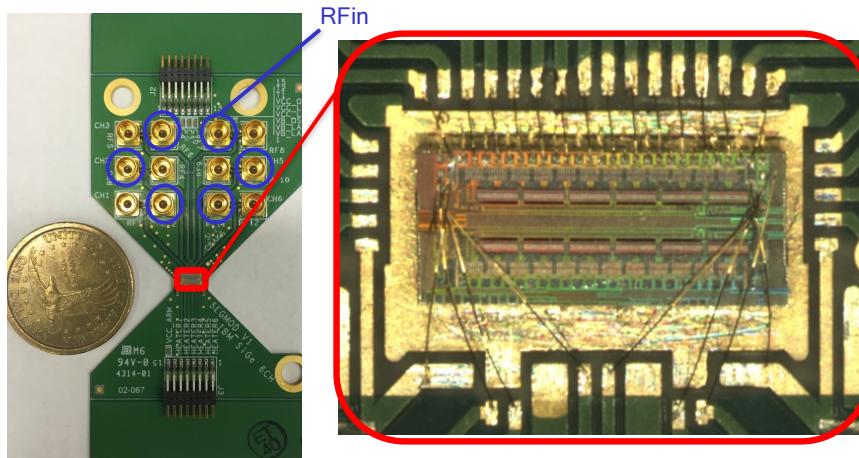
Fig. 7.8 Custom PCB and photomicrograph of six segments MZM

Fig. 7.7 shows a schematic of six segments MZM experimental setup. In general, the setup is similar with three segments MZM except the driving circuit connection. In six segments MZM setup, each pair of segments is driven single ended, means that the line of each pairs is terminated with 50 Ω impedance. For this experimental setup, the VDD is supplied at 1.2 V and the cathode modulator biased at 0.6 V. Fig. 7.8 shows a custom circuit board (left) and a photomicrograph of wire bonding connection of monolithic six segments MZM. Due to a limitation in the number of RF input channels available, the setup only use a single ended configuration as shown in Fig. 7.7.

7.4   Experimental Results

We run the transmission experiments at different bit rates for three and six segments MZM transmitters and explore different bias voltage.
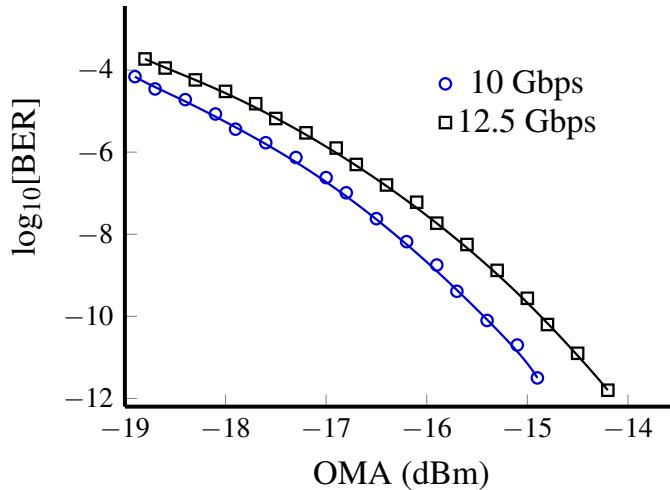
Fig. 7.9 Receiver sensitivity of three segments modulator

7.4.1   Three Segmented MZM Test Results

Fig. 7.9 shows the receiver sensitivity test of three segments MZM with different bit rates at 10 Gbps and 12.5 Gbps. The curves in this figure indicate -14.9 dBm optical modulation amplitude (OMA) link sensitivity for 10 Gbps and -14.1 dBm for 12.5 Gbps, both at BER = 10^{-12}. Jitter measurement for 10 Gbps and 12.5 Gbps are shown in Fig. 7.10. From this bathub curve, the eye opening is 0.65 UI at BER = 10^{-12} with 10.77 ps random jitter and 24.05 ps deterministic jitter at 10 Gbps. At 12.5 Gbps, the curve exhibits 0.5 UI eye-opening at BER = 10^{-12} with 11.36 ps random jitter and 25.71 ps deterministic jitter.

Fig. 7.11 presents eye diagram for both transmitter and receiver at 10 Gbps and 12.5 Gbps. The receiver electrical eye diagram exhibits 180 mV eye opening at 10 Gbps. Similar to 10 Gbps, the receiver electrical eye at 12.5 Gbps is 180 mV, both with -4.9 dB receiver input power. The jitter contributions as shown in eye diagrams are mainly from low precision delay matching of driving signal between segments. The power consumption for both 10 Gbps and 12.5 Gbps CMOS driver were 116 mW and 144 mW respectively, which corresponds to a power efficiency of 11.64 pJ/bit and 11.52 pJ/bit.

The receiver sensitivity and jitter measurement were also conducted with different bias voltage. Fig. 7.12 shows -11.9 dBm OMA link sensitivity at a BER = 10^{-12} at 12.5 Gbps
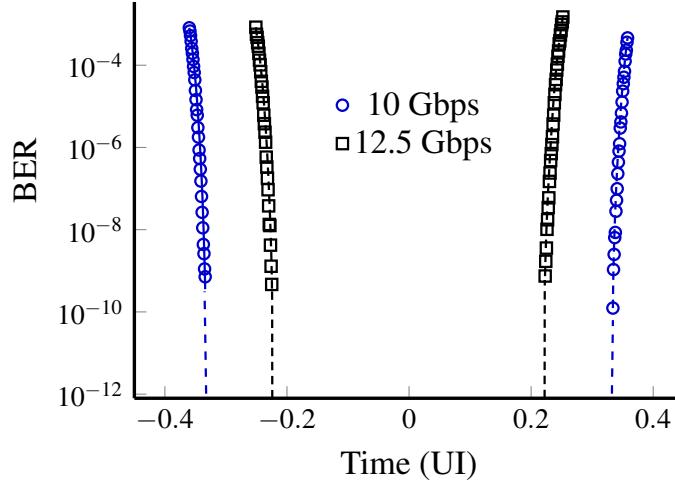
Fig. 7.10 Three segments MZM jitter measurement
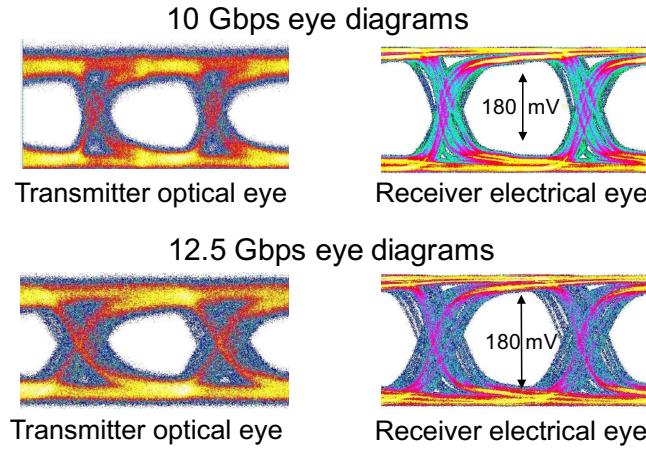
Fig. 7.11 Three segments MZM transmitter and receiver eye diagrams

with bias 2.8 V. This figure exhibits -4 dBm different with bias at 2.4 V at the same BER and bit rate. From jitter measurement as shown in Fig. 7.13, the eye opening is 0.43 UI at BER = 10^{-12} with 32.81 ps random jitter and 23.45 ps deterministic jitter. This result shows smaller opening eye and higher jitter compared to 2.4 V bias voltage setting. The monolithic three segments MZM transmitter exhibited a 5.2 dB extinction ratio and low insertion loss of 1.5 dB.

We also characterized the transmitter loss performance by calculating its relative optical modulation amplitude (R-OMA) [36], which defined as the transmitter output OMA divided by CW optical input into the transmitter. Since this is an integrated device, this calculation does not include optical IO coupling loss on and off chip, and the chip was designed to
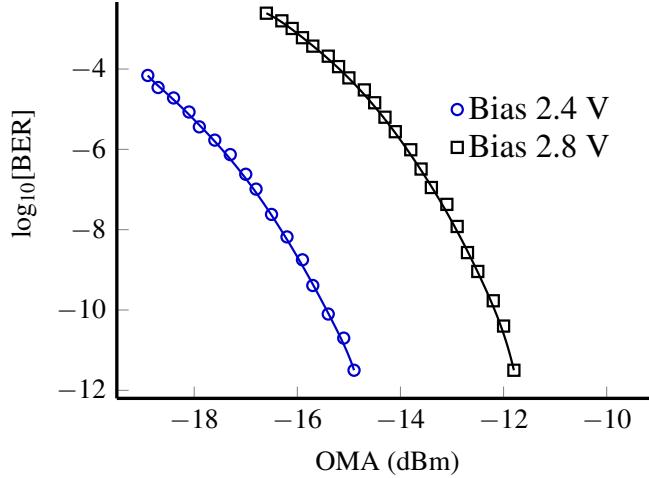
Fig. 7.12 Three segments modulator with different bias voltage
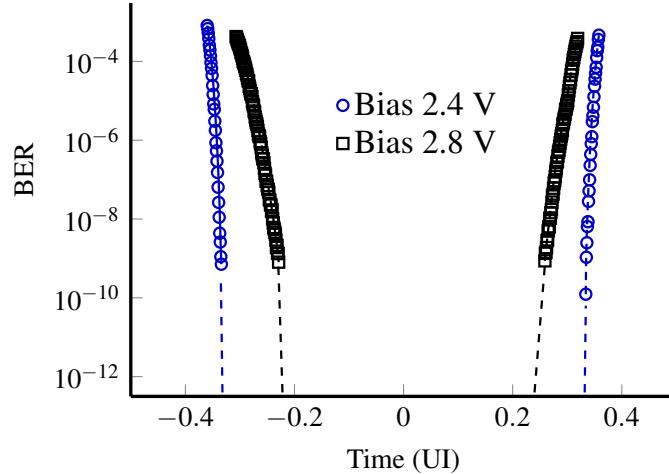
Fig. 7.13 Three segments MZM jitter measurement with different bias voltage

enable low-loss fiber packaging without any specific structure. The 5.2 dB extinction ratio and 1.5 dB insertion loss from this transmitter exhibits a 4.2 dB R-OMA, which shows better compared with other result in the literature. For instance, this R-OMA is 2.3 dB better than the R-OMA of -6.5 dB realized in [199] at 20 Gbps, and 2.9 dB better than the -7.1 dB R-OMA presented in [196] at 50 Gbps. We note that although our demonstration exhibits a maximum bit rate of 12.5 Gbps, other monolithic transmitter from this technology have shown operation out to 32 Gbps [199].

7.4.2   Six Segmented MZM Test Results

From jitter measurement results as shown in Fig. 7.14, the opening eye for 10 Gbps is 0.615 UI with 21.61 random jitter and 16.84 deterministic jitter. At 12.5 Gpbs the opening eyes is 0.5 UI with 17.28 random jitter and 14.23 deterministic jitter. In higher bit rates at 16 Gbps, the opening eyes close to 0.29 UI. All of above jitter measurements are at BER = 10^{-12}.
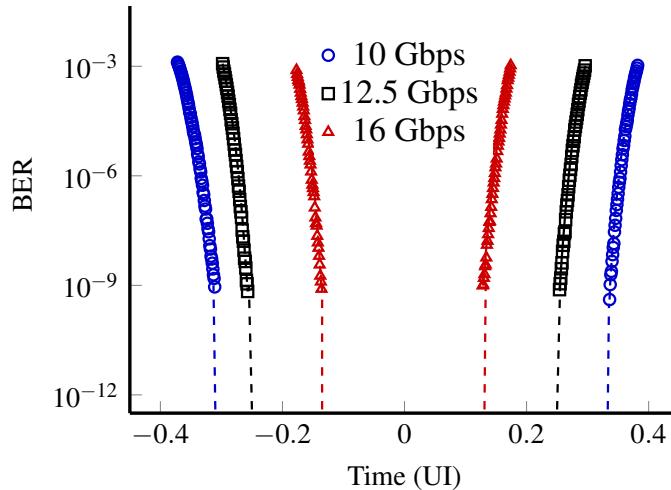
Fig. 7.14 Six segments MZM jitter measurement
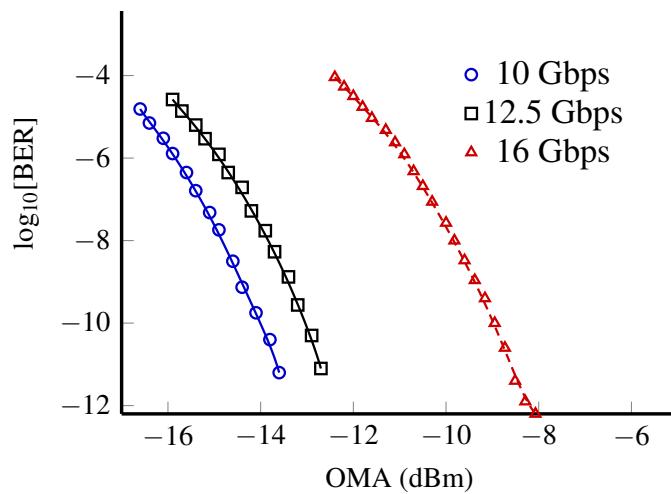
Fig. 7.15 Receiver sensitivity of six segments modulator

The receiver sensitivity measurement results for six segments MZM are presented in Fig. 7.15, confirming error free operations for three different bit rates. At 10 Gbps, the OMA is -13.8 dBm at a BER = 10^{-12}. For test at 12.5 Gbps, the OMA is -12.8 dBm at the same BER = 10^{-12}. The eye diagrams for segmented MZM transmitter and receiver are presented

in Fig. 7.16 with three different bit rates, all with -4.9 dBm receiver input power. Receiver sensitivity and BER test experiment with different PRBS inputs were also conducted.

10 Gbps eye diagrams

Transmitter optical eye   Receiver electrical eye

12.5 Gbps eye diagrams

Transmitter optical eye   Receiver electrical eye

16 Gbps eye diagrams

Transmitter optical eye   Receiver electrical eye
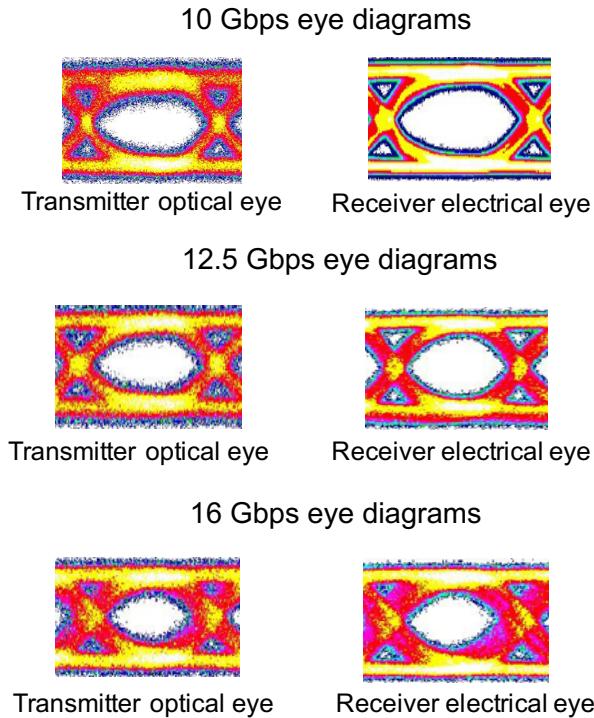
Fig. 7.16 Six segments MZM transmitter and receiver eye diagrams

Fig. 7.17 shows six segments MZM receiver sensitivity with different PRBS inputs: PRBS 2^7-1 and PRBS 2^{31}-1 at 10 Gbps and 16 Gbps. From this figure, the OMA penalty for 10 Gbps is about -1 dBm at a BER = 10^{-12}. The larger penalty is shown at 16 Gbps, which larger error occurs with PRBS 2^{31}-1 at a BER = 10^{-8}. Fig. 7.18 presents jitter measurement at 10 Gbps with different PRBS inputs. For PRBS 2^7-1 input, the opening eye is 0.65 UI at BER = 10^{-12}. For PRBS 2^{31}-1, the eye opening is 0.45 UI at BER = 10^{-12}.

Power consumption for six segments transmitter CMOS driver at 10 Gbps and 12.5 Gbps were 15.6 mW and 16.8 mW respectively, which corresponds to a power efficiency of 1.6 pJ/bit and 1.3 pJ/bit. For 16 Gbps, the driver power consumption was 22.8 mW or equal to 1.4 pJ/bit power efficiency. The monolithic six segments transmitter showed 2.65 dB insertion loss, with a 4.2 dB extinction ratio under operation at 12.5 Gbps. For 10 Gbps and 16 Gbps, the extinction ratio were 4.1 dB and 3.6 dB respectively. We also characterized the R-OMA of six segments MZM transmitter. The 2.65 dB insertion loss and 4.2 dB extinction ratio at 12.5 Gbps from this transmitter gives a -6.1 dB R-OMA which also shows better result compared with the literature [196, 199].
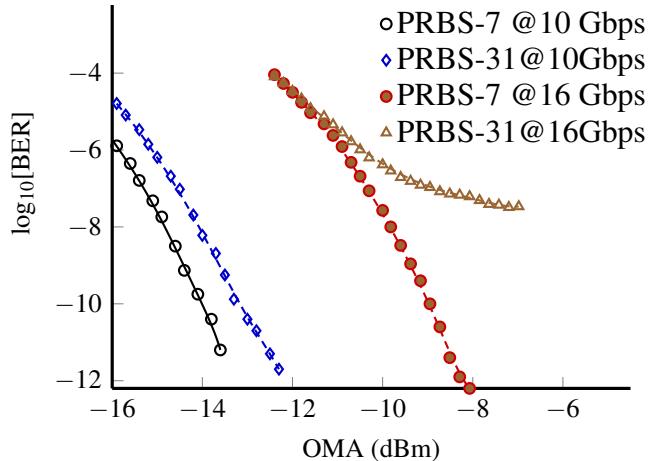
Fig. 7.17 Six segments MZM receiver sensitivity with different PRBS input
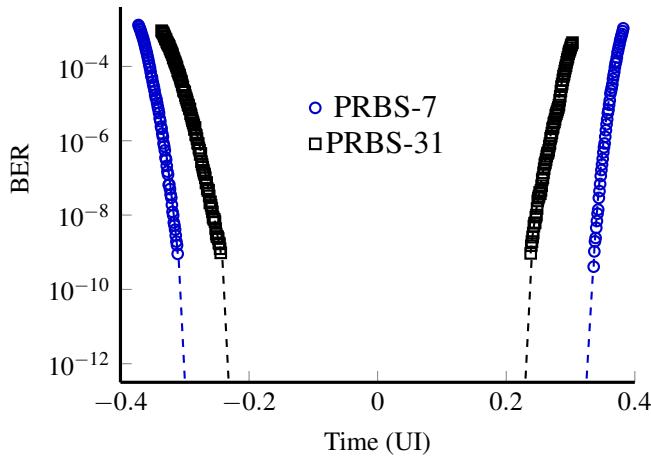
Fig. 7.18 Six segments MZM jitter measurement with different PRBS input

7.5   Summary

Monolithically integrated CMOS nanophotonic multi segments Mach-Zehnder transmitters have been successfully realized in IBM's CMOS9WG technology. The three segments MZM achieves low insertion loss at 1.5 dB and -14.1 dBm transmitter link sensitivity at 12.5 Gbps at BER = 10^{-12}. The transmitter also showed better R-OMA at about 2.6 dB. The six segments MZM attains 1.3 pJ/bit at 12.5 Gbps power efficiency. Error free testing was demonstrated with a PRBS 2^7-1 sequence, as is suitable for links that use a coding scheme such as 8b/10b, which has historically been extensively used in high performance computing systems. The monolithic CMOS nanophotonic multi segments MZM design holds promise for high energy efficiency applications.

Chapter 8

Conclusion and Outlook

Electronic photonic integration provides a wide range of unique advantages which can be exploited for a variety of applications, including quantum computing, telecommunications and high performance computing. This thesis has presented the use of hybrid and monolithic integration combine with several control techniques for enabling better system accuracy, compactness, reconfigurability, and energy efficiency.

8.1 Summary of Achievements

The specific aims and contributions of this thesis are listed in Section 1.1 and Section 1.2, and experimental finding are detailed in Chapters 3 through 7. The primary aim of this thesis was the development of methods that allow electronic-photonic system to have high accuracy, reconfigurability and energy efficiency for quantum and communication applications. The key contribution of this work lie in the proposed hybrid and monolithic electronic-photonic system design. These design methodologies rely on the integration of low loss and CMOS compatible material such as silicon and silicon nitride combine with microcontroller, FP-GAs, dual proportional integral reference tracking technique and segmented modulator design. These system have been designed to allow the discovery of integrated entanglement sources and analysis circuits on a chip and also creating near-deterministic heralded single-photon sources for large scale quantum computation. A two-photon interference (TPI) fringe with 88.4% visibility without subtracting any noise was measured. This result displayed not only high performance but also compactness, tunability and stability offered by time-bin entanglement circuits. Moreover, the probability of the single-photon output has been demonstrated with 100% enhancement without introducing additional multi-photon noise using fibre-integrated optics and off-the-shelf electronic components. This work also addressed issues with accuracy and reconfigurability, encouraging adoption by reducing

the cost of implementation typically associated with these methods. The MIMO control with a multi-proportional reference tracking technique combine with system identification scheme improved the control accuracy by reducing peak drift due to internal and external disturbances from 0.5 to 0.1 nm. Furthermore, nanophotonic multi segments modulator have been successfully integrated monolithically and realized in IBM's CMOS9WG technology. The segmented design achieves low insertion loss at 1.5 dB and -14.1 dBm transmitter link sensitivity at 12.5 Gbps at BER = 10^{-12}. The six segmented design attains 1.3 pJ/bit at 12.5 Gbps power efficiency, demonstrates error free with a PRBS 2^7-1 sequence which suitable for high performance computing system with high energy efficiency.

8.2 Roadmap to Future Research

One of the key goals of electronic photonic integration is the creation of a fully compact, reliable, reconfigurable system with high energy efficiency. This thesis has demonstrated that hybrid and monolithic integration provide effective means to achieve this goal. The challenge that remain now is the full integration and the capability to apply in the real world, in particular, photon detector, laser and modulator.

To this end, recently IBM, Samsung and GlobalFoundries jointly announced the capability of continuing Moore's Law that enabling electronic circuits to be scaled down to 5 nm. This will enable extremely high dense electronic circuit which allow much more sophisticated integration with CMOS compatible photonic integrated circuits. Nevertheless, as progress is made in these areas, the objective is to migrate electronic control functionalities to monolithic circuits, preferably in silicon, so as to finally achieve more complex devices and reduce fabrication cost through high integration density.

An ultimate benefit of full electronic and photonic integration is the possibility for packaging of both nanoelectronic and nanophotonic circuits into a single component. Integration can reduce the current gap in form-factor between electronic and photonic circuit, and lead to a fully-packaged control system platform with high accuracy, reconfigurability and energy efficiency brought about through the power of nanoelectronic and nanophotonic circuits.

References

[1] K. J. Aström and R. M. Murray, *Feedback systems: an introduction for scientists and engineers*. Princeton university press, 2010.

[2] L. Pavesi, D. J. Lockwood *et al.*, *Silicon Photonics III*. Springer, 2016.

[3] M. S. Nawrocka, T. Liu, X. Wang, and R. R. Panepucci, "Tunable silicon microring resonator with wide free spectral range," *Applied physics letters*, vol. 89, no. 7, pp. 71 110–71 110, 2006.

[4] J. Mower and D. Englund, "Efficient generation of single and entangled photons on a silicon photonic integrated chip," *Physical Review A*, vol. 84, no. 5, p. 052326, 2011.

[5] C. Sun, M. T. Wade, Y. Lee, J. S. Orcutt, L. Alloatti, M. S. Georgas, A. S. Waterman, J. M. Shainline, R. R. Avizienis, S. Lin *et al.*, "Single-chip microprocessor that communicates directly using light," *Nature*, vol. 528, no. 7583, pp. 534–538, 2015.

[6] C. Xiong, X. Zhang, A. Mahendra, J. He, D.-Y. Choi, C. Chae, D. Marpaung, A. Leinse, R. Heideman, M. Hoekman *et al.*, "Compact and reconfigurable silicon nitride time-bin entanglement circuit," *Optica*, vol. 2, no. 8, pp. 724–727, 2015.

[7] A. Mahendra, C. Xiong, X. Zhang, B. J. Eggleton, and P. H. W. Leong, "Dynamic thermal control of silicon nitride photonic integrated circuits," in *Optical Fibre Technology, 2015 40th Australian Conference on*, 2015.

[8] C. Xiong, X. Zhang, Z. Liu, M. Collins, A. Mahendra, L. Helt, M. Steel, D.-Y. Choi, C. Chae, P. Leong *et al.*, "Active temporal multiplexing of indistinguishable heralded single photons," *Nature communications*, vol. 7, 2016.

[9] A. Mahendra, C. Xiong, X. Zhang, B. J. Eggleton, and P. H. W. Leong, "Multiwavelength stabilization control of a thermo-optic system with adaptive reconfiguration," *Appl. Opt.*, vol. 56, no. 4, pp. 1113–1118, Feb 2017. [Online]. Available: http://ao.osa.org/abstract.cfm?URI=ao-56-4-1113

[10] A. M. et.al, "Monolithically integrated cmos nanophotonic segmented mach zehnder transmitter," in *CLEO: Science and Innovations*, 2017.

[11] I. Present, "Cramming more components onto integrated circuits," *Readings in computer architecture*, vol. 56, 2000.

[12] D. C. Schleher, *Electronic warfare in the information age*. Artech House, Inc., 1999.

[13] A. D. Chandler, T. Hikino, A. Von Nordenflycht, and A. D. Chandler, *Inventing the electronic century: The epic story of the consumer electronics and computer industries, with a new preface.* Harvard University Press, 2009, vol. 47.

[14] R. L. Freeman, *Telecommunication system engineering.* John Wiley & Sons, 2015, vol. 82.

[15] N. Budnev, I. Astapov, A. Bogdanov, V. Boreyko, M. Büker, M. Brückner, A. Chiavassa, A. Gafarov, O. Chvalaev, N. Gorbunov *et al.*, "Taiga the tunka advanced instrument for cosmic ray physics and gamma astronomy—present status and perspectives." *Journal of Instrumentation*, vol. 9, no. 09, p. C09021, 2014.

[16] I. Willner, R. Baron, and B. Willner, "Integrated nanoparticle–biomolecule systems for biosensing and bioelectronics," *Biosensors and Bioelectronics*, vol. 22, no. 9, pp. 1841–1852, 2007.

[17] F. A. Zwanenburg, A. S. Dzurak, A. Morello, M. Y. Simmons, L. C. Hollenberg, G. Klimeck, S. Rogge, S. N. Coppersmith, and M. A. Eriksson, "Silicon quantum electronics," *Reviews of modern physics*, vol. 85, no. 3, p. 961, 2013.

[18] R. R. Schaller, "Moore's law: past, present and future," *IEEE spectrum*, vol. 34, no. 6, pp. 52–59, 1997.

[19] R. N. Noyce, "Microelectronics," *Scientific American*, vol. 237, no. 3, pp. 62–69, 1977.

[20] S. Chih-Tang, "Evolution of the mos transistor-from conception to vlsi," *Proceedings of the IEEE*, vol. 76, no. 10, pp. 1280–1326, 1988.

[21] A. E. Dunlop, W. J. Evans, and L. A. Rigge, "Managing complexity in ic design—past, present, and future," *Bell Labs technical journal*, vol. 2, no. 4, pp. 103–125, 1997.

[22] G. E. Moore, "Intel: Memories and the microprocessor," *Daedalus*, pp. 55–80, 1996.

[23] [Online]. Available: https://www.qualcomm.com/news/releases/2016/11/17/qualcomm-and-samsung-collaborate-10nm-process-technology-latest-snapdragon

[24] T. He, S. Krishnamurthy, L. Luo, T. Yan, L. Gu, R. Stoleru, G. Zhou, Q. Cao, P. Vicaire, J. A. Stankovic *et al.*, "Vigilnet: An integrated sensor network system for energy-efficient surveillance," *ACM Transactions on Sensor Networks (TOSN)*, vol. 2, no. 1, pp. 1–38, 2006.

[25] G. M. Rebeiz, *RF MEMS: theory, design, and technology.* John Wiley & Sons, 2004.

[26] E. Garmire, J. Hammer, H. Kogelnik, and F. Zernike, *Integrated optics.* Springer Science & Business Media, 2013, vol. 7.

[27] S. Brown, *Fundamentals of digital logic design with VHDL.* Tata McGraw Hill, 2010.

[28] M. Richardson and S. Wallace, *Getting started with raspberry PI.* " O'Reilly Media, Inc.", 2012.

[29] (2015). [Online]. Available: http://www.arduino.cc

[30] G. Keiser, *Optical communications essentials*. McGraw-Hill, 2003.

[31] N. Savage, "Linking with light [high-speed optical interconnects]," *Spectrum, IEEE*, vol. 39, no. 8, pp. 32–36, 2002.

[32] C. Batten, A. Joshi, J. Orcutt, A. Khilo, B. Moss, C. Holzwarth, M. Popovic, H. Li, H. I. Smith, J. Hoyt *et al.*, "Building manycore processor-to-dram networks with monolithic silicon photonics," in *High Performance Interconnects, 2008. HOTI'08. 16th IEEE Symposium on*. IEEE, 2008, pp. 21–30.

[33] L. Chrostowski and M. Hochberg, *Silicon Photonics Design: From Devices to Systems*. Cambridge University Press, 2015.

[34] R. Soref, "The past, present, and future of silicon photonics," *IEEE Journal of selected topics in quantum electronics*, vol. 12, no. 6, pp. 1678–1687, 2006.

[35] G. T. Reed, *Silicon Photonics: the state of the art*. John Wiley & Sons, 2008.

[36] D. M. Gill, J. E. Proesel, C. Xiong, J. S. Orcutt, J. C. Rosenberg, M. H. Khater, T. Barwicz, S. Assefa, S. M. Shank, C. Reinholm *et al.*, "Demonstration of a high extinction ratio monolithic cmos integrated nanophotonic transmitter and 16 gb/s optical link," *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 21, no. 4, pp. 212–222, 2015.

[37] J. S. Orcutt, B. Moss, C. Sun, J. Leu, M. Georgas, J. Shainline, E. Zgraggen, H. Li, J. Sun, M. Weaver *et al.*, "Open foundry platform for high-performance electronic-photonic integration," *Optics express*, vol. 20, no. 11, pp. 12 222–12 232, 2012.

[38] G. Z. Xiao, Z. Zhang, F. G. Sun, and C. P. Grover, "Effects of environment temperature induced heater resistance change on the attenuation of mzi type variable optical attenuators," *Photonics Technology Letters, IEEE*, vol. 16, no. 2, pp. 482–484, 2004.

[39] M. Lenzi, S. Tebaldini, D. Di Mola, S. Brunazzi, and L. Cibinetto, "Power control in the photonic domain based on integrated arrays of optical variable attenuators in glass-on-silicon technology," *Selected Topics in Quantum Electronics, IEEE Journal of*, vol. 5, no. 5, pp. 1289–1297, 1999.

[40] T. Shibata, M. Okuno, T. Goh, T. Watanabe, M. Yasu, M. Itoh, M. Ishii, Y. Hibino, A. Sugita, and A. Himeno, "Silica-based waveguide-type 16 x 16 optical switch module incorporating driving circuits," *Photonics Technology Letters, IEEE*, vol. 15, no. 9, pp. 1300–1302, 2003.

[41] M. Harjanne, M. Kapulainen, T. Aalto, and P. Heimala, "Sub-s switching time in silicon-on-insulator mach-zehnder thermooptic switch," *Photonics Technology Letters, IEEE*, vol. 16, no. 9, pp. 2039–2041, 2004.

[42] C. K. Madsen, P. Oswald, M. Cappuzzo, E. Chen, L. Gomez, A. Griffin, A. Kasper, E. Laskowski, L. Stulz, and A. Wong-Foy, "Reset-free integrated polarization controller using phase shifters," *Selected Topics in Quantum Electronics, IEEE Journal of*, vol. 11, no. 2, pp. 431–438, 2005.

[43] Y. A. Vlasov, M. O'Boyle, H. F. Hamann, and S. J. McNab, "Active control of slow light on a chip with photonic crystal waveguides," *Nature*, vol. 438, no. 7064, pp. 65–69, 2005.

[44] C. Qiu, J. Shu, Z. Li, X. Zhang, and Q. Xu, "Wavelength tracking with thermally controlled silicon resonators," *Optics Express*, vol. 19, no. 6, pp. 5143–5148, 2011.

[45] K. Huang, H. Le Jeannic, J. Ruaudel, O. Morin, and J. Laurat, "Microcontroller-based locking in optics experiments," *Review of Scientific Instruments*, vol. 85, no. 12, p. 123112, 2014.

[46] W. D. Oliver, Y. Yu, J. C. Lee, K. K. Berggren, L. S. Levitov, and T. P. Orlando, "Mach-zehnder interferometry in a strongly driven superconducting qubit," *Science*, vol. 310, no. 5754, pp. 1653–1657, 2005.

[47] R. Palupi, A. Syahriar, A. Lubis, S. Rahardjo *et al.*, "Simulation of mach zehnder interleaver based thermo-optic effect in l-band range," in *Micro and Nanoelectronics (RSM), 2013 IEEE Regional Symposium on*. IEEE, 2013, pp. 269–272.

[48] X.-D. Wu, C. Schmidt-Hattenberger, K. Krüger, and J. Chen, "Temperature-controlled fiber bragg grating dynamic strain detection system," *Sensors and Actuators A: Physical*, vol. 119, no. 1, pp. 68–74, 2005.

[49] J. Snoddy, Y. Li, F. Ravet, and X. Bao, "Stabilization of electro-optic modulator bias voltage drift using a lock-in amplifier and a proportional-integral-derivative controller in a distributed brillouin sensor system," *Applied optics*, vol. 46, no. 9, pp. 1482–1485, 2007.

[50] K. Volyanskiy, J. Cussey, H. Tavernier, P. Salzenstein, G. Sauvage, L. Larger, and E. Rubiola, "Applications of the optical fiber to the generation and measurement of low-phase-noise microwave signals," *JOSA B*, vol. 25, no. 12, pp. 2140–2150, 2008.

[51] R. Amatya, C. W. Holzwarth, H. I. Smith, and R. J. Ram, "Precision tunable silicon compatible microring filters," *Photonics Technology Letters, IEEE*, vol. 20, no. 20, pp. 1739–1741, 2008.

[52] F. Kärtner, R. Amatya, M. Araghchini, J. Birge, H. Byun, J. Chen, M. Dahlem, N. DiLello, F. Gan, C. Holzwarth *et al.*, "Photonic analog-to-digital conversion with electronic-photonic integrated circuits," in *Proc. SPIE*, vol. 6898, no. 689806, 2008, pp. 689 806–15.

[53] D. T. Bui and B. Journet, "Electro-optic modulator bias point optimization by detecting its nonlinear behavior," in *Communications and Electronics (ICCE), 2010 Third International Conference on*. IEEE, 2010, pp. 118–123.

[54] B.-W. Shiau, T.-P. Ku, and D.-J. Han, "Real-time phase difference control of optical beams using a mach–zehnder interferometer," *Journal of the Physical Society of Japan*, vol. 79, no. 3, 2010.

[55] X.-s. Ma, S. Zotter, N. Tetik, A. Qarry, T. Jennewein, and A. Zeilinger, "A high-speed tunable beam splitter for feed-forward photonic quantum information processing," *Optics express*, vol. 19, no. 23, pp. 22 723–22 730, 2011.

[56] G. Xavier and J. von der Weid, "Stable single-photon interference in a 1 km fiber-optic mach–zehnder interferometer with continuous phase adjustment," *Optics letters*, vol. 36, no. 10, pp. 1764–1766, 2011.

[57] E. Camargo, H. Chong, and R. De La Rue, "2d photonic crystal thermo-optic switch based on algaas/gaas epitaxial structure," *Optics Express*, vol. 12, no. 4, pp. 588–592, 2004.

[58] R. Espinola, M. Tsai, J. T. Yardley, and R. Osgood Jr, "Fast and low-power thermooptic switch on thin silicon-on-insulator," *Photonics Technology Letters, IEEE*, vol. 15, no. 10, pp. 1366–1368, 2003.

[59] R. Jones, J. Doylend, P. Ebrahimi, S. Ayotte, O. Raday, and O. Cohen, "Silicon photonic tunable optical dispersion compensator," *Optics express*, vol. 15, no. 24, pp. 15 836–15 841, 2007.

[60] J. Song, S. Tao, Q. Fang, T. Liow, M. Yu, G. Lo, and D. Kwong, "Thermo-optical enhanced silicon wire interleavers," *Photonics Technology Letters, IEEE*, vol. 20, no. 24, pp. 2165–2167, 2008.

[61] M. Li, W. Pernice, C. Xiong, T. Baehr-Jones, M. Hochberg, and H. Tang, "Harnessing optical forces in integrated photonic circuits," *Nature*, vol. 456, no. 7221, pp. 480–484, 2008.

[62] A. Politi, J. C. Matthews, M. G. Thompson, and J. L. O'Brien, "Integrated quantum photonics," *Selected Topics in Quantum Electronics, IEEE Journal of*, vol. 15, no. 6, pp. 1673–1684, 2009.

[63] L.-W. Luo, S. Ibrahim, A. Nitkowski, Z. Ding, C. B. Poitras, S. Ben Yoo, and M. Lipson, "High bandwidth on-chip silicon photonic interleaver," *Optics express*, vol. 18, no. 22, pp. 23 079–23 087, 2010.

[64] B. Guha, B. B. Kyotoku, and M. Lipson, "Cmos-compatible athermal silicon microring resonators," *Optics Express*, vol. 18, no. 4, pp. 3487–3493, 2010.

[65] P. Sun and R. M. Reano, "Submilliwatt thermo-optic switches using free-standing silicon-on-insulator strip waveguides," *Optics express*, vol. 18, no. 8, pp. 8406–8411, 2010.

[66] Y. Ding, M. Pu, L. Liu, J. Xu, C. Peucheret, X. Zhang, D. Huang, and H. Ou, "Bandwidth and wavelength-tunable optical bandpass filter based on silicon microring-mzi structure," *Optics express*, vol. 19, no. 7, pp. 6462–6470, 2011.

[67] K. Suzuki, H. C. Nguyen, T. Tamanuki, F. Shinobu, Y. Saito, Y. Sakai, and T. Baba, "Slow-light-based variable symbol-rate silicon photonics dqpsk receiver," *Optics Express*, vol. 20, no. 4, pp. 4796–4804, 2012.

[68] W. Green, R. Lee, G. DeRose, A. Scherer, and A. Yariv, "Hybrid ingaasp-inp mach-zehnder racetrack resonator for thermooptic switching and coupling control," *Optics Express*, vol. 13, no. 5, pp. 1651–1659, 2005.

[69] R. A. Mayer, K. Jung, W. Lee, D.-L. Kwong, and J. C. Campbell, "Thin-film thermo-optic gexsi 1- x mach–zehnder interferometer," *Optics Letters*, vol. 17, no. 24, pp. 1812–1814, 1992.

[70] M.-C. Oh, H.-J. Lee, M.-H. Lee, J.-H. Ahn, and S. G. Han, "Asymmetric x-junction thermooptic switches based on fluorinated polymer waveguides," *Photonics Technology Letters, IEEE*, vol. 10, no. 6, pp. 813–815, 1998.

[71] A. Lentine, W. Zortman, D. Trotter, and M. Watts, "Active wavelength control of silicon microphotonic resonant modulators," in *Optical Interconnects Conference, 2012 IEEE*, May 2012, pp. 46–47.

[72] X. Zhu, M. Wang, K. Bergman, H. Lira, L.-W. Luo, and M. Lipson, "Fpga controlled microring based tunable add-drop filter," in *Optical Interconnects Conference, 2013 IEEE*, May 2013, pp. 102–103.

[73] H. Byun, I.-s. Joe, S. Kim, K. Lee, S. Hong, H. Ji, J. Pyo, K. Cho, S.-g. Kim, S. Suh *et al.*, "Fpga-based ddr3 dram interface using bulk-si optical interconnects," in *Group IV Photonics (GFP), 2013 IEEE 10th International Conference on*.   IEEE, 2013, pp. 5–6.

[74] S. Le Beux, Z. Li, C. Monat, X. Letartre, and I. O'Connor, "Reconfigurable photonic switching: Towards all-optical fpgas," in *Very Large Scale Integration (VLSI-SoC), 2013 IFIP/IEEE 21st International Conference on*.   IEEE, 2013, pp. 180–185.

[75] D. J. Richardson, "Silicon photonics: Beating the electronics bottleneck," *Nature Photonics*, vol. 3, no. 10, pp. 562–564, 2009.

[76] G. Hendry, E. Robinson, V. Gleyzer, J. Chan, L. P. Carloni, N. Bliss, and K. Bergman, "Time-division-multiplexed arbitration in silicon nanophotonic networks-on-chip for high-performance chip multiprocessors," *Journal of Parallel and Distributed Computing*, vol. 71, no. 5, pp. 641 – 650, 2011, networks-on-Chip. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0743731510001966

[77] D. Fey, M. Schneider, J. Jahns, and H. Knuppertz, "Optical multiplexing techniques for photonic clos networks in high performance computing architectures," *The Journal of Supercomputing*, vol. 62, no. 2, pp. 620–632, 2012.

[78] S. Yoo, "Integrated photonic-electronic technologies for next generation data centers and the future internet," in *Photonics in Switching*, 2012.

[79] Y. Hu, L. Zhang, X. Xiao, Z. Li, Y. Li, T. Chu, Y. Su, Y. Yu, and J. Yu, "An ultra-high-speed photonic temporal differentiator using cascaded soi microring resonators," *Journal of Optics*, vol. 14, no. 6, p. 065501, 2012.

[80] C. G. Roeloffzen, L. Zhuang, C. Taddei, A. Leinse, R. G. Heideman, P. W. van Dijk, R. M. Oldenbeuving, D. A. Marpaung, M. Burla, and K.-J. Boller, "Silicon nitride microwave photonic circuits," *Optics Express*, vol. 21, no. 19, pp. 22 937–22 961, 2013.

[81] C. Sun, M. Georgas, J. Orcutt, B. Moss, Y.-H. Chen, J. Shainline, M. Wade, K. Mehta, K. Nammari, E. Timurdogan *et al.*, "A monolithically-integrated chip-to-chip optical link in bulk cmos," *Solid-State Circuits, IEEE Journal of*, vol. 50, no. 4, pp. 828–844, 2015.

[82] A. Nicolas, L. Veissier, L. Giner, E. Giacobino, D. Maxein, and J. Laurat, "A quantum memory for orbital angular momentum photonic qubits," *Nature Photonics*, vol. 8, no. 3, pp. 234–238, 2014.

[83] E. G. Rieffel and W. H. Polak, *Quantum computing: A gentle introduction.*   MIT Press, 2011.

[84] L. K. Grover, "A fast quantum mechanical algorithm for database search," in *Proceedings of the twenty-eighth annual ACM symposium on Theory of computing.*   ACM, 1996, pp. 212–219.

[85] P. W. Shor, "Polynomial-time algorithms for prime factorization and discrete logarithms on a quantum computer," *SIAM journal on computing*, vol. 26, no. 5, pp. 1484–1509, 1997.

[86] L. M. Vandersypen, M. Steffen, G. Breyta, C. S. Yannoni, M. H. Sherwood, and I. L. Chuang, "Experimental realization of shor's quantum factoring algorithm using nuclear magnetic resonance," *Nature*, vol. 414, no. 6866, pp. 883–887, 2001.

[87] E. Knill, R. Laflamme, and G. J. Milburn, "A scheme for efficient quantum computation with linear optics," *Nature*, vol. 409, no. 6816, pp. 46–52, 2001.

[88] M. A. Nielsen, "Optical quantum computation using cluster states," *Phys. Rev. Lett.*, vol. 93, p. 040503, Jul 2004. [Online]. Available: http://link.aps.org/doi/10.1103/ PhysRevLett.93.040503

[89] A. Laing, A. Peruzzo, A. Politi, M. R. Verde, M. Halder, T. C. Ralph, M. G. Thompson, and J. L. O'Brien, "High-fidelity operation of quantum photonic circuits," *Applied Physics Letters*, vol. 97, no. 21, p. 211109, 2010.

[90] V. R. Almeida, C. A. Barrios, R. R. Panepucci, and M. Lipson, "All-optical control of light on a silicon chip," *Nature*, vol. 431, no. 7012, pp. 1081–1084, 2004.

[91] K.-i. Harada, H. Takesue, H. Fukuda, T. Tsuchizawa, T. Watanabe, K. Yamada, Y. Tokura, and S.-i. Itabashi, "Generation of high-purity entangled photon pairs using silicon wire waveguide," *Optics express*, vol. 16, no. 25, pp. 20 368–20 373, 2008.

[92] T. Meany, L. A. Ngah, M. J. Collins, A. S. Clark, R. J. Williams, B. J. Eggleton, M. Steel, M. J. Withford, O. Alibart, and S. Tanzilli, "Hybrid photonic circuit for multiplexed heralded single photons," *Laser & Photonics Reviews*, vol. 8, no. 3, pp. L42–L46, 2014.

[93] G. Milburn, "Quantum optical fredkin gate," *Physical Review Letters*, vol. 62, no. 18, p. 2124, 1989.

[94] P. Kok, W. J. Munro, K. Nemoto, T. C. Ralph, J. P. Dowling, and G. Milburn, "Linear optical quantum computing with photonic qubits," *Reviews of Modern Physics*, vol. 79, no. 1, p. 135, 2007.

[95] X.-C. Yao, T.-X. Wang, P. Xu, H. Lu, G.-S. Pan, X.-H. Bao, C.-Z. Peng, C.-Y. Lu, Y.-A. Chen, and J.-W. Pan, "Observation of eight-photon entanglement," *Nat Photon*, vol. 6, no. 4, pp. 225–228, 04 2012. [Online]. Available: http://dx.doi.org/10.1038/nphoton.2011.354

[96] Y. Yamamoto and K. Semba, *Principles and Methods of Quantum Information Technologies.* Springer, 2016.

[97] M. J. Collins, C. Xiong, I. H. Rey, T. D. Vo, J. He, S. Shahnia, C. Reardon, T. Krauss, M. Steel, A. S. Clark *et al.*, "Integrated spatial multiplexing of heralded single-photon sources," *Nature communications*, vol. 4, 2013.

[98] T. Honjo, K. Inoue, and H. Takahashi, "Differential-phase-shift quantum key distribution experiment with a planar light-wave circuit mach-zehnder interferometer," *Optics letters*, vol. 29, no. 23, pp. 2797–2799, 2004.

[99] X.-s. Ma, S. Zotter, J. Kofler, T. Jennewein, and A. Zeilinger, "Experimental generation of single photons via active multiplexing," *Physical Review A*, vol. 83, no. 4, p. 043814, 2011.

[100] E. Jeffrey, N. A. Peters, and P. G. Kwiat, "Towards a periodic deterministic source of arbitrary single-photon states," *New Journal of Physics*, vol. 6, no. 1, p. 100, 2004.

[101] J. H. Shapiro and F. N. Wong, "On-demand single-photon generation using a modular array of parametric downconverters with electro-optic polarization controls," *Optics letters*, vol. 32, no. 18, pp. 2698–2700, 2007.

[102] K. T. McCusker and P. G. Kwiat, "Efficient optical quantum state engineering," *Physical review letters*, vol. 103, no. 16, p. 163602, 2009.

[103] M. A. Broome, M. P. Almeida, A. Fedrizzi, and A. G. White, "Reducing multi-photon rates in pulsed down-conversion by temporal multiplexing," *Optics express*, vol. 19, no. 23, pp. 22 698–22 708, 2011.

[104] G. Li, T. Mason, and P. Yu, "Analysis of segmented traveling-wave optical modulators," *Journal of lightwave technology*, vol. 22, no. 7, p. 1789, 2004.

[105] E. Temporiti, G. Minoia, M. Repossi, D. Baldi, A. Ghilioni, and F. Svelto, "23.4 a 56gb/s 300mw silicon-photonics transmitter in 3d-integrated pic25g and 55nm bicmos technologies," in *Solid-State Circuits Conference (ISSCC), 2016 IEEE International.* IEEE, 2016, pp. 404–405.

[106] I. G. Lỳpez, P. Rito, L. Zimmermann, D. Kissinger, and A. Ulusoy, "A 40 gbaud sige: C bicmos driver for inp segmented mzms with integrated dac functionality for pam-16 generation," in *Microwave Symposium (IMS), 2016 IEEE MTT-S International.* IEEE, 2016, pp. 1–4.

[107] T. N. Huynh, N. Dupuis, R. Rimolo-Donadio, J. E. Proesel, D. M. Gill, C. W. Baks, A. V. Rylyakov, C. L. Schow, W. M. Green, and B. G. Lee, "Flexible transmitter employing silicon segmented mach-zehnder modulator with 32nm cmos distributed driver," *Journal of Lightwave Technology*, vol. 34, no. 22, p. 5129, 2016.

[108] P. Rito, I. G. Lỳpez, D. Petousi, L. Zimmermann, M. Kroh, S. Lischke, D. Knoll, D. Kissinger, and A. Ulusoy, "A monolithically integrated segmented driver and modulator in 0.25 ỳm sige: C bicmos with 13 db extinction ratio at 28 gb/s," in *Microwave Symposium (IMS), 2016 IEEE MTT-S International.* IEEE, 2016, pp. 1–4.

[109] S. Assefa, S. Shank, W. Green, M. Khater, E. Kiewra, C. Reinholm, S. Kamlapurkar, A. Rylyakov, C. Schow, F. Horst *et al.*, "A 90nm cmos integrated nano-photonics technology for 25gbps wdm optical communications applications," in *Electron Devices Meeting (IEDM), 2012 IEEE International.* IEEE, 2012, pp. 33–8.

[110] I. Marcikic, H. De Riedmatten, W. Tittel, H. Zbinden, and N. Gisin, "Long-distance teleportation of qubits at telecommunication wavelengths," *Nature*, vol. 421, no. 6922, pp. 509–513, 2003.

[111] I. Afek, O. Ambar, and Y. Silberberg, "High-noon states by mixing quantum and classical light," *Science*, vol. 328, no. 5980, pp. 879–881, 2010.

[112] D. Gottesman and I. L. Chuang, "Demonstrating the viability of universal quantum computation using teleportation and single-qubit operations," *Nature*, vol. 402, no. 6760, pp. 390–393, 1999.

[113] N. Matsuda, H. L. Jeannic, H. Fukuda, T. Tsuchizawa, W. J. Munro, K. Shimizu, K. Yamada, Y. Tokura, and H. Takesue, "A monolithically integrated polarization entangled photon pair source on a silicon chip," *arXiv preprint arXiv:1211.2885*, 2012.

[114] L. Olislager, J. Safioui, S. Clemmen, K. P. Huy, W. Bogaerts, R. Baets, P. Emplit, and S. Massar, "Silicon-on-insulator integrated source of polarization-entangled photons," *Optics letters*, vol. 38, no. 11, pp. 1960–1962, 2013.

[115] J. W. Silverstone, R. Santagati, D. Bonneau, M. J. Strain, M. Sorel, J. L. O'Brien, and M. G. Thompson, "Qubit entanglement between ring-resonator photon-pair sources on a silicon chip," *Nature communications*, vol. 6, 2015.

[116] B. J. Metcalf, J. B. Spring, P. C. Humphreys, N. Thomas-Peter, M. Barbieri, W. S. Kolthammer, X.-M. Jin, N. K. Langford, D. Kundys, J. C. Gates *et al.*, "Quantum teleportation on a photonic chip," *Nature Photonics*, vol. 8, no. 10, pp. 770–774, 2014.

[117] H. De Riedmatten, I. Marcikic, H. Zbinden, and N. Gisin, "Creating high dimensional time-bin entanglement using mode-locked lasers," *arXiv preprint quant-ph/0204165*, 2002.

[118] R. Wakabayashi, M. Fujiwara, K.-i. Yoshino, Y. Nambu, M. Sasaki, and T. Aoki, "Time-bin entangled photon pair generation from si micro-ring resonator," *Optics express*, vol. 23, no. 2, pp. 1103–1113, 2015.

[119] L. Zhuang, D. Marpaung, M. Burla, W. Beeker, A. Leinse, and C. Roeloffzen, "Low-loss, high-index-contrast si 3 n 4/sio 2 optical waveguides for optical delay lines in microwave photonics signal processing," *Optics Express*, vol. 19, no. 23, pp. 23 162–23 170, 2011.

[120] K. Wörhoff, R. G. Heideman, A. Leinse, and M. Hoekman, "Triplex: a versatile dielectric photonic platform," *Advanced Optical Technologies*, vol. 4, no. 2, pp. 189–207, 2015.

[121] P. G. Kwiat, A. M. Steinberg, and R. Y. Chiao, "High-visibility interference in a bell-inequality experiment for energy and time," *Physical Review A*, vol. 47, no. 4, p. R2472, 1993.

[122] J. Zhang, R. Thew, J.-D. Gautier, N. Gisin, and H. Zbinden, "Comprehensive characterization of ingaas–inp avalanche photodiodes at 1550 nm with an active quenching asic," *IEEE Journal of Quantum Electronics*, vol. 45, no. 7, pp. 792–799, 2009.

[123] Z. Zhang, B. Huang, X. Zhang, Z. Zhang, C. Cheng, X. Mao, S. Liu, and D. Chen, "Monolithic integration of si3n4 microring filters with bulk cmos ic through post-backend process," *Photonics Technology Letters, IEEE*, vol. PP, no. 99, pp. 1–1, 2015.

[124] S. Ramelow, A. Farsi, S. Clemmen, K. Luke, M. Lipson, and A. L. Gaeta, "Monolithic source of tunable narrowband photons for future quantum networks," in *Lasers and Electro-Optics (CLEO), 2015 Conference on*.   IEEE, 2015, pp. 1–2.

[125] J. P. Epping, M. Hoekman, R. Mateman, A. Leinse, R. G. Heideman, A. van Rees, P. J. van der Slot, C. J. Lee, and K.-J. Boller, "High confinement, high yield si 3 n 4 waveguides for nonlinear optical applications," *Optics express*, vol. 23, no. 2, pp. 642–648, 2015.

[126] N. Hosseini, R. Dekker, M. Hoekman, M. Dekkers, J. Bos, A. Leinse, and R. Heideman, "Stress-optic modulator in triplex platform using a piezoelectric lead zirconate titanate (pzt) thin film," *Optics express*, vol. 23, no. 11, pp. 14 018–14 026, 2015.

[127] Y. Varshni, "Temperature dependence of the energy gap in semiconductors," *Physica*, vol. 34, no. 1, pp. 149–154, 1967.

[128] K. Padmaraju, J. Chan, L. Chen, M. Lipson, and K. Bergman, "Thermal stabilization of a microring modulator using feedback control," *Optics Express*, vol. 20, no. 27, pp. 27 999–28 008, 2012.

[129] K. Padmaraju and K. Bergman, "Resolving the thermal challenges for silicon microring resonator devices," *Nanophotonics*, vol. 3, no. 4-5, pp. 269–281, 2014.

[130] J. A. Cox, A. L. Lentine, D. C. Trotter, and A. L. Starbuck, "Control of integrated micro-resonator wavelength via balanced homodyne locking," *Optics Express*, vol. 22, no. 9, pp. 11 279–11 289, 2014.

[131] J. L. O'Brien, "Optical quantum computing," *Science*, vol. 318, no. 5856, pp. 1567–1570, 2007.

[132] A. Aspuru-Guzik and P. Walther, "Photonic quantum simulators," *Nature Physics*, vol. 8, no. 4, pp. 285–291, 2012.

[133] D. E. Browne and T. Rudolph, "Resource-efficient linear optical quantum computation," *Physical Review Letters*, vol. 95, no. 1, p. 010501, 2005.

[134] M. Varnava, D. E. Browne, and T. Rudolph, "How good must single photon sources and detectors be for efficient linear optical quantum computation?" *Physical Review Letters*, vol. 100, no. 6, p. 060502, 2008.

[135] T. Jennewein, M. Barbieri, and A. G. White, "Single-photon device requirements for operating linear optics quantum computing outside the post-selection basis," *Journal of Modern Optics*, vol. 58, no. 3-4, pp. 276–287, 2011.

[136] M. Eisaman, J. Fan, A. Migdall, and S. Polyakov, "Invited review article: Single-photon sources and detectors," *Review of scientific instruments*, vol. 82, no. 7, p. 071101, 2011.

[137] P. Michler, A. Kiraz, C. Becher, W. Schoenfeld, P. Petroff, L. Zhang, E. Hu, and A. Imamoglu, "A quantum dot single-photon turnstile device," *Science*, vol. 290, no. 5500, pp. 2282–2285, 2000.

[138] A. J. Shields, "Semiconductor quantum light sources," *Nature photonics*, vol. 1, no. 4, pp. 215–223, 2007.

[139] S. V. Polyakov, A. Muller, E. B. Flagg, A. Ling, N. Borjemscaia, E. Van Keuren, A. Migdall, and G. S. Solomon, "Coalescence of single photons emitted by disparate single-photon sources: The example of inas quantum dots and parametric down-conversion sources," *Physical review letters*, vol. 107, no. 15, p. 157402, 2011.

[140] N. Mizuochi, T. Makino, H. Kato, D. Takeuchi, M. Ogura, H. Okushi, M. Nothaft, P. Neumann, A. Gali, F. Jelezko *et al.*, "Electrically driven single-photon source at room temperature in diamond," *Nature photonics*, vol. 6, no. 5, pp. 299–303, 2012.

[141] Y.-J. Wei, Y.-M. He, M.-C. Chen, Y.-N. Hu, Y. He, D. Wu, C. Schneider, M. Kamp, S. Höfling, C.-Y. Lu *et al.*, "Deterministic and robust generation of single photons on a chip with 99.5% indistinguishability using rapid adiabatic passage," *arXiv preprint arXiv:1405.1991*, 2014.

[142] K. Konthasinghe, M. Peiris, Y. Yu, M. Li, J. He, L. Wang, H. Ni, Z. Niu, C. Shih, and A. Muller, "Field-field and photon-photon correlations of light scattered by two remote two-level inas quantum dots on the same substrate," *Physical review letters*, vol. 109, no. 26, p. 267402, 2012.

[143] A. Sipahigil, K. D. Jahnke, L. J. Rogers, T. Teraji, J. Isoya, A. S. Zibrov, F. Jelezko, and M. D. Lukin, "Indistinguishable photons from separated silicon-vacancy centers in diamond," *Physical review letters*, vol. 113, no. 11, p. 113602, 2014.

[144] A. Politi, M. J. Cryan, J. G. Rarity, S. Yu, and J. L. O'Brien, "Silica-on-silicon waveguide quantum circuits," *Science*, vol. 320, no. 5876, pp. 646–649, 2008.

[145] J. B. Spring, B. J. Metcalf, P. C. Humphreys, W. S. Kolthammer, X.-M. Jin, M. Barbieri, A. Datta, N. Thomas-Peter, N. K. Langford, D. Kundys *et al.*, "Boson sampling on a photonic chip," *Science*, vol. 339, no. 6121, pp. 798–801, 2013.

[146] B. Bell, D. Herrera-Martí, M. Tame, D. Markham, W. Wadsworth, and J. Rarity, "Experimental demonstration of a graph state quantum error-correction code," *Nature communications*, vol. 5, 2014.

[147] X.-L. Wang, L.-K. Chen, W. Li, H.-L. Huang, C. Liu, C. Chen, Y.-H. Luo, Z.-E. Su, D. Wu, Z.-D. Li *et al.*, "Experimental ten-photon entanglement," *Physical review letters*, vol. 117, no. 21, p. 210502, 2016.

[148] A. Migdall, D. Branning, and S. Castelletto, "Tailoring single-photon and multiphoton probabilities of a single-photon on-demand source," *Physical Review A*, vol. 66, no. 5, p. 053805, 2002.

[149] T. Pittman, B. Jacobs, and J. Franson, "Single photons on pseudodemand from stored parametric down-conversion," *Physical Review A*, vol. 66, no. 4, p. 042303, 2002.

[150] D. Bonneau, G. J. Mendoza, J. L. O'Brien, and M. G. Thompson, "Effect of loss on multiplexed single-photon sources," *New Journal of Physics*, vol. 17, no. 4, p. 043057, 2015.

[151] G. J. Mendoza, R. Santagati, J. Munns, E. Hemsley, M. Piekarek, E. Martín-López, G. D. Marshall, D. Bonneau, M. G. Thompson, and J. L. O'Brien, "Active temporal and spatial multiplexing of photons," *Optica*, vol. 3, no. 2, pp. 127–132, 2016.

[152] F. Kaneda, B. G. Christensen, J. J. Wong, H. S. Park, K. T. McCusker, and P. G. Kwiat, "Time-multiplexed heralded single-photon source," *Optica*, vol. 2, no. 12, pp. 1010–1013, 2015.

[153] X. Zhang, I. Jizan, J. He, A. S. Clark, D.-Y. Choi, C. Chae, B. J. Eggleton, and C. Xiong, "Enhancing the heralded single-photon rate from a silicon nanowire by time and wavelength division multiplexing pump pulses," *Optics letters*, vol. 40, no. 11, pp. 2489–2492, 2015.

[154] H. Jiang, Y. Zou, Q. Chen, K. Li, R. Zhang, Y. Wang, H. Ming, and Z. Zheng, "Transparent electro-optic ceramics and devices," in *Photonics Asia 2004*. International Society for Optics and Photonics, 2005, pp. 380–394.

[155] H. Takesue and K. Shimizu, "Effects of multiple pairs on visibility measurements of entangled photons generated by spontaneous parametric processes," *Optics Communications*, vol. 283, no. 2, pp. 276–287, 2010.

[156] C. Hong, Z.-Y. Ou, and L. Mandel, "Measurement of subpicosecond time intervals between two photons by interference," *Physical Review Letters*, vol. 59, no. 18, p. 2044, 1987.

[157] P. B. Dixon, J. H. Shapiro, and F. N. Wong, "Spectral engineering by gaussian phase-matching for quantum photonics," *Optics express*, vol. 21, no. 5, pp. 5879–5890, 2013.

[158] K.-i. Harada, H. Takesue, H. Fukuda, T. Tsuchizawa, T. Watanabe, K. Yamada, Y. Tokura, and S.-i. Itabashi, "Indistinguishable photon pair generation using two independent silicon wire waveguides," *New Journal of Physics*, vol. 13, no. 6, p. 065005, 2011.

[159] A. McMillan, L. Labonté, A. Clark, B. Bell, O. Alibart, A. Martin, W. Wadsworth, S. Tanzilli, and J. Rarity, "Two-photon interference between disparate sources for quantum networking," *arXiv preprint arXiv:1306.5801*, 2013.

[160] F. Marsili, V. Verma, J. Stern, S. Harrington, A. Lita, T. Gerrits, I. Vayshenker, B. Baek, M. Shaw, R. Mirin *et al.*, "Detecting single infrared photons with 93% system efficiency," *Nature Photonics*, vol. 7, no. 3, pp. 210–214, 2013.

[161] L. Helt, Z. Yang, M. Liscidini, and J. Sipe, "Spontaneous four-wave mixing in microring resonators," *Optics letters*, vol. 35, no. 18, pp. 3006–3008, 2010.

[162] Q. Liu, X. Tu, K. W. Kim, J. S. Kee, Y. Shin, K. Han, Y.-J. Yoon, G.-Q. Lo, and M. K. Park, "Highly sensitive mach–zehnder interferometer biosensor based on silicon nitride slot waveguide," *Sensors and Actuators B: Chemical*, vol. 188, pp. 681–688, 2013.

[163] A. W. Poon, X. Luo, F. Xu, and H. Chen, "Cascaded microresonator-based matrix switch for silicon on-chip optical interconnection," *Proceedings of the IEEE*, vol. 97, no. 7, pp. 1216–1238, 2009.

[164] F. Morichetti, S. Grillanda, and A. Melloni, "Breakthroughs in photonics 2013: Toward feedback-controlled integrated photonics," *Photonics Journal, IEEE*, vol. 6, no. 2, pp. 1–6, 2014.

[165] K. Padmaraju, D. F. Logan, T. Shiraishi, J. J. Ackert, A. P. Knights, and K. Bergman, "Wavelength locking and thermally stabilizing microring resonators using dithering signals," *Lightwave Technology, Journal of*, vol. 32, no. 3, pp. 505–512, 2014.

[166] S. Grillanda, M. Carminati, F. Morichetti, P. Ciccarella, A. Annoni, G. Ferrari, M. Strain, M. Sorel, M. Sampietro, and A. Melloni, "Non-invasive monitoring and control in silicon photonics using cmos integrated electronics," *Optica*, vol. 1, no. 3, pp. 129–136, 2014.

[167] J. Fisher, A. Kodanev, and M. Nazarathy, "Multi-degree-of-freedom stabilization of large-scale photonic-integrated circuits," *Lightwave Technology, Journal of*, vol. 33, no. 10, pp. 2146–2166, May 2015.

[168] J. A. Juárez-Abad, J. Linares-Flores, E. Guzmán-Ramírez, and H. Sira-Ramirez, "Generalized proportional integral tracking controller for a single-phase multilevel cascade inverter: An fpga implementation," *IEEE Transactions on Industrial Informatics*, vol. 10, no. 1, pp. 256–266, 2014.

[169] K. J. Åström and B. Wittenmark, *Computer-controlled systems: theory and design*. Courier Corporation, 2013.

[170] (2012). [Online]. Available: http://au.mathworks.com/products/sysid/

[171] J. C. Doyle, B. A. Francis, and A. R. Tannenbaum, *Feedback control theory*. Courier Corporation, 2013.

[172] S. Skogestad and I. Postlethwaite, *Multivariable feedback control: analysis and design*. Wiley New York, 2007, vol. 2.

[173] (2016) Mimo transfer functions. [Online]. Available: https://au.mathworks.com/help/control/ug/mimo-transfer-function-models.html

[174] (2014). [Online]. Available: http://au.mathworks.com/videos/control-system-tuning-in-simulink-made-easy-81839.html

[175] J. Silverstone, D. Bonneau, J. O. Brien, and M. Thompson, "Silicon quantum photonics," *IEEE Journal of Selected Topics in Quantum Electronics*, 2016.

[176] A. Hayakawa, H. Ebe, Y. Chen, and T. Mori, "Silicon photonics optical transceiver for high-speed, high-density and low-power lsi interconnect," *FUJITSU SCIENTIFIC & TECHNICAL JOURNAL*, vol. 52, no. 1, pp. 19–26, 2016.

[177] F. Fresi, A. Malacarne, V. Sorianello, G. Meloni, P. Velha, M. Midrio, V. Toccafondo, S. Faralli, M. Romagnoli, and L. Potì, "Reconfigurable silicon photonics integrated 16-qam modulator driven by binary electronics," *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 22, no. 6, pp. 1–10, 2016.

[178] M. Streshinsky, R. Ding, Y. Liu, A. Novack, Y. Yang, Y. Ma, X. Tu, E. K. S. Chee, A. E.-J. Lim, P. G.-Q. Lo *et al.*, "Low power 50 gb/s silicon traveling wave mach-zehnder modulator near 1300 nm," *Optics express*, vol. 21, no. 25, pp. 30 350–30 357, 2013.

[179] S. Menezo, E. Temporiti, J. Lee, O. Dubray, M. Fournier, S. Bernabé, D. Baldi, B. Blampey, G. Minoia, M. Repossi *et al.*, "Transmitter made up of a silicon photonic ic and its flip-chipped cmos ic driver targeting implementation in fdma-pon," *Journal of Lightwave Technology*, vol. 34, no. 10, pp. 2391–2397, 2016.

[180] P. Dong, J. Lee, Y.-K. Chen, L. L. Buhl, S. Chandrasekhar, J. H. Sinsky, and K. Kim, "Four-channel 100-gb/s per channel discrete multitone modulation using silicon photonic integrated circuits," *Journal of Lightwave Technology*, vol. 34, no. 1, pp. 79–84, 2016.

[181] T. N. Huynh, A. Ramaswamy, R. Rimolo-Donadio, C. Schow, J. E. Roth, E. J. Norberg, J. Proesel, R. S. Guzzon, J. Shin, A. Rylyakov *et al.*, "Four-channel wdm transmitter with heterogeneously integrated iii-v/si photonics and low power 32 nm cmos drivers," *Journal of Lightwave Technology*, vol. 34, no. 13, pp. 3131–3137, 2016.

[182] Q. Cheng, A. Wonfor, R. V. Penty, and I. H. White, "Scalable, low-energy hybrid photonic space switch," *Journal of Lightwave Technology*, vol. 31, no. 18, pp. 3077–3084, 2013.

[183] V. Katopodis, P. Groumas, Z. Zhang, J.-Y. Dupuy, E. Miller, A. Beretta, L. Gounaridis, J. H. Choi, D. Pech, F. Jorge *et al.*, "-gb/s nrz-ook integrated transmitter for intradata center connectivity," *IEEE Photonics Technology Letters*, vol. 26, no. 20, pp. 2078–2081, 2014.

[184] C. Zhang, P. A. Morton, J. B. Khurgin, J. D. Peters, and J. E. Bowers, "Highly linear heterogeneous-integrated mach-zehnder interferometer modulators on si," *Optics Express*, vol. 24, no. 17, pp. 19 040–19 047, 2016.

[185] P. Groumas, V. Katopodis, J. H. Choi, H.-G. Bach, J.-Y. Dupuy, A. Konczykowska, Z. Zhang, P. Harati, E. Miller, A. Beretta *et al.*, "Multi-100 gbe and 400 gbe interfaces for intra-data center networks based on arrayed transceivers with serial 100 gb/s operation," *Journal of Lightwave Technology*, vol. 33, no. 4, pp. 943–954, 2015.

[186] V. Katopodis, P. Groumas, Z. Zhang, R. Dinu, E. Miller, A. Konczykowska, J.-Y. Dupuy, A. Beretta, A. Dede, J. Choi *et al.*, "Polymer enabled 100gbaud connectivity for datacom applications," *Optics Communications*, vol. 362, pp. 13–21, 2016.

[187] G. de Valicourt, G. Levaufre, Y. Pointurier, A. Le Liepvre, J.-C. Antona, C. Jany, A. Accard, F. Lelarge, D. Make, and G.-H. Duan, "Direct modulation of hybrid-integrated inp/si transmitters for short and long reach access network," *Journal of Lightwave Technology*, vol. 33, no. 8, pp. 1608–1616, 2015.

[188] G.-H. Duan, C. Jany, A. Le Liepvre, A. Accard, M. Lamponi, D. Make, P. Kaspar, G. Levaufre, N. Girard, F. Lelarge *et al.*, "Hybrid iii–v on silicon lasers for photonic integrated circuits on silicon," *IEEE Journal of selected topics in quantum electronics*, vol. 20, no. 4, pp. 158–170, 2014.

[189] M. Sadiq, M. Gleeson, N. Ye, J. O'Callaghan, P. Morrissey, H. Zhang, K. Thomas, A. Gocalinska, E. Pelucchi, F. Gunning *et al.*, "10 gb/s inp-based mach-zehnder modulator for operation at 2 μm wavelengths," *Optics express*, vol. 23, no. 9, pp. 10 905–10 913, 2015.

[190] Z. Qi, G. Hu, L. Li, B. Yun, R. Zhang, and Y. Cui, "Design and analysis of a compact soi-based aluminum/highly doped p-type silicon hybrid plasmonic modulator," *IEEE Photonics Journal*, vol. 8, no. 3, pp. 1–11, 2016.

[191] C. Haffner, W. Heni, Y. Fedoryshyn, A. Josten, B. Baeuerle, C. Hoessbacher, Y. Salamin, U. Koch, N. DJordjević, P. Mousel *et al.*, "Plasmonic organic hybrid modulators—scaling highest speed photonics to the microscale," *Proceedings of the IEEE*, 2016.

[192] H. Yamazaki, H. Takahashi, T. Goh, Y. Hashizume, T. Yamada, S. Mino, H. Kawakami, and Y. Miyamoto, "Optical modulator with a near-linear field response," *Journal of Lightwave Technology*, vol. 34, no. 16, pp. 3796–3802, 2016.

[193] G.-W. Lu, T. Sakamoto, and T. Kawanishi, "Flexible high-order qam transmitters for elastic optical networks," *Photonic Network Communications*, vol. 31, no. 2, pp. 345–352, 2016.

[194] R. Palmer, L. Alloatti, D. Korn, P. Schindler, R. Schmogrow, W. Heni, S. Koenig, J. Bolten, T. Wahlbrink, M. Waldow *et al.*, "Silicon-organic hybrid mzi modulator generating ook, bpsk and 8-ask signals for up to 84 gbit/s," *IEEE Photonics Journal*, vol. 5, no. 2, pp. 6 600 907–6 600 907, 2013.

[195] T. Ohyama, Y. Doi, W. Kobayashi, S. Kanazawa, T. Tanaka, K. Takahata, A. Kanda, T. Kurosaki, T. Ohno, H. Sanjoh *et al.*, "Compact hybrid-integrated 100-gb/s tosa using eadfb laser array and awg multiplexer," *IEEE Photonics Technology Letters*, vol. 28, no. 7, pp. 802–805, 2016.

[196] G. Denoyer, C. Cole, A. Santipo, R. Russo, C. Robinson, L. Li, Y. Zhou, B. Park, F. Boeuf, S. Crémer *et al.*, "Hybrid silicon photonic circuits and transceiver for 50 gb/s nrz transmission over single-mode fiber," *Journal of Lightwave Technology*, vol. 33, no. 6, pp. 1247–1254, 2015.

[197] N. Feilchenfeld, F. Anderson, T. Barwicz, S. Chilstedt, Y. Ding, J. Ellis-Monaghan, D. Gill, C. Hedges, J. Hofrichter, F. Horst *et al.*, "An integrated silicon photonics technology for o-band datacom," in *2015 IEEE International Electron Devices Meeting (IEDM)*.   IEEE, 2015, pp. 25–7.

[198] C. Xiong, D. M. Gill, J. E. Proesel, J. S. Orcutt, W. Haensch, and W. M. Green, "Monolithic 56 gb/s silicon photonic pulse-amplitude modulation transmitter," *Optica*, vol. 3, no. 10, pp. 1060–1065, 2016.

[199] D. M. Gill, C. Xiong, J. E. Proesel, J. C. Rosenberg, J. Orcutt, M. Khater, J. Ellis-Monaghan, A. Stricker, E. Kiewra, Y. Martin *et al.*, "Demonstration of error-free 32-gb/s operation from monolithic cmos nanophotonic transmitters," *IEEE Photonics Technology Letters*, vol. 28, no. 13, pp. 1410–1413, 2016.

[200] P. Dong, X. Liu, S. Chandrasekhar, L. L. Buhl, R. Aroca, and Y.-K. Chen, "Monolithic silicon photonic integrated circuits for compact 100 gb/s coherent optical receivers and transmitters," *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 20, no. 4, pp. 150–157, 2014.

[201] P. Dong, Y.-K. Chen, T. Gu, L. L. Buhl, D. T. Neilson, and J. H. Sinsky, "Reconfigurable 100 gb/s silicon photonic network-on-chip [invited]," *Journal of Optical Communications and Networking*, vol. 7, no. 1, pp. A37–A43, 2015.

[202] P. Schindler, D. Korn, C. Stamatiadis, M. O'Keefe, L. Stampoulidis, R. Schmogrow, P. Zakynthinos, R. Palmer, N. Cameron, Y. Zhou *et al.*, "Monolithic gaas electro-optic iq modulator demonstrated at 150 gbit/s with 64qam," *Journal of Lightwave Technology*, vol. 32, no. 4, pp. 760–765, 2014.

[203] D. Knoll, S. Lischke, L. Zimmermann, B. Heinemann, D. Micusik, P. Ostrovskyy, G. Winzer, M. Kroh, R. Barth, T. Grabolla *et al.*, "Monolithically integrated 25gbit/sec receiver for 1.55 μm in photonic bicmos technology," in *Optical Fiber Communication Conference*.   Optical Society of America, 2014, pp. Th4C–4.

[204] D. Petousi, L. Zimmermann, P. Rito, M. Kroh, D. Knoll, S. Lischke, C. Mai, I. G. Lopez, A. C. Ulusoy, G. Winzer *et al.*, "Monolithic photonic bicmos sub-system comprising mzm and segmented driver with 13 db er at 28 gb/s," in *CLEO: Science and Innovations*.   Optical Society of America, 2016, pp. STu4G–3.

[205] E. Fu, P. Wu, Z. R. Huang, and V. J. Koomson, "Monolithic low-power 6-gb/s optical transmitter for a silicon hbt-based carrier injection electroabsorption modulator," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 63, no. 6, pp. 598–602, 2016.

[206] B. G. Lee, A. V. Rylyakov, W. M. Green, S. Assefa, C. W. Baks, R. Rimolo-Donadio, D. M. Kuchta, M. H. Khater, T. Barwicz, C. Reinholm *et al.*, "Monolithic silicon integration of scaled photonic switch fabrics, cmos logic, and device driver circuits," *Journal of Lightwave Technology*, vol. 32, no. 4, pp. 743–751, 2014.

[207] M. Kroh, M. O'Keefe, K. Voigt, S. Fedderwitz, G. B. Preve, S. Lischke, T. Brast, D. Petousi, C. Stamatiadis, E. Kehayas *et al.*, "Photonic-electronic platform for next generation optical transport network," in *2013 15th International Conference on Transparent Optical Networks (ICTON)*. IEEE, 2013, pp. 1–5.

[208] E. Temporiti, A. Ghilioni, G. Minoia, P. Orlandi, M. Repossi, D. Baldi, and F. Svelto, "Insights into silicon photonics mach-zehnder-based optical transmitter architectures," *IEEE Journal of Solid-State Circuits*, 2016.

[209] T. Fujisawa, S. Kanazawa, Y. Ueda, W. Kobayashi, K. Takahata, A. Ohki, T. Ito, M. Kohtoku, and H. Ishii, "Low-loss cascaded mach–zehnder multiplexer integrated 25-gbit/s x 4-lane eadfb laser array for future cfp4 100 gbe transmitter," *IEEE Journal of Quantum Electronics*, vol. 12, no. 49, pp. 1001–1007, 2013.

[210] D. Feng, W. Qian, H. Liang, C.-C. Kung, Z. Zhou, Z. Li, J. S. Levy, R. Shafiiha, J. Fong, B. J. Luff *et al.*, "High-speed gesi electroabsorption modulator on the soi waveguide platform," *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 19, no. 6, pp. 64–73, 2013.

[211] D. M. Gill, J. E. Proesel, C. Xiong, J. Rosenberg, M. Khater, T. Barwicz, S. Assefa, S. M. Shank, C. Reinholm, E. Kiewra *et al.*, "Monolithic travelling-wave mach-zehnder transmitter with high-swing stacked cmos driver," in *CLEO: Science and Innovations*. Optical Society of America, 2014, pp. SM2G–3.

Appendix A

# Detail Si$_3$N$_4$ photonic integrated circuits and electrical connection
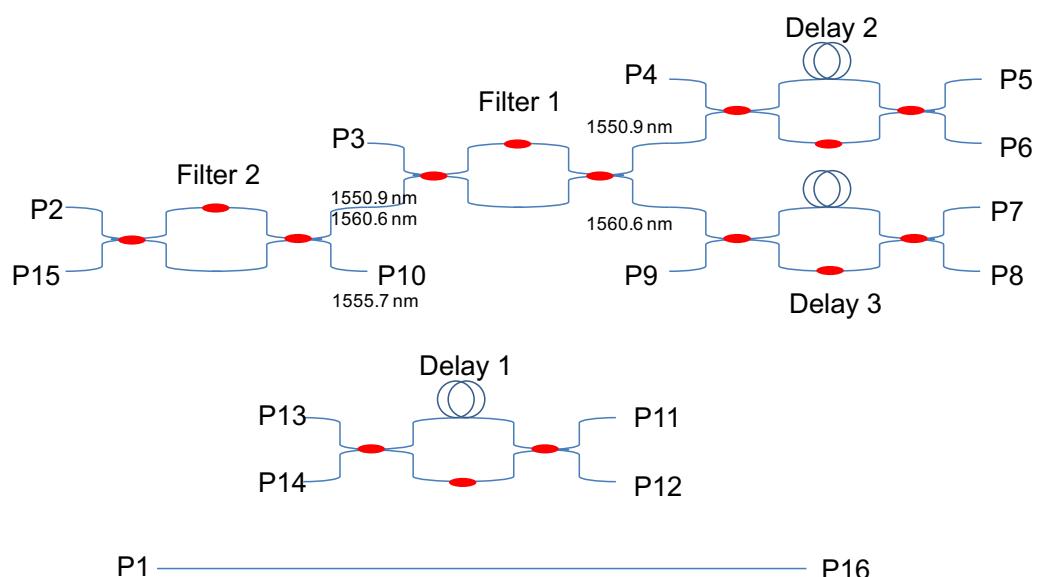
Fig. A.1 Si$_3$N$_4$ chip layout
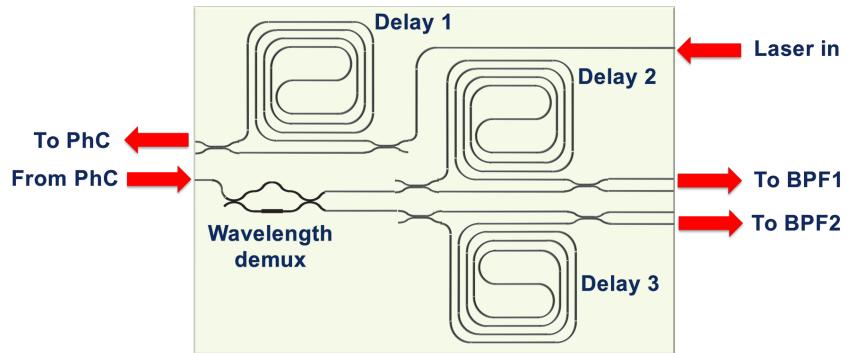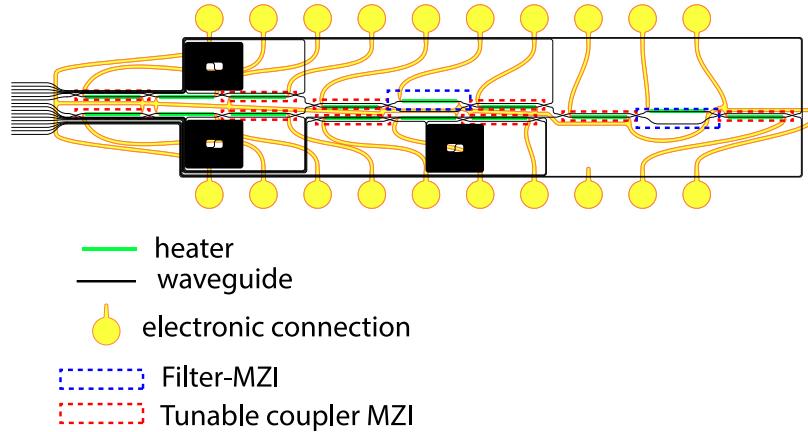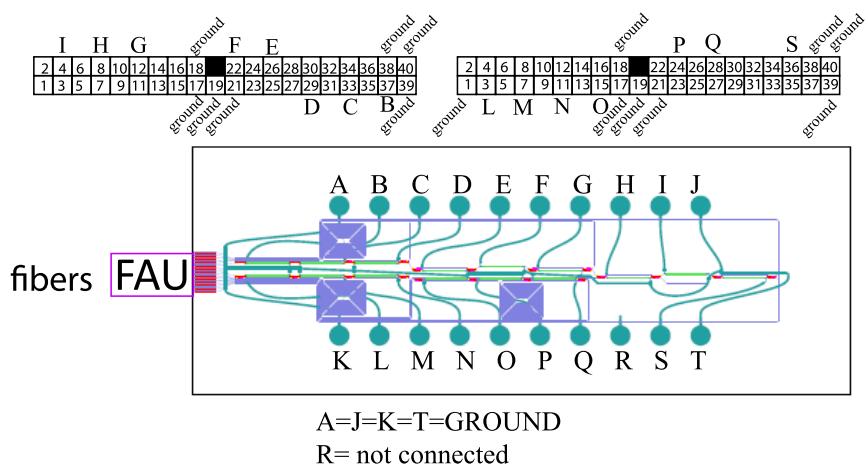
Fig. A.2 Chip delay layout on Si$_3$N$_4$

Fig. A.3 Si$_3$N$_4$ chip interface to electronic schematic

A=J=K=T=GROUND
R= not connected

Fig. A.4 Electrical and optical arrangement
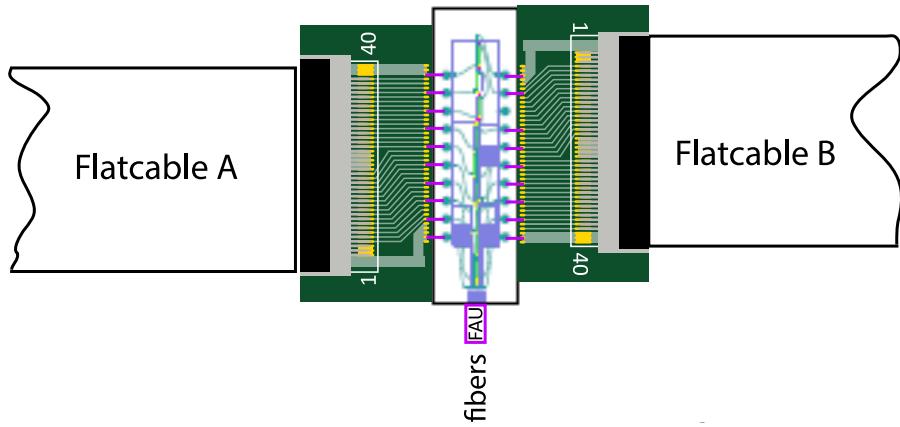
Fig. A.5 Flatcable arrangement on Si_3N_4 chip
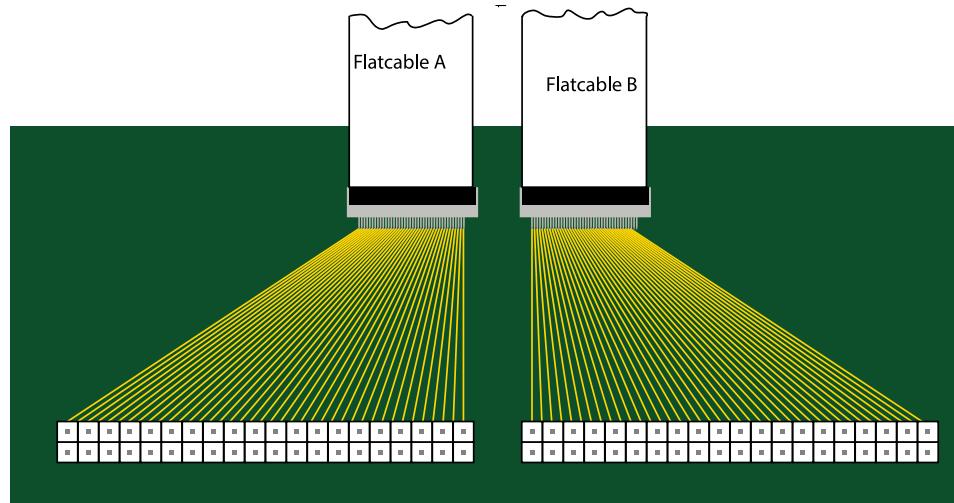
Fig. A.6 Flatcable arrangement on Si_3N_4 chip to ribbon cable