

Computer Engineering Lab

Thesis Projects 2022

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<http://phwl.org/talks>



THE UNIVERSITY OF
SYDNEY

CruxML
REAL-TIME COMPUTING & MACHINE LEARNING





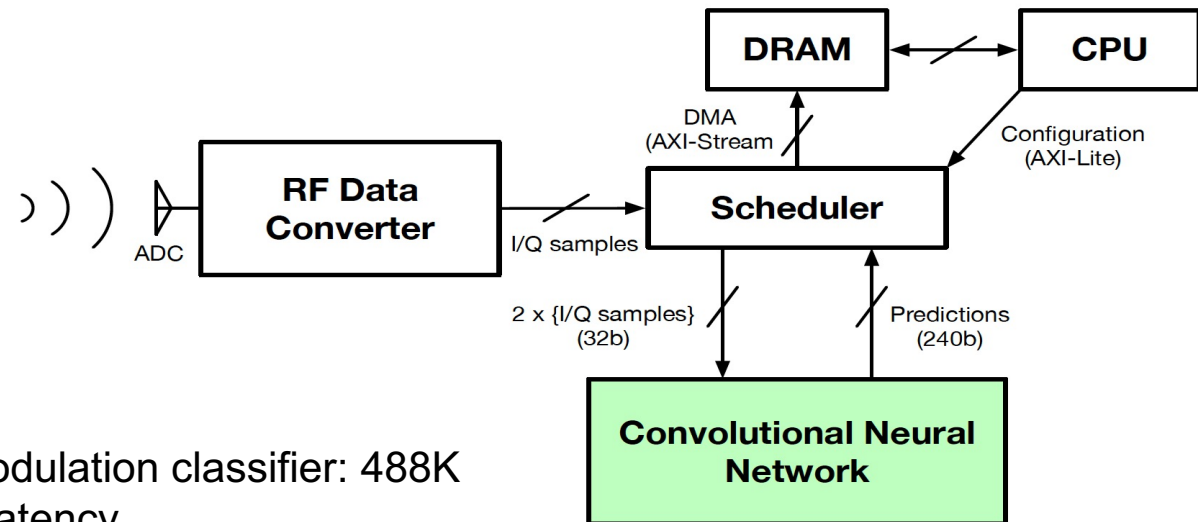
Computer Engineering Laboratory

- › Focuses on how to use parallelism to solve demanding problems
 - Novel architectures, applications and design techniques using FPGAs
- › Research: reconfigurable computing, radio frequency machine learning



Theme: Understanding Radio Signals

- › Understanding of radio signals in low SNR difficult problem
- › Radio data is high speed and low latency often required (ML will never be fast enough)
- › FPGAs offer possibility of integrating radio, signal processing and ML on the same chip



Automatic Modulation classifier: 488K
class/s, 8us latency

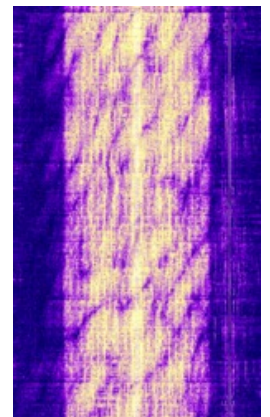
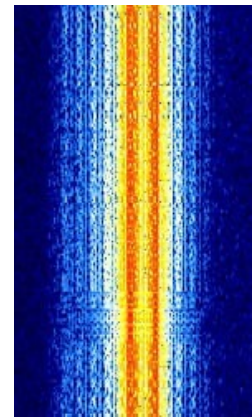
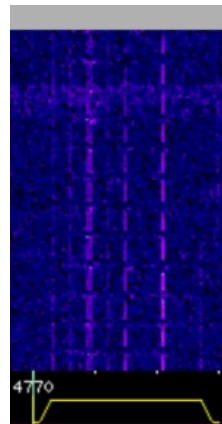
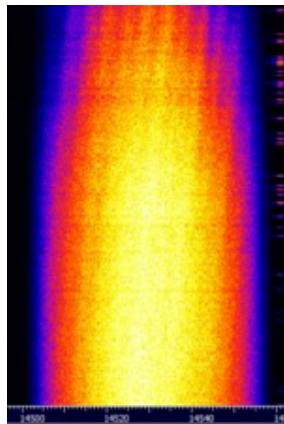
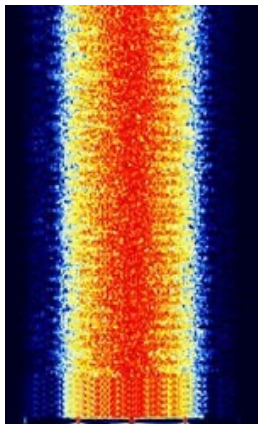
CEL1: Software Defined Radio

- › Problem: develop new SDR using front end of open source ADALM-Pluto which uses the new Kria module
<https://www.xilinx.com/products/som/kria.html>
 - Based on ADALM-Pluto <https://wiki.analog.com/university/tools/pluto>
 - Advantages: can do on-FPGA processing, has USB 3.0 and GbE
- › Task: hardware design of radio, PCB and FPGA interface



CEL2: Offline HF Radio Signal Classification

- › Problem: scan high frequency (HF) bands (3-30MHz), identify strongest signals and classify them
 - https://www.sigidwiki.com/wiki/Signal_Identification_Guide
 - Use few shot learning <https://neptune.ai/blog/understanding-few-shot-learning-in-computer-vision> for classification
- › Task: develop novel machine learning and signal processing techniques to solve this problem

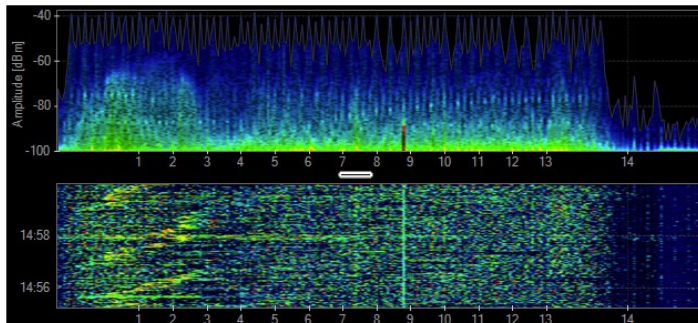


CEL3: Real-time 2.4GHz Radio Signal Classification

- › Problem: identify different 2.4GHz Bluetooth, Zigbee, wifi signals and extract information about them in real-time
 - Starting point https://github.com/Xilinx/Vitis-AI-Tutorials/blob/master/Design_Tutorials/10-RF_modulation_recognition/files/vai_2018_RadioML_VAI_keras.ipynb
- › Task: develop convolutional neural network on FPGA using Vitis

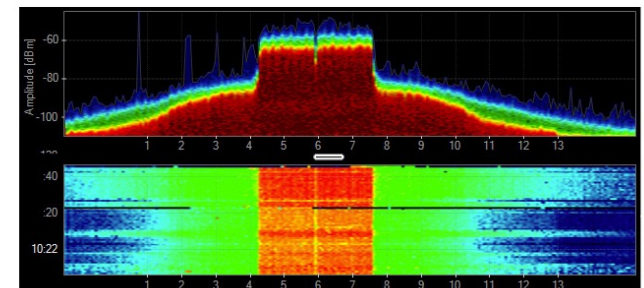
Bluetooth

Bluetooth devices are active in the 2.4 GHz band. These devices are frequency hoppers that impact all channels, so you can't move your WiFi to avoid their transmissions. However, Bluetooth devices are relatively low-powered and hop very quickly, and will have limited impact on WiFi devices. It isn't until many Bluetooth devices are active simultaneously that you are likely to see problems with your WiFi.

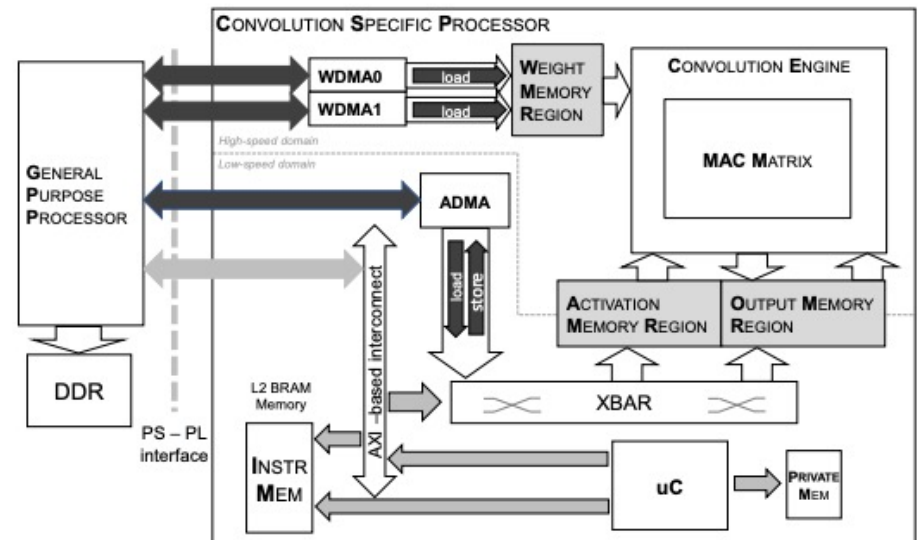


802.11g - ERP-OFDM

- PHY: 2.4 GHz
- Data Rates: 6-54Mbps
- Channel Width: 20 MHz

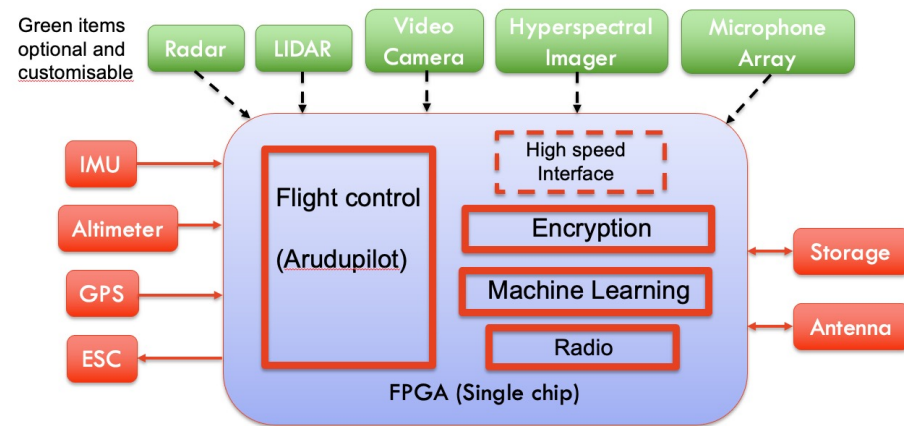


- › Problem: develop accelerator for training based on http://phwl.org/assets/papers/bm_iclr21.pdf
 - Starting point is RISCv+custom convolution accelerator design <https://arxiv.org/pdf/2005.03775.pdf>
- › Task: add ability to train based on NEURAghe (Verilog+RISCv)



CEL5: Mission Optimised Drones

- › Problem: Develop a drone on-demand capability, taking mission parameters as inputs and producing optimized drone with associated sensors, communications and AI
- › Task: develop FPGA-based flight control based on Ardupilot which can be customized for different applications (embedded software and control)

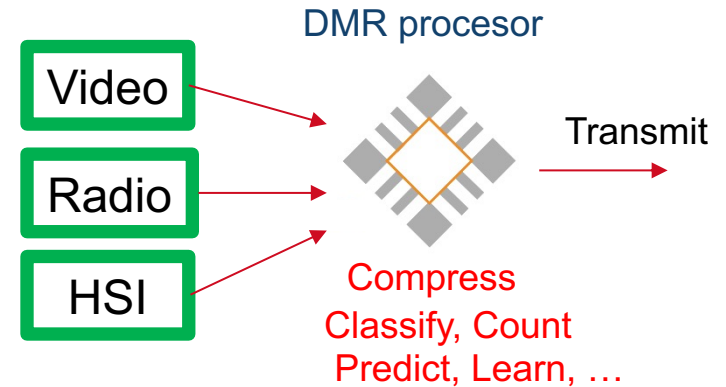


with A/Prof Dries Verstraete (AMME)

CEL6: Data Modelling and Reduction (DMR)

Computer Engineering Lab (philip.leong@sydney.edu.au)

- › Problem: CubeSat experiments limited by power and data volume. DMR is a common goal but algorithms are problem-specific
- › Solution: reconfigurable low-power, FPGA-based module
 - › Parallel real-time sensors and instruments
 - › Lossless & lossy compression, DNN inference and on-chip training
- › Task: implement IP for this using Vitis HLS
 - Jian Yan et. al. Lossless compression decoders for bitstreams and software binaries based on high-level synthesis. *IEEE TVLSI*, 2017



with Prof Iver Cairns (Physics) and