A Comprehensive Graphene FET Model for Circuit Design

Saul Rodriguez, *Member, IEEE,* Sam Vaziri, *Student Member, IEEE,* Anderson Smith, *Student Member, IEEE,*
Sébastien Frégonèse, Mikael Ostling, *Fellow, IEEE,* Max C. Lemme, *Senior Member, IEEE,*
and Ana Rusu, *Member, IEEE*

Abstract—During the last years, Graphene based Field Effect Transistors (GFET) have shown outstanding RF performance; therefore, they have attracted considerable attention from the electronic devices and circuits communities. At the same time, analytical models that predict the electrical characteristics of GFETs have evolved rapidly. These models, however, have a complexity level that can only be handled with the help of a circuit simulator. On the other hand, analog circuit designers require simple models that enable them to carry out fast hand-calculations, i.e., to create circuits using small-signal hybrid-π models, calculate figures of merit, estimate gains, pole-zero positions, etc. This paper presents a comprehensive GFET model that is simple enough for being used in hand-calculations during circuit design and at the same time it is accurate enough to capture the electrical characteristics of the devices in the operating regions of interest. Closed analytical expressions are provided for the drain current I_D, small-signal transconductance gain g_m, output resistance r_o, and parasitic capacitances C_{gs} and C_{gd}. In addition, figures of merit such as intrinsic voltage gain A_V, transconductance efficiency g_m/I_D, and transit frequency f_T are presented. The proposed model has been compared to a complete analytical model and also to measured data available in current literature. The results show that the proposed model follows closely to both the complete analytical model and the measured data; therefore, it can be successfully applied in the design of GFET analog circuits.

Index Terms—Graphene, FET, Analytic Model

I. INTRODUCTION

THE reduction of dimensions in Silicon based transistors faces great challenges as dimensions approach atomic sizes and physical limits will be eventually reached. A great deal of research has focused during the last years in new materials that alleviate these limitations. One of these materials is Graphene [1], a two-dimensional structure with outstanding electrical characteristics such as very high electron mobilities in the order of 20000 cm^{2}V^{-1}s^{-1} on silicon substrates [2]. The possibility of achieving such high electron mobilities,

which are orders of magnitude higher than silicon based technologies, makes GFETs excellent candidates for replacing nanometer CMOS transistors in future high-speed analog electronic circuits [3].

Since the demonstration of the first GFET [4], the technology has evolved very fast. In just very few years it has been shown that de-embedded, intrinsic GFETs transit frequencies f_T are comparable to or higher than those of similarly sized nanometer CMOS devices [5][6][7]. Actual measured f_T is, in fact, much lower than CMOS, mainly due to the presence of interface and contact resistances. These resistances are a serious issue in GFET technology and therefore there are active research efforts on finding ways to reduce their impact. Latest research results have shown that contact resistances well bellow 100 Ω μm are possible; for instance, contact resistances as low as 20 Ω μm were measured for hydrogen intercalated graphene growth [8]. RF/Analog design uses seldom the minimum width transistors of a technology. Minimum transistor sizes in RF applications are generally above 20 μm - 30 μm, whereas in analog-baseband circuits the dimensions can be as large as hundreds of micrometers. Transistors with these widths would present small contact resistances with values similar to those of parasitic resistances on the metallic interconnection/vias in nanometer CMOS technologies. Their impact on the circuit performance would be the same as other parasitics, and therefore, they can be handled using the same circuit design techniques that are used in todays CMOS circuits.

Likewise, high transconductance gain g_m values were also demonstrated [9][5]. In addition, it has been shown that the drain current in GFET transistors has a saturation region [10]. This is an important characteristic since it facilitates the use the GFETs as voltage-controlled current sources, and consequently, the design of analog circuits in general. Until now, drain current saturation has been mainly observed in long gate GFET devices, and short-channel GFETs still present unsatisfying current saturation behavior. Nevertheless, it has been reported that the use of bilayer graphene can result in important current saturation improvements [11]. Likewise, lateral graphene heterostructures have also been suggested as a possible solution to enhance the current saturation [12]. Although GFET technology still faces technological challenges, projections of GFET vs. CMOS high-speed analog IC performance [13] have shown that GFET technology can potentially surpass CMOS in the near future provided that the

low field mobility μ is kept above certain values.

The development of GFET devices has been accompanied by the appearance of electrical models that can be used to describe the electrical characteristics of the device and also to simulate circuits [14][15][16][17][18][19]. Some of these initial models are physical models which do not have closed expressions and therefore require the use of numerical methods to find solutions. These models are very useful to explain the device physics; however, they are not suitable for implementation in analog circuit modeling languages such as SPICE or Verilog-A. Other models are compact analytical models which can be written in SPICE or Verilog-A and used to simulate circuits with EDA CAD tools. These models, however, are still very complex for being used during circuit design. Analog circuit designers make many decisions based on hand-calculations, and therefore require simple analytical expressions.

This paper introduces a comprehensive model which provides the circuit design community with simple mathematical expressions to analyze GFETs. The proposed model is based on [19] and consists of simplifications and assumptions which are valid for the first triode region and saturation/negative output resistance region which are relevant for analog circuit design. The paper is organized as follows. Section II presents a brief summary of the large signal model that is used as base of this work. A simplified analytical expression for the drain current as a function of internal voltages and technology parameters is provided in Section III. Section IV provides closed expressions for small-signal hybrid-π models (g_m, r_o, C_{gs}, C_{gd}). Section V presents closed expression for figures of merit A_V, g_m/id and f_T . Finally, a summary of the simplified model is provided.

II. LARGE SIGNAL MODEL

An exhaustive study of the drain-source current using the drift equation for GFET transistors can be found in [19]. The result of this study shows that the drain-source current can be expressed as:

$$I_D = \mu W \frac{\int_0^{V_{DSi}} \left(|Q_{net}| + e n_{puddle} \right) dV}{L + \mu \left| \int_0^{V_{DSi}} \frac{1}{v_{SAT}} dV \right|} \tag{1}$$

where μ is the mobility, W the transistor width, L the transistor length, Q_{net} the net mobile charge density per unit area, e the elementary charge (1.6×10^{-19} As), $n_{puddle} = \frac{\Delta^2}{\pi \hbar^2 v_f{}^2}$, and V_{DSi} the internal drain-source voltage. The parameter Δ represents the spacial inhomogeneity of the electrostatic potential, $\hbar$ is the reduced Planck constant, and v_f is the Fermi velocity.

For simplicity, the integral in the numerator of (1) can be split and solved independently.

$$I_D = \mu W \frac{NUM}{DEN} = \mu W \frac{NUM_1 + NUM_2}{DEN} \tag{2}$$

where the first term in the numerator is:

$$NUM_1 = \beta \int_0^{V_{DSi}} \left[\frac{-C_{TOP}}{2\beta} + \frac{\sqrt{C_{TOP}{}^2 + 4\beta \left| C_{TOP}(V_{GSi} - V) + e N_f \right|}}{2\beta} \right]^2 dV \tag{3}$$

and the factor $\beta = e^3/(\pi \left(\hbar v_f\right)^2)$. C_{TOP} is the top oxide capacitance, V the potential variation along the channel due to V_{DS} and N_f is a term that accounts for the net acceptor/donor doping. Since the graphene material does not have a bandgap, GFETs do not switch off completely like other FET devices. Instead, they show a minimum conduction point which is known as the Dirac point. The doping level set by N_f is responsible of shifting the Dirac point in a similar way than the intentional doping used to control the threshold voltage in MOS devices. In practice, the Dirac point is also affected by V_{DS}; nevertheless, N_f sets an absolute offset which is biasing independent. Accordingly, it is possible to define a zero-bias threshold voltage for GFET devices as :

$$V_{TH,0} = e N_f / C_{TOP} \tag{4}$$

and the effective gate-source overdrive voltage as:

$$V_{eff} = V_{GSi} + V_{TH,0} \tag{5}$$

where V_{GSi} is the internal gate-source voltage. Accordingly, (3) can be rewritten as:

$$NUM_1 = \beta \int_0^{V_{DSi}} \left[\frac{-C_{TOP}}{2\beta} + \frac{\sqrt{C_{TOP}{}^2 + 4\beta \left| C_{TOP}(V_{eff} - V) \right|}}{2\beta} \right]^2 dV \tag{6}$$

Equation (6) is simplified by introducing the integration variable to $z = C_{TOP}(V_{eff} - V)$. The integral has the following symbolic solution:

$$NUM_{1(z>0)} = -\frac{1}{\beta^2 C_{TOP}} \left[\frac{C_{TOP}{}^4}{32} - \frac{C_{TOP} \left(C_{TOP}{}^2 + 4\beta z \right)^{3/2}}{12} + \frac{\beta^2 z^2}{2} + \frac{\beta C_{TOP}{}^2 z}{2} \right]\Bigg|_{z_1}^{z_2}$$

$$NUM_{1(z<0)} = -\frac{1}{\beta^2 C_{TOP}} \left[-\frac{C_{TOP}{}^4}{32} + \frac{C_{TOP} \left(C_{TOP}{}^2 - 4\beta z \right)^{3/2}}{12} - \frac{\beta^2 z^2}{2} + \frac{\beta C_{TOP}{}^2 z}{2} \right]\Bigg|_{z_1}^{z_2} \tag{7}$$

where $z_1 = C_{TOP} V_{eff}$ and $z_2 = C_{TOP}(V_{eff} - V_{DSi})$.

The second term of the numerator is given by:

$$NUM_2 = \int_0^{V_{DSi}} e n_{puddle} dV = e n_{puddle} V_{DSi} \tag{8}$$

The denominator in (2) can be expressed as:

$$DEN = L + \mu \left| \int_0^{V_{DSi}} \frac{1}{v_{SAT}} dV \right| \qquad (9)$$

which can be simplified assuming an average v_{SAT} given by:

$$v_{SAT,AV} = \frac{\omega}{\sqrt{\pi \frac{|Q_{NET,AV}|}{e} + n_{puddle}}} \qquad (10)$$

where ω is obtained from the surface phonon energy of the substrate $\hbar\omega$ and $Q_{NET,AV}$ is the average charge given by:

$$Q_{NET,AV} = \beta \left[\frac{-C_{TOP}}{2\beta} + \frac{\sqrt{C_{TOP}^2 + 4\beta |C_{TOP}(V_{eff} - V_{DSi}/2)|}}{2\beta} \right]^2 \qquad (11)$$

With the previous assumption, the denominator can be expressed as:

$$DEN = L + \frac{\mu}{v_{SAT,AV}} |V_{DSi}| \qquad (12)$$

The accuracy of the model has been successfully evaluated by its authors by comparing it against numeric models and measured data of different GFET devices built by different groups [20] [21] [9].

The whole model is very compact and perfectly suitable for building SPICE and Verilog-A models; and consequently, it is also suitable for circuit simulation purposes. While the model shows outstanding accuracy, it can be appreciated that it is still complicated to be used by analog circuit designers. The main problem is that it lacks a simple closed mathematical expression for the drain current like the one that is available for CMOS FET transistors (Shichman-Hodges model) [22] or like the collector current in bipolar transistors (Ebers-Moll model) [23]. A simple expression for the drain current is fundamental since the parameters for small-signal hybrid-π model and figures of merit are directly derived from this equation. The later ones represent the foundation of electronic circuit theory and are the main tools that analog circuit designers have in order to analyze circuit topologies and make design decisions. Therefore, it is of paramount importance to obtain a simplified expression for the GFET drain current.

III. SIMPLIFIED LARGE SIGNAL MODEL

The difficulty in finding a simple expression for the GFET drain current lies in the complexity of (7). Fortunately, the replacement of technology dependent parameters taken from the measured GFETs and physical constants unveils that there is a term that dominates and therefore (7) can be reduced to:

$$NUM_1 \simeq -\frac{1}{2} \frac{z^2}{C_{TOP} \times sign(z)} \Big|_{z_1}^{z_2} \qquad (13)$$
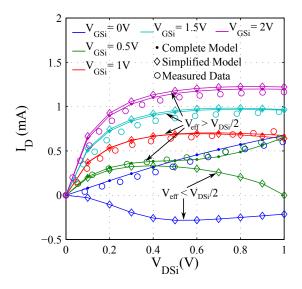

Fig. 1. Drain current for a 440 nm length, 1 μm width GFET calculated using the complete model, simplified model, and measured data from [20].

which for $z > 0$ (typical case in analog design) can be expressed as:

$$NUM_1 \simeq C_{TOP} V_{DSi} \left(V_{eff} - \frac{V_{DSi}}{2} \right) \qquad (14)$$

For typical technology parameters $NUM_1 \gg NUM_2$. As a result, NUM_2 can be disregarded and $NUM \simeq NUM_1$.

Expression (12) becomes complicated when $v_{SAT,AV}$ is replaced by (10) and $Q_{NET,AV}$ by (11) . However, it can also be simplified under the assumption that $V_{eff} > V_{DSi}/2$, and $n_{puddle} \ll \pi|Q_{NET,AV}|/e$. Under these conditions, $|Q_{NET,AV}| \approx C_{TOP} (V_{eff} - V_{DSi}/2)$ and the denominator can be simplified to:

$$DEN \simeq L + \frac{\mu}{\omega} \sqrt{\frac{\pi C_{TOP}}{e}} V_{DSi} \sqrt{V_{eff} - \frac{V_{DSi}}{2}} \qquad (15)$$

Finally, the GFET drain current is found by replacing (14) and (15) into (2):

$$I_D \simeq \frac{\mu W C_{TOP} (V_{eff} - V_{DSi}/2)}{\frac{L}{V_{DSi}} + \frac{\mu}{\omega} \sqrt{\frac{\pi C_{TOP}}{e}} \sqrt{V_{eff} - V_{DSi}/2}} \qquad (16)$$

which is a closed analytical expression that relates the main technology parameters and biasing conditions. Fig. 1, Fig. 2, and Fig. 3 show I_D vs. V_{DS_i} plots for GFETs of 1 um width and 440 nm, 1 um, and 3um length respectively from [20]. I_D is calculated by using (16) and the complete model including fitting parameters from [19]. For these devices, N_f is approximately 0, and therefore $V_{TH,0} \approx 0$ V. The other parameters have the following values: $C_{TOP} = 3.6 \times 10^{-3}$F/m^2, $\mu = 7000$ cm^{2}V^{-1}s^{-1}, and $\hbar\omega = 56$ meV. V_{GS_i} takes values from 0 V to 2 V in steps of 500 mV. It can be appreciated that the simplified model matches very well both the complete model and the measured data for $V_{eff} > V_{DS_i}/2$. The plots show that both the first triode region and the saturation/negative resistance region are correctly modeled by
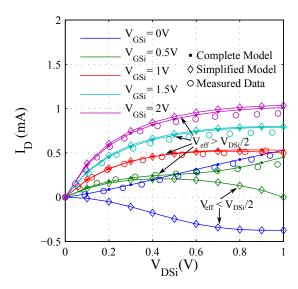
Fig. 2. Drain current for a 1 μm length, 1 μm width GFET calculated using the complete model, simplified model, and measured data from [20].

Fig. 4. Drain current vs. V_{GSi} for a 440 nm length, 1 μm width GFET from [20] calculated using the complete model, and simplified model
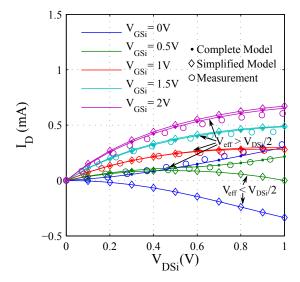

Fig. 3. Drain current for a 3 μm length, 1 μm width GFET calculated using the complete model, simplified model, and measured data from [20].

(16). The first triode region can be used to build resistive loads or switches whereas the saturation region can be used to build voltage-controlled current-sources and in some biasing conditions negative resistance loads. The second triode region is not modeled by (16) since the assumption $V_{eff} > V_{DS_i}/2$ does not hold anymore. This region, nevertheless, seems to have little practical value in analog design.

Fig. 4 shows I_D vs. V_{GSi} curves for the 440 nm lenght, 1 μm width GFET transistor from [20]. The ambipolar curves show also that the simplified model follows closely the complete model for $V_{eff} > V_{DS_i}/2$.

One important observation that can be made from the simplified expressions is the impact of short-channel lengths on the GFET drain current. It has been experimentally shown
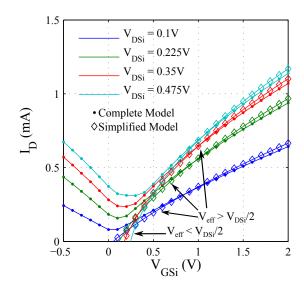
that there is strong dependence of short lengths in the GFET transport characteristics [24] [25]. This dependence can be analytically explained by (15) where it can be seen that $DEN \simeq L$ only for $V_{DS_i} \approx 0$. Once the gate and drain bias voltages increase, the value of DEN departs from L and increases quickly. For very short lengths and high electric fields, the current becomes independent of the channel length, something that has also been confirmed experimentally in [26]. Under these conditions, the drain current saturates, stops depending on μ, and takes a value of approximately:

$$I_D \simeq \omega W \sqrt{\frac{C_{TOP} \times e}{\pi}} \sqrt{V_{eff} - V_{DSi}/2} \qquad (17)$$

IV. SMALL SIGNAL MODEL

While the large signal model in (16) encloses the physics of the device in a single expression, it is still too complex to be used in quantitative circuit analyses of the behavior of amplifier configurations. These analyses are normally performed by taking advantage of linear system theory in which a simplified small-signal representation of the transistor biased in the operating point is used. The small-signal representation, also called hybrid-π model, is shown in Fig. 5. The parameters g_m, r_o, C_{gs}, and C_{gd} can be obtained by linearization of the large signal model. Naturally, the small-signal representation provides only limited information which is valid for small excursions from the operating point. However, it allows to calculate and estimate in an easy way small-signal dynamic linear behavior of gain, phase, poles, zeros, impulse response, etc. Large-signal behavior is non-linear and therefore its analysis requires the use of the complete model and a circuit simulator.

The derivation of small-signal parameters for the GFET transistor is presented in the following subsections.
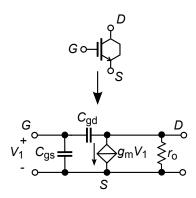
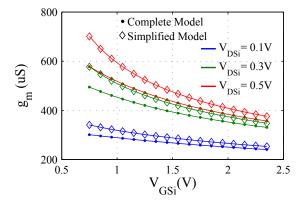Fig. 5. GFET Symbol and equivalent hybrid-π model for small-signal analysis.
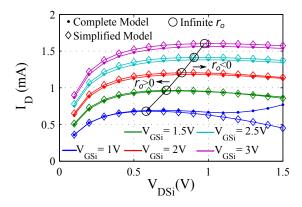

Fig. 7. Calculation of negative r_o biasing requirements for the 440 nm length, 1 μm width GFET from [20]. $N_f \approx 0$, $V_{TH,0} \approx 0$ V, $C_{TOP} = 3.6 \times 10^{-3}$F/m^2, $\mu = 7000$ cm^{2}V^{-1}s^{-1}, and $\hbar\omega = 56$ meV.

be directly derived from (16):

$$g_o = \left. \frac{\delta I_D}{\delta V_{DSi}} \right|_{V_{GSi,const.}} \tag{20}$$

$$g_o = \frac{I_D}{V_{eff} - V_{DSi}/2} \left[-\frac{1}{2} + \frac{I_D}{\mu W C_{TOP}} \left(\frac{L}{V_{DSi}^2} + \frac{\frac{\mu}{\omega}\sqrt{\frac{\pi C_{TOP}}{e}}}{4\sqrt{V_{eff} - V_{DSi}/2}} \right) \right] \tag{21}$$

One important characteristic of the GFET device is that under some biasing conditions, g_0 becomes negative [27] [28]. A negative g_0 makes the device unstable, and in general this region needs to be avoided in amplifier design. On the other hand, a negative g_0 is a very welcome asset when designing oscillators. The biasing conditions in which g_o changes from positive to negative values can be found by making $g_0 = 0$ in (21) and solving for V_{DS}. The expression for this boundary condition is:

$$V_{DS,lim} = \frac{-2L + \sqrt{4L\left(L + \frac{\mu}{\omega}\sqrt{\frac{\pi C_{TOP}}{e}} V_{eff}^{3/2}\right)}}{\frac{\mu}{\omega}\sqrt{\frac{\pi C_{TOP}}{e}}\sqrt{V_{eff}}} \tag{22}$$

Fig 7 shows I_D vs. V_{DS} plots for different V_{GS} voltages. In addition, the plot shows the points in which $g_o = 0$ ($r_o = \infty$) which were found by using (22). It can be seen that (22) predicts very well the transition from positive to negative output resistance.

C. Total Channel Charge

The distributed gate capacitance in GFET devices is modeled as the series capacitance of C_{TOP} and the quantum capacitance C_q in the graphene channel [15]:

$$Cg = \frac{C_q \times C_{TOP}}{C_q + C_{TOP}} \tag{23}$$

where the parameter C_q relates the distributed charge along the graphene channel and its potential V_{CH}, which depends

Fig. 6. Transconductance g_m calculated using the complete and simplified model for the 440 nm length, 1 μm width GFET from [20]. $N_f \approx 0$, $V_{TH,0} \approx 0$ V, $C_{TOP} = 3.6 \times 10^{-3}$F/m^2, $\mu = 7000$ cm^{2}V^{-1}s^{-1}, and $\hbar\omega = 56$ meV.

A. Transconductance g_m

The expression for the transconductance gain can be directly derived from (16):

$$g_m = \left. \frac{\delta I_D}{\delta V_{GSi}} \right|_{V_{DSi,const.}} \tag{18}$$

$$g_m = \left(\frac{I_D}{V_{eff} - V_{DSi}/2} \right) \left(1 - \frac{1}{2}\frac{I_D}{W\omega} \times \sqrt{\frac{\pi}{e \times C_{TOP}}} \frac{1}{\sqrt{V_{eff} - V_{DSi}/2}} \right) \tag{19}$$

Fig. 6 shows g_m values calculated using (19) and the complete model. It can be seen that (19) follows closely the complete model in particular for $V_{eff} > V_{DSi}/2$. It is interesting to notice that g_m drops substantially at large V_{GSi} biasing voltages, mainly due to the effect of V_{SAT}. Therefore, the best g_m performance is actually achieved at low V_{eff} voltages.

B. Output resistance r_o

The output resistance can be calculated as $r_0 = 1/g_0$ where g_0 is the output conductance. An expression for g_o can also

strongly on both V_{GS} and V_{DS}. The total charge stored in the gate capacitance can be found by considering that the charge of all capacitors is the same when they are connected in series. Accordingly, the total charge stored in the gate capacitance is equal to the total charge in the graphene channel Q_{CH}. The separation of the gate capacitance between Gate-Source capacitance and Gate-Drain capacitance can be done by taking partial derivatives of Q_{CH}. Consequently, it is beneficial to find a simple closed expression for Q_{CH} which can be easily differentiated. Q_{CH} can be expressed as [19]:

$$Q_{CH} = W \int_{0}^{L} \left(Q_{NET}(x) + en_{puddle} \right) dx \tag{24}$$

By changing the integration variable dx to dV and reordering the expression, Q_{CH} becomes:

$$Q_{CH} = \frac{eW}{E_{AV}} \int_{0}^{V_{DSi}} \left(\frac{\beta}{e} |V_{CH}| V_{CH} + n_{puddle} \right) dV \tag{25}$$

where E_{AV} is the average electric field which is given by:

$$E_{AV} \approx \frac{dV}{dx} \approx \frac{V_{DSi}}{L} \tag{26}$$

The integral in (25) is similar to that in (6) and therefore it is solved in the same way. Likewise, there is a quadratic term that dominates and therefore Q_{CH} can be reduced to:

$$Q_{CH} \approx \frac{e \times W}{2E_{AV}} \left(-\frac{z^2}{C_{TOP} \times e} \right) \Bigg|_{z_1}^{z_2} \tag{27}$$

which after replacing z_1 and z_2 becomes:

$$Q_{CH} \approx \frac{WC_{TOP}}{E_{AV}} V_{DSi} \left(V_{eff} - \frac{V_{DSi}}{2} \right) \tag{28}$$

Finally, a simplified expression for Q_{CH} is found by replacing (26) into (28):

$$Q_{CH} \approx C_{TOP} W L \left(V_{eff} - V_{DSi}/2 \right) \tag{29}$$

D. Gate-Source Capacitance C_{gs}

The small-signal gate-source capacitance can be calculated as:

$$C_{gs} = \frac{\delta Q_{CH}}{\delta V_{GSi}} \Bigg|_{V_{DSi,const.}} \tag{30}$$

$$C_{gs} = C_{TOP} W L \tag{31}$$

Fig. 8 shows plots of C_{gs} calculated using (31) and the complete model. It can be seen that for $V_{eff} > V_{DS}/2$, C_{gs} approaches the value of the total oxide capacitance. For large V_{eff} values the error is within 5%.
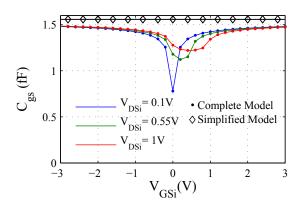

Fig. 8. C_{gs} calculation using the complete and simplified model for the 440 nm length, 1 μm width GFET from [20]. $N_f \approx 0$, $V_{TH,0} \approx 0$ V, $C_{TOP} = 3.6 \times 10^{-3} \text{F/m}^2$, $\mu = 7000 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$, and $\hbar\omega = 56$ meV.
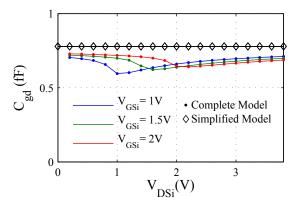

Fig. 9. C_{gd} calculation using the complete and simplified model for the 440 nm length, 1 μm width GFET from [20]. $N_f \approx 0$, $V_{TH,0} \approx 0$ V, $C_{TOP} = 3.6 \times 10^{-3} \text{F/m}^2$, $\mu = 7000 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$, and $\hbar\omega = 56$ meV.

E. Gate-Drain Capacitance C_{gd}

The small-signal gate-drain capacitance can be calculated as:

$$C_{gd} = -\frac{\delta Q_{CH}}{\delta V_{DSi}} \Bigg|_{V_{GSi,const.}} \tag{32}$$

$$C_{gd} = \frac{C_{TOP} W L}{2} \tag{33}$$

Fig. 9 shows plots of C_{gd} calculated using (33) and the complete model. In this case it is also possible to see that even though C_{gd} values calculated with the complete model have valleys at different drain biasing conditions, their values are close to the value predicted by (33). For large V_{DS} values the error is within 15%.

Fig. 10 shows C_{gs}, C_{gd}, and I_D vs. V_{GSi}. It is interesting to see that despite the fact that the capacitances change for different biasing conditions, their values approximate very well the simplified model when enough V_{GSi} and V_{DSi} bias is present.
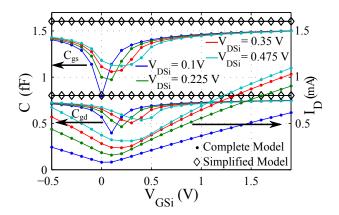
Fig. 10. C_{gs}, C_{gd}, and I_D calculation using the complete and simplified model for the 440 nm length, 1 μm width GFET from [20]. $N_f \approx 0$, $V_{TH,0} \approx 0$ V, $C_{TOP} = 3.6 \times 10^{-3}$F/m^2, $\mu = 7000$ cm^{2}V^{-1}s^{-1}, and $\hbar\omega = 56$ meV.
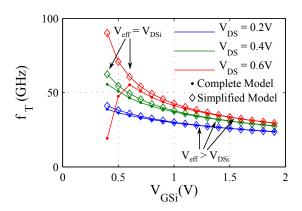

Fig. 11. Transit Frequency f_T calculation using the complete and simplified model for the 440 nm length, 1 μm width GFET from [20]. $N_f \approx 0$, $V_{TH,0} \approx 0$ V, $C_{TOP} = 3.6 \times 10^{-3}$F/m^2, $\mu = 7000$ cm^{2}V^{-1}s^{-1}, and $\hbar\omega = 56$ meV.

V. FIGURES OF MERIT

The extraction of small-signal parameters allows the calculation of figures of merit that can be used to make performance comparisons. The main figures of merit used to evaluate amplifying devices are: intrinsic voltage gain A_V, transconductance efficiency g_m/I_D, and transit frequency f_T. Expressions for these figures of merit are found in the following subsections.

A. Intrinsic Voltage Gain A_V

The intrinsic voltage gain estimates the low frequency voltage amplification capabilities of the device and can be calculated as:

$$A_V = g_m \times r_0 \tag{34}$$

$$
A_V = \left(1 - \frac{I_{DSi}}{2W\omega}\sqrt{\frac{\pi}{eC_{TOP}}}\frac{1}{\sqrt{V_{eff}-V_{DSi}/2}}\right) \Bigg/
$$
$$
\left[-\frac{1}{2} + \frac{I_{DSi}}{\mu WC_{TOP}}\left(\frac{L}{V_{DSi}{}^2} + \frac{\mu}{4\omega}\sqrt{\frac{\pi C_{TOP}}{e}}\times \right.\right. \tag{35}
$$
$$
\left.\left.\frac{1}{\sqrt{V_{eff}-V_{DSi}/2}}\right)\right]
$$

B. Transconductance Efficiency g_m/I_D

The g_m/I_D relates the transconductance amplification capability of the device and the drain current that is required to produce it. Therefore, it is a measure of the power consumption efficiency of the amplifying device. The expression for g_m/I_D can be directly obtained from (19):

$$
\frac{g_m}{I_D} = \left(\frac{1}{V_{eff}-V_{DSi}/2}\right) \times
$$
$$
\left(1 - \frac{1}{2}\frac{I_D}{W\omega}\sqrt{\frac{\pi}{e\times C_{TOP}}}\frac{1}{\sqrt{V_{eff}-V_{DSi}/2}}\right) \tag{36}
$$

TABLE I
SUMMARY OF THE SIMPLIFIED GFET MODEL

Name	Expression	Units
I_D	$\dfrac{\mu W C_{TOP}(V_{eff}-V_{DSi}/2)}{L/V_{DSi}+\frac{\mu}{\omega}\sqrt{\pi C_{TOP}/e}\sqrt{V_{eff}-V_{DSi}/2}}$	[A]
V_{eff}	$V_{GSi} + eN_f/C_{TOP}$	[V]
C_{gs}	$C_{TOP}WL$	[F]
C_{gd}	$C_{TOP}WL/2$	[F]

C. Transit Frequency f_T

The transit frequency estimates the frequency at which the current gain of the device drops to 1, and it is a measure of its high-speed and bandwidth capabilities. The transit frequency is defined as:

$$f_T = \frac{g_m}{2\pi\left(C_{gs}+C_{gd}\right)} \tag{37}$$

$$
f_T = \frac{\left(\frac{I_D}{V_{eff}-V_{DSi}/2}\right)}{2\pi\left(\frac{3}{2}C_{TOP}WL\right)} \times
$$
$$
\left(1 - \frac{1}{2}\frac{I_D}{W\omega}\sqrt{\frac{\pi}{e\times C_{TOP}}}\frac{1}{\sqrt{V_{eff}-V_{DSi}/2}}\right) \tag{38}
$$

Fig. 11 shows plots of f_T calculated using (38) and the complete model. It can be seen that there is very good matching for most biasing points, and disagreements start to become visible only when $V_{eff} < V_{DS}$.

VI. SUMMARY

A summary of the simplified GFET model is shown in Table I. The expressions in this table were used to extract small-signal hybrid-π model parameters and figures of merit typically used to compare the performance of transistors. The proposed model has been validated by comparing it against a complete analytical model and to measured data available in current literature. Whereas the complete analytical model hides the effects of physical parameters behind many separate

calculations, the proposed model provides a simple expression that enables direct identification of dominant physical parameters. In addition, the proposed GFET model is ready for use in circuit design in exactly the same way as the Shichman-Hodges and Ebers-Moll models are used for CMOS and bipolar circuit design respectively.

REFERENCES

[1] K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, Y. Zhang, S. V. Dubonos, I. V. Grigorieva, and A. A. Firsov, "Electric Field Effect in Atomically Thin Carbon Films," *Science*, vol. 306, no. 5696, pp. 666–669, 2004.

[2] J. Chen, C. Jang, and S. Xiao, "Intrinsic and extrinsic performance limits of graphene devices on SiO2," *Nature Nanotechnology*, vol. 3, no. 4, pp. 206–209, 2008.

[3] F. Schwierz, "Graphene transistors." *Nature Nanotechnology*, vol. 5, no. 7, pp. 487–96, Jul. 2010.

[4] M. C. Lemme, T. J. Echtermeyer, M. Baus, and H. Kurz, "A Graphene Field-Effect Device," *IEEE Electron Device Letters*, vol. 28, no. 4, pp. 282–284, Apr. 2007.

[5] Y. Wu, D. Farmer, A. Valdes-Garcia, W. Zhu, K. Jenkins, C. Dimitrakopoulos, P. Avouris, and Y.-M. Lin, "Record high RF performance for epitaxial graphene transistors," in *Proc. IEEE Electron Devices Meeting (IEDM)*, Sep. 2011, pp. 23.8.1–23.8.3.

[6] Y.-M. Lin, S. Member, D. B. Farmer, K. A. Jenkins, Y. Wu, J. L. Tedesco, R. L. Myers-Ward, C. R. Eddy, D. K. Gaskill, C. Dimitrakopoulos, and P. Avouris, "Enhanced Performance in Epitaxial Graphene FETs With Optimized Channel Morphology," *IEEE Electron Device Letters*, vol. 32, no. 10, pp. 1343–1345, 2011.

[7] L. Liao, Y.-C. Lin, M. Bao, R. Cheng, J. Bai, Y. Liu, Y. Qu, K. L. Wang, Y. Huang, and X. Duan, "High-speed graphene transistors with a self-aligned nanowire gate," *Nature*, vol. 467, no. 7313, pp. 305–308, Sep. 2010.

[8] J. S. Moon, M. Antcliffe, H. C. Seo, D. Curtis, S. Lin, A. Schmitz, I. Milosavljevic, a. a. Kiselev, R. S. Ross, D. K. Gaskill, P. M. Campbell, R. C. Fitch, K.-M. Lee, and P. Asbeck, "Ultra-low resistance ohmic contacts in graphene field effect transistors," *Appl. Phys. Lett.*, vol. 100, no. 20, p. 203512, 2012.

[9] J. Moon, D. Curtis, S. Bui, M. Hu, D. Gaskill, J. Tedesco, P. Asbeck, G. Jernigan, B. VanMil, R. Myers-Ward, C. Eddy, P. Campbell, and X. Weng, "Top-Gated Epitaxial Graphene FETs on Si-Face SiC Wafers With a Peak Transconductance of 600 mS/mm," *IEEE Electron Device Letters*, vol. 31, no. 4, pp. 260–262, Apr. 2010.

[10] I. Meric, M. Y. Han, A. F. Young, B. Ozyilmaz, P. Kim, and K. L. Shepard, "Current saturation in zero-bandgap, top-gated graphene field-effect transistors." *Nature Nanotechnology*, vol. 3, no. 11, pp. 654–9, Nov. 2008.

[11] B. N. Szafranek, G. Fiori, D. Schall, D. Neumaier, and H. Kurz, "Current saturation and voltage gain in bilayer graphene field effect transistors." *Nano letters*, vol. 12, no. 3, pp. 1324–8, Mar. 2012.

[12] J. S. Moon, H.-c. Seo, F. Stratan, M. Antcliffe, A. Schmitz, R. S. Ross, A. a. Kiselev, V. D. Wheeler, L. O. Nyakiti, D. K. Gaskill, K.-M. Lee, and P. M. Asbeck, "Lateral Graphene Heterostructure Field-Effect Transistor," *IEEE Electron Device Letters*, vol. 34, no. 9, pp. 1190–1192, Sep. 2013.

[13] S. Rodriguez, S. Vaziri, M. Ostling, A. Rusu, E. Alarcon, and M. Lemme, "RF Performance Projections of Graphene FETs vs. Silicon MOSFETs," *ECS Solid State Letters*, vol. 1, no. 5, pp. 39–41, 2012.

[14] K. L. Shepard, I. Meric, and P. Kim, "Characterization and modeling of graphene field-effect devices," in *Proc. IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Nov. 2008, pp. 406–411.

[15] S. Thiele, J. Schaefer, and F. Schwierz, "Modeling of graphene metal-oxide-semiconductor field-effect transistors with gapless large-area graphene channels," *J. Appl. Phys.*, vol. 107, no. 9, p. 094505, 2010.

[16] D. Jimenez and O. Moldovan, "Explicit drain-current model of graphene field-effect transistors targeting analog and radio-frequency applications," *IEEE Trans. Electron Devices*, vol. 58, no. 11, pp. 4049–4052, 2011.

[17] O. Habibpour, S. Cherednichenko, J. Vukusic, and J. Stake, "Mobility Improvement and Microwave Characterization of a Graphene Field Effect Transistor With Silicon Nitride Gate Dielectrics," *IEEE Electron Device Letters*, pp. 1–3, 2011.

[18] S. Fregonese, N. Meng, H.-N. Nguyen, C. Majek, C. Maneux, H. Happy, and T. Zimmer, "Electrical compact modelling of graphene transistors," *Solid-State Electronics*, vol. 73, pp. 27–31, 2012.

[19] S. Fregonese, M. Magallo, C. Maneux, H. Happy, and T. Zimmer, "Scalable Electrical Compact Modelling for Graphene FET Transistors," *IEEE Trans. on Nanotechnology*, vol. 12, no. 4, pp. 539–546, 2013.

[20] I. Meric, C. Dean, A. Young, J. Hone, P. Kim, and K. L. Shepard, "Graphene field-effect transistors based on boron nitride gate dielectrics graphene," in *Proc. IEEE Electron Devices Meeting (IEDM)*, 2010, pp. 556–559.

[21] J. Kedzierski, A. Reina, P. Healey, P. Wyatt, and C. Keast, "Graphene-on-Insulator Transistors Made Using C on Ni Chemical-Vapor Deposition," *IEEE Electron Device Letters*, vol. 30, no. 7, pp. 745–747, Jul. 2009.

[22] H. Shichman and D. A. Hodges, "Modeling and Simulation of Insulated-Gate Field-Effect Transistor Switching Circuits," *IEEE J. Solid-State Circuits*, vol. 3, no. 3, pp. 285–289, 1968.

[23] J. J. Ebers and J. L. Moll, "Large-Signal Behavior of Junction Transistors," in *Proc. of the IRE*, 1954, pp. 1761–1772.

[24] S. Han, Z. Chen, and A. Bol, "Channel-Length-Dependent Transport Behaviors of Graphene Field-Effect Transistors," *IEEE Electron Device Letters*, vol. 32, no. 6, pp. 812–814, 2011.

[25] A. Venugopal, J. Chan, X. Li, C. W. Magnuson, W. P. Kirk, L. Colombo, R. S. Ruoff, and E. M. Vogel, "Effective mobility of single-layer graphene transistors as a function of channel dimensions," *J. Appl. Phys.*, vol. 109, no. 10, p. 104511, 2011.

[26] I. Meric, C. R. Dean, A. F. Young, N. Baklitskaya, N. J. Tremblay, C. Nuckolls, P. Kim, and K. L. Shepard, "Channel length scaling in graphene field-effect transistors studied with pulsed current-voltage measurements." *Nano letters*, vol. 11, no. 3, pp. 1093–7, Mar. 2011.

[27] Y. Wu, D. B. Farmer, W. Zhu, S.-J. Han, C. D. Dimitrakopoulos, A. a. Bol, P. Avouris, and Y.-M. Lin, "Three-terminal graphene negative differential resistance devices." *ACS Nano*, vol. 6, no. 3, pp. 2610–6, Mar. 2012.

[28] R. Grassi, T. Low, A. Gnudi, and G. Baccarani, "Contact-Induced Negative Differential Resistance in," *IEEE Trans. Electron Devices*, vol. 60, no. 1, pp. 140–146, 2013.

Saul Rodriguez received the B.Sc. degree in Electrical Engineering from the Army Polytechnic School (ESPE), Quito, Ecuador in 2001, the M.Sc. degree in System-on-Chip Design in 2005 and the Ph.D. degree in Electronic and Computer Systems in 2009 from the Royal Institute of Technology (KTH), Stockholm, Sweden. His research area covers from RF CMOS circuit design for wideband front-ends, ultra-low power circuits for medical applications, and graphene-based RF and AMS circuits.

Sam Vaziri received the B.Sc. and M.Sc. in Solid State Physics from Shahid Beheshti University and K.N.Toosi University of Technology, Tehran, Iran. In 2011, he received his second M.Sc. degree in Nanotechnology from KTH Royal Institute of Technology, Stockholm, Sweden. He is currently a PhD candidate at KTH, investigating graphene electronic and optoelectronic devices.

Anderson Smith received his bachelors and masters degrees from the Georgia Institute of Technology in mechanical engineering and then a second masters degree in nanotechnology at KTH Royal Institute of technology. He is currently working on his Ph.D. at KTH Royal Institute of Technology in the school of Information and Communication Technology. His research focuses primarily on graphene sensors and transistors for more and Moore applications.

Sébastien Frégonèse received the M.Sc. and the Ph.D. degrees in electronics from the Universit Bordeaux, Talence, France, in 2002 and 2005, respectively. From 2005 to 2006, he was with the Technical University of Delft, The Netherlands. In 2007, he joined the Centre National de la Recherche Scientifique (CNRS), France. His research interests focus on electrical compact modeling and characterization of devices such as the SiGe HBTs and carbon based transistors.

Mikael Ostling (M85SM97F04) received the Ph.D. degree from Uppsala University, Uppsala, Sweden, in 1983. He is a Professor and Head of the Department of Integrated Devices and Circuits with the School of Information and Communication Technology, KTH.

Max Lemme received the Dr.-Ing. (2003) degree in Electrical Engineering from RWTH Aachen University, Germany. He is Heisenberg-Professor for Graphene-based Nanotechnology at the University of Siegen, Germany. From 2010-2013 He was Guest Professor at KTH, Sweden and from 2008-2010 he was a research fellow at Harvard University. From 1998-2008 he worked at nanotechnology start-up AMO GmbH, Germany, as Head of Technology Department. His research interests include non-conventional nano-CMOS devices and graphene and 2D-material technology, devices and circuits.

Ana Rusu received degrees of MSc (1983) in Electronics and Telecommunications and PhD (1998) in Electronics. Since September 2001, she has been with KTH Royal Institute of Technology, Stockholm, Sweden, where she is Professor in Electronics Circuits for Integrated Systems. Her research interests spans from low/ultra-low power high performance CMOS circuits and systems for a wide range of applications to circuits using emerging technologies, such as graphene and SiC.