Explicit Drain Current, Charge and Capacitance Model of Graphene Field-Effect Transistors

David Jiménez

***Abstract*—This paper presents a compact physics-based model of the drain current, charge, and capacitance of graphene field-effect transistors, which is of relevance for the exploration of dc, ac, and transient behavior of graphene-based circuits. The physical framework is a field-effect model and drift-diffusion carrier transport incorporating saturation velocity effects. First, an explicit model has been derived for the drain current. Using it as a basis, explicit closed-form expressions for the charge and capacitances based on the Ward–Dutton partition scheme were derived, covering continuously all the operation regions. The model is of special interest for analog and radio-frequency applications where bandgap engineering of graphene is not needed.**

***Index Terms*—Analog, field-effect transistor (FET), graphene, modeling, radio frequency (RF).**

I. Introduction

GRAPHENE has emerged as a material of special interest to make nanoelectronic integrated circuits beyond silicon-based technology. This is due to remarkable electronic properties like high mobility ($\sim 10^5$ cm^2/V-s) and saturation velocity ($\sim 10^8$ cm/s), together with a promising ability to scale to short gate lengths and high speeds by virtue of its thinness. In addition, advances on the synthesis of large-scale graphene sheets of high quality and low cost using chemical vapor deposition (CVD) techniques are creating an appropriate framework for a new technology based on graphene to be introduced [1]. The main concern with graphene is the absence of a gap, which results in a poor ON–OFF current ratio, therefore limiting the usefulness of graphene in digital applications. However, zero gap graphene could still be very useful in analog and radio-frequency (RF) applications, where high ON/OFF current ratios are not required [2]. In small signal amplifiers, for instance, the transistor is operated in the ON-state, and small RF signals that are to be amplified are superimposed onto the dc gate–source voltage. Instead, what is needed to push the limits of many analog/RF figures of merit, for instance, the cutoff frequency or the intrinsic gain, is an operation region where high transconductance together with a small output conductance is accomplished. These conditions are realized for state-of-the-art graphene field-effect transistors (GFETs). Specifically, for large-area GFETs, the output characteristic shows a saturation-like behavior that could be exploited for analog/RF applications [3]. Recently, important progress for obtaining a saturated output characteristic has been made based on CVD graphene [4]. Using GFET technology, cutoff frequencies in the terahertz range are envisioned [5]. It is worth noting that cutoff frequencies in the range of hundreds of gigahertz have been demonstrated with a nonoptimized technology [1], [6], [7].

To boost the development of GFET technology, modeling of the electrical characteristics is essential to cover aspects as device design optimization, projection of performances, and exploration of analog/RF circuits, providing new or improved functionalities [8], [9].

Recently, an explicit compact model for the current–voltage (I–V) characteristics of GFET was proposed [9]. Taking this work as a basis, which provides the dc behavior, we further develop a compact physics-based model of the charge and capacitances of GFETs. This is necessary to address ac and transient simulations of graphene-based circuits. The physical framework is a field-effect model and drift-diffusion carrier transport with saturation velocity effects, which is accurate in explaining the I–V behavior of GFETs [3], [10]. Ward–Dutton's charge partition scheme provides the technique to model the terminal charges together with self-capacitances and transcapacitances of GFET [11]. Explicit closed-form expressions have been derived for these quantities continuously covering all operation regions. The model is intended to be the kernel to build up computer-aided design simulators of graphene-based circuits.

II. Drain Current Model

In this section, we present the drain current model, which provides the basis for both charge and capacitance models. More details can be found in [9]. Let us consider a dual-gate GFET with the cross-section depicted in Fig. 1. It consists of a graphene sheet playing the role of the active channel. The source and drain electrodes are contacting the graphene channel and are assumed to be ohmic. The electrostatic modulation of the carrier concentration in graphene is achieved via a double-gate stack consisting of top and bottom gate dielectrics and the corresponding metal gate. The source is grounded and considered the reference potential in the device.

The electrostatics of this device can be understood using the equivalent capacitive circuit depicted in Fig. 2 (see [10]). Here, C_t and C_b are the top and bottom oxide capacitances,

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The author is with the Departament d'Enginyeria Electrònica, Escola d'Enginyeria, Universitat Autònoma de Barcelona, 08193 Bellaterra, Spain (e-mail: david.jimenez@uab.es).

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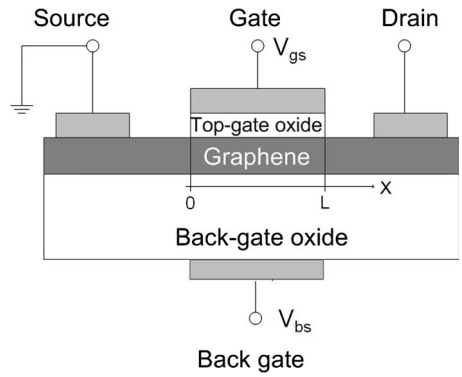

Fig. 1. Cross section of the dual-gate GFET.

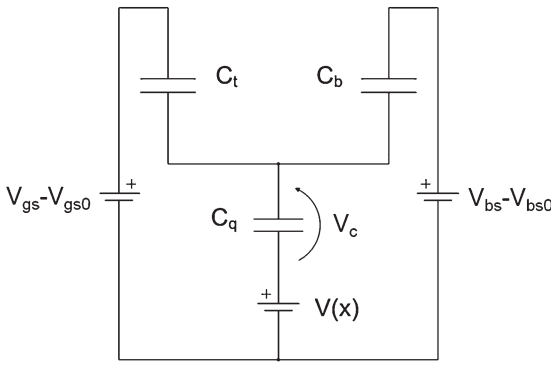

Fig. 2. Equivalent capacitive circuit of the dual-gate GFET.

and C_q represents the quantum capacitance of graphene. The potential V_c represents the voltage drop across C_q, and the relation between them is given by $C_q = k|V_c|$, where $k = (2q^2/\pi)(q/(\hbar v_F)^2)$, and $v_F (= 10^6$ m/s) is the Fermi velocity [12]. This expression is valid under the condition $qV_c \gg k_B T$. The potential $V(x)$ is the voltage drop in the graphene channel, which is zero at the source end $(x = 0)$ and equal to the drain–source voltage $V_{\rm ds}$ at the drain end $(x = L)$. Applying basic circuit laws to the equivalent capacitive network and noting that the overall net mobile sheet charge density in the graphene channel, which is defined as $Q_c = q(p - n)$, is equal to $-(1/2)C_q V_c$, the following relation can be obtained:

$$V_c(x) = (V_{\rm gs} - V_{\rm gs0} - V(x))\,\frac{C_t}{C_t + C_b + \frac{1}{2}C_q} + (V_{\rm bs} - V_{\rm bs0} - V(x))\,\frac{C_b}{C_t + C_b + \frac{1}{2}C_q} \quad (1)$$

where $V_{\rm gs} - V_{\rm gs0}$ and $V_{\rm bs} - V_{\rm bs0}$ are the top and back gate–source voltage overdrives, respectively. These quantities comprise work-function differences between the gates and the graphene channel, eventual charged interface states at the graphene/oxide interfaces, and intentional or unintentional doping of graphene.

To model the drain current of the GFET, a drift-diffusion transport is assumed under the form $I_{\rm ds} = -W|Q_c(x)|v(x)$, where W is the gate width, $|Q_c|$ is the free carrier sheet density in the channel at position x, and $v(x)$ is the carrier velocity. The absolute value of Q_c is taken because negative charged electrons and positive charged holes move in opposite directions under the electric field action, additively contributing to the drain current. Using a soft saturation model, consistent with Monte Carlo simulations [13], $v(x)$ can be expressed as $v = \mu E/(1 + \mu|E|/v_{\rm sat})$, where E is the electric field, μ is the carrier low-field mobility, and $v_{\rm sat}$ is the saturation velocity. We assume that the saturation velocity is pinned to the Fermi velocity $(v_{\rm sat} = v_F)$, greatly simplifying the algebra. A more refined model, relating the saturation velocity with the carrier density, could be considered instead [9]. Applying $E = -dV(x)/dx$, combining the foregoing expressions for v and $v_{\rm sat}$, and integrating the resulting equation over the device length, the drain current becomes

$$I_{\rm ds} = \frac{\mu W \int_0^{V_{\rm ds}} |Q_c| dV}{L + \mu \frac{|V_{\rm ds}|}{v_F}}. \quad (2)$$

The denominator represents an effective length $L_{\rm eff}$ that takes into account the saturation velocity effect. To get an explicit expression for the drain current, the integral in (2) is solved using V_c as the integration variable and consistently expressing Q_c as a function of V_c, i.e.,

$$I_{\rm ds} = \frac{\mu W \int_{V_{\rm cs}}^{V_{\rm cd}} |Q_c(V_c)| \frac{dV}{dV_c} dV_c}{L + \mu \frac{|V_{\rm ds}|}{v_F}}. \quad (3)$$

Here, V_c is obtained from (1) and can be written as (4), shown at the bottom of the page, where the positive (negative) sign applies when $(V_{\rm gs} - V_{\rm gs0} - V)C_t + (V_{\rm bs} - V_{\rm bs0} - V)C_b > 0 (< 0)$. The channel potential at the source $V_{\rm cs}$ is determined as $V_c(V = 0)$. Similarly, the channel potential at the drain $V_{\rm cd}$ is determined as $V_c(V = V_{\rm ds})$. Moreover, (1) provides the relation $dV/dV_c = -(1 + kV_c\,{\rm sgn}(V_c)/(C_t + C_b))$ entering in (3), where sgn refers to the sign function. On the other hand, the charge sheet density can be written as $|Q_c(V_c)| = kV_c^2/2$. Inserting these expressions into (3), the following explicit drain current expression can finally be obtained:

$$I_{\rm ds} = \frac{\mu k}{2}\frac{W}{L_{\rm eff}}\{g(V_c)\}_{V_{\rm cs}}^{V_{\rm cd}}$$
$$g(V_c) = \frac{-V_c^3}{3} - {\rm sgn}(V_c)\frac{kV_c^4}{4(C_t + C_b)}$$
$$L_{\rm eff} = L + \mu\frac{|V_{\rm ds}|}{v_F}. \quad (5)$$

Useful expressions for both transconductance $(g_m = (\partial I_{\rm ds}/\partial V_{\rm gs}))$ and output conductance $(g_{\rm ds} = (\partial I_{\rm ds}/\partial V_{\rm ds}))$ are given in the Appendix.

To test the proposed model, we have benchmarked the resulting I–V characteristics with experimental results

$$V_c = \frac{-(C_t + C_b) + \sqrt{(C_t + C_b)^2 \pm 2k\left[(V_{\rm gs} - V_{\rm gs0} - V)C_t + (V_{\rm bs} - V_{\rm bs0} - V)C_b\right]}}{\pm k} \quad (4)$$

extracted from the device in [14]. This is a top-gate device with $L = 10\ \mu$m, $W = 5\ \mu$m, and hafnium oxide as a dielectric with thickness of 40 nm. The flatband voltage was $V_{\rm gs0} = 0.85$ V according to the experiment. A low-field mobility of 7500 cm^2/V-s for both electrons and holes and source/drain resistance of 300 Ω provides a good fit with the experiment.

To reproduce any experimental current–voltage characteristics of GFETs, accounting of the voltage drop at the source/drain contacts is necessary. This quantity must be removed from the external applied bias $V_{\rm ds\_ext}$ to get the internal $V_{\rm ds}$. This is simply done by solving the equation $V_{\rm ds} = V_{\rm ds\_ext} - I_{\rm ds}(R_s + R_d)$, where R_s and R_d represent the source and drain contact resistances, respectively. Finally, note that $I_{\rm ds}$ is a function of $V_{\rm ds}$, as given by (5). Another effect, not considered here for the sake of simplicity, is the effect of R_s on $V_{\rm gs}$, namely, $V_{\rm gs} = V_{\rm gs\_ext} - I_{\rm ds}R_s$.

The resulting I–V characteristics are shown in Fig. 3. We have extended the analyzed drain–source voltage range beyond the experiment to show the predictive behavior of the model. The transfer characteristics exhibit the expected ambipolar behavior dominated by holes (electrons) below and above the Dirac gate voltage. The output characteristics show a saturation-like behavior with a second linear region. The agreement between the proposed model (solid lines) and the experiment (symbols) demonstrates its accuracy. A closer agreement can even be obtained using a more refined model given in [9] (dashed lines).

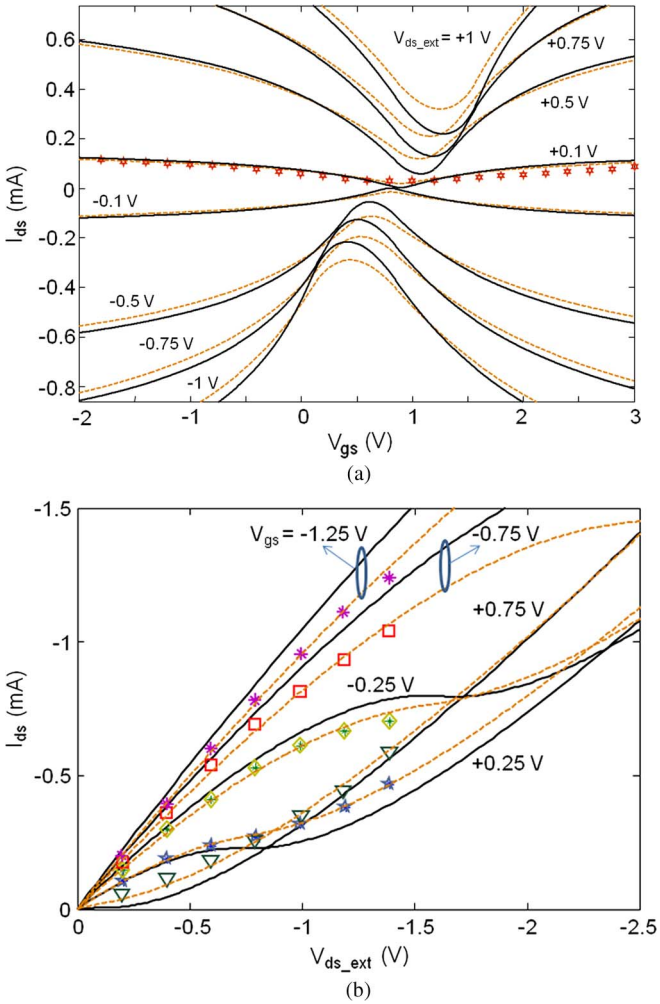

Fig. 3. (a) Transfer and (b) output characteristics obtained from the analytical model (solid lines) compared with the experimental results from [14] (symbols) and a more elaborated analytical model (dashed lines), which incorporates the effect of doping and a saturation velocity model that takes into account the carrier density (see [9]).

III. Charge Model

This section provides analytical and continuous expressions of charges associated with each terminal. To keep the complexity of the formulation within reasonable limits, a simplified case of a double-gate configuration with aligned top and gate electrodes has been considered, where the two gates are connected together. This allows considering the GFET as a three-terminal device, therefore making the analysis simpler. Extension to four-terminal devices could be done using the same principles outlined in this work.

The terminal charges Q_g, Q_d, and Q_s associated with the gate, drain, and source electrodes have to be considered. The gate charge can be computed by integrating the net mobile carrier concentration along the channel. On the other hand, the drain and source charges can be computed based on Ward–Dutton's linear charge partition scheme, which preserves the charge conservation [11], i.e.,

$$\begin{aligned} Q_g &= -W\int_0^L Q_c(x)dx \\ Q_d &= W\int_0^L \frac{x}{L}Q_c(x)dx \\ Q_s &= -(Q_g+Q_d). \end{aligned} \tag{6}$$

These expressions can conveniently be written using V_c as the integration variable, as it was done to model the drain current. There, the channel charge density is given by $Q_c(V_c) = -{\rm sgn(V_c)kV_c^2}/2$. A negative (positive) V_c means that the channel charge density is dominated by holes (electrons). Notice that the absolute value of the channel charge density, which is needed for drain current calculation, is absent here. As a consequence, integration of this quantity over the channel length could result in cancelation of the terminal charges. This situation physically would correspond to the appearance of pinchoff at some point in the channel. On the other hand, according to the current continuity equation, $dx = -\mu W|Q_c(x)|(dV/I_{\rm ds}(x))$, and x is equal to $L_{\rm eff}(g(V_{\rm cs}) - g(V_c))/(g(V_{\rm cd}) - g(V_{\rm cs}))$ based on the fact that the drain current is the same at any point x in the channel. Substituting Q_c, dx, and x into (6) allows integrals to be expressed as

$$\begin{aligned} Q_g &= -W\int_{V_{\rm cs}}^{V_{\rm cd}} Q_c(V_c)\left(\frac{-\mu W\,|Q_c(V_c)|}{I_{\rm ds}}\right)\frac{dV}{dV_c}dV_c \\ Q_d &= W\int_{V_{\rm cs}}^{V_{\rm cd}} \frac{1}{L}\left(\frac{L_{\rm eff}\,(g(V_{\rm cs})-g(V_c))}{g(V_{\rm cd})-g(V_{\rm cs})}\right) \\ &\quad\times\left(\frac{-\mu W\,|Q_c(V_c)|}{I_{\rm ds}}\right)Q_c(V_c)\frac{dV}{dV_c}dV_c. \end{aligned} \tag{7}$$

These integrals have been carried out to yield the charge model

$$Q_g = k\frac{WL_{\rm eff}}{2}\frac{\{f(V_c)\}_{V_{\rm cs}}^{V_{\rm cd}}}{\{g(V_c)\}_{V_{\rm cs}}^{V_{\rm cd}}}$$
$$Q_d = -k\frac{WL_{\rm eff}^2}{2L}\frac{g(V_{\rm cs})\{f(V_c)\}_{V_{\rm cs}}^{V_{\rm cd}} + \{m(V_c)\}_{V_{\rm cs}}^{V_{\rm cd}}}{\left[\{g(V_c)\}_{V_{\rm cs}}^{V_{\rm cd}}\right]^2}$$
$$Q_s = -(Q_g + Q_d) \tag{8}$$

where

$$f(V_c) = {\rm sgn(V_c)}\frac{\rm V_c^5}{5} + \frac{\rm kV_c^6}{6(C_t + C_b)}$$
$$m(V_c) = {\rm sgn(V_c)}\frac{\rm V_c^8}{24} + \frac{\rm 7kV_c^9}{108(C_t + C_b)} + {\rm sgn(V_c)}\frac{\rm k^2V_c^{10}}{40(C_t + C_b)^2}. \tag{9}$$

These expressions apply to a long-channel double-gate GFET incorporating saturation velocity effects, as given by (5).

IV. Capacitance Model

In this section, we present explicit expressions for the self-capacitances and transcapacitances of the GFET. For the three-terminal case under consideration, it results in nine nonreciprocal capacitances for transient or small-signal simulation. These are defined as

$$C_{\rm vw} = -\frac{\partial Q_v}{\partial V_w}\ v \neq w$$
$$C_{\rm vv} = \frac{\partial Q_v}{\partial V_v}\quad otherwise \tag{10}$$

where v and w stand for g, s, and d. Applying the charge conservation law, the following relation between capacitances can be obtained [15]:

$$C_{\rm ss} = C_{\rm sd} + C_{\rm sg} = C_{\rm ds} + C_{\rm gs}$$
$$C_{\rm gg} = C_{\rm gs} + C_{\rm gd} = C_{\rm sg} + C_{\rm dg}$$
$$C_{\rm dd} = C_{\rm ds} + C_{\rm dg} = C_{\rm sd} + C_{\rm gd}. \tag{11}$$

This relation leaves only four independent capacitances, namely, 1) $C_{\rm gd}$; 2) $C_{\rm dd}$; 3) $C_{\rm dg}$; and 4) $C_{\rm gg}$, which can be derived using the previous charge model given by (8) and (9), i.e.,

$$C_{\rm gg} = \frac{\partial Q_g}{\partial V_{\rm cd}} \times \frac{\partial V_{\rm cd}}{\partial V_g} + \frac{\partial Q_g}{\partial V_{\rm cs}} \times \frac{\partial V_{\rm cs}}{\partial V_g}$$
$$C_{\rm gd} = -\frac{\partial Q_g}{\partial V_{\rm cd}} \times \frac{\partial V_{\rm cd}}{\partial V_d}$$
$$C_{\rm dd} = \frac{\partial Q_d}{\partial V_{\rm cd}} \times \frac{\partial V_{\rm cd}}{\partial V_d}$$
$$C_{\rm dg} = -\frac{\partial Q_d}{\partial V_{\rm cd}} \times \frac{\partial V_{\rm cd}}{\partial V_g} - \frac{\partial Q_d}{\partial V_{\rm cs}} \times \frac{\partial V_{\rm cs}}{\partial V_g} \tag{12}$$

where we have (13) shown at the bottom of the next page. In the derivation of the capacitances, it should be noted that $\partial V_{\rm cd}/\partial V_s = \partial V_{\rm cs}/\partial V_d = 0$ because the voltage applied to the source has no control over the charge at drain, and vice versa [16].

V. Model Assessment With Discussion of the Operation Regions

To illustrate the model outcome, Fig. 4 shows the terminal charges and capacitances for the examined device [14] as a function of $V_{\rm gs}$, where $V_{\rm ds}$ has been fixed ($= -0.5$ V). An insight of the terminal charge evolution can be obtained by looking at the quantities $V_{\rm cs}$ and $V_{\rm cd}$, informing of the type of carriers that dominate at the source and drain end, respectively. The examined case corresponds to $V_{\rm cd} > V_{\rm cs}$ whatever is the $V_{\rm gs}$ value. With regard to the n-type or p-type character of the channel, three different situations can be distinguished depending on the gate voltage, as follows:

1) Hole channel ($V_{\rm gs} < V_{\rm gs,p-off-d}$), where $V_{\rm gs,p-off-d} = V_{\rm ds} + V_{\rm gs0}$ ($= 0.35$ V) labels the gate voltage that exactly places the pinchoff point at $x = L$ [Fig. 4(b)]. In this region, the channel is entirely p-type because both $V_{\rm cs}$, $V_{\rm cd} < 0$. As a consequence, both Q_g, $Q_d > 0$, as can be observed in Fig. 4(a).
2) Ambipolar channel ($V_{\rm gs,p-off-d} < V_{\rm gs} < V_{\rm gs,p-off-s}$), where $V_{\rm gs,p-off-s} = V_{\rm gs0} (= 0.85$ V) labels the gate voltage that places the pinchoff point at $x = 0$. In this region, the channel has a mixed character, being p-type at the source end and n-type close to the drain end, respectively, consistent with $V_{\rm cs} < 0$ and $V_{\rm cd} > 0$. At some specific $V_{{\rm gs},D} = V_{\rm gs0} + V_{\rm ds}/2 (= 0.65$ V), belonging to this interval, the condition $V_{\rm cs} = -V_{\rm cd}$ is satisfied, shifting the pinchoff point to $x = L/2$. For this particular gate voltage, which is named Dirac voltage, electron and hole charges are exactly balanced over the channel length, resulting in $Q_g = 0$. Note, however, that Q_d goes across zero at $V_{\rm gs}$ slightly smaller than $V_{{\rm gs},D}$. The reason being that Q_d, defined from Ward–Dutton's linear charge partition scheme, weights the carriers at the drain side (electrons) more than carriers at the source side (holes).
3) Electron channel ($V_{\rm gs} > V_{\rm gs,p-off-s}$). In this region, the channel is entirely n-type because both $V_{\rm cs}$, $V_{\rm cd} > 0$, consistent with the quantities Q_g, $Q_d < 0$.

It is worth noting that if the selected $V_{\rm ds}$ results in $V_{\rm cs} > V_{\rm cd}$, the operation regions would be instead 1) hole channel ($V_{\rm gs} < V_{\rm gs,p-off-s}$); 2) ambipolar channel ($V_{\rm gs,p-off-s} < V_{\rm gs} < V_{\rm gs,p-off-d}$); and 3) electron channel ($V_{\rm gs} > V_{\rm gs,p-off-d}$).

Next, the capacitances of the GFET under test [Fig. 4(c)] are examined. Interestingly, the self-capacitance $-C_{\rm gg}$ is symmetric around the Dirac voltage, where a maximum value arises. It also presents two local minimum at $V_{\rm gs,p-off-d}$ and $V_{\rm gs,p-off-s}$, respectively. The transcapacitances $-C_{\rm sg}$ and $C_{\rm dg}$ show a similar behavior, although the curves are slightly asymmetric due to the position-dependent weighting of the mobile charge in Ward–Dutton's partition scheme. Moreover, the position of the maximum is slightly shifted respect to the Dirac voltage. On the other hand, the capacitances $C_{\rm sd}$,

$-C_{\rm gd}$, and $C_{\rm dd}$ $(-C_{\rm ss}, -C_{\rm gs}, -C_{\rm ds})$ exhibit a zero value at $V_{\rm gs,p-off-d}$ $(V_{\rm gs,p-off-s})$ and a maximum at around $V_{{\rm gs},D}$. The appearance of singular points can be related with screening effects. For instance, let us discuss the transcapacitance $C_{\rm gs}$. The minimum appears when the channel is pinched off at the source side. In this situation, communication between the gate and the source is cut off, and Q_g is not affected by the variation of V_s. A similar effect occurs for the observed minimum in $C_{\rm gd}$. Here, the channel is pinched off at the drain side, precluding the communication between the gate and the drain, which results in a Q_g not affected by the variation of V_d. The maximum in both $C_{\rm gs}$ and $C_{\rm gd}$ occurs at the Dirac point, once the channel is exactly partitioned into n-type and p-type halves, resulting in minimum screening between the gate and source/drain terminals, respectively.

Next, I examine the terminal charges and capacitances as a function of $V_{\rm ds}$ for a fixed $V_{\rm gs}(=-0.25$ V) (see Fig. 5). In this case, $V_{\rm cs}$ is constant (<0), and different operation regions appear driven by $V_{\rm cd}$. Two different channel types are then possible according to the drain voltage, as follows:

1) Ambipolar channel $(V_{\rm ds} < V_{\rm ds,p-off-d})$, where $V_{\rm ds,p-off-d} = V_{\rm gs} - V_{\rm gs0}(=-1.1$ V) labels the drain voltage that places the pinchoff point at $x = L$. In this region, the channel has a mixed p-type and n-type character at the source and drain ends, respectively, consistent with $V_{\rm cs} < 0$ and $V_{\rm cd} > 0$. On the other hand, $Q_g < 0$ as long as $V_{\rm ds} < V_{{\rm ds},D}$, where $V_{{\rm ds},D} = 2\ V_{\rm ds,p-off-d}(=-2.2$ V) is the drain voltage that places the pinchoff just in the middle of the channel $(x = {\rm L}/2)$, where the relation $V_{\rm cs} = -V_{\rm cd}$ is fulfilled. Regarding the drain current, this is roughly linear with $V_{\rm ds}$. This region is named as second linear region. As long as $V_{\rm ds}$ approaches $V_{\rm ds,p-off-d}$, the

$$
\begin{aligned}
\frac{\partial Q_g}{\partial V_{\rm cd}} &= k\frac{WL_{\rm eff}}{2}\left\{\frac{-g'(V_{\rm cd})\left\{f(V_c)\right\}_{V_{\rm cs}}^{V_{\rm cd}}}{\left[\left\{g(V_c)\right\}_{V_{\rm cs}}^{V_{\rm cd}}\right]^2} + \frac{h(V_{\rm cd})}{\left\{g(V_c)\right\}_{V_{\rm cs}}^{V_{\rm cd}}}\right\}\\
\frac{\partial Q_g}{\partial V_{\rm cs}} &= k\frac{WL_{\rm eff}}{2}\left\{\frac{g'(V_{\rm cs})\left\{f(V_c)\right\}_{V_{\rm cs}}^{V_{\rm cd}}}{\left[\left\{g(V_c)\right\}_{V_{\rm cs}}^{V_{\rm cd}}\right]^2} - \frac{h(V_{\rm cs})}{\left\{g(V_c)\right\}_{V_{\rm cs}}^{V_{\rm cd}}}\right\}\\
\frac{\partial Q_d}{\partial V_{\rm cd}} &= -k\frac{WL_{\rm eff}^2}{2L}\left\{\frac{-2g'(V_{\rm cd})}{\left[\left\{g(V_c)\right\}_{V_{\rm cs}}^{V_{\rm cd}}\right]^3}\left(g(V_{\rm cs})\left\{f(V_c)\right\}_{V_{\rm cs}}^{V_{\rm cd}} + \left\{m(V_c)\right\}_{V_{\rm cs}}^{V_{\rm cd}}\right)\right.\\
&\qquad\left. + \frac{1}{\left[\left\{g(V_c)\right\}_{V_{\rm cs}}^{V_{\rm cd}}\right]^2}\left(g(V_{\rm cs})h(V_{\rm cd}) + n(V_{\rm cd})\right)\right\}\\
\frac{\partial Q_d}{\partial V_{\rm cs}} &= -k\frac{WL_{\rm eff}^2}{2L}\left\{\frac{2g'(V_{\rm cs})}{\left[\left\{g(V_c)\right\}_{V_{\rm cs}}^{V_{\rm cd}}\right]^3}\left(g(V_{\rm cs})\left\{f(V_c)\right\}_{V_{\rm cs}}^{V_{\rm cd}} + \left\{m(V_c)\right\}_{V_{\rm cs}}^{V_{\rm cd}}\right)\right.\\
&\qquad\left. + \frac{1}{\left[\left\{g(V_c)\right\}_{V_{\rm cs}}^{V_{\rm cd}}\right]^2}\left(g'(V_{\rm cs})\left\{f(V_c)\right\}_{V_{\rm cs}}^{V_{\rm cd}} - g(V_{\rm cs})h(V_{\rm cs}) - n(V_{\rm cs})\right)\right\}\\
\frac{\partial V_{\rm cd}}{\partial V_g} &= -\frac{\partial V_{\rm cd}}{\partial V_d} = \left(1 + {\rm sgn(V_{cd})}\frac{\rm kV_{cd}}{\rm C_t + C_b}\right)^{-1}\\
\frac{\partial V_{\rm cs}}{\partial V_g} &= \left(1 + {\rm sgn(V_{cs})}\frac{\rm kV_{cs}}{\rm C_t + C_b}\right)^{-1}\\
g'(V_c) &= -V_c^2 - {\rm sgn(V_c)}\frac{\rm kV_c^3}{\rm C_t + C_b}\\
h(V_c) &= {\rm sgn(V_c)V_c^4} + \frac{\rm kV_c^5}{\rm C_t + C_b}\\
n(V_c) &= {\rm sgn(V_c)}\frac{\rm V_c^7}{3} + \frac{\rm 7kV_c^8}{\rm 12(C_t + C_b)} + {\rm sgn(V_c)}\frac{\rm k^2V_c^9}{\rm 4(C_t + C_b)^2}
\end{aligned}
\tag{13}
$$

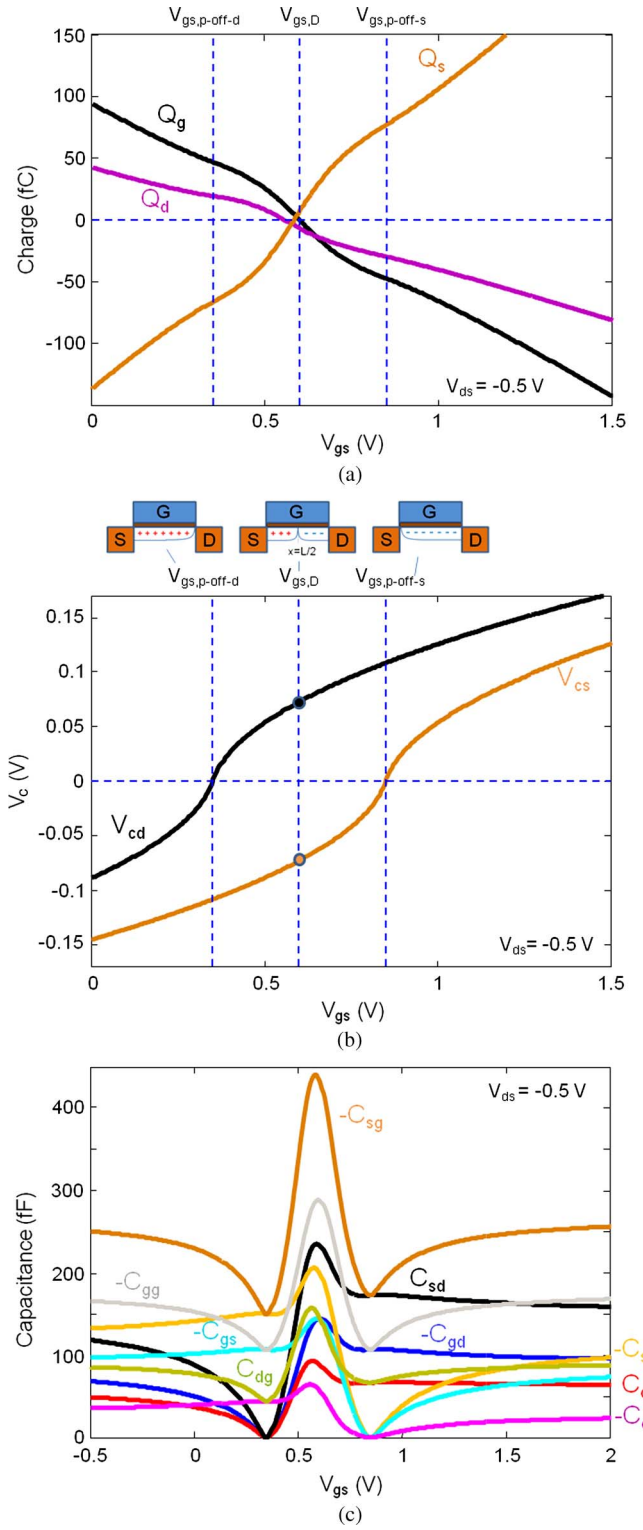

Fig. 4. (a) Terminal charges, (b) channel voltage drop, and (c) capacitances for the examined device as a function of gate voltage. The channel is shown to be p-type, mixed p and n-type, or p-type, depending on the gate voltage.

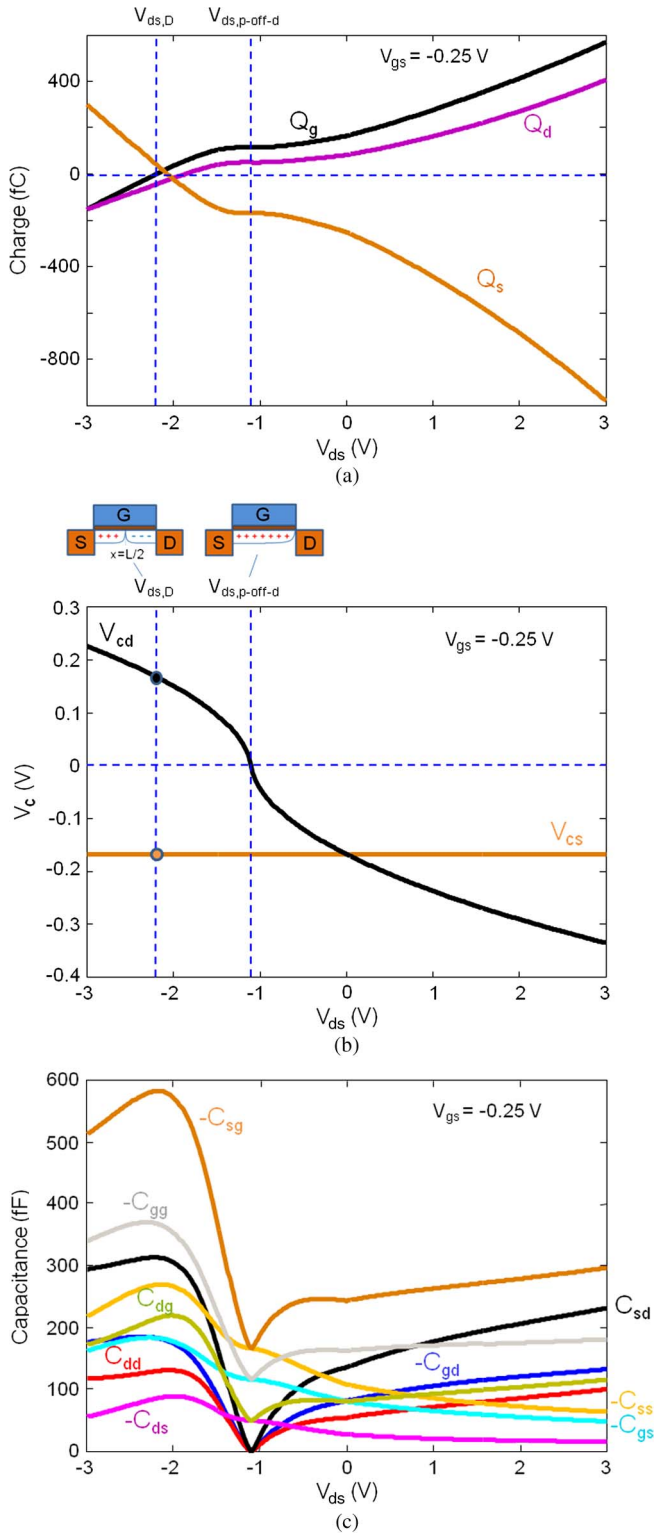

Fig. 5. (a) Terminal charges, (b) channel voltage drop, and (c) capacitances for the examined device as a function of drain voltage. The channel is shown to be mixed p and n type, or p-type, depending on the drain voltage.

output characteristics get saturated. This behavior can be observed in the GFET output characteristics of the device under test in Fig. 3(b). Note that $V_{\mathrm{ds\_ext}}$ has been considered as the independent variable for plotting this figure, being different from V_{ds}; the later meaning the internal drain–source voltage.

2) Hole channel $(V_{\mathrm{ds}} > V_{\mathrm{ds,p-off-d}})$. In this region, the channel is entirely p-type, consistent with V_{cs}, $V_{\mathrm{cd}} < 0$ and Q_g, $Q_d > 0$. For this particular range of V_{ds}, the output characteristic is linear with V_{ds}, and it is named as first linear region.

It is worth noting that if the selected $V_{\rm gs}$ results in $V_{\rm cs} > 0$, the operation regions would be instead 1) electron channel ($V_{\rm ds} < V_{\rm ds,p-off-d}$) and 2) ambipolar channel ($V_{\rm ds} > V_{\rm ds,p-off-d}$).

The capacitances $C_{\rm sd}$, $-C_{\rm gd}$, and $C_{\rm dd}$ as a function of $V_{\rm ds}$ show a maximum of around $V_{{\rm ds},D}$ and a minimum zero capacitance at $V_{\rm ds,p-off-d}$, where all the terminal charges Q_s, Q_g, and Q_d get saturated [Fig. 5(b) and (c)].

VI. Conclusion

In conclusion, this paper has presented an explicit and compact drain current, charge and capacitance model for GFETs based on a field-effect model and drift-diffusion carrier transport, including saturation velocity effects. The model captures the physics of all operation regions within a single expression for the drain current and each terminal charge and capacitance. It is of special interest as a tool for the design of analog and RF applications [17]. Additional physical effects as, for example, short-channel effects, nonquasi-static effects, extrinsic capacitances [5], and mobility model [3], [18], need to be incorporated into the long-channel core presented here to build a complete GFET compact model.

Appendix

In this section, useful expressions for both g_m and $g_{\rm ds}$ are provided as follows:

$$g_m = \frac{\partial I_{\rm ds}}{\partial V_{\rm gs}} = \frac{\partial I_{\rm ds}}{\partial V_{\rm cd}} \times \frac{\partial V_{\rm cd}}{\partial V_{\rm gs}} + \frac{\partial I_{\rm ds}}{\partial V_{\rm cs}} \times \frac{\partial V_{\rm cs}}{\partial V_{\rm gs}}$$
$$= \frac{\mu k}{2} \frac{W}{L_{\rm eff}} \left(\frac{g'(V_{\rm cd})}{1+{\rm sgn(V_{cd})}\frac{\rm kV_{cd}}{\rm C_t+C_b}} - \frac{g'(V_{\rm cs})}{1+{\rm sgn(V_{cs})}\frac{\rm kV_{cs}}{\rm C_t+C_b}} \right) \quad \text{(A1)}$$

$$g_{\rm ds} = \frac{\partial I_{\rm ds}}{\partial V_{\rm ds}} = \frac{\partial I_{\rm ds}}{\partial V_{\rm cd}} \times \frac{\partial V_{\rm cd}}{\partial V_{\rm ds}} + \frac{\partial I_{\rm ds}}{\partial V_{\rm cs}} \times \frac{\partial V_{\rm cs}}{\partial V_{\rm ds}}$$
$$= -\frac{\mu k}{2} \frac{W}{L_{\rm eff}} \frac{g'(V_{\rm cd})}{1+{\rm sgn(V_{cd})}\frac{\rm kV_{cd}}{\rm C_t+C_b}}. \quad \text{(A2)}$$

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David Jiménez received the Ph.D. degree in electronics engineering from the Universitat Autònoma de Barcelona, Barcelona, Spain, in 2000.

In 2002, he was a Visiting Researcher with the Universidad Autónoma de Madrid, Madrid, Spain; in 2003, with the Universitat Rovira i Virgili, Tarragona, Spain; in 2009, with the Tokyo Institute of Technology, Tokyo, Japan; and in 2010, with the Universidad de Granada, Granada, Spain and the École Polytechnique Fédérale de Lausanne, Lausanne, Switzerland. Since 2004, he has been an Associate Professor with the Departament d'Enginyeria Electrónica, Universitat Autónoma de Barcelona. His research interests include the compact modeling of nanoscale transistors, including multiple-gate MOSFETs, silicon nanowire transistors, and carbon-based transistors. His recent research interests include the research of new transistor architectures based on materials that exhibit negative capacitance and memristance.