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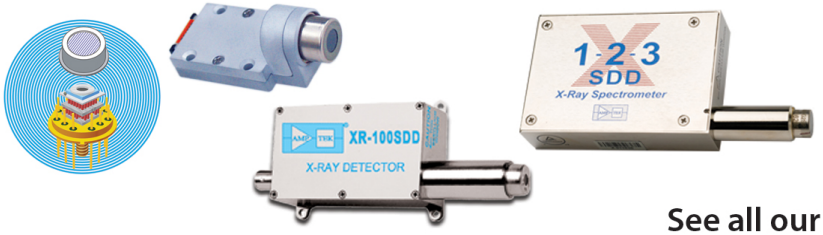

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Modeling of graphene metal-oxide-semiconductor field-effect transistors with gapless large-area graphene channels

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A quasianalytical modeling approach for graphene metal-oxide-semiconductor field-effect transistors (MOSFETs) with gapless large-area graphene channels is presented. The model allows the calculation of the *I-V* characteristics, the small-signal behavior, and the cutoff frequency of graphene MOSFETs. It applies a correct formulation of the density of states in large-area graphene to calculate the carrier-density-dependent quantum capacitance, a steady-state velocity-field characteristics with soft saturation to describe the carrier transport, and takes the source/drain series resistances into account. The modeled drain currents and transconductances show very good agreement with experimental data taken from the literature {Meric *et al.*, [Nat. Nanotechnol. **3**, 654 (2008)] and Kedzierski *et al.*, [IEEE Electron Device Lett. **30**, 745 (2009)]}. In particular, the model properly reproduces the peculiar saturation behavior of graphene MOSFETs with gapless channels.
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I. INTRODUCTION

Graphene is a new carbon-based, purely two-dimensional material discovered only six years ago.[1,2] It shows a multitude of fascinating properties and the prospect of ultrahigh carrier mobilities exceeding those of the conventional semiconductors.[1,3–5] This has motivated intensive work focused on the development of graphene metal-oxide-semiconductor field-effect transistors (MOSFETs).[6–12]

Since large-area graphene has no band gap, graphene MOSFETs with large-area graphene channels do not switch off and are not suited for logic applications. For radio frequency (rf) transistors, on the other hand, complete switch off is not mandatory. Recently, rf graphene MOSFETs with large-area graphene channels showing cutoff frequencies f_T in the Gigahertz range have been realized[10–12] and a record f_T of 100 GHz has been reported for a 240-nm gate transistor.[10] If graphene is narrowed into slender graphene nanoribbon (GNRs), a sizeable band gap opens.[13,14] Graphene MOSFETs with GNR channels showing complete switch off and large on-off rations have been demonstrated[7,15] and are considered as a possible building block for future logic circuits. In the following, the abbreviation GFET will be used for graphene MOSFETs with gapless large-area graphene channel, while graphene MOSFETs with semiconducting GNR channels will be designated as GNR MOSFETs.

The first experimental GFETs did show either no saturation of the drain current at all or only very weak saturation. Only since late 2008, GFETs with saturated output characteristics have been reported.[8,9] However, the saturation of these transistors is peculiar since it shows a kinklike feature, i.e., an inflection point followed by a subsequent increase in the current at high drain voltages. A phenomenological explanation for this behavior has been proposed in Ref. 8. Recently the importance of a pronounced drain current saturation for the frequency performance of FETs has been discussed and by qualitative arguments it has been shown that this type of saturation behavior observed for GFETs in Refs. 8 and 9 is not desirable since it limits the transistor's rf performance.[16]

While extensive theoretical studies on the dc characteristics of GNR FETs have been published, e.g,[17–19] there is only a few reports on the modeling and simulation of the dc behavior of GFETs. In Ref. 20 the drain currents of GFETs in the ballistic limit have been simulated using the nonequilibrium Green's function formalism and in Ref. 8 the *I-V* characteristics of GFETs have been calculated using a quasianalytical approach.

The aim of the present paper is to derive a model for GFETs that properly reproduces the peculiar saturation behavior and that allows the modeling of the small-signal behavior and the cutoff frequency of these transistors. The ideas formulated in Refs. 8 and 12 serve as the starting point of the model derivation. It should be noted that the focus of the present paper is the development of a suitable modeling framework while a quantitative assessment of GFET performance limits is beyond the scope of this work.

The paper is organized as follows. In Sec. II, the theory do describe the dc behavior of GFETs is presented and Sec. III deals with the modeling of the small-signal parameters and the cutoff frequency. Modeling results are presented and compared with experimental data in Sec. IV and finally Sec. V concludes the paper.

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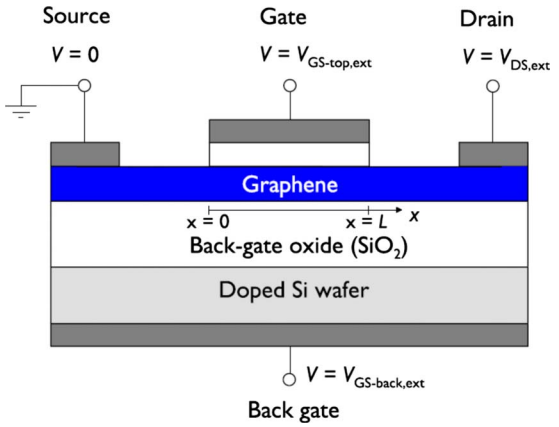

FIG. 1. (Color online) Cross section of the model GFET. The voltages $V_{GS\text{-}top,ext}$, $V_{DS,ext}$, and $V_{GS\text{-}back,ext}$ are the external, i.e., terminal, top-gate-source, drain-source, and backgate-source voltages. The corresponding internal voltages (not shown in the Fig.) are $V_{GS\text{-}top}$, V_{DS}, and $V_{GS\text{-}back}$.

II. GFET DC MODEL

A. Model transistor

In the following we focus on *p*-channel GFETs, but an analogous approach applies to *n*-channel transistors as well. Figure 1 shows the cross-section of our model transistor. It consists of a large-area graphene channel located on a thick SiO_2 layer that is grown on a heavily doped Si wafer. The SiO_2 serves as the backgate dielectric and the Si wafer acts as backgate. By applying a constant backgate voltage, the conductivity type of the channel can be adjusted. The ohmic source/drain contacts and the top-gate stack consisting of the top-gate dielectric and the gate with length L are located on top of the graphene channel. The source is grounded and the zero source potential serves as the reference potential in the device.

In general, the drain current I_D of a field-effect transistor can be expressed as

$$I_D = -q\rho_{sh}(x)v(x)W = -q\rho_{sh}[V(x)]v[V(x)]W, \tag{1}$$

where q is the elementary charge, $\rho_{sh}(x)$ the free carrier sheet density in the channel at position x, $v(x)$ the carrier drift velocity, and W the gate width. To each position x in the channel belongs a certain local potential $V(x)$. Therefore, the x dependence of ρ_{sh} and v can be translated into a $V(x)$ dependence as shown on the right-hand-side of Eq. (1).

B. Calculation of the carrier sheet density and quantum capacitance

Graphene behaves differently compared to the channel materials of conventional MOSFETs in several respects. Therefore, in the following the calculation of the carrier sheet density in a graphene MOS channel including the quantum capacitance is presented in detail. It is known from general MOS theory that the gate capacitance (per unit area) C_G of a MOS structure with a semiconductor having a finite density of states (DOS) cannot be described properly by the oxide capacitance C_{ox} alone:

$$C_G \neq C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}, \tag{2}$$

where ε_{ox} and t_{ox} are the dielectric constant and the thickness of the gate oxide. Instead, the gate capacitance has to be considered as a series connection of the oxide capacitance, the quantum capacitance C_q accounting for the limited DOS, and a capacitance C_{th} taking the finite (nonzero) thickness of the mobile sheet charge in the semiconductor into account.[21] Thanks to the purely two-dimensional nature of graphene, the capacitance C_{th} can be neglected for graphene MOS structures. It is important, however, to take the effect of the quantum capacitance into account properly.[22,23] Therefore, we consider the gate capacitance as the series connection of C_{ox} and C_q and the voltage drop across C_G as the sum of the voltage drops across C_{ox} and across C_q. The voltage across C_q is called V_{ch} in the following.

First, expressions for the hole and electron sheet densities in graphene MOS structures with only one gate on top, i.e., without a backgate, are established. Large-area graphene shows a linear dispersion relation around the K point of the Brillouin zone that can be written as[22]

$$E(K) - E_{CV} = E(k) = s\hbar v_F|k|, \tag{3}$$

where E is the energy, s is 1 in the conduction band and -1 in the valence band, $\hbar$ the reduced Planck constant, v_F the Fermi velocity equal to 10^8 cm/s, and k is the wave vector (measured from the K point). Due to the zero band gap the conduction band minimum E_C and the valence band maximum E_V coincide, i.e., $E_C = E_V = E_{CV}$. In ideal undoped and unbiased graphene the Fermi level E_F is located at E_{CV}. Thus, any variation in the Fermi level by an applied gate voltage is equivalent to the voltage drop across C_q, i.e., $E_F - E_{CV} = q \times V_{ch}$.

The number of available states N in k space is given by

$$N = g_S g_D \frac{\pi k^2}{(2\pi/L)^2} = \frac{g_S g_D A k^2}{4\pi} = \frac{g_S g_D A}{4\pi}\left(\frac{E - E_{CV}}{\hbar v_F}\right)^2, \tag{4}$$

where g_S and g_D are the spin and valley degeneracy factors, and $A = L^2$ is the graphene area in real space. Using Eq. (4), with $g_S = g_D = 2$, the DOS per unit area $D(E)$ for graphene is obtained as

$$D(E) = \frac{1}{A}\frac{dN}{dE} = \frac{2}{\pi}\frac{|E - E_{CV}|}{(\hbar v_F)^2}. \tag{5}$$

The next step is to derive expressions for the gate voltage dependence of the hole and electron sheet densities in the graphene channel. The hole sheet density is given by

$$p = \int_{-\infty}^{E_{CV}} D(E)[1 - f(E)]dE, \tag{6}$$

where $f(E)$ is the Fermi–Dirac distribution. It can be shown that using $D(E)$ from Eq. (5) and the usual expression for $f(E)$, and changing the integration limits, Eq. (6) becomes

$$p = \int_{-\infty}^{E_{CV}} \frac{2}{\pi} \frac{|E - E_{CV}|}{(\hbar v_F)^2} [1 - f(E)] dE$$

$$= \int_{-E_{CV}}^{\infty} \frac{2}{\pi} \frac{E + E_{CV}}{(\hbar v_F)^2} \frac{1}{\exp\left(\frac{E + E_F}{k_B T}\right) + 1} dE. \quad (7)$$

Using E_{CV} as reference energy (i.e., $E_{CV}=0$ and $E_F = q \times V_{ch}$) we get

$$p = \frac{2}{\pi(\hbar v_F)^2} \int_0^{\infty} \frac{E}{\exp\left(\frac{E + E_F}{k_B T}\right) + 1} dE. \quad (8)$$

A similar expression can be derived for the electron sheet density in graphene. The overall net mobile sheet charge density Q_{sh} in the graphene channel is simply the difference between the hole and electron sheet densities multiplied by the elementary charge, i.e., $Q_{sh} = q \times (p - n)$:

$$Q_{sh} = q \frac{2}{\pi(\hbar v_F)^2} \int_0^{\infty} E \left[\frac{1}{\exp\left(\frac{E + E_F}{k_B T}\right) + 1} - \frac{1}{\exp\left(\frac{E - E_F}{k_B T}\right) + 1} \right] dE. \quad (9)$$

An approach to calculate the quantum capacitance for graphene MOS structures has been presented in Ref. 22. Following the treatment from Ref. 22, the quantum capacitance is defined as the derivative of the net channel sheet charge density Q_{sh} with respect to V_{ch}

$$C_q = -\frac{d Q_{sh}}{d V_{ch}}. \quad (10)$$

The minus sign stems from the fact that a more positive gate voltage results in a more positive channel voltage and thus leads to a more negative charge in the graphene. Taking the derivative and carrying out some algebraic manipulations one arrives at[22]

$$C_q = \frac{2q^2 k_B T}{\pi(\hbar v_F)^2} \ln\left[2\left(1 + \cosh\frac{q V_{ch}}{k_B T}\right)\right]. \quad (11)$$

Under the condition $q \times V_{ch} \gg k_B T$ this expression can be simplified to[22]

$$C_q = \frac{2q^2}{\pi} \frac{q|V_{ch}|}{(\hbar v_F)^2}. \quad (12)$$

Equation (12), together with Eq. (10), leads to the useful expression

$$Q_{sh} = -\int C_q dV_{ch} = -\frac{1}{2} C_q V_{ch}. \quad (13)$$

Note that Q_{sh} is not equal to $-C_q V_{ch}$ as one would expect for a classical plate capacitor but only half of it due to the specific dependence of C_q on V_{ch} as shown in Eq. (12).

Now the model is applied to a transistor having both top-gate and backgate. To this end the oxide capacitance of the backgate oxide, $C_{ox\text{-}back}$, is added and a capacitive network consisting of C_q, $C_{ox\text{-}back}$, and $C_{ox\text{-}top}$ as shown in the equivalent circuit in Fig. 2 is to be considered. Here, $V(x)$ is the voltage drop in the graphene channel. It is zero at $x=0$ and equal to the drain-source voltage V_{DS} at $x=L$.

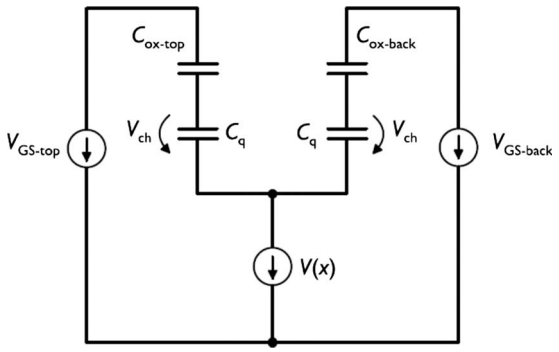

FIG. 2. Equivalent capacitive circuit of a GFET with both top-gate and backgate. $C_{ox\text{-}top}$ and $C_{ox\text{-}back}$ are the oxide capacitances of the two gates. Note that the voltages $V_{GS\text{-}top}$ and $V_{GS\text{-}back}$ refer to the internal voltages.

Applying Kirchhoff's laws to the equivalent circuit from Fig. 2, the following equation connecting V_{ch}, $V(x)$, and the top-gate and backgate voltages $V_{GS\text{-}top}$ and $V_{GS\text{-}back}$ is obtained

$$V_{ch} = [V_{GS\text{-}top} - V(x)] \frac{C_{ox\text{-}top}}{C_{ox\text{-}top} + C_{ox\text{-}back} + \frac{1}{2} C_q} + [V_{GS\text{-}back} - V(x)] \frac{C_{ox\text{-}back}}{C_{ox\text{-}top} + C_{ox\text{-}back} + \frac{1}{2} C_q} \quad (14)$$

Note the prefactor 1/2 of C_q those results from Eq. (13). Since C_q is not constant but depends on V_{ch}, Eqs. (12) and (14) have to be solved self-consistently. The solution provides the values for C_q and V_{ch}. Using Eq. (13), we finally get the carrier sheet density as

$$q\rho_{sh} = Q_{sh} = \left|-\tfrac{1}{2} C_q V_{ch}\right|, \quad (15)$$

which will be needed for the calculation of the drain current.

So far the fact that the gate and the graphene channel may possess different work functions has been neglected. This work function difference, together with possibly existing charged interface states at the graphene/oxide interfaces and an intentional or unintentional doping of the graphene contribute to the potential conditions and to the carrier sheet densities in the graphene channel. This is taken into account by replacing $V_{GS\text{-}top}$ in Eq. (14) by the effective top-gate-source voltage $V_{GS\text{-}top,eff}$ given by

$$V_{GS\text{-}top,eff} = V_{GS\text{-}top} - V_{GS\text{-}top0}, \quad (16)$$

where $V_{GS\text{-}top0}$ is the top-gate voltage at the Dirac point (where the carrier sheet density becomes minimal) for zero applied backgate and drain-source voltages. Similarly, for the backgate a voltage $V_{GS\text{-}back0}$ is introduced. The role of $V_{GS\text{-}top0}$ and $V_{GS\text{-}back0}$ is similar to that of the flatband voltage in a conventional Si MOS structure. Finally, there is always a minimum sheet carrier concentration ρ_{sh0} caused by disorder

and thermal excitation in a graphene channel that has to be added to ρ_{sh}.[8,24]

C. Calculation of the drain current

For the calculation of the drain current we go back to Eq. (1) and now focus on the carrier velocity $v=v(x)$. Monte Carlo simulations have shown that the steady-state velocity-field characteristics of graphene shows a soft saturation[25–27] that can be approximated by the expression

$$v = \frac{\mu\mathcal{E}}{1+\frac{\mu|\mathcal{E}|}{v_{sat}}}, \tag{17}$$

where $\mathcal{E}$ is the electric field, μ is the carrier low-field mobility, and v_{sat} is the saturation velocity. In a graphene channel located on SiO_2 the maximum carrier velocity, i.e., the saturation velocity, is strongly affected by remote interfacial phonon scattering.[3,28] It has been shown that mainly the two surface optical phonons of SiO_2 with energies of 59 and 155 meV are involved in this process. With sufficient accuracy, the phenomenon can be described by only one phonon with an effective energy $\hbar\Omega$.[3] This approach has been used in Ref. 8 to derive an expression for the saturation velocity which depends on this effective energy and therefore also on the sheet carrier density ρ_{sh}

$$v_{sat} = \frac{\Omega}{\sqrt{\pi\rho_{sh}}}, \tag{18}$$

Meric *et al.*[12] suggested that the effect of carrier-phonon interactions in GFET channels is overestimated by Eq. (18) and introduced a correction term. We follow this approach by introducing a correction term $A\times V^2(x)$ and model the saturation velocity by

$$v_{sat} = \frac{\Omega}{(\pi\rho_{sh})^{0.5+AV^2(x)}}. \tag{19}$$

Note that Eq. (19) is a correlation equation providing v_{sat} in cm/s when ρ_{sh} is used in cm^{-2}, $V(x)$ in V, and A as a dimensionless empirical factor of the order of 10^{-3}.

Applying $\mathcal{E}=-dV(x)/dx$ and combining Eqs. (19), (17), and (1), the drain current becomes

$$I_D = -q\rho_{sh}\frac{\mu(-dV/dx)}{1+\frac{\mu(-dV/dx)}{v_{sat}}}W, \tag{20}$$

where $V=V(x)$. Solving this equation by the separation of variables, integrating the left-hand-side over x from $x=0$ to $x=L$, and the right-hand-side over $V(x)$ from $V(0)=0$ to $V(L)=V_{DS}$ results in the final expression of the drain current:

$$I_D = q\mu W\frac{\int_0^{V_{DS}}\rho_{sh}dV}{L-\mu\int_0^{V_{DS}}\frac{1}{v_{sat}}dV}. \tag{21}$$

As a last step, the source/drain series resistances are taken into account by relating the external terminal voltages $V_{DS,ext}$, $V_{GS\text{-}top,ext}$, and $V_{GS\text{-}back,ext}$ to the corresponding internal voltages V_{DS}, $V_{GS\text{-}top}$, and $V_{GS\text{-}back}$.

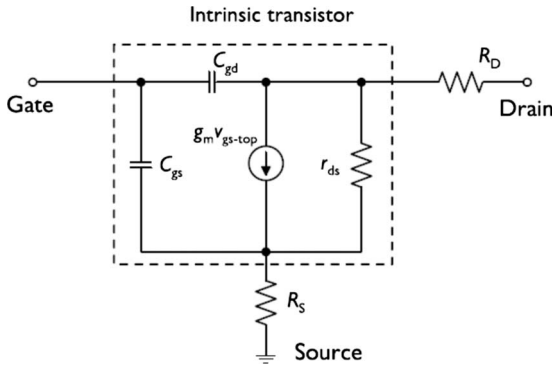

FIG. 3. Small-signal equivalent circuit of a GFET.

III. GFET SMALL-SIGNAL AND RF MODEL

The small-signal and rf behavior of GFETs can be modeled by a small-signal equivalent circuit commonly used for rf FETs as shown in Fig. 3.[29] The intrinsic transistor is described by the transconductance g_m, the drain conductance g_{ds}, the gate-source capacitance C_{gs}, and the gate-drain capacitance C_{gd}.

The transconductance is defined as the variation in the drain current caused by a small variation in the top-gate voltage $V_{GS\text{-}top}$ as

$$g_m = \left.\frac{dI_D}{dV_{GS\text{-}top}}\right|_{V_{DS}=const.}. \tag{22}$$

The drain conductance is the inverse of the differential drain resistance r_{ds} from Fig. 3 and is defined as the variation in I_D caused by a small variation in V_{DS} given by

$$g_{ds} = \frac{1}{r_{ds}} = \left.\frac{dI_D}{dV_{DS}}\right|_{V_{GS\text{-}top}=const.}. \tag{23}$$

The mobile channel charge depends on the top-gate and drain-source voltages $V_{GS\text{-}top}$ and V_{DS}. This dependence is modeled by the gate-source capacitance C_{gs} and the gate-drain capacitance C_{gd} defined as

$$C_{gs} = -\left.\frac{dQ_{ch}}{dV_{GS\text{-}top}}\right|_{V_{DS}=const.}, \tag{24}$$

and

$$C_{gd} = -\left.\frac{dQ_{ch}}{dV_{DS}}\right|_{V_{GS\text{-}top}=const.}. \tag{25}$$

The overall net channel charge is calculated by

$$Q_{ch} = qW\int_0^L [p(x)-n(x)]dx. \tag{26}$$

The x dependence of the local hole and electron sheet densities can be translated into a dependence on the local voltage $V(x)$. Using

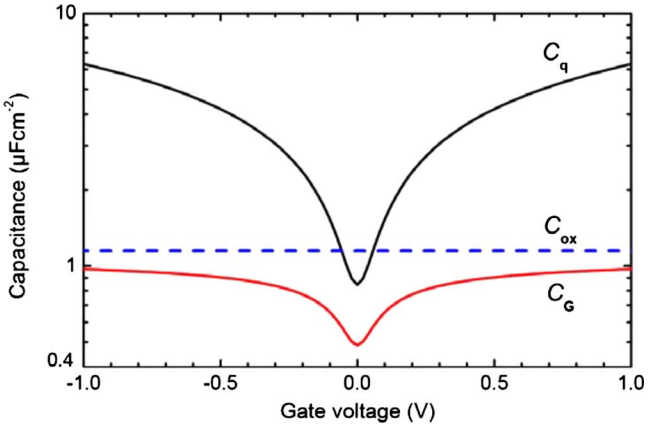

FIG. 4. (Color online) Gate capacitance C_G, quantum capacitance C_q, and oxide capacitance C_{ox} of a graphene MOS structure as a function of gate voltage.

$$\frac{dx}{dV} = \frac{q\rho_{sh}\mu W}{I_D} + \frac{\mu}{v_{sat}}, \tag{27}$$

obtained from Eq. (20), the overall net channel charge can be expressed as

$$Q_{ch} = qW\int_0^{V_{DS}} (p-n)\left(\frac{q\rho_{sh}\mu W}{I_D} + \frac{\mu}{v_{sat}}\right)dV. \tag{28}$$

Note that in Eqs. (22)–(28) the internal voltages have to be used. Finally, with the help of the equivalent circuit from Fig. 3 the cutoff frequency f_T of the GFET can be calculated as[30,31]

$$f_T = \frac{g_m}{2\pi\{(C_{gs}+C_{gd})[1+g_{ds}(R_S+R_D)]+C_{gd}g_m(R_S+R_D)\}}. \tag{29}$$

IV. RESULTS

First we investigate the effect of the quantum capacitance on the overall gate capacitance. To this end, a simplified graphene MOS structure without backgate, a 3-nm SiO_2 top-gate dielectric, zero $V_{GS\text{-}top0}$, and zero applied V_{DS} is considered. Figure 4 shows the calculated overall gate capacitance given by $C_G = C_{ox} \times C_q/(C_{ox}+C_q)$, the quantum capacitance C_q, and the oxide capacitance C_{ox} as a function of gate voltage. In the voltage range shown the quantum capacitance varies by a factor 7.5 and the overall gate capacitance by a

TABLE I. Dimensions and parameters of the modeled GFET1 and GFET2 from Figs. 5(a) and 5(c).

	GFET1	GFET2
$L(\mu m)$	1	10
$W(\mu m)$	2.1	5
$t_{ox\text{-}top}$(nm)	15	40
$t_{ox\text{-}back}$(nm)	285	⋯
$V_{GS\text{-}top0}$(V)	1.45	0.95
$V_{GS\text{-}back0}$(V)	2.7	⋯
$\rho_{sh0}(cm^{-2})$	1.5×10^{12}	3×10^{11}
$R_S=R_D(\Omega)$	900	320
$\mu_p(cm^2/V\,s)$	1500	6500
$\mu_n(cm^2/V\,s)$	1500	6500
$\hbar\Omega$(meV)	55	99
$V_{GS\text{-}back,ext}$(V)	−40	⋯

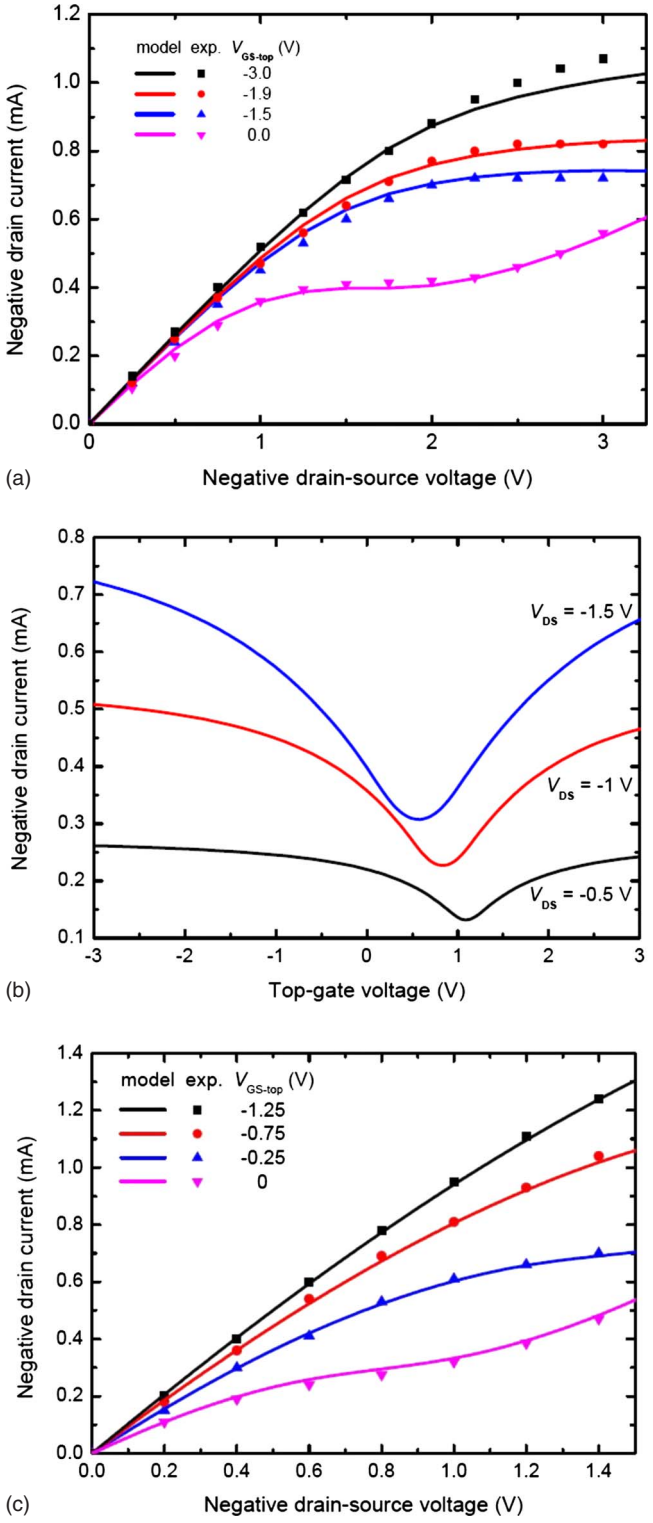

FIG. 5. (Color online) (a) Modeled output characteristics of GFET1 (lines) and comparison with experimental data from Ref. 8 (symbols). (b) Modeled transfer characteristics of GFET1. (c) Modeled output characteristics of GFET2 (lines) and comparison with experimental data from Ref. 9 (symbols).

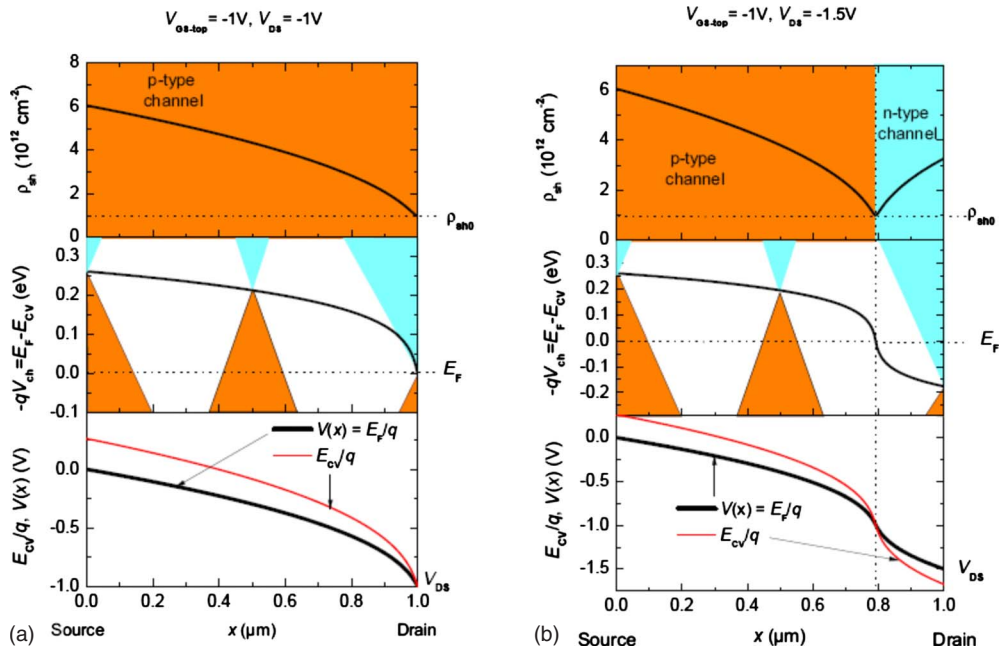

FIG. 6. (Color online) Conditions in the channel of a GFET. (a) Conditions at the inflection point of the output characteristics occurring for $V_{GS\text{-}top}=V_{DS}=-1$ V. The entire channel shows *p*-type conduction. (b) Conditions for $V_{GS\text{-}top}=-1$ V and $V_{DS}=-1.5$ V, i.e., beyond the inflection point. Near drain the conduction type of the channel changes from *p*-type to *n*-type.

factor of two. This shows that a correct treatment of the quantum capacitance including its voltage dependence is important for an accurate modeling of GFETs.

Next the GFET reported in Ref. 8 is considered. This transistor is called GFET1 and features an exfoliated graphene channel, an HfO_2 top gate dielectric (relative dielectric constant $\varepsilon_r=16$), and a SiO_2 backgate dielectric. Table I summarizes the GFET dimensions and the parameters used for the modeling.

Figure 5(a) shows the modeled output characteristics for this transistor. For −40 V applied backgate voltage the transistor behaves as a *p*-channel FET. The comparison of our modeled output characteristics with the experimental results from Ref. 8 shows an excellent agreement. Merely for large (absolute) values of the applied top-gate and drain-source voltages the modeled currents are slightly below the experimental data. Figure 5(b) shows the calculated transfer characteristics. It can be seen that the Dirac point shifts when the drain-source voltage is varied. Such a shift is observed in experimental GFETs as well.[32,33] The output characteristics from Fig. 5(a) deserve a closer inspection. While in the shown V_{DS} range the upper three curves for $V_{GS\text{-}top}=-3$, −1.9, and −1.5 V seemingly have a shape as known from conventional FETs, i.e., a linear region followed by a saturation of the drain current, the curve for $V_{GS\text{-}top}=0$ V shows a kinklike shape with an inflection point around 1.7 V, followed by a subsequent increase in I_D (like a "second" linear region). It should be noted that at higher drain-source voltages the *I-V* curves for more negative gate voltages also show an inflection point. Meric *et al.*[8] have attributed this behavior to a change in the conduction type at the drain end of the channel from *p*-type to *n*-type.

In the following, this peculiar behavior is discussed in more detail. To this end, we have simulated a simplified GFET structure having no backgate, zero series resistances, and a zero $V_{GS\text{-}top0}$, while the remaining parameters are those from Table I. Figure 6 shows the conditions in the channel for two different drain voltages of −1 and −1.5 V.

Let us start the discussion for an applied $V_{GS\text{-}top}=-1$ V and zero V_{DS}. Then the hole concentration is constant at any position in the channel and no current is flowing. If we gradually vary V_{DS} to −1 V, an increasing current flows and the hole concentration at $x=L$ decreases for increasing absolute V_{DS}. At $V_{DS}=-1$ V the Fermi level at the source end of the channel ($x=0$) is at 0 eV and at the drain end ($x=L$) it is shifted downwards by 1 eV due to V_{DS}. Thus, the local gate-to-channel voltage is −1 V at $x=0$ and zero at $x=L$ as shown in Fig. 6(a). The bottom of the conduction band is shifted upwards by V_{ch} with respect to E_F at the source end of the channel, which results in a *p*-type (i.e., hole) conduction. At $x=L$, the bottom of the conduction band is located just at E_F—this corresponds to the Dirac condition, i.e., zero gate-induced carriers in the graphene and $\rho_{sh}=\rho_{sh0}$. We are now at the inflection point of the I_D-V_{DS} characteristics.

If V_{DS} is further decreased to −1.5 V, see Fig. 6(b), we will obtain a positive gate-to-channel voltage of +0.5 V at $x=L$. This gives rise to an accumulation of electrons and a corresponding increase in the carrier density leading to a further increase in the current. Now the majority charge carriers are holes at the source end of the channel and electrons at the drain end. In other words, ambipolar conduction occurs and the conductivity type of the channel changes between source and drain. Such a behavior is specific for GFETs, caused by the gapless nature of the channel, and does not occur in conventional field-effect transistors.

In order to demonstrate that our model is not tailored for a specific transistor but is capable to reproduce the *I-V* characteristics of GFETs in general, we have modeled the output

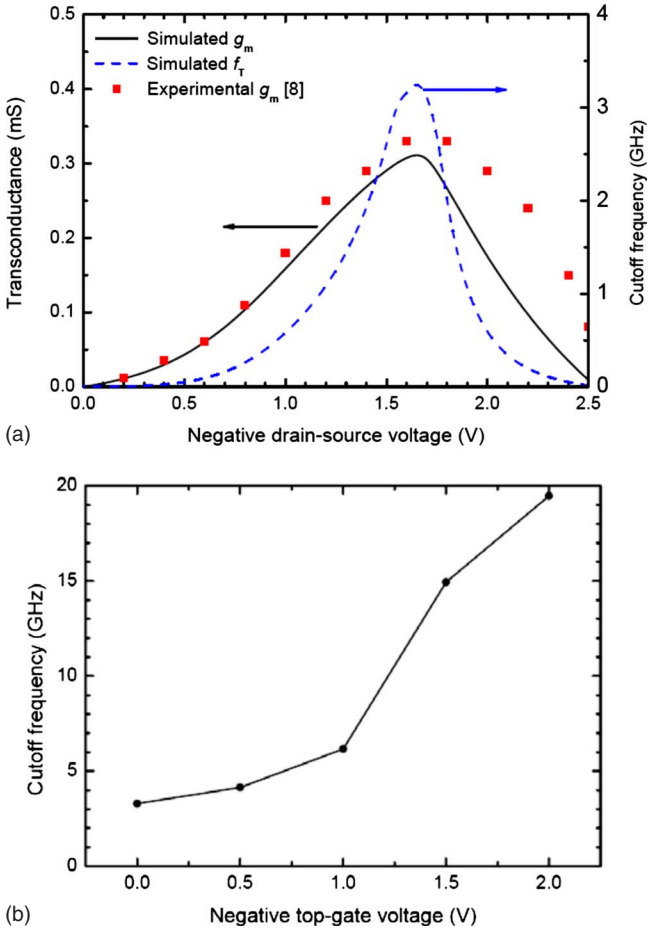

FIG. 7. (Color online) (a) Modeled and measured transconductance of GFET1 from Table I as a function of drain-source voltage for zero applied top-gate voltage. The experimental g_m data are taken from Ref. 8. Also shown is the simulated cutoff frequency. (b) Simulated peak f_T vs applied top-gate voltage. Note that the modeled peak f_T is shown for the top-gate voltage range where the drain voltage for the onset of the second linear regime could be verified by the experimental data from Ref. 8.

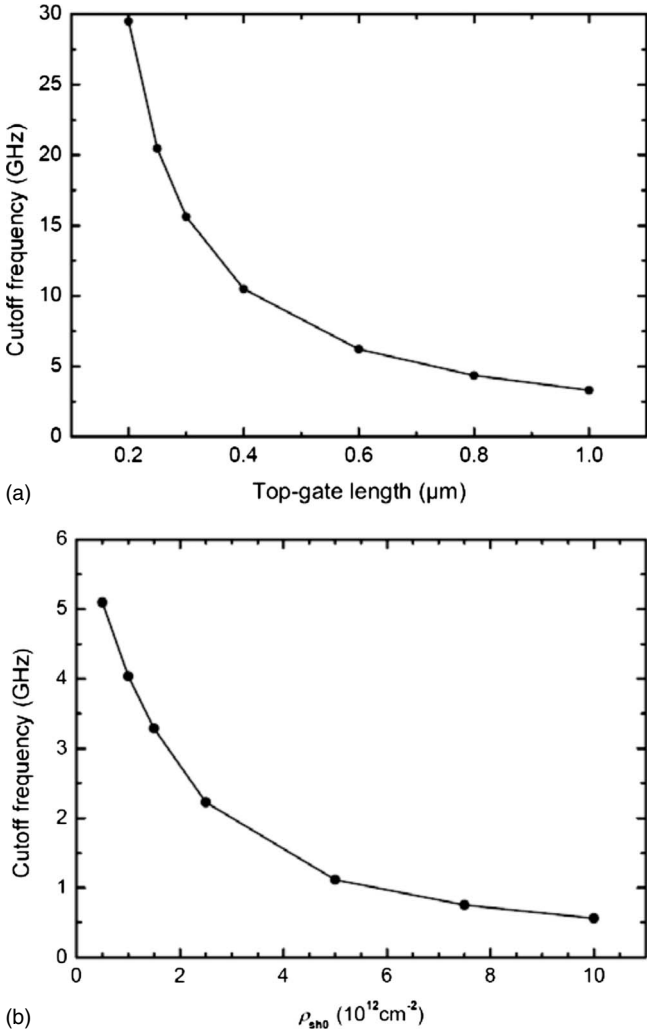

FIG. 8. Calculated dependence of the cutoff frequency of GFET1 from Table I for zero applied top-gate voltage (a) on the gate length and (b) on the residual carrier sheet density.

characteristic of a completely different GFET that was presented in Ref. 9. This transistor we call GFET2 was made by transferring graphene grown on Ni onto SiO_2. The output characteristics of this GFET have been calculated using the parameters from Table I and show also a very good agreement with experimental data, see Fig. 5(c).

We now come back to the GFET1 from Table I. The modeled transconductance versus drain-source voltage characteristics of this transistor, together with experimental data from,[8] are shown in Fig. 7(a). The important features of the experimental curves, i.e., the peak g_m of 0.3 mS at -1.7 V drain-source voltage and the absence of a g_m plateau as usually found for conventional transistors, are reproduced properly by the model. Also shown is the modeled cutoff frequency. As expected from Eq. (29), the trend of f_T qualitatively follows that of the transconductance. The peak f_T is 3 GHz and occurs at $V_{DS}=1.7$ V, i.e., at the inflection point of the output characteristics. Since for the transistor under consideration zero $V_{GS\text{-}top}$ is not the optimum bias condition for high f_T, in Fig. 7(b) the peak f_T of the GFET is shown as a function of $V_{GS\text{-}top}$. The peak f_T increases for more negative $V_{GS\text{-}top}$ and reaches almost 20 GHz for $V_{GS\text{-}top}=-2$ V.

Finally, the effects of the gate length L, residual carrier sheet density ρ_{sh0}, mobility μ, and series resistances on the cutoff frequency are investigated. Figure 8 shows the modeled cutoff frequency of GFET1 from Table I as a function of gate length and residual carrier sheet density. The calculations have been carried out exemplarily for zero $V_{GS\text{-}top}$. As expected, shorter gates cause significantly enhanced cutoff frequencies. Shortening the gate from 1 to 0.2 μm leads to an increase in f_T by one order of magnitude. Interestingly, the residual carrier density has also a sizeable effect on f_T. Decreasing ρ_{sh0} by a factor of 10 from 10^{13} to 10^{12} cm^{-2} causes an increase in f_T again by a factor of almost 10.

Calculations assuming varying mobility and series resistances resulted, as expected, in increased cutoff frequencies for enhanced mobilities and decreased series resistances. It should be noted that the f_T's in Fig. 8 have been calculated for zero $V_{GS\text{-}top}$ which is not the optimum gate bias. The trends observed in Fig. 8, however, are representative.

V. CONCLUSION

A model for the calculation of the dc and small-signal behavior of GFETs has been presented. The model is an ex-

tension of the approach proposed in Refs. 8 and 12. Most importantly, we have included a correct modeling of the quantum capacitance and the channel charge, and have developed a framework for the modeling of the small-signal behavior of GFETs. Using the new model, the *I-V* characteristics, the small-signal parameters, and the cutoff frequency of GFETs have been calculated. The modeled output characteristics show very good agreement with experimental data and reproduce the peculiar saturation behavior of GFETs properly. Based on the new dc model, the elements of the small-signal equivalent circuit and the cutoff frequency of GFETs have been calculated. We found that the cutoff frequency plotted versus the drain-source voltage shows a narrow peak that coincides with the inflection point of the output characteristics. The f_T-V_{DS} dependence of the investigated GFET is different from conventional field-effect transistors such as Si MOSFETs and III–V high electron mobility transistors that usually show a wide plateau of f_T in the saturation region. The peculiar saturation behavior of GFETs leads to the situation that they cannot exploit their inherent speed potential effectively. The rise of f_T abruptly diminishes for drain voltages beyond the inflection point of the output characteristics due to the decreasing transconductance and increasing drain conductance. This effect seriously limits the speed performance of GFETs. On the other hand it has been shown that by reducing the gate length, the residual carrier sheet concentration, and series resistances, as well as by increasing the mobility significant improvements of the cutoff frequency are possible.

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